Development of a Laboratory Readout System for DEPFET Pixel Detector Modules and Investigation of Radiation Backgrounds at the SuperKEKB Accelerator

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Abstract

With the upgrade from the e^+e^--collider KEKB to SuperKEKB, a 40-fold increase in instantaneous luminosity is targeted posing new challenges for the Belle II detector. Particularly the innermost detector layers, consisting of a silicon strip and Depleted *P*-channel Field-Effect Transistor (DEPFET) based pixel detector, operate in an environment of high event rates and increased background radiation.

In the first part of this thesis, the measurements of the FANGS detector are presented, which was one of five dedicated background monitors for the commissioning phase BEAST II of the SuperKEKB accelerator. Consisting of ATLAS hybrid pixel detector modules, the detector is suitable for studies under high radiation and particle rate especially caused by synchrotron radiation. The benefit of highly segmented sensors enables the spatial measurement of radiation present close to the interaction point. Furthermore, the capability of energy resolution using a precise charge measurement method is demonstrated.

The second part deals with the development of the BDAQ-PXD readout system for single DEPFET pixel detector modules which are successfully operated in the innermost layers of Belle II. BDAQ-PXD is intended to be an easily accessible and adjustable laboratory test system for irradiation and test beam environments using the custom designed BDAQ53 readout board. The implementations of FPGA firmware, software and first measurements are presented. Within the scope of this work, the DEPFET sensor properties are investigated, e.g. hit-detection efficiencies and the influence of biasing voltages on charge collection. Specifically, a hit-detection efficiency of above 99.7 % is measured confirming the functionality of the BDAQ-PXD system.

Contents

1 Introduction

The fundamental question concerning the constituents of our universe drives humankind to develop new theories and technologies to answer it. The most accurate description of the fundamental constituents of matter, called elementary particles, and their interactions between each other is provided by the Standard Model (SM) of particle physics. However, the SM reaches its limits in describing some observed phenomena, shifting the focus towards new theories describing them. For probing the SM and searching for physics beyond it, high-energy particle experiments use particle collisions to observe rare physics processes. The demand for collisions at high rates and energies requires particle accelerators as well as large detectors capable of measuring the collision products.

One of these facilities is the electron-positron collider SuperKEKB, operated by the research organisation KEK[1] located in Tsukuba, Japan. Compared to the Large Hadron Collider (LHC), which operates at the energy frontier and searches for new physics at high-energy collisions, SuperKEKB tackles the intensity frontier and sets a new record for particle collision rates. The collider delivers frequent particle productions and decays with a targeted design luminosity of $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ for precise measurements of their properties. SuperKEKB is an upgrade of the KEKB collider and its luminosity is successively increased up to a factor of 40 with respect to the predecessor. The Belle II experiment at SuperKEKB is a multi-purpose detector for the complex task of measuring particle properties such as trajectory, momentum, energy and type. Due to the large particle currents and number of collisions, the collision products are accompanied by a significant amount of noise. This increases the requirements on the detectors to discern the signal from the noise and withstand the strain of continuous irradiation.

Therefore, the first part of this thesis focuses on one of the most prevalent sources of noise in precise measurements, namely background radiation. For the commissioning of the SuperKEKB accelerator, specialised detectors were deployed forming the BEAST II experiment to examine the beam-induced background radiation and to support the tuning of the accelerator. The FE-I4 ATLAS Near Gamma Sensor (FANGS) detector is especially suited to monitor particle rates in high radiation environments and therefore a crucial part of a complementary beam monitor. During commissioning, FANGS recorded particle rates, 2 D hit information and energy. The detailed description of the implementation, installation, performance studies and dedicated measurements is covered in this thesis.

The newly developed Pixel Detector (PXD) of the Belle II experiment, which is the innermost

[1] engl.: High Energy Accelerator Research Organisation

sub-detector located only a few mm from the collision point, has the challenge of reconstructing particle tracks originating from the collisions in an environment of high particle densities and background radiation. The PXD is based on the Depleted P-channel Field-Effect Transistor (DEPFET) technology operating successfully in Belle II.

To enable customisable laboratory operation of the PXD modules (DEPFET modules), a new Field-Programmable Gate Array (FPGA)-based readout system, called BDAQ-PXD, was developed as part of this thesis. Built for the characterisation of single modules, the system is capable of configuring, reading out and operating DEPFET modules in laboratory conditions. The functionality and operation of the DEPFET module using the BDAQ-PXD system are demonstrated with an electron beam measurement at the DESY test beam facility.

The thesis is structured as follows: Chap. 2 introduces the SuperKEKB accelerator together with the Belle II detector and accelerator beam backgrounds. In Chap. 3, the properties of the semiconductor silicon as a sensor material are described. Furthermore, two detector implementations are presented, i.e. hybrid pixel detectors and DEPFET sensors, which are used in this work. The BEAST II experiment used to commission the accelerator using the FANGS detector is discussed in Chap. 4. For the investigation of beam-induced background radiation, the whole process from installation to analysis of the recorded data is presented.

The pixel detector of the Belle II experiment is described in detail in Chap. 5 with focus on the design, readout electronics implementation and functioning of the DEPFET modules. Chap. 6 focuses on the newly developed readout system BDAQ-PXD with its individual hardware components and the implementation details of firmware and software. The applicability of the system is demonstrated through the configuration process and measurements of particles from a radioactive source. In Chap. 7, the hit-detection efficiency of the detector is measured in a test beam campaign. Furthermore, causes for possible inefficiency are investigated. In conclusion, a summary of the results is given in Chap. 8, followed by a brief outlook.

2 The Belle II experiment at SuperKEKB

The SuperKEKB accelerator and the Belle II detector located at the KEK National High Energy Physics Research Centre in Tsukuba, Japan, are focused on the continuation of the search for physics beyond the Standard Model. Both originate from an upgrade of the KEKB accelerator and the Belle detector, which provided the data for the validation of *CP*-violating processes in the B-meson (b-flavoured meson) system [Abe+01]. The *CP*-violating process was first proposed by M. Kobayashi and T. Maskawa in 1973 [KM73] and used in 1981 to predict a large *CP* violation in certain B-meson decays [BS81]. In *B-factories* designed for the production and measurement of B mesons, such as the KEKB accelerator with the Belle detector, *CP* violation was confirmed and M. Kobayashi and T. Maskawa were awarded the Nobel Prize in 2008 [Bro+12, p. 3].
The goal of SuperKEKB is to push the intensity frontier of high-energy particle physics even further and achieve a 40-fold increase in the luminosity compared to its predecessor. This chapter provides a detailed description of the SuperKEKB accelerator and Belle II detector which have been providing collisions and recording data since *March 11, 2019*.

2.1 The SuperKEKB accelerator

SuperKEKB is an electron-positron collider operating with asymmetric beam energies and tailored for the production of B mesons. At a centre-of-mass energy of 10.58 GeV, it operates at the $\Upsilon(4S)$ resonance which decays almost exclusively to a B-meson pair with a probability of more than 96 % [Zyl+20, p. 1812]. The aim is to gain insight into B-meson decays and to observe rare decays. A schematic drawing of SuperKEKB is shown in Fig. 2.1.
In two separate rings, namely the High Energy Ring (HER) and the Low Energy Ring (LER), electrons and positrons are accelerated to an energy of 7 GeV and 4 GeV, respectively. A 600 m-long Linear accelerator (Linac) consists of 60 accelerating units in order to inject electrons and positrons into the SuperKEKB main ring [AFK18, p. 13]. In addition, a 1.1 GeV damping ring improves the beam quality by reducing the emittance of the positron beam [Ike+19, p. 29]. Electrons and positrons move clockwise and counter-clockwise in the HER and LER, respectively, before they collide at the Interaction Point (IP). The IP is enclosed by the Belle II detector which is described in Sec. 2.2. The instantaneous luminosity for a circular collider with beam

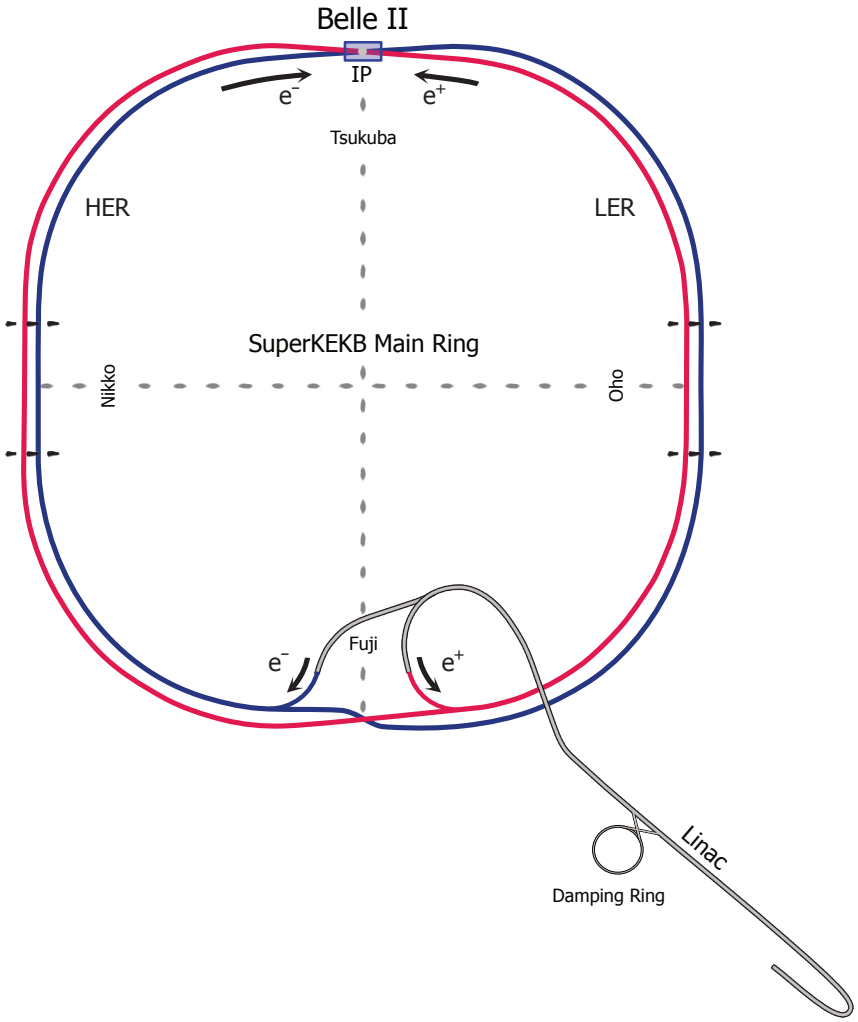


Figure 2.1: Drawing of the SuperKEKB main ring. Electrons and positrons are injected into the HER and LER, respectively. At an energy of 7 GeV (HER) and 4 GeV (LER), they collide at the Interaction Point (IP). The Belle II detector encloses the IP. Adapted from [Ish+20, p. 2].

currents $I_\pm$ for electrons and positrons is given by [AFK18, p. 2]:

$$\mathcal{L} = \frac{\gamma_\pm}{2er_e}\left(1+\frac{\sigma_y^*}{\sigma_x^*}\right)\left(\frac{I_\pm \xi_{y\pm}}{\beta_y^*}\right)\left(\frac{R_L}{R_{\xi_y}}\right), \tag{2.1}$$

with the Lorentz factors $\gamma_\pm$, the elementary charge e, the classical electron radius r_e and the horizontal and vertical beam size at the IP, σ_x^* and σ_y^* (assuming Gaussian profiles). The beam currents $I_\pm$, the vertical beam-beam parameters $\xi_{y\pm}$ and the vertical beta function at the IP β_y^* are the main machine parameters which were influenced by the upgrade. The parameters R_L and R_{ξ_y} are geometrical factors and form a correction term. Some of the most important

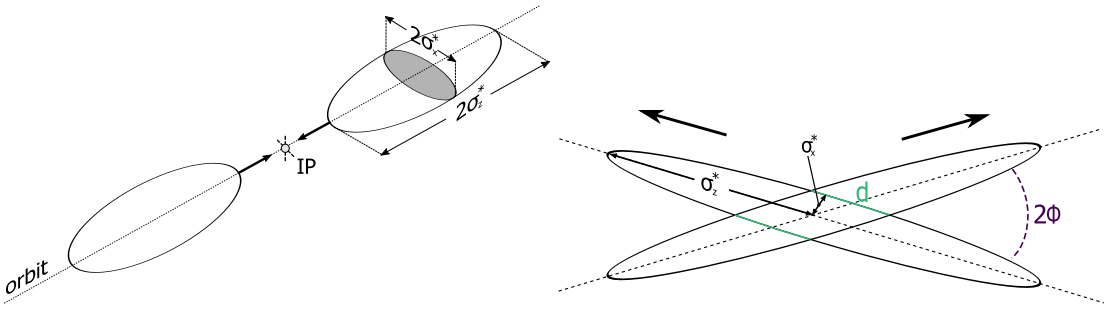
changes resulting from the upgrade are listed in Tab. 2.1.
By reducing the vertical beta function at the IP (β_y^*) to 1/20 of the design value of KEKB, the instantaneous luminosity of SuperKEKB is expected to be 40 times higher [AFK18, p. 2]. To achieve the reduction of β_y^*, a new final-focusing magnet system (QCS) was developed and implemented [Ohu+22]. The QCS system includes eight quadrupole magnets, 43 corrector magnets and four compensation solenoid coils focussing the two particle beams from HER and LER to the desired values [Ohu+22, p. 3]. The reduction of vertical beam sizes is described in Sec. 2.1.1.

		KEKB		SuperKEKB	
Parameters		LER	HER	LER	HER
Beam energy	E /GeV	3.5	8.0	4.0	7.0
Beam current	$I_\pm$ /A	1.64	1.19	3.60	2.60
Vertical beta function at IP	β_y^* /mm	5.90	5.90	0.27	0.30
Beam-beam parameter	$\xi_{y\pm}$	0.129	0.090	0.088	0.081
Instantaneous luminosity	$\mathcal{L}$ /cm^{-2}s^{-1}	2.108×10^{34}		8×10^{35}	

Table 2.1: Selection of machine parameters during the operation of KEKB and design values of SuperKEKB. From [AFK18, p. 4].

2.1.1 Nano-beam scheme

The essential difference of SuperKEKB to KEKB is the reduction of the overlap region of both beams at the IP allowing for a compression of the vertical beta function β_y^*. This technique is referred to as *nano-beam scheme* and was first proposed in [RSZ07]. Fig. 2.2 illustrates the approach for head-on collisions compared to a larger crossing angle 2ϕ in the nano-beam scheme.



(a) **(b)**

Figure 2.2: Illustration of the (a) head-on collision (adapted from [Wil00, p. 203]) and (b) the nano-beam collision scheme.

The longitudinal size of the overlap region d of two crossing beam bunches can be expressed as:

$$d \approx \frac{\sigma_{\mathrm{x}}^*}{\phi}, \tag{2.2}$$

with the half crossing angle ϕ of both bunches and the horizontal beam spread at the IP σ_x^*. The dependence on ϕ adjusted to 41.5 mrad and σ_{x}^* (10 µm/10 µm for LER/HER) which is significantly smaller than the bunch length σ_z^* (6 mm/5 mm for LER/HER), allows for a compression of β_y^*. [AFK18, p. 3]
In combination with the increased beam currents and reduction of emittances, it causes the increase of a factor of 40 in instantaneous luminosity (according to Eq. 2.1). The reduction of the beam-energy asymmetry results in a reduction of the boost from $\beta\gamma = 0.42$ to 0.28 [AFK18, p. 3]. However, this adjustment reduces the beam losses caused by Touschek scattering in the LER (explained in Sec. 2.3) [Kou+19, p. 22]. The new conditions of the accelerator associated with increased particle and background rates pose new challenges for the detector.

2.2 The Belle II detector

Advancing the SuperKEKB accelerator to higher luminosity and thus higher event rates poses new challenges for the experiment to record and understand the collisions. The Belle II detector has the capabilities required for particle track reconstruction, particle identification and energy measurement. Due to the versatility of the Belle II detector with its several detector components, Belle II is considered a multi-purpose detector. At increasing distances, seven sub-detectors cover the interaction point where positrons and electrons are brought to collision. The layout of the detector is depicted in Fig. 2.3.
The two innermost detector layers consisting of pixel and strip detectors form the Vertex Detector (VXD) and facilitate the reconstruction of primary interaction and secondary vertices, e.g. of B-meson decays, due to their high spatial resolution. Inside the Belle II volume, a superconducting solenoid magnet generates a magnetic field of 1.5 T. The field deflects charged particles on their trajectory and thus facilitates the determination of the particle momentum. A description of the seven sub-detectors is given below in ascending distance from the interaction point.

- *Pixel Detector (PXD)*: The PXD [Fis+07] is the detector closest to the interaction point. The detector uses DEPFET pixel sensors with a sensitive thickness of only 75 µm. In the final concept, 8 million pixels are distributed over 40 modules, which are arranged in two layers around the IP. The DEPFET technology and the PXD are described in more detail in Sec. 3.3 and Chap. 5, respectively.

- *Silicon Vertex Detector (SVD)*: The SVD [Tan+20] is divided into 4 layers cylindrically covering the interaction point in radii of 39 mm, 80 mm, 104 mm and 135 mm. Each layer

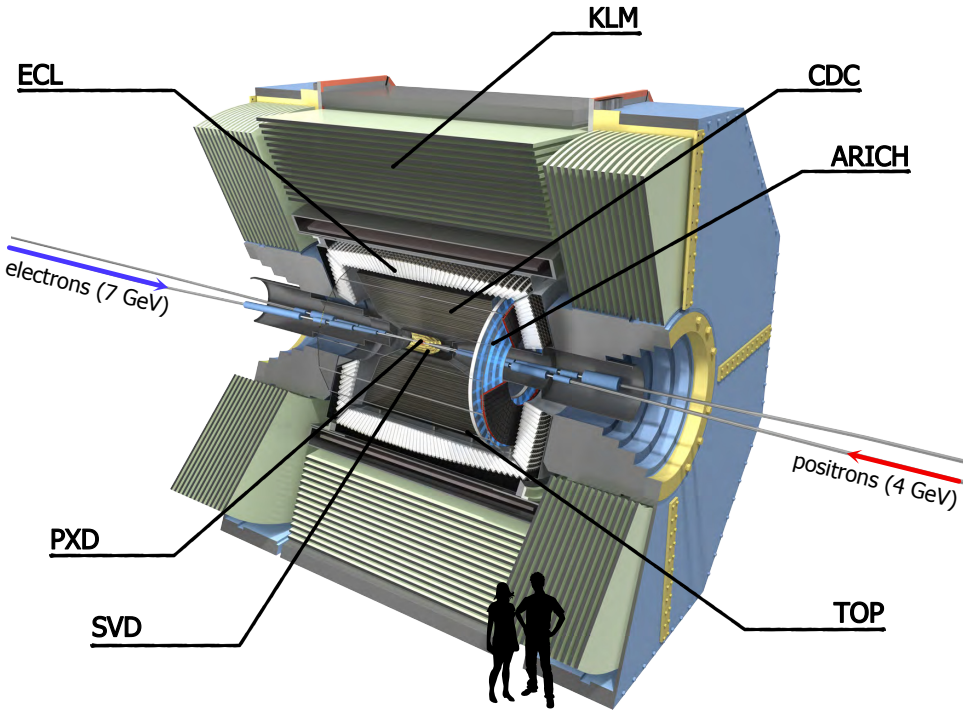


Figure 2.3: Schematic of the Belle II detector with its sub-detectors. Seven sub-detectors measure the properties of particles generated by collisions of electrons and positrons at the interaction point. From [Bel].

consists of Double-Sided Silicon Strip Detectors (DSSDs). The sensors are thinned to approximately 300 µm. The front-end chip APV25 is used to read out the orthogonally arranged strips and reconstruct the hit timing of incoming particles with a precision of a few ns [Fri+12, p. 872].

- *Central Drift Chamber (CDC)*: The cylindrical volume of 2.3 m length and 2.2 m diameter enclosing the VXD is the CDC [Tan17]. The inside of the CDC is filled with a gas mixture composed of 50 % helium and 50 % ethane. Moreover, 14 336 sense wires (30 µm gold-plated tungsten wires) and 42 240 field wires (126 µm aluminium wires) are distributed within the volume. The main task is to reconstruct trajectories and momenta of charged particles. Additionally, by measuring the specific energy loss (dE/dx), particle identification is performed. [Ada+18, p. 5]
  Charged particles traversing the CDC volume ionise the gas molecules and generate electron-ion pairs. The electrons drift towards the sense wires and are accelerated by the electric field creating avalanches which are measured by the sense wires. Consequently, the signal is read out and digitised by Analogue-to-Digital Converters (ADCs). There are two different orientations of the sense wires: Axial wires are parallel and stereo wires

skewed with respect to the beam direction. The arrangement in the CDC is shown in Fig. 2.4. Using the hit position measurement and arrival time of charges drifting to the sense wires, the particle trajectory can be reconstructed. [Fro13, pp. 11-18]

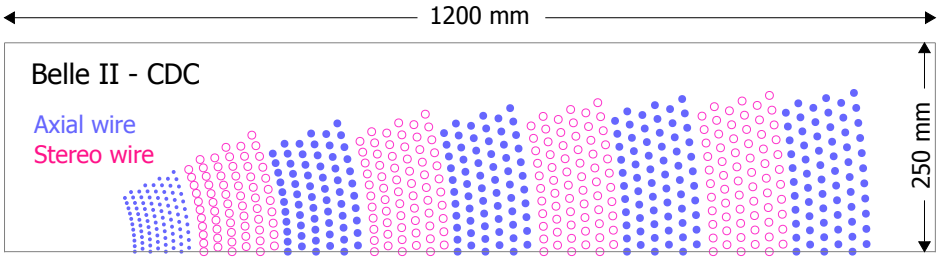
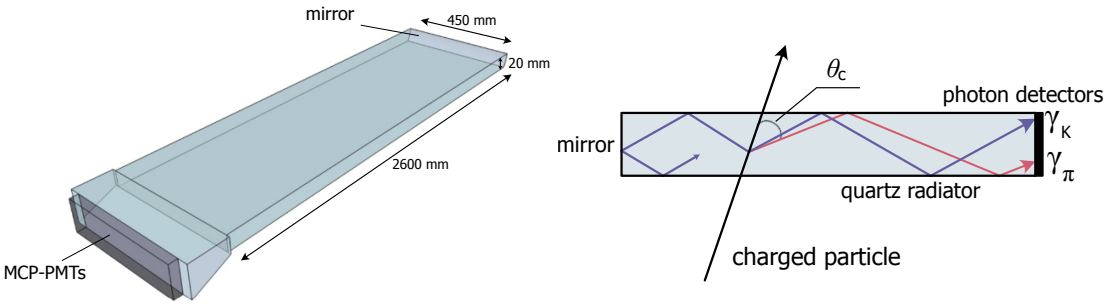


Figure 2.4: Wire configuration of the central drift chamber in Belle II. Axial and stereo wires are used to reconstruct the particle trajectory in all spatial directions. From [Ada+18, p. 6].

- *Time-Of-Propagation Detector (TOP)*: TOP [Fas17] is one of two sub-detectors used for particle identification in the central region of Belle II. It consists of 16 quartz radiator bars with an attached array of Micro-Channel-Plate Photomultiplier Tubes (MCP-PMTs) on one of the sides (see Fig. 2.5a). As shown in Fig. 2.5b, charged particles crossing the quartz emit Cherenkov radiation which is captured inside the radiator bars due to their internal reflection. The Cherenkov photons are guided to the MCP-PMTs measuring a coarse position and a precise time of arrival. [Tam20, p. 1]
  Based on the resulting Cherenkov angle, the velocity of the charged particle can be obtained. Furthermore, the particle can be identified using the precise time information. The TOP detector is particularly reliable in distinguishing between kaons and pions. [Tam20, p. 2]



(a) Model of a single quartz bar.

(b) Illustration of the working principle.

Figure 2.5: Schematic drawings of (a) the quartz radiator bar (from [Tam20, p. 1]) and (b) the working principle of the TOP detector. Charged particles (pions and kaons in this picture) emit Cherenkov photons with the Cherenkov angle θ_C. The photons are internally reflected and guided to photon detectors. Adapted from [Fas17, p. 2].

- *Aerogel Ring Cherenkov Detector (ARICH)*: Similar to the TOP detector, ARICH uses the measurement of Cherenkov radiation for particle identification. The detector is placed in the forward region of the Belle II detector and facilitates the discrimination between charged kaons and pions from 0.5 GeV to 4 GeV. Two 20 mm thick layers of aerogel with different refractive indices ($n_1 = 1.045$ and $n_2 = 1.055$) are used to focus the Cherenkov rings of charged particles on arrangements of Hybrid Avalanche Photo-Detectors (HAPDs). Fig. 2.6 illustrates the working principle. With 144 channels in a single HAPD, it is capable of single photon detection with precise position resolution. The reconstructed Cherenkov rings can be used to determine the opening angle and consequently the velocity of the particle. [Kin+20, p. 1]

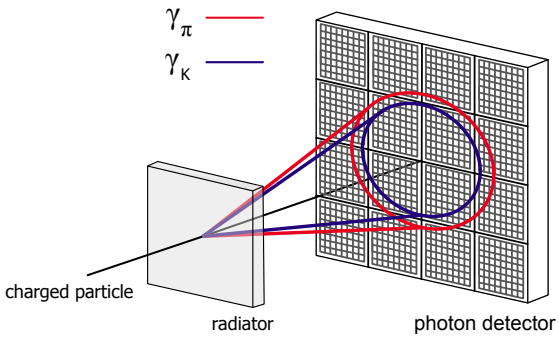


Figure 2.6: Illustration of the ARICH detection principle. Charged particles crossing the aerogel layer generate Cherenkov rings projected on an array of photon detectors. The measurement provides particle identification. From [Kin+20, p. 2].

- *Electromagnetic Calorimeter (ECL)*: The ECL consists of 8736 thallium-doped caesium iodide (CsI(Tl)) scintillator crystals distributed in the central, forward and backward region. Two photodiodes are glued to the surface of a single crystal to perform mainly energy and angular measurements of electrons, positrons and photons. Moreover, the ECL facilitates the separation of electrons and hadrons (e.g. pions) creating electromagnetic and hadronic showers. In combination with the KLM detector, it allows for long-lived neutral kaons (K_L) detection. In addition, the ECL is used for luminosity measurements and trigger generation for the other sub-detectors. [Abe+10, pp. 284-312]

- *K_L and Muon Detector (KLM)*: The outermost sub-detector is the KLM and is located outside of the solenoid magnet. The KLM is composed of 14 active layers and 15 passive iron layers (the solenoid's flux return yokes with a thickness of 4.7 cm) which are alternately built up in the central, forward and backward region. In the forward and backward region, the active layers are based on scintillator strips [Aus+14]. Resistive Plate Chambers (RPCs) are used for the central region [Yam+00]. In the absorber material, K_L mesons can produce hadronic showers. Furthermore, muons can be detected with the additional use of the CDC track information.

2.3 Accelerator beam backgrounds

An unavoidable consequence of operating particle beams in an accelerator is the occurrence of beam backgrounds. To gain an understanding of the measurements provided by each sub-detector of Belle II, it is therefore important to consider the origin of occurring background effects and their dependencies on the beam parameters and beam interactions. Backgrounds can be categorised into *beam-induced* and *luminosity-induced backgrounds*. The background types are described in the following.

Beam-induced backgrounds

Beam-gas scattering: For particles in the accelerator beams, scattering can occur with residual gas molecules present in the beam pipe. For electron and positron beams, the two dominant processes are Coulomb scattering and bremsstrahlung. In the first process, the initial direction of the beam particle is changed whereas in the second, the initial energy is reduced by emitting photons. The rate of interaction scales proportionally to the beam current and the vacuum pressure inside the beam pipe. [Lew+19, p. 71]
By increasing the beam currents at approximately the same vacuum pressure, an increase by a factor of ∼100 in Coulomb scattering is expected for SuperKEKB compared to KEKB [Iwa+12, p. 1826]. As a result, electrons or positrons may escape from the bunches and collide with the material of the inner beam pipe.

Touschek effect: Similar to the previous process, the Touschek effect occurs within the individual beams of the accelerator. It refers to the Coulomb scattering of two particles within a single bunch resulting in the loss of both scattering partners due to an energy transfer [Piw99, p. 2]. The consequence is the reduction of beam lifetime and the interaction of the scattered particles with the inner surface of the beam pipe creating particle showers. By introducing the nano-beam scheme in SuperKEKB, this effect is enhanced particularly in the interaction region. Particle showers entering the detector layers are termed Touschek background. The rate of scattering is proportional to the square of the number of particles per bunch and inversely proportional to the square of the beam size and the third power of the beam energy [Mol15, p. 164]. Therefore, the impact on the LER beam is higher than on the HER beam.

Synchrotron radiation: A charged particle that is accelerated, such as electrons and positrons in the SuperKEKB accelerator, emits a portion of its initial energy in form of electromagnetic radiation (photons), so-called synchrotron radiation. The energy loss ΔE in keV that occurs during one revolution for a charged particle in a circular accelerator can be expressed as follows, assuming a constant bending radius R in m [Wil00, p. 33]:

$$\Delta E = \frac{q^2}{3\epsilon_0 (m_0 c^2)^4} \frac{E^4}{R} \quad \overset{\text{electron}}{\Longrightarrow} \quad \Delta E = 88.5 \frac{E^4}{R}, \tag{2.3}$$

where ϵ_0 is the permittivity of free space, m_0 the mass of the charged particle and E its energy in GeV.

For relativistic charged particles undergoing transverse acceleration, a strongly collimated distribution of synchrotron radiation is produced. The conical shape has an half-opening angle of approximately $1/\gamma$ [Mol15, p. 185]. It is shown for the centre-of-mass frame and the laboratory frame in Fig. 2.7. At SuperKEKB, the energy of the photons originating from synchrotron

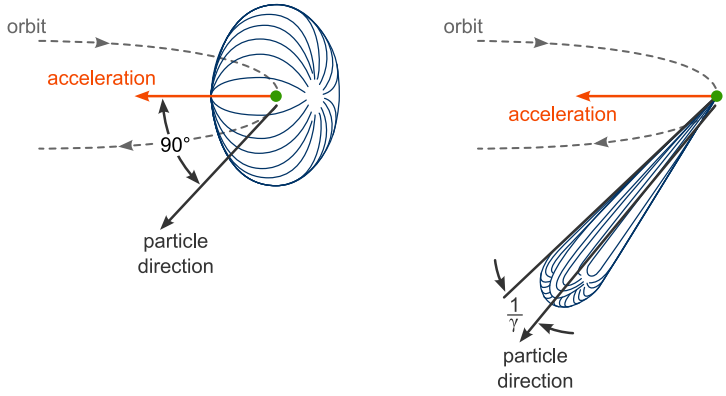


Figure 2.7: Accelerated charged particle emitting synchrotron radiation. *Left*: In the centre-of-mass frame (movement alongside the particle). *Right*: In the laboratory frame, the particle emits synchrotron radiation in a narrow cone. From [Mol15, p. 186].

radiation ranges from a few keV to tens of keV [Lew+19, p. 71]. As a result, one of the main challenges of the accelerator is the prevention of radiation damage to the detectors. These preventive measures are discussed in Chap. 4.

Luminosity-related backgrounds

Radiative Bhabha scattering: A luminosity-dependent background is the radiative Bhabha scattering. The process involves the scattering of an electron with a positron mostly at a small scattering angle. Additionally, a photon can be emitted (see Fig. 2.8a) which can collide with the material of the beam pipe or the magnets. It can cause a giant dipole resonance of an atomic nucleus in the material which de-excites by the emission of a neutron [Mol15, p. 206]. The production rate of these events is proportional to the luminosity, resulting in a significant increase for the SuperKEKB accelerator compared to KEKB [Lew+19, p. 71]. The neutrons resulting from this effect are the main background source for the KLM detector.

Two-photon process: In the two-photon process, two photons emitted from the initial electron-positron pair are interacting and create a low-energy fermion pair ($f\overline{f}$-pair, most likely e^-e^+). The process is depicted in Fig. 2.8b. Due to the low momentum of the pairs, they can spiral within the solenoid field and cause multiple hits, especially in the inner detector layers [Lew+19, p. 72].

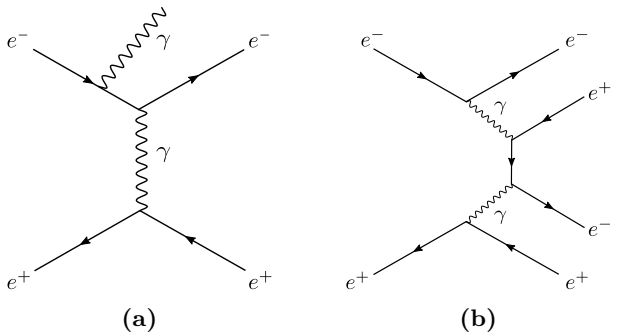


Figure 2.8: Feynman diagrams of two luminosity-related backgrounds. (a) Radiative Bhabha scattering creates an additional photon. (b) One fermion pair is created by the two-photon process, here an additional electron-positron pair.

3 Silicon pixel detectors

Pixel detectors have become indispensable in modern high-energy physics experiments thanks to their high granularity and application for precision particle tracking (e.g. [Mag16; CMS20]). This chapter first describes the charge generating process in the interaction of particles with matter, especially for charged particles and photons. It is followed by an introduction to silicon and its use as sensing material. Finally, two different pixel detector technologies are presented, both of them are used in this thesis.

3.1 Charge generation in silicon detectors

Detectors based on silicon are the most common type for pixel detectors. The interaction of charged particles with the sensor material causes a generation of secondary charges which serve as a signal that is further processed in dedicated readout electronics (see Sec. 3.2.2). In this section, the interaction processes are described first, followed by a discussion of the characteristics of silicon as a detector material. A comprehensive description can be found in [KW20; Zyl+20].

3.1.1 Charged particle interaction with matter

Charged particles lose energy as they pass through matter due to ionisation and excitation of atoms and bremsstrahlung. In these processes, a distinction between electrons and heavy charged particles ($M \gg m_e$) is necessary. The mean rate at which a heavy charged particle loses energy (mean rate of energy loss) per path length is described by the Bethe formula [Zyl+20, p. 536]:

$$\left\langle -\frac{dE}{dx} \right\rangle = K \frac{Z}{A} \frac{z^2}{\beta^2} \left[\frac{1}{2} \ln \frac{2 m_e c^2 \beta^2 \gamma^2 W_{\max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right].$$

The occurring quantities in the formula are listed in Tab. 3.1.
The formula for the so-called *mass stopping power* is accurate within a range of $\beta\gamma \sim 0.1$ - 1000 with uncertainties of only a few percent [Zyl+20, p. 536]. In the case of electrons and positrons, the Bethe formula cannot be used without additional correction terms [Zyl+20, p. 539]. Particularly, the effect of bremsstrahlung for high energies is an essential difference to the energy loss of heavy particles [KW20, p. 35]. This interaction of a charged particle with the Coulomb field of the nucleus leads to the emission of a high-energy photon.

Symbol	Definition
K	$4\pi N_A r_e^2 m_e c^2 = 0.307\,\mathrm{MeV mol^{-1} cm^2}$, coefficient consisting of Avogadro's number N_A, classical electron radius r_e and electron rest mass $m_e c^2$
Z, A	atomic number/atomic mass of material atoms
z	charge of traversing particle
β, γ	velocity of particle ($\beta = \frac{v}{c}$) and Lorentz factor ($\gamma = \frac{1}{\sqrt{1-\beta^2}}$)
$W_{\max}$	maximum energy transfer to electron in atom shell
I	mean excitation energy
$\delta(\beta\gamma)$	density correction factor for high energies

Table 3.1: Short explanation of symbols in the Bethe formula. From [KW20, p. 30].

The effect scales with the inverse quadratic mass of the incident particle ($\propto \frac{E}{m^2}$) [KW20, p. 54]. Fig. 3.1 illustrates the mean energy loss rate for electrons in silicon.

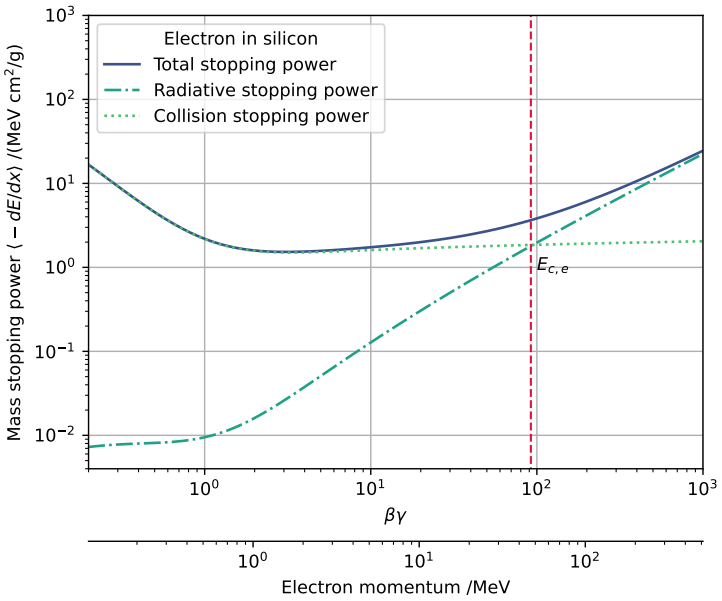


Figure 3.1: Mass stopping power ($\langle -\frac{dE}{dx} \rangle$) for electrons in silicon as a function of $\beta\gamma$ and electron momentum. The critical energy ($E_{c,e}$) describes the point at which energy loss from radiation outweighs the loss from collisions. Data from the ESTAR database [Ber+05].

The contributions of energy losses by ionisation and by bremsstrahlung are shown separately. The mean energy loss for an electron in silicon shows a broad minimum for $\beta\gamma \sim 3\text{-}3.5$. Particles in this range and with $\beta\gamma > 3.5$ are termed *Minimum Ionising Particles* (MIPs) [Zyl+20, p. 537]. Initially, the energy loss due to collisions dominates for smaller energies while bremsstrahlung

has the largest impact at higher energies. The intersection point of the two contributions is referred to as critical energy $E_{c,e}$. Using the extracted electron momentum, the two distributions intersect at an energy of approximately 48 MeV.

Radiation length

A measure of the energy loss of high-energy electrons when passing through matter is the radiation length X_0. It characterises the loss occurring primarily due to bremsstrahlung. The radiation length indicates the distance after which the electron loses $1 - 1/e = 63\,\%$ of its initial energy due to radiation. In detector physics, the radiation length is often used to describe the thicknesses of detector materials. In addition, it is used in the characterisation of other effects in the Coulomb field of the nucleus, e.g. pair production of photons and multiple scattering.[KW20, p. 61]

3.1.2 Photon interaction with matter

Compared to the energy loss of charged particles in matter, photon beams experience an attenuation in intensity as they traverse matter with a thickness d. The number of photons decreases exponentially which leads to a reduction of the initial beam intensity I_0 and can be expressed with the following formula [Kle98, p. 17]:

$$I = I_0 \, \mathrm{e}^{-\mu d}.$$

The linear attenuation coefficient μ reflects the density of the target material n and the cross-section σ, which is a measure of the probability of a photon being absorbed or scattered [KW20, p. 23].
The major contributors to the attenuation are three processes that have varying attenuation coefficients depending on the photon energy. The coefficient can be expressed by [Kle98, p. 17]:

$$\mu(E) = \mu_{\mathrm{Photo}} + \mu_{\mathrm{Compton}} + \mu_{\mathrm{Pair}}.$$

The mass attenuation (normalised to density ρ of the material: μ/ρ) for silicon as a function of the photon energy is depicted in Fig. 3.2a. The three main processes are described in detail below [KW20, pp. 70-85]:

1. *Photoelectric effect*: As shown in Fig. 3.2a, the photoelectric effect is the dominant process in the photon energy range from a few keV to about 70 keV. In this process, the energy of the incoming photon ($E_\gamma = h\nu$) is transferred to the material atom and a shell electron is emitted. The condition for absorption is a photon energy which exceeds the binding energy of the electron (E_{B}). In this case, the kinetic energy of the electron is the difference

between the photon energy and binding energy [KW20, p. 74]:

$$T = E_\gamma - E_\mathrm{B}.$$

This process leads to ionisation of the atom. Vacancies in the inner shell can be filled with electrons from the outer shells.
For the two sensor thicknesses of detector technologies used in this thesis, Fig. 3.2b shows the fraction of absorbed beam photons with intensity I as a function of photon energy. The curve indicates that especially for photon energies higher than 60 keV, the probability of observing an interaction in the silicon sensor almost vanishes.

2. *Compton scattering*: In the photon energy range from 100 keV to 100 MeV, the dominant process is Compton scattering. This process describes the elastic scattering of a photon off a shell electron which causes a partial energy transfer to the kinetic energy of the electron ($T_e = E_\gamma - E'_\gamma$). The electron is called quasi-free in the case of a photon energy that exceeds significantly the binding energy of the electron ($E_\gamma \gg E_\mathrm{B}$).[KW20, p. 78]
The energy of the deflected photon depends on the initial energy (E_γ) and the scattering angle (θ_γ) by [KW20, p. 79]:

$$E'_\gamma = \frac{E_\gamma}{1 + \frac{E_\gamma}{m_e c^2}(1 - \cos\theta_\gamma)}.$$

Therefore, the maximum energy transfer to the electron ($T_{e,\mathrm{max}}$) occurs for backscattered photons ($\theta_\gamma = 180°$).

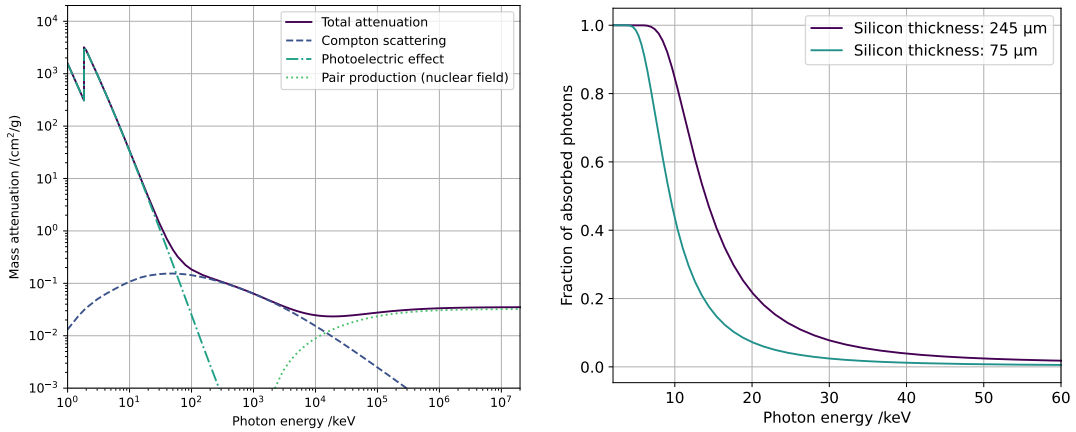
3. *Pair production*: In the presence of the Coulomb field of a nucleus (e.g. silicon nucleus), photons can convert into an electron-positron pair at an energy of at least twice the electron rest mass:

$$E_\gamma \gtrsim 2m_e = 1.022\,\mathrm{MeV}.$$

In addition, the nucleus experiences a recoil that contributes to the minimum energy for pair formation. In the case of light elements, pair production can additionally occur in the presence of the electron in the atomic shell. For silicon, pair production is the dominant effect for photon energies above 10 MeV. The cross section for pair production can be approximated to [Zyl+20, p. 543]:

$$\sigma_\mathrm{Pair} \approx \frac{7}{9}\frac{1}{X_0}\frac{A}{N_A \rho}.$$

An increased radiation length X_0 due to low-mass and low-density materials leads to a suppression of pair production.



(a) **(b)**

Figure 3.2: (a) Mass attenuation coefficient of silicon as a function of photon energy. The contributions of three processes (photoelectric effect, Compton scattering and pair production) sum up to the total mass attenuation coefficient. Data from [Sel87]. (b) Fraction of absorbed photons $(1 - I/I_0)$ as a function of photon energy for silicon thicknesses of 75 µm (DEPFET module, in Chap. 5) and 245 µm (FANGS, in Chap. 4). Data from [Sel95].

3.1.3 Silicon semiconductors as detector material

A fundamental process in the fabrication of silicon sensors is the doping of silicon. Doping describes a method of modifying the electrical properties of the semiconductor by introducing impurities into the crystal structure. For this purpose, elements from the third or fifth main group are used, which contain three or five valence electrons, respectively. In the case of inserting elements with five valence electrons, four of them form a covalent bond with silicon atoms. It is referred to as n-type doping in which the fifth electron is unbound in the crystal (donors). For elements from the third group, one electron is missing for the bond. The insertion of so-called holes (acceptors) into the silicon crystal is known as p-type doping. In the band model, p-type and n-type doping in silicon can be represented as in Fig. 3.3.

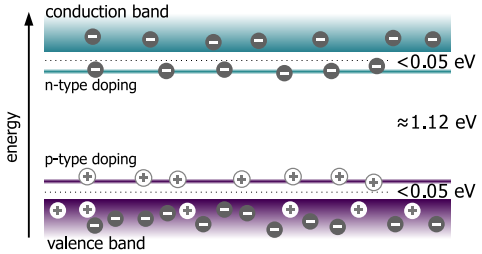


Figure 3.3: Schematic energy band representation for n- and p-type doping. Dopants introduce electrons or holes that are only weakly bound. In silicon, the band gap is 1.12 eV at room temperature [KW20, p. 264]. From [Poh20, p. 21].

The energy levels of the introduced electrons and holes have an energetically small distance to the conduction and valence band, respectively. At room temperature, there is sufficient energy for these charge carriers to enter the relevant band.[Poh20, p. 20]
Once doped semiconductors with different doping (p- and n-type doping) are brought into thermal contact, a *pn-junction* is formed. During this process, the electrons diffuse into the p-type region and the holes into the n-type region where they recombine. Consequently, the dopants are ionised and a region without free charge carriers is formed, called *space charge region* (or *depletion zone*). The outcome of this process is shown in Fig. 3.4.

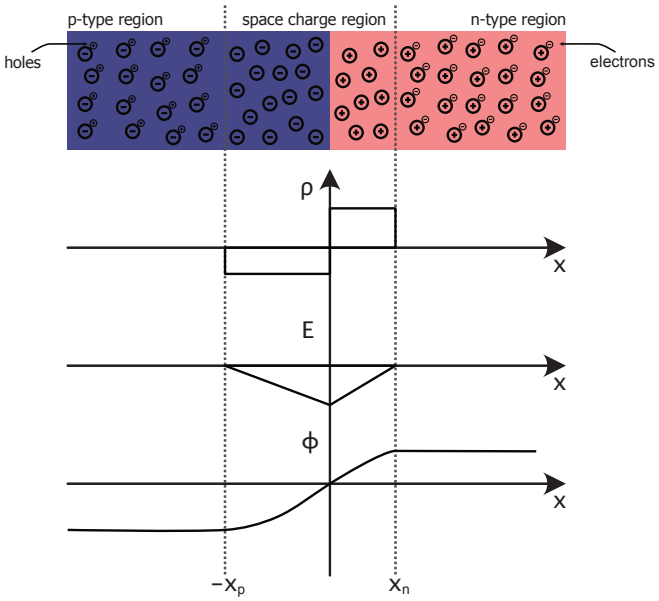


Figure 3.4: Schematic drawing of a *pn*-junction of two doped silicon regions. Due to diffusion and recombination of the charge carriers, a space charge region is created. The charge density ρ, electric field E and potential Φ are plotted against the location. Adapted from [KW16, p. 291].

A thermal equilibrium occurs when the resulting electric field counteracts diffusion. In the neutral regions, the concentration of majority charge carriers is high and the transition zone to the space charge region is very narrow, so that an abrupt change of the regions can be well assumed for the calculation of the potential. For this purpose, the one-dimensional Maxwell equation for the electric field $E(x)$ is considered [KW20, p.276]:

$$\frac{dE(x)}{dx} = \frac{1}{\epsilon\epsilon_0}\rho(x), \quad \text{with} \quad \rho(x) = \begin{cases} -eN_A, & -x_p < x < 0, \\ +eN_D, & 0 < x < x_n. \end{cases} \tag{3.1}$$

$$\Rightarrow E(x) = \begin{cases} \frac{-eN_A}{\epsilon\epsilon_0}(x + x_p), & -x_p < x < 0, \\ \frac{+eN_D}{\epsilon\epsilon_0}(x - x_n), & 0 < x < x_n. \end{cases} \tag{3.2}$$

The charge density $\rho(x)$ depends exclusively on the spatial doping concentration for n-type (N_D) and p-type (N_A) regions. The constants $\epsilon\epsilon_0$ define the vacuum and silicon permittivity and x_p, x_n describe the width of the depletion zone in the p- and n-type region, respectively. The electric field has a maximum at the junction ($x = 0$). The emerging potential difference between the n- and p-region is called *built-in voltage* V_{bi}. By integrating the electric field across the junction, the following expression for V_{bi} is obtained [KW20, p. 277]:

$$V_{\text{bi}} = -\int_{-x_p}^{x_n} E(x)\,dx = \frac{e}{2\epsilon\epsilon_0}(N_A x_p^2 + N_D x_n^2). \tag{3.3}$$

A commonly known value for the built-in voltage for a silicon junction is about 0.6 V [KW20, p. 275].
The depletion zone can be enlarged by applying a reverse voltage (n-doped side positive, p-doped side negative) resulting in an increase of the depletion width. The width d with external voltage V_{ext} can be approximated as [KW20, p.283]:

$$d \approx \sqrt{\frac{2\epsilon\epsilon_0}{e}\frac{1}{N_{D,A}}(V_{\text{bi}} + V_{\text{ext}})}. \tag{3.4}$$

The depletion region is a key factor in the use of silicon semiconductors as a sensing material for the detection of traversing charged particles. As explained in Sec. 3.1, charged particles and photons can deposit energy in matter (silicon sensor). Based on one of the effects discussed, the energy transfer results in an electron and a hole as a mobile charge carrier in the conduction band and valence band, respectively. The average energy to create an electron-hole pair in silicon is $E_{e/h} = 3.65\,\text{eV}$ at room temperature [KW20, p. 299].
The electric field generated by built-in potential and applied bias voltage causes the charges in the sensor (electrons and holes) to drift apart. In a frequently used sensor design, which is discussed in Sec. 3.2.1, readout electrode implantations with a high doping concentration (n^+-type) are located on one side and a single backside implementation (p^+-type) on the other. Based on the Shockley-Ramo theorem [Ram39, p. 584], a current is induced by the movement of the charge in the electric field of the readout electrode. The induced current can be represented as [Ram39, p. 584]:

$$i_{\text{ind}} = q\vec{E}_W\vec{v}, \tag{3.5}$$

with the charge q of the moving charge carrier, its drift velocity v and the weighting field $\vec{E}_W$. The weighting potential Φ_W can be derived from the weighting field via $\vec{E}_W = -\vec{\nabla}\Phi_W$. The weighting field and potential are shown for readout electrodes in the configuration of a pixel sensor in Fig. 3.5.

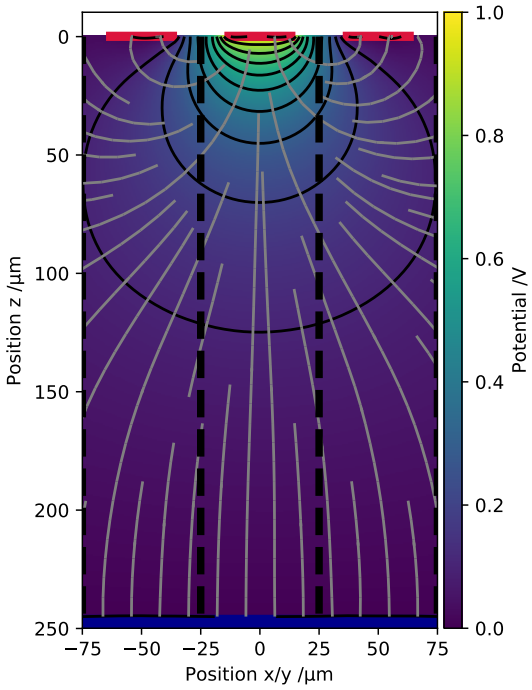


Figure 3.5: Weighting field and potential of a 30 µm readout electrode in a 245 µm thick pixel sensor. Simulated with scarce [Poh20, p. 89].

The total charge received at the electrode due to a single charge carrier drifting from position x_0 to x_1 is given by [He01, p. 254]:

$$Q = \int_{t_0}^{t_1} i_{\text{ind}}(t)\, dt = q\left[\Phi_W(x_0) - \Phi_W(x_1)\right]. \tag{3.6}$$

In the presence of an electric field, generated charge carriers move to the readout electrode or to the backside implementation of the sensor, depending on their charge. The drift velocity depends on the mobility μ and the electric field $\vec{E}$:

$$\vec{v} = \mu\vec{E}. \tag{3.7}$$

Due to a higher mobility resulting in a faster signal [KW20, p. 122], the collection of electrons is commonly used in silicon sensor designs, e.g. in [Unn+13; Göß+11]. In a sensor with a conventional electric field applied, the collection time is only a few nanoseconds [Poh20, p. 28].

3.2 Hybrid pixel detectors

The *hybrid pixel detector* technology combines signal generation in a silicon sensor with charge measurement capability in a readout chip. In the final manufacturing step, the individually produced sensor and readout chip are interconnected [Ros+06, p. 1]. The construction of this type of detector is shown in Fig. 3.6. Ionising particles traversing the sensor create charges

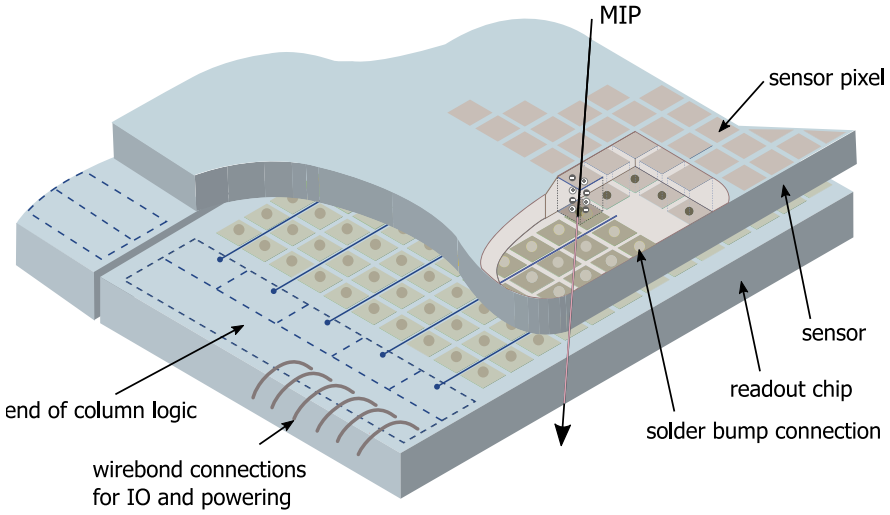


Figure 3.6: Layout of a hybrid pixel detector consisting of a sensor and a readout chip. An incoming MIP generates charge carriers in a pixel volume of the sensor. From [Poh20, p. 47].

that produce a signal in the readout electronics. For accurate spatial resolution, the sensor is pixelated with readout electrodes. Using bump pads, the sensor pixels are individually connected to the readout electronics of the readout chip utilising bump bonding [Ros+06, p. 203]. The connection to the outside world for data transmission and power supply is provided by wire bonds. In the following, the components of a hybrid pixel detector are explained using the example of a planar silicon sensor and the FE-I4 readout chip (see Sec. 3.2.2).

3.2.1 Planar silicon pixel sensor

A common sensor type for hybrid pixel detectors is the planar implementation of doped silicon layers with readout electrodes on the surface. For the FANGS detector (see Chap. 4), a planar n^+-in-n silicon sensor is used, which has been tested and used for the ATLAS Insertable B-Layer (IBL) [Göß+11]. To match the design of the readout chip, the n^+-readout electrodes on the frontside have a size of $50 \times 250\,\mu m^2$. Exceptions are the edge column pixels with a dimension of $50 \times 500\,\mu m^2$ [Bac14, p. 37]. The backside consists of a single p^+-implant through which the high voltage is applied to deplete the n-doped bulk material. Guard rings reduce the potential in the direction of the edges of the backside implant.

3.2.2 FE-I4 readout chip

The FE-I4B readout chip is used to read out the charge generated in the silicon sensor. It has been designed in a 130 nm CMOS process specifically for the ATLAS IBL [La 16]. Specifications for operation in the ATLAS experiment make the chip ideal for use in harsh radiation environments. In fact, the FE-I4 can endure a particle rate of up to 400 MHz/cm^2 (with less than 1 % data loss) and a Total Ionising Dose (TID) of 300 Mrad [FEI12, p. 10]. The chip provides the parallel processing of 26 880 readout channels in an array of 336×80 pixels (*rows* $\times$ *columns*). The dimensions of a single readout channel are $50 \times 250\,\mu m^2$. Fig. 3.7 shows the schematic of a single readout pixel in the FE-I4.

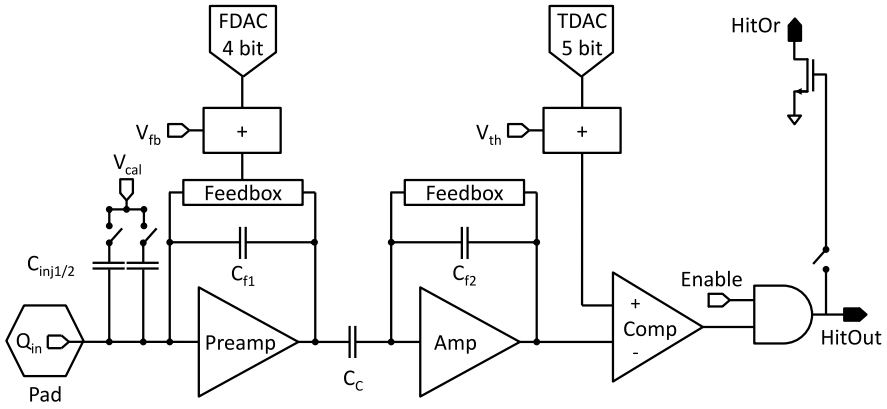


Figure 3.7: Schematic of the analogue pixel cell of the FE-I4 including a two staged AC-coupled amplifier (*Preamp*, *Amp*), comparator (*Comp*), an enable switch (*Enable*), a hit bus (*HitOr*) and the connection to the digital layer (*HitOut*). Amplifier and comparator are adjustable via V_{fb}/*FDAC* and V_{th}/*TDAC*, respectively. For tuning purposes, an internal charge injection is available ($C_{inj1,2}$ and V_{cal}). From [Poh+15, p. 3].

The connection to the sensor is made via the pad allowing charge to reach the analogue pixel cell of the FE-I4 (Q_{in}). Initially, the signal is processed by an AC-coupled two-staged Charge-Sensitive Amplifier (CSA). The output of the amplifier is fed into a comparator. Using Digital-to-Analogue Converters (DACs), the shaping time of the amplifier and the threshold of the comparator can be adjusted individually for each pixel via the 4-bit feedback DAC (*FDAC*), and the 5-bit threshold DAC (*TDAC*), respectively [Poh+15, p. 3]. In this way, a uniform charge response of all pixels can be ensured in a tuning procedure. The essential feature of pixel tuning is the possibility of internal charge injection using the voltage steps V_{cal} and the selectable capacitors $C_{inj1,2}$. The voltage steps can be set with a 12-bit DAC [Poh20, p. 108], hence the charge unit is referred to as PulserDAC (*PlsrDAC*). A detailed description of the tuning procedure is given in [Poh20, p. 102].
An additional functionality of the FE-I4 is the charge measurement using the *Time-over-*

Threshold (ToT) method. For this, an internal 40 MHz clock is applied to sample the signal above the threshold of the discriminator leading to charge information with 4-bit resolution. An improvement in the resolution of charge measurements is outlined in the next section.

TDC method for charge measurements

The output of the analogue pixel cell (*HitOut*) can be connected to a hit bus (*HitOr*) using a logical OR between all pixels [Bac14, p. 39]. The resulting signal from the HitOr contains the longest ToT of all signal-carrying pixels. An improvement in resolution of the charge measurement can be achieved by measuring the HitOr signal in counts of a 640 MHz clock instead of the usual 40 MHz. The clock is generated by the FPGA-based readout system and it is referred to as the *Time-Digital-Converter (TDC) method*. Regarding charge measurements, the resolution increases from 4 bits to 12 bits.

3.3 DEPFET principle

In 1986, J. Kemmer and G. Lutz published the concept of a transistor-based detector with the idea that this approach could possibly be used in pixel arrays [KL87]. The Depleted P-channel Field-Effect Transistor (DEPFET) structure combines charge detection and amplification within a single unit. This is achieved by the implementation of a Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) into a depleted n^--doped silicon bulk. A cross-section of the described structure is shown in Figure 3.8.

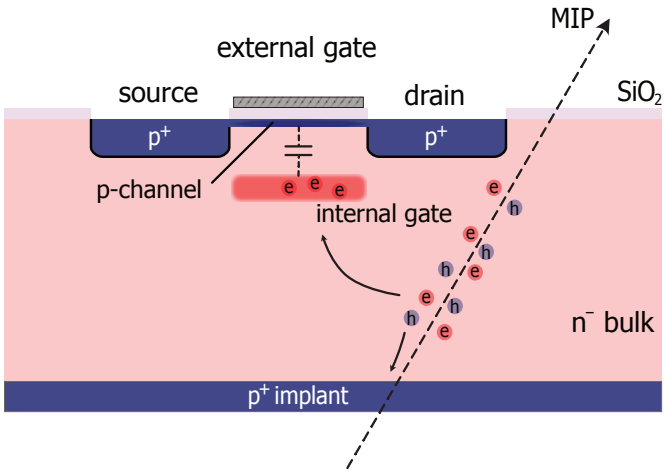


Figure 3.8: Cross-section of a DEPFET pixel cell. A MOSFET is implemented inside a fully depleted silicon bulk. Charged particles generate electron-hole pairs which drift to the potential minimum (*internal gate*).

In the upper part of the structure, a MOSFET is placed. The current flowing in the p-channel (holes are the majority carriers) from *source* to *drain* (short: *drain current*) is controlled by varying the voltage V_g applied to the *external gate*. The external gate electrode is electrically isolated from the p-channel by a very thin layer of insulating silicon dioxide (SiO_2). The drain current I_d of a MOSFET operated in saturation can be calculated by using [KW20, p. 330]:

$$I_d = \frac{W}{2L}\mu_h C_{ox}(V_g - V_{th})^2, \tag{3.8}$$

with width W and length L of the external gate, the hole mobility μ_h, the oxide capacitance per area C_{ox} and the gate and threshold voltages V_g and V_{th}, respectively. The MOSFET is located in a completely depleted n^--doped silicon bulk. The depleting mechanism is described in Sec. 3.3.2. The essential implementation in the DEPFET is the *internal gate* placed in the silicon less than 1 µm below the p-channel [Ric+03, p. 251]. The internal gate acts as a potential minimum for electrons created by ionising particles in the silicon bulk. These electrons accumulate in the internal gate while the holes drift to the p^+-backside. As a result, the electrons in the internal gate introduce mirror charges in the conductive p-channel. The effect is equivalent to an external gate voltage change by an amount of [Lut99, p. 248]:

$$\Delta V_g = \frac{\alpha q_{\text{sig}}}{C_g} = \frac{\alpha q_{\text{sig}}}{WLC_{ox}}, \tag{3.9}$$

with the fraction α of the induced charge due to the signal charge q_{sig} in the internal gate. The gate-channel capacitance C_g is composed of the gate area $W \times L$ times the oxide capacitance per area C_{ox}. As a result of ΔV_g, the modulated drain current can be described by:

$$I_d + \Delta I_d = \frac{W}{2L}\mu_h C_{ox}\left(V_g + \frac{\alpha q_{\text{sig}}}{WLC_{ox}} - V_{th}\right)^2 \tag{3.10}$$

$$= \frac{W}{2L}\mu_h C_{ox}\left((V_g - V_{th})^2 + \frac{2\alpha q_{\text{sig}}}{WLC_{ox}}(V_g - V_{th}) + \mathcal{O}(q_{\text{sig}}^2)\right), \tag{3.11}$$

where the q_{sig}^2 term is negligible. A parameter for describing the performance of a DEPFET sensor is the internal gain of the drain current, referred to as g_q:

$$g_q = \frac{d(I_d + \Delta I_d)}{dq_{\text{sig}}} = \frac{\alpha\mu_h}{L^2}(V_g - V_{th}) = \alpha\sqrt{\frac{2\mu_h I_d}{WL^3 C_{ox}}}. \tag{3.12}$$

Increasing the number of electrons in the internal gate leads to an increased drain current of approximately 400-500 pA per electron, which makes the DEPFET structure a detector and an amplifier at the same time [KW20, p. 330]. The DEPFET principle is based on non-destructive measurement of the charge inside the internal gate, i.e. the electrons remain inside the potential minimum for various readouts of the drain current. A dedicated clearing mechanism has to be introduced for the periodical removal of the electrons inside the internal gate.

3.3.1 Clearing mechanism

The removal of signal charges in the internal gate is realised by an n^+-implant (*clear* implant). The implant is located parallel to the source-drain arrangement of the MOSFET. An overview of this pixel design is shown in Fig. 3.9. On top of the silicon bulk, a polysilicon layer is placed

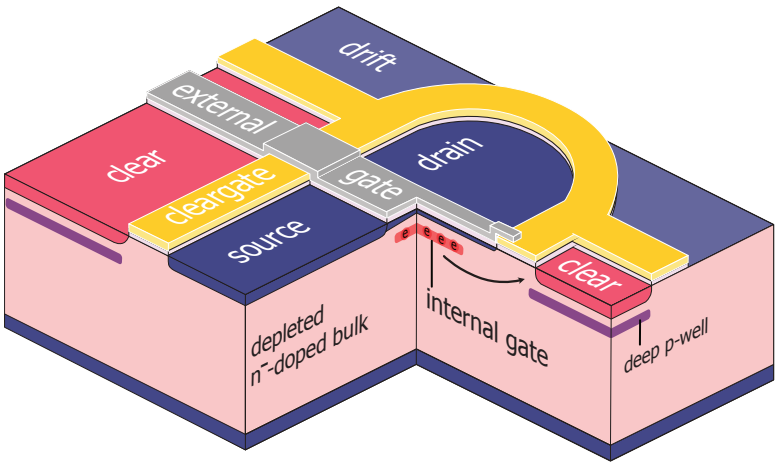


Figure 3.9: Overview of the DEPFET pixel design. In the clearing process, the signal charge in the internal gate is drifting to the clear implant.

between the n^+-doped clear implant and the internal gate. It is referred to as the *cleargate*. During charge collection and sampling of the signal, the layer below the polysilicon serves as a potential barrier between the clear and the internal gate. Once the clearing process starts, a positive voltage is applied to the clear contact and the barrier between the internal gate and clear implant is supposed to be overcome by the signal charge. Therefore, the potential barrier created by the voltage at cleargate must be reduced. A possible approach would be a dynamic shifting of the cleargate voltage. In the described DEPFET design, a constant cleargate voltage is applied, but it is capacitively coupled to the clear contact [Rum09, pp. 96-111] (shown in Fig. 3.10).

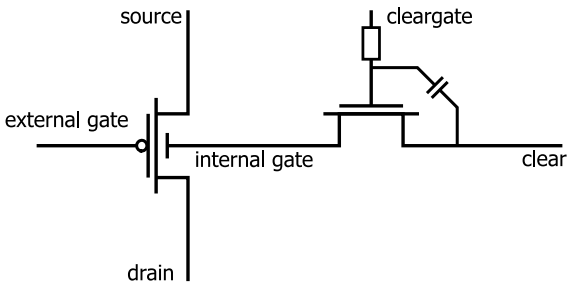


Figure 3.10: Simplified circuit diagram of a single DEPFET pixel. The implementations for removing signal charges in the internal gate represent an additional transistor. Cleargate is capacitively coupled to the clear contact.

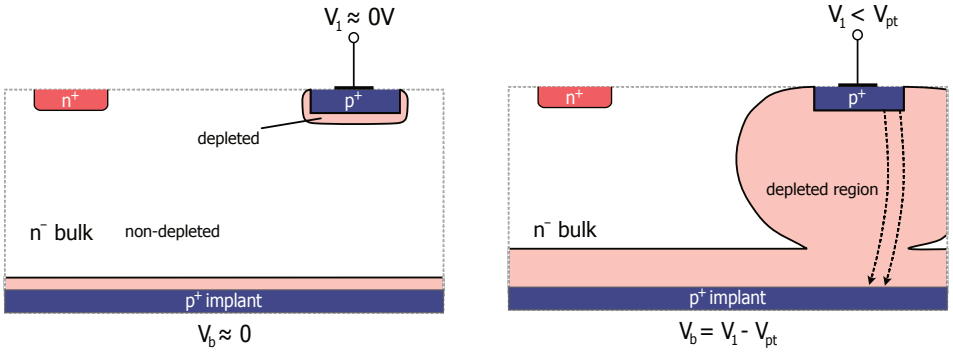
As a result, when a positive voltage is applied to the clear contact, the potential barrier below the cleargate is reduced and a punch-through is formed from the clear implant into the internal gate. Finally, the desirable complete removal of signal charges from the internal gate can be achieved. In order to prevent influencing the electron collection phase, the clear implant is shielded by a p region (*deep p-well*).
As a summary, the implants in a DEPFET pixel are listed and described in Tab. 3.2. The implementation of DEPFET pixels in a detector is discussed in Chap. 5.

Name	Material	Description
bulk	n^--doped silicon	Silicon bulk which can be fully depleted (see Sec. 3.3.2). Ionising particles create electron-hole pairs within the depleted bulk.
external gate	polysilicon	Gate of the MOSFET. The voltage at the external gate influences the current flowing from source to drain.
source / drain	p^+-doped silicon	Strongly p-doped implants. Without a voltage at external gate, charge carriers are (almost) prevented from flowing from source to drain.
internal gate	n-doped silicon	An n-doped region below the p-channel transistor. Potential minimum attracts electrons from the signal charge modulating the drain current.
clear	n^+-doped silicon	Region positioned parallel to the MOSFET structure allowing the clearing mechanism for removing signal charge in the internal gate. Electrons in the internal gate are attracted to clear by a punch-through between both regions.
cleargate	polysilicon	Polysilicon structure depending on the applied voltage on clear, either serves as a potential barrier to the clear region or, through capacitive coupling to the clear region, reduces this barrier and allows for a flow of electrons from the internal gate to the clear implant.
drift	p-doped silicon	Implant to create lateral drift fields for electrons to move to the internal gate. Due to the present fields, electrons first move to the frontside of the DEPFET structure before drifting vertically towards the internal gate.

Table 3.2: Short summary of the implementations used for a DEPFET pixel.

3.3.2 Depletion concept

In order to deplete the n^--bulk material of the DEPFET sensor, the *punch-through technique* is utilised [KW20, p. 305]. It facilitates depletion via the p^+-backside implant by using an additional p^+-implant (punch-through contact) without the need for a direct wire bond connection. If no voltage is applied at the implant ($V_1 \approx 0\,\mathrm{V}$), only the intrinsic depletion regions below and above the p^+-implant and p^+-backside are formed, respectively, as shown in Fig. 3.11a. As soon as a negative voltage is supplied, the depletion region grows underneath the implant. With increasing negative voltages, the zone grows until the depletion regions of the two implants touch each other. At this point, the punch-through voltage V_{pt} is reached and further reduction of the voltage causes the two regions to merge. Fig. 3.11b illustrates this process.



(a) Without applied voltage. **(b)** With applied voltage.

Figure 3.11: Schematic drawing of the depletion process using a punch-through contact. (a) Without applied voltage, only intrinsic depletion regions are formed in the n^--bulk at the contacts. (b) With increasing negative voltages applied to the contact, the depletion region expands until both regions combine ($V_1 < V_{pt}$). Adapted from [Lut99, p. 122].

The voltage at the p^+-backside follows the voltage at the punch-through contact. However, it is reduced by the voltage that is dropped over the distance corresponding to the thickness of the sensor. Due to the good conductivity of the backside, the entire n^--bulk sensor material can be depleted. Holes generated in the fully depleted material first migrate to the backside and along it towards the punch-through contact. Through thermal emission, they can overcome the potential barrier and cause the current to flow through the punch-through contact [Lut99, p. 122].

4 FANGS: A background radiation monitor

The process of increasing luminosity from KEKB to SuperKEKB required a sequential commissioning of the new machine. It was divided into several steps, called *phases*, depending on the state of accelerator and Belle II detector. To investigate the radiation environment in the VXD volume and to help in the commissioning of the accelerator, the FE-I4 ATLAS Near Gamma Sensors (FANGS) detector was developed. Combined with other dedicated sub-detectors for measuring background rates, it formed the Beam Exorcism for A Stable experiment II (BEAST II). The BEAST II experiment collected data from *March* to end of *July 2018* [Lip+21].
In this chapter, the commissioning phases are described. Furthermore, the FANGS detector is presented, concluding with beam-induced background measurements.

4.1 Commissioning of SuperKEKB

In order to achieve a stable operation of the new accelerator and Belle II detector, the commissioning was divided into three phases:

- **Phase 1:** The first phase in the commissioning process was the initial verification of a safe environment for rolling in the Belle II detector. At this stage, the final-focusing magnets (QCS) were not in place, prohibiting collisions of the beams at the IP. Nevertheless, a tolerable radiation environment for the Belle II detector and feedback to the accelerator control room during parameter scans and optimisation were essential. Therefore, a combination of sub-detectors was used to measure and investigate the background radiation, called the BEAST II detector (Phase 1) [Lew+19]. The list of sub-detectors used is shown in Tab. 4.1.

- **Phase 2:** In the second phase, the BEAST II experiment was restructured and the Belle II detector was moved to the final position. With the installation of the QCS focusing magnets, the main focus was on the first collisions and a radiation safe environment for the detectors, especially the VXD located closest to the IP. The BEAST II experiment in Phase 2 configuration [Lip+21] provided measurements to ensure a safe environment for the VXD installation. The set-up of this experiment involving the FANGS sub-detector is described in more detail in Sec. 4.2.

- **Phase 3:** The last phase involves the ongoing operation of the final Belle II detector, as described in Sec. 2.2. The beam currents are steadily increased while reducing the size of

the beam spot at the IP following the nano-beam scheme (described in Sec. 2.1.1) until the SuperKEKB design instantaneous luminosity of $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ is reached.

Detector	Type	#	Provided measurements
PIN	PIN diodes	64	Instantaneous dose rate at many positions.
Diamond	Diamond sensors	4	Near-IP fast dose rate, beam abort prototype.
Crystal	CsI(Tl), CsI, LYSO crystals	6,6,6	Electromagnetic energy spectrum, injection backgrounds.
BGO	BGO crystals	8	Electromagnetic dose rate.
CLAWS	Plastic scintillators	8	Injection backgrounds.
^{3}He	^{3}He tubes	4	Thermal neutron rate.
TPC	Time Projection Chambers	4	Fast neutron flux and directionality.
QCSS	Plastic scintillators	4	Charged particle rates, prototype for Phases 2 and 3.

Table 4.1: Overview of all detector components in Phase 1. From [Lew+19, p. 7].

4.2 BEAST II experiment (Phase 2)

The BEAST II experiment in Phase 2, like its predecessor in Phase 1, was an important step for the commissioning of the SuperKEKB accelerator. After the upgrade of the accelerator and the associated installation of the final-focusing magnets, the experiment served as a feedback system for the accelerator team, especially monitoring the background rates in the allocated space of the VXD.
During operation, beam-induced and luminosity-related machine backgrounds, as described in Sec. 2.3, impact the performance of the innermost sub-detectors with respect to particle tracking. Accordingly, two effects have a significant impact on the detection capabilities:

1. *High occupancy*: The increase in luminosity results in an increase in events originating from the collisions, also known as *pile-up*. The resulting rise in background radiation causes additional hits in the detector layers and consequently complicates, for example, the particle track reconstructions. Moreover, the particle rate can exceed the occupancy limit, leading to data loss of individual sub-detectors. For the PXD, this occurs for hits generated continuously in 3 % of all pixels (see Sec. 5.2.3).

2. *Radiation damage*: In the innermost layers consisting of silicon detectors, the exposure to non-ionising and ionising radiation leads to bulk and surface damage, respectively. Particularly for the inner layers, surface damage is the main factor changing the behaviour of the sensor, damaging or even destroying it [Sch+20, p. 3]. Furthermore, a high integrated dose can damage readout electronics placed close to the sensor material.

To reduce the described effects, an optimisation of the beam parameters and collimator settings is necessary.

The BEAST II experiment provided dedicated radiation detectors to monitor the effects of accelerator parameter changes on the VXD volume during commissioning. Measurements of time-resolved hit rates, spatially resolved hit distributions as well as energy and dose measurements were performed by the detectors. As part of the experiment, a segment of the two-layer PXD and the four-layer SVD was deployed. A detailed description of the PXD and the SVD is given in Sec. 2.2. The rest of the volume is occupied by the dedicated detector systems *FANGS*, *CLAWS* and *PLUME*. The layout of the VXD volume in Phase 2 is depicted in Fig. 4.1.

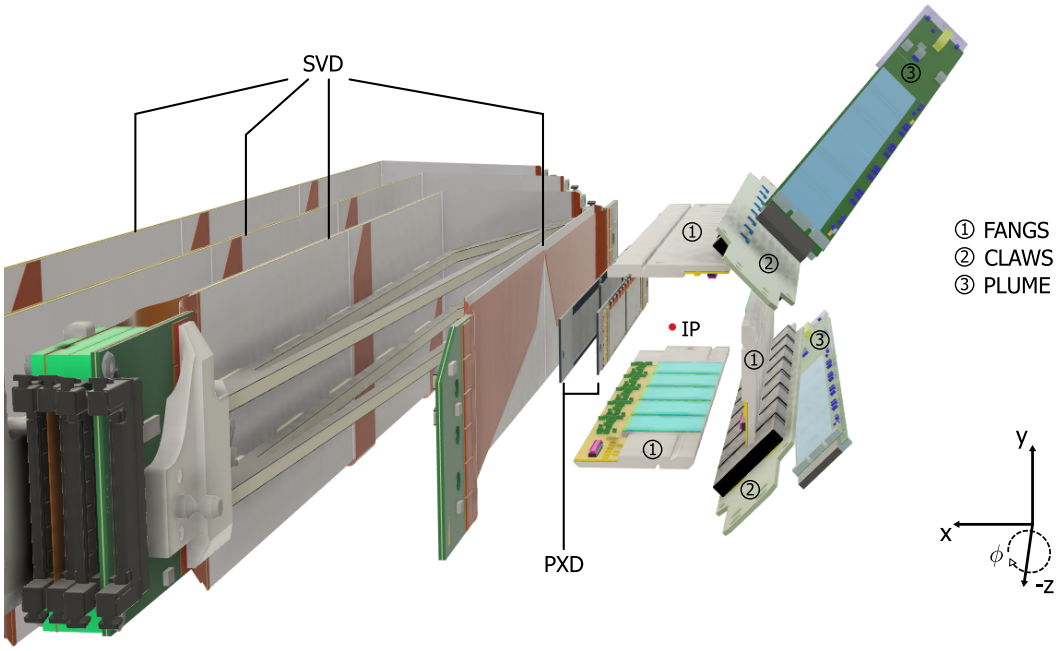


Figure 4.1: Layout of the sub-detectors in the BEAST II experiment without auxiliary structures. In the VXD volume, two layers of PXD and four layers of SVD are installed. Three dedicated detector systems FANGS, CLAWS and PLUME cover the remaining space around the IP. Adapted from [Ack16].

A brief description of the individual sub-systems is given below:

FANGS: At a radius of 22 mm and at azimuthal angles of $\phi = \{90°, 180°, 270°\}$, three FANGS staves are installed. Five hybrid pixel detector modules, as described in Sec. 3.2, are mounted on each of the staves, using the FE-I4 readout chip of the ATLAS IBL [Col12]. Due to the properties of the readout chip and the use of 245 µm thick silicon sensors, FANGS can be exposed to high hit rates and is sensitive to photon energies in the range from 10 to 60 keV. The FANGS detector is described in detail in Sec. 4.3.

CLAWS: The sCintillation Light And Waveform Sensors (CLAWS) detector provides time-dependent measurements of charged particles in a sub-nanosecond range [Win21]. Using plastic scintillator tiles combined with Silicon Photomultiplier (SiPM) readout, it can measure the time evolution of injection-induced backgrounds with regard to the bunch revolution in the accelerator rings. An elongated PCB houses eight CLAWS modules, each using scintillator tiles with a volume of $20 \times 20 \times 3\,\mathrm{mm}^3$. In the resulting gaps between the FANGS staves, two CLAWS units are placed in 135° and 225° in ϕ around the IP.

PLUME: The Pixelated Ladder with Ultra-low Material Embedding (PLUME) detector includes two double-sided ladders equipped with CMOS pixel sensors on both sides [Cue+20]. The MIMOSA 26 CMOS sensors feature a pixel size of $18.4 \times 18.4\,\mu\mathrm{m}^2$ and a thickness of 50 µm. Six of the sensors are mounted to each side of 2 mm thick SiC-foam. The detector monitors hit rates of charged particles. Furthermore, the two layers of sensors on a single ladder can be used to study particle tracks originating from the IP. In total, two ladders are integrated in the VXD volume. The first ladder is located behind the CLAWS module ($\phi = 225°$) at a radius of 5 cm. The second ladder is positioned at $\phi = 135°$, but is slightly tilted (18° with respect to the beam axis), allowing for a scan of hit rates caused by background at various radii.

Diamonds: In total, 28 single-crystal Chemical Vapour Deposition (sCVD) diamond sensors measure the instantaneous and integrated dose that is received at various positions along the beam pipe [Lic17]. Eight sensors are placed in the forward and backward region close to the IP. The reading of the instantaneous dose is used for transmitting an interlock signal to abort the beams of the accelerator in the event of an increasing dose or sudden background spikes ($\gtrsim$4 mrad in 10 µs), e.g. beam losses in the VXD volume.

TPC & Helium-3 tube: In addition to the systems in the inner volume, two additional detectors are placed in a reserved space for patch panels and cables outside the VXD volume, called VXD dock space. Eight gas-filled Time Projection Chambers (TPCs) measure fast neutrons via scattering with ionised gas nuclei [Sch+21]. The system creates 3 D images of reconstructed neutron interactions. Finally, one Helium-3 tube is placed to measure thermal neutron rates [Jon+17].

4.3 FANGS detector

The centrepiece of the FANGS system is the hybrid pixel detector module mounted on an aluminium bar, called *stave*. The hybrid module consist of an n^+-in-n planar silicon sensor as sensing material combined with the FE-I4 readout chip (see Sec. 3.2.2). The modules have an overall dimension of $18.8 \times 20.2\,\mathrm{mm}^2$.
On each FANGS stave, five modules are attached using a heat-conducting glue to transfer the heat produced by the FE-I4 to the aluminium carrier of the stave. By attaching the staves to

the PXD Support and Cooling Block (SCB), the heat can be removed. A picture of a FANGS stave is shown in Fig. 4.2. The connection point for supplying power, sending configurations

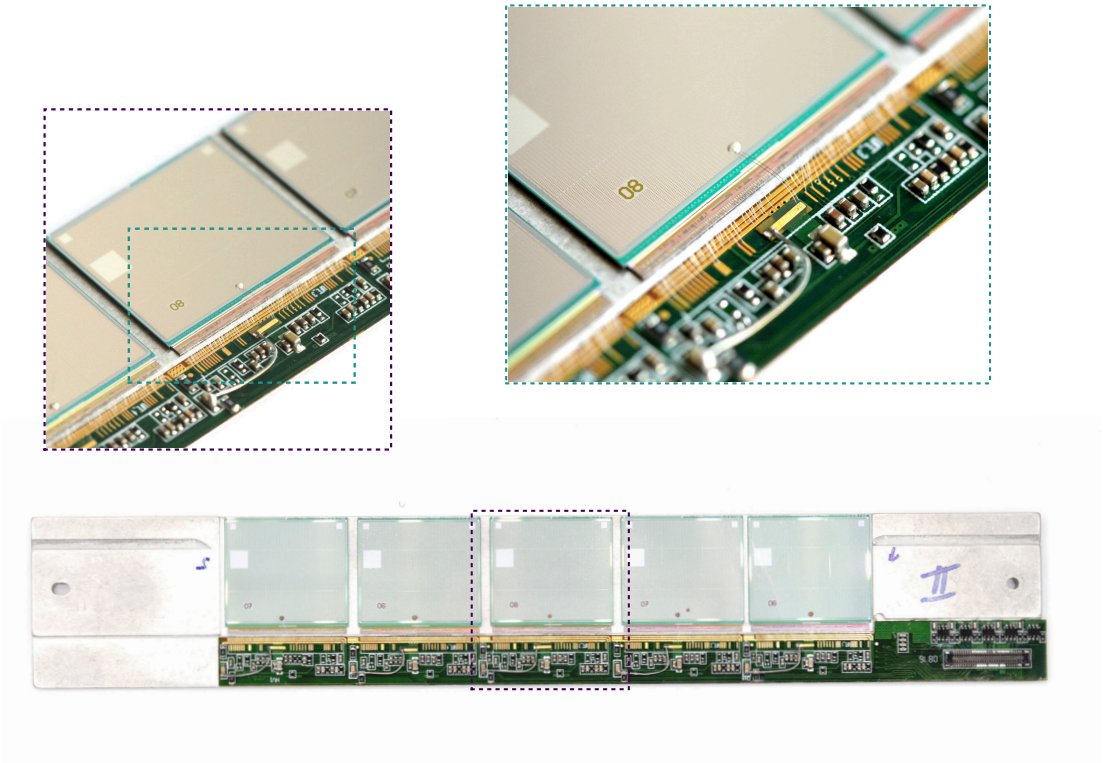


Figure 4.2: Photograph of a FANGS stave with its five hybrid pixel detector modules and the flex for data transmission. The stave has a size of $17.2 \times 2.9\,\mathrm{cm}^2$. In the two magnifications, the hybrid pixel detector module and the connection between flex and FE-I4 using wire bonds are depicted. The aluminium wires have a diameter of 25 µm.

and transmitting data is a customised flexible printed circuit board (*flex*) on the bottom of the stave. The hybrid pixel detector modules are connected to the flex using wire bonding. The link to the back-end electronics is established via a 60-pin connector at the end of the stave region. In addition to passive components such as resistors and capacitors, the flex contains five active components close to the connector, namely the Low-Voltage Differential Signalling (LVDS) drivers [Tex03]. The driver converts the single-ended HitOr signal of the FE-I4 (described in Sec. 3.2.2) into a differential signal ensuring the signal integrity over a total cable distance of 18 m from the FANGS stave to the readout board. Further details on the set-up can be found in [Ahl16].

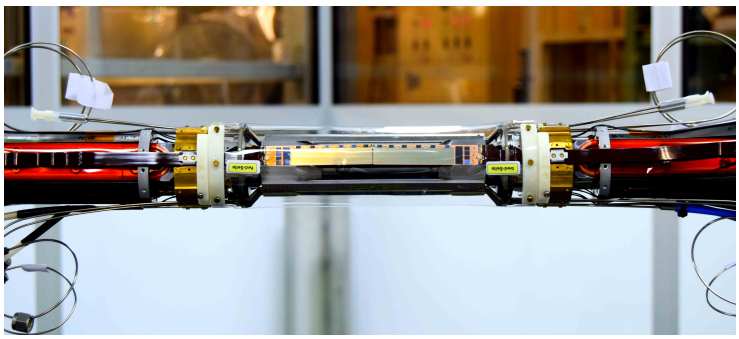
4.4 Integration process

In a cleanroom environment, the BEAST II sub-detectors were integrated sequentially into the VXD volume. A summary of this assembly sequence is given in the following.

1. In the first step, the beam pipe covering the area around the IP was prepared and aligned on a shockproof table, see Fig. 4.3a. Diamond sensors were placed behind the cooling manifold in the forward and backward directions.

2. The two PXD layers, corresponding to four modules, were attached to the SCBs. The modules cover the region at $\phi = 0°$ direction, as can be seen in Fig. 4.3b.

(a) Beam pipe and diamond sensors.



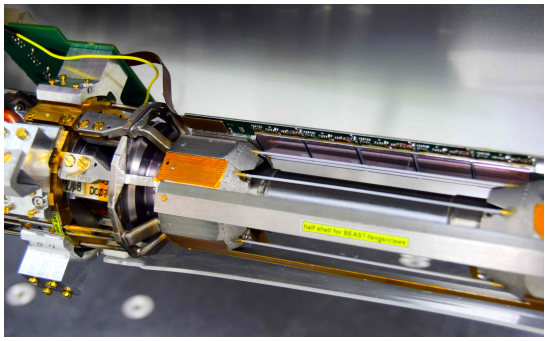
(b) SCB and PXD installation.

Figure 4.3: Four PXD modules mounted to the SCB surrounding the beam pipe. The inner layer is covered by the two modules of the outer layer.

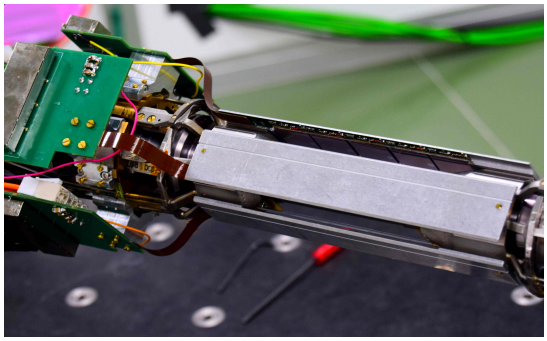
3. The FANGS staves were attached to the SCBs on both sides, starting with the stave in the 90°-direction in ϕ, see Fig. 4.4a. Afterwards, the remaining staves were attached at 180° and 270° in ϕ. The assembled FANGS detector is shown in Fig. 4.4b.

4. The emerging gaps in the acceptance region ($\phi = \{135°, 225°\}$) were covered by two CLAWS ladders. Since the SiPMs do not require active cooling, the CLAWS ladders were mounted outside the SCBs. The installed CLAWS detector is shown in Fig. 4.4c.

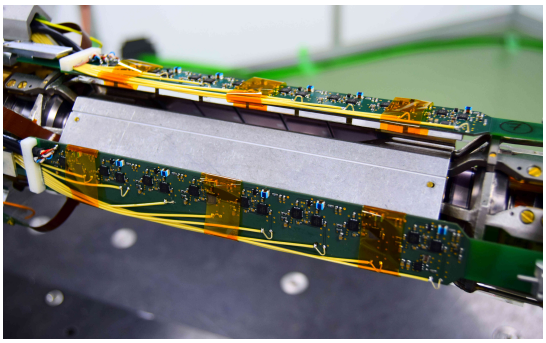
5. The PLUME detector was placed behind the CLAWS ladders ($\phi = \{135°, 225°\}$). The picture in Fig. 4.4d illustrates the special arrangement of one PLUME ladder mounted at an angle of about 18° relative to the CLAWS ladder.



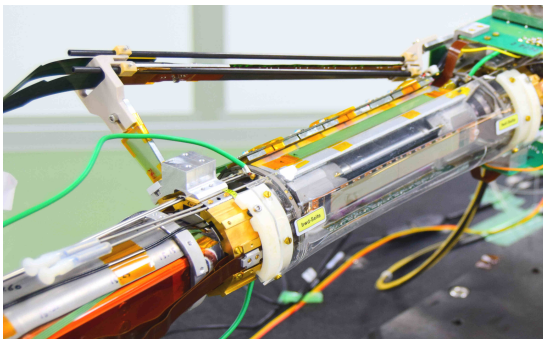
(a) First FANGS stave mounted.



(b) Installation of all FANGS staves.



(c) CLAWS integration.



(d) Placement of one PLUME ladder.

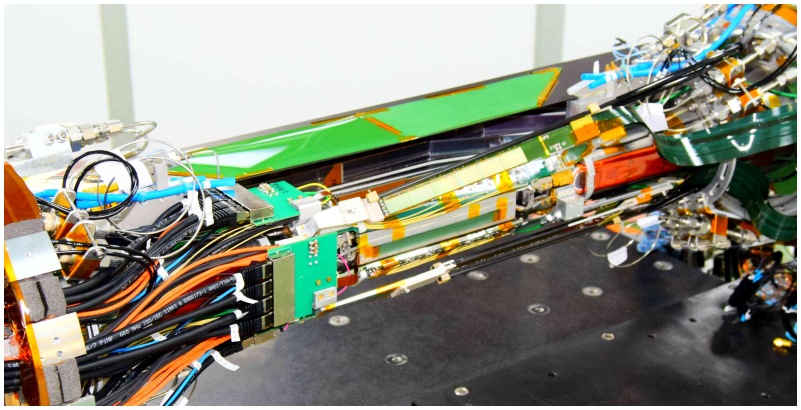


Figure 4.5: Completed assembly of the BEAST II sub-detectors within the VXD volume. The SVD cartridge is mounted behind the PXD and contains four layers of SVD.

4.5 Slow control and monitoring system

An important task in the operation of individual sub-detectors is the synchronisation of control and data output originating from the systems. For this reason, the Experimental Physics and Industrial Control System (EPICS) [EPI] is utilised. It is an open-source project that is used by several research facilities in high-energy physics. In a network of systems, EPICS can be used to send information and receive it on multiple computers, simultaneously. In the scenario of the BEAST II experiment, all sub-detectors provide the processed and analysed data to the Belle II and SuperKEKB control rooms via the EPICS network. This allows for quick feedback when tuning the accelerator. The communication between the connected hardware and the network is controlled via Input Output Controllers (IOCs) [Sch+20, p. 59]. An IOC generates Process Variables (PVs) that are equipped with observables and can thus be retrieved via the network. Furthermore, values can be set in certain PVs which can be used to control devices or change their status, referred to as *slow control*. In addition, PVs can carry further information, e.g. the unit of the measured value or a limit of the value to be set.
In the implementation of the system connected to the FANGS detector, PCASpy [Ins] is used, a high-level abstraction to simplify the creation of EPICS IOCs. The features of the IOCs can be summarised in two main aspects:

- Monitoring system to display data from current recordings of the detector and temperature measurements of the environment.
- Additional control and monitoring of the power supply system.

The IOC for transmitting the recorded data is directly connected to the raw data interpreter output. In this stage, hit rates can be determined and hit maps can be created. The refresh rate of the PVs is set to one second.
A Graphical User Interface (GUI) is provided by the Control System Studio (CSS) [CSS]. It can be used to create individual widgets supporting the monitoring and changing values of PVs. Pictures of the FANGS widget are depicted in Fig. 4.6 and Fig. 4.7. The slow control allows for remote control and provides real-time data for the accelerator team in dedicated machine studies. Additionally, the data is stored locally by the FANGS system for offline analysis.

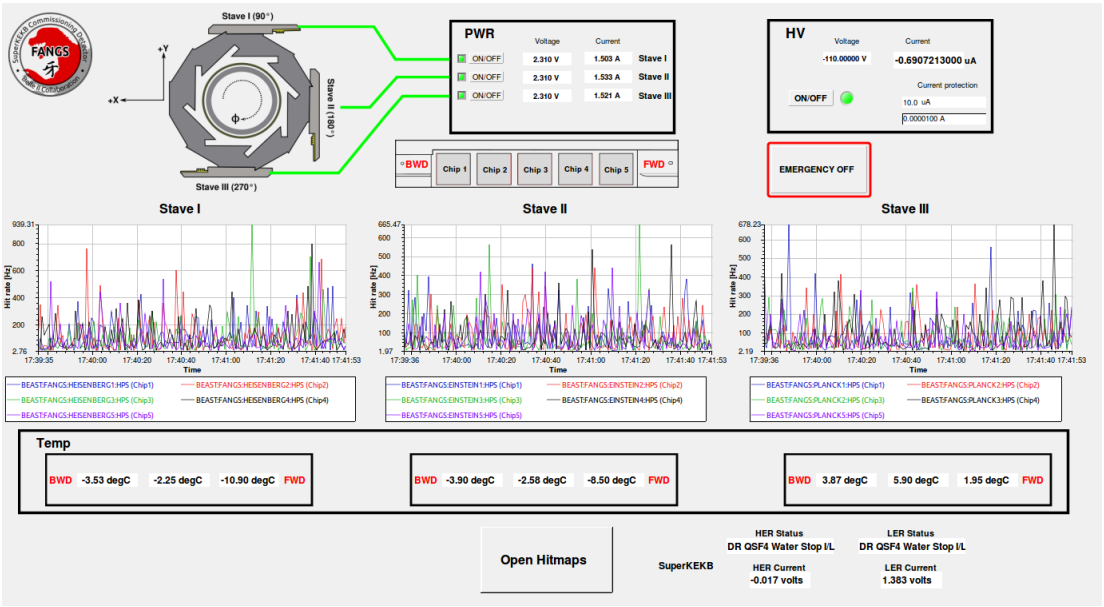


Figure 4.6: CSS widget of the FANGS detector. *Upper part*: Status of the power supplies with the possibility of value inputs. The system can be shut down with an *emergency off*. *Middle part*: Hit rates of all detector modules with a refresh rate of one second. *Lower part*: Temperature measured on the back of the FANGS stave and a tab button to display hit maps.

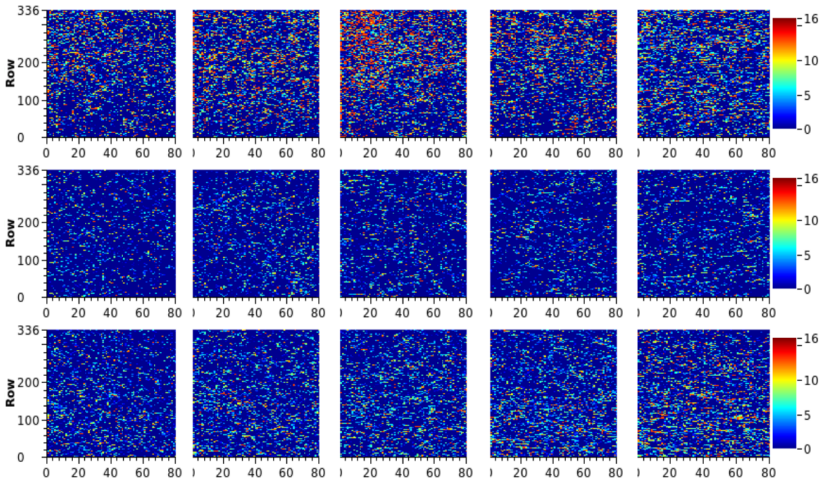


Figure 4.7: Section of the CSS widget showing the hit maps of the hybrid pixel detector modules on the FANGS staves during accelerator operation (screenshot from the SuperKEKB control room).

4.6 Beam-induced background studies

With the pixelated modules, the FANGS detector was able to record hit rates as well as the spatial distribution of detected particles. Furthermore, using the charge measurement capabilities in the FE-I4 and the enhancement by the *TDC method* (described in Sec. 3.2.2), it provided an energy measurement of the radiation to which the FANGS detector is sensitive. During the commissioning in Phase 2 from *March* to the end of *July 2018*, the FANGS detector continuously recorded data and provided it to the SuperKEKB and Belle II control rooms. The following analyses are based on a subset of data stored during the operation of the BEAST II experiment.

4.6.1 Hit-rate measurements

The recordings of the rate of traversing particles provide essential information for SuperKEKB commissioning and tuning of beam parameters. In order to reduce the complexity of optimising the accelerator for operation and to identify the effects of changes in the tuning procedure, *single-beam studies* are carried out. In these scans, the beam is operated in either HER or LER and effects of parameter changes are detected in the particle rates and doses of the BEAST II detectors. The three FANGS staves are used to record the hit rates occurring around the IP ($\phi = \{90°,180°,270°\}$). Fig. 4.8 shows the hit rate during a LER study recorded with a module on the stave in $\phi = 180°$ direction.

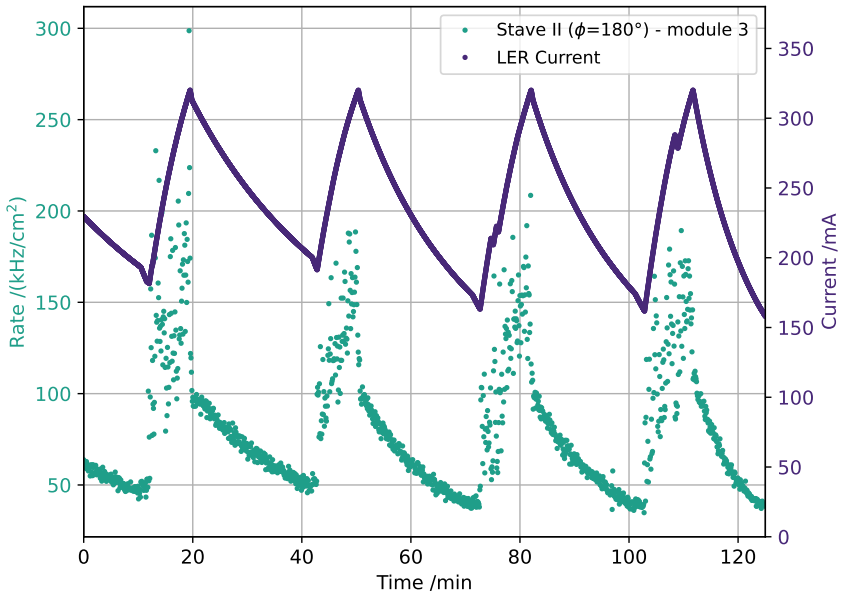


Figure 4.8: Hit rate measured with the centre module ($\phi = 180°$) on the FANGS stave during a LER beam study. The rate is scaled to the module area of $\sim 3.43\,\mathrm{cm}^2$.

The measurement shows an increase in the particle rate especially during the injection into the LER. During this period, the beam current is increased from 160 to 320 mA with an injection rate into the positron bunches of 12.5 Hz. The hit rate after injection follows the decay of the beam current, decreasing by 50 % within 20 min. The observed increase in background radiation is caused by the injection of particles into the bunches of the beam, resulting in a disturbance of the bunch orbit [Lew+19, p. 118]. Consequently, the background radiation increases once these noisy bunches pass the IP. The orbit recovers with each revolution in the ring of 10.0614 µs, referred to as *cooling time*. High time resolution measurements with the CLAWS detector in single-beam studies result in an injection-induced signal of up to 11 ms and 20 ms after injections for LER and HER, respectively [Win21, p. 88]. With regard to the final operation of the accelerator, in which the beam currents are kept constant over time using a continuous injection rate of 50 Hz, an important task is to tune the injection to achieve a tolerable level of background radiation. Based on the results, a major task in the commissioning of the accelerator is the optimisation of the injection process.

Spatially resolved hit distribution

The 2 D information about the pixel hit location is presented in so-called hit maps. For the FANGS detector, these hit maps are combined to obtain the spatial distribution of particle detections. Fig. 4.9 shows the hit maps of all FANGS modules combined.

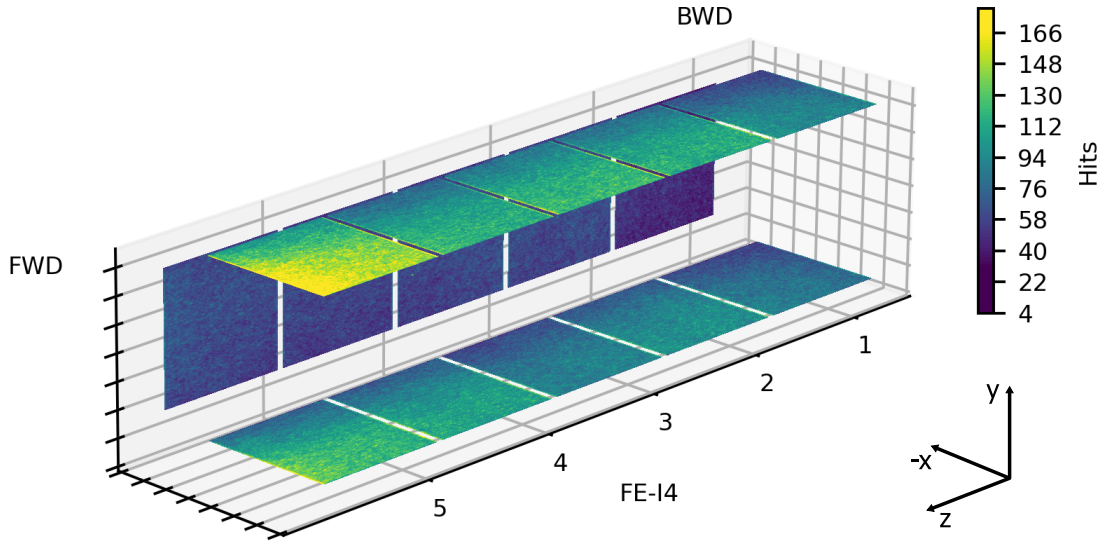


Figure 4.9: Perspective view of hit maps recorded by the FANGS detector.

Based on the hit maps obtained in a single-beam study, the highest activity is registered in the vertical FANGS staves. Furthermore, the hit rate is largest in the forward direction and

increases in the $+x$-direction where the PXD modules are located.
However, by constantly adjusting the setting of the accelerator to improve the performance of the operation, the appearance of the hit maps varies. Fig. 4.10 shows the hit maps of the FANGS stave attached in -x-direction ($\phi = 180°$) during HER injection tuning .

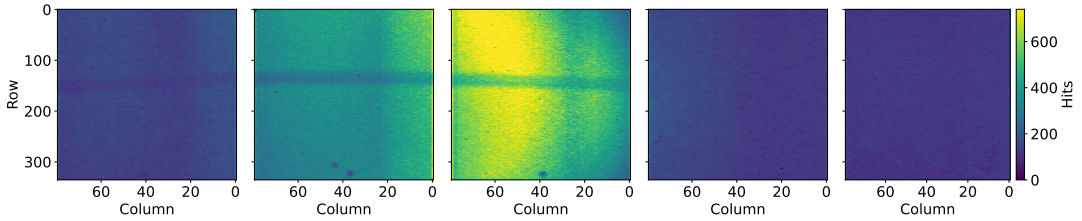


Figure 4.10: FANGS hit maps of the stave in -x-direction recorded during HER injection tuning on *July 14, 2018*.

A significant accumulation of hits is observed predominantly in the centre region of the stave. In addition, a curved hit pattern is formed. To further investigate the nature of the detected particles, the charge deposition in the sensor and the resulting hit cluster sizes are considered in Fig. 4.11. Therefore, the results of the centre module (module 3) are compared to the outermost module (module 5).

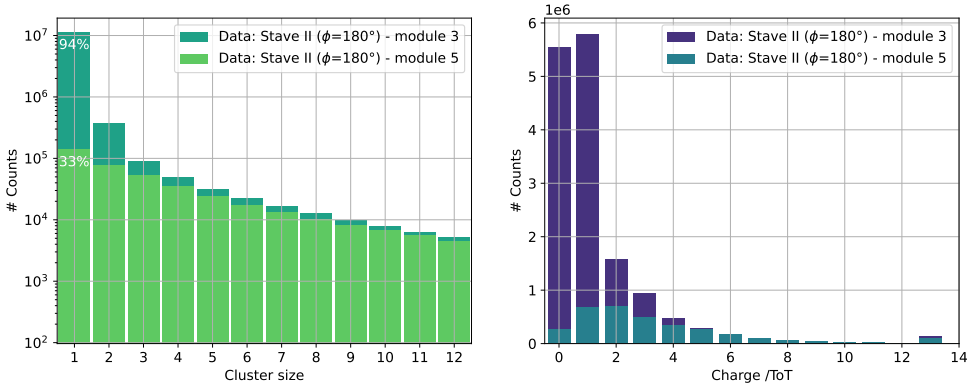


Figure 4.11: Histogram of cluster sizes (*left*) and charge distribution in units of ToT (*right*) for modules 3 and 5 on the stave in the -x-direction.

The cluster size distribution of the central module reveals a high occurrence of particle registration within a cluster size of 1 (94 % of all sizes). In the outer module, the effect is less apparent and the proportion is lower at 33 %. The charge deposition in single pixels indicates the enhanced detection of photons. Furthermore, the charge measurement yields a clear enhancement

in the two lowest ToT values, indicating low-energy photons. A determination of the energy is performed in Sec. 4.6.2.

Comparable to the observations of the FANGS detector, a similar hit pattern has been recorded by the PXD in Phase 3 [Liu+; Spr+20]. During the HER single-beam operation, large radiation background was observed in modules in -x-direction after changing the beam optics ($\beta_x^* = 80\,\text{mm}$ to $\beta_x^* = 60\,\text{mm}$). The origin can be explained by backscattering of synchrotron radiation and is illustrated in Fig. 4.12.

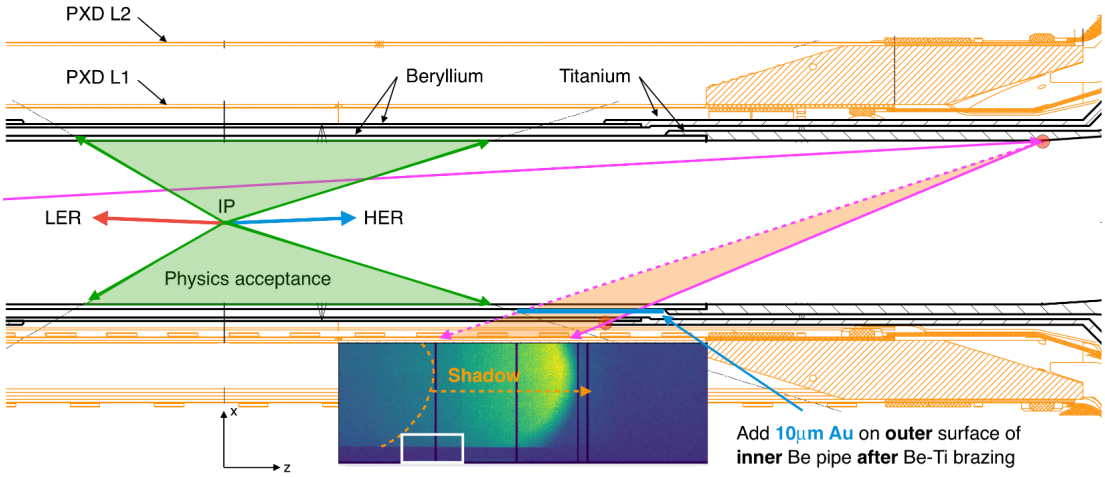


Figure 4.12: Cross-section of the beam pipe with the two layers of PXD covering the acceptance during Phase 3. Synchrotron radiation is reflected from the titanium (Ti) part of the beam pipe and results in the hit map shown below in the PXD module in -x-direction. The dark area at the edge of the hit map is caused by the partial overlap with an adjacent module. From [Liu+].

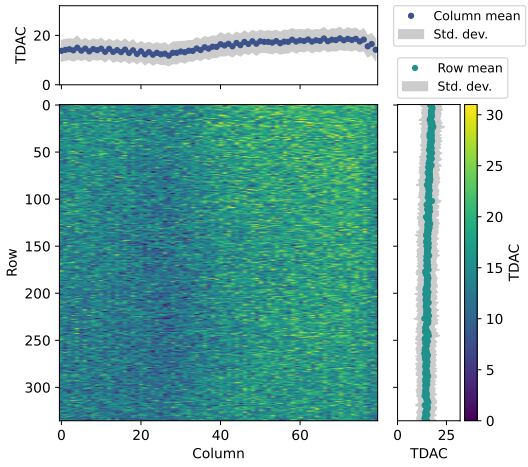
The electron beam in the HER emits synchrotron radiation into the interaction region. In the shape of synchrotron radiation fans [Wil00, p. 40], the photons hit the titanium part of the beam pipe in the $+x$-direction. A portion of the backscattered photons can penetrate the beryllium beam pipe and reach the innermost detector. Alternatively, the photons induce fluorescence in the gold coating of the beam pipe, leading to photons emitted perpendicular to the beam axis and reaching the detector [Lip+21, p. 14]. The curved pattern in the hit map is due to the shape of the titanium part where photons are reflected and subsequently hit the flat detector material. Furthermore, a shadow in the hit map is caused by the titanium material in -x-direction.

Consequently, the observed effect in the FANGS detector in Phase 2 originates from the generation of synchrotron radiation. In Phase 3, the backscattering of photons was reduced by adjusting the HER orbit and setting β_x^* to 80 mm. Nevertheless, focused radiation on the PXD modules can degrade the track reconstruction efficiency as well as lead to inhomogeneous irradiation effects [Wan+22]. To improve the shielding of the detector, an adapted beam pipe with slightly modified geometry and additional gold layers (see Fig. 4.12) will be installed

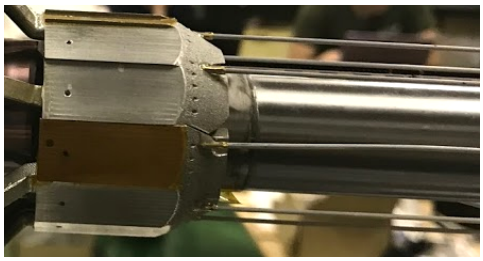
in 2023 [Nat+22, p. 14].

Together with the observation of synchrotron radiation in the hit maps in Fig. 4.10, two additional patterns are noticeable which are described below.

1. Dark vertical band: This band, which occurs in each of the detector modules, is caused by the threshold tuning procedure of the FE-I4 readout chip. The aim of tuning is to produce the most uniform response possible from all pixels to an injected signal using the integrated charge injection circuitry. One mechanism of tuning is the individual shifting of the threshold DAC (*TDAC*) per pixel. The TDAC settings for pixels of a single module after tuning are shown in Fig. 4.13a. Comparable to the dark vertical band, the noticeable columns are set to a lower average *TDAC* value. This local deviation could be caused by the position of the internal charge injection voltage (PlsrDAC) generation. From column 26, the voltage is distributed to the pixels via metal lines resulting in position-dependent impedances. The effect is described in detail in [Poh20, p. 112].
   Consequently, lower *TDAC* values are caused by higher charges injected into these pixel during threshold tuning. Further measurements indicate that the range of individual pixel thresholds is over 400 electrons after tuning [Poh20, p. 113]. In the case of photons generating charges in the sensor close to the threshold, this effect of tuning may become visible, since charges below the threshold in the affected columns are not registered by the readout chip.



(a)



(b)

Figure 4.13: (a) *TDAC* distribution of the FE-I4 readout chip after tuning. The upper and right plot show the column and row mean value, respectively. (b) Photo of the SCB with connected carbon tube after dismantling the BEAST II experiment. The bending of the tube is apparent.

2. Dark horizontal curved band: The horizontal band is created by one of the eight aluminium coated carbon fibre tubes connecting the SCBs on both sides. With an outer diameter of 1 mm, they feature small holes to support the cooling of the innermost detector layer with the supply of N_2 [Ye+18, p. 83]. The material of the tubes might cause the absorption of low-energy photons resulting in the reduction of recorded hits in the detector area behind the tube. Furthermore, the slight curvature of this pattern can be explained by the picture in Fig. 4.13. The photograph shows the SCB and carbon tube after de-installation of the BEAST II experiment. A slight undesired bending of this tube is recognisable.

The two effects described above support the hypothesis of low-energy synchrotron radiation in the innermost VXD volume recorded with the FANGS detector. Continuous irradiation by ionising radiation, which particularly affects the PXD, requires optimisation of the sensor to compensate for the inhomogeneous influences and may also reduce the lifetime of the detector [Sch20, p. 109].
To gain further insights into the characteristics of synchrotron radiation in Phase 2, the next section deals with the charge measurement to increase the energy resolution.

4.6.2 Charge measurement

The charge resolution of the FANGS detector is improved by using the *TDC method*, as described in Sec. 3.2.2. For this purpose, the charge signal is sampled with a 640 MHz clock instead of the usual 40 MHz. The clock is provided by the readout board, which receives the *HitOr* output carrying the largest charge signal of all pixels. To further obtain a conversion from the measured TDC values to charge and finally to energy, further steps involving calibrations are necessary. The required steps are briefly described below and explained in detail in [Ahl16, p. 31].

1. *Tuning*: To obtain an accurate charge reconstruction, the pixels are tuned to produce a uniform threshold and charge response. The tuning can be performed using the internal charge injection or the *baseline tuning* (explained in Sec. 4.6.2).

2. *HitOr calibration*: After each tuning and before charge measurement, a HitOr calibration is necessary. In this calibration, the response of ToT and TDC is recorded for a range of PlsrDAC values per pixel. Due to changes in threshold and DAC settings caused by tuning affecting the ToT/TDC response, this calibration has to be performed for an accurate conversion from TDC to PlsrDAC.

3. *PlsrDAC calibration*: In the PlsrDAC calibration, a conversion of charge in PlsrDAC to an equivalent charge in units of eV is carried out using radioactive sources. Due to the well-known gamma energies, a relation between PlsrDAC and eV is determined. Consequently, a linear transfer function is created and used for the individual FE-I4 readout chips. For the modules used in the FANGS detector, this calibration was carried out within the scope of my master's thesis [Ahl16].

The steps and their results are described in the next sections. In the TDC measurement, the HitOr signals serve as a trigger for the data readout of the respective module on the FANGS staves. To avoid exceeding the maximum trigger frequency of the FE-I4 of 200 kHz [Gar+11, p. 10] at the given hit rates, only a small area of the pixels is activated (16×11 pixels). Nevertheless, for charge reconstruction it has no effect except for the condition on sufficient statistical precision.

Baseline tuning

Early energy measurements in Phase 2 demonstrated an insufficiently low threshold by tuning with the internal charge injections to fully resolve the low energy spectrum. Therefore, the following measurements were performed with a preceding *baseline tuning* [Jan17, p. 4].

In this algorithm, the lowest possible threshold for the detection of signals is achieved by constantly comparing the recorded noise hits in the pixels to a chosen hit rate during the tuning. The noise is part of the ideally flat output signal of the CSA without any further charge flowing through the readout pixel. The basic principle involves two loops, one outer and one inner, which set the threshold by using the global DAC (*GDAC*: rough setting) and the local threshold DAC per pixel (*TDAC*: fine adjustment), respectively. Initially, the starting point of the loops is the highest setting of *GDAC* and the lowest setting of the *TDAC*. With each iteration of the loops, *GDAC* is reduced and a suitable *TDAC* value is found meeting the noise hit requirements. Pixels that still show noise at the highest *TDAC* value in the inner loop are disabled. The procedure continues until a set limit of disabled pixels is reached. [Jan17, p. 4]

The advantage of this tuning procedure is the independence of the internal charge injection circuits.

HitOr calibration

After tuning, the response of the TDC method to the internal charge injection is determined, called *HitOr calibration*. The result of the HitOr calibration for the 176 activated pixels is shown in Fig. 4.14. The curve describes the measured TDC value depending on the injected charge in units of PlsrDAC. Moreover, an existing offset (TDC value of $\sim$50) is noticeable for the setting of 0 PlsrDAC. At this value, charges are injected into the analogue pixel cells and result in measurable TDC values. This effect has already been noticed in measurements with the FE-I4 but is of unknown origin [Poh20, p. 112]. Accordingly, the injection circuits are incapable of generating sufficiently low charges to reach the set threshold limiting the conversion from TDC to PlsrDAC. Missing values of the stepwise injections are interpolated with a 1 D function, resulting in a look-up table for each calibrated pixel.

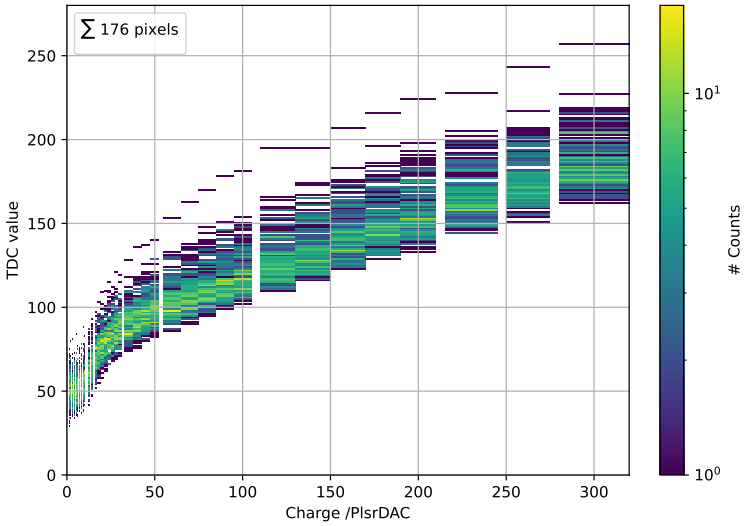


Figure 4.14: Per-pixel HitOr calibration for 176 activated pixels using 500 injections per PlsrDAC value. As a result, the TDC values are obtained as a function of PlsrDAC.

TDC measurement

The charge measurement using the TDC method was performed during a HER beam study on *July 7, 2018* and is shown in Fig. 4.15. The two distributions show the recorded TDC

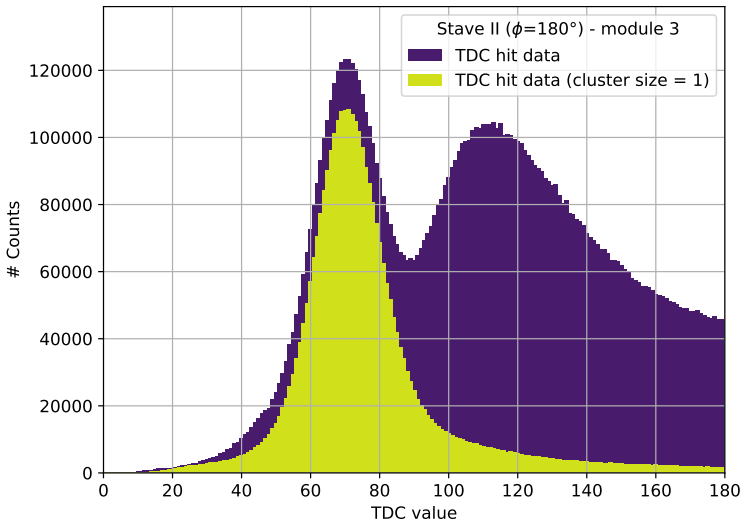


Figure 4.15: Charge measurement using the TDC method. The charge distributions without restriction of cluster size (*dark blue*) and with the condition of cluster size 1 (*yellow*) are shown.

values for HitOr signals originating from cluster size ≥ 1 and from single-pixel clusters (cluster size $= 1$). Without restriction to the cluster size, the so-called *seed pixel* (pixel with the highest charge in the cluster) is obtained. In the seed pixel distribution, a prominent peak appears around TDC values of 70 followed by a Landau-shaped distribution. The latter suggests the energy deposition of MIPs in the detector system, as described in Sec. 3.1.1. In the single-pixel cluster distribution, a Gaussian distribution is visible for the first peak with slight asymmetry towards higher energies. The asymmetry could be explained by MIPs producing only single-pixel clusters. Consequently, a recorded photon peak can be assumed. To express this measurement in physical quantities, the TDC values are converted to energy in the next section.

PlsrDAC to energy conversion

With the per-pixel HitOr calibration, the TDC values of the measurement are converted into PlsrDAC. The result for single-pixel clusters is depicted in Fig. 4.16.

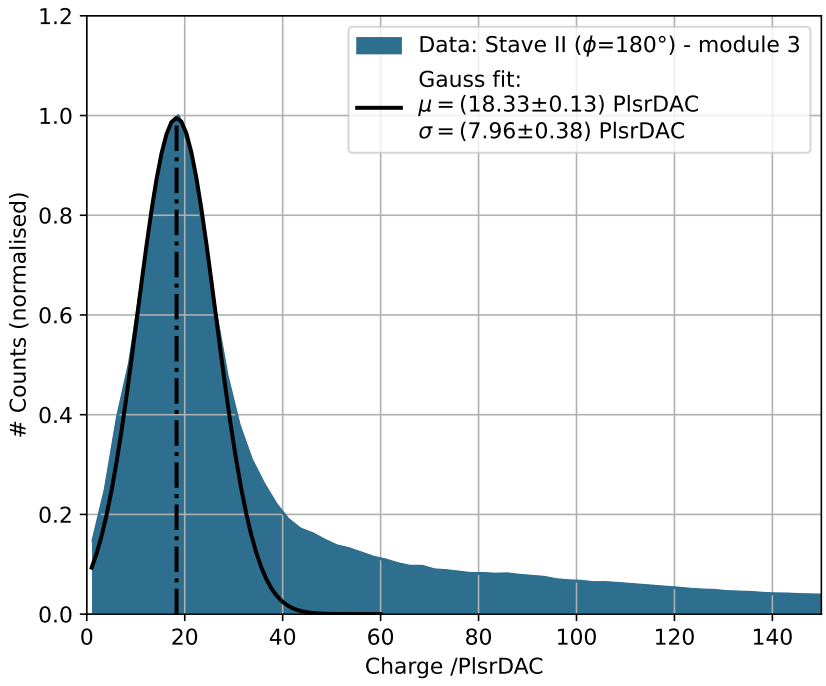


Figure 4.16: Recorded charge spectrum measured with the centre module ($\phi = 180°$) on the FANGS stave, using single-pixel clusters. For the extraction of the peak position, a Gaussian function is fitted.

The first peak resembles a Gaussian distribution with a mean value of (18.33 ± 0.13) PlsrDAC. Due to the mentioned limitation in the HitOr calibration, the peak is cut off at lower charges.

With the transfer function (stave II, module 3) determined in the PlsrDAC calibration (in [Ahl16, pp. 33-38]), the energy of the recorded peak is obtained:

$$\mu = (10.63 \pm 0.08)\,\mathrm{keV},$$

using Gaussian error propagation. The transfer functions of the individual FANGS modules are listed in Tab. 8.1 in the appendix.
A value for comparison can be obtained from the energy spectrum measured with the PXD modules in Phase 2. The innermost two modules measured a value in the range of 8.4 keV to 8.6 keV for the low-energy peak [Lip+21, p. 14].
The difference to the measured value of the FANGS detector derives from the inaccuracy of the transfer function related to the baseline tuning. Studies have shown that the transfer function from the PlsrDAC calibration deviates from the linear correlation when the baseline tuning is used [Ach17, p. 59]. For the recorded charge of 18.33 PlsrDAC, the comparison between linear and non-linear transfer function from [Ach17, p. 60] results in a $\sim$20 % deviation in the conversion to energy. As a consequence, the determined value can only be taken as a reference value with a systematic uncertainty which is higher than the stated one.

Conclusion: The BEAST II experiment with its dedicated detectors made comprehensive observations of the behaviour of the accelerator during the commissioning period and acted as a beam monitor for the accelerator team to improve the operation for the Belle II detector. The consequences of Phase 2 include [Lip+21, pp. 20-21]:

- A tolerable radiation background could be measured ensuring a safe installation environment for the VXD.
- Measurements were conducted to help the machine reducing the backgrounds from Touschek, beam-gas, injection, and synchrotron radiation.
- Thresholds of the diamond sensors were adjusted to interrupt the beam in case of excessive doses (beam loss events).
- Installation of a new beam pipe with additional gold coatings to reduce synchrotron radiation.

The BEAST II experiment was a valuable step towards the SuperKEKB accelerator goal of achieving an instantaneous luminosity of $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$.

5 The DEPFET pixel detector

The Pixel Detector (PXD) is the innermost sub-detector of the Belle II experiment and consists of an arrangement of 40 modules using DEPFET pixels (described in Sec. 3.3). Two modules are glued together to form a so-called ladder. In total, the PXD consists of 8 and 12 ladders, which are located at 14 mm and 22 mm from the IP, respectively. The PXD of the Belle II experiment has 8 million DEPFET pixels providing a high spatial resolution. The final design of the PXD is shown in the technical drawing in Fig. 5.1.

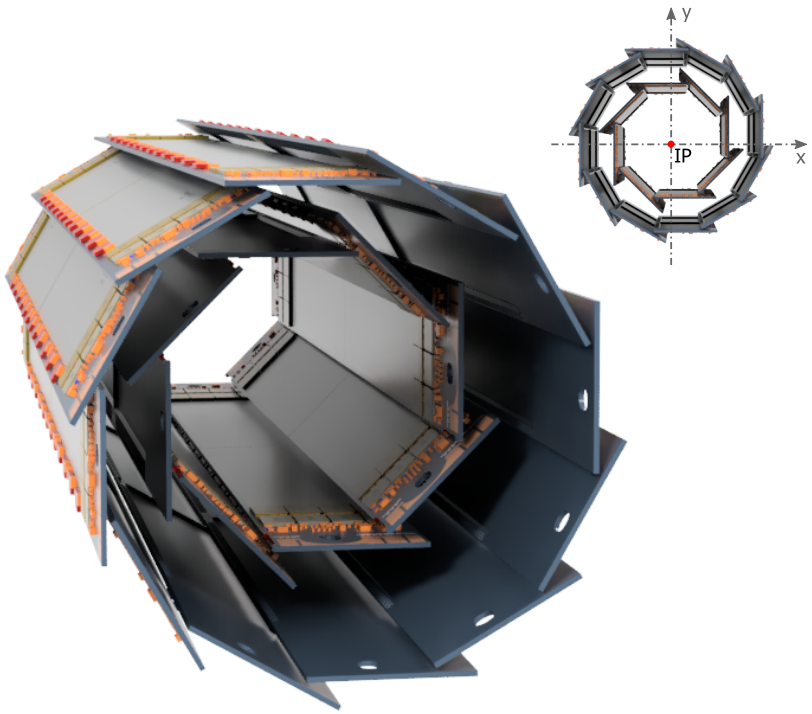


Figure 5.1: Illustration of the Pixel Detector (PXD) of Belle II in the final design configuration. Two layers enclose the beam pipe and the interaction point located inside it. Adapted from [Kit22].

The proximity to the IP can be achieved by attaching the ladders directly to the beam pipe resulting in a polar angle coverage of $17° \leq \theta \leq 150°$ [Abe+10, p. 78]. One layer of the PXD with its material accounts for only 0.21 % of a radiation length [Wie21, p. 45]. The next section focuses on the layout of a single DEPFET pixel detector module.

5.1 DEPFET pixel detector module

The PXD module is made of a monolithic piece of silicon requiring no additional support. The 75 µm thick sensor region comprises a matrix with 250×768 DEPFET pixels. A picture of the module can be seen in Fig. 5.2.

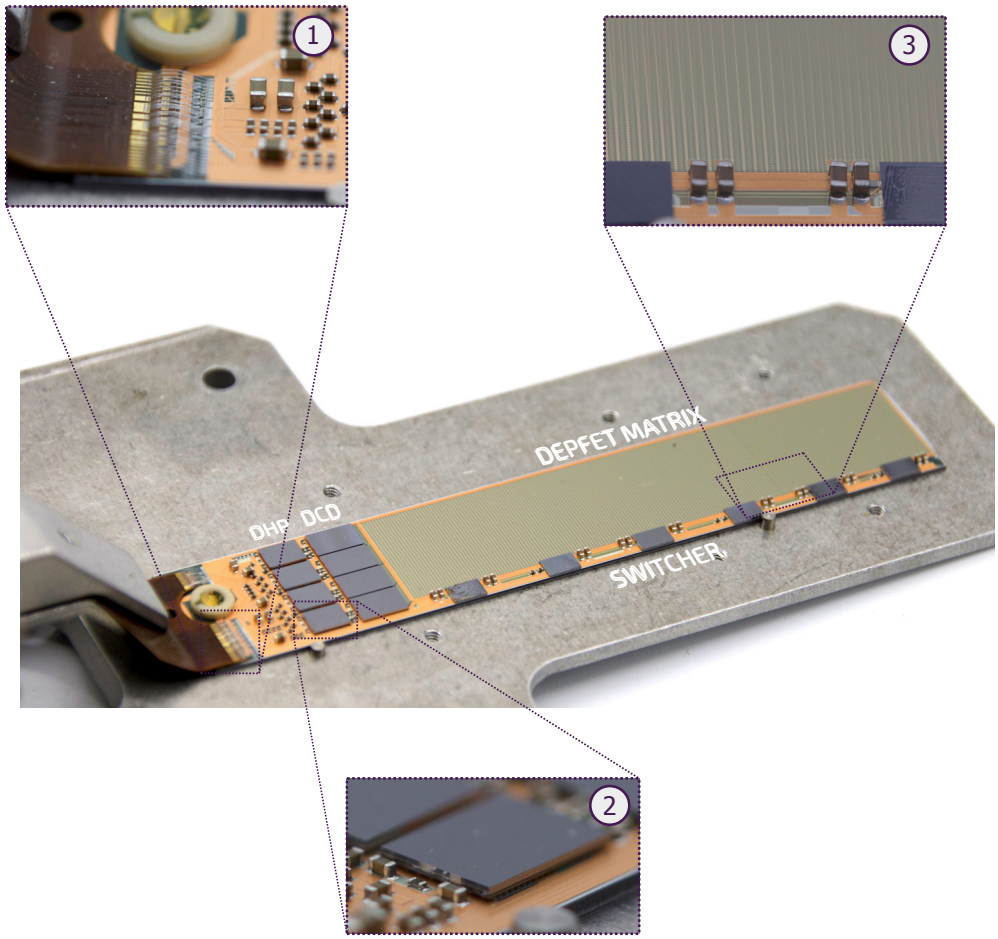


Figure 5.2: Picture of a DEPFET module attached to an aluminium jig including three magnifications. *Picture #1*: Wire bonds with a thickness of 32 µm connect the module to a flexible cable for data transfer and power supply. *Picture #2*: The ASICs are bump-bonded to the module. *Picture #3*: Transition from large pixels to small pixels on the DEPFET matrix.

In order to achieve the self-supporting structure, a 75 µm thick wafer is bonded to a handle wafer with a thickness of 450 µm in the manufacturing process [Ric+03, p. 254]. Subsequently, the DEPFET pixel implants are implemented and the handle wafer below the DEPFET matrix, which is partially thinned down to 75 µm using the etching process [PXD16, p. 29]. Due to the remaining silicon structure of the handle wafer, a support frame is created with a thickness of 525 µm.

The frame is used to place the Application Specific Integrated Circuits (ASICs) needed for the operation of the module, namely, SWITCHER, Drain Current Digitiser (DCD) and Data Handling Processor (DHP) (see Sec. 5.2). Six SWITCHERs are located on the so-called balcony, i.e. next to the long side of the sensitive area. In total, four DCDs and four DHPs are located in the End-Of-Stave (EOS) region of the module. Each of the ASICs is attached to on-module pads for signal transmission using a bump-bonding technology. In addition, SMD[1] components are placed in the EOS area and next to the SWITCHERs. A flexible cable (*Kapton flex*) is used for data transmission and power supply, which is connected to the module via 32 µm thick wire bonds.
In the design of the PXD, four different module types are categorised according to their location in the detector. The innermost layer consists of Inner-Forward (IF) and Inner-Backward (IB) modules. Analogously, the outer layer consists of Outer-Forward (OF) and Outer-Backward (OB) modules. Outer and inner modules differ in module size and pixel pitch. Opposite modules in the forward and backward direction that are glued together to form a ladder differ in the side on which the SWITCHERs are placed. Tab. 5.1 summarises the different sizes of sensitive areas and pixel pitches according to detector layer. In this thesis, measurements with an OB module are presented. A top view of this module is depicted in Fig. 5.3.

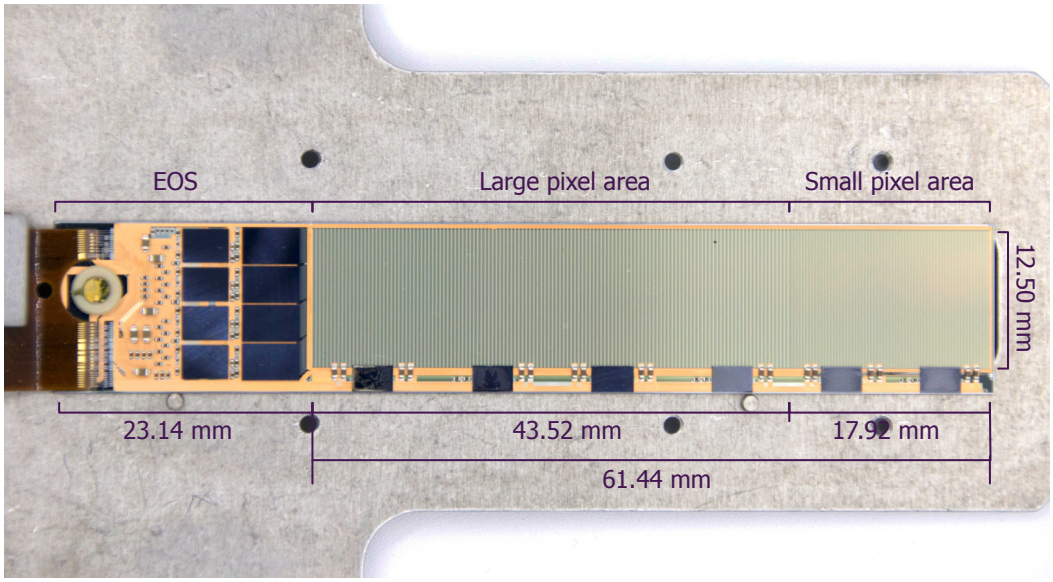


Figure 5.3: Top view picture of the OB module with its dimensions.

On a ladder, the pixels located in the central region have a smaller pixel pitch than those on the other parts of the sensor (see Tab. 5.1). This area has the shortest distance to the IP and thus measures a larger number of charged particles per area that pass through the detector layers at

[1] Surface-Mount Devices, e.g. resistors and capacitors

a small incident angle. The small pixels are beneficial to provide a high spatial resolution.

Type	Sensitive area	Large pixel pitch	Small pixel pitch
Inner modules (IF and IB)	$12.50 \times 44.80\,\mathrm{mm}^2$	$50 \times 60\,\mu\mathrm{m}^2$	$50 \times 55\,\mu\mathrm{m}^2$
Outer modules (OF and OB)	$12.50 \times 61.44\,\mathrm{mm}^2$	$50 \times 85\,\mu\mathrm{m}^2$	$50 \times 70\,\mu\mathrm{m}^2$

Table 5.1: Pixel pitch for the different PXD module types in the inner and outer layer (IF, OF, IB, OB).

5.2 Application Specific Integrated Circuits (ASICs)

The complexity of implementing DEPFET pixels in a detector architecture demands the development of custom control and readout circuits to utilise the technology. In the Belle II environment, they must also be suitable for use in harsh radiation environments. In total, three different types of ASICs handle control, digitisation and data processing. The functionalities are implemented in the design of the SWITCHER, DCD and DHP. This section explains the logic and functionality of the ASICs on the DEPFET pixel detector.

5.2.1 SWITCHER

The voltage steering ASIC on the DEPFET pixel detector module is the SWITCHER, which is produced in 180 nm AMS[2] technology. The SWITCHER ASIC is responsible for two tasks: Switching on the external gates of DEPFET pixels arranged in rows for sampling the drain current and clearing the signal charge present in the internal gate (explained in Sec. 3.3.1). [Per+11, p. 1536]
Both processes require a quasi-instantaneous change in the voltage level ($> 10\,\mathrm{V}$) applied to gate and clear lines. For a balance between fast readout of the DEPFET matrix and complete signal charge removal, a short clearing pulse ($\sim$20 ns [San+06, p. 180]) must be generated, taking into account the capacitive charge of the DEPFET matrix of 130 nF [FKP15, p. 1].
Activating all DEPFET pixels simultaneously would lead to high currents in the SWITCHER and each pixel would need its own readout electronics. Consequently, a row-wise readout is used, called *rolling-shutter mode*. To still ensure a fast readout time of the DEPFET matrix ($\sim$20 µs), the four-fold readout is applied in which four pixels per column are read out in parallel:

$$4 \text{ pixel rows} = 1 \text{ gate}_4.$$

With in total 192 gates$_4$, six SWITCHERs are bump-bonded on the 525 µm thick silicon balcony and serially connected (shown in Fig. 5.2). Each SWITCHER steers four voltages in 32 channels connected to the gate$_4$ and clear lines:

[2] Austria Micro Systems

$V_{\text{Gate-Off}}$ / $V_{\text{Gate-On}}$	Low voltage level $V_{\text{Gate-Off}}$ for pixels during charge collection. $V_{\text{Gate-On}}$ is applied for the readout cycle of pixels within a gate$_4$.
$V_{\text{Clear-Off}}$ / $V_{\text{Clear-On}}$	Low voltage level $V_{\text{Clear-Off}}$ at clear contact during charge collection. $V_{\text{Clear-On}}$ is applied for clearing signal charges in the internal gate.

The SWITCHER provides three different schemes for applying the voltages [FKP15, p. 12]. For the operation of DEPFET modules in the Belle II experiment and the measurements presented in this thesis, switching with non-overlapping gates$_4$ is used. In this rolling-shutter mode, only pixels within one gate$_4$ are activated at a time. The mode of operation can be described in four steps (illustrated in Fig. 5.4):

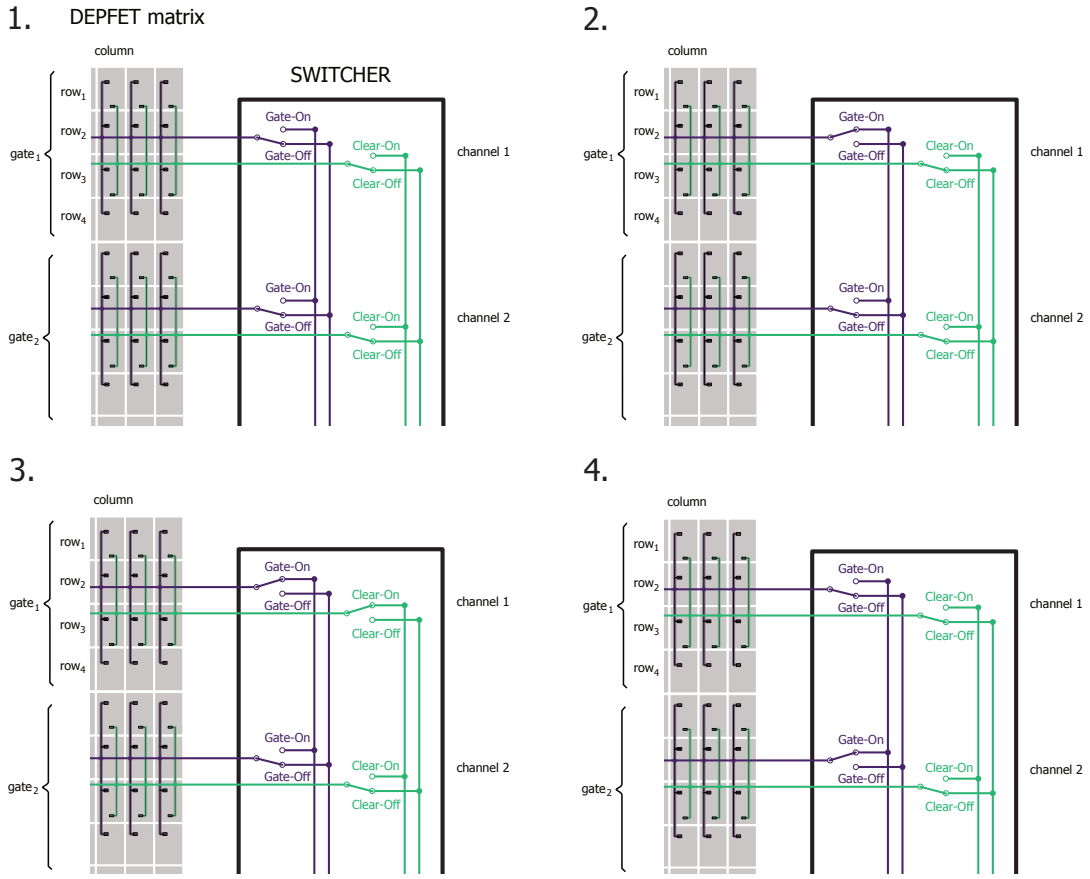


Figure 5.4: Principle of switching gates$_4$ of the DEPFET matrix using the SWITCHER. Via the gate$_4$ and clear line, four pixels per column are controlled (four-fold readout). Pixels in the first gate$_4$ are switched off for charge collection (*step #1*) and switched on for the readout process (*step #2*). The signal charges are cleared (*step #3*) before the pixels in the next gate$_4$ are activated (*step #4*).

1. **Charge collection**: $V_{\text{Gate-Off}}$ and $V_{\text{Clear-Off}}$ are applied to the external gates and clear contacts (via the gate_4 and clear line), respectively. Generated signal charges are drifting to the internal gate.

2. **Signal readout**: The SWITCHER applies $V_{\text{Gate-On}}$ at the gate_4 line while $V_{\text{Clear-Off}}$ is still connected. The DEPFET pixels in the gate_4 are switched on and the drain current (I_d) is sampled.

3. **Signal clearing**: While the DEPFET pixels in the current gate_4 are still on with $V_{\text{Gate-On}}$ applied, $V_{\text{Clear-On}}$ is supplied to the clear line. Electrons in the internal gate overcome the potential barrier created by cleargate and drift to the clear implant (described in Sec. 3.3.1).

4. **Switching to next gate**: The DEPFET pixels in the gate_4 are switched off using $V_{\text{Gate-Off}}$. The voltage at the clear line is set back to $V_{\text{Clear-Off}}$. The pixels in the next gate_4 are activated by the SWITCHER. The previous gate_4 is in the charge collection state (*step #1*).

Each output channel of the SWITCHER consists of two line drivers for gate_4 and clear lines. To control the state of the output channel, four control signals are used, namely, `Clock`, `Strobe Gate` (`StrG`), `Strobe Clear` (`StrC`) and `SerIn`. A digital logic block for a single channel is illustrated in Fig. 5.5.

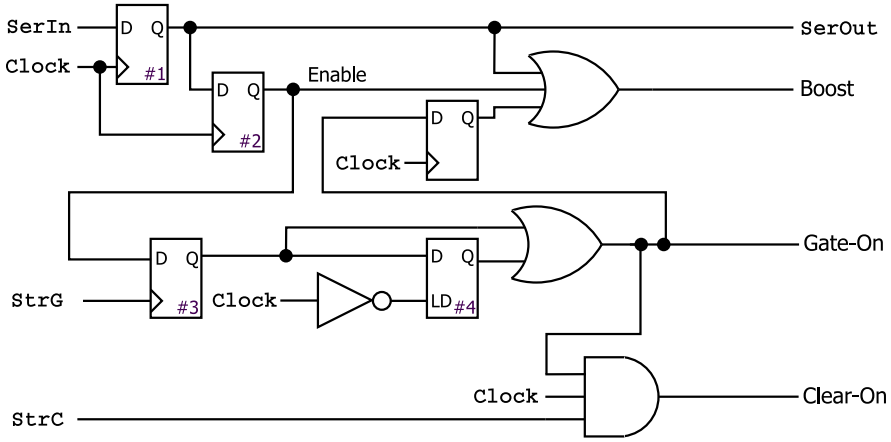


Figure 5.5: Simplified representation of a single digital logic block (corresponds to one SWITCHER channel). The flip-flops and latch are numbered for description. Adapted from [FKP15, p. 13].

The control signals of the logic are described below. The resulting sequence of two SWITCHER channels can be observed in Fig. 5.6.

– `Clock`: The `Clock` is used to drive the digital logic blocks in the individual channels of the SWITCHER. The signal is common to all channels and ensures that the flip-flops react to the input signal with predefined timing.

– `SerIn`: In contrast to `Clock` and the two strobe signals, the `SerIn` signal is transferred serially through the SWITCHER channels. It activates the SWITCHER channel and can be explained using Fig. 5.5. When a `SerIn` signal is received at *flip-flop #1*, the output line driver is set to the boosted state (*Boost*). This state is selected for the activated channel providing a circuit for high speed level shifting. In the unselected channels, power saving circuits are activated. [Kno11, pp. 26-28]
In the following clock cycle, the 1-level is transferred to *flip-flop #2*. This shift enables *flip-flop #3* to be sensitive to the signal of `StrG`. The `SerOut` signal of the last channel is transmitted to the next SWITCHER via an output pad. In this way, several SWITCHERs can be operated in a daisy chain.

– `StrG`: The strobe signal causes a level shift from $V_{\text{Gate-Off}}$ to $V_{\text{Gate-On}}$ (*Gate-On*) to the gate_4 line. *Latch #4* keeps *Gate-On* until the next falling edge of `Clock` (see Fig. 5.6). Moreover, `StrG` can only be sent after a falling edge of `Clock`.

– `StrC`: The `StrC` signal can be detected as long as *Gate-On* is applied to the line. In this case, the length of the transmitted control signal corresponds to the length of the level shift from $V_{\text{Clear-Off}}$ to $V_{\text{Clear-On}}$ (*Clear-On*). Consequently, the length can be set directly in the sequence.

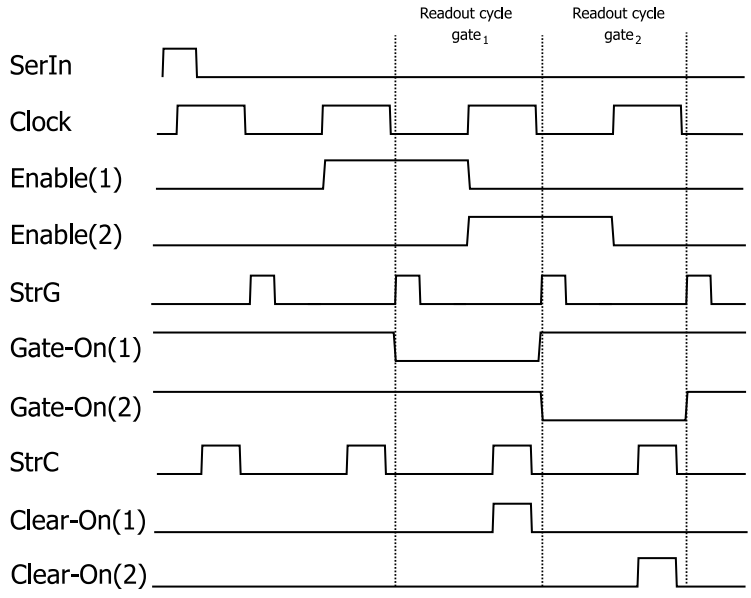


Figure 5.6: Signal sequence of two SWITCHER channels. The control signals `Clock`, `StrG`, `StrC` cause the level shift for activation and clearing. Adapted from [FKP15, p. 15].

The four differential signals are transmitted from the SWITCHER sequence memory inside the DHP ASIC via LVDS. The output clock frequency of the bits in the memory is 305 MHz [Lem13, p. 46]. Each 128-bit long word written into the memory is composed of the four 32-bit long signal sequences {`Clock`, `StrG`, `StrC`, `SerIn`}. The uploaded SWITCHER sequence is depicted in Fig. 8.1 in the appendix. A measurement of the output voltages resulting from the sequence is shown in Fig. 6.11 (Sec. 6.5.1). After the SWITCHER function has been discussed, the ASIC responsible for the drain current digitisation is described in the following.

5.2.2 Drain Current Digitiser (DCD)

The DCD ASIC provides 256 channels connected to the drain lines of the DEPFET pixels for further processing. It is manufactured in a 180 nm UMC[3] CMOS technology [Per+11]. On two stages, the analogue input signal gets amplified and digitised by ADCs with 8-bit resolution. This section describes the basic working principle of the DCD. More detailed descriptions are provided in [Kno11; Per16; Per+10].

DCD working principle

The drain lines are connected column-wise to the inputs of the channels, sampling the currents in parallel every ∼100 ns [Kno11, p. 38]. At first, the currents reach the analogue input stage in the DCD via a pad bump-bonded to the line on the module. A simplified illustration for a single channel is shown in Fig. 5.7.

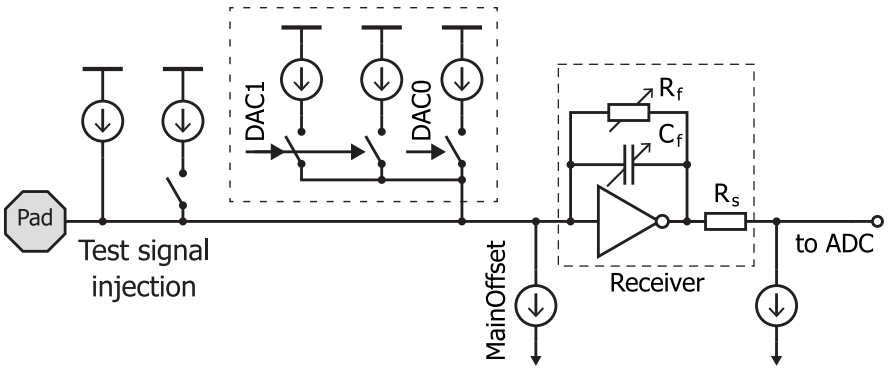


Figure 5.7: Schematic of the DCD analogue input channel. Main components are the current receiver and the 2-bit DAC that can be switched to the current. Resistors R_f/R_s are used to adjust the gain of the current receiver. The test injection circuit can be used for calibration of the ADCs. From [Koc11, p. 36].

The current receiver consists of a Trans-Impedance Amplifier (TIA) with a resistor connected at the feedback. Using a TIA with ideally constant potential at the input, the current is converted

[3] United Microelectronics Corporation

into a voltage following the relation [FKP15, p. 9]:

$$V_{\text{out}} = V_{\text{input}} - I_{\text{input}} \cdot R_f. \tag{5.1}$$

The resistor R_s is connected between the output of the TIA and the input of the ADC. With a constant potential at the ADC input, the current flowing into the ADC is:

$$I_{\text{out}} = I_{\text{offset}} - \frac{R_f}{R_s} \cdot I_{\text{input}}, \tag{5.2}$$

with the offset current $I_{\text{offset}} = (V_{\text{input}} - V_{\text{ADC}})/R_s$. The factor caused by the two resistors (R_f/R_s) is called *gain* of the TIA. The gain can be set globally by changing the values of the feedback resistor. Furthermore, the feedback capacitor C_f can be modified to adjust the settling time. The configuration is set via a JTAG register which is implemented on chip, see Sec. 5.3. The settings `En30`, `En60`, `En90` connect to a 26 kΩ, 13 kΩ and 19 kΩ resistor, respectively. Changes to the feedback capacity can be made with `Encap`.
To convert the analogue current into a digital value, the ADC performs a redundant signed-digit conversion using current-mode memory cells [Per16, pp. 10-12]. The operating principle, performance and dynamic range measurements of the ADC are described in detail in [Per16] and [Lüt19, pp. 36-40]. The output of the ADC is a code with 8-bit resolution offering a range from -127 to 127 given in an Arbitrary Digital Unit (ADU).

Serialisation: In the digital part of the DCD, the 256 output channels are divided into pairs of 8×32 channels. Afterwards, the 32 channels within one pair are multiplexed and sent to the DHP via an 8-bit wide bus [Kno11, p. 55]. For each DCD clock cycle (305 MHz) and channel pair, an 8-bit long output value of one channel is transmitted to the DHP. In total, there are eight channels between DCD and DHP (see Fig. 5.8).
A functional connection and the correct timing between DCD and DHP can be tested by activating a test pattern, which is programmed in the DCD.

5.2.3 Data Handling Processor (DHP)

The DHP is processed in 65 nm TSMC[4] CMOS technology. The main purpose of the DHP is the reduction of data coming from the DCD by performing a zero-suppression readout [Lem13, pp. 37-45]. It is motivated by the amount of data originating from the DCD (∼20 Gbps) and the bandwidth limit of the serial data link (∼1.6 Gbps). Within the DHP, the data is buffered and transmitted to the back-end electronics on request by an external trigger.
To ensure transmission over longer cables, a line driver, referred to as Common Mode Logic (CML), is used in the DHP [Lem+13, p. 5]. This technique performs a pre-amplification of the signal which counteracts the effect of signal degradation.

[4] Taiwan Semiconductor Manufacturing Company

In the following, the structures of the main memories, the data reduction and the data format are described in more detail.

DHP memory structure

The main memory of the DHP, which is responsible for storing the data received from the DCD, is divided into 16 Static Random-Access Memory (SRAM) cells. There are 8 channels with 8 physical connections between DCD and DHP. On these lines, the 8-bit ADC values of the DEPFET pixels are transmitted with the DCD clock of 305 MHz. On the DHP side, 32 clock cycles (in relation to DCD clock) are required to read the data from the DCD for data of one gate_4 and store it in the DHP main memory. An illustration of the SRAM cells is depicted in Fig. 5.8.

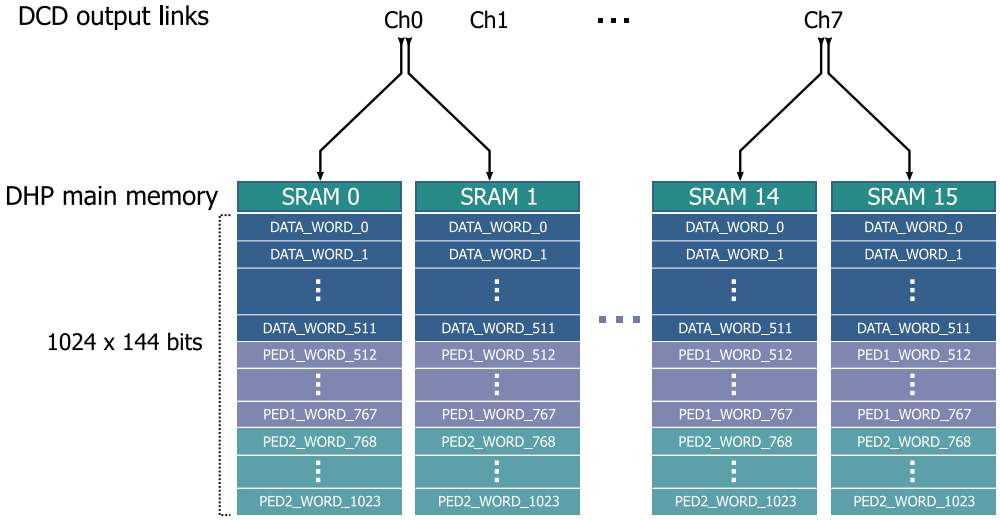


Figure 5.8: Layout of the DHP main memory. It consists of 16 SRAM cells each with a capacity of 1024×144 bits. The DCD sends 8-bit pixel data via 8 links in parallel ($8 \times 8 = 64$ bits). Adapted from [LGH16].

A single SRAM cell is divided into three parts:

- **Data memory**: The first 512 SRAM memory rows are reserved for data sent by the DCD. One row (`DATA_WORD`) in a single cell contains the 8-bit charge information of 16 DEPFET pixels ($16 \times 8 = 128$ bits). Therefore, the first row of all combined SRAM cells contains the data from one DEPFET gate_4 within 64 columns. A map for the so-called DHP mapping is shown in Fig. 8.2 in the appendix. Another 8 bits are parity bits and 8 bits are used for the Error Correction Code (ECC) with which Single Event Upsets (SEUs) can be corrected [Lem13, p. 95]. In total, 2.7 frames can be stored in the data memory.

- **Pedestal memory 1**: The rows from 512 to 727 are defined for the pedestal values. In the zero-suppressed readout, the stored content is subtracted from the respective data values. In contrast to the data memory, this memory is only written externally via JTAG.

- **Pedestal memory 2**: A second pedestal memory can be used for the process of subtraction. With a setting in the DHP, the rows from 768 to 1023 can be selected.

There are two methods of reading out the data from the DHP memory: Raw data dumping of the memory and zero-suppressed readout. Both types are described below.

Raw data memory readout

The full memory content is requested with the *memory dump* command via the trigger line. Consequently, the entire raw data as well as the equally sized contents of the two pedestal memories are sent. This function is mainly used for recording pedestal frames which are subsequently uploaded to one of the pedestal memories (see Sec. 6.5.3).
By setting the register `last_row_dump`, the output of the memory dump can be reduced. It specifies the number of rows in the SRAM (equal to the number of gates_4 of the frame) to be dumped. For a full frame readout, the value is set to 191.

Data processing in zero-suppressed readout

The second type of data readout is the *zero-suppressed readout* and is initiated by the trigger command. The length of the command determines the number of gates_4 in the memory which are further processed. Moreover, a latency register can be used to determine the starting row of the memory readout. This procedure is described in more detail in Sec. 7.2.2.
Compared to the memory dump, the data is handled internally in the DHP before it is sent to the back-end electronics. The processing stages are outlined in the following [Lem13; Ger19]:

1. **Pedestal subtraction**: The pedestal subtraction should lead to the isolation of the signal that modulates the drain current. For this process, pedestal values (digitised dark currents of the DEPFET pixels) are recorded using memory dumps and subsequently uploaded to the pedestal memory via the JTAG interface. Consequently, the respective pedestal values are subtracted from the corresponding value in the data memory. By subtraction, the dark current is removed pixel by pixel:

$$I_{\text{signal}} = I_{\text{signal+pedestal}} - \overline{I}_{\text{pedestal}}.$$

   Due to fluctuations occurring in the pedestals (e.g. temperature or environmental fluctuations), an average pedestal value $\overline{I}_{\text{pedestal}}$ is typically determined for several frames. Moreover, $\overline{I}_{\text{pedestal}}$ can vary over time and needs to be updated for a precise determination.

2. **Common-mode correction**: An effect occurring when reading out four pixel rows at the same time is the common-mode noise. Since this form of noise changes for every sampling period, a common-mode noise correction is carried out inside the DHP [Krü10, p. 340]. The Two Parse Average (TPA) algorithm is used to calculate the common-mode value that is added to the signal [Lem+12, p. 5]. First, the values of N pixels within one gate_4 are averaged:

$$\overline{CM} = \frac{\sum_j I_{\text{out,j}}}{N}.$$

Subsequently, the averaged common-mode value $\overline{CM}$ is added to an adjustable threshold and compared to the measured signal. If the signal is greater than or equal to $\overline{CM}$ + threshold, it is replaced with $\overline{CM}$ during the next averaging:

$$CM = \frac{\sum_j \widetilde{I}_{\text{out,j}}}{N} \quad \text{with} \quad \widetilde{I}_{\text{out,j}} = \begin{cases} I_{\text{out,j}} & \text{if } I_{\text{out,j}} < \overline{CM} + \text{threshold}, \\ \overline{CM} & \text{if } I_{\text{out,j}} \geq \overline{CM} + \text{threshold}. \end{cases}$$

In the common-mode correction step, the calculated CM is subtracted from all measured values. The resulting values are compared against the threshold and set to zero in case of a signal that is smaller or equal to the threshold. These cases are not considered further.

3. **Hit finder**: The processed data not equal to zero is inserted into an input buffer consisting of 64 First-In-First-Out (FIFOs) (one FIFO for each column of pixels). In the hit finder, the hit information (position and signal in ADU) is generated and stored in an additional buffer level [Lüt19, p. 44]. Because the hit finder produces data faster than the DHP serialises and sends it, this buffer level is necessary [Lem13, p. 45]. For high numbers of hits, this procession stage is susceptible to data loss.

4. **Serializer**: The hit data is structured in 16-bit words and are packed into frames [Lem13, p. 45]. Each frame transmitted by the DHP contains a frame header. The Aurora 8b/10b protocol [Xil14] is used to transfer the encoded data from the DHP to the back-end electronics via a high-speed link.

The data format to be transmitted is described in the following section.

Output data format

The structure and information included in the data format sent by the DHP differs for the two readout modes, i.e. raw data and zero-suppressed readout. In both modes, the frame header is transmitted first within two 16-bit words. The composition of the 32-bit frame header is shown in Tab. 5.2.
It contains the information about the mode (*data type*) in which the data is provided by the DHP: `3'b101` for zero-suppressed readout and `3'b000` for raw data.

3'b	2'b00	1'b	1'b	1'b	8'b	16'b
Data type	unused	*CM* error	Offset active	PED memory	Chip ID	Frame ID
		Flag				

Table 5.2: Data format of the frame header sent by the DHP.

Flag bits indicate whether an error occurred in the common-mode calculation (*CM error*), whether the offset correction is activated and which of the two pedestal memories is used for zero-suppression (*PED memory*). Finally, a programmable *chip ID* and the 16-bit *frame ID* (0 to 65535) are transmitted.
Subsequent data, which is divided into frame packages, differ in the readout modes as well. The raw data is transmitted by the DHP as follows:

Frame Header	ADC {4,3}	ADC {2,1}	···	PED1 {4,3}	···

It consists of 16-bit long ADC words containing the digitised drain currents of two DEPFET pixels followed by the pedestal values in the same format. For zero-suppressed readout, the following structure is used [LGH16, p. 14]:

Frame Header	Row Header1	Data Word1	···	Row Header2	Data Word1	···

Data words are subdivided according to their row (*row header*). The combination of both words contains the information of the hit, i.e. the position, the common-mode value and the signal (shown in Tab. 5.3).

Row Header			Data Word		
1'b0	9'b	6'b	1'b1	7'b	8'b
Flag	Row address	CM	Flag	Column address	Signal

Table 5.3: Bit assignment within the row header and the data word.

The row header can be identified by the flag bit which is set to `1'b0`. Corresponding data in turn have a `1'b1` as flag bit. With a total of 768 rows in the DEPFET matrix, the 9-bit row address is not sufficient (0 to 511). For this reason, the least significant bit (bit 1) of the row address is situated in the most significant bit (bit 7) of the column address in the data word.

5.3 ASIC configuration

With the increase in the complexity of integrated circuits and the expansion of functionalities, a standardised procedure for verifying the functionality of the circuits has been worked on since 1985. The cooperation of semiconductor manufacturers has been known as the Joint Test Action Group (JTAG), which is an abbreviation of the protocol from IEEE[5] Standard 1149.1 [IEE]. This interface is primarily used to check the functionality of the ASICs of the DEPFET detector module. The procedure is described in more detail in [Lei15].
For operating the module, JTAG is additionally used as slow control. It sets the configuration of the ASICs at any time of operation. In this section, the JTAG protocol is addressed before the configuration of the ASICs is described.

JTAG protocol

The intention of this interface is to verify integrated circuits after they have been assembled and, if necessary, during operation in the working environment. This feature is provided by the Test Access Port (TAP) which enables the so-called boundary scan in the chip. The TAP consists of 5 signals: Test Mode Select (`TMS`), Test Clock (`TCK`), Test Data In (`TDI`), Test Data Out (`TDO`) and Test Reset (`TRST`). On the chip side, a finite state machine (TAP controller) is controlled exclusively by the signals `TMS` and `TCK`. The `TMS` signal must be set before each rising edge of the `TCK` to change the state of the state machine. `TMS` is used to access the two main tasks in the state machine: Scanning of the Instruction Register (IR) or the Data Register (DR) [Par15, p. 12]. On the `TDI` line, the instruction is loaded serially into the IR. The TAP controller, steered by `TMS`, ensures that the instruction is only loaded after the end of the shift process. Subsequently, the instruction is executed, e.g. a test circuit is connected.
Using the DR, the response of this circuit can be modified. Moreover, implemented functions or connections in the chip can be tested. The data is loaded in the same way as the instruction and the response of the circuit is received by shifting out the data register (identical to a shift register) [IEE, p. 2].

Configuring via JTAG

For the three types of ASICs on the DEPFET module, JTAG is used for two tasks:

1. Checking the functionality of the ASICs after they have been placed on the module. Therefore, defective or missing connections and malfunctions of the ASICs can be detected (explained in [Lei15]).

2. The interface is used to configure the ASICs and provides slow control over their functionality and thus also over the detector module. Comparable to the test procedure, instruc-

[5] Institute of Electrical and Electronics Engineers

tions are used to call registers that can be overwritten with the data register changing functions in the ASICs.

For this purpose, the DHP, DCD and SWITCHER have a JTAG Interface (JTAG IF). As a standard configuration, all DHPs are initially connected in series, referred to as a daisy chain. They share the same `TMS` and `TCK` signal which causes the same status of the TAP controller. The data input (`TDI`) is always the data output (`TDO`) of the previous chip. In principle, this results in a long shift register. An illustration of the JTAG chain of the ASICs used is shown in Fig. 5.9.

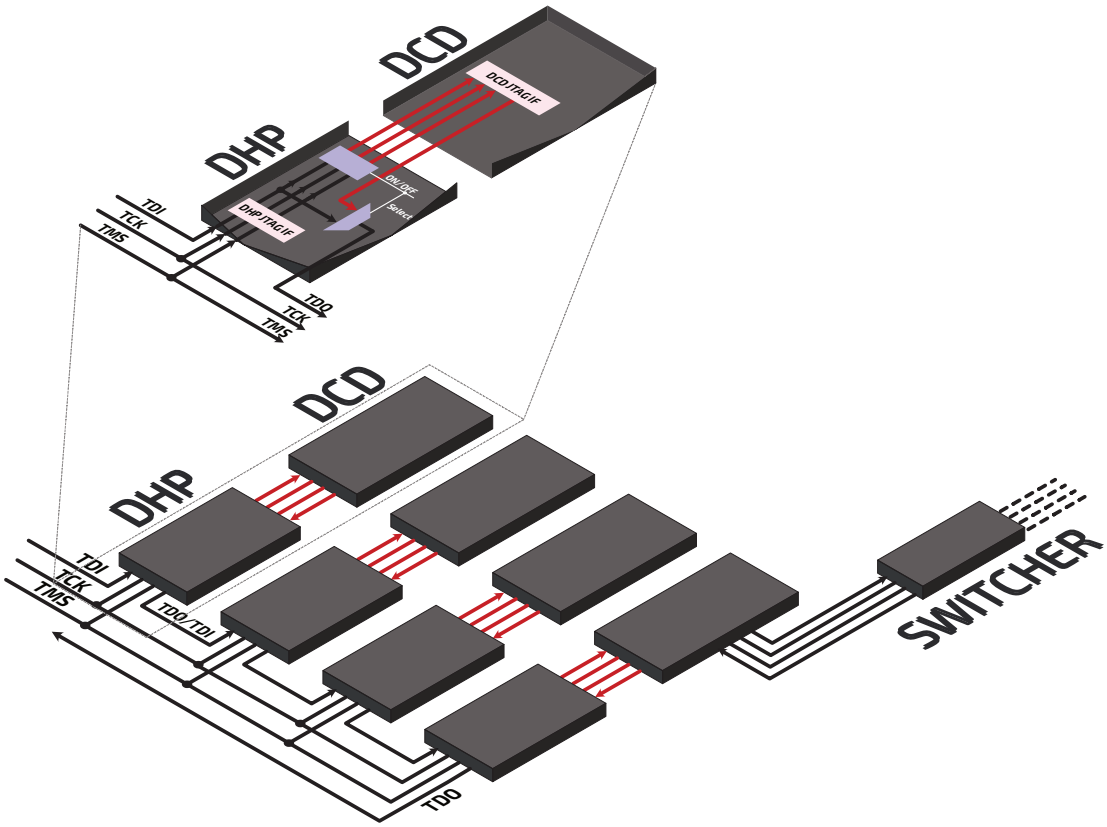


Figure 5.9: JTAG connection between DHPs, DCDs and SWITCHERs of the DEPFET module. The JTAG data input (`TDI`) is daisy chained for the ASICs. Red connections between DHPs and DCDs indicate the optionality of this connection.

The DCDs can be added to or removed from the JTAG chain. This option is set via a JTAG register in the respective DHP. If the DCD is excluded, no JTAG signals are routed to the DCD. As soon as the last DCD in the JTAG series is included, the six SWITCHERs are added to the chain. Various settings changing functional properties are accessible to the user via JTAG registers. Therefore, each option has dedicated bits within these registers. A list of all existing

registers can be found in Tab. 8.3 in the appendix. By writing the IR, the settings are set with the subsequent DR. While any other ASIC receives an instruction, there is the possibility of using a bypass register to prevent the ASIC from changing its function.
In addition to changing settings, JTAG is used to write to memories within the DHP. It facilitates the writing of data to an allocated memory address (pedestal upload described in Sec. 6.5.3). Furthermore, the SWITCHER memory inside the DHP, which generates the SWITCHER control signals, is programmed using this technique (described in Sec. 6.5.1).

6 BDAQ-PXD: A laboratory readout system

For the Data Acquisition (DAQ) of the PXD in Belle II, the *PXD-DAQ*, i.e. Data Handling Hub (DHH) [Hub+21], has been developed to handle and read out the entire detector, consisting of 40 modules. Consequently, PXD-DAQ is designed for the complex task of dealing with large amounts of data controlling all modules in parallel, making it a demanding system for the operation of a single module. In contrast, *BDAQ-PXD* is designed to be a lightweight test system with the aim of reducing complexity and simplifying applications in laboratory environments and to facilitate the readout of single DEPFET modules.
In this chapter, the set-up consisting of hard-, soft- and firmware elements is presented and the individual components as well as their implementation details are described. Afterwards, first measurements and application examples, using BDAQ-PXD, are demonstrated.

6.1 Hardware set-up

The BDAQ-PXD system is designed to be used in laboratory and test environments. Accordingly, the set-up comprises the minimum required components for the operation of DEPFET modules. A schematic of the set-up layout can be seen in Fig. 6.1.

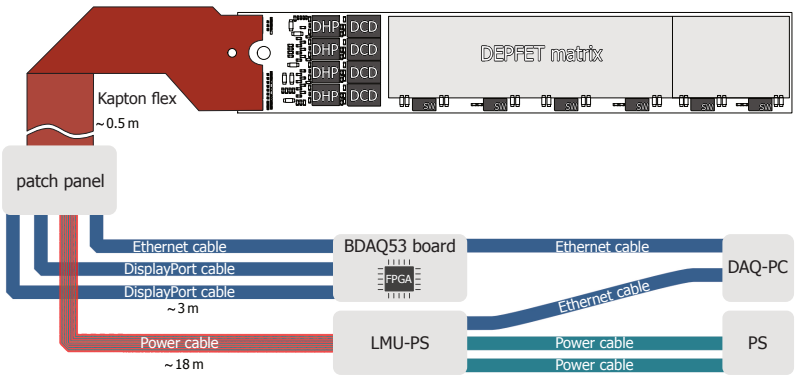


Figure 6.1: Schematic of the BDAQ-PXD set-up. A connection between DEPFET module and readout board (BDAQ53) is established via Kapton flex and patch panel. The LMU-PS produces voltages needed for powering the module. It is supplied by a commercial power supply. A DAQ-PC is used to operate the LMU-PS, BDAQ-PXD and consequently the DEPFET module.

The main unit of BDAQ-PXD is the BDAQ53 board (see Sec. 6.1.1). It houses a commercial Field-Programmable Gate Array (FPGA) and facilitates the readout and configuration of the detector. A custom-made Patch Panel (PP) (see Sec. 6.1.2) serves as an interface for readout-related, bidirectional signal transmission. Two DisplayPort (DP) connectors and an RJ45 connector are used for the communication between board and detector. Furthermore, it is the connection point for the custom-made power supply (LMU-PS, see Sec. 6.1.3), providing all voltages needed by the DEPFET sensor and ASICs on the module. A commercial power supply is used to operate the LMU-PS. Two 18 m-long cables are designed for use in the Belle II detector where the power supplies are placed on top of the detector to power PXD modules, located at the IP. All signals and voltages merge on the PP and are connected to the Kapton flex of the module via a single connector. Finally, the LMU-PS as well as the BDAQ53 board are connected to a DAQ-PC, allowing one to operate the set-up. A picture of the set-up in the laboratory environment is shown in Fig. 6.2.

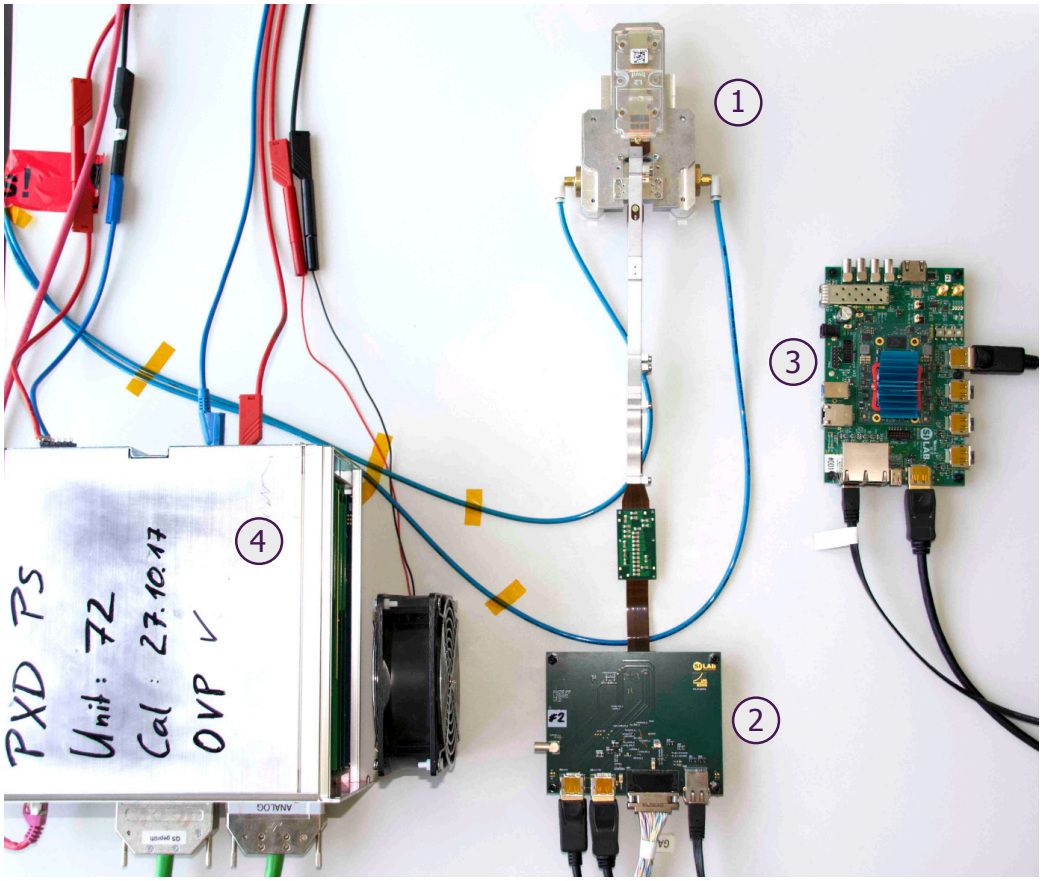


Figure 6.2: Layout of the BDAQ-PXD set-up in the laboratory environment. The DEPFET module (*#1*) is connected to the patch panel (*#2*). Cables connect to the readout board BDAQ53 (*#3*) and to the LMU-PS (*#4*).

6.1.1 BDAQ53 board

The BDAQ53 board has been developed for the readout of hybrid pixel detector chips for the upgrade of the inner tracking detectors of the ATLAS and CMS experiments at the Large Hadron Collider (LHC) [Daa+21]. The design and its versatile features make it also suitable for the readout of a single DEPFET module. The BDAQ53 board is depicted in Fig. 6.3.

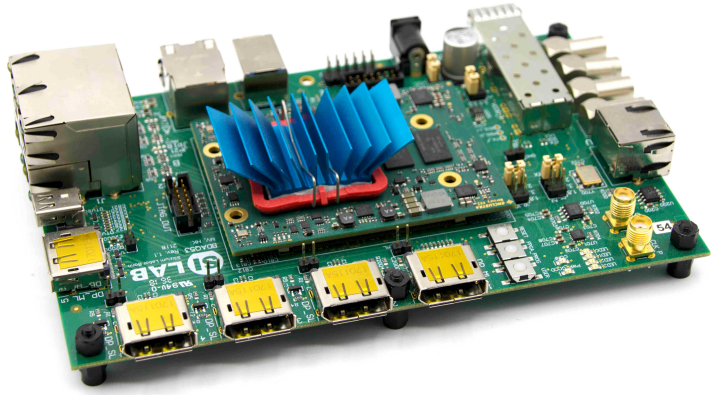


Figure 6.3: The BDAQ53 board with the *Enclustra Mercury+ KX2* module. The board offers numerous connection options: In addition to Ethernet, connections via DisplayPort, RJ45 and Mini-DisplayPort are possible.

The board consists of a commercial *Enclustra Mercury+ KX2* module embedding a *Xilinx Kintex-7* FPGA [Xil20], connected to a custom-made carrier board. The FPGA provides high-bandwidth for data in- and outputs. The base board is composed of a four-layer Printed Circuit Board (PCB) routing signals received and sent by the FPGA via various connectors. Especially relevant for BDAQ-PXD, Ethernet cables are used for module configuration and establishing the connection to the DAQ-PC, while DisplayPort is used for transmission of data, commands and clock.

6.1.2 Patch panel

The introduction of a new readout system requires the development of an interface between the detector and the readout board. The PP, a four-layer PCB, was developed within this work and provides the connection between BDAQ53 board and DEPFET module. A picture of the PP is shown in Fig. 6.4. It is equipped with a matching 100-pin *Samtec* connector that is used to connect to the Kapton flex of the DEPFET module. Moreover, it features three interfaces to the BDAQ53 board, namely a DP connector for clock and command signal transmission, a DP connector for data transmission, and an RJ45 connector for JTAG signals (described in Sec. 5.3). A 51-pin *GlenAir* [Gle] connector provides the connection to the custom-made power supply (see Sec. 6.1.3). The board offers dedicated test and measurement pins, distributed

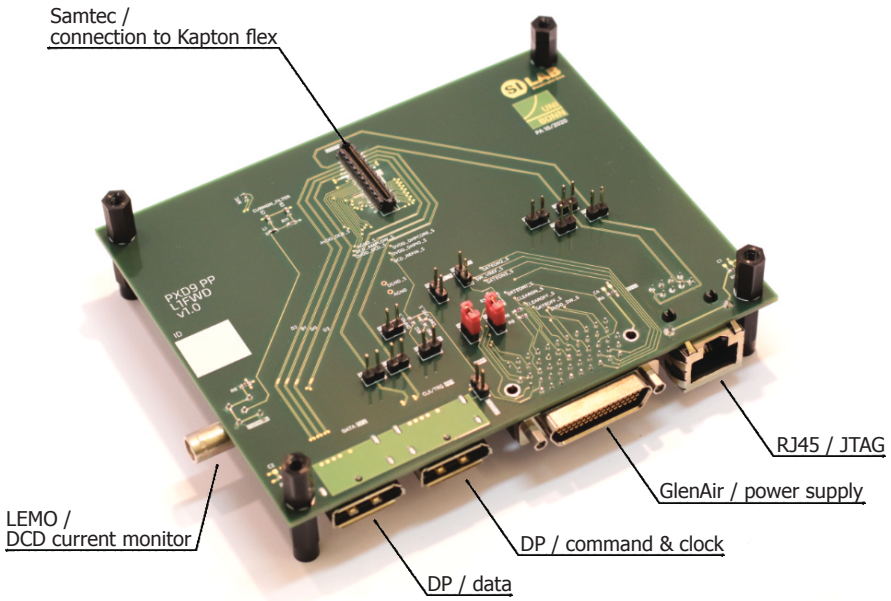


Figure 6.4: Picture of a patch panel (for IF DEPFET modules). Two DP connectors are used for clock/command signals and output data. Voltages and currents from the power supply are provided via *GlenAir* connector. An RJ45 connector and *LEMO* are the interface for JTAG communication and DCD monitoring, respectively. Finally, a *Samtec* connector with 100 pins can be connected to the Kapton flex of the module.

on the board, to probe data signals and measure power consumption. Furthermore, it features a *LEMO* connector for the so-called DCD current monitor, facilitating a calibration of the ADC channels inside the DCDs using an external current source (see Sec. 5.2.2).
To ensure a bit rate of ∼1.6 Gbps from the DHPs to the readout board, the impedance along the differential lines is maintained (100 Ω). Using dedicated PCB design tools, a suitable thickness as well as separation of differential pairs are determined. In addition, the difference of the propagation times within a pair are kept to a minimum to prevent introducing delays.
Due to the orientation of the DEPFET modules in the Belle II detector (explained in Sec. 5.1), the pin assignment on the *Samtec* connector changes for each module type. As a result, a PP design for each type is necessary. Within the scope of this thesis, patch panels for the first layer forward (IF) modules and second layer backward (OB) modules have been designed.

Grounding scheme

The grounding scheme plays an important role for data transfer from the detector to the readout system. In the DEPFET module, various power net domains are connected to individual grounds [Mül17, p. 122]. The voltages at the DHPs (*DHP_IO* and *DHP_CORE*) are applied with respect to digital ground (*DGND*). To ensure that transmitters on the DHP side and re-

ceivers on the readout board have a common ground, the use of grounding nets is necessary. A sketch of the implementation is shown in Fig. 6.5.

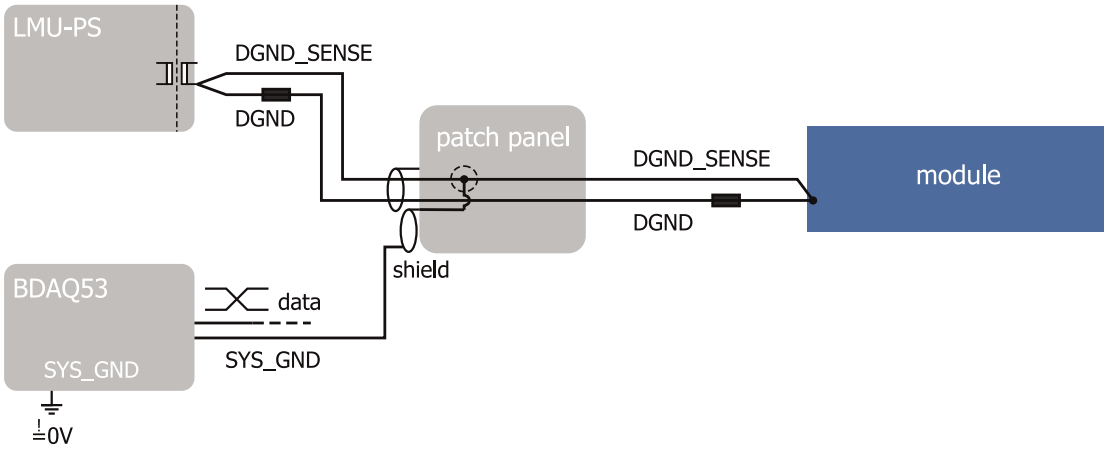


Figure 6.5: Schematic of the implemented grounding scheme. On the patch panel, the digital ground (*DGND_SENSE*) is connected to the system ground (*SYS_GND*) of the BDAQ53 board.

The digital supply voltage from the LMU-PS is transmitted via 18 m-long cables resulting in voltage drops proportional to the supplied current and cable resistance. To reach the desired voltage at the module over the full lengths of the cables, sense lines are used. The sense lines allow one to measure the voltage at load, enabling the power supply to readjust the output voltage (see Sec. 6.1.3).
An isolation transformer inside the LMU-PS allows for the connection of circuits with different ground potentials compared to the ground of the power supply itself. The BDAQ53 board has a system ground (*SYS_GND*) provided by the supply voltage. The system ground is established via the outer shields of the cables (DP and Ethernet), which in turn are conductively coupled to the connectors on the patch panel. This allows one to connect *DGND_SENSE* to *SYS_GND*. In this way, the grounding potentials on the detector and readout side can be balanced and a data transmission is established between the DHPs and the BDAQ53 board.

6.1.3 Custom power supply (LMU-PS)

In the design and implementation of a DEPFET module, as described in Sec. 3.3 and Sec. 5.1, 23 voltages (9 ASIC + 14 DEPFET matrix voltages) are required for operation. To provide these voltages, a custom-made power supply, called LMU-PS, has been developed and built [Rum13]. From a supply voltage of 24 V, the voltages are generated using DC/DC converters. A picture of the power supply is shown in Fig. 6.6.

Figure 6.6: Custom-made power supply (LMU-PS) for the Belle II PXD. The side view shows the modular structure with DC/DC and regulator cards. Two 18 m-long cables are used to provide the module with power. The Ethernet connection is used for remote control.

The LMU-PS has a modular structure with layers of regulator and DC/DC cards [Rum13, p. 54]. This ensures the interchangeability of the individual components. Furthermore, the power supply embeds a microcontroller that facilitates remote control of the voltages via Ethernet. Power-up and power-down sequences are used to ensure safe conditioning of the DEPFET matrix and ASICs.

6.2 Firmware development

In order to use the BDAQ53 board for the readout of a DEPFET module, the FPGA needs to be configured. In the initial state, an FPGA has no predefined function. Therefore, it allows for the configuration of customised functions by a dedicated *firmware*. The firmware functions, referred to as *modules*, are written in Verilog HDL[1] and built on top of the *basil* framework [Sila]. The framework offers specified firmware modules for the application of detector readout systems in laboratory environments (e.g.[Daa+21],[Hir19]). An overview of the essential modules included in the BDAQ-PXD system is shown in Fig. 6.7. The firmware components and their functions are described below.

basil bus: The *basil bus* is the core of the *basil* architecture. Various commands are sent via the bus with the assigned address of the module that needs to be accessed. The commands can serve to initiate and configure the modules or monitor internal values, signals and registers. In Sec. 6.3, the initialisation as well as communication with firmware modules are described.

[1] Hardware Description Language

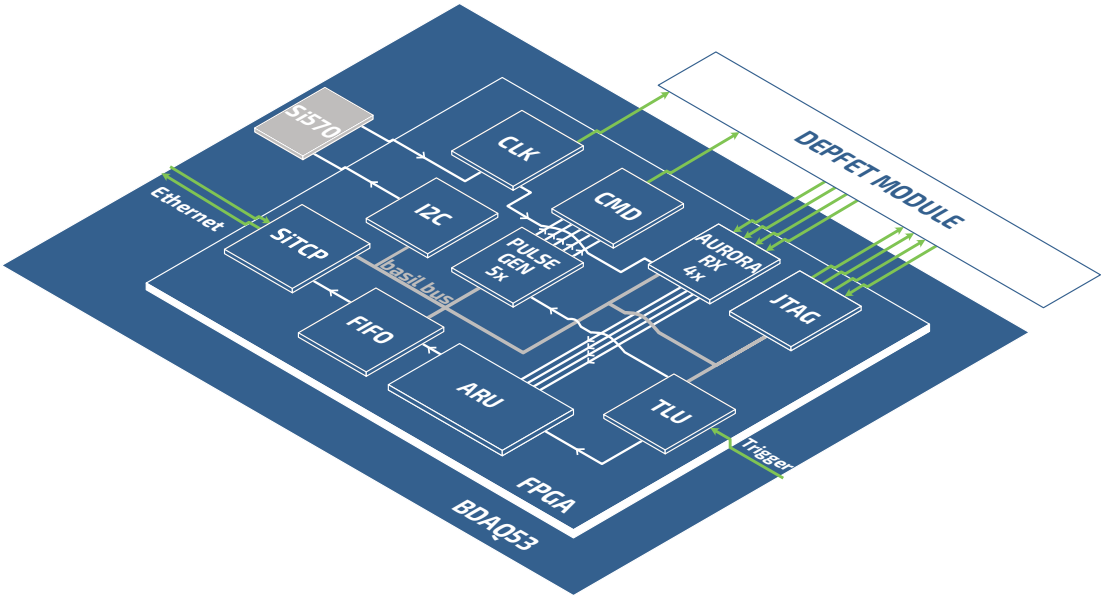


Figure 6.7: Block diagram of the firmware modules of BDAQ-PXD. The *basil bus* for control is marked in grey. In- and output signals are highlighted in green. The Si570-IC is placed on the BDAQ53 base board.

SiTCP: In order to transfer data from the FPGA to a DAQ-PC, SiTCP is used [Uch08]. It provides a hardware-based Transmission Control Protocol (TCP) processor which allows for a gigabit Ethernet link [Uch08, p. 1]. The module is suited for the purpose of transmitting large amounts of data such as in physics experiments. Furthermore, it offers remote bus control from the DAQ-PC to the FPGA.

Si570 and clock signal (`CLK`): The Si570-IC[2] from Silicon Labs provides a low-jitter clock in a frequency range from 10 to 945 MHz [Sky18]. The external component is located on the BDAQ53 base board. The oscillator is programmable and can be configured via an I^2C interface. The Si570 generated `CLK` is used as a reference clock for the high-speed transceivers of the FPGA. The clock transmitted from BDAQ-PXD to the DHPs has a frequency of 76.2 MHz.

Pulse generator (`PULSE_GEN`) and command signal (`CMD`): The pulse generator creates a pulse with configurable delay, width and frequency. Five pulse generators are used for the different command signals, i.e. memory dump, frame synchronisation, trigger, reset and veto. In a command encoder, the status of the pulse generators is retrieved and transformed to a DHP command. As an example, if a trigger and a frame synchronisation are applied at the

[2]Integrated Circuit

same time, the following command is generated:

Pulser state: (high:1 low:0)
{Reset}{Veto}{Trigger}{Fsync}{Memdump} = `5'b10010`

Command: (high:10 low:01)
{Reset}{Veto}{Trigger}{Fsync} = `8'b01011010`

An exception is the command for retrieving raw data (memory dump: `8'b111000xx`). The 2 bits per command state are part of the Manchester encoding used to introduce DC balancing [Ger19, p. 17]. A summary of all relevant commands can be found in Tab. 8.2 in the appendix. The command word is shifted out every 8^{th} clock cycle ($\sim$10 MHz) and sent to the DHPs. Since the frequency corresponds to the gate_4 switching frequency (see Sec. 5.2.1), the number of gates_4 to be readout can be determined by the pulse signal length. The pulse generator modules can be controlled by the corresponding BDAQ-PXD software, as described in Sec. 6.3.

Aurora receiver (`AURORA RX`): Within the DHP, the *Aurora 8b/10b core* [Xil14] is used for data transmission. BDAQ-PXD receives data from up to four DHPs. In order to ensure proper data transmission at a bit rate of 1.6 Gbps, the Xilinx aurora core is set up in receiving mode, wrapping the transceiver on the FPGA. The individual modules allow one to monitor and reset the links between receivers and DHPs independently. Idle data frames are sent continuously to keep the link established even if no data is transmitted. The data reaches the readout system on one differential line pair per DHP. Data frames from the individual DHPs are tagged with an unique identifier after reaching the readout system. Subsequently, data streams are processed in the Arbiter Unit (`ARU`).

Arbiter Unit (`ARU`): The arbiter unit is used to handle multiple data streams arriving at the same time while writing to the memory. The arbiter processes incoming data from the four high-speed receivers and, if connected, data from the Trigger Logic Unit (TLU) (explained in Sec. 7.2.1). With the ability to prioritise data streams, data from the TLU is written to memory first. In an event of simultaneous incoming DHP data, the trigger word is always stored first. The outgoing data stream is connected to the `FIFO`.

First-In-First-Out (`FIFO`): The `FIFO` is implemented with a depth of 128×1024 bits. It can hold an entire raw data frame in the case that the TCP transfer of the data is pending.

JTAG: The JTAG interface is used for the configuration of ASICs on the DEPFET module and is described in detail in Sec. 5.3. The JTAG module works on the basis of a Serial Peripheral Interface (SPI) and is schematically shown in Fig. 6.8.

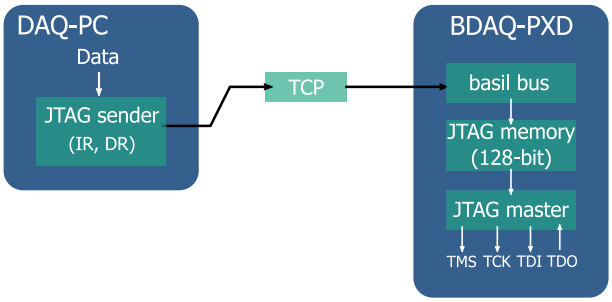


Figure 6.8: Working principle of the JTAG module. Data is transmitted from the DAQ-PC to BDAQ-PXD, in which the signals are then sent to the ASICs via a JTAG memory.

The data to be sent to the JTAG module is selected on the software side, e.g. pedestal data (explained in Sec. 6.5.3). Either the IR or the DR are transmitted via the TCP connection between DAQ-PC and BDAQ-PXD. On the FPGA side, the data can be stored in a memory with 128-bit depth until it is sent by the JTAG master module to the ASICs. The four separate JTAG signals `TCK`, `TDI`, `TDO` and `TMS` are managed by the firmware. For proper operation of all ASICs, the JTAG master operates at a clock frequency of 100 kHz.

Trigger Logic Unit controller (`TLU`): This general purpose trigger module enables the communication with the *EUDET TLU* (see Sec. 7.2.1). The main task of the module is to initiate the readout of the detector once a trigger is received. While the readout is busy, no further triggers are accepted [Die17, p. 18]. In Sec. 7.2.1, a measurement using the trigger logic is demonstrated. Trigger words received by the TLU module on the FPGA are propagated to the `FIFO` data interface through the `ARU`.

6.3 Software development

The development of a laboratory readout system for DEPFET modules using the multi-purpose BDAQ53 board requires the development of a tailored *software*. The data acquisition framework to handle data coming from the readout board is written in Python and designed for simplicity and scalability. It consists of multiple, individual components called *classes*, which are connected for data processing and interpretation. An overview of the software is outlined in Fig. 6.9.
The core part of the software is the *dhpt* class including functions for initialising readout hardware and DEPFET module (high-speed links), data handling and storage. Measurement scripts (*scans*) can be included independently of the *dhpt* class, ensuring simplicity of use. The *JTAG sender* is used to *configure* the ASICs by uploading the defined JTAG registers (see Sec. 5.3) with the corresponding settings (*configuration DHP*). In *yaml*[3] *files*, the settings for each DHP

[3]data language that is used for writing configuration files

and DCD pair are set as well as the configuration of the SWITCHERs. The configuration is handled in a stand-alone process, as the individual steps must be carried out with the sequence of applying voltages to the module during commissioning.
The interface for controlling the readout hardware and consequently the DEPFET module is provided by the *basil* framework (see Sec. 6.2). It contains the drivers for the firmware modules on the FPGA. Their individual addresses are loaded from *configuration BdaqPxd*. Specific functions and commands which are not part of *basil* are defined in the *BdaqPxd* class. Similarly, *BdaqPxd RX* contains commands for the Aurora receivers.
The data received from the BDAQ53 board is continuously stored in *raw data files*. Therefore,

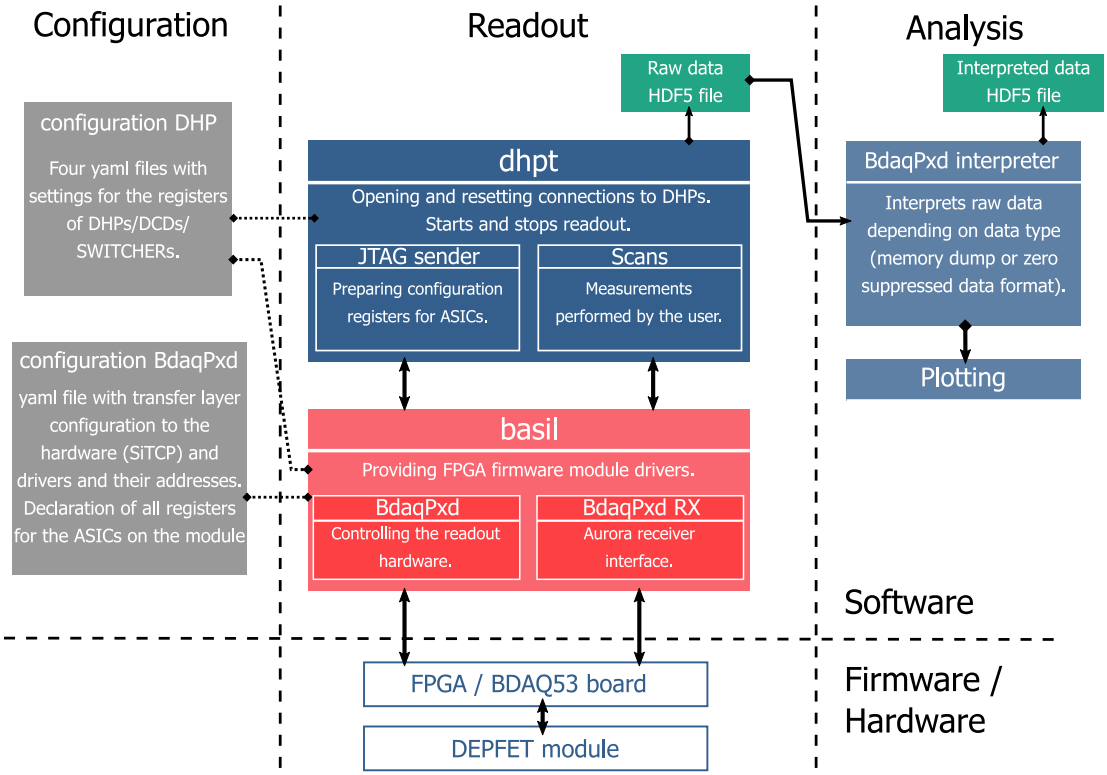


Figure 6.9: Simplified schematic of the BDAQ-PXD software. It can be divided into three parts, i.e. *configuration*, *readout* and *analysis*. Main software parts for communicating with the hardware (*basil*) and for providing necessary functions for measurements are marked in red and blue, respectively.

HDF5 files [HDF] are used, which are designed to store large datasets. The *analysis* part of the software facilitates the interpretation of the raw data. Based on the data format (explained in Sec. 5.2.3), the *BdaqPxd interpreter* can recognise the type of readout, namely *memory dump* or *zero-suppressed* readout. Accordingly, the interpreted data is stored in a separate file. This file contains histograms and tables, e.g. hit table with information of the recorded charge and

its pixel location on the module. Furthermore, all settings of the ASICs and parameters used in the scan are saved.
The visualisation of data is the final element of a scan. In addition to the default representations, e.g. a histogram of the charge distribution and the hit map of the module, other plots can be added to represent the occurrence and quality of the recorded data.

6.4 Simulation environment for DHP

The ability of simulating BDAQ-PXD and its communication with the DHP is a key factor for developing the soft- and firmware. For this purpose, a testbench environment called *cocotb* [Pot] is used. *Cocotb* serves as an interface between the tests written in Python (functions of the software) and a Verilog simulator [Daa+21, p. 3]. The simulator facilitates the testing of the communication between Verilog firmware and *DHP model* using the DHP source code (written in SystemVerilog RTL[4]). Since the DHP is the interface for the readout system and handles communication with the other ASICs (see Sec. 5.2.3), a DEPFET module was not required in the firmware and software development phase.
In the testbench, in- and outputs of the firmware modules are connected to the DHP model and are driven by a Python test. The sequence of the test routine is presented below.

1. *Implementation in firmware (core structure)*: The firmware modules, as presented in Sec. 6.2, belong to the core functionalities. When a new module is implemented (e.g. pulse generator, command encoder, high-speed receiver), it is connected to the DHP model in the testbench.

2. *Simulation*: The firmware module and the DHP model are operated with a Verilog simulator. The interface provided by *cocotb* allows the test (or software functions) to communicate with the firmware module via the *basil bus*. Accordingly, the functions can be debugged and the effects on the DHP model or the readout system can be tested. The output of the simulation is a waveform file containing signals obtained within the firmware modules of BDAQ-PXD and the DHP model.

3. *Implementation in firmware (top structure)*: Once the functionality of the core module is successfully tested, it is connected to physical interfaces on the readout board (top structure).

4. *Test on hardware*: The final test is performed using the DHPs on the DEPFET module and validates the desired functions.

For an illustration of the simulation step, a typical section of the output is shown in Fig. 6.10. Here, a reset signal is transmitted from BDAQ-PXD to the DHP model. As explained in

[4]Register Transfer Level: Abstraction layer for modelling integrated circuits

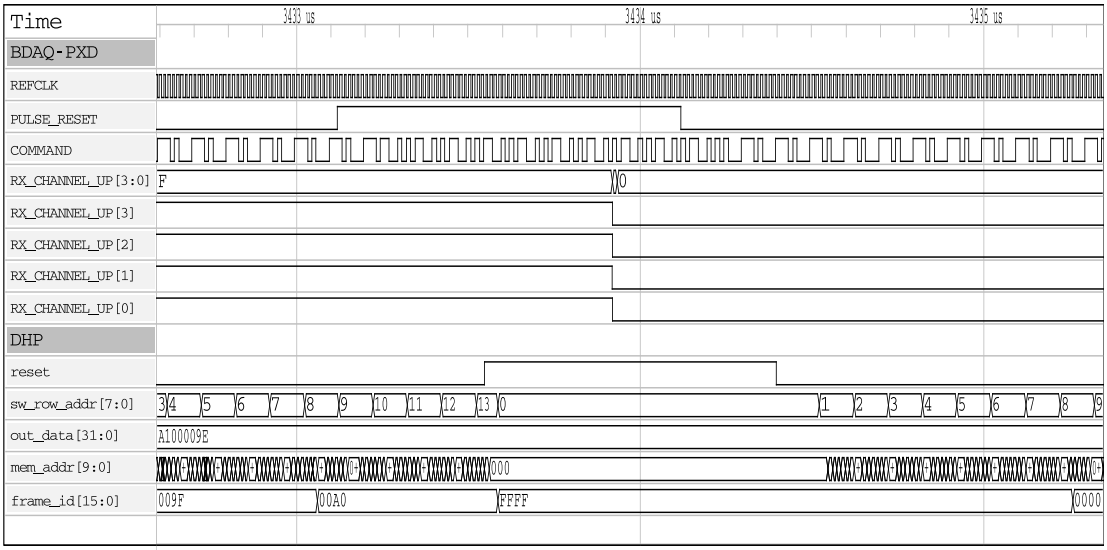


Figure 6.10: Section of the simulation output. Signals are divided according to their origin (BDAQ-PXD firmware modules and DHP model). The `PULSE_RESET` and the resulting `COMMAND` in BDAQ-PXD initiate a `reset` in the DHP model.

Sec. 6.2, the pulse generator (`PULSE_RESET`) is started resulting in a `COMMAND` sent to the DHP. In the DHP model, the `reset` is recognised and initiated. As a result, the high-speed links are suspended, as can be seen on the readout side (`RX_CHANNEL_UP`). In the simulation, the four receivers are connected to the same DHP model.
The `reset` restores all state machines within the DHP model [Ger19, p. 27]. This involves the read pointer of the memories such as in the SWITCHER sequence memory to be restarted with the first SWITCHER row (`sw_row_addr`). Additionally, the write addresses of the data storage memories (`mem_addr`) and the framing (`frame_id`) are set back to 0.

The simulation of the DHP is a crucial point in the development of the BDAQ-PXD system composed of firmware and software. Furthermore, troubleshooting on a simulated set-up does not pose a risk of incorrect ASICs settings on the DEPFET module. An investigation of the DHP performance using simulation in combination with the BDAQ-PXD readout system is presented in Sec. 6.5.6.

6.5 Operation of a DEPFET module using BDAQ-PXD

After introducing the BDAQ-PXD readout system, this section focuses on deploying it for operation of the DEPFET module. For this purpose, the procedure of configuring the DEPFET module in sequential steps is explained in detail. A short description of the required steps is given below:

1. *SWITCHER sequence upload*: With applied voltages to the module and the upload of the sequence, the operation of the SWITCHER starts. As described in Sec. 5.2.1, the rolling-shutter mode ($gate_4$-wise switching on and clearing of the DEPFET pixels) is activated and the drain current is sampled.

2. *Pedestal recording*: The pedestal measurement represents the drain current without signal charge present in the internal gate. To determine the change in the drain current caused by signal charges, pedestal recording is required prior to each measurement.

3. *Pedestal upload*: The pedestal values are uploaded into the DHP memory via JTAG, enabling the subtraction in the zero-suppressed readout (explained in Sec. 5.2.3).

Finally, the detection response to a radioactive source is measured to validate the functionality of the BDAQ-PXD system. The DEPFET module used is *W05_OB1*, which has already been used in a radiation campaign using X-ray photons up to an ionising dose of approximately 266 kGy [Sch+20]. As a result, impacts on the module include a higher noise level as well as defective switcher channels causing non-functional $gates_4$. Nevertheless, it has no influence on demonstrating the functionality of the BDAQ-PXD system.

6.5.1 SWITCHER sequence upload

In combination with applying the voltages to the DEPFET module, the operation of the SWITCHER is achieved by uploading the SWITCHER sequence. As described in Sec. 5.2.1, the sequence determines the timing of the signal switching connected to the DEPFET pixels to read out the drain current and remove the signal charges in the internal gate. It is written to the switcher sequence memory located inside the DHP closest to the six SWITCHERs. From there, the control signals (`StrG`, `StrC`, `Clock`, `SerIn`) are sent to the SWITCHERs (see Fig. 5.6 in Sec. 5.2.1). Once the SWITCHER sequence is uploaded and the output is enabled, the SWITCHERs start to serially switch on the $gates_4$ and subsequently apply the clearing voltage. To gain a better understanding of voltages and timings resulting from the uploaded sequence, a measurement is performed on one of the 32 SWITCHER channels. Since the channels are not freely accessible on the DEPFET module, a test board is used carrying only one ASIC per type without a DEPFET matrix. Therefore, the output signals of a single channel can be probed. Keeping the sequence unchanged, the oscilloscope image shown in Fig. 6.11 is obtained.

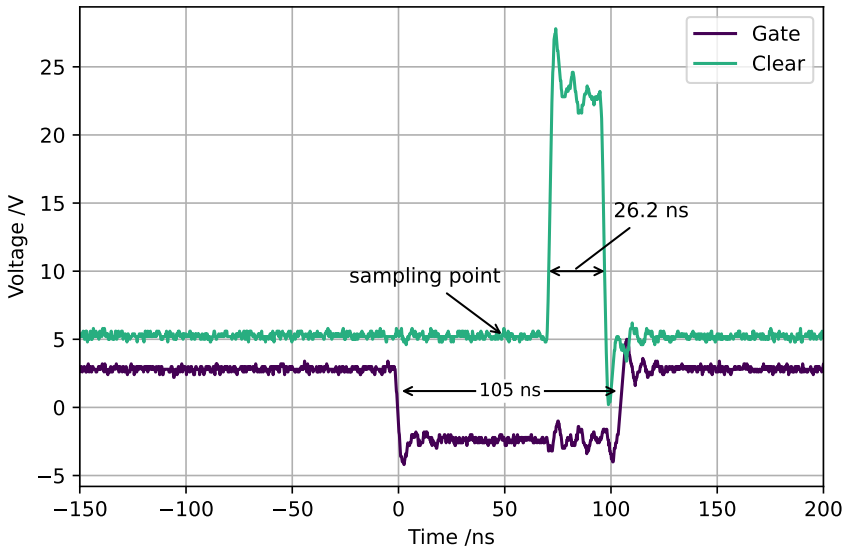


Figure 6.11: Oscilloscope measurement of a SWITCHER channel on a test board. A negative voltage is applied to the gate_4 line to activate the DEPFET pixels. At the end of the readout (*sample point*), the signal charges in the internal gate are cleared by applying a more positive voltage to the clear line.

The measurement illustrates the application of voltages in a SWITCHER channel corresponding to a gate_4 of DEPFET pixels. In this case, the pixels within a gate_4 are activated and the drain current is measured by the DCDs, referred to as *sampling point*. The clearing process starts as soon as the output voltage of ∼20 V is applied to the clear contacts of the pixels. In total, the pixels are activated for approximately 105 ns, including clearing of the signal of about 26 ns. At this stage, the DEPFET matrix is set to rolling-shutter mode (see Fig. 5.4 in Sec. 5.2.1) and further measurements can be performed.

6.5.2 Pedestal recording

In the pedestal measurement, it is assumed that no signal charge is present in the internal gate. The unprocessed pedestal values are obtained by reading the raw data of the DHP memory using the *memory dump* command. The length of the command determines the number of gates_4 for which the pedestal values are to be retrieved. Accordingly, the entire DEPFET matrix of 192 gates_4 is referred to as a *frame*. The pedestals are typically recorded for several frames to determine an average value for each pixel and to identify pixels with high pedestal fluctuations (*noise*). In Fig. 6.12, the pedestals of 60 recorded frames are shown.

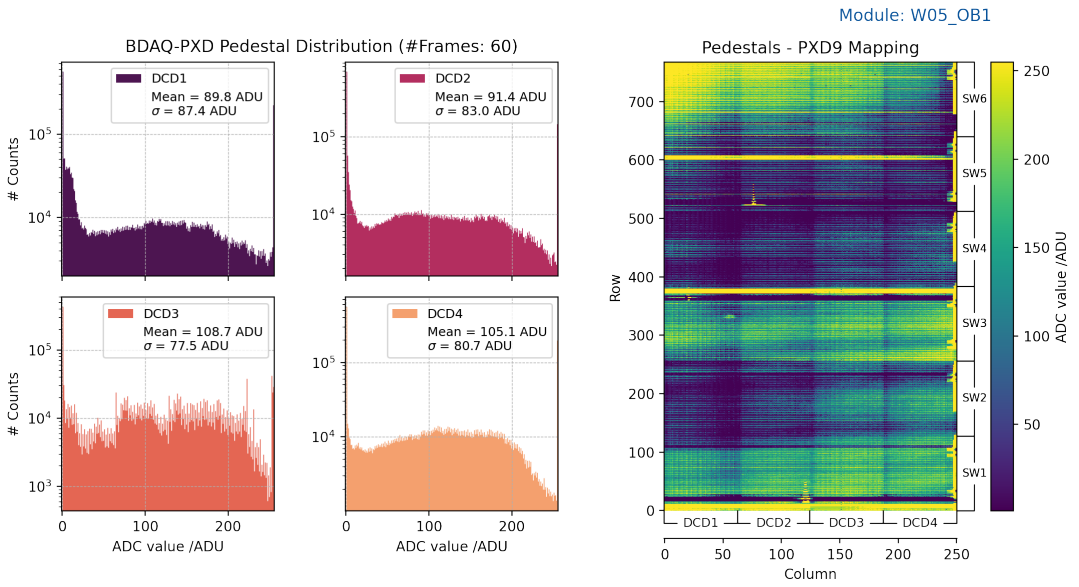


Figure 6.12: Pedestal distribution of the *W05_OB1* module recorded by BDAQ-PXD. *Left:* Subdivided into the pixels of the respective DCDs, the count of pedestal values is shown on a logarithmic scale. *Right:* The mean pedestal values distributed on the DEPFET matrix. The matrix range of DCDs and SWITCHERs are marked.

The recorded pedestals cover the entire dynamic range of the ADCs inside the DCDs. Many of the pixels result in a value of 1 and 255 ADU, which are referred to as non-functional pixels. The matrix shows some areas that are particularly affected. Moreover, entire rows with pedestal values of 255 ADU point to defective SWITCHER channels. Constant pedestal values of 1 ADU can be caused by broken drain lines. A possible explanation for the defects and the non-uniform distribution of pedestals is the impact of the irradiation campaign previously performed with the *W05_OB1* DEPFET module.

To identify pixels showing high fluctuations in the pedestal values within the recorded frames, for example due to temperature fluctuations, the standard deviation of the pedestal values in the recorded frames is considered, referred to as *pedestal noise*. The pedestal noise distribution is presented in Fig. 6.13.

The noise profile shows that the DCD3 records pedestals with the highest noise. The fact that the effect occurs locally in DCD3 suggests that this ASIC is malfunctioning. For further use of the module in this thesis, this ASIC pair of DCD and DHP is masked for the readout.

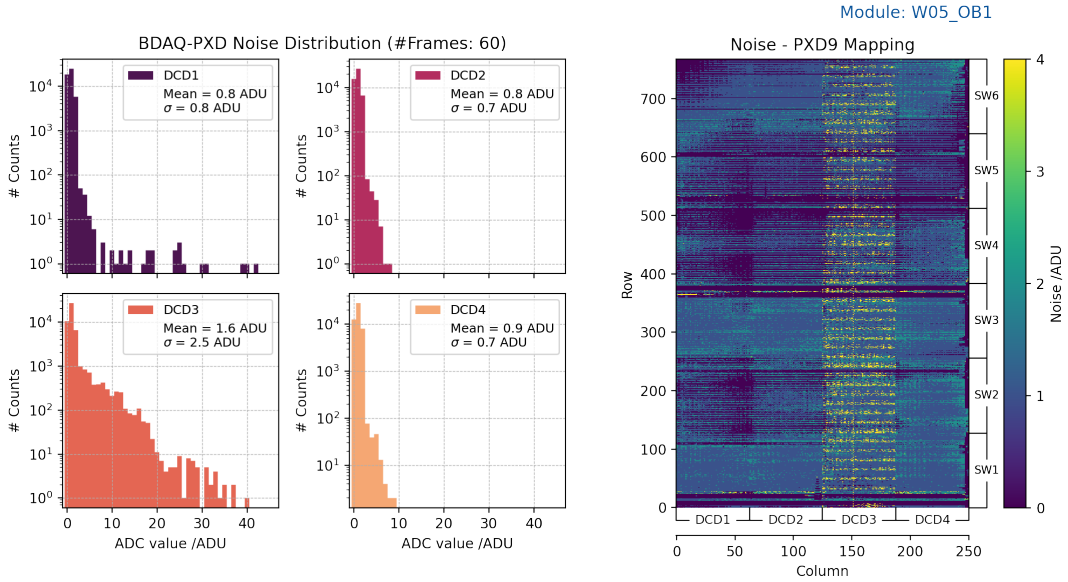


Figure 6.13: Pedestal noise distribution of the *W05_OB1* module recorded by BDAQ-PXD. *Left:* Subdivided into the pixels of the respective DCDs, the pedestal noise is shown on a logarithmic scale. *Right:* Noise values distributed on the DEPFET matrix. DCD3 shows significantly more noisy pixels than the remaining DCDs.

Analogue common-mode correction (ACMC)

The DCD offers a built-in optimisation to reduce common-mode noise, affecting all simultaneously sampled pixels within a gate_4. To suppress this time-dependent offset, the mean value of the drain currents is calculated in all DCD input channels and rerouted by using an analogue feedback [Sch20, p. 48]. Due to the rolling-shutter mode, the calculation is carried out for all pixels within a gate_4. Consequently, a subtraction of the mean value from the measured drain currents is performed. This technique facilitates the compensation of radiation-induced offsets and temperature variations [Per+11, p. 1537].

The correction leads to a narrowing of the pedestal distribution and consequently to a more homogeneous response of the entire sensor, as can be seen in Fig. 6.14. The standard deviation σ of the pedestal distributions is reduced by more than 30 %. Reducing the spread of the pedestal distributions decreases the fraction of the occupied dynamic range of the DCDs. This yields more margin for the measurement of signal charges for the affected pixels. Furthermore, ACMC improves the pedestal noise distribution which can be observed in Fig. 6.15.

Pixels with a pedestal noise of more than 3 ADU are masked for subsequent measurements. The recorded and analysed pedestals are used to perform the zero-suppressed readout of the detector.

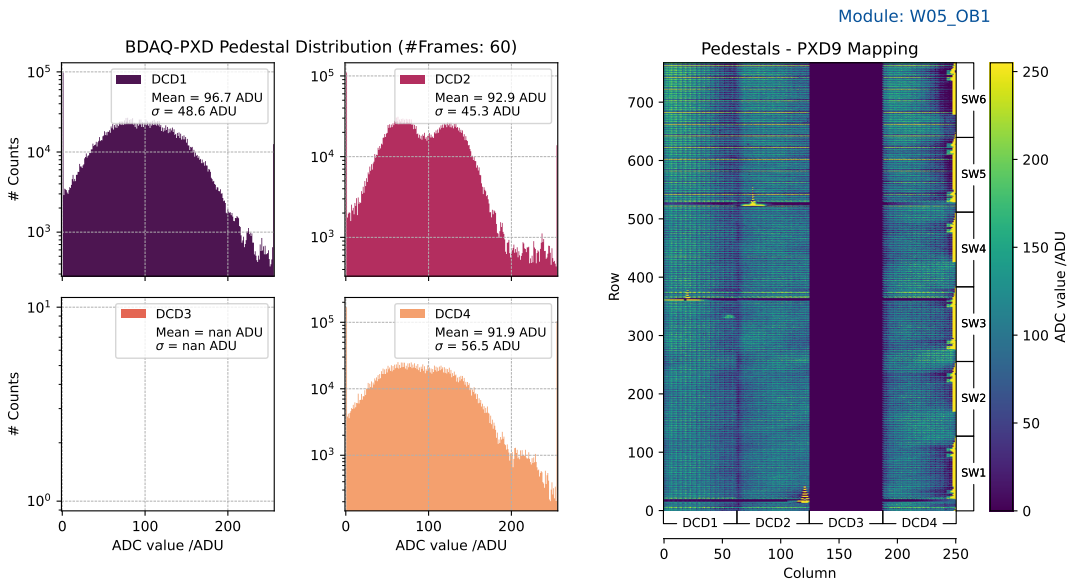


Figure 6.14: Pedestal distribution using ACMC. *Left:* Subdivided into the pixels of the respective DCDs, the count of pedestal values is shown on a logarithmic scale. *Right:* The mean pedestal values distributed on the DEPFET matrix. The third DCD is masked due to malfunction.

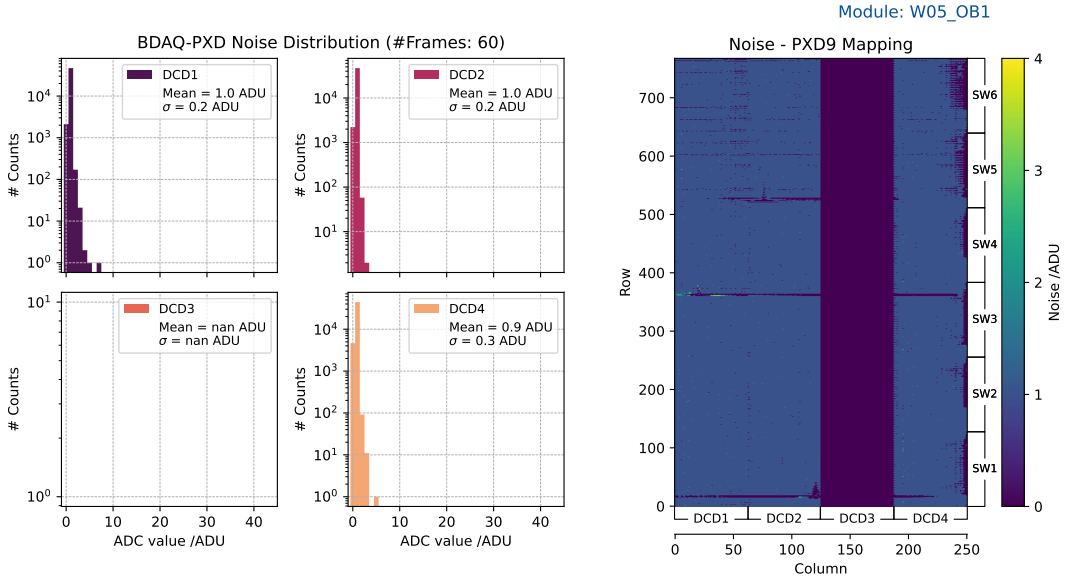


Figure 6.15: Pedestal noise distribution using ACMC. *Left:* Subdivided into the pixels of the respective DCDs, the pedestal noise is shown on a logarithmic scale. *Right:* Noise values distributed on the DEPFET matrix. The third DCD is masked due to malfunction.

6.5.3 Pedestal upload

To perform the DHP-internal zero-suppression (see Sec. 5.2.3), the pedestals are loaded into the dedicated pedestal memory within the DHPs. Via the JTAG interface, the pedestal values are combined into 128-bit words and sent to the corresponding memory address based on their pixel position. The memory structure is described in detail in Sec. 5.2.3.
In BDAQ-PXD, the *JTAG sender* handles the formatting and transfer of the analysed pedestals. Due to temperature influences, the pedestal values of the DEPFET pixels can vary over time. To obtain an accurate result in the zero-suppression, it is necessary to record and upload pedestals prior to each measurement with the detector.

6.5.4 Measurement settings

The settings and functionalities of the ASICs and correspondingly the detector are controlled via the JTAG registers, as described in Sec. 5.3. In the BDAQ-PXD software, the setting values are specified using the configuration-yaml files and loaded into the respective ASICs before starting the measurement. The main settings for the zero-suppressed readout are set in the DHPs and are briefly described in Tab. 6.1. The specified settings affect the output data of the detector. These are described in detail in Sec. 5.2.3.

Setting	Value	Description
`threshold`	7	Data with a value above the threshold + *CM* value are further processed.
`common_mode_correction_en`	1	Triggered data are corrected by the DHP-internal common-mode correction.
`active_ped_mem`	1	Selection of the two pedestal memories to be accessed during subtraction.
`pedestal_subtraction`	1	Pedestals are subtracted from the measured data. Possibility to add a global value to the pedestals (pedestal offset).
`test_mode_en`	0	Test mode to write in DHP memory and store the written data.

Table 6.1: Main settings and default values for the zero-suppressed operation of the DEPFET module.

The *test mode* (`test_mode_en`) feature facilitates the storage of values in the data memory of the DHP (compare Fig. 5.8 in Sec. 5.2.3). In this mode, the DHP does not accept incoming data from the DCD. Consequently, the memory content remains until the mode is deactivated or the DHP is reset. This way, test patterns can be uploaded and, for example, the utilisation of the DHP and the BDAQ-PXD system can be tested with different memory occupancies in

the zero-suppressed readout (see Sec. 6.5.6).

6.5.5 Measurement with a radioactive source

Once all commissioning steps for the detector using the BDAQ-PXD system have successfully been completed, a measurement with a radioactive source is performed. A cadmium source (^{109}Cd) is used to check the response of the DEPFET module to ionising radiation. A picture of the measurement set-up is shown Fig. 6.16.

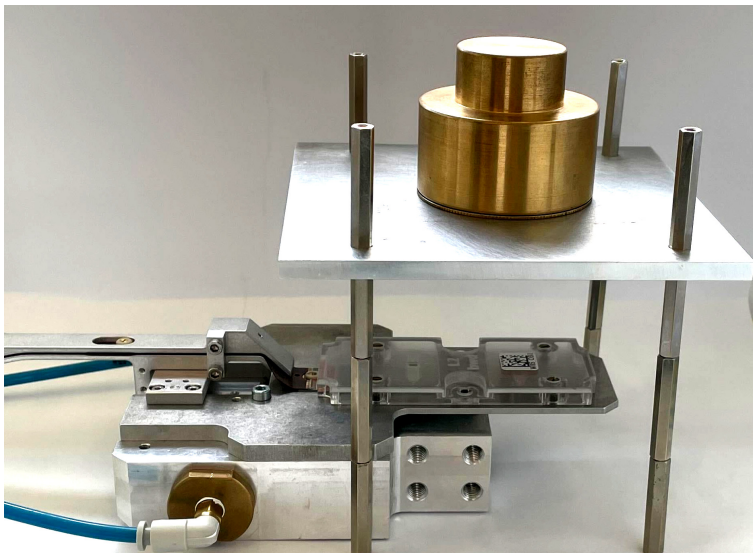


Figure 6.16: Measurement set-up with the cadmium source. The source is placed at a distance of 10 cm above the DEPFET module which is covered by a protective plastic cap. The aluminium holder has a cut-out.

The cadmium source emits photons with an energy of about 22 keV. The data readout is triggered with a frequency of 5 kHz using a TLU (described in detail in Chap. 7). Therefore, the communication between TLU and BDAQ-PXD is tested additionally. The result of the measurement can be seen in Fig. 6.17.
The charge distribution of the single-pixel clusters (charge detected only in one pixel) shows a Gaussian distribution. In the hit map, 15.1 % of the pixels (DCD3 excluded) are masked due to defects in SWITCHER channels, drain lines and noisy pixels. The occupancy offset visible for rows 120 to 220 is caused by the protective plastic cap, located between radioactive source and sensor.

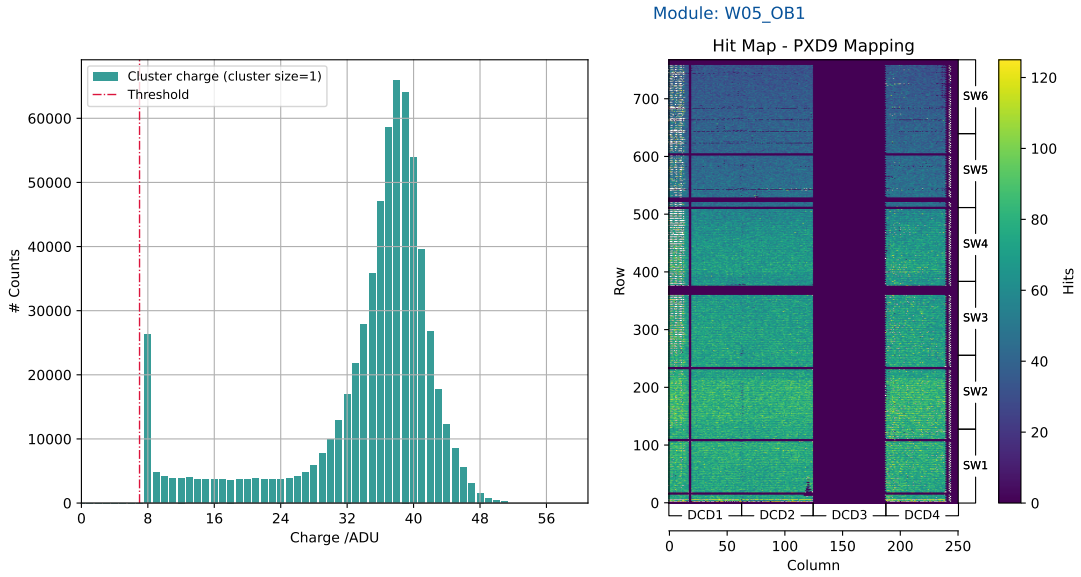


Figure 6.17: Analysed data of the measurement with a cadmium source using the BDAQ-PXD readout system. *Left*: Charge distribution of single-pixel clusters in units of ADU. *Right*: Hit map of the DEPFET matrix. White pixels represent noisy pixels masked after data acquisition.

6.5.6 Error tracing in the DHP

As highlighted in Sec. 6.4, a major advantage of the BDAQ-PXD system is the usability of DHP simulations in combination with real-time measurements. This includes finding and identifying errors and their origin, i.e. in the DHP or the readout system.

An example of an application of BDAQ-PXD is the operation of the PXD in the Belle II detector. Errors can be examined parallel to the running system. During operation of PXD in the Belle II detector using the PXD-DAQ, the recording of corrupted data has occurred repeatedly in high occupancy events [Spr+20, p. 6]. These incidents can be caused by increased background radiation during injections into the accelerator rings.

The corruption of data was perceived by non-continuous frame identifiers (`frame_ID`s) within a triggered event. In order to identify the problem, a high-occupancy event is simulated in the DHP model. A section of the simulation output is depicted in Fig. 6.18.

The data input channels (`DI0-7`) of the DCD mimic a pixel occupancy of 4 %. Subsequently, the zero-suppressed data readout in the DHP model is triggered with a length of four consecutive frames (`trigger_en`). The data buffer (`data_buf_out`) displays the data procession. Indicators for data loss (`data_lost`, `cm_almost_full`, `cm_fifo_full`) show no response.

Afterwards, the output FIFO (`fifo_out_data`) contains the zero-suppressed data and writes it to the output stage. The error becomes obvious when looking at the internal counter of `frame_ID` and the `frame_ID_out` which is attached to the output data.

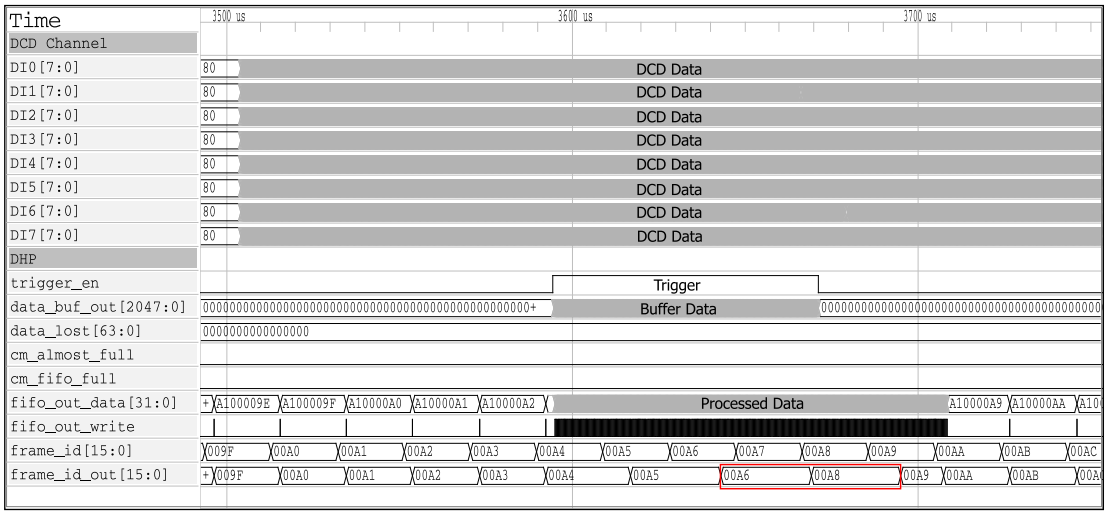


Figure 6.18: Simulation output showing the malfunction in the DHP model. Incoming data from the DCD (`DI0-7`) corresponding to an occupancy of 4 % is triggered for four consecutive frames (`trigger_en`). The `frame_ID_out` jump is marked with a red box.

In this case, the processing time until the data frame is sent exceeds ∼20 µs (corresponds to one frame), resulting in a jump from `0x00A6` (=166) to `0x00A8` (=168).

On-module test: By confirming this error in the DHP model using the simulation, BDAQ-PXD is used to perform a test on the DEPFET module to rule out data loss in these events. Using the test mode featured by the DHP, a test pattern is written to the DHP memory reproducing a localised occupancy of 4 %. In the test pattern, the high-occupancy event is present in DHP2, the remaining DHP memories contain an occupancy of 1 %. The uploaded pattern can be seen in Fig. 6.19.
The right plot shows the recorded `frame_ID` numbers for a certain period of time. First, only the `frame_ID`s without data content are recorded. Once the trigger is received by the DHPs, the zero-suppressed readout starts for exactly four frames. For the three DHPs with 1 % occupancy, four consecutive frames containing data are recorded. Comparable to the simulation, DHP2 skips one `frame_ID` after the third triggered frame. In the measurement, this effect occurs twice.
However, a comparison with the test pattern concludes that all data is obtained, i.e. the data loss in the DHP2 containing a high-occupancy event can be excluded. Nevertheless, this behaviour may cause problems when operating PXD in the Belle II experiment. In case of localised high occupancies (>3 % hit occupancy within the area of a single DHP), it can lead to a misalignment of data from different DHPs due to different `frame_ID`s. Furthermore, a continuous hit occupancy of more than 3 % (∼2 hits per row) leads to possible data loss in the DHPs [Ger19, p. 32].

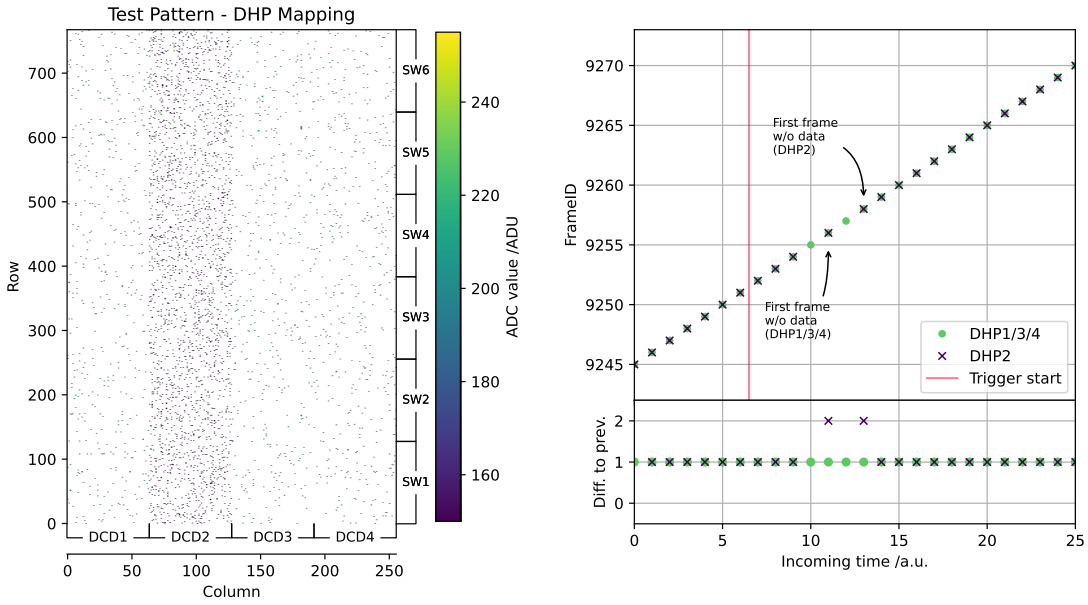


Figure 6.19: Measurement of the DHP malfunction using BDAQ-PXD. *Left:* The test pattern which is loaded into the four DHP memories. In the memory of DHP2, 4 % of the values are assigned with a signal, in the others only 1 %. *Right:* The recorded `frame_ID`s which are sent by the DHPs. Once a trigger is sent, the frames contain data resulting in a `frame_ID` jump in DHP2 (*top*). The *bottom* plot shows the difference to the previous recorded `frame_ID`.

For emerging events during particle injections into the accelerator rings, countermeasures should be taken. Firstly, data could not be triggered using a veto signal. Secondly, the sensor specific mode called *gated mode* could be used. In this mode, no additional charge is collected in the internal gate of the DEPFET pixel for a certain time interval using a modified SWITCHER sequence [Mül17, p. 213].

Based on the evaluation of simulation and measurements, the applicability of BDAQ-PXD has been demonstrated. As a concluding measurement, the BDAQ-PXD system is used in a test beam campaign, which allows for a determination of the hit-detection efficiency of the DEPFET module. The measurement is presented and discussed in Chap. 7.

7 Test beam measurements

The measurements at the Deutsches Elektronen-Synchrotron[1] (DESY) in Hamburg are an essential part of the verification of the functionality of the BDAQ-PXD system. The facility provides electron beams for testing particle physics detectors for the research and development of detectors and their readout systems [Die+19, p. 1].
Dedicated beam telescopes facilitate accurate tracking of individual beam particles traversing the Device Under Test (DUT) to study the hit-detection efficiency of the DUT. Using BDAQ-PXD and the DEPFET pixel detector module, a determination of the hit-detection efficiency can provide insights into the performance of the detector and the newly developed readout system. Moreover, detector parameters, e.g. bias voltages of the DEPFET sensor, can be varied to investigate their impact on the charge collection and detection efficiencies.
This chapter first describes the DESY test beam facility and the measurement set-up. Afterwards, the results of time-integrated and time-resolved efficiency studies of the DEPFET module are presented.

7.1 DESY test beam facility

Electron or positron beams with energies from 1 to 6 GeV can be independently extracted from the DESY II electron synchrotron into three test beam areas simultaneously [Die+19, p. 266]. A drawing of the test beam facility is shown in Figure 7.1.

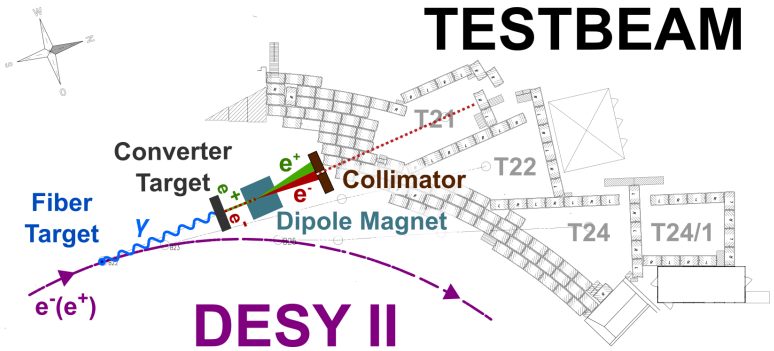


Figure 7.1: Test beam facility at DESY with its beam lines. From [Die+19, p. 267].

[1] engl.: German Electron Synchrotron

The electrons for extraction into the test beam areas are generated in four steps [Die+19, pp. 267-273]:

i Bremsstrahlung photons are generated when electrons in the DESY II synchrotron impinge on a carbon fibre target.

ii After 22 m, photons hit a secondary target. Depending on the test beam area, different target materials and thicknesses can be selected: The interaction of the photons with the target in turn produces electrons and positrons.

iii Using a dipole magnet located 60 m behind the second target, the selection of charge and momentum of the particles (electrons/positrons) is possible. Users are able to change the particle momentum by remotely changing the current of the magnet.

iv The last component is a collimator that can be moved vertically and horizontally.

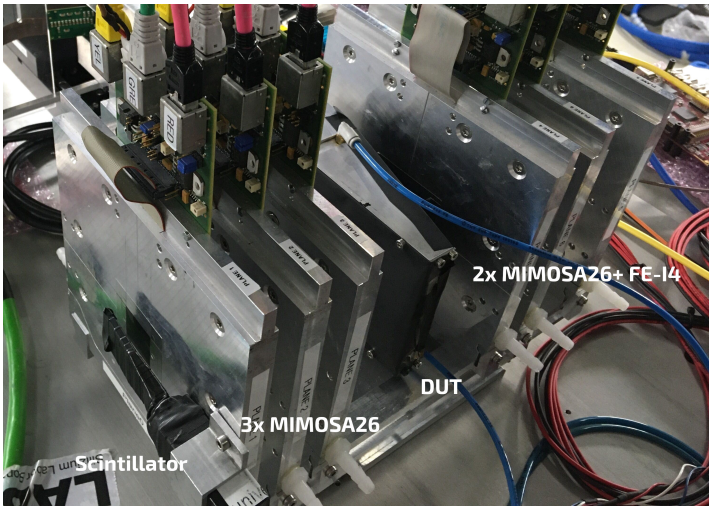
The measurements in the following sections were performed at the test beam area TB22 with an electron energy of 4 GeV. The next section introduces the set-up used in the test beam measurement.

7.2 Test beam set-up

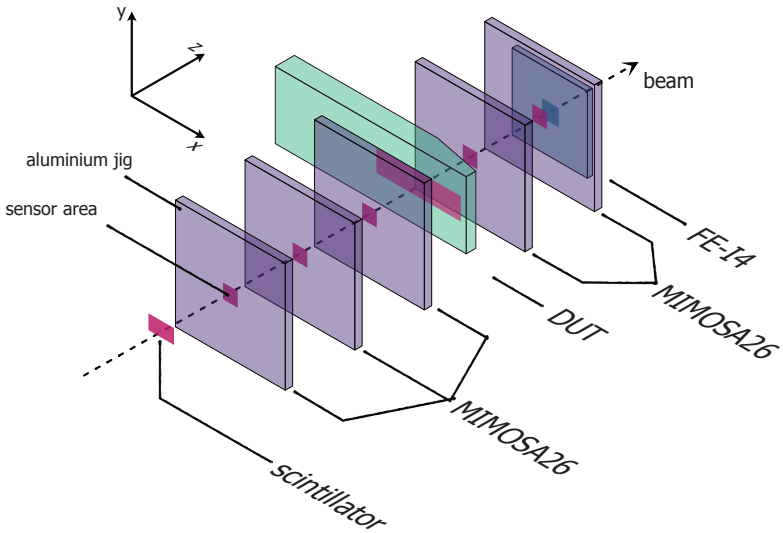
In order to investigate the performance of a DUT connected to a readout system, reference detectors are used in a telescope arrangement. In a typical test beam set-up, the DUT is placed in the centre of the telescope planes which serve as tracking references. In front of the telescope, a scintillator is positioned to generate a trigger once a beam electron traverses the set-up. An additional detector is used as a time reference plane providing a sufficient timing resolution. A picture of the set-up is shown in Fig. 7.2. The set-up consists of one scintillator, five MIMOSA 26 planes and one ATLAS FE-I4 plane (presented in Sec. 3.2.2). The five MIMOSA 26 planes form the ANEMONE telescope (A Nice Mimosa Bonn Telescope) [Hir19, p. 56], a EUDET-type telescope [Jan+16]. The components are briefly described below:

Scintillator : A scintillator is used for triggering on particles passing through the acceptance region of the telescope covered by the pixel sensors. It consists of a scintillator medium and a *Hamamatsu* photo-multiplier tube in combination with light guides. [Die+19, p. 5]

MIMOSA 26 : With a pixel size of $18.4 \times 18.4\,\mu m^2$, the MIMOSA 26 sensor is used to measure the particle trajectories of the incoming beam particles with high resolution. The sensor is fabricated with the AMS 350 nm CMOS technology. [Jan+16, p. 4]
With 1152 columns and 576 rows, the total active area is $10.6 \times 21.1\,mm^2$. Comparable to the DEPFET readout mechanism, MIMOSA 26 sensors are read out in a rolling-shutter mode. Due to a readout frequency of 5 MHz per row (16 cycles of a 80 MHz clock), one frame is read out in a period of 115.2 µs. [Hir19, p. 56]



(a) Picture of the test beam set-up



(b) Schematic drawing of the detector arrangement.

Figure 7.2: (a) Photograph showing the set-up used at the test beam facility at DESY. (b) Schematic drawing of the arrangement for better visualisation. The beam direction is indicated with an arrow pointing in $+z$-direction. Beam particles traverse a scintillator, three MIMOSA 26 planes, the DUT, two more MIMOSA 26 sensors and the FE-I4. The FE-I4 is attached to the back of the aluminium jig of the last MIMOSA 26 plane. The sixth MIMOSA 26 plane of the telescope (shown in the picture) is non-functional.

FE-I4: The hybrid pixel detector using the FE-I4 readout chip is described in detail in Sec. 3.2.2. The readout chip has a size of $18.8 \times 20.2\,\mathrm{mm}^2$ and is divided into 80 columns and 336 rows with 250 µm and 50 µm pixel pitch, respectively. In contrast to the MIMOSA 26

sensor, each pixel cell has its own directly connected readout channel. Moreover, it serves as a time reference plane because timestamps can be recorded with a high precision of 25 ns. The signal generation occurs in the silicon sensor bump-bonded to the readout chip.

The first data recording of the DEPFET module using BDAQ-PXD during activated beam is shown in Fig. 7.3.

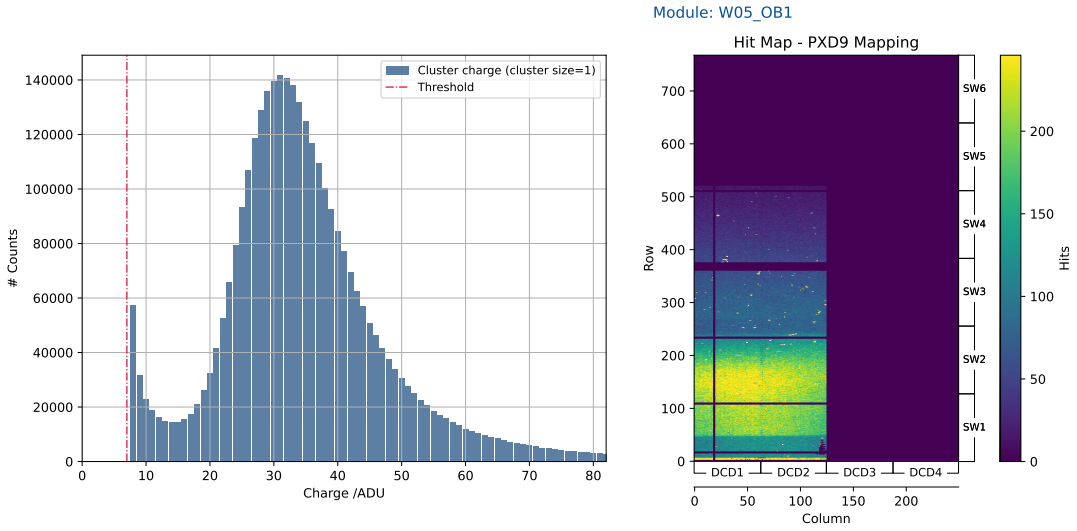


Figure 7.3: *Left:* The clustered charge spectrum of the electron beam recorded using minimum ionising particles and a detector threshold of 7 ADU. *Right:* Hit map of the DEPFET matrix. The areas DCD3/4 and SW5/6 are masked due to low number of hits. Single gates$_4$ are masked if they either do not work or have a large number of noisy pixels.

The charge spectrum for single-pixel clusters follows a Landau distribution. The specified threshold is 7 ADU and hits with charges below that value are not transmitted by the DHPs in the zero-suppressed readout. The corresponding hit map shows the occurrence of most hits in the range of row 40 to 220 and column 0 to 125 of the DEPFET matrix. This can be explained by the beam profile in combination with the detector planes, which transmit a trigger signal to initiate the data readout. The trigger scheme is discussed in the next section.

Pixel masking scheme: The drain lines of DCD3 and DCD4 (columns 125 to 250) as well as the upper rows of the DEPFET matrix are masked for data taking as they register a low number of hits and are not crucial for the following measurements. In addition, four pixel columns and eight gates$_4$ are non-functioning and are consequently masked. Noisy pixels (as described in Sec. 6.5.2), which are identified during the pedestal recording before each new measurement, are masked in the pedestal upload process. In total 6.58 % of the activated area of 520×125 pixels is masked.

7.2.1 Trigger scheme

The scintillator is used to generate a signal for initiating the data collection of all other detectors when a beam electron traverses the telescope. However, since beam electrons do not necessarily cross all sensitive areas, depending on the incidence angle, the use of a single trigger plane can lead to a decrease of the particle reconstruction performance of the telescope. To increase the probability of recording data for electrons whose trajectories cross each telescope plane, a coincidence trigger scheme is used. In the applied scheme, the scintillator and FE-I4 are placed at the beginning and at the end (as seen from beam electrons) of the detector arrangement, respectively (see Fig. 7.2), and used to trigger the readout. The inclusion of the FE-I4 to generate a trigger signal creates a more distinct Region Of Interest (ROI) on the enclosed DUT, as shown in the hit map in Fig. 7.3. The size of the ROI on the DUT is roughly defined by the overlapping region of the sensitive areas of the scintillator ($10 \times 10\,\mathrm{mm}^2$) and FE-I4 ($19 \times 20\,\mathrm{mm}^2$) and is small compared to the DEPFET matrix ($13 \times 61\,\mathrm{mm}^2$). Consequently, a reduction of the data rate is generated with simultaneous improvement of the data quality regarding the telescope. From both devices, the signals are transmitted to the TLU. The TLU serves to process the two signals and transmits a trigger signal to the readout systems of the detectors. The TLU type used is the *EUDET TLU v0.2c* [Cus09]. Fig. 7.4 illustrates the trigger and readout scheme.

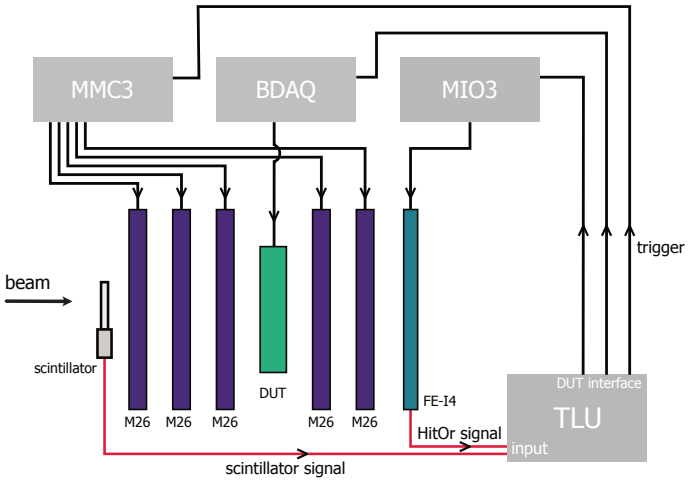


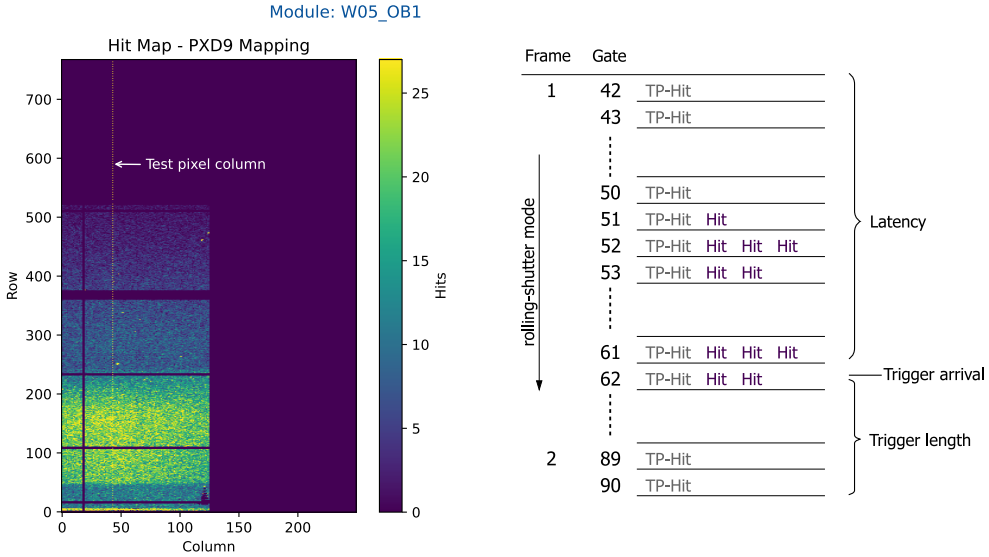
Figure 7.4: Schematic drawing of the trigger scheme using a scintillator and FE-I4 as trigger planes. The TLU receives the two signals and transmits a trigger to the readout systems.

The analogue signal of the scintillator is fed directly into the input channel of the TLU. The signal emitted by the FE-I4 corresponds to the HitOr pulse (see Sec. 3.2.2). If both signals are above the tunable input threshold and arrive in a coincidence time window (maximum length: $31 \times 1.5625\,\mathrm{ns}$), a 32-bit long trigger word (consisting of a trigger number) is sent to the individual readout systems (i.e. MMC3 board for five MIMOSA 26 planes, BDAQ for the DEPFET module (DUT) and MIO3 for FE-I4). For the operation, the TLU uses a 40 MHz clock.

7.2.2 Latency measurement

The relative timing of the individual detector readouts has to be carefully evaluated for a correct measurement. Therefore, the signal delays of the sub-systems have to be determined. In the event of an incoming particle crossing the detector layers and leaving a signal in the scintillator and FE-I4, the trigger generation process is started using the TLU. If a hit is also generated in the DEPFET matrix, the random gate_4 position of the rolling-shutter causes the hit to be either in a gate_4 before or after it. Since at least one complete frame (192 gates_4) is triggered, the hit is written to the DHP memory between 1 and 192 gates_4 later. Therefore, depending on the duration of the trigger generation, memory data containing gates_4 before the trigger arrival have to be regarded.

The ability to read previous data (in relation to the trigger arrival) is facilitated by the *latency* setting. The setting defines which data from the DHP memory is considered to belong to a particular readout window. It describes the difference between data written into the memory and trigger arrival to the DHP in the number of gates_4. To determine the correct latency setting, test pixels are activated by setting the corresponding DHP stored pedestal value to 0. Consequently, after zero-suppression, these pixels yield a hit as long as their actual pedestal value surpasses the threshold setting. In Fig 7.5a, the hit map with an activated test pixel column is shown.



(a) Hit map with test pixel column.

(b) Working principle of test pixels.

Figure 7.5: (a) Hit map showing the activated test pixel column. Each working gate contains at least one pixel in every readout. The colour scale is limited to the 99^{th}-percentile of the hit distribution. (b) Schematic drawing showing the process of using test pixels. One test-pixel hit (*TP-hit*) appears in every readout gate_4. TP-hits can be used to determine the first gate_4 of the readout and its distance from a particle hit (*Hit*).

The activated test pixels allow for a determination of the beginning of the readout frame from the recorded data. A sketch of the working principle is depicted in Fig. 7.5b.
Using the marked outline of the readout frame, the position of the hits caused by the triggering electron can be found in relation to the frame. To determine the optimal latency, measurements are performed with two different settings and the distance between the first transmitted gate_4 (test pixel) and the first hit different from a test pixel is plotted. In both cases, a trigger length of 211 gates_4 is used. The result is depicted in Fig. 7.6.

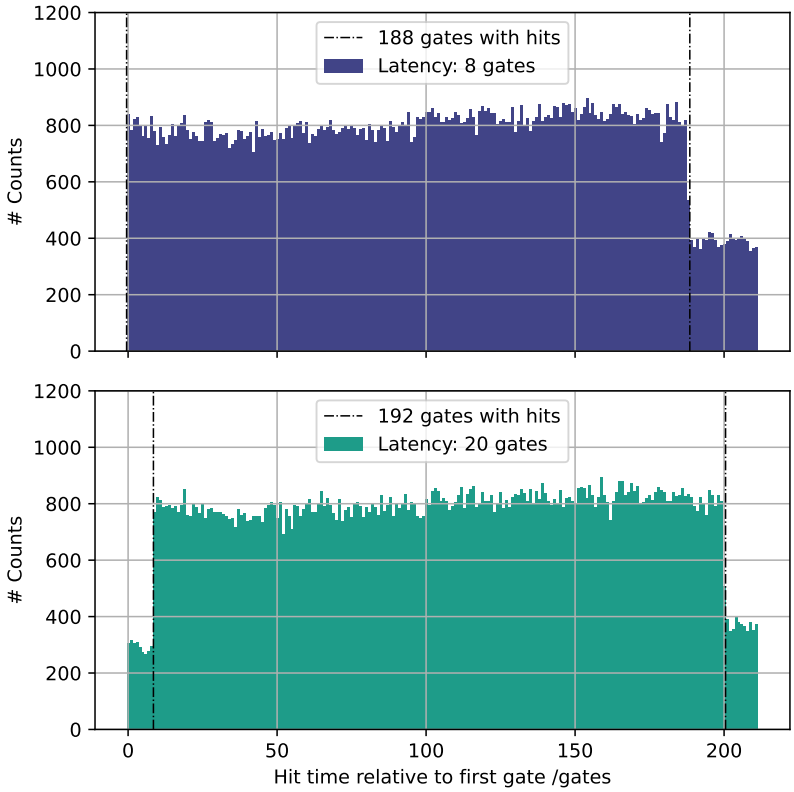


Figure 7.6: Trigger-timing measurement with selected latency settings of 8 gates_4 (*top*) and 20 gates_4 (*bottom*). The distance of the hit relative to the first gate_4 read out is given in units of gates_4.

As mentioned before, the position of the active gate_4 (in the rolling-shutter readout) is randomly distributed. Therefore, the plotted hit distance relative to the first gate_4 read out yields a uniform distribution. Both plots of the assumed hit positions within the readout frame show an increased number of counts corresponding to the actual trigger window. To correctly include the DEPFET module data of the triggering particle, the readout frame chosen by latency and trigger length has to include the entire trigger window of 192 gates_4.
For a latency setting of 8 gates_4, the window is truncated and shows no clear boundaries. It

indicates that potential hits are not considered as they are stored before the first readout gate_4 in the DHP memory. In order to take the delay of trigger generation into account, the latency setting must be increased, as can be seen in the measurement at latency setting of 20 gates_4. The resulting plot shows the entire trigger window with its 192 gates_4. Hits prior to and after the trigger window are caused by noise hits and hits from non-triggering electrons. In the following, all measurements are carried out with a latency setting of 20 gates_4.

7.3 Test beam analysis

For the investigation of the performance of the DEPFET module and thus also of the BDAQ-PXD system, a comprehensive analysis including all detector layers is essential. For the following hit-detection efficiency analysis, the *Beam Telescope Analysis* (BTA) framework is used [Silb]. The software offers a fast and precise analysis of the recorded data of all telescope planes in combination with the DUT in a test beam environment. Particle tracks are reconstructed from the recorded hits of the telescope.
For the set-up shown in Sec. 7.2, the telescope geometry with previously measured distances is depicted in Fig. 7.7.

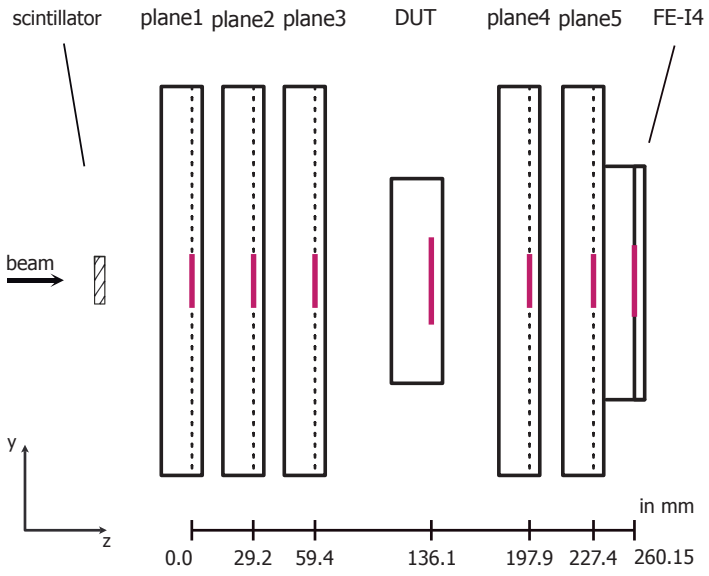


Figure 7.7: Cross-section of the test beam set-up at DESY showing the measured distances between individual telescope planes and the DUT. The DUT (DEPFET module) is enclosed by the telescope consisting of three MIMOSA 26 and one scintillator on the upstream side and two MIMOSA 26 and a FE-I4 on the other.

The reconstruction of particle tracks and the further calculation of hit-detection efficiencies in BTA is performed in sequential steps and produces plots after each step to analyse the quality

of the selected settings. The analysis stages of the framework are described in detail in [Poh20, pp. 75-78] and [Die22, pp. 65-69].
In the following, a brief outline of the sequential structure is presented:

1. Create hit table of all detector planes
   - Convert hit information of DUT, telescope planes and FE-I4: Event number, column and row position of the hit and the deposited charge.
2. Generate noisy pixel masks
   - Neighbouring pixels are compared to each other on the basis of their occupancy and masked in the case of large discrepancies. Additionally, hits below a set limit are masked.
3. Clustering
   - Neighbouring hits in an event are merged and depending on the weighting of the recorded charge of the pixels, a centre of gravity is determined as the new cluster position.
4. Alignment of planes
   - Correlate hit positions on each detector plane with the first MIMOSA 26 plane.
   - Create pre-alignment, take first plane as reference.
   - Create alignment, take first and last telescope plane as reference.
5. Track finding and fitting
   - A track candidate list is generated with a rough classification of the distance of the hits in the detector planes to each other.
   - Fit the track candidates using a Kalman filter [Sch14, p. 53], assign quality flags, and create a track table.
   - Additional track selection cuts are applied on the tracks in the table (track quality $\chi^2_{\text{red}} \leq 10$).
   - Calculate the unconstrained *residuals* (shown in Fig. 7.8) from the selected tracks to verify the track reconstruction.
6. Hit-detection efficiency calculation

After each step, a validation of the analysed test beam data is necessary. A quality measure for the alignment of the detector planes and track reconstruction using BTA is the *residual* distribution. The residual is defined as the distance between a recorded DUT hit and the intersection of the associated reconstructed track with the DUT. A correct alignment of the

planes and track reconstruction results in a Gaussian distribution with width σ_{res}. Assuming negligible influences of the reconstruction software, the width is composed of [Die22, p. 68]:

$$\sigma_{\text{res}} = \sqrt{\sigma_{\text{int}}^2 + \sigma_{\text{point}}^2},$$

with the intrinsic resolution σ_{int} and the pointing resolution of the telescope σ_{point} (few µm [Die22, p. 68]). The residual distribution in x-direction (pixel size of 50 µm) measured with the DEPFET module after alignment is shown in Fig. 7.8.

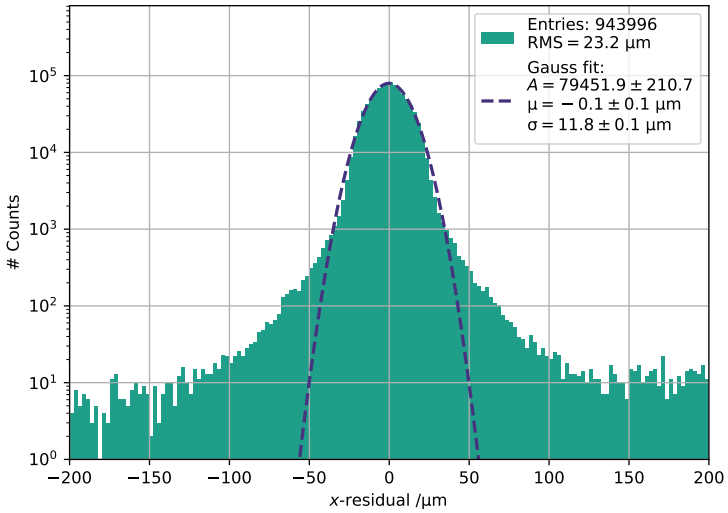


Figure 7.8: Residual profile of the DUT in x-direction (pixel pitch of 50 µm). The distribution is fitted with a Gaussian function. The counts are shown on a logarithmic scale.

The result of the fit with a Gaussian function shows no observable offset. Furthermore, a standard deviation of 11.8 µm is measured which is slightly lower than the binary intrinsic resolution of $50\,\mu\text{m}/\sqrt{12} = 14.4\,\mu\text{m}$ due to charge sharing [Wie21, p. 113]. The uniform background of the distribution arises from incorrectly reconstructed tracks.

7.4 Hit-detection efficiency measurement

The hit-detection efficiency measurement is an essential part of test beam measurements in order to qualify the DUT and to find possible errors in the readout chain of the BDAQ-PXD readout system. As explained above, reconstructed tracks are extrapolated onto the DUT. Within a search radius d_{search} of 150 µm, it is examined whether a spatially and temporally correlated hit can be associated to the reconstructed track. Accordingly, the hit-detection efficiency ϵ can be

expressed as:

$$\epsilon = \frac{n_{\text{detected}}}{n_{\text{total}}}, \tag{7.1}$$

with the number of tracks with an associated hit on the DUT n_{detected} and the number of all reconstructed tracks n_{total}. For the purpose of this measurement, the hit-detection efficiency is calculated for the DEPFET module *W05_OB1* controlled with the BDAQ-PXD readout system and the result is shown in Fig. 7.9. To get a better overview of the relevant area of the DEPFET matrix, an enlargement is included in the plot on the left.

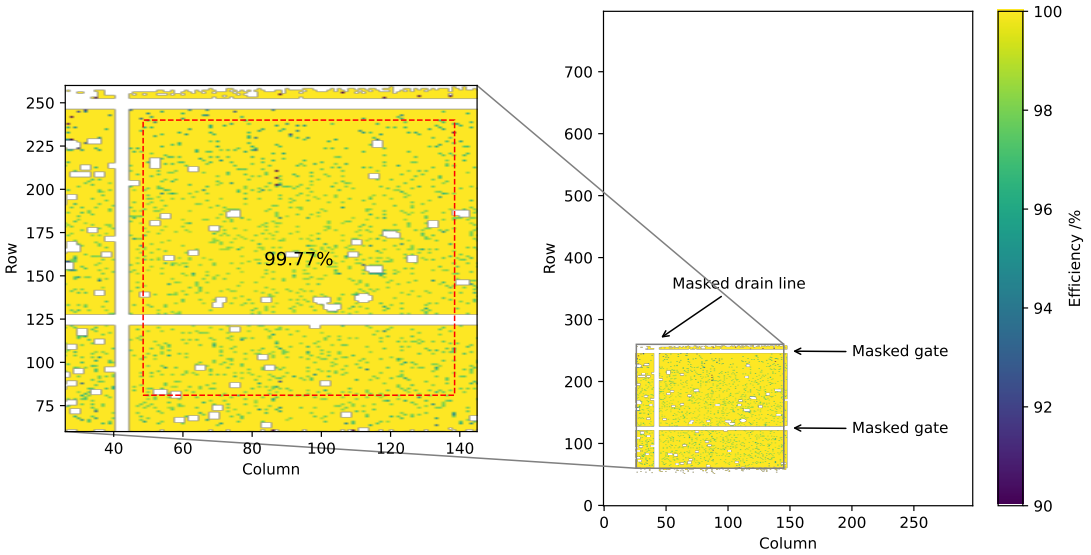


Figure 7.9: Hit-detection efficiency of the DEPFET module using the BDAQ-PXD readout. The considered area of the DEPFET matrix is created by the overlap of the small sensor areas of the trigger planes (scintillator and FE-I4). Noisy pixels, two gates$_4$ and four pixel columns are additionally masked (*white pixels*).

Additional white pixels/areas in the efficiency map originate from the masking of non-functioning or noisy pixels excluded from analysis. Clearly visible are the two masked gates$_4$ and four pixel columns (corresponding to 16 drain lines). The measured average hit-detection efficiency with statistical uncertainty for a selected threshold of 5 ADU is:

$$\epsilon = (99.77 \pm 0.01)\,\%.$$

An evaluation of this result and thus a conclusion about the functionality of the readout system can only be made by comparing further efficiency measurements using DEPFET modules. In [Sch20, p. 142] and [Wie21, p. 123], hit-detection efficiency measurements are presented using the same DEPFET module (*W05_OB1*) but independent readout system (PXD-

DAQ) and test beam analysis framework. The results: $(99.69 \pm 0.04)\,\%$[2] [Sch20, p. 142] and $(99.6 \pm 0.2)\,\%$[3] [Wie21, p. 123] are comparable to the measured value, which supports the statement about the successful development and testing of the BDAQ-PXD readout.

7.4.1 Statistical and systematic uncertainties

The error in determining the average hit-detection efficiency is composed of a *statistical* and a *systematic uncertainty*. The origin and the effect of the uncertainties on the hit efficiency are described in detail in [Poh20, pp. 79-88]. This section summarises the most important effects.

The *statistical uncertainty* depends on the detector efficiency and the number of reconstructed tracks. For the test beam measurements presented in this thesis, about 1×10^6 tracks are reconstructed. At a detector efficiency of more than 99.0 %, a statistical uncertainty of less than 0.03 % is obtained [Poh20, p. 80].

The determination of *systematic uncertainties* is not trivial and requires the consideration of many effects in the analysis of test beam data. In the following, only the most important selection effects of the track reconstruction and the association with a DUT hit cluster on the hit efficiency are discussed:

- d_{search}: The parameter specifies the maximum radius around the reconstructed track in which a hit cluster of the DUT is associated with the track. The influence on the hit-detection efficiency is shown in Fig. 7.10a by varying the parameter. For the increase of d_{search} above 100 µm, a flattening of the efficiency increase is observed. Therefore, it can be concluded that the influence of, for example, the association of noise hits to a track as well as of incorrectly reconstructed tracks on the efficiency is not significant. Moreover, the impact of noise masking before data recording and in the analysis cause a decrease in efficiency overestimation. Under the assumption that a search radius of less than 10 % of the beam size D is chosen (assuming a square beam), the overestimation of the efficiency is below 0.03 % [Poh20, p. 84]. With an applied value for d_{search} of 150 µm and a beam size of a few millimetre [Die+19, p. 40], this estimation is met.

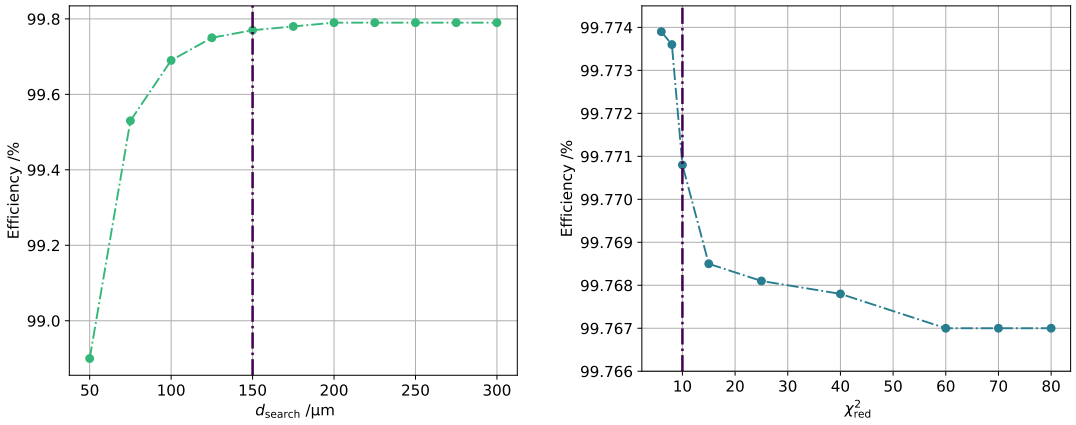
- Track quality χ^2_{red}: The quality of a track is given by the reduced χ^2_{red} of the track fit. Large values of the track χ^2_{red} can result from the inclusion of noise hits in the track reconstruction. Consequently, this can increase the probability of selecting fake tracks. The effect of the track quality on the hit-detection efficiency using cuts on the χ^2_{red} distribution is given in Fig. 7.10b. An increase in efficiency can be seen for smaller maximum χ^2_{red} values which is equivalent to a selection of higher quality tracks. Nevertheless, the maximum deviation in the selected cut range does not exceed 0.01 %.

[2] The stated hit-detection efficiency is the mean value over the entire sensor. The uncertainty is the standard deviation over the measured areas.
[3] See footnote 2

- N_{hit}: This setting determines the minimum number of telescope detector planes from which a track can be reconstructed.
  Due to a hit-detection efficiency of roughly $\epsilon_{\text{M26}} = 98\,\%$ [Jan+16, p. 14] for the five individual MIMOSA 26 detectors, a restriction of the maximum value of N_{hit} causes a decrease in the number of reconstructed tracks. Consequently, the efficiency is overestimated if hits from unreconstructed tracks contribute to a track with no hit on the DUT [Poh20, p. 81]. The binomial distribution can be used to calculate the probability with which a track is reconstructed with at least N_{hit} hits in N_{tel} telescope planes [Die22, p. 84]:

$$P_{\text{rec}} = \sum_{k=N_{\text{hit}}}^{N_{\text{tel}}} \binom{N_{\text{tel}}}{k} \epsilon_{\text{M26}}^{k} (1 - \epsilon_{\text{M26}})^{N_{\text{tel}}-k}.$$

  Reducing $N_{\text{hit}} = 5$ to $N_{\text{hit}} \geq 4$, only 1 % of the tracks are not reconstructed instead of 10 %. As a result, the overestimation of efficiency can be reduced.



(a) Variation of the search radius d_{search}

(b) Variation of track χ^2_{red}

Figure 7.10: (a) Hit detection efficiency for variation of the search radius d_{search} for an associated hit. Calculated with $\chi^2_{\text{red}} \leq 10$ and $N_{\text{hit}} \geq 4$. (b) Efficiency depending on track χ^2_{red} determined with $d_{\text{search}} = 150\,\mu\text{m}$. After [Die22, p. 85].

7.4.2 High-voltage and threshold influences

A common type of detector test for high-energy physics experiments is to consider the effects of changing parameter settings (e.g. bias voltages) on the hit-detection efficiency. The aim of this study is to investigate the impact of varying the detection threshold and the High Voltage (HV) of the DEPFET module on the hit-detection efficiency. For different parameters of both settings, data is recorded in the test beam and the efficiency is determined. The result for various thresholds and HV settings can be seen in Fig. 7.11.

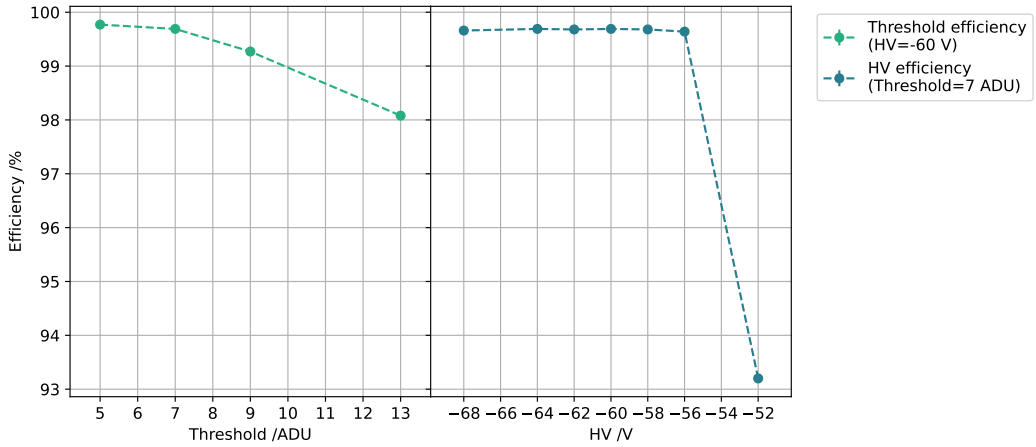


Figure 7.11: Hit-detection efficiency for various thresholds (*left*) and high-voltage (*right*) settings. For an increasing threshold and for more positive high voltage, the efficiency decreases. The same area as shown in Fig 7.9 is used for the hit-detection efficiency calculation. The error bars are too small to be seen.

The observed decrease in hit-detection efficiency of $\sim$1.7 % for increasing thresholds can be explained as following. When the threshold in the DHP is raised, pixel hit information with charge below the threshold is not transmitted. Consequently, individual hits or charge shares of a cluster could not be considered. The higher the threshold, the more charge is removed from the charge distribution in Fig. 7.3. However, reducing the threshold to very small values leads to an increase in noisy pixels resulting in an increase of detector occupancy and data size. In the case of continuous occupancies above 3 %, a loss of data in the DHPs is possible (described in Sec. 5.2.3).
In comparison, the hit-detection efficiency seems to decrease more sharply for more positive high-voltage settings for the active area of the DEPFET module. In the next section, this effect is investigated in more detail at pixel level by performing an in-pixel study.

7.4.3 In-pixel charge and efficiency measurement

In the in-pixel study, the recorded test beam data is mapped onto 2×2 DEPFET pixels. This is achieved by a pointing resolution at the DUT of a few µm. Fig 7.12 shows the in-pixel mean cluster charge map for high-voltage settings of -52 V and -60 V. The average collected charge is noticeably highest in the centre of the pixels. At the longer sides of the pixels, a reduction of the collected charge can be seen in the case of HV $= -52$ V. The lowest mean charge is found in the corners of the pixels. The fact that these low-charge regions do not appear between the two pixels on top of each other is due to the design of the pixels, in which two pixels share one source implant. The pixel design of 2×2 DEPFET pixels is depicted in Fig. 7.13.

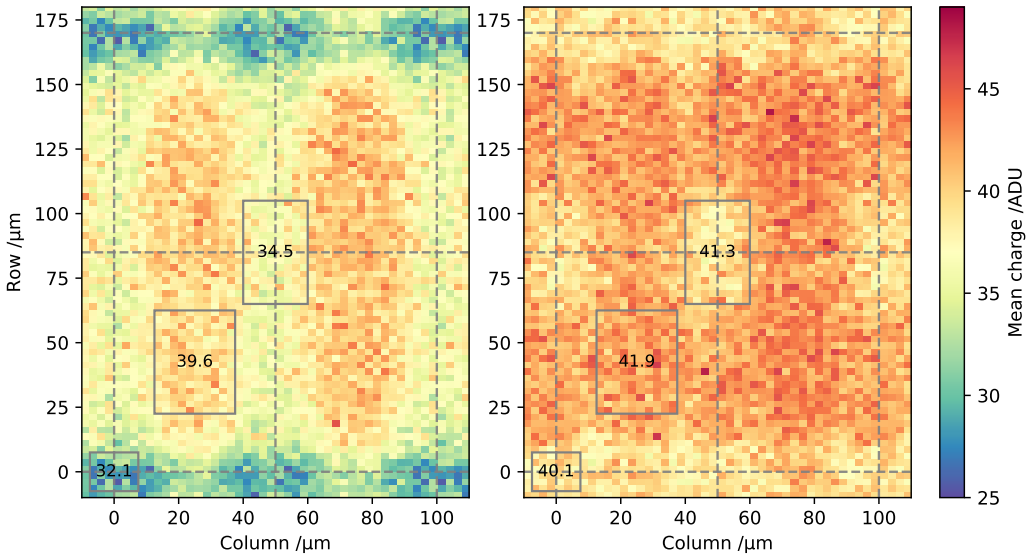


Figure 7.12: In-pixel mean cluster charge map for two HV settings (*left*: HV = −52 V, *right*: HV = −60 V). The grey dashed lines indicate a pixel pitch of $50 \times 85\,\mu m^2$.

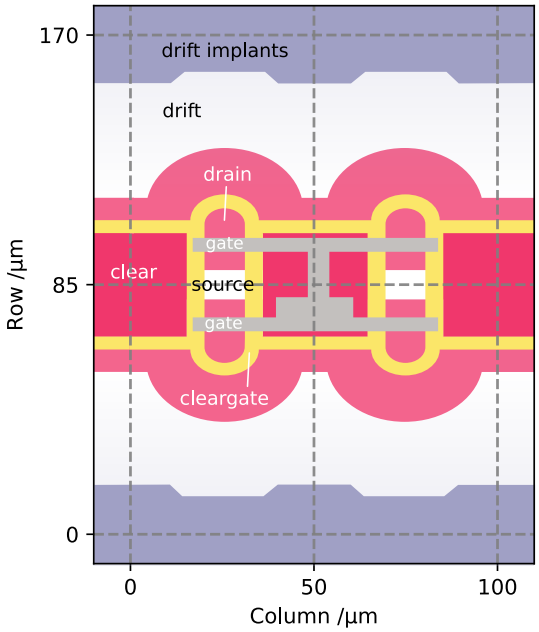


Figure 7.13: DEPFET pixel layout for 2×2 pixels. One source and clear implant are each shared by two pixels. The cleargate surrounds the pixels and, like the external gate, is made of polysilicon. Light red indicates an n-doped implant. Enclosing drift implants (p-doped) enhance the field by creating space charge. Both provide shorter lateral drift times of the signal charges. Adapted from [Mül17, p. 85].

As described in Sec. 3.3, the generated signal charges first drift through the silicon bulk towards the frontside of the DEPFET structure before drifting laterally towards the internal gate. The higher the voltage at the backside, the closer are the potential minimum and thus the trajectories of the signal charges to the frontside [Mül17, p. 88]. The lateral drift is mainly caused by the drift voltage and the implementation of deeper implants [PXD16, p. 31]. As shown in Fig. 7.13, drift implants and an n-implant (light red) attract the signal charges in the direction of the internal gate. At $\mathrm{HV} = -52\,\mathrm{V}$, the minimum potential is created further from the frontside and charges generated below the outer drift implants are less affected by the drift field. Especially in the corners of the pixels, the signal charges can diffuse further and reach other pixels, possibly generating a signal below the threshold. Comparably, a reduced charge collection for signal generation below the clear implant is obtained. In this case, the *deep p-well* located 1 µm [Ric22] below the clear implant (see Fig. 3.9 in Sec. 3.3.1), and influenced by the backside voltage, is not a sufficient barrier.
At more negative HV ($\mathrm{HV} = -60\,\mathrm{V}$), these effects are suppressed. Nevertheless, it is visible that less charge is collected when it is generated below the clear implant and in the distant drift implants. In addition, the change in the electric fields becomes obvious when looking at the mean cluster size map in Fig. 7.14.

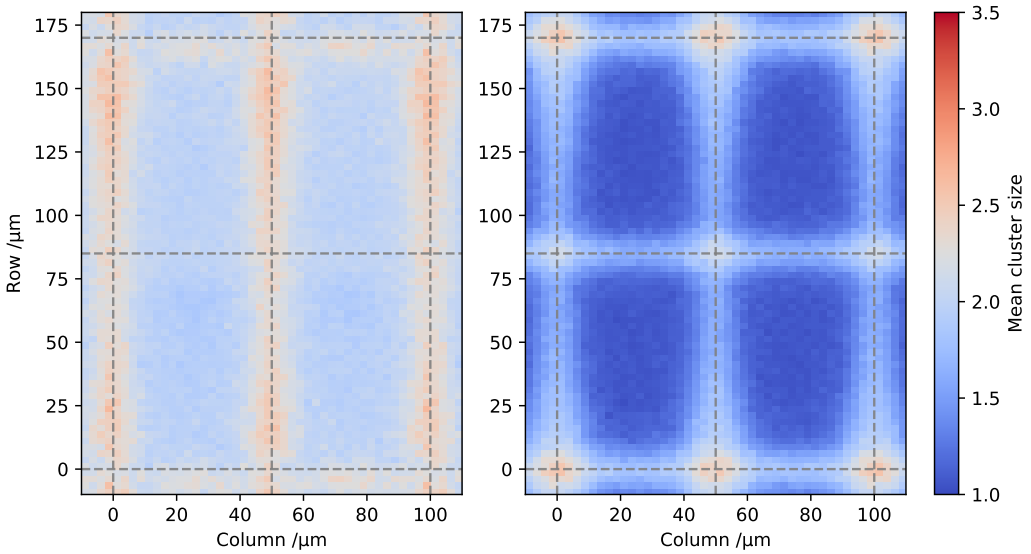


Figure 7.14: In-pixel mean cluster size for different HV settings (*left*: $\mathrm{HV} = -52\,\mathrm{V}$, *right*: $\mathrm{HV} = -60\,\mathrm{V}$). The grey dashed lines indicate a pixel pitch of $50 \times 85\,\mu\mathrm{m}^2$.

For an insufficient HV, the mean cluster size in the centre of the pixels is ∼2. Accordingly, charges generated in the centre can still be shared with surrounding pixels. Once the HV is increased ($\mathrm{HV} = -60\,\mathrm{V}$), a mean cluster size of ∼1 is obtained in the central region. Therefore, the charge is collected on average in one internal gate. Exceptions are the edges of the pixels,

where the probability of charge sharing is increased.
The final consideration addresses the spatial degradation of the in-pixel hit-detection efficiency. For this reason, the high-voltage settings of $-52\,\mathrm{V}$ and $-60\,\mathrm{V}$ are used again. In Fig. 7.15, the in-pixel efficiency maps are presented for both settings.

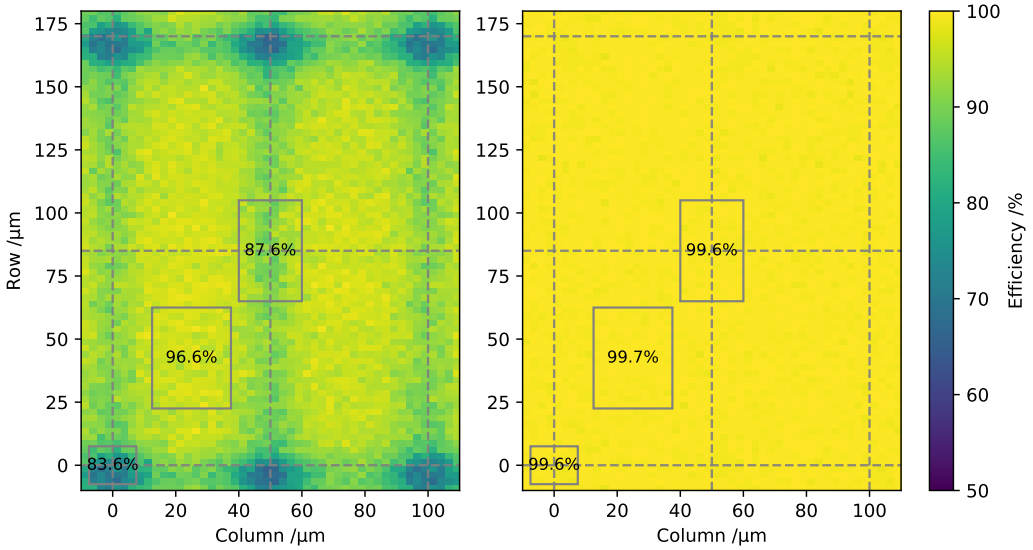


Figure 7.15: In-pixel mean hit-detection efficiency for different HV settings (*left*: $\mathrm{HV} = -52\,\mathrm{V}$, *right*: $\mathrm{HV} = -60\,\mathrm{V}$). The grey dashed lines indicate a pixel pitch of $50 \times 85\,\mu\mathrm{m}^2$.

The effect described above, which leads to the loss of generated charge on the way to the internal gate, is also reflected in the in-pixel hit-detection efficiencies. For an insufficient high voltage, the charges generated at the edges of the pixel contribute less likely to a signal, resulting in inefficiencies in these areas. At larger high voltages, these effects are suppressed resulting in an improvement of the hit-detection efficiency.

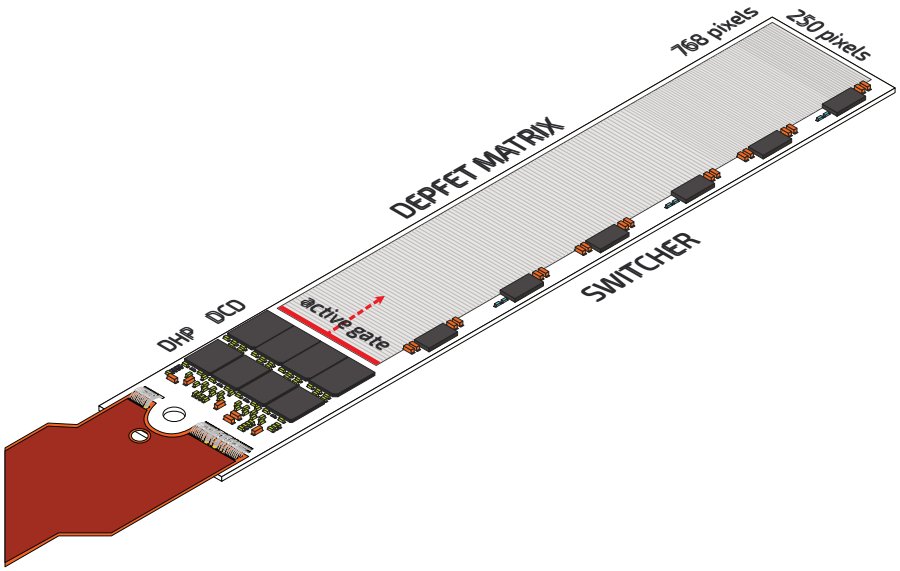
7.5 Time-dependent efficiency measurement

Ideally, the measurement principle of the DEPFET technology, measuring non-destructively the signal charge in the internal gate, should be fully efficient in the detection of the electrons in the test beam. The motivation for this qualitative study derives from the determination of the hit-detection efficiency in the previous section as well as measurements with different DEPFET modules [Wie21, p. 123], each of which shows an emerging, albeit small, inefficiency. An effect of the detection threshold cannot fully explain this inefficiency as the efficiency appears to saturate at a decreasing threshold as can be concluded from Fig. 7.11.
One process that is indispensable in the operation of DEPFET pixels and is particularly relevant to consider is the clearing mechanism described in Sec. 3.3.1. As described in Sec. 5.2.1, the DEPFET pixels are read out in a rolling shutter mode, see Fig. 7.16a. Therefore, the SWITCHER turns on the gate_4 to enable the sampling of the drain currents by the DCDs, followed by the clearing of the signal charges. During the clearing period, a more positive voltage is applied to the clear implant.
In this study, the influence of the activation and clearing process on the hit-detection efficiency of the DEPFET module is investigated. At any time during operation, a gate_4 of the DEPFET matrix is activated. With 192 gates_4 in total, the probability for an electron traversing the activated gate_4 is $1/192 \approx 0.52\,\%$, as shown in Fig. 7.16b. In Sec. 5.2.1, Fig. 5.4 shows a clearing pulse sent by the SWITCHER for about 1/4 of the time the pixels are activated. This reduces the probability of passing through gate_4 during the clearing process to $0.13\,\%$. Consequently, generated charges of beam electrons could not reach the internal gate but are attracted by the clear implant. In case the clearing process affects the charge collection of generated charge by impinging ionising particles, it could be an essential component of the inefficiency. The next section outlines the steps required to conduct the study.

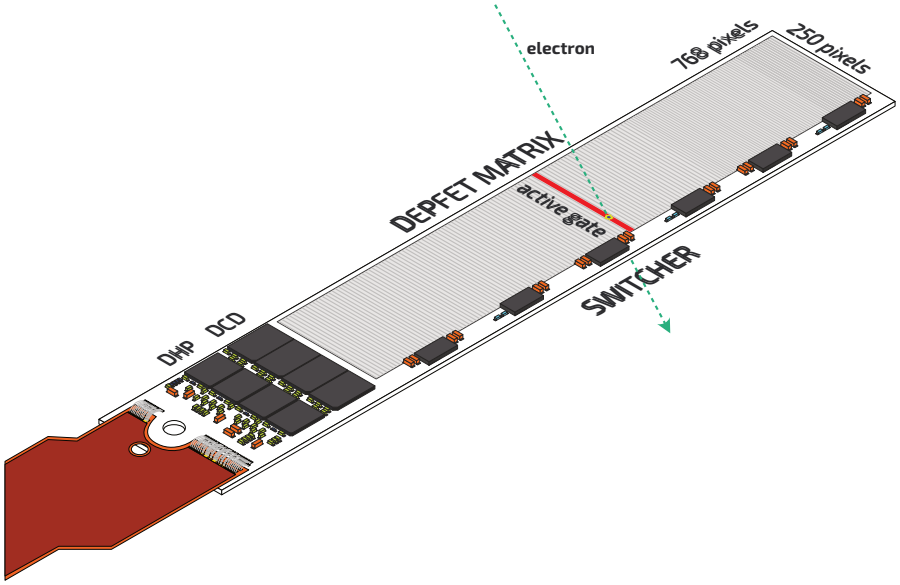
7.5.1 Timestamp measurement

A crucial part of this measurement is the information about the state of the readout cycle, i.e. which gate_4 is activated. Therefore, a timestamp counter is integrated into the BDAQ-PXD firmware. The timestamp is incremented by one every 100 ns (10 MHz), corresponding to the gate_4 switching time ($\sim$100 ns). The required steps for the measurement in the test beam are listed below.

1. The counter is started (timestamp is set to 0) by transmitting a reset signal to the DHPs. On the detector side, the SWITCHER sequence in the DHP is restarted, referred to as a *frame synchronisation* (see Sec. 5.2.3). Accordingly, $\text{gate}_4 = 1$ is activated and cleared next resulting in a temporal alignment of the timestamp with the gate_4 switching of the DEPFET matrix.



(a) In the rolling-shutter mode, the DEPFET matrix is read out gate_4-wise (4 rows at the same time). Within ∼100 ns, the pixels in the gate_4 are activated and the drain current is sampled by the DCDs. To remove the charge in the internal gate, a more positive voltage is applied to the clear implant. The direction of the rolling-shutter is shown in the figure starting from gate_4 1 to 192.



(b) An incoming electron hits the active gate_4 of the DEPFET matrix. The pixels in the gate_4 can be either in the signal readout stage or in the signal clearing stage.

Figure 7.16: A schematic drawing of the DEPFET module illustrating the rolling-shutter readout mode. The probability of electrons crossing the active gate_4 is 1/192.

2. Relevant hits requested by a trigger must receive the timestamp information. Therefore, as soon as a trigger is received by BDAQ-PXD, the current timestamp is retrieved. A 64-bit timestamp word is appended to the event, transmitted to the DAQ-PC and stored in the raw data.

3. The timestamp with the temporal information is converted into a gate_4 position according to the following estimate: $\text{timestamp} = 0 \quad \Leftrightarrow \quad \text{gate}_4 = 1$.
Therefore, each event contains the information about the activated gate_4 when the trigger was received.

4. Based on the event number, the active gate_4 is attached to each reconstructed track candidate found by the BTA framework. Tracks that have no associated hit on the DUT within a certain search radius are collected.

5. Finally, all tracks in the hit-detection efficiency calculation feature the active gate_4 information. With the extrapolation on the DUT, the information of the traversed gate_4 is provided.

In order to determine a correlation between the intersection point of inefficient particle tracks with the DUT ($\text{gate}_{\text{inefficient}}$) and the active gates_4 ($\text{gate}_{\text{active}}$), the distances between the two gates_4 on the DEPFET matrix is plotted, as can be seen in Fig. 7.17.
The distribution indicates that about 80 % of all inefficiencies occur when the distance between the active gate_4 and the traversed gate_4 is 10 or 11 gates_4 apart. A correlation would be revealed if the highest occurrence would be at a distance between 0 and 1 gate_4. However, an offset causes a shift between the timestamp start and the first activated gate_4 in the measurement procedure. In the presence of an offset, the following relation applies:

$$\text{gate}_4 = 1 \quad \Leftrightarrow \quad \text{timestamp} = 0 + \text{offset}.$$

Sec. 7.5.2 focuses on this emerging offset.
Further evidence can be obtained from the average charge generated by particles registered in the DEPFET module. Here, all reconstructed tracks are used resulting in Fig. 7.18. The mean charge deposited by traversing beam particles still supports the theory of charge loss due to the respective activation of DEPFET pixels and clearing of the internal gate.

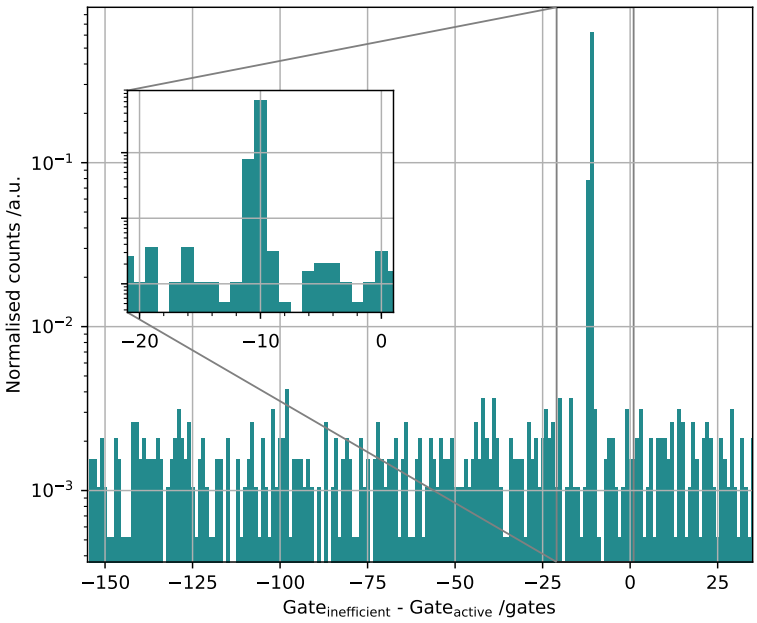


Figure 7.17: Histogram of the distance between the gate$_4$ of an inefficient track (gate$_{\text{inefficient}}$) and the active gate$_4$ (gate$_{\text{active}}$) (defined by the timestamp) in units of gates$_4$. The count is normalised to the sum of all inefficient tracks. A magnification of the region around the two peaks at gate$_4$={-10,-11} can be seen in the centre of the plot.

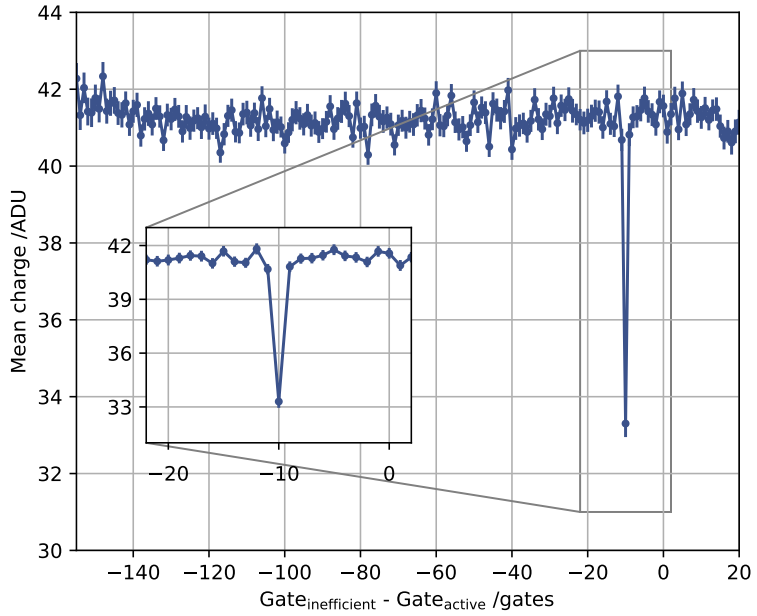


Figure 7.18: Histogram of the mean charge deposited by particles in a gate$_4$ depending on the distance to the active gate$_4$.

7.5.2 Offset determination

There are two possible sources of an offset and the observed shift between the active gate_4 and the traversed gate_4 of not detected tracks. In the following part, the two offsets are explained.

1. Reset of timestamp - frame synchronisation: To start the timestamp counter, a reset is transmitted to the DHPs at the beginning of the readout. By triggering the reset pulser module within the FPGA (explained in Sec. 6.2), the counter of the timestamp is directly set to 0. At the same time, the command to reset the DHPs is composed via the command encoder and shifted out every 8^{th} clock cycle of the 76.2 MHz command clock. Due to this process, the timestamp counter is started earlier than the reset is registered by the fourth DHP, initiating the restart of the SWITCHER sequence. Consequently, an offset between timestamp = 0 and $\text{gate}_4 = 1$ occurs.
An estimation of this delay can be made by simulating the signal processing in BDAQ-PXD and the DHP model. In the simulation, a reset is transmitted to the readout system and consequently to the DHP model containing the uploaded SWITCHER sequence. A section of the simulation can be seen in Fig. 7.19.

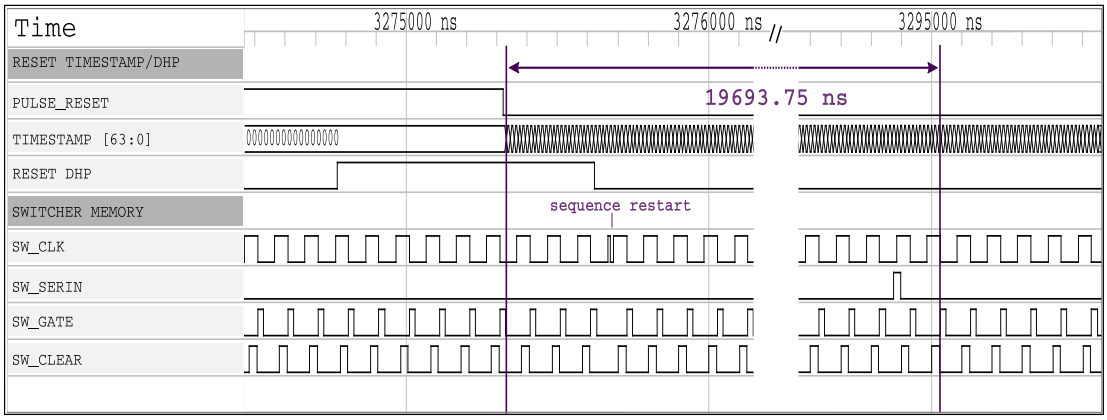


Figure 7.19: Section of the simulation of BDAQ-PXD and DHP model to reset the timestamp. The reset sets the `TIMESTAMP` to 0 and is received by the DHP model (`RESET DHP`) initiating the restart of the SWITCHER sequence. Originally, the timestamp is designed for 640 MHz, but due to incorrect links, only 10 MHz are reliable.

As already mentioned, the process starts with the reset transmitted to the BDAQ-PXD system. The reset pulse (`PULSE_RESET`) is distributed to the FPGA modules and starts the 64-bit counter of the timestamp module (`TIMESTAMP[63:0]`). The signal (`RESET DHP`) shown below is the reset recognised by the DHP model initiating a restart of the SWITCHER sequence. The four bottom signals are sent to the SWITCHER, namely, the SWITCHER clock (`SW_CLK`), the signal to activate the gate_4 (`SW_GATE`), the signal for clearing the gate_4 (`SW_CLEAR`) and the signal (`SW_SERIN`) clocked through the SWITCHER logic to activate the channels sequentially

(described in Sec. 5.2.1). As shown in Fig. 5.6 (Sec. 5.2.1), the activation starts after the second clock cycle (`SW_CLK`) with the prior arrival of the `SW_SERIN` signal. The following `SW_GATE` activates the first SWITCHER channel and `SW_CLEAR` initiates the clearing. Therefore, the generated offset results from the time difference between timestamp = 0 and the activation of the first gate after the reset resulting in:

$$\text{offset}_{\text{reset}} \approx 19\,694\,\text{ns}.$$

First, one readout cycle of the DEPFET matrix passes (19 200 ns), followed by additional 494 ns. However, two further effects need to be considered:

- In the simulation, the DHP model is supplied with a 80 MHz clock instead of the actual 76.2 MHz, decreasing the active time of the gate_4 from 105 ns (see measurement in Fig. 6.11) to 100 ns. Therefore, the result is multiplied by a factor of 1.05 resulting in 519 ns.
- An unconsidered aspect in the simulation is the delay due to the runtime of the reset signal between the readout board and the DHP. With a cable length of roughly 3 m (DP cable + patch panel + Kapton cable), the runtime is estimated to be 15 ns (5 ns/m).

In summary, an offset of 534 ns (5 gates_4) is assumed. This type of offset is caused at the start of each run.

2. Incoming particle - trigger registration: When a beam electron is detected by the two trigger planes (scintillator and FE-I4), both transmit a signal to the TLU. If the delay between both signal rise times at the TLU input is less than 31×1.5625 ns (coincidence window), a trigger is transmitted to all detector systems in the beam telescope (explained in Sec. 7.2.1). As soon as the trigger reaches BDAQ-PXD, the timestamp is retrieved and appended to the event. Consequently, an offset is created by the time difference between the electron traversing the telescope and the trigger arriving at BDAQ-PXD. To determine the offset, the propagation time of the signal from the scintillator (corresponds to incidence of the electron) to the arrival of the trigger in BDAQ-PXD is measured using an oscilloscope. The measurement is shown in Fig. 7.20. The scintillator is the first to detect the traversing electron shown in the centre plot. As the last detector plane, the FE-I4 sends the HitOr signal to the TLU. In the top plot, the histogram of the temporal occurrence of 100 000 recorded HitOr signals in relation to the scintillator can be observed. The width of the distribution results from the variation of the processing time depending on the charge deposited in the sensor (time walk). This effect arises from the discriminator response inside the FE-I4 which shifts depending on the collected charge. Nevertheless, the fluctuation is only small and not decisive for a delay in sending a trigger to the readout system.
The offset is defined by the time elapsed between scintillator signal and trigger arrival at the readout board. In the bottom plot, 100 000 waveforms are recorded to measure this time difference resulting in two peaks recognised in a time interval of 25 ns. Accordingly, a trigger

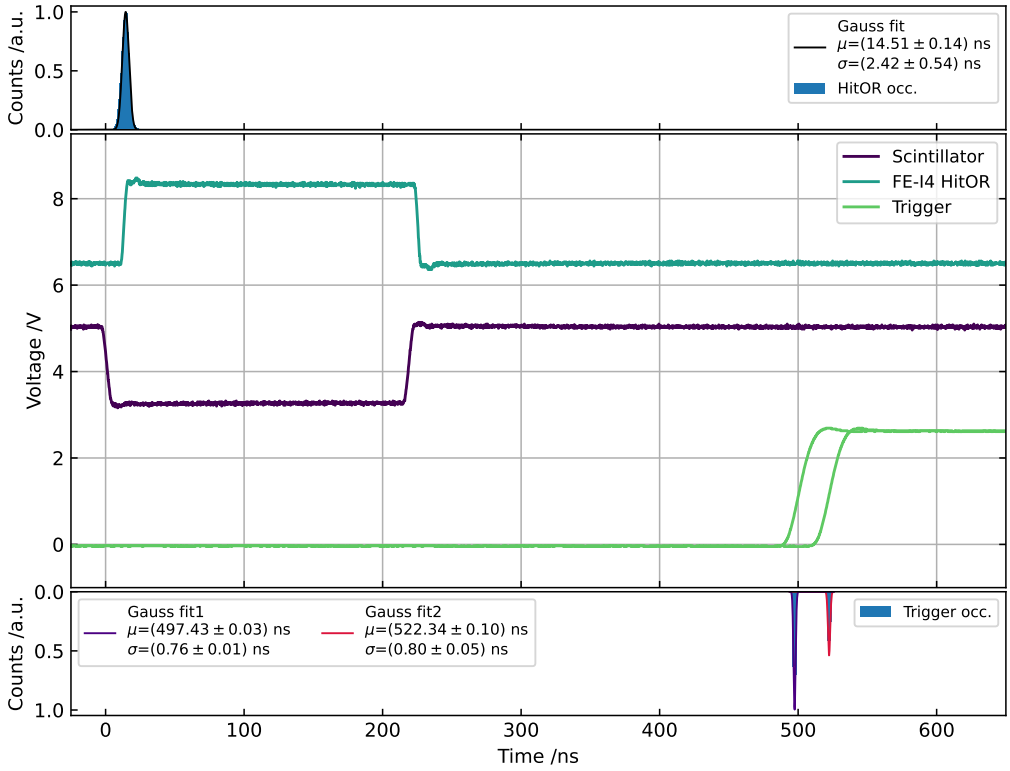


Figure 7.20: Oscilloscope measurement of the signal propagation times responsible for triggering BDAQ-PXD. The *centre plot* shows the different signals: Scintillator at the TLU (*blue*), HitOR from FE-I4 at the TLU (*dark green*), Trigger from TLU at the BDAQ board (*light green*). *Top plot*: Temporal occurrence of the HitOR in relation to the scintillator output. *Bottom plot*: Temporal occurrence of the trigger measured at BDAQ-PXD. Two occurrences are clearly visible.

signal is transmitted at two different times while the timing delay between scintillator and FE-I4 remains almost constant. In this regard, it is an unintentional feature of the TLU caused by the coincidence trigger. Moreover, the ratio of the occurrence of the two distributions depends on the delay between scintillator and FE-I4 signal. Despite this, the offset can be determined by including both time intervals between the scintillator and the trigger signal arriving at BDAQ-PXD. Since the scintillator signal is measured at the TLU, the propagation time on the 50 Ω-coaxial cable has to be taken into account: $3\,\mathrm{m} \times 5\,\mathrm{ns/m} = 15\,\mathrm{ns}$. Consequently, the two offsets yield:

$$\mathrm{offset}_{\mathrm{trigger}_1} \approx 512\,\mathrm{ns} \quad \wedge \quad \mathrm{offset}_{\mathrm{trigger}_2} \approx 537\,\mathrm{ns}.$$

This offset type occurs with every event recorded by the telescope.

Conclusion: Both determined offsets contribute to the shift between the active gate_4 and the inefficient gate_4. Taking both offsets into account, this delay results in:

$$\text{offset}_{\text{total}\,1,2} \approx \text{offset}_{\text{start}} + \text{offset}_{\text{trigger}\,1,2},$$

$$\boxed{\begin{aligned} \text{offset}_{\text{total}\,1} &\approx 1046\,\text{ns}, \\ \text{offset}_{\text{total}\,2} &\approx 1071\,\text{ns}. \end{aligned}}$$

Assuming that a gate_4 is active for 105 ns including clearing, the offset is approximately 10 gates_4. This is consistent with the histogram in Fig. 7.17 showing a peak at -10 gates_4. Furthermore, the two offset values obtained explain the occurrence of a second observed peak at -11 gates_4. In conclusion, the result provides evidence of a relationship between inefficiencies in particle detection and the activation of DEPFET pixels with subsequent signal clearing.

7.5.3 Adapted hit-detection efficiency

Based on the previous observation, it is evident that the clearing process creates a temporal inefficiency window. In the following, the effect of excluding this process is discussed. The target is to calculate the hit-detection efficiency without test beam electrons passing through an active gate_4. Therefore, reconstructed tracks located within the two peaks in Fig. 7.17 ($\text{gate}_{\text{inefficient}}$-$\text{gate}_{\text{active}}$={-10,-11}) are excluded from the calculation. Only the average value of the remaining inefficient tracks is retained. The histogram showing the hit-detection efficiency per pixel is presented in Fig. 7.21.

Applying the cut on tracks crossing the active gate_4, a reduction of the spread of pixels with an hit-detection efficiency below 99 % is noticeable. Consequently, more pixels become fully efficient. The empty range between 99 % and 100 % is due to the statistical effect that less than 100 reconstructed tracks are associated with each individual pixel. With exclusion, an average hit-detection efficiency of (99.93 ± 0.01) % can be achieved. For the module used, this represents an improvement of 0.16 %. Remaining inefficiencies could be caused by the detection threshold, track reconstruction and post-irradiation effects.

For the BDAQ-PXD system, it is a further proof of functionality as well as it demonstrates the suitability of the system for the investigation of single DEPFET modules.

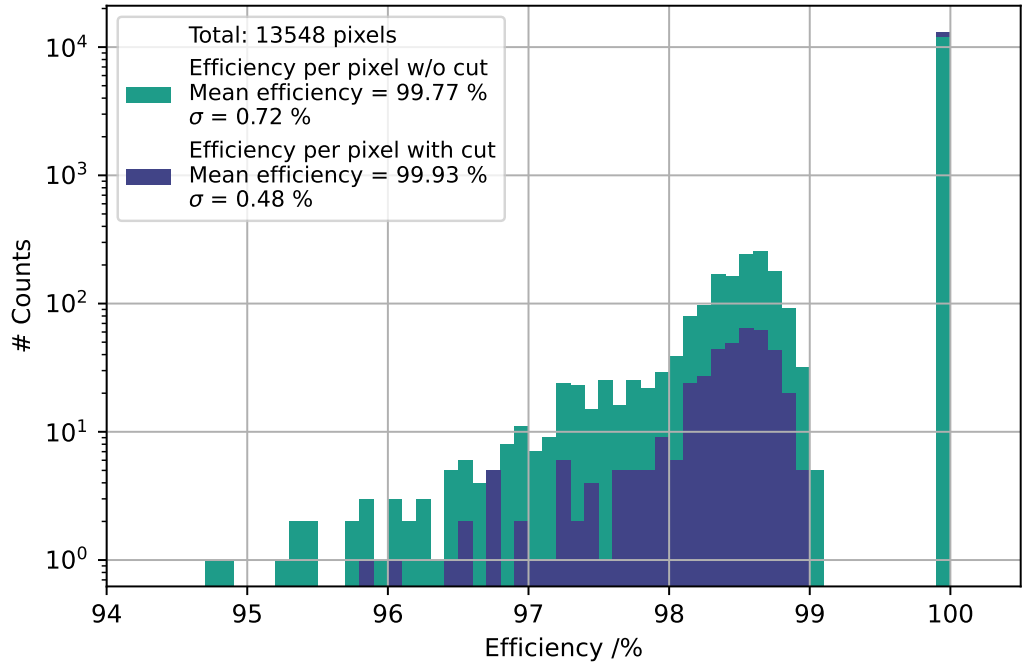


Figure 7.21: Efficiency distribution for the selected pixels with and without consideration of tracks traversing active gates$_4$ of the DUT. The mean efficiency value improves from 99.77 % to 99.93 %. Five pixels with an efficiency of less than 94 % lie outside the chosen plotting range.

8 Summary

The upgrade of the KEKB accelerator at the KEK research facility in Tsukuba, Japan, to SuperKEKB targets an instantaneous luminosity of $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, 40 times higher than for its predecessor. This goal poses new challenges for the detector systems of the Belle II detector. In particular, a new Pixel Detector (PXD) has been introduced using the Depleted P-channel Field-Effect Transistor (DEPFET) technology and positioned closest to the interaction point at radii of 14 and 22 mm.
This thesis addressed two detector systems, namely the FE-I4 ATLAS Near Gamma Sensors (FANGS) detector for the BEAST II experiment used in the commissioning of the SuperKEKB accelerator and the DEPFET pixel detector of Belle II.

The FANGS detector consists of three so-called staves, each equipped with five hybrid pixel detectors composed of the ATLAS FE-I4 readout chip and a planar silicon sensor. The components are suitable for high particle rate environments (up to $400\,\mathrm{MHz/cm}^2$) and harsh radiation conditions (up to 300 Mrad).
In this thesis, the FANGS system was integrated into the BEAST II experiment and a control and monitoring system for the FANGS detector using EPICS was developed. The measurements shown focused on the investigation of the background radiation in the operation of the accelerator. By measuring the hit rate during single-beam studies, a strong correlation between particle hits in the detector and the beam currents was observed. Furthermore, in the FANGS stave positioned at $\phi = 180°$ (-x-direction), a significant number of hits was detected in the central region of the detector. A more detailed analysis of the affected module on the stave showed a 61 % increase in single-pixel cluster hits. In addition, the internal FE-I4 charge measurement revealed a shift to smaller charges recorded in the central region module compared to the module at the outer edge.
After the commissioning, this observation in a single-beam study was also recorded in the PXD as beam parameters changed. The distribution of the recorded hits indicated a reflection of synchrotron photons at the inner beam pipe reaching the innermost detector layer. To obtain a more accurate energy resolution, a fast charge sampling capability was enabled by the Time-Digital-Converter (TDC) method using the 640 MHz clock provided by the FPGA-based readout board. According to prior calibration, a peak energy of (10.63 ± 0.08) keV was determined. This effect is still present in the operation of the Belle II detector and will be mitigated by a new beam pipe featuring additional gold coating scheduled for installation in 2023.

For investigations of DEPFET modules and their sensor properties used in the PXD, a new readout system called BDAQ-PXD was developed and tested within the scope of this thesis. The system uses the versatile BDAQ53 readout board incorporating an FPGA. As compared to the existing PXD readout system, BDAQ-PXD provides a simpler, more flexible and expandable readout in particular for measurements in laboratory, irradiation and test beam environments. The developed FPGA firmware and the software used for communication and data processing were presented. A BDAQ-PXD test containing all configuration steps necessary for operation as well as a measurement with a radioactive source demonstrated the functionality of the system. Besides the verification of the BDAQ-PXD readout system, the time-integrated and time-resolved hit-detection efficiency was studied for one DEPFET module using an electron beam at the DESY test beam facility. As a result, an efficiency of $(99.77 \pm 0.01)\,\%$ was obtained, comparable to published values for the same DEPFET module. Furthermore, the influence of different high-voltage biasing settings was shown in an in-pixel investigation. At an insufficient high voltage of -52 V, a degradation in charge collection and efficiency of up to 16 % was observed, occurring especially in the corners of the pixels below the drift implants.
As a final study, a timestamp provided by BDAQ-PXD was used to conduct a time-dependent investigation of inefficiencies occurring in the DEPFET module. The readout technique involving switching on the DEPFET pixels with subsequent clearing of the signal charges was identified as a source of undetected electrons. The hit-detection efficiency excluding pixels in this state exceeded 99.9 %.
In conclusion, BDAQ-PXD is very well suited for operating DEPFET modules in laboratory and test environments, and beyond that, it can provide further insights into the behaviour of the DEPFET technology. Further potential uses of BDAQ-PXD include future DEPFET applications which require an FPGA-based readout system.

Appendices

PulserDAC calibration using radioactive sources

Stave		slope **a** / PlsrDAC/keV	offset **b** / PlsrDAC
Stave I	Module1	(4.889 ± 0.004)	(-30.342 ± 0.198)
	Module2	(4.568 ± 0.005)	(-23.883 ± 0.237)
	Module3	(4.074 ± 0.007)	(-14.763 ± 0.289)
	Module4	(4.389 ± 0.017)	(-27.565 ± 1.012)
	Module5	(4.599 ± 0.001)	(-22.474 ± 0.044)
Stave II	Module1	(3.969 ± 0.003)	(-18.649 ± 0.090)
	Module2	(4.571 ± 0.011)	(-29.138 ± 0.482)
	Module3	(4.560 ± 0.010)	(-30.154 ± 0.346)
	Module4	(4.101 ± 0.013)	(-26.072 ± 0.568)
	Module5	(4.181 ± 0.006)	(-29.331 ± 0.335)
Stave III	Module1	(4.007 ± 0.011)	(-20.570 ± 0.412)
	Module2	(3.778 ± 0.008)	(-12.382 ± 0.290)
	Module3	(3.871 ± 0.003)	(-22.943 ± 0.113)
	Module4	(3.654 ± 0.004)	(-14.703 ± 0.135)
	Module5	(4.104 ± 0.006)	(-21.770 ± 0.227)

Table 8.1: Slope and offset of the transfer function for each module on the three FANGS stave. The function can be used to convert from PlsrDAC to keV.

SWITCHER sequence

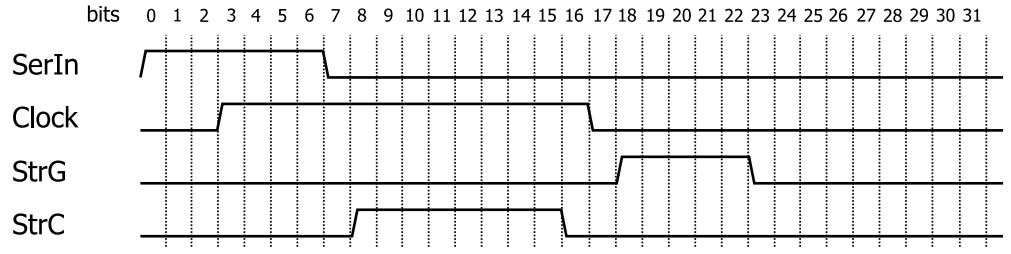


Figure 8.1: SWITCHER control signal loaded from the 128-bit word in the dedicated memory. Adapted from [Mül17, p. 101].

DHP mapping

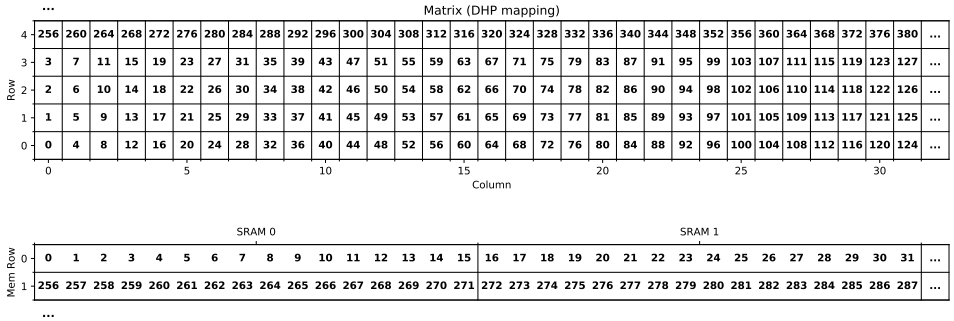


Figure 8.2: Representation of the relationship between the content of the SRAM memory (DHP main memory) and the pixel position assumed by the DHP.

DHP commands

Pulser state (10 MHz)	CMD (80 MHz)	Description
`5'b00000`	`8'b00011101`	Synchronisation word used for the alignment between transmitter and receiver.
`5'b00001`	`8'b11100001`	Memory dump word for request of data in the raw memory (w/o pedestal subtraction).
`5'b00010`	`8'b01010110`	Frame synchronisation causes the switcher sequence to restart.
`5'b00011`	`8'b11100010`	Memory dump + frame synchronisation.
`5'b00100`	`8'b01011001`	Trigger for reading out zero-suppressed data.
`5'b00110`	`8'b01011010`	Trigger + frame synchronisation.
`5'b10000`	`8'b10010101`	Reset signal to the DHP. The type of reset is determined by the length of the signal. E.g. reinitialises the high-speed link.
`5'b01000`	`8'b01100101`	Veto signal switches to *gated mode operation* [Mül17, pp. 213-248] of the SWITCHER.

Table 8.2: Selection of commands generated by the command encoder of BDAQ-PXD.

JTAG registers

ASIC	Register	Instruction	Length /bits
DHP	IDCODE_DHP	8'b00000001	32
	BYPASS	8'b11111111	1
	MEM_ADDRESS	8'b10100000	16
	MEM_DATA	8'b10100001	128
	JTAG_OFFSET_MEM_ADDRESS	8'b10100010	16
	JTAG_OFFSET_MEM_DATA	8'b10100011	128
	JTAG_SW_MEM_ADDRESS	8'b10100100	16
	JTAG_SW_MEM_DATA	8'b10100101	128
	JTAG_CORE_REG	8'b11100000	147
	JTAG_GLOBAL_REG	8'b11100001	600
	JTAG_CORE_READBACK_REG	8'b11100010	336
	JTAG_CORE_MASK_DCD_INPUTS	8'b11100011	128
	JTAG_ADC	8'b10000111	96
DCD	IDCODE_DCD	4'b0010	32
	BYPASS	4'b1111	1
	DCD_GLOBAL_REG	4'b0100	264
	DCD_PIXEL_REG	4'b1000	256
SWITCHER	IDCODE_SW	3'b010	32
	BYPASS	3'b111	1
	USERREG_SW	3'b011	48

Table 8.3: Main JTAG registers for the configuration of the ASICs [LGH16],[Per16],[FKP15]. The option of an identification number request (IDCODE) or bypassing the ASIC (BYPASS) is possible.

Abbreviations

ADC	Analogue-to-Digital Conversion	7
ADU	Arbitrary Digital Unit	57
ARICH	Aerogel Ring Cherenkov detector	9
ARU	Arbiter Unit	72
ASIC	Application Specific Integrated Circuit	50
BEAST	Beam Exorcism for A Stable Experiment	1
BTA	Beam Test Analysis	94
CDC	Central Drift Chamber	7
CLAWS	sCintillation Light And Waveform Sensors	31
CML	Common Mode Logic	57
CMOS	Complementary Metal-Oxide-Semiconductor	22
CSA	Charge-Sensitive Amplifier	22
CSS	Control System Studio	36
DAC	Digital-to-Analogue Converter	22
DAQ	Data Acquisition	65
DCD	Drain Current Digitiser	51
DEPFET	Depleted P-channel Field-Effect Transistor	2
DESY	Deutsches Elektronen-Synchrotron	2
DHH	Data Handling Hub	65
DHP	Data Handling Processor	51
DP	DisplayPort	66
DR	Data Register	62
DSSD	Double Sided Silicon Strip Detector	7
DUT	Device Under Test	87
ECC	Error Correction Code	58
ECL	Electromagnetic Calorimeter	9
EOS	End-Of-Stave	51
EPICS	Experimental Physics and Industrial Control System	36

FANGS	FE-I4 ATLAS Near Gamma Sensors	1
FIFO	First-In-First-Out	60
FPGA	Field-Programmable Gate Array	2
GUI	Graphical User Interface	36
HAPD	Hybrid Avalanche Photo-Detector	9
HER	High Energy Ring	3
HV	High Voltage	99
IB	Inner-Backward	51
IBL	Insertable B-Layer	21
IF	Inner-Forward	51
IOC	Input Output Controller	36
IP	Interaction Point	4
IR	Instruction Register	62
JTAG	Joint Test Action Group	57
KLM	K_L and muon detector	9
LER	Low Energy Ring	3
LHC	Large Hadron Collider	1
Linac	Linear accelerator	3
LVDS	Low-Voltage Differential Signalling	33
MCP-PMT	Micro-Channel-Plate Photomultiplier Tube	8
MIP	Minimum Ionising Particle	14
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor	23
OB	Outer-Backward	51
OF	Outer-Forward	51
PCB	Printed Circuit Board	67
PLUME	Pixelated Ladder using Ultra-light Material Embedding	31
PP	Patch Panel	66
PV	Process Variable	36
PXD	Pixel Detector	1

ROI	Region Of Interest	91
RPC	Resistive Plate Counter	9
SCB	Support and Cooling Block	33
sCVD	single-crystal Chemical Vapour Deposition	32
SEU	Single Event Upset	58
SiPM	Silicon Photomultiplier	32
SM	Standard Model	1
SRAM	Static Random-Access Memories	58
SVD	Silicon Vertex Detector	6
TAP	Test Access Port	62
TCK	Test Clock	62
TCP	Transmission Control Protocol	71
TDC	Time-Digital-Converter	23
TDI	Test Data In	62
TDO	Test Data Out	62
TIA	Trans-Impedance Amplifier	56
TID	Total Ionising Dose	22
TLU	Trigger Logic Unit	72
TMS	Test Mode Select	62
TOP	Time-Of-Propagation	8
ToT	Time-over-Threshold	23
TPA	Two Parse Average	60
TPC	Time Projection Chamber	32
TRST	Test Reset	62
VXD	Vertex Detector	6

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> "I knew exactly what to do. But in a much more real sense, I had no idea what to do."
>
> Michael G. Scott (*The Office*)

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