Universität Bonn

Physikalisches Institut

High bandwidth pixel detector modules for the ATLAS Insertable B-Layer

Malte Backhaus

The investigation of the nature of the recently discovered electro-weak symmetry breaking mechanism of the standard model of particle physics as well as the search for physics beyond the standard model with the LHC require to collect even more data. To achieve this goal, the luminosity of the LHC will be increased in two steps. The increased luminosity results in serious challenges for the inner tracking systems of the experiments at the LHC. The ATLAS pixel detector will also be upgraded in a two stage program. During the shutdown in 2013 and 2014 a fourth hybrid pixel detector layer, the so-called Insertable B-Layer (IBL) is inserted inside the existing pixel detector. This thesis focuses on the characterization, performance measurement, and production quality assurance of the central sensitive elements of the IBL, the modules. This includes a full characterization of the readout chip (FE-I4) and of the assembled modules. A completely new inner tracking system is mandatory in ATLAS after the second luminosity increase in the shutdown of 2022 and 2023. The final chapter of this thesis introduces a new module concept that uses an industrial high voltage CMOS technology as sensor layer, which is capacitively coupled to the FE-I4 readout chip.

Physikalisches Institut der
Universität Bonn
Nussallee 12
D-53115 Bonn

BONN-IR-2014-02
January 2014
ISSN-0172-8741

Universität Bonn

Physikalisches Institut

High bandwidth pixel detector modules for the ATLAS Insertable B-Layer

Malte Backhaus
aus
Hagen

Dieser Forschungsbericht wurde als Dissertation von der Mathematisch-Naturwissenschaftlichen Fakultät der Universität Bonn angenommen und ist 2014 auf dem Hochschulschriftenserver der ULB Bonn http://hss.ulb.uni-bonn.de/diss_online elektronisch publiziert.

1. Gutachter:	Prof. Dr. Norbert Wermes
2. Gutachter:	Prof. Dr. Klaus Desch
Angenommen am:	21.10.2013
Tag der Promotion:	30.01.2014

Contents

Chapter 1

Introduction

Since the beginning of modern physics in the 16th and 17th century, the discoveries of physics have changed the perception of the world we live in. The interplay of theoretical models and experimental methods allowed to reveal the fundamental mechanisms of nature. The increase of knowledge of these within the last three centuries is astonishing. Starting from the examination of macroscopic objects in classical mechanics, the revelation of the nature of the atom in the early 20th century paved the way for the development of a fundamental model describing the building blocks of the world we live in and the forces between them, the Standard Model of particle physics. The Standard Model is confirmed in great details over the past decades. The investigation of its electro-weak symmetry breaking mechanism is currently one of the major goals of particle physics. Albeit the Standard Model is very successful, different deficiencies (many parameters, so called hierarchy problem, no explanation for dark matter) indicate that the story of particle physics is not yet at its end and physics beyond the Standard Model is likely to exist.
The impact of physics discoveries and experimental technologies goes well beyond the scope of fundamental research. They have direct impact on the human society. For instance, the understanding of classical mechanics and thermodynamics enabled the industrial revolution. The discovery of Roentgen radiation revolutionized the medical diagnostic. The world wide web, now accessible to a large scale, was initially motivated by the need to share experimental data between world wide collaborations. The progress in physics was driven by outstanding scientists in the past centuries. But the complexity of the present particle physics experiments requires a huge number of collaborating physicists, with specialization on different aspects of physics, for their development, operation, and maintenance, as well as to link their results to fundamental theories. The organizational structure of these collaborations is currently investigated by scientists from other areas of research. The outcomes can have an impact on unexpected domains of the society.
The collaboration of the ATLAS[1] experiment is such an example and consists of more than 3000 scientists from 174 institutes in 38 countries. ATLAS is an experiment at the proton-proton collider LHC[2] at CERN[3] and investigates a large variety of particle physics at the TeV energy scale. The main focus of ATLAS is on the electro-weak symmetry breaking mechanism, but also physics beyond the Standard Model is investigated. The physics program and the planned upgrade programs to increase the luminosity of the LHC and the foreseen ATLAS detector upgrades are introduced in chapter 2.
The ATLAS detector consists of several sub-detector systems with dedicated tasks. One of the key requirements to reach the goals of the physics program is the detection of primary and secondary vertices. The primary vertex is at the collision point, but long-lived particles generated at the primary vertex can travel a significant distance at almost the speed of light before they decay. This way secondary vertices are generated that are displaced from the primary vertex. A prominent example are hadrons containing

[1] A Toroidal LHC ApparatuS
[2] Large Hadron Collider
[3] Conseil Européen pour la Recherche Nucléaire

b-quarks. The detection of those is very important. ATLAS has a dedicated vertex detector that consists of three layers of segmented silicon detectors, the pixel detector. The pixel detector has the most stringent requirements of all sub-detector systems. It is the innermost detector layer, located near the proton-proton collision point. The huge number of particles generated in the collisions travel through the pixel detector, so the particle occupancy per area and the required radiation tolerance is challenging. Last but not least, the pixel detector is the innermost sub-detector and the interaction of particles with the pixel detector material influence the performance of the subsequent layers. Thus the pixel detector is required to have a low material budget. The basic principles of vertex reconstruction with pixel detectors and the constituents of state of the art pixel detectors for high radiation environments are explained in chapter 3.
The innermost layer of the pixel detector is of special importance for the detection of the secondary vertices and is also called B-Layer. To improve the existing vertex resolution of ATLAS and to ensure the performance at even increased collision rates and in a scenario with accidental loss of the present B-Layer, a new insertable B-Layer (IBL) is developed. The IBL and its components as well as the expected performance improvement in two scenarios, with and without a loss of the existing B-Layer, are described in detail in chapter 4.
The development and characterization of the central sensitive elements of the IBL, the detector modules, are the main scope of this thesis. The IBL modules consist of different sensor types that are connected to a custom developed Front-End chip with a sophisticated readout architecture. The results of the study of this readout chip are presented in chapter 5 and the achieved performance of the IBL modules is shown in chapter 6. Both chapters contain detailed summary results of the quality assurance tests performed during the IBL production.
Chapter 7 focuses on the development of a completely new pixel detector for the LHC run phase after 2024. The planned increase of the LHC luminosity requires a new inner detector with a significantly increased pixel surface. The development of new module concepts has started, one of which using an industrial high voltage CMOS process for the sensor layer. This approach potentially provides a number of benefits: fast signal detection, radiation hardness and not least a reduction of the costs. These benefits make the concept a promising candidate for the foreseen outer pixel layers of the new pixel detector.

Chapter 2

The Large Hadron Collider and the ATLAS experiment

The Large Hadron Collider (LHC) is the world's most powerful particle accelerator and is constructed at CERN[1], close to Geneva, to exploit a rich physics program. A brief introduction to this program, the resulting requirements for the accelerator and its experiments, and their design properties is provided in this chapter.

2.1 Physics at the Large Hadron Collider

The Standard Model (SM) of particle physics is a quantum field theory describing the building blocks of matter and the interactions between them in a wide energy range. The SM makes use of a limited amount of particles with no internal structure to describe all observable matter and forces. The matter building and the force mediating particles can be separated using a quantum number called spin. The building blocks of matter consist of fundamental fermions, which are spin $1/2$ particles. The SM describes the interactions between the fermions using three fundamental forces. These forces are mediated between the fermions by the exchange of fundamental bosons with integer spin, i.e. spin 1.
The SM groups the fermions symmetrically. They are sorted into quarks and leptons by the interactions they take part in. Each group is subdivided in three flavors of increasing mass. The leptons carry integer electrical charge of $-e$ or neutral charge, while the quarks carry either $2/3\,e$ or $-1/3\,e$ of electrical charge.
The leptons take part in the weak force and in the electromagnetic force. The weak force is mediated by charged $W^{\pm}$ bosons and the neutral Z boson. The bosons carrying the weak force are massive and as a consequence the range of the weak interaction is short. The mass of the $W^{\pm}$ bosons has been measured to $(80.403 \pm 0.029)\,\mathrm{GeV}$ and the Z boson mass to $(91.1876 \pm 0.0021)\,\mathrm{GeV}$. In contrary the electromagnetic force, which acts between all charged particles, is described by the exchange of a massless and neutral photon (γ). Therefore the range of the electromagnetic force is infinite. The strong force has by far the largest coupling strength and acts between quarks only. It is mediated by massless gluons (g) of spin 1. The shape of the strong interaction potential is responsible for the confinement of quarks in hadrons, which explains why quarks in contrary to leptons can not be observed as free particles, but only in compound states of two or more quarks. Table 2.1 summarizes the fundamental ingredients of the SM and their properties listing the fermion families by increasing mass and the bosons by the coupling strength of the force they carry.
Due to the mass difference between the three fermion families, the members of family 2 and family 3 decay into lighter fermions. Therefore all standard matter in the current universe is constructed of fermions of family 1. The members of family 2 and family 3 are generated in high energy interactions, either

[1] Conseil Européen pour la Recherche Nucléaire

fermions	family 1		family 2		family 3		charge	coupling to
leptons	e	0.511 eV	μ	105.7 eV	τ	1777 MeV	$-1\,e$	γ, $W^{\pm}$, Z
	ν_e	< 2 eV	ν_μ	< 2 eV	ν_τ	< 2 eV	neutral	$W^{\pm}$, Z
quarks	u	~ 1.5 MeV	c	1.25 GeV	t	171 GeV	$2/3\,e$	γ, $W^{\pm}$, Z, g
	d	~ 3 MeV	s	95 MeV	b	4.2 GeV	$-1/3\,e$	γ, $W^{\pm}$, Z, g
bosons	weak force		em force		strong force		gravitation	
	$W^{\pm}$	~ 80 GeV	γ	massless	g	massless	G	massless
	Z	~ 91 GeV						
strength [α_s]	10^{-6}		1/137		1		10^{-39}	
	H	~ 126 GeV						

Table 2.1: Fundamental ingredients of the Standard Model of particle physics. The fermions are the building blocks of matter and the bosons mediate the fundamental forces. Even though the gravitation is not described in the current Standard Model, it is listed here to illustrate the huge difference in its coupling strength. Therefore the gravitation can be neglected in the LHC experiments.

naturally generated such as in cosmic radiation, or human generated such as in collider experiments. When decaying to lighter fermions the conservation laws of the SM must be respected. These decays to lower families are mediated by the weak force, resulting in lifetimes long enough for the particles to travel a significant distance at the speed of light before decaying. The detection of the decay vertex of such particles is crucial for the success of high energy physics collider experiments.The improvement of the detectors for this task called vertex measurement is a field of permanent research. Further details can be found in chapter 3.

The SM unifies the electromagnetic and the weak force into the electro-weak force, which builds a $SU(2) \times U(1)$ symmetry group (electro-weak symmetry). The mass of all particles is generated in the SM by interaction with a scalar background field. This mechanism was proposed by Robert Brout, Francois Englert, Peter Higgs, Gerald Guralnik, C. R. Hagen and Tom Kibble in 1964 and is called Higgs-mechanism. As the $W^{\pm}$ and the Z bosons are massive and the photon is massless, the Higgs-mechanism must break the electro-weak symmetry. This requires the existence of an additional massive boson with spin 0. This boson is called Higgs boson (H). Although the Higgs particle has been eagerly searched for by the HEP community, the proof for its existence could not be made for close to 50 years. The SM does not predict the mass of the Higgs boson. In fact the mass of the Higgs boson is the only open parameter of the theory. It determines all couplings of the Higgs boson and thus all production cross sections and branching ratios of its decay modes can be predicted. Precision measurements of other SM parameters favored a mass of the Higgs smaller than 144 GeV and direct searches at former accelerators exclude a Higgs mass below 114.4 GeV. As will be explained later, the Higgs boson has finally been discovered by the LHC experiments exactly in the favored mass range. The probing of the Higgs-mechanism is one of the main goals in the LHC physics program in 2012 and thus drives the requirements of experiments searching for the Higgs boson. These requirements are explained in detail in chapter 2.2 and further information about the first observation of the Higgs boson at the LHC will be provided in chapter 2.3.

The SM has been tested in great details in the past decades and no discrepancy is found so far. Furthermore the SM predicted the existence of a number of particles long before their first experimental observation such as the top quark (t) and the H. But despite these huge successes the SM fails to describe all observations and leaves several questions unanswered. For example gravitational observations in the dynamics of galaxies show that there is unaccounted mass present (so called dark matter), which

is not included in the SM framework. The SM also provides no explanation why the mass of the SM particles ($\lesssim 100\,\text{GeV}$) differ in many orders of magnitude from the Planck-mass ($\sim 10^{19}\,\text{GeV}$. This deficiency is called the hierarchy problem. Several theoretical extensions of the SM exist which provide mechanisms answering open questions. All such theories predict new phenomena to be observed in the TeV-range and thus can be tested with the help of the LHC.

2.2 The Large Hadron Collider

The cross sections of the Higgs production as well as of new physics are about three orders of magnitude smaller than the cross sections of well measured SM processes, such as of Z and $W^{\pm}$ production. This requires the experiments to collect very large data samples to be able to measure unexplored physics processes. The event rate $\dot{N}_{event}$ is derived from the luminosity L and the cross section σ_{event} of the examined event by

$$\dot{N}_{event} = L \cdot \sigma_{event} \tag{2.1}$$

with the luminosity given by

$$L = \frac{n \cdot N_1 \cdot N_2 \cdot f}{A} \tag{2.2}$$

for a ring collider. Here n denotes the number of bunches in the accelerator, N_i the number of particles in the bunches of the two beams, f the collision frequency of the bunches and A the cross sectional area. The LHC is designed for a very high luminosity of $10^{34}\,\text{cm}^{-2}\text{s}^{-1}$ in order to provide enough statistics for its rich physics program, covering both high precision measurements of established SM processes and the search for so far unexplored phenomena.
Due to the internal structure of hadrons, hadron collisions provide the possibility to probe a wide energy range simultaneously. This makes hadron collisions a well suited tool for searches for particles with unpredicted mass, such as the former introduced Higgs boson. Additionally, in comparison to electrons the reduced energy loss due to Bremsstrahlung when using hadrons in ring accelerators enables higher collision energies. Thus the LHC is designed as a proton-proton collider with a center of mass energy of 14 TeV, which promises to be suitable to observe new phenomena. It is placed in the former LEP[2] tunnel about 100 m underground and provides four interaction points where the experiments are located. At the design luminosity, 2808 bunches consisting of 1.15×10^{11} protons each collide with 25 ns bunch spacing. The two multi-purpose experiments, ATLAS[3] and CMS[4], are designed to explore new physics and to examine the Higgs-mechanism, and are therefore operated at the maximum LHC luminosity. LHCb[5] and ALICE[6] are specialized respectively in b-physics and heavy ion physics and collect data at reduced luminosity. The immense luminosity provided by the LHC results in challenges for the design of the detectors, especially for ATLAS and CMS. Details are provided in chapter 2.3 and solutions are given with focus on the ATLAS vertex detector.
LHC operation started in 2009. In a first run period, the LHC delivered $\sim 5\,\text{fb}^{-1}$ of data at a center of mass energy of 7 TeV. Starting in 2012 the center of mass energy was increased to 8 TeV and $> 20\,\text{fb}^{-1}$ have been delivered since then until the LHC was shut down in early 2013 to undergo its first upgrade program. Several upgrades for the LHC and the detectors are foreseen and chapter 2.4 introduces the upgrade plans of LHC and ATLAS.

[2] Large Electron-Positron Collider
[3] A Toroidal LHC ApparatuS
[4] Compact Muon Solenoid
[5] Large Hadron Collider beauty
[6] A Large Ion Collider Experiment

2.3 The ATLAS experiment

Requirements

In order to utilize the full physics capability of the LHC, the two multi purpose detectors ATLAS and CMS must fulfill a number of requirements. These requirements are explained here and the derived detector layout is shown for the example of ATLAS.

- Good lepton and neutrino reconstruction including the detection of τ-leptons. This is needed for the detection of the Higgs boson decays $H \rightarrow \tau\,\tau$ and $H \rightarrow W^{\pm}\,W^{\pm}$.
- High reconstruction capability of multi-jets and simultaneous tagging of jets originating from b-quarks. This is needed for precision measurements of the t-quark properties using the decay of the produced $t\bar{t}$ pairs and their decay in the channel $t \rightarrow b\,W^{\pm}$ and with the $W^{\pm}$ decaying either into leptons or quarks, and also for Higgs studies in the channel $H \rightarrow b\bar{b}$.
- Excellent reconstruction of the transverse momentum of charged leptons and neutrinos to measure the electroweak parameters with very high precision. The neutrino itself can not be detected and thus the transverse momentum can only be reconstructed from the discrepancy in the total transverse momentum balance.
- Unobserved phenomena as predicted by theories beyond the SM are expected to be identified by a large number of jets due to the expected long decay chains. Additionally, a large deficiency in the reconstructed energy (E_T^{miss}) originating from escaping particles is expected.
- High momentum electron and muon reconstruction for the detection of potentially new resonances decaying into leptons.

Layout

These requirements are addressed in the ATLAS detector layout shown in figure 2.1. The detector's overall layout is a shell structure with several specialized sub-detectors. All subsystems are cylinder shaped with additional end-caps and allow a large acceptance in pseudorapidity $\eta := -\tan(\frac{\Theta}{2})$, with Θ being the angle to the beam direction. ATLAS contains an inner tracking system which allows high transverse momentum lepton measurement at high luminosity, electron and photon identification as well as tagging of long lived heavy hadron and τ-lepton decay. At lower luminosity the tracking system is capable of full event reconstruction. The inner detector is placed in a solenoid magnetic field of 2 T and contains three subsystems. The vertex measurement is performed by a silicon pixel detector which is the main focus of this work and thus is covered separately in the following chapters. Moving radially outwards, the vertex detector is followed by a silicon strip detector (SCT) with four barrel layers and nine disks on each side. Outside of the SCT volume a continuous straw tube tracking detector is installed. Additionally, this sub-tracker uses transition radiation (TRT, Transition Radiation Tracker) for the electron identification.
The very high LHC luminosity presents serious experimental difficulties. Following equation (2.1), LHC produces at its design luminosity - assuming a total cross section for inelastic events of about 80 mb - 10^9 inelastic events per second. That results in an average of 23 inelastic interactions per bunch crossing (pile-up) and around 1000 charged particles traversing the detector every bunch crossing. Those events must be distinguished and the decay products must be assigned to the particular interactions. This task is called primary vertex detection and is covered by the ATLAS tracking system, which reconstructs the

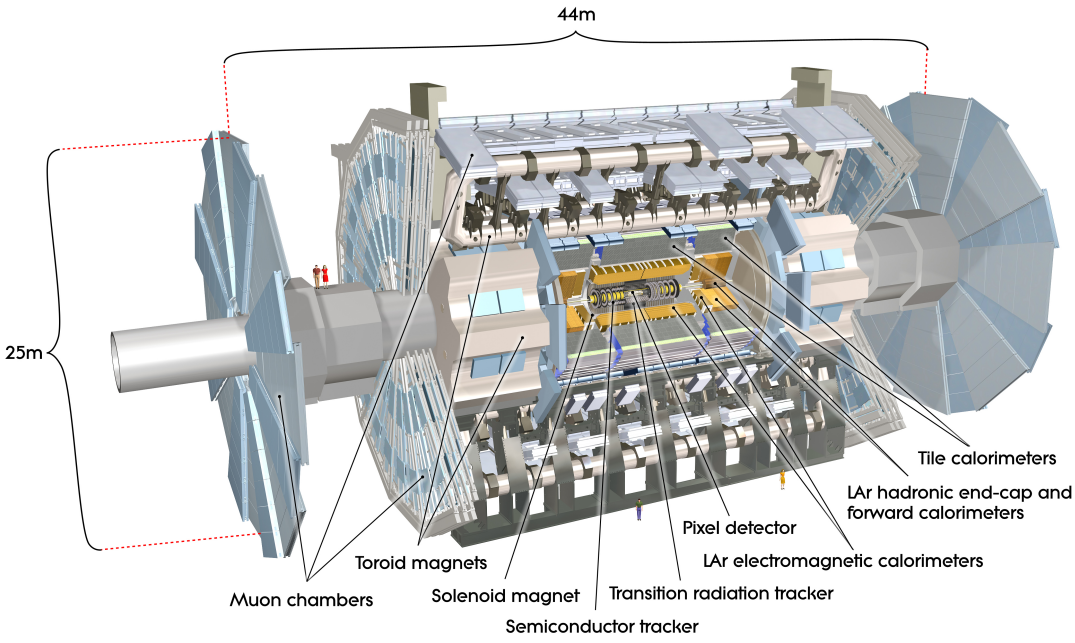


Figure 2.1: Overall layout of the ATLAS detector [1].

tracks of the particles traveling through the detector. Additionally, the ATLAS vertex detector identifies secondary vertices of long lived hadrons containing b-quarks or c-quarks, and of τ-leptons.
The multi-jet reconstruction requires a highly granular calorimeter system. The electromagnetic calorimeter is constructed as a liquid-argon sampling calorimeter and shows excellent performance in position and energy resolution. Liquid-argon is also chosen for the end-caps of the hadronic calorimeter, whereas the barrel volume of the hadronic calorimeter is provided by a scintillator-tile calorimeter. Both systems together allow ATLAS to benefit from their very good jet and E_T^{miss} measurement.
The measurement of high momentum leptons is crucial for the success of several physics goals. High momentum muons escape the calorimeter system and therefore a large muon tracking system is installed in the outermost volume. This system consists mainly of monitored drift tubes for track measurement and air-core toroid magnet coils providing strong bending power for momentum measurement while consisting of a light and open structure.
A Cartesian ATLAS coordinate system is defined by the LHC ring. x points towards the center of the ring, z along the beam axis and y perpendicular to both. Commonly, also cylindrical coordinates are used in ATLAS. Again z denominates the beam direction, ϕ the angle to the x-axis in the xy-plane, and r the distance from the z-axis.

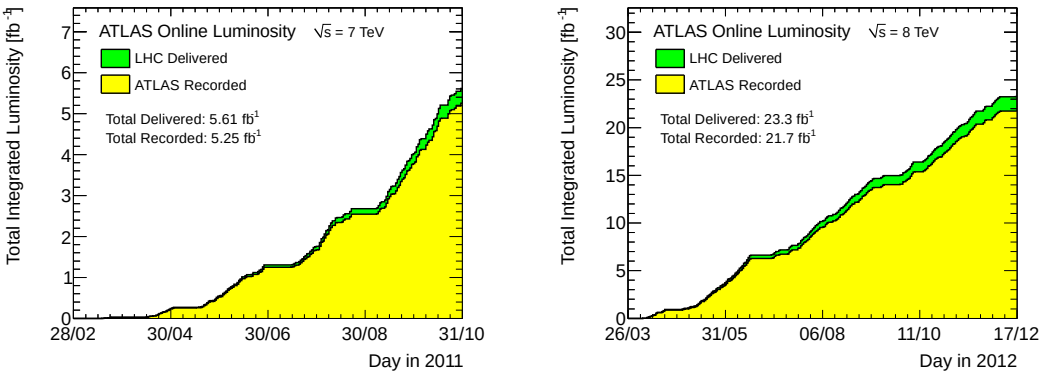
Trigger system

The on-tape recording of all events exceeds by far the present technical data storage possibilities. A multi-level Trigger and Data Acquisition system (TDAQ) to preselect and store the data of main interest for the physics program is used in ATLAS [2]. The data rate is reduced by a factor of 10^5 at nominal LHC luminosity. The first selection stage is the Level-1 trigger that reduces the rate of selected events to $\sim 75\,\text{kHz}$ in standard operation. An increased Level-1 trigger rate of $\sim 100\,\text{kHz}$ is possible in the ATLAS readout electronics with slightly increased dead time. A high level trigger (HLT) must provide

an event rate reduction of 10^3 to not exceed the storage capability of a few hundred Mbyte per second of the mass storage devices.
The Level-1 trigger is a hardware based trigger system that mainly uses the calorimeter and the muon system to select events of potential interest. It uses an algorithm to identify e, γ, τ and hadron events in the calorimeter. The transverse momentum p_T is discriminated against programmable thresholds. Keeping the threshold as low as possible for isolated leptons (~ 25 GeV), at a compatible event rate, is crucial for a highly efficient data selection, especially for events with $W^{\pm}$ and Z contribution such as H decays. Additionally, E_T^{miss} is discriminated to improve the sensitivity to new physics events. The muon system uses an algorithm estimating the muons p_T by hit coincidences within a geometrical region-of-interest. Similar to the calorimeter system, the muon p_T can also be discriminated against an adjustable threshold. The ATLAS readout electronics stores the events during the full Level-1 trigger latency of up to 3 µs and discards un-triggered events afterwards.
The events selected by the Level-1 trigger are stored on readout buffers (ROBs) for further processing by the HLT. The HLT itself is a two stage system running on a commercial PC farm. It consists of the Level-2 trigger and the Event Filter (EF) algorithm. First the Level-2 trigger requests the data from the ROBs in the region-of-interest and reduces the event rate by a factor of 20 to 30 within its latency of 10 ms. Finally, after being selected by the Level-2 trigger, the full event is transferred and built. The EF uses fast and simplified reconstruction algorithms, that are close to the reconstruction performed during the off-line analysis, to perform the last selection based on the full event shape. After the HLT the event rate is reduced to about 200 Hz.

LHC and ATLAS performance in 2011 and 2012

The ATLAS and the CMS experiments have shown great performance in the first run period of LHC. Figure 2.2 illustrates the great efficiency of the ATLAS detector and its operators. ATLAS has collected more than 93% of the luminosity delivered by LHC in the first run periods with proton-proton collisions.



(a) (b)

Figure 2.2: Cumulative luminosity versus day delivered to (green), and recorded by ATLAS (yellow) during stable beams and for pp collisions at 7 TeV centre-of-mass energy in 2011 (a) and at 8 TeV center-of-mass energy in 2012 (b) [3]. The collected luminosity in the previous years of operation is by three orders of magnitude below the 28 fb^{-1} collected in 2011 and 2012 and thus not displayed.

Well known SM processes provide an excellent reference for the calibration of the ATLAS detector.

Detailed measurements have been performed and used to calibrate the ATLAS detector. Figure 2.3 compares the measured production cross section for several SM processes with the theoretical predictions. Very good agreement over five orders of magnitude in the cross section is reached.

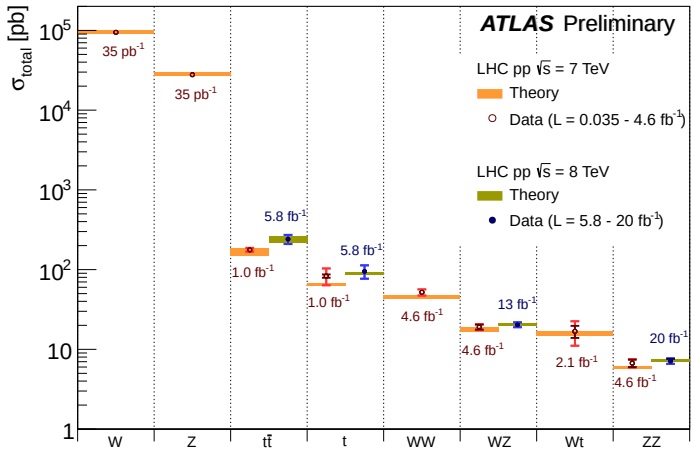


Figure 2.3: Summary of several Standard Model total production cross section measurements, corrected for leptonic branching fractions, compared to the corresponding theoretical expectations. The dark-color error bar represents the statistical uncertainly. The lighter-color error bar represents the full uncertainty, including systematics and luminosity uncertainties. All theoretical expectations are calculated at next to leading order or higher [3].

This great performance of LHC and its experiments lead to the first confirmation of the long expected Higgs boson in 2012 by ATLAS and CMS. ATLAS as well as CMS have consistently found a significant excess of events at an energy of about 126 GeV. It can be computed that this excess has a chance to come from a statistical background fluctuation of less than 10^{-9} (less than one chance in one billion!). This excess is compatible with the discovery of a Higgs boson mass of approximately 126 GeV as shown in figure 2.4. Both ATLAS and CMS have published the observation of a Higgs boson [4, 5].

2.4 The LHC upgrade program

These exciting achievements of the LHC experiments motivate further efforts to measure the characteristics of the recently discovered boson in great details. This requires to collect even more data and therefore to increase the LHC luminosity, run at the final center-of-mass energy, and improve the detector performance. Also the discovery potential for unexplored physics will greatly benefit from higher collision rates and energies, which increases the probed mass range. To reach this goal, a three stage upgrade of the machine is planned, with a parallel upgrade of the detectors to handle the rougher working conditions and enhance the detector's reconstruction capabilities. Figure 2.5 summarizes the upgrade steps with focus on the ATLAS Inner Detector, which are explained in detail in the following sections.

2.4.1 Upgrades of the accelerator

Phase-0

A first long shutdown (LS1) is ongoing at the time of writing (from February 2013 to July 2014) to consolidate the magnet inter-connects of the LHC machine. This is needed to run LHC at the design

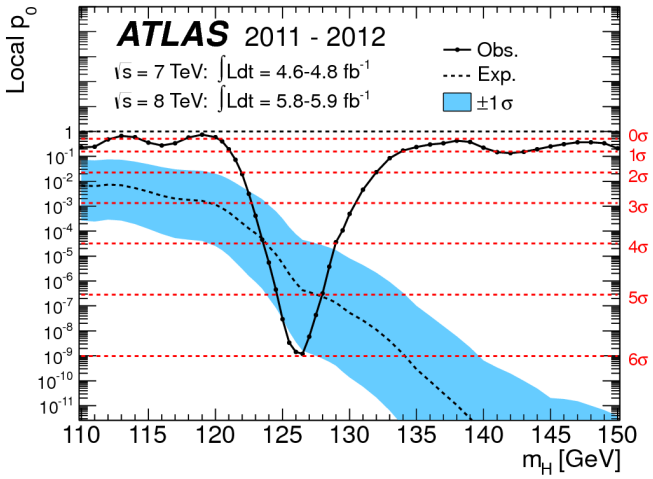


Figure 2.4: The observed probability that the experimental observations are consistent with a "background only" hypothesis (local p_0) as a function of the Higgs mass in the low mass range. The dashed curve shows the expected local p_0 under the hypothesis of a SM Higgs boson signal at that mass with its ± one sigma band. The horizontal dashed lines indicate the p-values corresponding to a significance of 1 to 6 sigma [4].

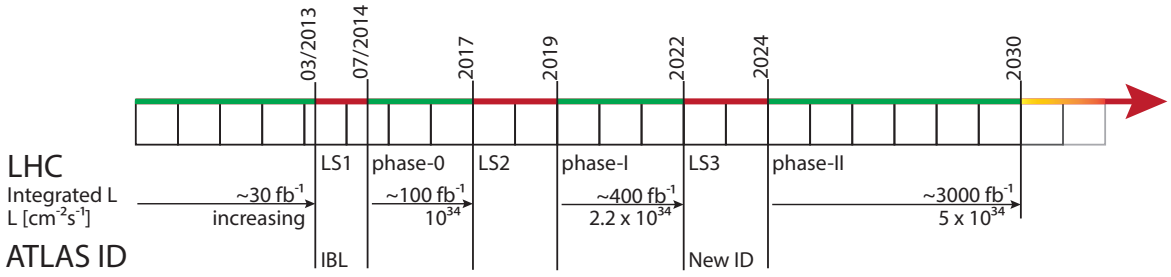


Figure 2.5: Time schedule for the long LHC shutdowns, the run phases, and the ATLAS Inner Detector upgrades.

energy of 7 TeV per beam and at the design luminosity of $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. This shutdown will be followed by the run period Phase-0, which will last from 2015 to 2017 and should collect up to $100\,\mathrm{fb}^{-1}$ of data.

Phase-I

After Phase-0, the LHC will undergo a major upgrade to increase its luminosity to $2.2 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ during another long shutdown from 2017 to 2019. To achieve this goal, two upgrades are foreseen during this second long shutdown (LS2). The Linac4[7] will be inserted as injector system to the Proton Synchrotron Booster (PSB) and will replace the existing Linac2. An increase in the beam brightness of the PSB by a factor of two is expected, which will allow to increase the LHC luminosity. Additionally, an upgrade of the LHC collimation system will increase the luminosity further by reducing the cross sectional area. During the following Phase-I run, the LHC should deliver up to $400\,\mathrm{fb}^{-1}$.

Phase-II

A second major machine upgrade is foreseen in a shutdown after 2022 (LS3). In order to deliver up to $3000\,\mathrm{fb}^{-1}$ until the end of the Phase-II run period, that is planned from 2024 to 2034, the LHC luminosity will be increased to $5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The technologies needed to realize this goal are under research and development. The changes include all parts of the accelerator chain, from an improved injector chain over crab cavities to new final focus quadrupole magnets (NbSn). During a fill of the LHC the instantaneous luminosity decreases. Therefore the maximum instantaneous luminosity is higher than the average luminosity. Techniques to level the luminosity during the data taking fill are investigated in order to relax the resulting harsh challenges for the experiments.

2.4.2 Upgrade program of the ATLAS experiment

The ATLAS collaboration plans to use the above introduced LHC shutdowns to ensure and improve the detector performance in the high luminosity scenarios and maintain the detector electronics.

LS1

The major upgrade project for the LS1 is the insertion of a fourth pixel layer, the so-called Insertable B-Layer (IBL), inside the existing vertex detector as well as the revision of the current pixel detector services. Both upgrades are shortly introduced in chapter 2.4.3. As the development and test of the IBL modules is the main focus of this work, the IBL project is described in detail in chapter 4.
Additionally to this pixel detector upgrade, a number of smaller repairs and improvements as well as service works are foreseen during LS1.

LS2

Large efforts are undertaken to ensure and even improve the ATLAS detector performance in the scenario of the LHC Phase-I, when the delivered luminosity will exceed the nominal design luminosity by a factor of about two. These upgrades primarily address the ATLAS trigger system. The low p_T trigger threshold for isolated leptons needs to retain good physics performance. At even higher event rate this is a serious challenge for the trigger system.
ATLAS needs to cope with 55 to 80 pile-up events per bunch crossing at a luminosity of $2.2 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

[7] Linear Accelerator

A strong reduction of background events is needed to avoid increasing the p_T threshold to control the event rates, which would significantly reduce the physics signal efficiency. The main sources of background are jets that are recognized as electrons in the calorimeter and fake muons in the spectrometer. Therefore, the foreseen Phase-I upgrade will involve a higher calorimeter granularity in the level-1 trigger generation to add robustness versus fake electrons. New calorimeter readout boards for the electromagnetic and forward calorimeters are needed to achieve this goal. The fake muon background is addressed by introducing a new muon trigger device and new tracking detectors in the forward muon spectrometer.
Additionally, all upgrades inserted during LS2 are foreseen to be operated also during HL-LHC. Therefore, they must be able to cope with the challenges introduced by the even higher luminosity during Phase-II. A detailed motivation and complete description of all Phase-I upgrades can be found in [6].

LS3

As introduced above, the LHC upgrade plan for Phase-II aims to increase the nominal luminosity by a factor of ~ 5. This corresponds to approximately 140 instantaneous interactions per bunch crossing. This huge increase requires a detector that is able to cope with the increased occupancy as well as radiation damage. At such high luminosity the occupancy in the TRT system will reach 100 % and also the performance of the two silicon sub-trackers will suffer severely from the increased luminosity. Furthermore, the expected end of lifetime of the silicon pixel detector is supposed to correspond to the collection of $400\,\text{fb}^{-1}$ of data, and for the strip detector it should correspond to the recording of about $700\,\text{fb}^{-1}$. Integrated luminosities in this order of magnitude will be achieved at the beginning of the LHC Phase-II. Thus a complete replacement of the inner tracking system is necessary to ensure good track reconstruction, vertex resolution and b-tagging, and lepton identification performance of ATLAS until the end of Phase-II. The proposed new inner tracker consists of an all-silicon-tracker with a four layer pixel system at smaller radii to provide good pattern recognition and vertex measurement, and three short-strip layers that are followed by two long strip layers. This layout promises to even improve the tracking performance of the inner detector in scenarios with up to 200 pile-up events [7]. The readout of the new inner tracker must be upgraded as well for two reasons: The readout must cope with the increased data rate due to the high occupancy and should additionally provide input for the new region-of-interest based track trigger.
A completely new, highly efficient trigger architecture is needed during Phase-II. Using the present trigger architecture would result in a Level-1 trigger rate of 500 kHz or even above, which is well above the 100 kHz trigger rate supported by the ATLAS readout electronics. The preferred solution is a two stage hardware trigger system. It is planned to consist of a Level-0 trigger at a rate of about 500 kHz, which is further reduced to 200 kHz by a Level-1 trigger using the information of the tracking system. As the current detector readout system is designed for the Level-1 trigger rate of 100 kHz during Phase-I, the readout electronics for all detector components needs to be replaced. Especially the new calorimeter readout electronics should provide the full granularity of the calorimeter as input for the trigger system, to reduce the background as much as possible. A successful implementation of the track trigger based Level-1 trigger, with additional input of the calorimeter with full granularity can potentially enable ATLAS to explore the full physics potential of the increased luminosity [7].

2.4.3 ATLAS pixel upgrades

LS1

The ATLAS pixel detector will undergo a major revision already during the LS1. As no pixel detector upgrade is foreseen during LS2, the upgrades during LS1 target both the LHC run Phase-0 and run Phase-I. The main project is the insertion of the Insertable B-Layer (IBL). This fourth pixel layer at a very small radius of 3.3 cm and with decreased pixel size will:

- **Recover from eventual failures** in the present pixel system, especially the innermost layer (B-Layer). Irreparable failures will occur in the present pixel system with operation time due to radiation damage and thermal stress. In particular, data losses in the present B-Layer significantly decrease the vertex resolution (see chapter 4.2) and thus influence the b-tagging performance. The IBL is capable to fully restore the b-tagging efficiency of the present pixel detector even in the hypothesis of a loss of the complete B-Layer.

- **Ensure excellent vertexing and b-tagging performance** during LHC Phase-I. The readout inefficiency of the present pixel system will rise due to the increased occupancy caused by the pile-up during Phase-I. Again the effect on the B-Layer will be most severe, resulting in decreased b-tagging performance. The IBL guarantees excellent future performance by the addition of a layer with reduced occupancy due to the decreased pixel size and high readout efficiency (see chapter 5).

- **Add robustness to tracking** with a fourth track point in the high luminosity pile-up environment. The track reconstruction becomes even more challenging in the presence of high luminosity pile-up background. The addition of a fourth track point with high granularity and comparably low occupancy helps the pattern recognition to suppress fake tracks and ensure the tracking performance in the presence of high luminosity effects.

The development and test of the IBL pixel modules is the main focus of this work. Therefore the IBL project is described in detail in chapter 4. Affiliated to the IBL barrel layer is the insertion of a beam monitor detector based on diamond sensors (Diamond Beam Monitor, DBM). This detector consists of four telescopes at very high η with three planes each, facing the interaction point. Each plane consists of a single chip hybrid pixel module (see chapter 3.3) using diamond as sensor material. Due to its very high granularity this new beam monitor promises to improve the luminosity measurement especially in the high occupancy environment of Phase-I [8], when the present Beam Condition Monitor (BCM), which consists of diamond pad detectors, saturates [9].
Additionally to the IBL insertion, the pixel detector has been brought to the surface for repair and service replacements during LS1. The electrical to optical data transmission conversion was originally implemented on dedicated boards (Patch Panel 0, PP0) located inside the pixel detector volume. Losses of the laser diodes driving the signals to the detector have been observed during the first run period. Such laser diodes could be replaced as they are located outside the detector volume. To be able to improve the replacement time of the laser diodes inside the detector volume, new detector services (new Service Quarter Panel (nSQP) have been developed. These nSQPs route the signals electrically to the outside of the pixel detector volume and locate the electrical to optical data conversion further away from the interaction point. This change enables the repair of eventual laser diode failures during the short yearly shutdowns of LHC.

LS2

No update of the pixel detector is currently foreseen during LS2. As explained above, the IBL, which is installed during LS1, will ensure a good performance of the pixel detector also during LHC Phase-I. Only under unexpected scenarios, such as an accident, the LS2 would provide a good window of opportunity to intervene.

LS3

As previously motivated, a complete redesign of the pixel detector is essential for the LHC run Phase-II. The new pixel system should in particular sustain the harsh radiation environment and provide fast information for the intended new track based trigger system.
For the estimated 3000 fb^{-1} collected during Phase-II, a total ionizing dose (TID) of 7.7 MGy and a 1 MeV neutron equivalent fluence of $1.4 \times 10^{16}\,\mathrm{cm}^{-2}$ is predicted for the innermost layer, which is well above the tolerances of the present pixel detector technology. The outermost layer at larger radii will be exposed to a TID of 0.9 MGy and a 1 MeV neutron equivalent fluence of $1.7 \times 10^{15}\,\mathrm{cm}^{-2}$. This huge difference in the required radiation tolerance motivates the usage of different pixel technologies for the inner and outer layers. Especially for the large silicon area of the outer two layers it is reasonable to use a less costly technology than for the extremely challenging innermost layers of comparably smaller silicon area.
The track based trigger system requires the new pixel detector readout electronics to provide sufficient bandwidth for the Level-0 trigger with a rate of 500 kHz. This requirement is a consequence of the proposed trigger algorithm using regions-of-interest to estimate the p_T of the tracks, which is then used in the Level-1 trigger algorithm. The minimum bandwidth is the only restriction of this track trigger approach. However, a complementary idea using self-triggering double layers reduces the restrictions on the bandwidth, but has strong implications on the mechanical layout.
Furthermore, the new pixel detector must be able to resolve the multiple pile-up vertices in the high luminosity environment and assign the high p_T jets, tracks and secondary vertices to the vertex of particular interest. This affects especially the needed granularity for the different radii.
A pixel detector layout capable to fulfill the above requirements is proposed. This layout splits the pixel detector in two parts using different technologies. Two inner barrel layers with a small pixel size of only 25 µm × 150 µm in very radiation hard technology are foreseen. These are surrounded by two outer barrel layers and six additional disks in the forward regions with a pixel size of 50 µm × 250 µm. This design increases the number of individual pixel readout channels by nearly one order of magnitude (above 600 million channels) compared to the ∼ 80 million channels of the present pixel detector and distributes them on a total surface of 8.2 m^2 (about 3.6 times higher than the present 2.3 m^2). R&D for both pixel flavors has started. For the innermost layers the requirements, especially pixel size and radiation hardness, are the main fields of research. Among several competing technologies, a hybrid pixel detector layout using thin ($\lesssim$ 150 µm thickness) n-in-n pixel sensors connected to readout electronics produced in a 65 nm CMOS[8] technology is the baseline. For the two outer layers the constraints of the radiation hardness and granularity are lower, but due to the huge silicon surface of these layers the cost is an important factor to be reduced. The IBL pixel modules fulfill the requirements of the outer layers in terms of granularity and radiation hardness and consequently only a comparable small revision of the readout chips would be needed to meet the requirements in terms of bandwidth and track trigger information. Thus a re-use of the IBL technology is attractive as well as to reduce development costs. To further reduce the costs, new silicon sensor types, that are cheaper to produce, are under investigation.

[8] Complementary Metal Oxide Semiconductor

Another approach uses industrial CMOS processes with the possibility to deplete the bulk material for the sensor production, which has several advantages. A first amplifier step and additional logic can be implemented in the sensor itself and the resulting high signals can be capacitively coupled to the readout chip. This avoids the costly bump bonding procedure, which furthermore limits the possible granularity due to the needed bump spacing. This module concept is studied in chapter 7. An even further step in this direction is the possibility to use the bulk of the readout chip itself as sensor material, which becomes possible with new industrial processes using deep implants. This new and very promising technology is also under investigation.

Chapter 3

Particle Tracking with pixel detectors

3.1 Interaction of particles with matter

In tracking detectors the particles ideally deposit only a small amount of their energy in the sensitive material, as the complete absorption of the particle should happen in the calorimeter system. Furthermore, energy transfer to the insensitive material such as mechanical support structures and services leads to an error in the track reconstruction. The physics processes resulting in the energy transfer from the particle to the trackers material differ for charged and neutral particles. The particles introduced in chapter 2.1 can only interact with matter using the force they are sensitive to. For example the neutrinos can only interact via the weak force and are thus generally not detected, whilst all charged particles interact electro-magnetically and neutrons take part in strong interactions with the matters' nuclei. All these interactions are described in detail in the literature [10, 11] and only a short introduction to the interactions of main interest for silicon trackers is given here. The detection of charged particles, as in the experiment, is covered in chapter 3.1.1, and that of photons in chapter 3.1.2, as they are mainly used in this work to test and qualify the IBL modules.

3.1.1 Detection of charged particles

Three fundamental processes can lead to the detection of charged particles. These are the ionization of the atoms of the material, the emission of Cherenkov light and the emission of transition radiation in case of inhomogeneities in the refraction index of the material. All three are caused by the electromagnetic interaction.
The mean energy loss dE per length dx, taking into account all these processes, is approximated by the Bethe-Bloch-formula [12]:

$$-\frac{dE}{dx} = \frac{4\pi r_e^2 m_e c^2 N_A Z z^2}{A\beta^2} \cdot \left(\frac{1}{2} \ln \left(\frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} \right) - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right), \tag{3.1}$$

with Z and A being the atomic and the mass number of the material, N_A the Avogadro constant and r_e the classical electron radius of 2.8 fm. z is the charge of the incident particle in units of e and the kinematic variables $\beta = \frac{v}{c}$ and $\gamma = \frac{1}{\sqrt{1-v^2/c^2}}$. The mean excitation energy I of the material can be approximated further assuming $I \simeq I_0 Z$ with $I_0 = 12\,\text{eV}$. T_{max} is the maximum kinetic energy which can be imparted to a free electron in a single collision.
The energy loss depends only on the velocity of the particle and not on its mass. Thus figure 3.1 shows the mean energy loss as a function of $\beta\gamma$. Equation (3.1) describes the displayed $\frac{dE}{dx}$ above its first maximum from about $\beta\gamma \simeq 0.05$. Below this $\beta\gamma$ value, other processes than ionization become dominant. For $\beta\gamma > 0.05$ the $\frac{1}{\beta^2}$-term is dominant until $\frac{dE}{dx}$ reaches a minimum at approximately $\beta\gamma = 3$. Above this, the energy loss increases only slightly ($\propto \ln\beta\gamma$) for all heavy charged particles and saturates for

high $\beta\gamma$ due to polarization effects in the material. For light charged particles, especially electrons, the $\frac{dE}{dx}$ rises then steeply for high $\beta\gamma$ due to the Bremsstrahlung, which is a physics process related closely to the pair creation of photons and thus will be explained in chapter 3.1.2.

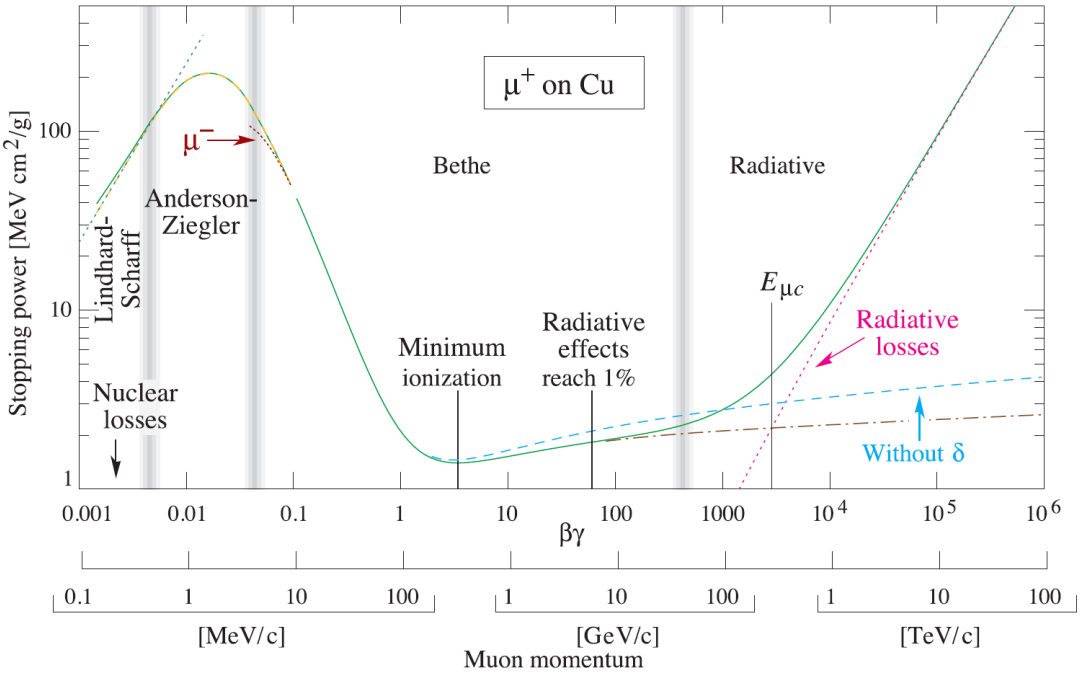


Figure 3.1: Energy loss (or stopping power) for μ^+ penetrating copper as a function of $\beta\gamma$ [12]. The dashed lines for $\beta\gamma > 1$ illustrate the energy loss for heavy charged particles as described by the Bethe-Bloch-Formula, while the total energy loss includes Bremsstrahlung which becomes dominant at high momentum for light charged particles.

Due to the only rather reduced increase above the minimum, all particles with $\beta\gamma > 3$ are commonly called Minimum Ionizing Particles (MIP). This condition is especially fulfilled for all charged particles to be detected in high energy physics experiments.
Equation (3.1) describes the mean energy loss in a material of thickness dx. However, the differential energy loss in thin material layers is not gaussian distributed. Starting from the probability for an interaction $\sigma\rho x$ within the distance x and a material with the atomic density ρ, Landau and Sternheimer have calculated the distribution of the energy loss in thin material layers. The resulting Landau distribution is not symmetric but shows a tail to high energy transfers. This tail has its origin in single interactions transferring enough energy to the atomic electron to be an ionizing particle itself (δ-electron). This tail shifts the mean energy transfer to a higher energy than the most probable energy transfer. Figure 3.2 illustrates the distribution of the energy loss for a MIP in silicon layers of different thickness.

3.1.2 Energy deposition of photons

The interactions of photons with matter are different from the interactions of charged particles. Only pair-creation is important for high energetic photons. If the photon energy is at least twice the rest energy of an electron, it can create an electron-positron pair in the electro-magnetic field of a nucleus. This process is the only important interaction of the high energetic photons produced in collider experiments and actually an unwanted process, as the photon does not enter the calorimeter system as such, and

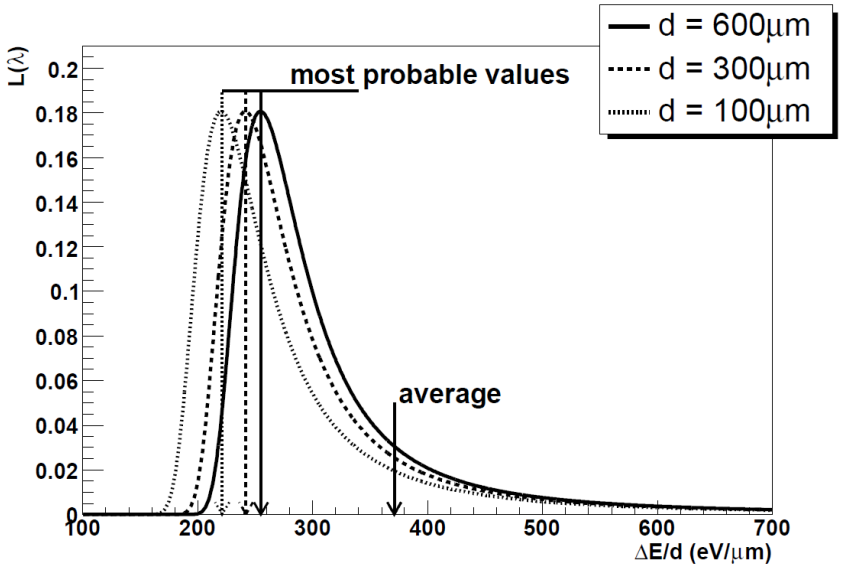


Figure 3.2: The energy loss distribution for a MIP in thin silicon layers of thickness d, normalized to d [13]. The shift of most probable value (here normalized to $\Delta E/d$) with respect to the most probable value is obvious due to the high energy loss tail coming from δ-electrons.

the reconstruction of the photon from the electron and positron tracks is difficult. Figure 3.3a shows the basic feynman diagram of a pair creation. The interaction vertex of the bremsstrahlung illustrated in figure 3.3b consists of the same particles and reversed time line and is thus described similarly. As

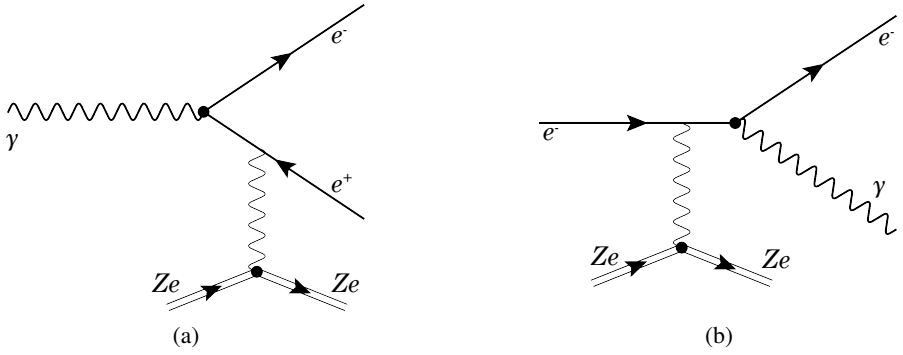


Figure 3.3: Feynman diagrams for pair creation (a) and bremsstrahlung (b). As the vertices of both processes are the same, it is physically a similar process and thus can be described similarly.

mentioned above, additionally to the ionization processes, electrons - due to their small mass - loose a significant amount of their energy due to bremsstrahlung. Due to their small mass, high energetic electrons are slowed down in the electro-magnetic field of the nuclei and therefore emit radiation. The amount of radiative energy loss is proportional to the energy of the particle and can be described by

$$-\left(\frac{dE}{dx}\right)_{rad} = \frac{1}{X_0} \cdot E. \tag{3.2}$$

The proportionality constant X_0 is a material property called radiation length. The energy $E(x)$ of a particle with an incident energy E_0 after traversing a material layer of thickness x is therefore

$$E(x) = E_0 \cdot e^{-\frac{x}{X_0}}.$$

So the radiation length can be expressed by the distance after which the particle energy is reduced to E_0/e due to bremsstrahlung. As the process of pair creation is a similar process, the distance after that $1/e$ of the photons (mean free path λ) have undergone a pair creation process can be expressed by $\lambda = \frac{9}{7}X_0$. Accordingly, it is beneficial for trackers to have a small x/X_0 to minimize the unwanted pair creation processes.
The interaction of low energetic photons with matter is described by the photoelectric- and compton-effect. Both processes are not important in high-energy physics experiments and are thus not described here. However, low energetic photons provide a useful tool to characterize and test the properties of silicon tracker modules for two reasons: their convenient availability in laboratory environment from nuclear decays and laser setups, and their well known energy deposition in the sensitive material.

3.2 Properties of segmented trackers

As introduced in chapter 2, the main task of the pixel detector is the resolution of the primary and secondary vertices and the association of high momentum isolated tracks and jets to those. Additionally, pixel detectors contribute to the measurement of the momentum of the tracks. These tasks are nowadays addressed by a set of finely segmented silicon layers surrounding the collision point. The data of these layers are analyzed using pattern recognition programs that transform the coordinate measurements to tracks, and assign the point of origin and the momentum vector to each track. The combination of all tracks is then used to resolve the primary and secondary vertices. Often the impact parameter d_0 is used instead of the vertex position. The impact parameter is the smallest perpendicular distance between the fitted trajectory and the primary vertex. So tracks originating from the primary vertex have a d_0 within the impact parameter resolution, whereas a larger impact parameter indicates tracks originating from secondary vertices.
The main properties driving the design of inner tracking systems in high energy physics experiments are the spatial resolution of the vertex (or alternatively the impact parameter resolution) and the error on the momentum measurement. Both are influenced by the spatial resolution of the layers and multiple scattering, introduced in chapter 3.2.1 and chapter 3.2.2. The influence of multiple scattering on the impact parameter resolution will not be discussed in detail here, but a simple approximation of a two layer segmented vertex detector reveals already the main dependencies that should be respected when designing a vertex detector with emphasis on secondary vertex tagging, and thus is shown in chapter 3.2.6.

3.2.1 Spatial resolution

The spatial resolution in one direction is determined by the segmentation width, the signal sharing between neighboring segments and the threshold of the readout electronics (see chapter 4). A simple approximation, neglecting all effects but the segmentation width, is sufficient to understand the basic principles of vertex measurement. The resolution can be calculated very easily assuming a uniform particle occupancy, binary readout, and full efficiency over the whole segmentation. Then the occupancy distribution $f(x)$ per segment with the width d can be presumed to be constantly 1 from $-d/2$ to $d/2$. The error on the position measurement is thus the standard deviation σ of $f(x)$, which is in this case

given by

$$\sigma = \sqrt{\frac{\int x^2 f(x)\, dx}{\int f(x)\, dx}} = \sqrt{\frac{\int_{-d/2}^{d/2} x^2\, dx}{\int_{-d/2}^{d/2} dx}} = \frac{d}{\sqrt{12}}. \tag{3.3}$$

Additionally, analog hit information in more than single segment clusters can improve the spatial resolution further. Commonly, center of gravity or eta calculations [14] are used for this task.

3.2.2 Multiple scattering

Additionally to the spatial resolution, another effect influences the detector performance. A charged particle traversing a material scatters elastically off the nuclei. Albeit this process is described by the Rutherford formula [15], and thus the probability for scattering at small angles is the largest, multiple independent scattering processes can result in a significant deviation of the particle direction after a material layer of thickness l. An approximation derived in [16] shows that the net scattering angles can be assumed to be gaussian distributed with a mean value of 0°. The standard deviation σ_Θ of this distribution depends on the radiation length X_0 of the material as defined in chapter 3.1.2, the momentum p, and the velocity v of the incident particle [17, 18]:

$$\sigma_\Theta \approx \frac{13.6\,\text{MeV}}{pv} \cdot \sqrt{\frac{l}{X_0}}. \tag{3.4}$$

The uncertainty on the vertex resolution due to multiple scattering increases for low momentum particles, because of the inverse dependency of p. Reducing the detector thickness l and using detector material with larger X_0 decreases the standard deviation of the scattering angle distribution.

3.2.3 Charged particle trajectories in magnetic fields

The trajectories of particles with charge q and momentum $\vec{p}$ in a static magnetic field $\vec{B}(r)$ is bent by the Lorentz Force

$$\frac{d\vec{p}}{dt} = q\left(\vec{v} \times \vec{B}\right).$$

As the magnetic force does not change the particles energies, the path length s can be used to substitute $ds = vdt$. The trajectory is then given by the differential equation

$$\frac{d^2\vec{r}}{ds^2} - \frac{q}{p}\frac{d\vec{r}}{ds} \cdot B(\vec{r}) = 0.$$

For large momentum tracks, the solution can be expressed differently in two planes. In the plane containing the magnetic field the track is a straight line $f(z) = a + mz$, with a being the intercept at the origin and m the slope at the origin. For not too low momenta, the track can be approximated with the quadratic polynomial $f(x) = a + mx + (c/2)x^2$ in the bending plane[1]. Here only the parameter $c = 1/R$ describes the radius R of the curvature and thus the transverse momentum [19]. The fitting of a straight line in this plane is sufficient to obtain the impact parameter. The impact parameter resolution is discussed in chapter 3.2.4. Due to the kinematics of proton-proton collisions in LHC experiments, the

[1] In solenoid magnetic fields this plane is the transverse plane.

momentum conservation is used only in the transverse plane and thus it is sufficient to study the error of the quadratic term of the fit for the transverse momentum resolution (chapter 3.2.5).

3.2.4 Impact parameter resolution

When fitting a straight line to $N+1$ equally distributed coordinates measured with spatial resolution σ, the errors on the two fit parameters σ_a and σ_m are fully uncorrelated, if the origin of the reference frame is chosen in the center of the track [19]:

$$\begin{aligned}\sigma_a &= \sqrt{\frac{\sigma^2}{(N+1)}} \\ \sigma_m &= \sqrt{\frac{\sigma^2}{(N+1)}\frac{12N}{(N+2)}\frac{1}{L^2}} \\ \sigma_{am} &= 0\end{aligned}$$

Here L denominates the distance between the first and the last layer ($L = z_N - z_0$ with planes positioned at coordinates z_i). The distance between the interaction point and the center of the track is $z_c = (z_N - z_0)/2$. Obviously the impact parameter d_0 is then

$$d_0 = f(-z_c) = a - mz_c$$

and thus the error on the impact parameter σ_{d_0} is the simple error propagation of σ_a and σ_m to the interaction point [19]:

$$\begin{aligned}\sigma_{d_0} &= \sqrt{\sigma_a^2 + \sigma_m^2 \cdot z_c^2} \\ &= \sqrt{\frac{\sigma^2}{(N+1)} + \frac{\sigma^2}{(N+1)}\frac{12N}{(N+2)}\frac{z_c^2}{L^2}}\end{aligned} \tag{3.5}$$

The influence of the spatial resolution σ in both terms shows the need to use fine segmented layers to achieve good impact parameter resolution. At the same time, a large lever arm L reduces the error on the slope. As fine segmented layers at large radii and thus with large surface are very expensive, a compromise that splits the tracker in layers with different technologies is used. Technologies with high granularity such as hybrid pixel detectors (see chapter 3.3) are used for the inner most layers. The layers at larger radii, which provide the needed large lever arm, consist of less expensive concepts such as silicon strip detectors.

3.2.5 Momentum resolution

Similarly to chapter 3.2.4, a detector with $N+1$ layers is assumed. For the transverse momentum resolution the coordinates of the tracks are measured at the positions x_0, ..., x_N with again $L = x_N - x_0$ being the length of the detector. The error on the curvature c is given by [19]

$$\sigma_c = \frac{\sigma}{L^2} \cdot \sqrt{\frac{720N^3}{(N-1)(N+1)(N+2)(N+3)}}.$$

With the curvature $c = -1/R$ and $R = p/(0.3B)$[2], the relative transverse momentum resolution then is [19]

$$\frac{\sigma_{p_T}}{p_T} = p_T \cdot \frac{\sigma}{0.3BL^2} \cdot \sqrt{\frac{720N^3}{(N-1)(N+1)(N+2)(N+3)}}. \tag{3.6}$$

Obviously the relative transverse momentum resolution is proportional to the transverse momentum itself and again a large lever arm L is necessary to achieve good resolution. The dependence on the number of measured coordinates is only of order $1/\sqrt{N}$, but the influence of the robustness of the tracking algorithms on the number of coordinates needs to be considered as well.
The multiple scattering introduced in chapter 3.2.2 influences the transverse momentum resolution, especially for low momentum tracks. Then the uncertainty introduced by multiple scattering in the passed layers exceeds the spatial resolution of the segments. In this case the relative transverse momentum resolution is given by [20, 21]

$$\frac{\sigma_{p_T}}{p_T} = \frac{1}{0.3B} \frac{0.0136}{\beta} \sqrt{\frac{C_N}{X_0 L}} \tag{3.7}$$

and does not depend on the transverse momentum itself of these low momentum tracks. The N-dependent coefficient C_N is equal to 1.3 within 10% accuracy [19].

3.2.6 Vertex resolution with multiple scattering

A simplified vertex detector model to derive the vertex resolution consists of two one dimensional segmented layers at radii r_1 and r_2 from the collision point ($r_1 < r_2$). Albeit assuming a similar segmentation for both layers (which is the case for all currently existing LHC vertex detectors), the resolution of the two layers are not identical due to the effect of multiple scattering at the beam pipe (radius r_0) and at the first detector layer. It is a quadratic combination of the spatial resolution as derived in chapter 3.2.1 and the uncertainty due to multiple scattering, which follows from simple geometrical arguments:

$$\sigma_1 = \sqrt{\left(\frac{d}{\sqrt{12}}\right)^2 + \left((r_1 - r_0)\,\sigma_\Theta^0\right)^2} \tag{3.8}$$

$$\begin{aligned}\sigma_2 &= \sqrt{\left(\frac{d}{\sqrt{12}}\right)^2 + \left((r_2 - r_0)\,\sigma_\Theta^0\right)^2 + \left((r_2 - r_1)\,\sigma_\Theta^1\right)^2} \\ &\approx \sqrt{\left(\frac{d}{\sqrt{12}}\right)^2 + \left((r_2 - r_0)\,\sigma_\Theta^0\right)^2}\end{aligned} \tag{3.9}$$

Here the last approximation assumes the effect of multiple scattering at the innermost detector layer to be small compared to multiple scattering at the beam pipe.
The vertex resolution can be calculated using again similar simple geometrical considerations and equations (3.8) and (3.9). The vertex resolution is then the error propagation of these, and additionally the correlation of the error in the two detector layers due to multiple scattering at the beam pipe must be

[2] This follows considering the sagitta of a part of a circle. In case of a uniform magnetic field the particle trajectory is a circle in the transverse plane.

taken into account in a third term:

$$\begin{aligned}
\sigma_{vtx} &= \sqrt{\left(\frac{r_2}{r_2 - r_1}\,\sigma_1\right)^2 + \left(\frac{r_1}{r_2 - r_1}\,\sigma_2\right)^2 + \frac{2r_1 r_2 (r_2 - r_0)(r_1 - r_0)}{(r_2 - r_1)^2}\,\sigma_\Theta^2} \\
&= \sqrt{\left(\frac{d}{\sqrt{12}}\right)^2 \cdot \left(\frac{r_2^2 + r_1^2}{(r_2 - r_1)^2}\right) + \left(\frac{r_2^2 (r_1 - r_0)^2 + r_1^2 (r_2 - r_0)^2 + 2r_1 r_2 (r_2 - r_0)(r_1 - r_0)}{(r_2 - r_1)^2}\right)\sigma_\Theta^2} \\
&\approx \sqrt{\left(\frac{d}{\sqrt{12}}\right)^2 \cdot \left(1 + \frac{r_1^2}{(r_2 - r_1)^2}\right) + (2r_1 - r_0)^2 \cdot \left(\frac{13.6\,\mathrm{MeV}}{pv}\right)^2 \frac{l}{X_0}}
\end{aligned} \tag{3.10}$$

The dependency on $\frac{1}{(r_2 - r_1)}$ reveals the benefit of a large lever arm of the vertex detector for high momentum tracks, and the factor d shows the importance of a small detector segmentation. The inverse influence of p (if $v \simeq c$ and $c = 1$) describes the dominance of multiple scattering for low momentum tracks. Both terms depend on r_1, so a distance from the beam to the first detector layer as small as possible is crucial for all track momenta to achieve a good vertex resolution. This fact is addressed in ATLAS by the installation of the Insertable B-Layer at a very small radius to improve the vertex resolution further. The simulated improvement due to this upgrade are described in chapter 4.

3.3 Hybrid pixel detectors

Additionally to the main properties needed to achieve good tracking performance as derived above, i.e. small segmentation, low mass, and operation close to the interaction point and thus in a very high radiation environment, fast detectors also are needed in the LHC experiments due to the high bunch crossing frequency. All these requirements are met by hybrid pixel detectors. Hybrid pixel detectors use a two layer approach with particle detection in a first layer, the sensor, and signal processing in a second layer, the readout chip. Each sensor pixel is connected to a readout chain using inter chip connection technologies. In case of the ATLAS pixel detector, solder and indium bump-bonding technologies [22] have been used. A cross section of a single hybrid pixel readout channel is shown in figure 3.4. Typical hybrid pixel modules consist of several ten thousand of such readout channels with very fine pitch, which is a challenge for the bump-bonding technologies.

The main benefit of the hybrid concept is the possibility to use different technologies and even materials for the task of signal generation and processing. Sensors using gas, diamond and several semi-conductor materials exist. In chapter 3.3.1 a short introduction to the working principle of electron collecting silicon sensors as used in IBL is given. A brief overview of the readout electronics then follows in chapter 3.3.2.

3.3.1 Signal generation in silicon sensors

An ionizing particle crossing a silicon layer transfers energy to the silicon atoms (see chapter 3.1). In the band theory [23] this is described by the creation of electron-hole pairs, which can move through the silicon. Although the width of the forbidden gap of silicon is only 1.1 eV, in average 3.6 eV is needed to create an electron-hole pair in silicon since lattice excitations also absorb energy. The electrons or the holes are used to detect the penetrating particle. Immediate recombination of the electrons and holes must be prevented by an electrical field. Therefore they must be separated from each other and the silicon bulk must be empty of free charge carriers. Both are achieved by reversely biasing a pn-junction. The sensor consists of a junction of n-doped and p-doped material, a pn-diode. When two pieces of sil-

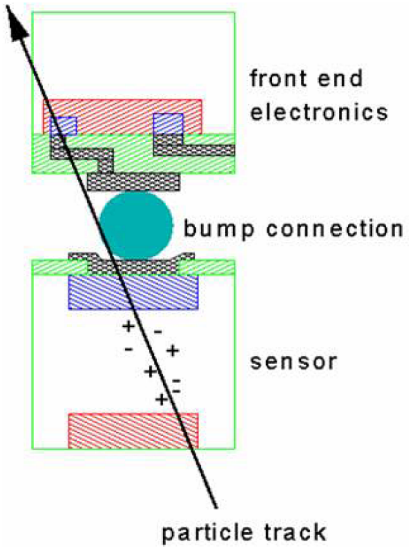


Figure 3.4: Cross section of a single hybrid pixel readout channel [22]. Shown here are the sensor at the bottom, for signal generation, the bump connection in the middle for the interconnection and the readout electronics for the signal amplification and data processing.

icon, one p-doped and the other n-doped, are brought into contact, the electrons of the n-doped material diffuse to the p-doped side (and vise versa) due to the charge carrier density gradient at the junction and recombine. This process stops as soon as an equilibrium between the potentials originating from the arising space charge and the density gradients is reached. An intrinsic zone without free charge carriers is then formed. The movement of electron-hole pairs created in this depletion zone induces currents at the readout electrodes which can be detected. The width of the depletion zone and thus the

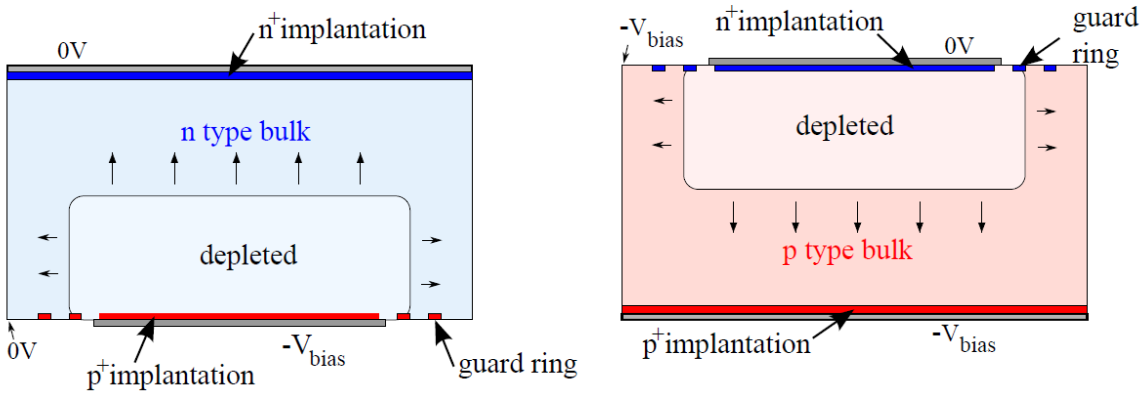


Figure 3.5: Cross section of a n-bulk (a) and a p-bulk (b) planar silicon sensor. The guard ring location and the direction of the depletion zone growth is indicated. Adapted from [24].

number of electron-hole pairs contributing to the signal can be increased by an external electrical field compensating the intrinsic electrical field. Optimally the depletion zone grows through the full sensor bulk material. Additionally, this electrical field separates the electron-hole pairs and the charge carriers

move through the silicon due to drift instead of diffusion, which results in a faster induced signal on the electrode and a faster collection time. This field is created by applying a high voltage (HV) reversely to the pn-diode.
Electron-collecting silicon pixels sensors have highly n-doped readout electrodes connected to the readout electronics through the bump connection. A second electrode, highly p-doped, is connected to the HV. This electrode is necessary to prevent the break-through of the HV as soon as the full bulk of the sensor is depleted. Several electrode layouts exist. Both versions used in the IBL are described in detail in chapter 4. Figure 3.5 illustrates the growth of the depletion zone and the charge carrier drift for n-bulk and p-bulk silicon sensors. In case of n-bulk sensors the pn-diode is at the biasing electrode, while for p-bulk sensors the pn-diode is at the readout electrode itself.

Leakage current

Albeit the diode is reversely operated, a small leakage current arises. This current is induced by thermally created electron-hole pairs and it is proportional to the volume V and to the temperature dependent intrinsic density $n_i(T)$ of charge carriers (with charge e) in pure silicon. The recombination of charge carriers with a life-time of τ decreases the leakage current, and thus the leakage current is given by [25]

$$I_{leak} = \frac{e\, n_i(T)\, V}{2\tau}$$

for a given bias voltage. With the charge carrier density calculated using the Fermi-Dirac statistics [26] this results in the proportionality [13]

$$I_{leak} \propto T^{\frac{3}{2}} \cdot \exp\left(-\frac{E_G}{2k_B T}\right). \tag{3.11}$$

E_G denominates the size of the band-gap and k_B the Boltzmann constant. The leakage current is highly temperature dependent. An increase in temperature of about 7 °C doubles the leakage current.
The leakage current is a source of shot noise to the input of the amplifier (see chapter 3.3.2 and chapter 5.3). The influence of this contribution on the total electronics noise is typically negligible for the low leakage current of un-irradiated silicon sensors. But with increasing leakage current due to radiation induced damage as explained below, the leakage current becomes a significant noise source.
A pn-diode has a break-down voltage (V_{bd}) at which uncontrolled avalanche starts, and thus the current through the sensor will rise drastically above a certain break-down voltage. The V_{bd} and the leakage current as a function of the HV are an important characteristic to qualify silicon sensors.

Effects of radiation damage

Non-ionizing interactions of particles with silicon atoms change the sensor properties. Most of these changes degrade the sensor performance. If the incident particle has enough energy to displace a silicon atom from the crystal lattice or to undergo nuclear interactions, the defect is not reversible. A non silicon impurity, a vacancy in the crystal lattice or an atom in between the regular lattice locations (interstitial) are called point defects. If enough energy was transferred, the recoiled atom produces further damage and cluster defects are formed. All these defects can add new energy levels to the band structure, which act as combination and recombination centers and increase the amount of thermally generated charge carriers. This effect has a huge influence on the leakage current, which increases with radiation damage. The radiation damage differs for different particles, so it is needed to scale the radiation damage caused

by Non-Ionizing Energy Loss (NIEL) to a standard irradiation in order to compare the damage caused by different particles. Usually it is scaled to the damage caused by a fluence of 1 MeV neutrons. So the equivalent fluence is $\Phi_{eq} = \kappa \cdot \Phi_{irr}$. The 1 MeV neutron equivalent fluence will be expressed in $n_{eq}cm^{-2}$ in the following. The damage factor κ depends on the type and the energy of the particles causing the radiation and on the irradiated material. The leakage current increase in irradiated silicon I^{irr}_{leak} is proportional to the depleted volume dA and to the particle fluence Φ_{eq}. Therefore, the leakage current after irradiation is [13]

$$I_{leak} = I^{unirr}_{leak} + \alpha \Phi_{eq} dA.$$

The displacement of silicon atoms has two additional effects influencing the sensor properties. First, the displacement of atoms from the lattice structure decreases the effective concentration of donors N_D and at the same time the fact that these damages act as acceptor-like states increases the acceptor concentration N_A. Thus the effective doping concentration $N_{eff} = N_D - N_A$, which is positive for n-type silicon, will flip its sign after a certain fluence and thus type inversion from n-type silicon to effective p-type silicon will happen. This effect is observable, if the depletion voltage is measured as a function

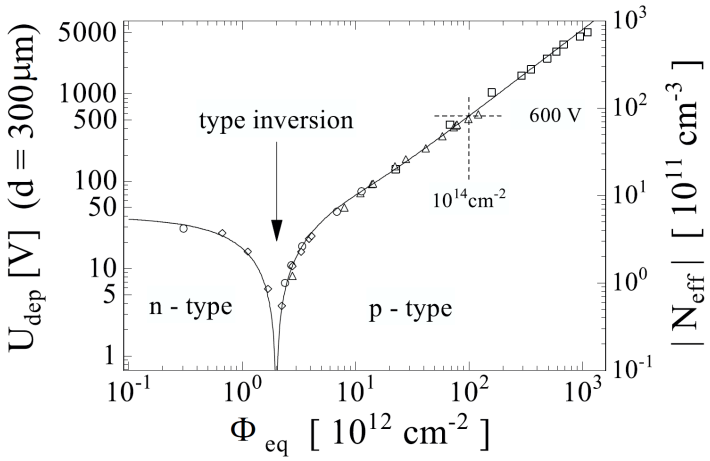


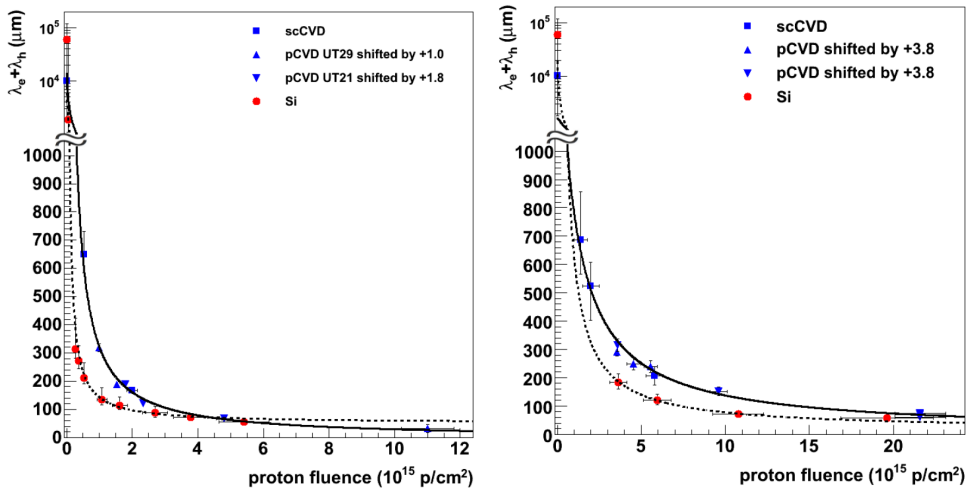
Figure 3.6: The measured depletion voltage and the effective doping concentration as a function of the 1 MeV equivalent fluence [27].

of the fluence. This measurement is shown in figure 3.6.
The second effect is the reduction of the mean free path of the charge carriers due to trapping in potential minima originating from the defects. This reduces the mean free path of the charge carriers and the signal size decreases. Detailed studies have been performed to compare this effect in different sensor materials [28, 29]. Figure 3.7 shows the measured mean free path in silicon and different diamond materials as a function of the proton fluence[3] in comparison to the expectations.

3.3.2 Signal processing in the readout electronics

The readout electronics usually consist of an analog part to amplify and shape the signal and a digital data processing logic. The analog readout chain typically uses a charge sensitive amplifier (CSA) with a feedback circuitry to discharge the feedback capacitance as shown simplified in figure 3.8. Several dis-

[3] Here the fluence is not scaled to the 1 MeV equivalent fluence, because the hardness factor for diamond has a large uncertainty.



(a) (b)

Figure 3.7: Total mean free path ($\lambda_e+\lambda_h$) for different diamond and silicon sensors irradiated with 25 MeV protons (a) and 24 GeV protons (b) [28].

charge mechanisms exist, for example constant current feedback, ohmic resistor discharge or switched discharge. The CSA output signal is then amplified further or directly compared to a threshold voltage. If a constant current feedback is used, as in case of the ATLAS Front-End chips, the result of the comparison is a binary signal, which is high for the time of the CSA output being above the threshold voltage (Time over Threshold, TOT). The TOT is then in first order proportional to the charge at the input of the CSA. Secondary order effects, such as the time-walk and non constant discharge rate, lead to non-linearities. Two different effects contribute to the time-walk. The first effect originates from the fact, that due to the finite amplifier rise-time, the time needed by the preamplifier to achieve the full signal heights depends on the input signal size itself. The preamplifier rise-time depends (among others) on the preamplifier bias current and on the detector capacitance. A second contribution to the time-walk originates from the signal dependent propagation delay of the comparator while switching. The comparator needs to charge a parasitic capacitance at it's output. The current, that is available to charge this capacitance, depends mainly on the comparator bias current, but also on the signal size. This results in a propagation delay that again is increased for small input signals. Thus, for very small input signals the hit detection time can be significantly delayed. The time-walk dependency on the signal size of both time-walk sources is illustrated in figure 3.8. The time-walk effect is of particular importance for detector operation, when the hit detection time must be known very precisely to associate the hit to the correct bunch crossing. The discriminator output signal is routed to the digital readout chain and the digital readout logic stores the hit information in buffers. In the case of ATLAS pixel modules, the hit information consists of a time-stamp to associate the hit to the correct LHC bunch crossing, the pixel address and the digitized TOT information. A detailed description of the IBL readout chip will be provided in chapter 4.3.3.

Radiation damage in readout electronics

As the sensor material, also the readout electronics suffers from radiation induced damages. In contrary to the sensor, the bulk damages due to NIEL described in chapter 3.3.1 have nearly no influence on

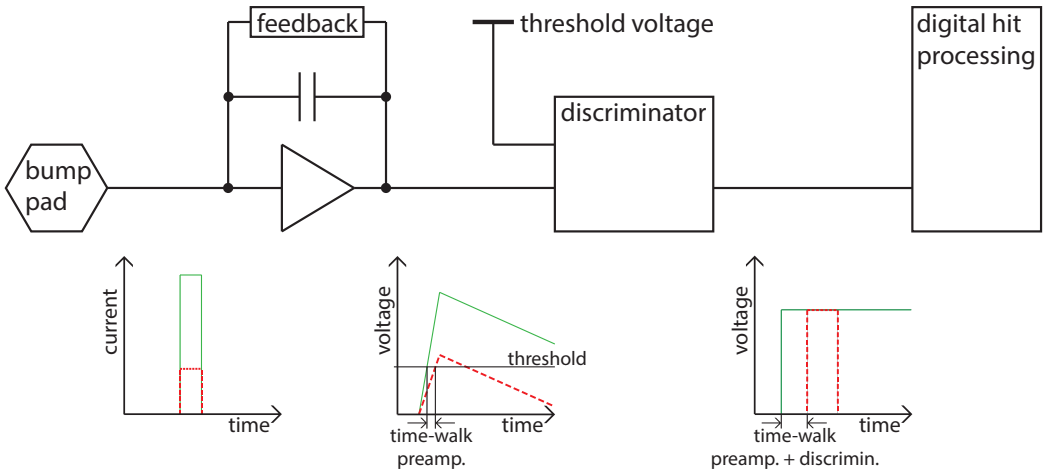


Figure 3.8: Simplified schematics of a typical analog readout chain for hybrid pixel detectors. The signal shape is illustrated for a large input charge (solid green line) and for a small input charge (dashed red line) after each building block.

the readout electronics properties, because the doping densities used for the active devices (MOSFETs) are much higher compared to the sensor material, and therefore the CMOS layer is rather insensitive to changes of the effective doping concentration. But the transistor characteristics suffer from radiation damage close to the SiO_2-Si interface [30]. This damage is called surface damage. Two type of defects in the surface can be distinguished, that occur with increasing Total Ionizing Dose (TID). On one hand, the radiation activates existing precursors of traps in the SiO_2 for positive charge carriers. The accumulation of a positive space charge in these traps, which is located right below the gate contact, influences the transistor characteristics. On the other hand, traps at the SiO_2-Si interface exist due to the abrupt transition from the crystal lattice of the silicon to the amorphous silicon dioxide material. The density of these interface traps increases by orders of magnitudes with the absorbed dose [31, 32]. The interface traps attract positive as well as negative charge carriers and thus influence the electron current in the case of NMOS transistors differently from the hole current in the case of PMOS transistors. To decrease the effect of these radiation damage types, transistors with very thin SiO_2 layers and a small feature size are used.

Digital readout logic additionally suffers from a transient effect, that comes with a high linear energy transfer from charged heavy particles. Such particles, in particular ions created in hadronic interactions of the silicon lattice with neutrons or charged hadrons, hitting the depleted gain region of a transistor can change the state of memory cells by depositing large amounts of charge. This effect is called Single Event Upset (SEU). SEUs can lead to wrong information stored in or transmitted by the chip, and in the worst case the chip can enter a unrecoverable state due to change of chip configuration registers. Several methods exist to increase the hardness against SEUs of memory cells. Examples are DICE-cells [33] and the addition of logic to detect and correct SEUs. An example of the latter is the replication of memory cells combined with a majority vote logic. In very high radiation tolerant electronics like the FE-I4 readout chip (see chapter 5) a combination of such methods is used.

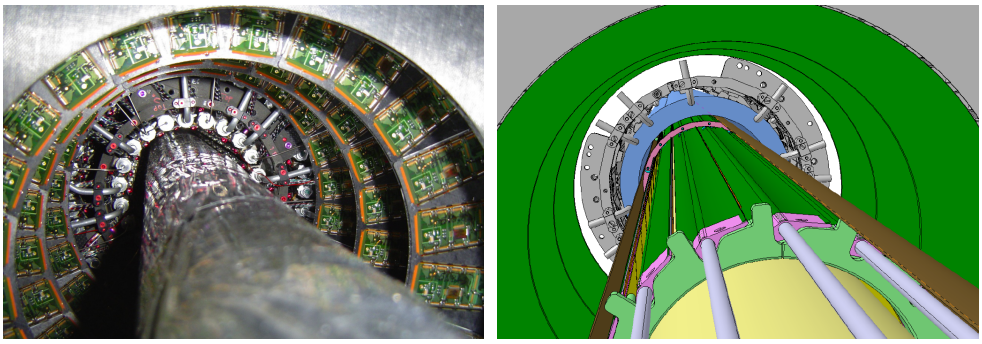
Chapter 4

ATLAS Insertable B-Layer Upgrade project

In order to achieve the goals of the IBL described in chapter 2.4.3, the design rules motivated in chapter 3.2 (small segmentation width, small radius, low radiation length) must be taken into account. An additional challenge for IBL is the fact that this new sub-detector is inserted into an existing detector. This results in additional stringent engineering constraints.

4.1 Challenges and design of the ATLAS IBL detector

The IBL is inserted inside the existing pixel detector package. The tight clearance between the innermost pixel layer and the beam pipe is too small for the insertion of an additional layer. Therefore, the IBL is mounted on a new beam pipe with smaller radius. Figure 4.1 demonstrates the tight mechanical



(a) (b)

Figure 4.1: A photo of the pixel detector surrounding the beam pipe (a) demonstrating the tight mechanical clearance. A drawing of the inserted IBL mounted on a new beam pipe with reduced radius (b) [8].

environment.
The beam pipe outer radius is reduced from 36 mm to 29 mm to clear space for the IBL. The inner envelope of the existing pixel detector has a radius of 45.5 mm. Additional space for the IBL Insertion Tube (IST) and safety clearances must be respected. Thus the allowed space for the IBL staves including all services is only 9 mm. The mean radius of the sensitive area is 33.25 mm and the smallest distance of the sensitive electronics to the interaction point is only 31.95 mm. Figure 4.2 lists all important radii and constraints in $r\phi$ view. These mechanical constraints set strong challenges on the technologies required for the IBL.

- The high radiation dose due to the small radius makes very radiation hard technologies mandatory. The sensors need to withstand a NIEL fluence of $5 \times 10^{15}\,\mathrm{n_{eq}cm^{-2}}$ and still have a hit detection

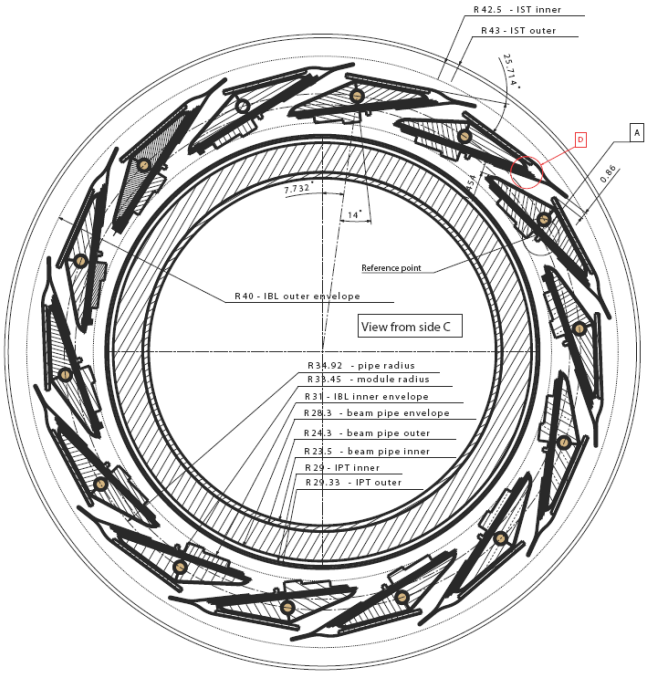


Figure 4.2: Cross section of the IBL layout in $r\,\phi$ view [34].

efficiency above 97%. In the readout electronics a TID of 250 Mrad at the IBL end of lifetime is expected. These specifications include safety factors.

- The small clearance of 9 mm does not allow tilting of modules in the direction along the beam pipe, which is usually done to overlap the modules and reduce the inactive area. Therefore, sensors with slim inactive edges in the z-direction need to be used to reduce the geometrical inefficiencies. Additionally, full coverage in ϕ requires modules with a large active width, but only one row of readout chips. So a very large readout chip is used, that increases the active area fraction from 75 % (present pixel detector case) to 90 % (IBL case).

- In total, the IBL is a 7 m long object, including the services and the new beam pipe, that needs to be inserted into the very fragile pixel package. The radial clearance for insertion is only 2 mm. This requires complex engineering of the installation procedures and tools. The bow of the whole package needs to be controlled and a very precise alignment is mandatory. A full scale mockup is developed to extensively test all necessary operations.

These challenges are addressed in the module design as well as in the layout of the mechanical and electrical support structures.

4.2 Expected ATLAS performance improvement with the IBL

Detailed simulations of the inner detector (ID) performance with and without the IBL have been performed. The study evaluates the performance improvement of the ATLAS inner detector with IBL at the luminosity during Phase-I. The IBL has been added to the ATLAS Geant4 [8] geometry model and into the ID software chain. The detector response model is derived from the existing pixel digitization

algorithm. A full description of the simulated model and the results is given in [8], while selected results

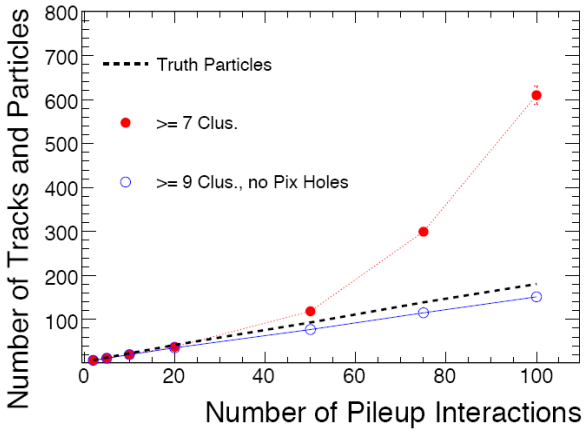
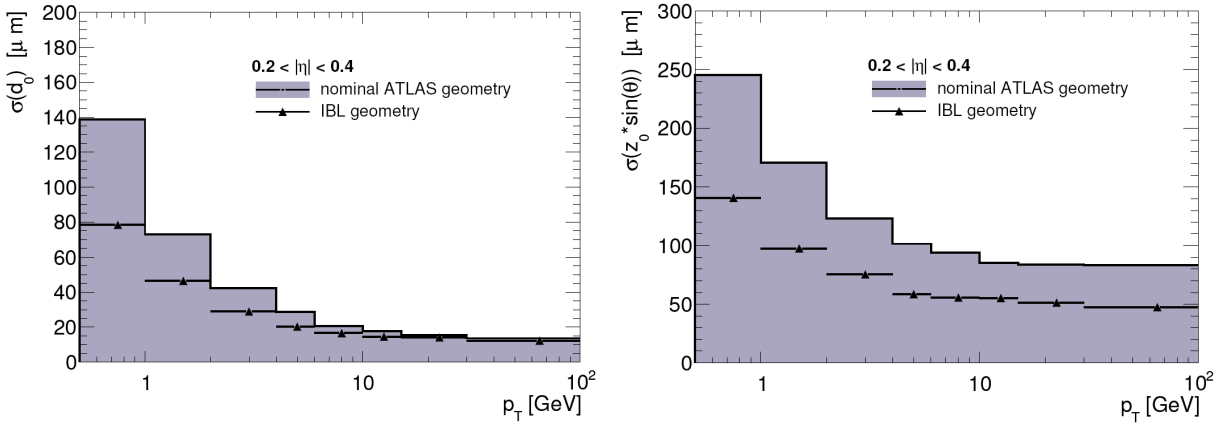


Figure 4.3: Number of reconstructed tracks per event for the current ATLAS inner detector as a function of the average number of pileup interactions. The results are shown for different track selections for track candidates with $p_T > 1$ GeV and $\eta < 1.0$ accepted by the pattern recognition [8].

motivating the main physics performance improvements with IBL during Phase-I are presented here. Figure 4.3 demonstrates that with the current ID layout in high luminosity pile-up, a minimum number of ≥ 9 measured space points (clusters) in the silicon layers of the ID and simultaneously no missing cluster in the pixel layers must be requested in the pattern recognition algorithm. This cut is called tight

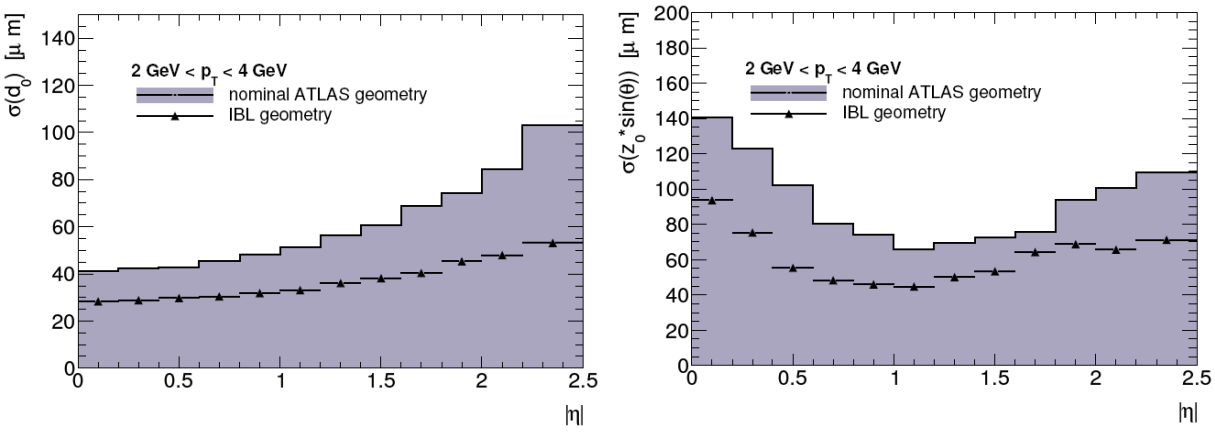


(a) (b)

Figure 4.4: Impact parameter resolution as a function of p_T for tracks in $t\bar{t}$ events without pile-up [8]. The impact parameter resolution $\sigma(d_0)$ in the transverse plane (a) and in z-direction $\sigma(z_0 \cdot \sin(\theta))$ (b) are compared for the ID layout with and without IBL.

selection. With the nominal selection of ≥ 7 clusters the number of fake tracks increases drastically in the high luminosity pile-up scenario.
As derived in chapter 3.2, a first detector layer with small radius and fine pitch is especially beneficial for low momentum tracks. This is shown in figure 4.4a, which compares the impact parameter resolution with and without IBL in the transverse plane in slices of $0.2 < |\eta| < 0.4$ for tracks in $t\bar{t}$ events without pile-up. The impact parameter resolution improves significantly for low p_T tracks, while for

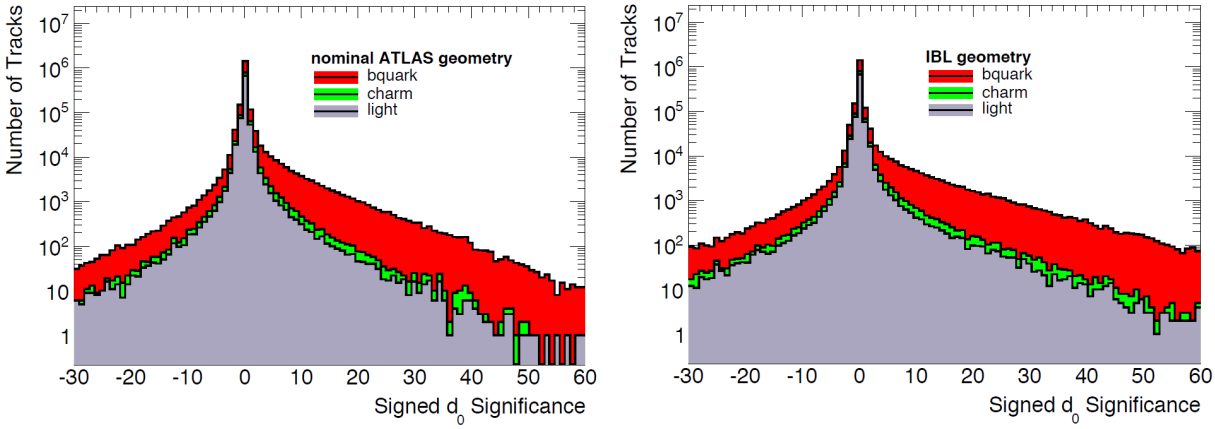
high p_T tracks the improvement is negligible. This changes considering the longitudinal impact parameter resolution ($z_0 \cdot \sin(\theta)$), which is shown in figure 4.4b. The constant improvement of the $z_0 \cdot \sin(\theta)$



(a) (b)

Figure 4.5: Impact parameter resolution as a function of η for tracks in $t\bar{t}$ events without pile-up [8]. The impact parameter resolution $\sigma(d_0)$ in the transverse plane (a) and in z-direction $\sigma(z_0 \cdot \sin(\theta))$ (b) are compared for the ID layout with and without IBL.

resolution results from the smaller pitch of the IBL pixels in z-direction.
Figure 4.5 shows the simulated impact parameter resolution in both planes for tracks with $2\,\text{GeV} < p_T < 4\,\text{GeV}$ as a function of η. The impact parameter resolution improves for all η in both planes. The increase at low η in the z-direction is caused by the increased cluster size due to the Lorentz angle [35]. The vertex resolution without pile-up improves from 15 µm without IBL to 11 µm with IBL in the x-

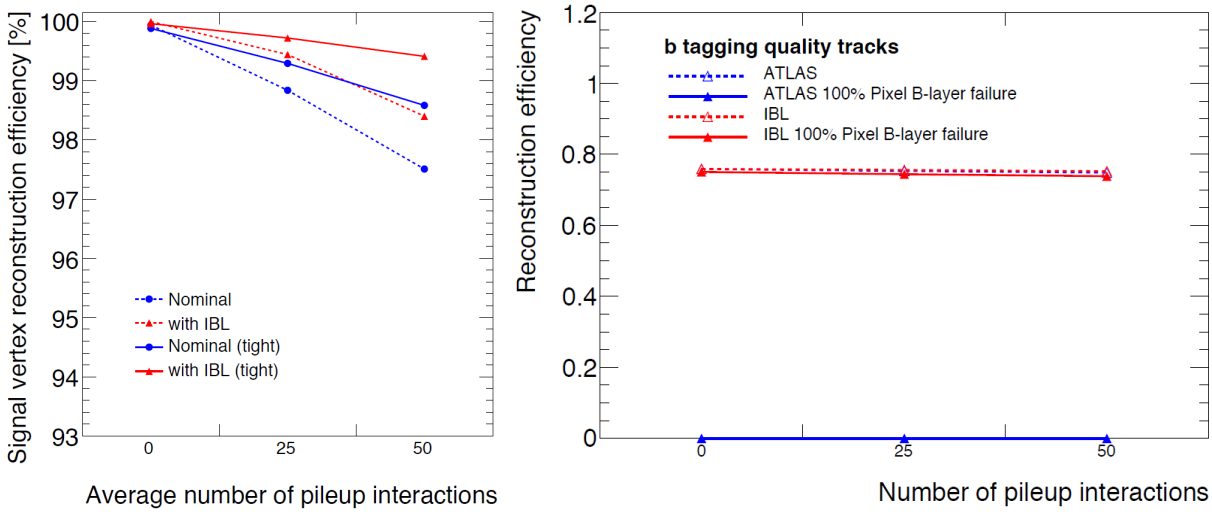


(a) (b)

Figure 4.6: Transverse impact parameter significance distributions for b, c and *light* quark jets from $t\bar{t}$ events without pile-up [8]. The distribution with the nominal ATLAS ID layout is shown in (a) and with the ID layout including IBL is shown in (b).

and y-direction and from 34 µm to 24 µm in the z-direction [8].
The simulations show no significant improvement of the relative momentum resolution. This is expec-

ted recalling equation (3.6) ($dp_T \propto 1/L^2$), because the total track length in the ID does not increase significantly with the additional layer of the IBL.
The b-tagging performance is mainly influenced by the impact parameter resolution. Therefore, a significant gain in the b-tagging performance is expected. A measure for the b-tagging performance is the impact parameter significance. It is defined in the transverse plain by $d_0/\sigma(d_0)$. Additionally, the displacement direction of the b-decay and the assigned jet direction should be correlated. Thus the impact parameter significance is signed positive, if the direction of displacement and the jet coincide, and is signed negative otherwise. The signed impact parameter significance is compared in figure 4.6 for the transverse plane. A clear excess at high impact parameter significance in the distribution with the IBL is visible, which demonstrates the improved b-tagging capability. A similar excess is observed in the z-direction (see [8]).
Two scenarios simulating the effect of the IBL on the ATLAS ID performance with Phase-I luminosity pile-up have been studied in detail. These are the improvement with a full functional pixel detector and



(a) (b)

Figure 4.7: Vertex reconstruction efficiencies in $t\bar{t}$ events with pile-up in two scenarios: The vertex reconstruction efficiency of the ID with a fully functional pixel system with and without IBL for nominal and tight selection in the pattern recognition (a) [8], and the comparison of the track reconstruction efficiency with and without full B-Layer failure for both layouts (b) [8].

the recovery potential of the IBL in case of B-Layer failures in the current pixel system. As shown in figure 4.7a, the vertex reconstruction inefficiency is about halved at Phase-I luminosity with IBL using the nominal as well as the tight selection. This is a consequence of the improved vertex resolution with IBL.
Figure 4.7b demonstrates, that the ID without IBL will basically loose the reconstruction efficiency completely in case of a catastrophal B-Layer failure in the existing pixel system. The IBL will recover the full reconstruction efficiency of b-tagging quality tracks in this scenario.

4.3 Module concepts

The IBL uses two different sensor layouts. All modules use the FE-I4B readout chips. The modules need to fulfill a number of requirements that influence the sensor design. The geometrical inefficiency must be below 2.2%, which translates into an inactive edge in z-direction for double chip modules of less than 450 µm and and less than 225 µm for single chip modules. The hit efficiency of the sensitive area after a fluence of 5×10^{15} $n_{eq}cm^{-2}$ must exceed 97% at a maximum bias voltage of 1 kV. The maximally allowed power consumption of the sensor, at the operation temperature of −15 °C, must be below 200 mW cm^{-2}. This specification is driven by the capability of the cooling system. All these requirements have been extensively tested in the laboratory and in test beams by the ATLAS IBL collaboration and both sensor layouts fulfill the specifications equally well [36]. Selected results will be shown in chapter 6.2. While the planar silicon sensor technology is well established and has a high production yield, the IBL is the first detector using the 3D silicon sensor technology.

4.3.1 IBL planar silicon pixel sensor

All planar modules use a single planar silicon pixel sensor (PPS) produced by CiS[1], that is connected to two FE-I4B readout chips. The planar modules are also called double chip (DC) modules. The sensor wafer material is n-doped DOFZ[2] silicon with a resistivity of 2 to 5 kΩ cm^{-1}. The production wafers are 200 µm thick and have a diameter of four inches. Each wafer holds four IBL double chip sensors and several additional test structures. The sensor layout is similar to an ATLAS pixel sensor with a pixel size that was reduced to 250 µm × 50 µm to match the footprint of the FE-I4B readout chips. The readout electrodes are n^+-doped implants separated by modulated p-spray and a single p^+-doped high voltage pad at the back side. The pixels in the central double column are enlarged to 450 µm × 50 µm to accommodate the region between the two FE-I4B chips. An additional bias-grid is implemented to allow full quality control of the sensor before flip-chip connection to the readout chips. This bias-grid consists of metal lines that provide the possibility to connect the bias dot to ground. The bias dot is a small, separated n^+-doped implant inside the n^+-doped readout electrodes. If the readout electrode is floating, the bias dot connects the readout electrode via the punch through effect [37] to ground. The pixel implants and the bias dots are shown in figure 4.8. Additionally, the 13 guard rings are visible

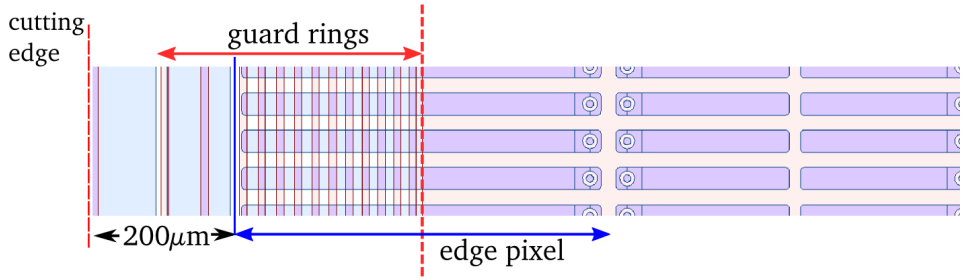


Figure 4.8: Design of the implants of an IBL planar sensor [36]. The edge region is shown, with the n^+-implants in purple. The 13 p^+-doped guard rings are displayed in blue and are located on the opposite side of the pixel implants. In the IBL slim edge design they are shifted over the enlarged edge pixels.

in figure 4.8 that are used to generate a well controlled potential drop from the high voltage pad to the

[1] CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH, Konrad-Zuse-Straße 14, 99099 Erfurt, Germany.
[2] Diffusion Oxygenated Float Zone. The oxygen is diffused into the thinned wafer for 24 hours at 1150 °C before the implantation process.

sensor edge. A new design feature was developed for IBL to achieve the slim edge specification. The outermost pixels are extended to 500 µm length and the innermost eleven guard rings are placed over the outermost half of the edge pixel implants. This is only possible on n^+-in-n planar sensors, where the guard rings are on the opposite side of the pixel implants, see figure 4.8.

4.3.2 IBL 3D silicon pixel sensor

The 3D silicon sensor technology avoids the structural constraints of planar sensors by a change of the geometrical readout electrode orientation: in general, a small distance between the readout electrode and the biasing electrode increases the signal size after heavy irradiation. Research with very thin planar pixel sensors is ongoing [38], but with reduced sensor thickness, the number of initially generated electron-hole pairs in the sensor is reduced. The 3D sensor technology avoids this problem by decoupling the direction of charge generation from the direction of charge drift. Pillar shaped electrodes penetrating the sensor bulk orthogonal to the surface are used in this technology. The distance between the readout electrodes is therefore independent of the sensor thickness and very radiation hard sensors can be produced. The price to pay is a more difficult production and thus a reduced yield. Therefore, the 3D modules consist of a sensor connected to a single FE-I4 readout chip and are called single chip (SC) modules.
Two different manufacturers process the 3D sensors for IBL: CNM[3] and FBK[4]. Both are supplied with four inch (230 ± 20) µm thick FZ[5] wafers produced at TOPSIL[6]. The wafers consist of p-type high resistivity silicon as usually used for planar n-in-p sensor productions. The process at CNM and FBK is mainly similar. Both use the double sided etching technique called Bosch-process [39] that allows to edge narrow pillars through the silicon bulk. A subsequent high temperature thermal diffusion doping process forms the n^+ and p^+ electrodes. Both sensor types connect two n^+-doped pillars as readout electrodes to the bump pad (2E electrode configuration). The electrodes of the FBK process fully penetrate

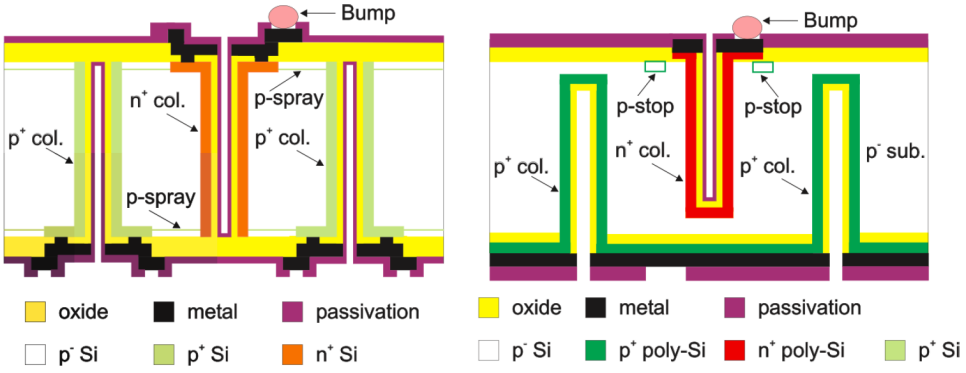


Figure 4.9: Cross sections of the 3D pixel sensors fabricated at FBK (a) and CNM (b) [36].

the silicon bulk, while the electrodes processed at CNM stop a short distance from the surface of the

[3] Centro Nacional de Microelectronica (CNM-IMB-CSIC), Campus Universidad Autonoma de Barcelona, 08193 Bellaterra (Barcelona), Spain.
[4] Fondazione Bruno Kessler (FBK), Via Sommarive 18, 38123 Povo di Trento, Italy.
[5] Float Zone
[6] Topsil Semiconductor Materials A/S, Linderupvej 4, DK-3600 Frederikssund, Denmark

opposite side. Figure 4.9 compares the cross sections of the two 3D sensor flavors.
As visible in the picture, the FBK sensors use p-spray technology to isolate the electrodes on both sides, while the electrodes of the CNM sensors are isolated by p-stop implants on the front side only. To control the potential drop towards the cut line, the CNM sensors use a n^+-doped grounded guard ring and fences at the high voltage potential. The FBK sensors use several rows of ohmic columns for this task.

4.3.3 The FE-I4 readout chip

The current pixel detector [40] readout chip (FE-I3) is not capable of coping with the expected hit occupancies and radiation doses [41], so a completely new readout chip architecture was designed [42]. This chip (FE-I4) is built in a 130 nm CMOS feature size technology using thin gate oxide transistors to increase the radiation hardness. The large chip (20.2 mm x 18.8 mm) has an active area holding 80

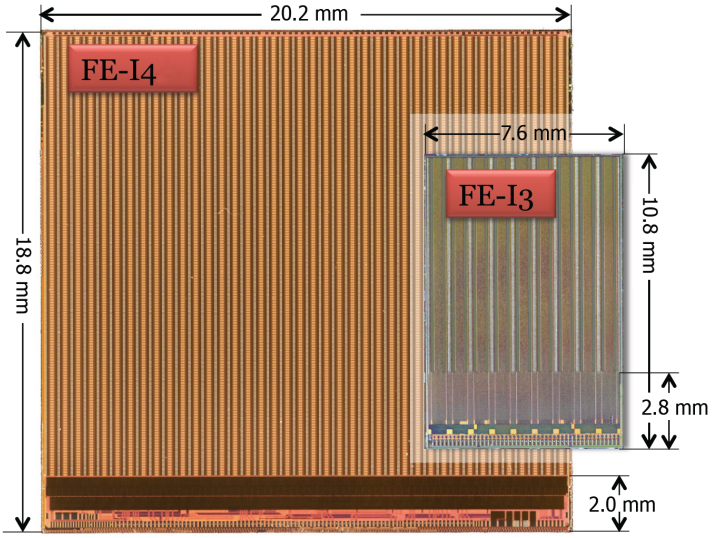


Figure 4.10: Picture of an FE-I4 chip and a to-scale picture of an FE-I3 chip [36]. The pixel matrix and the approximately 2 mm high periphery can be seen.

columns with 336 pixels each and an approximately 2 mm high periphery (see figure 4.10), which results in an active over inactive area fraction of about 90%.
The pixels have a size of 250 µm × 50 µm holding an analog and a digital circuitry. The analog part is a two stage amplifier plus discriminator design shown in figure 4.11. The preamplifier (Preamp) and second stage amplifier (Amp2) are AC coupled, and the feedback current of both amplifiers can be adjusted. These adjustments are implemented globally (V_{fb} and V_{fb2}), so all pixels of the matrix are affected simultaneously. For the preamplifier feedback an additional current adjustment using the 4-bit FDAC allows the fine tuning of the TOT response for each pixel individually. The output of the Amp2 is compared to a threshold voltage (V_{th}) by the discriminator. The threshold voltage can again be adjusted globally as well as individually for each pixel, using the 5 bit TDAC setting.
Additionally, each pixel contains test hit injection circuitries. Analog test signals are injected using a voltage step defined by the calibration voltage (V_{cal}) and two test charge injection capacitances ($C_{inj1/2}$), which can be selected independently. The injected charge is given by

$$Q\,[e] = C_{inj}\,[\mathrm{F}] \cdot V_{cal}\,[\mathrm{V}] \cdot \frac{1}{e\,[\mathrm{C}]}, \tag{4.1}$$

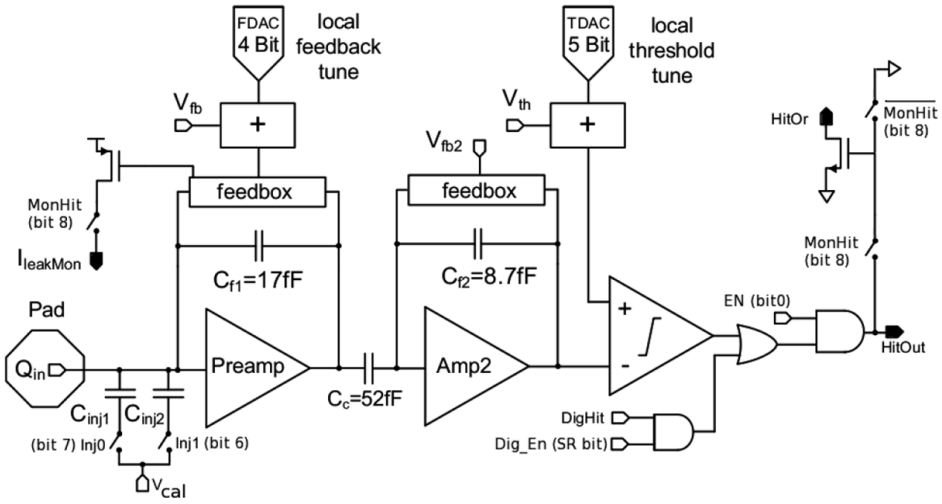


Figure 4.11: Schematic view of the analog pixel cell [36]. A detailed explanation of the functionality is given in the text.

with e being the elementary charge and

$$V_{cal}\,[\mathrm{V}] = a\,[\mathrm{V}] + b\,[\mathrm{V/DAC}] \cdot PulserDAC\,[\mathrm{DAC}]. \tag{4.2}$$

a denominates the offset and b the slope of the linear transfer function. Digital test hits are injected to an OR element at the output of the discriminator. The output of the analog readout chain of each pixel can be disabled using an AND connected to the discriminator output and the enable bit (EN) on each pixel. The output (HitOut) can be connected to the HitOR bus, which is routed to each pixel of the matrix using a logical OR and a pull.down transistor, and thus is low in case of any discriminator being above threshold. The HitOR signal at the wire bond pad is active high due to an additional inverter in the periphery of the chip. This signal is used for test purposes and enables the selectable self trigger operation of the chip. Additionally, when the MonHit bit is set, the bus $I_{leakMon}$ can be used to measure the current that is compensated by the leakage current compensation logic implemented in the feedback current circuitry of the preamplifier.
Four pixels share a common digital logic cell for further hit processing, which mirrors the clustered nature of real hits. The FE-I4 digital hit processing is based on the 4-pixel digital region. Detailed studies show that the transfer of the hit information to the chip periphery is the main inefficiency source at the expected IBL hit occupancy [41]. The FE-I4 hit processing architecture therefore stores the hits in the pixel array close to the analog readout chain and the hits are processed only if a trigger signal is received. Detailed information on this architecture can be found in [43]. The 4-pixel digital region is sketched in figure 4.12. Four pixels share a set of five latency counters, while each pixel holds his own set of five TOT counters. A hit in one of the analog pixel cells allocates and starts the first unallocated latency counter to count down from the programmed latency (in units of 25 ns). The charge information belonging to this specific time stamp is stored in the buffers for all pixels connected to the 4-pixel digital region. An incoming Level-1 trigger in coincidence with the latency value of zero initiates the transfer of the hit data to the end of chip logic, and deallocates the latency counters and buffers. If no corresponding Level-1 trigger arrives, the hit information is deleted and the counter and buffers are deallocated as well. A full scale prototype chip implementing this sophisticated architecture (FE-I4A) is available since fall 2010 and has been extensively characterized in this work. The FE-I4A contains several test structures

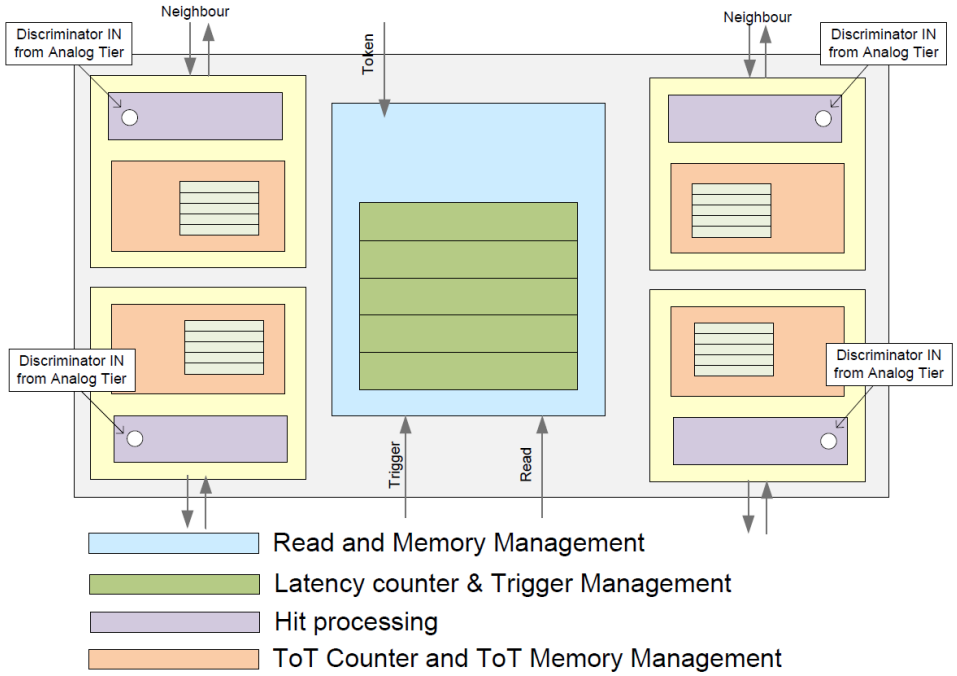


Figure 4.12: Block diagram of the digital 4-pixel region [43]. The complex functionality of this logic is explained in the text.

and different pixel prototype flavors. In the FE-I4A chip different variants of the pixel design are used in some columns in order to measure performance options. These variants include different types of configuration memory cells, that must be SEU tolerant, different types of feedback capacitors, and different discriminator designs. Based on the test results of the FE-I4A, the production version readout chip (FE-I4B) has been produced. As the FE-I4B is the final chip for the IBL, all pixels are identical, using the variant with the best SEU performance, a metal-metal feedback capacitor, and a conservative discriminator design. Chapter 5 presents the major characteristics of the FE-I4 readout ICs tested in this work. The motivations and details of the implemented changes from FE-I4A to FE-I4B are explained also there.

Each of the readout chips holds two on-chip LDO (Low Drop Out) regulators [44, 45] to generate the analog and digital supply voltages. These are linear regulators, which keep a constant output voltage independently of the input voltage and the load current. A minimum difference between the input voltage and the output voltage (dropout voltage) is used to achieve a high power efficiency. The on-chip LDOs are operated in partial shunt mode. This means that they are operated as usual LDO as long as the current consumption is above an adjustable minimum input current. If below, an additional current is shunted to ground by the regulators. This operation mode does not increase the power consumption of the Front-End chip as long as its current consumption in working conditions is above the shunt current. The advantage of this mode is the reduction of the transients in comparison to the pure LDO mode in case of load current fluctuations. This will happen in case of configuration of the Front-End chips or accidental configuration loss. The reference voltages needed for the operation of the two LDOs are generated on-chip.

The FE-I4 chip contains a master current reference, nominally 2 µA, from which all internal biases and Digital Analog Converters (DAC) are fed [46]. This reference was present in FE-I4A and carried over to FE-I4B. However, this reference is designed for 1.5 V rail operation and therefore must be powered

from the output of a voltage regulator. This presents a startup challenge in the case one wishes to use this reference to control the output of the built-in voltage regulators. A start-up circuit is introduced in FE-I4B to make this possible. Additionally, new band-gap voltage reference circuits [47] are added in FE-I4B for use as optional voltage regulator references. These circuits are designed for 2.5 V rail operation and therefore can be powered from the same unregulated voltage feeding the internal regulators.
The left most box in figure 4.13 shows simplified schematics of the on-chip LDOs. The LDO compares the reference voltage sourced from a wire bond pad to 0.5 times the output voltage and adjusts the output voltage accordingly. Therefore, the potential connected to the reference voltage pad should be 0.5 times the required output voltage. There are two independent on-chip reference voltage generation circuitries implemented for each of the two LDOs. One is the above mentioned band-gap reference with fixed output voltage, the other converts the global reference current of 2 µA into a voltage using a resistor in parallel to a variable current sink. The sinked current can be adjusted using an on-chip DAC and therefore this voltage reference is called tunable voltage reference. For flexibility one can wire bond the input to the LDOs reference voltage to the band-gap based reference voltage output or to the tunable reference voltage. The design of both references is compatible with parallel connection. Detailed studies of the LDO and both reference voltage options are presented in chapter 5.5. Based on these results the reference voltage connection scheme of the IBL readout chips is chosen. The digital regulator uses the tunable reference voltage only and for the analog regulator the tunable reference voltage and the band-gap reference output are tied together for reasons that will be underlined later (see section 5.5).

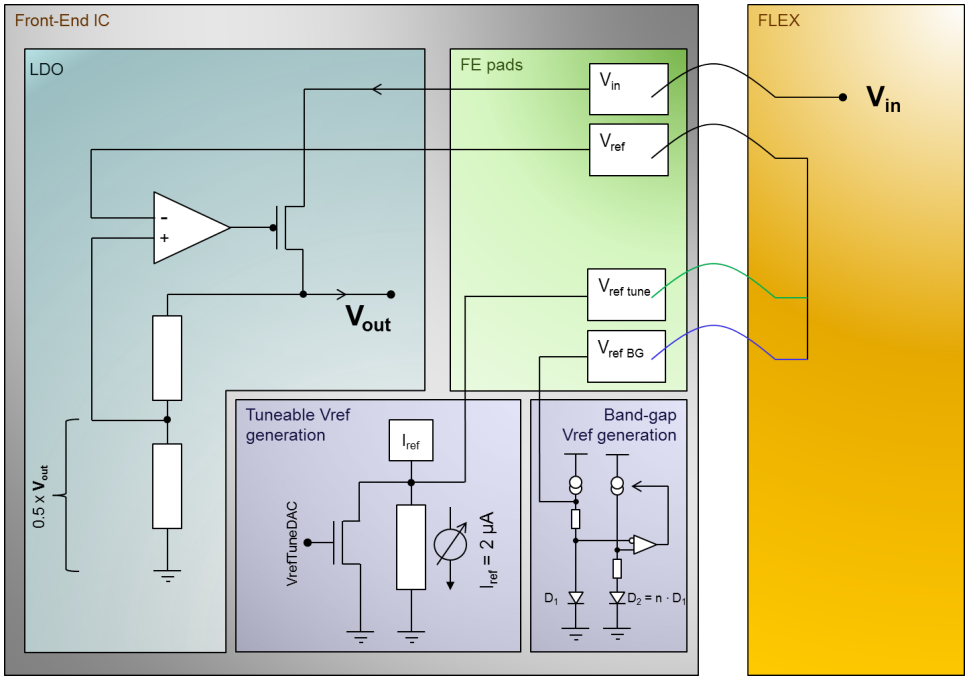
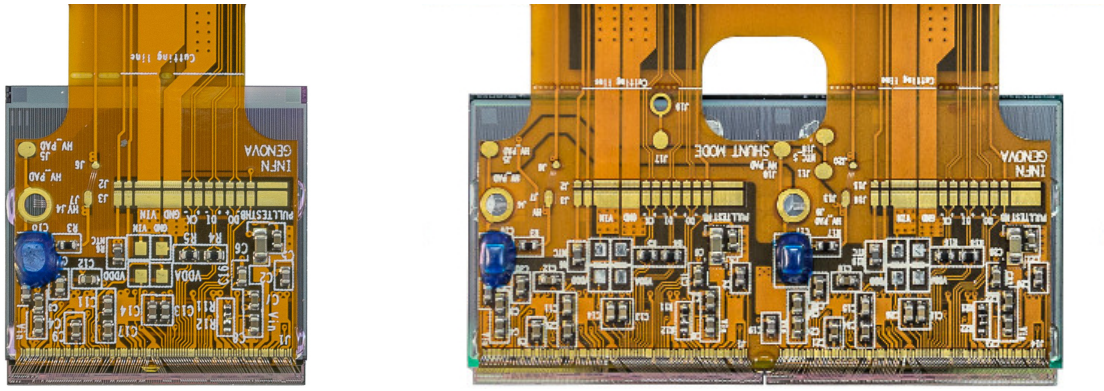


Figure 4.13: Simplified schematics of the on-chip low-dropout regulators and reference voltage connection options.

4.3.4 Flip-chip and module dressing

Thin readout chips are necessary for modules with a low material budget, because the readout chip bulk is passive material with a short radiation length. The thinning and bump-bonding of the IBL

modules is done at IZM[7]. In this process, the IBL readout chips are thinned to a thickness of 150 µm. The subsequent flip-chip process using SnAg solder bumps requires a temperature of 260 °C during the reflow process. Thin readout chips bend up, resulting in open bumps at the edges of the module. The bend is proportionally to the cubic inverse diagonal of the chip [48]. An additional process step, that uses a glass carrier wafer glued to the backside of the readout chips, was developed by IZM, that allows safe bump-bonding of FE-I4 size readout electronics down to a thickness of 90 µm [48]. The glass carrier is glued using a polyimide glue, that can be dissolved by laser exposure. After the laser exposure the glass carrier can be detached from the assembly and the sensor plus readout chip assembly is ready to be ”dressed” to a complete module.
Two laboratories in Bonn and Genoa ”dress” the assemblies delivered by IZM and qualify the IBL modules. The first assembly step is the cleaning and attachment of the module flex. The module flex is a two copper layer flex circuitry of 130 µm thickness. It routes the signals from the wing, that is attached to the stave flex (see chapter 4.4), to the wire bond pads of the readout chip and to the HV pad of the sensor. Additionally, it is loaded with passive SMD[8] components such as filter capacitances and termination resistors for the LVDS links. The module flex is glued to the sensor backside using a tape strip (PPI RD-577F) under the wire bond pads and dots of epoxy glue (UHU EF 300) at several locations. A weight is applied while curing the glue. The last assembly step is the electrical connection of the readout chip and the sensor to the module flex using 25 µm aluminum wire bond connections. A dressed 3D single chip module and planar double chip module is shown in figure 4.14.



(a) (b)

Figure 4.14: Photo of a dressed IBL single chip module (a) and a double chip module (b). The flex extension called pigtail is present to allow testing of the module prior to the loading of the module on the stave and is cut during the stave loading procedure at the indicated cutting line.

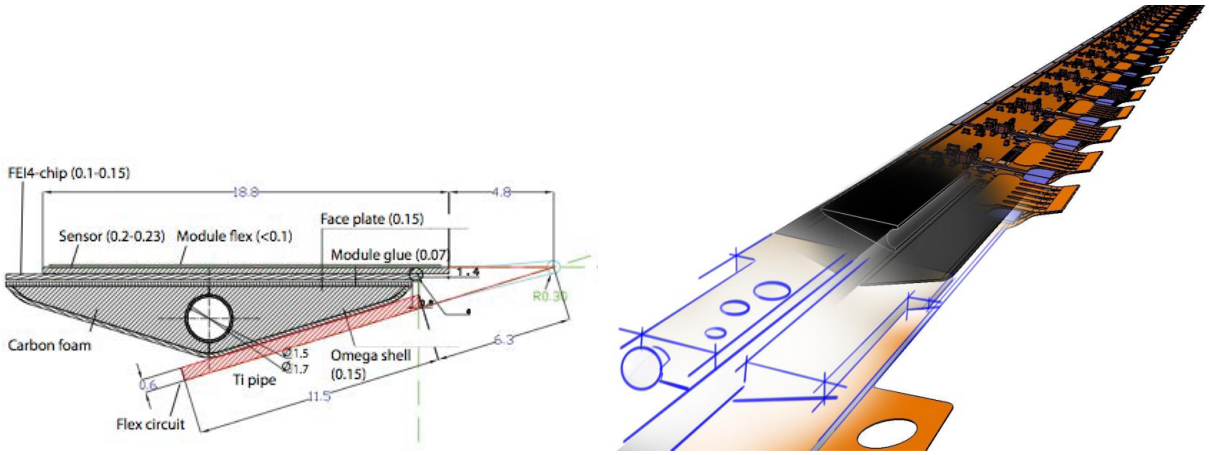
4.4 Stave layout

The IBL modules are mounted on 14 local support and cooling structures (stave) surrounding the beam pipe cylindrically. Each stave is tilted by 14 degrees to allow an overlap of the sensitive area in ϕ and full geometrical efficiency in this direction. The staves are the mechanical and thermal support of the modules and also carry the electrical services for the modules. Twelve double chip planar silicon pixel modules and eight single chip 3D silicon pixel modules are loaded on each IBL stave.

[7] Fraunhofer-Institut für Zuverlässigkeit und Mikrointegration, Gustav-Meyer-allee 25, 13355 Berlin, Germany.
[8] Surface Mounted Device

Mechanical stave design

An IBL stave is a 724 mm long object and consists of three major mechanical parts. The main structure is an Ω-shaped carbon foam that serves as path for the heat generated in the modules to the cooling fluid. The cooling is realized using CO_2 bi-phase cooling in a titanium cooling pipe with 1.7 mm outer radius. The maximum design pressure is 100 bar and all cooling pipes are qualified to withstand a pressure of 150 bar. The cooling pipe is integrated in the carbon foam to allow maximum thermal contact. A 150 µm thick layer of quasi-isotropic carbon fiber laminate (omega) is glued on the back side of the stave to provide mechanical stiffness. A cross section of the staves and a 3D drawing of a loaded stave are drawn in figure 4.15. The modules are glued with the readout chip backside on the base of the stave.



(a) (b)

Figure 4.15: Cross section of an IBL stave [8] (a) and a 3D drawing of the IBL stave loaded with electrical support and modules (b).

The electrical services (stave flex) routing the power and signal lines are glued on the opposite side of the stave (in red in figure 4.15a). For each module a bent extension wing provides the connection to the module flex, which is glued on the sensor, around the stave corner.

Electrical services

The IBL staves are split electrically into two half staves. Each half stave holds six double chip modules. The double chip modules are mounted towards the middle of the stave. Additionally, four single chip modules with either CNM or FBK sensors are mounted at the outside of each half stave.
The stave flex provides the electrical connection of the modules to the end of stave card. It is a mixed multi-layer circuit that holds four copper layers for the signal links and the high voltage line and two additional aluminum layers for the supply voltage and return lines. Figure 4.16 shows the schematic

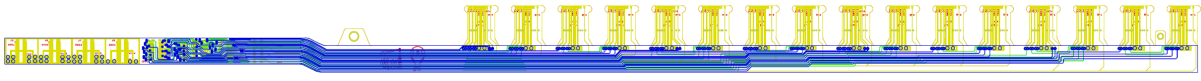


Figure 4.16: Longitudinal view of the multi-layer stave flex for a half stave. The other side stave flex is a mirrored design. On the left side the PP0 connectors are located and on the right side the wings to be bent and connected to the module flex is visible.

longitudinal view of the stave flex.
The modularity of the IBL is complex. Each front end chip is read out independently using a dedicated data out link with a bandwidth of 160 MBit/s. Two neighboring readout chips build one configuration group and share one clock link and one command link. The Detector Control System (DCS), that provides the supply voltages of the readout chips and the high voltage for the sensors as well as the temperature readout, has a 4-chip modularity, which means that two double chip modules or four single chip modules are connected to one DCS channel. Thus, four FE-I4B chips electrically build an IBL power group and connect to one IBL low voltage power supply channel regardless of the module type. On the module flex, the low voltage lines are routed in parallel to the two on-chip LDOs. The sensor

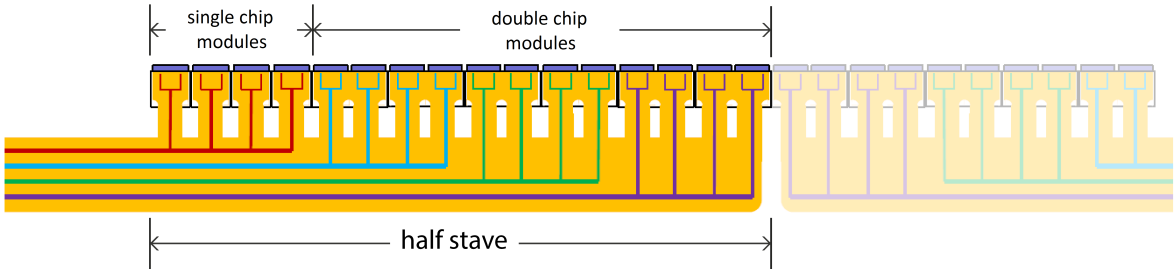


Figure 4.17: Overview of the module position and low voltage connection of an IBL half stave.

high voltage is connected with the similar modularity of four readout chips, so at each end of the stave four single chip modules from the same 3D silicon sensor vendor are always grouped together, which is important because of the different breakdown voltages which can be experienced from one vendor to the other (see chapter 6.1.1). An overview of the half stave and of the IBL power groups is shown in figure 4.17.

Chapter 5

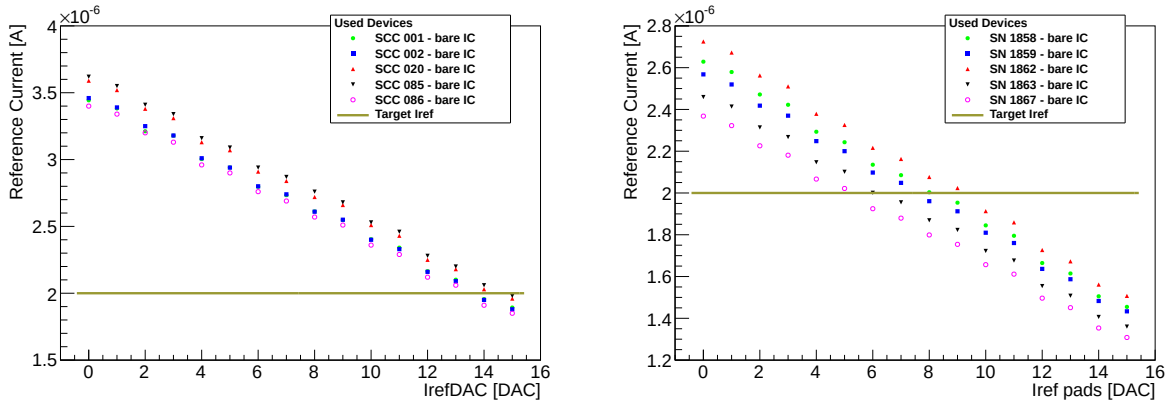
Characterization of the IBL pixel chip FE-I4

Both FE-I4 readout chip flavors introduced in chapter 4.3.3 are intensively characterized in this thesis. The analog and digital blocks are tested and results about their characterization are shown in this section. Some of these results motivated the changes that are implemented in the transition from the prototype chip FE-I4A to the production chip of the IBL, the FE-I4B. Studies concerning the on-chip LDOs presented in chapter 5.5 mainly influence the selected powering scheme of the IBL, as described in chapter 4.3.3.
The test system that is used for all characterizations of FE-I4 readout chips and FE-I4 based modules is called USBpix. USBpix is a compact and modular system including hardware as well as software. It is based on a custom made FPGA[1] card that provides also the USB[2] interface to the computer. This board can be connected to a set of adapter cards for the connection to the readout chip and module. The high level software contains the readout chip configuration, scan routines, and data analysis functionalities. This software communicates with the hardware layer via an interface library, which translates the generic protocol of the high level software to the readout chip specific protocol. A detailed description of the USBpix system can be found in [49]. The FPGA firmware, the interface library, and an extensive library of scan routines have been developed in this thesis to test all features in the FE-I4 chip that are necessary for successful operation in the ATLAS experiment. These routines are also used during the IBL production wafer probing and generate approximately 18 000 individually measured quantities per wafer that are automatically analyzed. Cuts are then applied on the values automatically recorded to select readout chips with a performance suitable to be used in the IBL, and to reject those that fail the selection criteria. This section starts with a description and the result of the tests of a few blocks included in the Front-End's periphery. Afterwards the results of the performance characterization of the pixel matrix and of several digital functionalities are presented and the chapter closes with a sample of results from the production wafer probing.

5.1 Reference current

As explained in chapter 4.3.3, the FE-I4 generates a current used as reference for all digital to analog converters, that are used to generate voltages and currents needed in multiple places in the chip. This reference current can be measured and needs to be adjusted to the design value of 2 µA using a dedicated register in the global memory of the chip. The reference current setting is characterized on several bare FE-I4A chips on single chip support cards (SCC) and on every FE-I4B chip at wafer level. The result for both chip flavors is plotted in figure 5.1.
For all tested FE-I4A chips the design reference current of 2 µA is within the dynamic DAC range, but is on the edge of the trimming range (figure 5.1a). The DAC range is adjusted in FE-I4B to achieve a better

[1] Field Programmable Gate Array.
[2] Universal Serial Bus.



(a) (b)

Figure 5.1: Measured reference current as a function of the corresponding setting for FE-I4A (a) and FE-I4B (b). The target reference current of 2 µA is marked for both chip flavors. The DAC dynamic range is adjusted and the register for the DAC is replaced by wire bond pads in the FE-I4B design. No unique Serial Number (SN) is assigned to the FE-I4A chips, the number of the support card (Single Chip Card, SCC) is used instead to identify the chips.

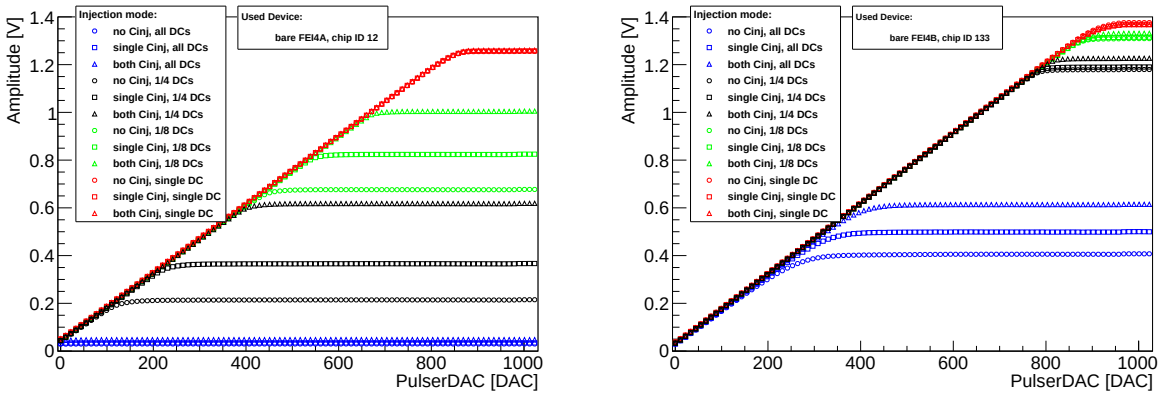
centering of this range. Additionally, the corresponding DAC setting is removed from the global register and routed to wire bond pads to achieve a SEU hard reference current setting. Figure 5.1b proves the effectiveness of the adjustment.

5.2 Test charge injection circuitry

The test charge injection circuit is used for all measurements of the analog performance. Its charge calibration is a very important measurement, which is performed on each individual readout chip during the IBL production. This calibration relates to two characterizations: the pulser circuitry characterization and the injection capacitance measurement.

5.2.1 Pulser circuit characterization

The voltage V_{cal}, which defines the voltage step over the injection capacitance, is measured using an external voltmeter. The resulting voltage as a function of the corresponding DAC setting (PulserDAC) for both FE-I4 flavors is shown in figure 5.2.
The test charge injection circuitry has poor performance in FE-I4A as can be seen in figure 5.2a. The achievable voltage step is limited. It ranges from a reduced maximum step when a single column is enabled to complete loss of function with all columns enabled. Figure 5.2b demonstrates the good performance of this block in FE-I4B. The only significant saturation observed in FE-I4B happens when injecting into all 26880 pixels at the same time. It is also possible to inject in every eighth or every fourth double column and into single double columns. All these other modes allow a voltage step across the injection capacitors well above 1.1 V with good linearity. The saturation that is still visible in the single DC mode is the expected limitation of the voltage step due to the supply voltage of the pulser circuit.
Deviations from linearity can be shown by the integrated nonlinearity (INL) which is defined as the



(a) (b)

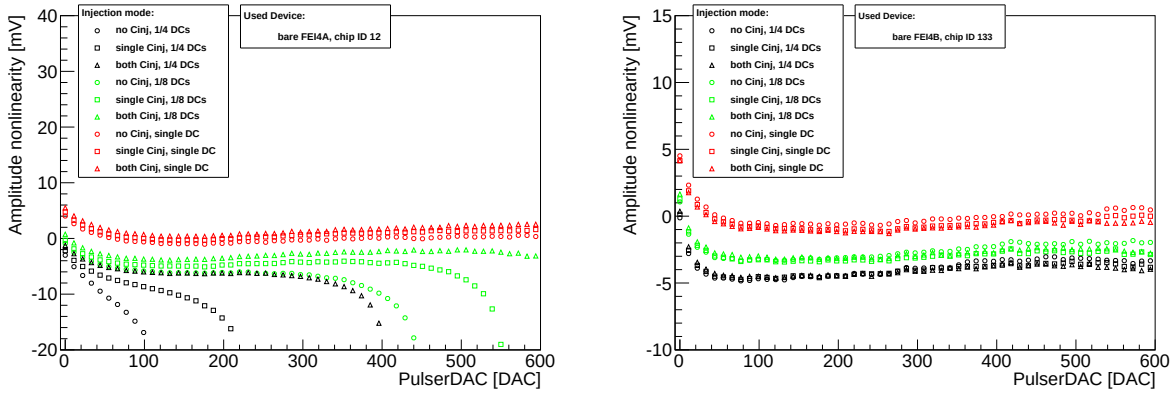
Figure 5.2: Test charge injection circuitry output pulse amplitude as a function of the corresponding 4-bit DAC setting for FE-I4A (a) and FE-I4B (b) in all injection modes.

maximum distance of the measured value from the ideal one for an expected linear dependence. The ideal value is commonly derived from a linear function fitted to the measured data. Here, the ideal amplitude is obtained from a fit to the result in single DC injection mode with both injection capacitors enabled, because this is the mode which is expected to have the best performance (figure 5.2). The difference of the measured amplitude to the ideal amplitude as a function of the corresponding DAC setting is presented in figure 5.3 for both FE-I4 flavors. Only PulserDAC values below 600 are shown to exclude the dominance of the saturation in this measurement. It has to be said that in most measurements that are sensitive to the charge calibration of the injection circuitry, such as threshold scans, PulserDAC values above 600 are indeed not used.

Three sources of nonlinearity can be identified considering the schematics of the pulser circuitry sketched in figure 5.4. In figure 5.3a the saturation for high PulserDAC values of FE-I4A when injecting in more double columns at the same time and with less injection capacitances enabled results in large differences of the measured amplitude from the ideal amplitude. This saturation is caused by leakage current in the transmission gates which select the injection capacitors. The more double columns are used for injection and the more injection capacitors are switched off (the more transmission gates are opened), the more leakage current is seen by the pulser. This leakage current limits the maximum output voltage of the pulser resulting in the saturation observed. Another type of transmission gates which exhibits less leakage current is used in FE-I4B, and thus the saturation appears at much higher PulserDAC settings (see figure 5.3b).

This source of leakage current is also responsible for the second nonlinearity source. The leakage current flows through a series resistor at the output of the pulser. Thus, a voltage drop in this resistor occurs, which again depends on the number of double columns enabled for injection and the settings of the transmission gates. This results in an offset for the whole PulserDAC range which depends on the double column injection mode.

In both chip flavors a similar third nonlinearity is observed. The effect is more obvious in figure 5.3b due to the reduced y-axis scale. For very low PulserDAC values, which correspond to very low output voltages, the nonlinearity rises. Two sources are possible. One possibility is a nonlinearity at very low output voltages of the DAC itself, which is used as input to the pulser circuit. Another possibility is a nonlinearity due to operation outside of the linear range of the two operational amplifiers, that are used



(a) (b)

Figure 5.3: Difference between the measured amplitude and the ideal amplitude (obtained from a linear regression to the single DC injection mode) for FE-I4A (a) and FE-I4B (b). The maximum distance from zero in this representation corresponds to the integral nonlinearity (INL).

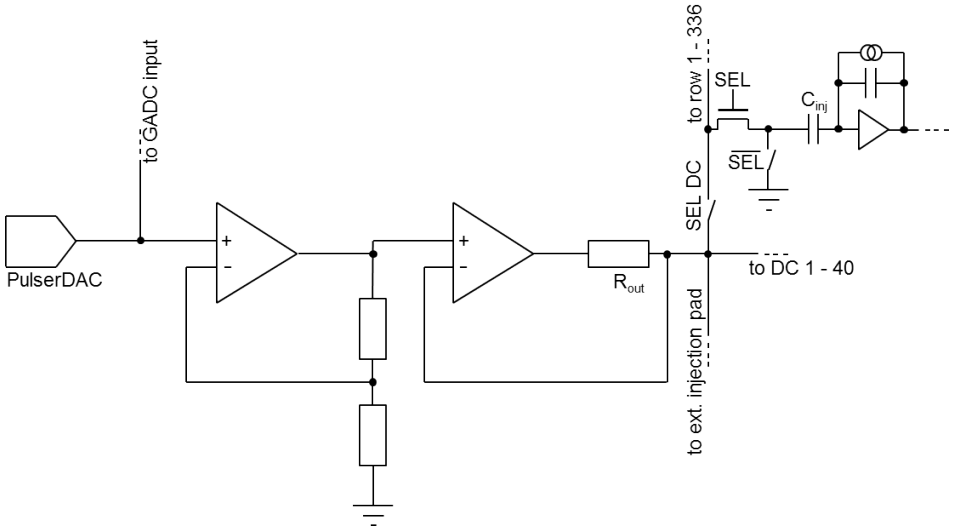
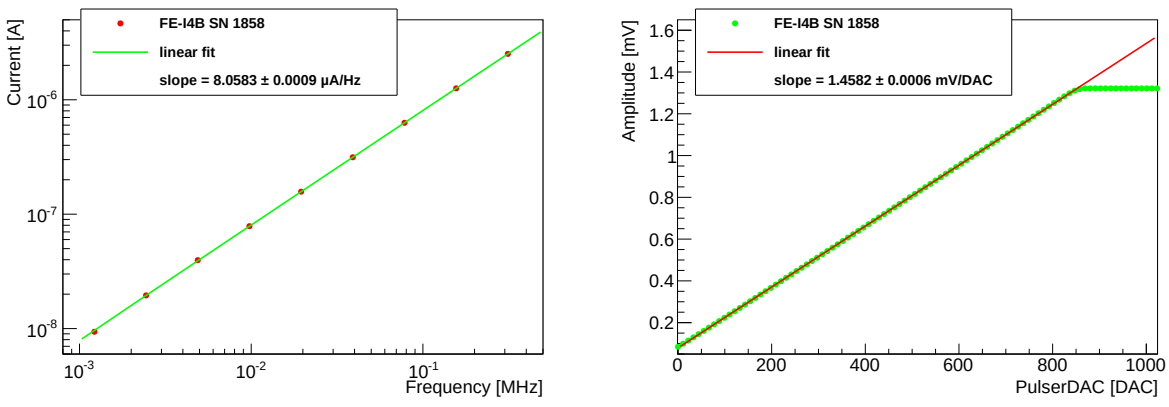


Figure 5.4: Simplified schematics of the pulser circuitry and injection capacitance selection. The pulser output can be overwritten using the external injection pad. The external injection pad is bi-directional and is also used to measure the pulser circuitry output characteristics.

in series in the pulser circuit (see figure 5.4), when generating output voltages close to the GND potential. These can not be easily disentangled, because the node between the DAC output and the pulser input is not accessible with external voltmeters. This node is connected as input to the generic on-chip ADC in FE-I4B, which could be used to measure the nonlinearity at this node. But the calibration of the generic ADC is a work in progress at the time of writing.
The absolute maximum difference in this data corresponds to the INL of the pulser circuitry. The INL in FE-I4A is measured below 4.4 mV in the single DC injection mode. The other modes are not used in the USBpix system to achieve the best possible performance in terms of charge calibration. A similar INL of less than 4.7 mV results for the FE-I4B.

5.2.2 Injection capacitance measurement

In the FE-I4A, no circuitry for direct measurement of the test charge injection capacitances is implemented. Simulations predict a capacitance of 5.7 fF if both injection capacitors are used. The injection capacitance can nevertheless be measured using the known charge deposited in the sensor by monoenergetic x-ray sources. A method allowing to measure the injection capacitance without using the TOT information (whose calibration is tuned using the injection capacitance) and the results of its first realization is presented in chapter 6.
A dedicated circuit to measure the average value of representative injection capacitors has been included in FE-I4B. This circuit is not accessible once modules have been assembled. Therefore the test charge injection capacitance must be measured during the wafer level test to achieve a proper charge calibration for each FE-I4B. The needed functionality has been implemented to the USBpix system to perform this measurement. A voltage is applied across an array of 1000 replica injection capacitors in parallel and is switched with variable frequency between input and ground using non-overlapping clocks. The average



(a) (b)

Figure 5.5: Measurements for the charge calibration of FE-I4B with Serial Number (SN) 1885. For the extraction of the injection capacitance a voltage across an array of replica injection capacitances is switched with variable frequency and the average current is measured (a). The calibration of the pulser circuitry is derived from the amplitude of the voltage step over the injection capacitance as a function of the corresponding DAC setting (b).

current is measured, resulting in the linear behavior shown in figure 5.5a.

The test charge injection capacitance is computed from the slope m of the linear regression using

$$C_{inj} = \left(\frac{m}{N} + a\right) \cdot \frac{1}{b}, \tag{5.1}$$

where N is the number of capacitors in parallel, the offset $a = -1360 \pm 1$ and the correction factor $b = 1.081 \pm 0.002$, which follow from the exact implementation of the injection capacitance measurement circuitry. For this particular FE-I4B the resulting injection capacitance is

$$C_{inj} = (6.196 \pm 0.016)\,\text{fC}.$$

Using this result, the charge calibration of the injection circuit can be calculated once the amplitude of the voltage step per DAC step is known (pulser circuit output calibration). This is given by the slope of the pulser output voltage measurement as a function of the corresponding DAC setting, as shown in figure 5.5b. The injected charge Q_{inj} in terms of the number of electrons per DAC step is given by

$$\frac{Q_{inj}}{\text{DAC}} = m \cdot \frac{C_{inj}}{e} \tag{5.2}$$

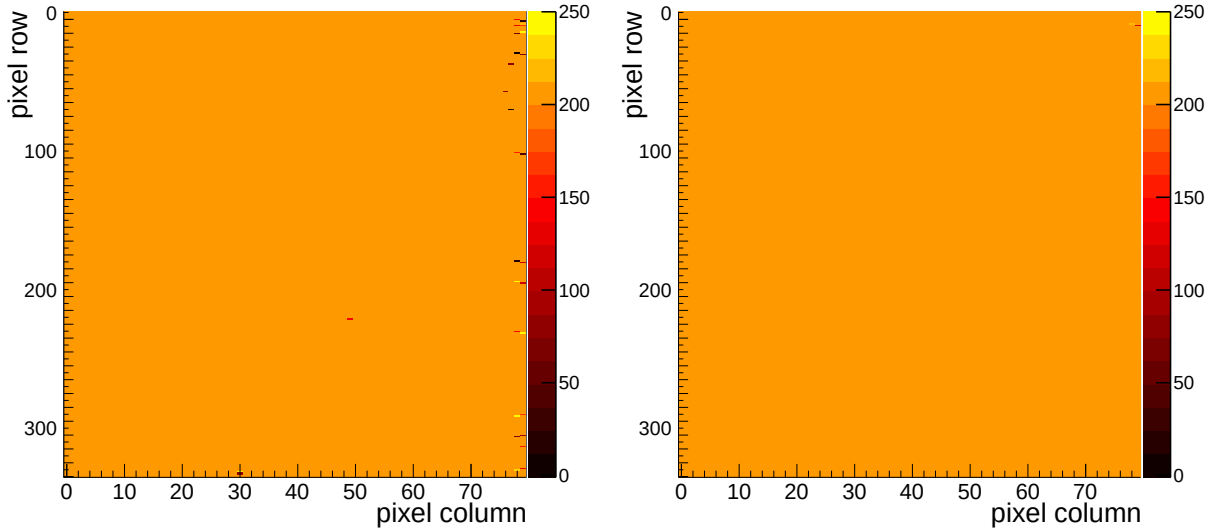
with the slope of the pulser output calibration m. The offset of the pulser output is commonly not taken into account, because the measured offset in this method is dominated by the voltage drop across the resistance of the wire bonds. The offset can be measured for each pixel by threshold measurements using the different injection capacitances, if the ratio between these capacitance values is known. This threshold based offset measurement (not shown here) results in a rather large chip-to-chip spread and therefore an systematical error of 300 e is assumed. Additionally, the integrated nonlinearity of the pulser circuitry results is a systematical error of 182 e
The charge calibration of the injection circuitry of the FE-I4B with SN 1885 that is shown here results in

$$\frac{Q_{inj}}{\text{DAC}} = (56.40 \pm 0.15)\,\frac{1}{\text{DAC}} + (300 \pm 300 \pm 182)\ e.$$

5.3 Performance of the pixel matrix

Most of the automated standard test routines used to measure the performance of the pixel matrix, such as threshold scans and tuning algorithms, are inherited in the USBpix test system from the existing pixel detector calibration routines. The command flow needed by the readout chip to run these routines differs drastically from the command flow needed by the FE-I3 based modules of the existing pixel detector. The command flows are implemented newly within the framework of this thesis respecting the needs of the inherited high level algorithms. A detailed description of the test routines and the used algorithms is provided in [13]. No difference in the performance of the pixel matrix is expected between FE-I4A and FE-I4B. Only FE-I4B results are presented here unless explicitly mentioned to demonstrate differences between the two chip flavors.

The performance of the pixel matrix is characterized using the calibrated test charge injection circuitry. A first functionality test is the injection of a large test charge to each pixel. The result of this so-called analog test, a map with the occupancy of each pixel, is shown in figure 5.6. A number of 200 injections with a charge corresponding to 24 ke have been performed into each pixel. This specific FE-I4 readout



(a) (b)

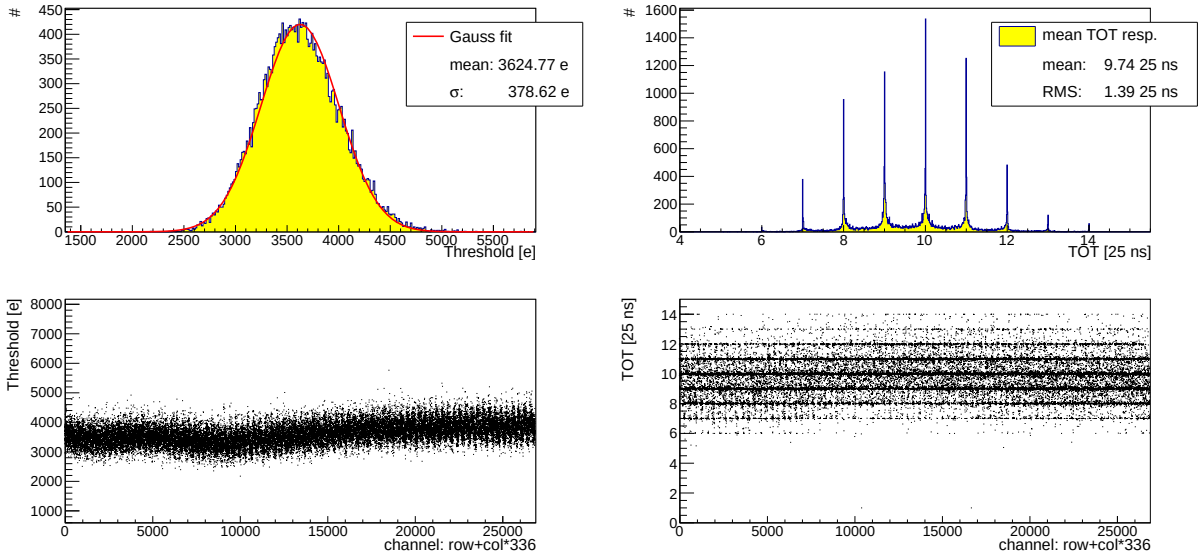
Figure 5.6: Occupancy maps of the FE-I4 pixel matrix. (a) shows the response to 200 analog test hit injections with ~ 24 ke at a threshold of ~ 3000 e, and (b) shows a map of digital test hit injections in the same readout chip.

chip shows a well working pixel array with only 32 pixels (0.12 %) not responding exactly 200 times. To disentangle errors in the analog readout chain from errors in the digital readout chain, a digital test (200 injections using the digital test hit injection circuitry) at high threshold can be used under similar conditions. The resulting occupancy map is shown in figure 5.6b. Only two pixels show an occupancy different from the number of injected test hits.

A uniform threshold and TOT response over the full pixel matrix is necessary for detector operation and data reconstruction. The threshold and feedback current is widely distributed over the pixel matrix due to process variations. Figure 5.7a shows the threshold distribution of an un-tuned FE-I4B chip. The width of a gaussian fit to the threshold distribution is about 380 e.

A similar result for the TOT response to test charge injections of 16 ke, which corresponds to the most probable charge generated by a MIP in the sensor, is shown in figure 5.7b. The pixels respond with a mean TOT between six and fourteen, which is more than half of the dynamic TOT range of the chip. This makes the charge information unusable and the adjustment at pixel level is mandatory.

Several algorithms are implemented in the USBpix system to adjust the threshold and feedback current setting globally and at pixel level. The tuning procedure is an iterative process of threshold and feedback current adjustments, because both influence each other. The IBL modules are tuned during the production quality assurance tests to a threshold of 3000 e and a feedback current resulting in a TOT of 10 in units of 25 ns for an injected charge of 16 ke. These values are motivated by the initial operation of the un-irradiated IBL detector. The threshold setting is a trade-off between the need to have a high enough signal above the threshold, which is needed to achieve a high hit detection efficiency, and the need to have a low noise hit occupancy, which is crucial to avoid fake hits which degrade the performance of the pattern recognition algorithms. The chosen feedback current setting allows the resolution of small hits due to charge charing between neighboring pixels while keeping the possibility to detect larger charges due to the high charge tail in the landau distribution. A very robust tuning algorithm is found and used later on for the generation of the initial module configurations. It consists of

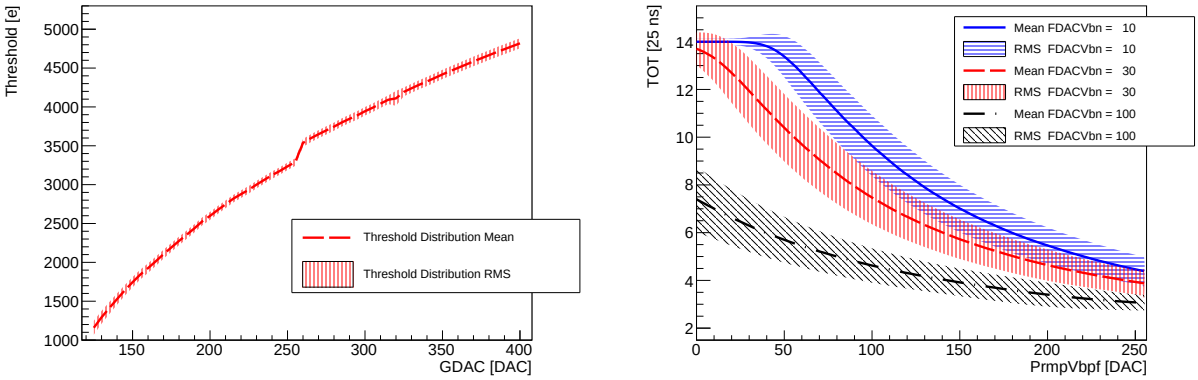


(a) (b)

Figure 5.7: An un-tuned threshold distribution of an FE-I4B chip (a). The large width of the distribution is due to production variations and indicates the need to adjust the threshold at the pixel level. The TOT response to injected charges of 16 ke of the same chip before adjustment at pixel level (b). The large TOT bins in the FE-I4 are visible as well as the need to tune the feedback current at pixel level.

1. global threshold adjustment
2. global feedback current tuning
3. global threshold tuning
4. pixel level threshold tuning
5. pixel level feedback current adjustment
6. pixel level threshold re-tuning starting from the previous result.

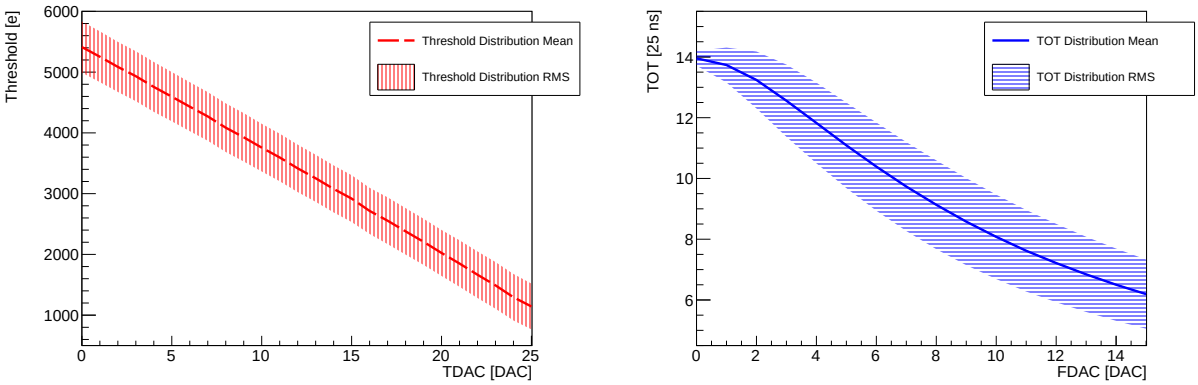
The influence of the global threshold and feedback current settings on the threshold and TOT distribution of the chip is shown in figure 5.8. Figure 5.8a shows the dependency of the threshold on the global setting for a tuned FE-I4B chip. In the FE-I4, the global threshold is generated by two DACs, a coarse and a fine DAC. A monotonous combination of both is constructed in the USBpix scan variable GDAC. To achieve the monotonicity in FE-I4B, the least significant bit of the coarse DAC is ignored, resulting in a step at a GDAC of 256 which is visible in figure 5.8a. This result already demonstrates the possibility to operate the FE-I4 pixel chip at a threshold in the order of 1500 e. Dedicated low threshold characterizations are performed on IBL prototype modules and the results are given in chapter 6.1.8.
A similar characterization for the global feedback current setting (PrmpVbpf) is shown in figure 5.8b. The average TOT response to 100 test charge injections of 16 ke is recorded as a function of the PrmpVbpf, resulting in TOT histograms as shown in figure 5.7b. The measurement is repeated for several settings of the step width of the feedback current adjustment at pixel level (FDACVbn). This setting influences also the PrmpVbpf dynamic range, so a trade-off between the achievable TOT response and



(a) (b)

Figure 5.8: Threshold as a function of the global threshold setting (a) and the TOT response as a function of the global feedback current setting (b) for an FE-I4B chip. The global threshold setting is realized by two DACs with overlapping dynamic range. The shown scan variable GDAC is a monotonous combination of both DACs implemented in the USBpix system. The global feedback current is adjusted by the DAC *PrmpVbpf*.

the adjustment performance needs to be found. The step width of $FDACVbn = 30$ is chosen for the initial tuning of all IBL production modules based on this result, because it is the lowest FDAC step width with a monotonous characteristic, and with still enough safety margin in the dynamic range to meet the target TOT response.
A similar characterization of the pixel level threshold and feedback current settings is shown in figure 5.9. Figure 5.9a shows the threshold as a function of the threshold setting at pixel level (TDAC). For

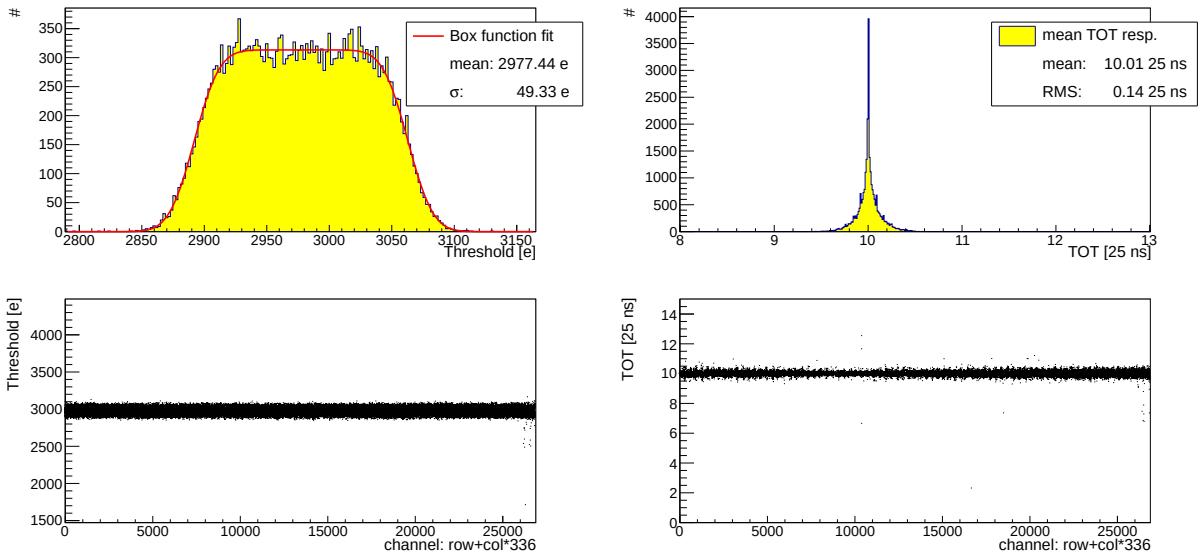


(a) (b)

Figure 5.9: The threshold as a function of the pixel level threshold setting (a) and the TOT response as a function of the pixel level feedback current setting (b) for an FE-I4B chip.

TDAC settings above 25 the threshold is too low on this specific chip to be operated in an un-tuned way and thus no reasonable threshold distributions are measured. The chip is tuned globally to a threshold of 3000 e beforehand. The TDAC setting resulting in 3000 e threshold is well centered in the dynamic

range of the TDAC. For the FDAC step width of $FDACVbn = 30$ motivated in figure 5.8b, the mean TOT response of the chip to injected charges corresponding to 16 ke and the RMS of the TOT distribution as a function of the feedback current setting at pixel level (FDAC) is shown in figure 5.9b. Again, the chip was tuned globally to the target value for initial IBL operation of 10 TOT for 16 ke of injected charge.
Figure 5.10 demonstrates the effectiveness of this tuning algorithm. The tuning procedure is used on an FE-I4B chip and the threshold distribution is displayed in figure 5.10a. The distribution demonstrates

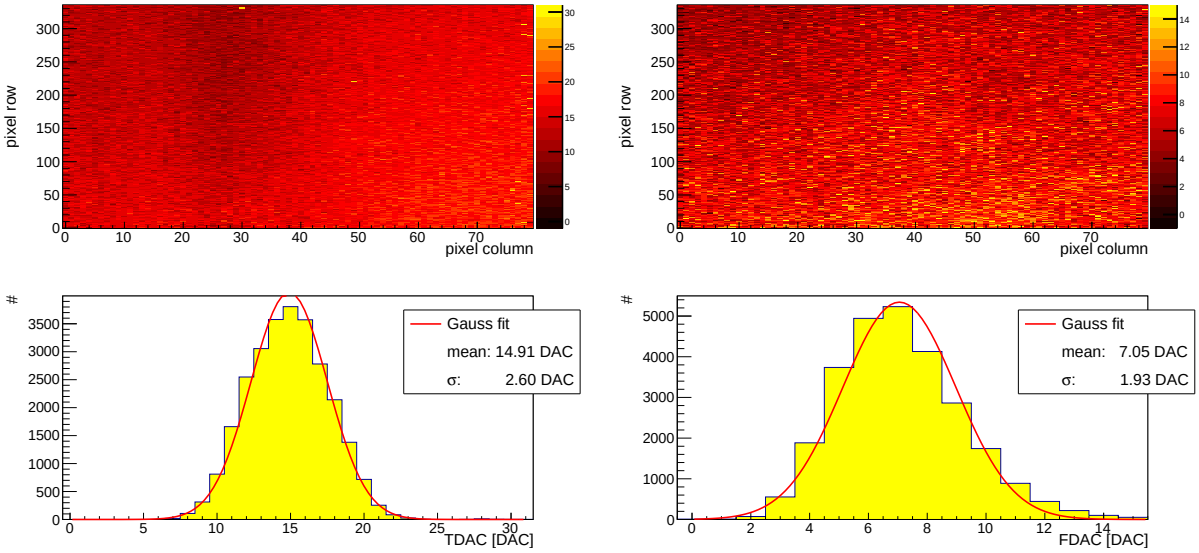


(a) (b)

Figure 5.10: A threshold distribution of an FE-I4B chip after a successful automated tuning procedure (a). The width of the distribution is reduced to the minimal achievable width with the TDAC step width of about 50 e. The TOT response to injected charges of 16 ke of the same chip after adjustment at pixel level (b). Nearly all pixels respond with the target TOT of 10.

the successful adjustment of the threshold to the target value. The expected threshold distribution after the tuning is uniform and centered around the target value. It is box-shaped and the width corresponds to the TDAC step width (LSB). As the TDAC step width varies slightly from pixel-to-pixel, the edges of the uniform distribution are convoluted with a gaussian in the fit function. This distribution is expected, if the algorithm finds the best setting for each pixel. The standard deviation of this threshold distribution is about 50 e after tuning, compared to the standard deviation of the un-tuned distribution of about 380 e. The pixels with a measured threshold of more or less than five times the standard deviation of this distribution are counted. For this particular chip, only eleven pixels, which is about 0.4 ‰, are outside of this region.
With the FDAC step width setting of $FDACVbn = 30$, the width of the mean TOT response distribution to 16 ke is reduced to a RMS of only 0.14 e using the automated tuning algorithm (figure 5.10b). Only 27 pixels, which is about 1 ‰ of all pixels, respond with a mean TOT outside the 5 RMS of the distribution. It could be shown that the same kind of tuning results are obtained in the entire temperature range of −40 °C to 40 °C and after proton irradiation up to 300 Mrad [36].
Another indicator for the quality of the tuning are the TDAC and FDAC distributions. After the tuning both should be gaussian distributed around the central value and ideally cover the full dynamic range.

However, some margin to the extreme values makes the tuning algorithm more capable to adjust pixels with extreme initial feedback current and threshold values successfully. Figure 5.11 shows the TDAC

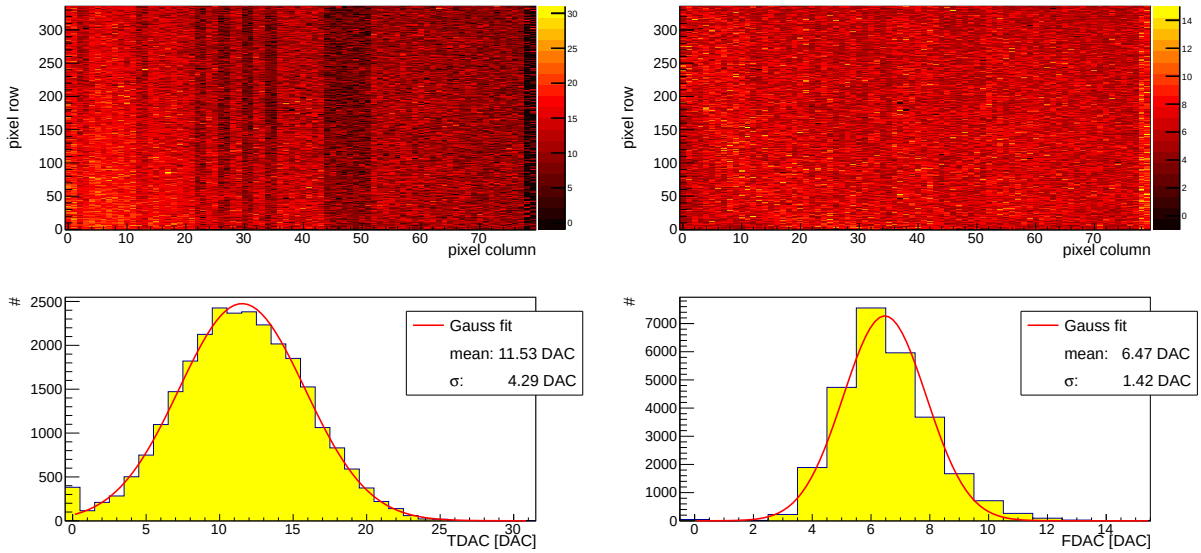


(a) (b)

Figure 5.11: TDAC (a) and FDAC (b) map and distribution of an FE-I4B chip after the tuning procedure.

and the FDAC distribution of this FE-I4B. The distributions are well homogenous and centered around the central value of the DAC setting.
The TDAC map is very sensitive to inhomogeneities in the charge calibration of the chip or of the test pulse injection circuitry. Therefore, the different pixel prototypes in FE-I4A are visible in the TDAC and FDAC distribution shown in figure 5.12, which are recorded on an FE-I4A chip. In figure 5.12a in particular, the various double-column flavors can clearly be distinguished by their different TDAC values. Different preamplifier feedback capacitor flavors are implemented in column 3-4, 13-14, 23-24, 27-28, 31-32, 35-36, and 45-52. The different feedback capacitors influence the gain of the preamplifier and thus the charge calibration of the pixels. Low power discriminators are prototyped in column 79-80. The resulting charge calibration differs between the double column flavors. This is not respected in the tuning algorithm and as a consequence the threshold tuning compensates the charge calibration differences by the setting of the TDAC values.
The electronic noise is another important performance characteristic of the analog pixel cell. The noise is commonly expressed as the equivalent amount of charge at the input node of the amplifier chain, which results in a signal of equal amplitude as the noise (Equivalent Noise Charge, ENC). The expected ENC is calculated for the FE-I4, see [28]. Three major noise sources are considered in these calculations:

- thermal and 1/f-noise originating from the transistor channel of the preamplifier input transistor.
- thermal noise in the preamplifier feedback loop.
- shot noise from the sensor leakage current and thermal noise from the leakage current compensation transistor.



(a) (b)

Figure 5.12: A typical TDAC map and distribution of an FE-I4A chip after threshold adjustment at pixel level (a). The TDAC map is very sensitive to any inhomogeneities in the matrix and the different feedback capacitor flavors prototyped in the FE-I4A chip are visible in the map. The FDAC map shown in (b) is less sensitive due to the large TOT bins of FE-I4.

The calculations result in [28]

$$ENC = \sqrt{\alpha \cdot (2I_{leak} + I_{fb}) \cdot \frac{\tau_b^2}{\tau_b + \tau_c} + \beta \cdot C_{det}^2 \cdot \left(\frac{1}{\tau_c} + \frac{\tau_a^2}{2\tau_c^3}\right) + \gamma \cdot K_F \cdot C_{det}^2 \left(\frac{\tau_a^2}{2\tau_c^2} + ln\left(\frac{\tau_b}{\tau_c}\right)\right)} \qquad (5.3)$$

with the leakage current I_{leak}, the feedback current I_{fb}, and the detector capacitance C_{det}. α, β, and γ are constants depending on several capacitances and resistors, the temperature and the preamplifier gain. K_F is the 1/f-noise coefficient for a NMOS transistor and $\tau_a = C_f/g_m$, $\tau_b = C_f/g_{ds,fb}$, and $\tau_c = C_{det}/g_m$ are time constants. The ENC is therefore proportional to the detector capacitance as well as to the square root of the leakage current of the sensor and of the feedback current of the preamplifier. For a low sensor leakage current, the dominant term for a high detector capacitance of about 400 fF is the thermal noise of the preamplifier input. For a low sensor leakage current and a low detector capacitance, the thermal noise of the feedback transistor is dominant [44]. The calculated as well as the simulated ENC as a function of the detector capacitance is shown in figure 5.13.

The detector capacitance is measured with a dedicated chip, the PixCap [50]. The PixCap chip has the same pixel segmentation and the same bump pad dimensions as the FE-I4. The detector capacitance without a sensor is dominated by the bump pad capacitance and is (11.6 ± 0.1) fF. The detector capacitance of a planar silicon sensor is measured to be (111.7 ± 3.8) fF. The detector capacitance measurement of a 3D sensor fabricated at CNM results in (169.4 ± 1.5) fF.

Figure 5.14 shows the noise distribution of a FE-I4A chip after tuning to the operation point of the IBL detector as explained above. No difference in the ENC of FE-I4B is observed. The mean value of 120 e is as expected from the calculations and the ENC is uniformly distributed over the whole chip. The ENC as a function of the feedback current is measured at a threshold of 3000 e, see figure 5.15a. The

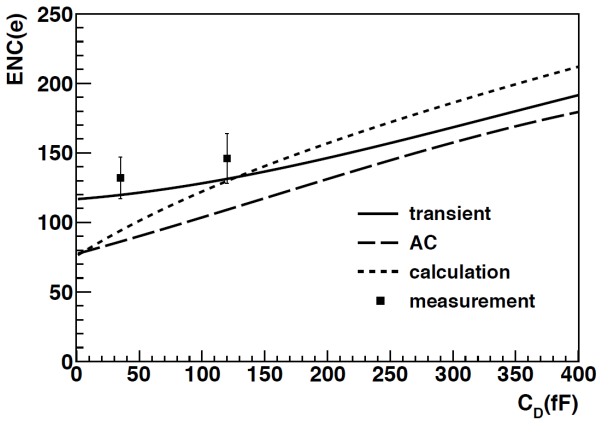


Figure 5.13: The calculated as well as the simulated ENC as a function of the detector capacitance [28].

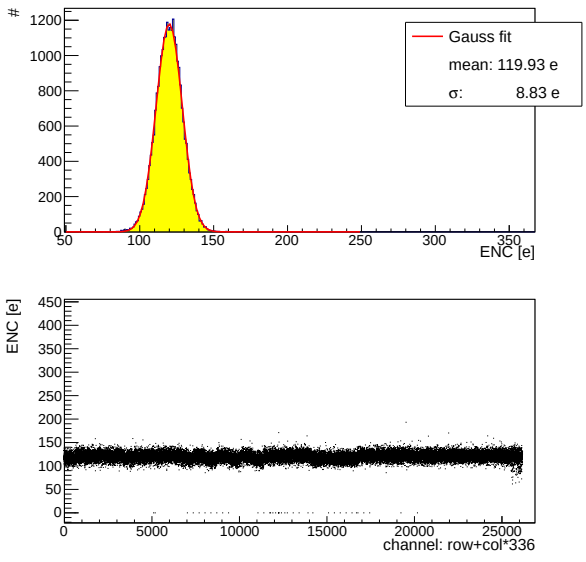
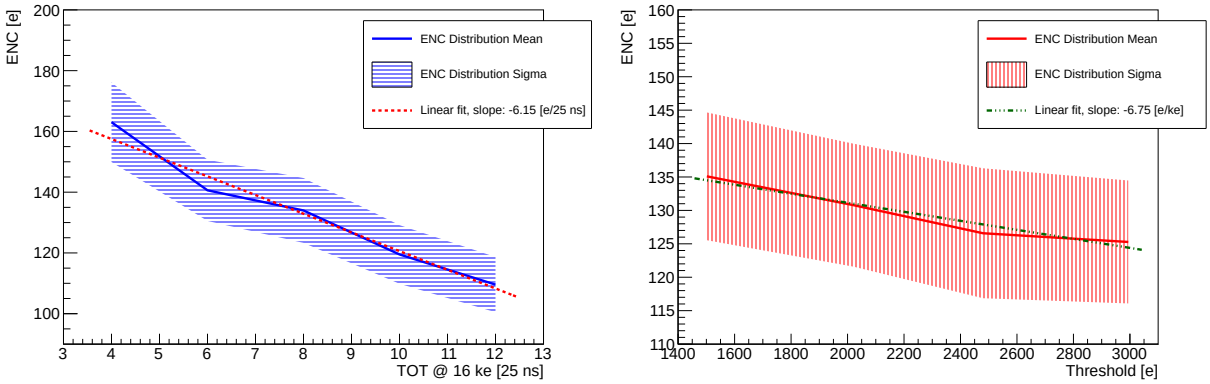


Figure 5.14: A noise distribution of a FE-I4A chip at the IBL operation point of the chip.



(a) (b)

Figure 5.15: The ENC as a function of the operation point in terms of feedback current (a) and threshold (b). The feedback current is tuned to several TOT responses at an injected charge corresponding to the charge deposited in the sensor by a MIP.

expected rise for increasing feedback current is observed. The ENC increases approximately by 6 e per TOT step of 25 ns at 16 ke of injected charge.
An additional small influence of the discriminator threshold on the ENC is observed and presented in figure 5.15b. The ENC increases by approximately 6.8 e for a threshold decrease of 1000 e. A more detailed characterization of the operation at low thresholds in the order of 1500 e is done on the IBL prototype modules and is presented in chapter 6.1.8.

5.4 Characterization of digital functionalities

The small feature size of the 130 nm IBM technology used for the FE-I4 enables chips with high logic density. Consequently, many digital functionalities that are beneficial for the detector operation or chip testing are present in FE-I4. Test routines for all these functionalities have been developed and implemented into the USBpix system in this thesis and all blocks are characterized in detail. Presenting the test routines and the obtained results of all the blocks would go beyond the scope of this thesis. Results for some important functionalities for detector operation are presented below. The biggest blocks with digital functionality are:

- Configuration registers. Configuration and read-back of global as well as pixel registers with several bit-patterns. Global register read-back is problem-free in both chip flavors. Pixel register read-back shows timing problems in FE-I4A, that have been fixed in the FE-I4B design.

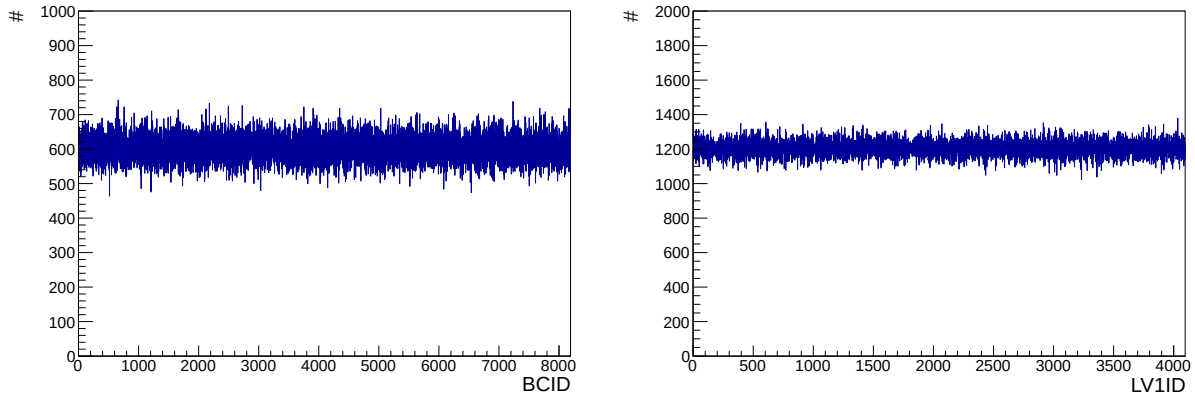
- Data output block. Data encoding of the chip works in 8bit/10bit [51] mode (default for operation) and in raw data mode for several data transmission rates. The loop-back of several on-chip clock nets and debug patterns is functional (for debugging purposes).

- Error counters. Several error counters allow the detection of problems such as reference clock frequency mismatch, incoming trigger skipping and many more. A few error counters are not working in FE-I4A, the functionality of all counters is verified in FE-I4B.

- Bunch crossing counter (BCID) and Level-1 trigger counter (LV1ID). For operation in ATLAS the BCID and LV1ID counter sizes are increased in FE-I4B. All versions are operational. See chapter 5.4.1.
- Service records. Dedicated words in the data stream transmit messages from the error counters and BCID and LV1ID counters. Generation and transmission as well as the masking option of service records is functional.
- Self-trigger. Both chip flavors provide a self-triggering operation mode. This mode works without problems in FE-I4A as well as in FE-I4B.
- Four pixel digital region. The performance of the sophisticated new architecture of the four pixel digital region is characterized in detail and shows great performance in both chip flavors. As an example, the result of the maximum hit occupancy test (coincident hit in all 26880 pixels) is presented in chapter 5.4.2.
- Event size limit. The ability of the digital readout chain to transmit huge numbers of coincident hit information requires the implementation of an adjustable event size limit for detector operation, which additionally provides the possibility to request the restrained hits at a later time. This new functionality is added in the FE-I4B and is functional.
- Event counter reset. The possible hit accumulation due to the event size limit requests the possibility to erase the restrained hits. This event counter reset is proven to be operational.
- Small hit discrimination. This functionality addresses the time-walk of small hits. The complex functionality and its test is described in chapter 5.4.3.
- Small hit erase. The small hit discrimination is designed for single bunch crossing readout during detector operation. Discriminated hits are duplicated in case of several consecutive Level-1 triggers as used for testing. The possibility to delete discriminated hits after assignment to neighboring big hits is added in FE-I4B and working as expected.
- EFUSE registers. Both chip flavors contain non-rewritable registers. These are used to burn a unique serial number into each readout chip of the IBL production during the wafer probing. The burn and read-back functionality is operational.
- Scan chain test. The three big digital blocks of the readout chip, command decoder, end of chip logic and data output block, can be tested using a industrialized test method called scan chain test at flip-flop level. This is used on each readout chip of the IBL production during the tests at wafer level.

5.4.1 BCID and LV1ID counter

A Bunch Counter ID (BCID) and a Level-1 trigger ID (LV1ID) are assigned to each hit in the FE-I4. They provide an ATLAS wide time-stamp information and are very important for data reconstruction. The bit number of the counters is increased in FE-I4B with respect to FE-I4A to fulfill the requirements of the data reconstruction. An adjustment of the data stream format in FE-I4B is necessary to transmit the increased amount of information. The least significant bits are transmitted in the data header word that is sent for each Level-1 trigger and a new service word is implemented to transmit the most significant bits, if they are incremented. The data acquisition system needs to combine the information



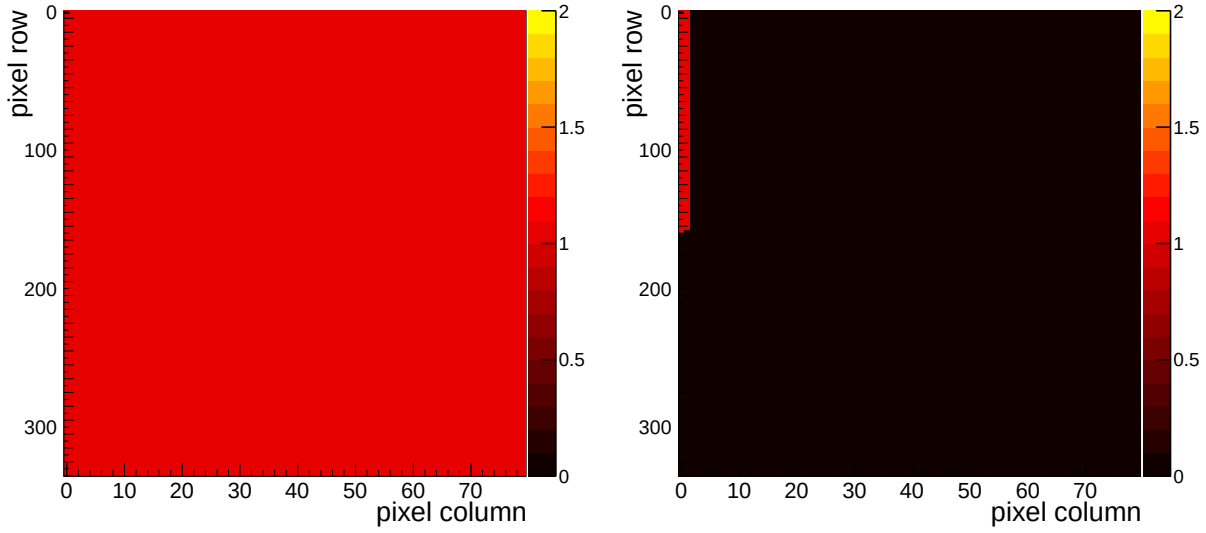
(a) (b)

Figure 5.16: Bunch crossing ID (BCID) distribution of hits randomly distributed in time (a). The flat distribution without counter values with significant lower number of hits proves the functionality of the counter and the transmission of the BCID. Level-1 trigger ID (LVL1ID) distribution assigned to the same hits (b). The result is similar and the lower bit number of the LV1ID counter is visible.

from both words to assign the correct time-stamp to each hit. Several tests are performed with injections at known time stamps, proving the correct functionality of the counters. Additionally, each bit of the counters is tested on all chips during the IBL production using hits from a radioactive source which are by nature randomly distributed in time. The number of hits per BCID and LV1ID is thus expected to be constant in this test. Figure 5.16 demonstrates that both counters work as expected.

5.4.2 Four pixel digital region and event size limit

In contrary to the existing ATLAS and CMS pixel detector readout chips, the FE-I4 architecture stores the hit information inside the pixel matrix until the arrival of the Level-1 trigger to avoid the inefficiency due to peripheral buffer limitation and copy procedure to the periphery. The hits are processed and stored in the 4-pixel digital region which is described in chapter 4.3.3. The 4-pixel digital region can handle hit occupancies up to a simultaneous hit in all 26880 pixels. Figure 5.17a shows a hit-map of a simultaneous digital hit injection into all pixels. The perfect response of the chip proves, that the 4-pixel digital region and subsequent data processing logic processes events up to the maximum possible instantaneous hit occupancy as expected.
On the other hand, this can result in events followed by a very long dead time due to data transmission. To prevent this during operation in ATLAS, an adjustable event size limit is implemented in FE-I4B. After the number of hits specified by the event size limit were transmitted, the FE-I4B stops sending hits and closes the event data stream. Figure 5.17b shows the result of a similar simultaneous injection with the event size limit set to ten. Only a fraction of the hits is received by the USBpix system until the event data stream is closed by the chip. The remaining hit information is not deleted unless the event counter reset is sent to the chip. Thus, they can be requested at a later time, if a new Level-1 trigger is sent before the event counter reset command is issued. Several combinations of event size limit settings and event counter resets are tested and all work as expected.



(a) (b)

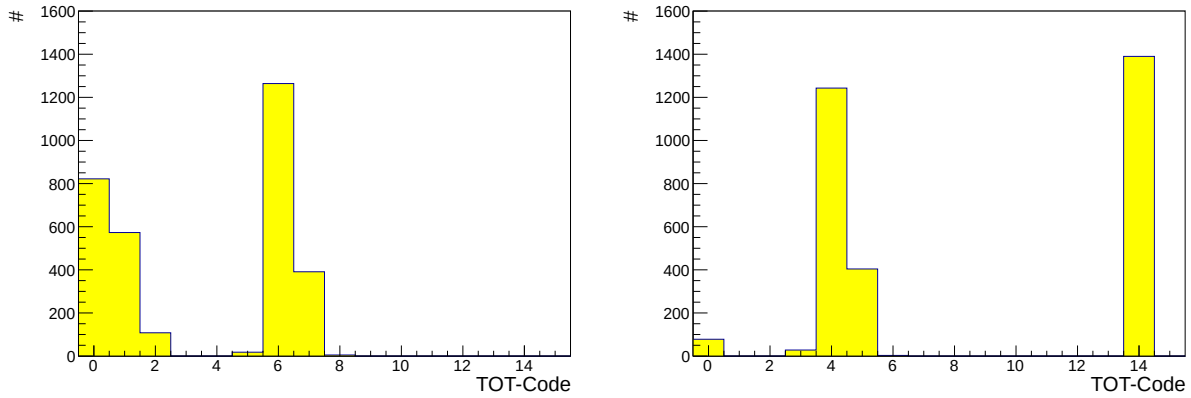
Figure 5.17: The occupancy map of a simultaneous digital hit injection into all pixels with disabled (a) and enabled (b) event size limit.

5.4.3 Small hit discrimination

Due to charge sharing hits with small charge are expected during detector operation in pixels close to hits with large charge. There is a probability that the small hits are detected within the subsequent clock cycles due to time-walk (see chapter 6.1.5). The small hit discrimination provides an adjustable small hit discrimination threshold (which uses the TOT information) and assigns the small hit to a potential neighboring and (or) precedent big hit, or discards the hit in case no neighboring big hit is present. A hit that is a small hit is assigned a TOT-Code of 14.
All discrimination thresholds are tested during the IBL production. Figure 5.18 illustrates the result of one of these tests. A small and a big charge are simultaneously injected into neighboring pixels for different settings of the small hit discrimination circuit. The result presented in figure 5.18a is obtained with the small hit discrimination disabled, while the highest discrimination threshold is used for the result in figure 5.18b. The TOT-Code of the FE-I4 changes with the discrimination threshold setting. In case of disabled discrimination, the TOT of a hit is given by TOT [25 ns] = TOT-Code + 1, while for the presented maximum discrimination threshold it is TOT [25 ns] = TOT-Code + 3. The resulting shift in the TOT-Code by two is visible in the peak position of the large injected charge from TOT-Code six to TOT-Code four. The small hits in figure 5.18a with a TOT-Code of zero and one are discriminated and transmitted with an assigned TOT-Code of 14. This proves the functionality of the small hit discrimination circuit.

5.5 Low dropout regulator and reference voltages

Detailed characterizations of the blocks needed for the powering of the FE-I4B are performed in the framework of this thesis. This includes in particular the characterization of the two on-chip reference voltage options for the LDOs and the LDO output voltage itself. The minimum temperature that can



(a) (b)

Figure 5.18: Results of the small hit discrimination test. The TOT-Code distribution is shown for simultaneous analog injections corresponding to a small and to a big charge in neighboring pixels. The small hit discrimination is switched off in (a) and set to maximum discrimination threshold in (b). The expected shift in the TOT-Code and the assignment of a TOT-Code equal to 14 to the discriminated small hits is visible.

occur in IBL (due to the cooling system) is −40 °C, so a reliable power-up down to temperatures as low as −40 °C is mandatory for safe operation of the IBL. The results presented below motivated the implemented IBL powering scheme.

5.5.1 Characteristics of the band-gap reference voltage

The performance of the voltage reference after irradiation is crucial. Therefore FE-I4B bare chips have been irradiated at the Los Alamos irradiation facility using 800 MeV protons. The output voltage of the

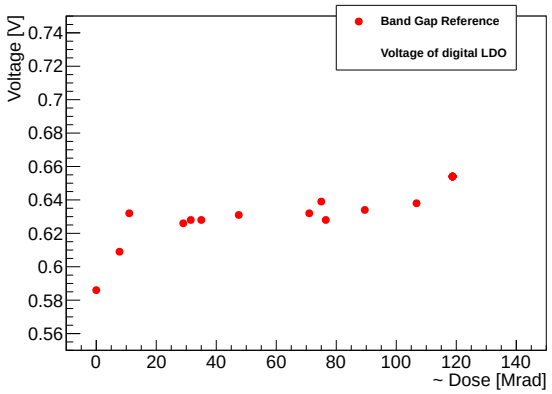


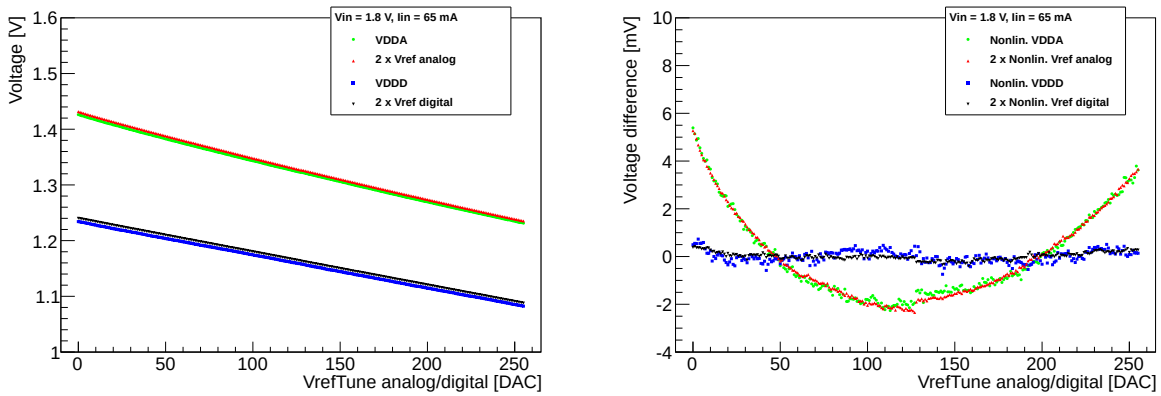
Figure 5.19: The output voltage of the band gap based reference voltage measured during the 2011 irradiation campaign at Los Alamos.

band gap based voltage reference for the digital LDO has been measured during the irradiation and is plotted as a function of the total ionizing dose in figure 5.19. The band-gap based reference voltage increases with dose. A similar behavior is expected for the band gap based reference for the analog

LDO. This could endanger the chip after irradiation if the analog input voltage of the chip increases above 1.6 V. Consequently, this reference voltage can not be used stand-alone for the analog LDO. As explained in chapter 5.5.3 a solution is found by using it in combination with the tunable reference.

5.5.2 Characteristics of the tunable reference voltage

The tunable reference voltage for the analog and digital supply voltage as well as the resulting LDO output voltages have a good dynamic range and linearity, see figure 5.20. Figure 5.20a shows twice the



(a) (b)

Figure 5.20: Characteristics of the tunable reference voltage. The regulator output voltages for analog and digital supply voltage and twice the reference voltages as a function of the tune DAC is shown in (a) and the difference between the measured voltage and the ideal output voltage (obtained from a linear regression) is shown in (b). Again, for the reference voltages twice the nonlinearity is given. The maximum distance from zero corresponds to the integrated nonlinearity.

reference voltage for both LDOs and the LDO output voltages, that are routed to the core of the chip as analog and digital supply voltages. A good dynamic range is achieved by both LDOs. The nonlinearity, here defined as difference between the measured voltage and the ideal voltage, is shown in figure 5.20b. The ideal voltage is derived from a linear function fitted to the data. The digital reference voltage and as a consequence also the digital supply voltage have a very good linearity with an integrated nonlinearity (INL) of the digital LDO output that is smaller than 0.75 mV. The INL of the digital reference voltage is less than 0.22 mV. A clear bow is observed in the output voltage of the analog LDO of this specific device. This bow is already present in the analog reference voltage, so the origin of the nonlinearity is the reference voltage. The LDO output voltage follows this nonlinearity. However, the resulting INL of the analog supply voltage is below 5.4 mV, which corresponds to only about 0.4 % of the supply voltage of 1.4 V. The INL of the analog reference voltage is smaller than 2.65 mV.
Although a start-up circuit has been added, the fact that the reference current circuitry, which is used to generate the tunable reference voltages (see chapter 4.3.3), is powered by the analog supply voltage is a concern for the start-up of this block. If the start-up is not fully reliable under all conditions, then also the adjustable reference can not be used stand-alone to control the analog regulator. The start-up behavior is shown in figure 5.21, where the reference voltage for the analog LDO and the resulting analog LDO output voltage are measured for 1000 power-cycles at −40 °C. A number of 529 start-up cycles (52.9 %) results in too low reference voltage and therefore also low LDO output voltage. The

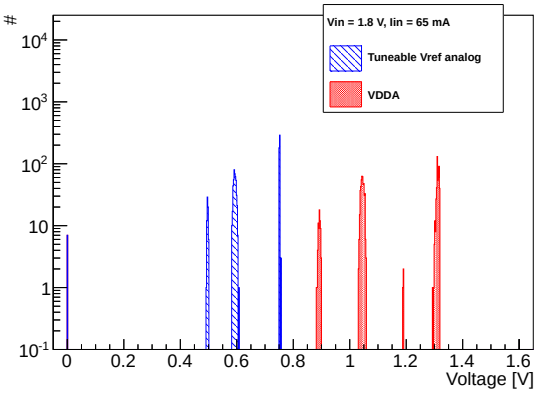
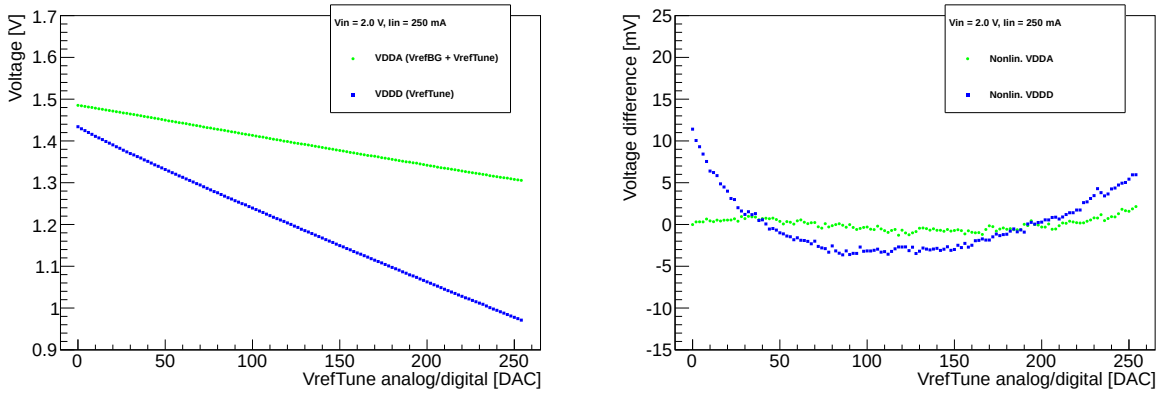


Figure 5.21: Tunable reference voltage and analog supply voltage for 1000 power up processes at −40 °C. A fraction of 53 % of power-up processes results in too low reference voltage and thus analog supply voltage.

behavior becomes reliable for all chips tested above −10 °C, but the minimum reliable temperature varies from chip-to-chip, and in any case the operation must be qualified down to −40 °C.

5.5.3 The IBL reference voltage connection scheme

A reference voltage connection scheme which provides reliable power-up in a large temperature range while keeping the tunability of the LDO output voltage for both LDOs (and therefore safe operation after heavy irradiation) has been achieved. For the analog regulator the tunable reference voltage and the band-gap reference output are tight together. This provides the benefit of a higher startup current for the reference current and results in safe power-up of the analog regulator. The increased value of the band-gap reference voltage with dose can be compensated due to the kept tunability. The design of



(a) (b)

Figure 5.22: The regulator output voltage as a function of the tuning DAC using the IBL powering scheme (a), and the INL of this measurement (b).

both references is compatible with parallel connection. For the digital regulator it is sufficient to use the tunable reference voltage only, because the reference current generation block is powered from the

analog regulator. This increases the dynamic range of the digital regulator output voltage.
The regulator output characteristics and the nonlinearity of the analog and digital regulators in this powering scheme are shown in figure 5.22. Both regulators have a good dynamic range (figure 5.22a). The bow in the nonlinearity is present in the digital LDO for this specific chip. The INL of the digital

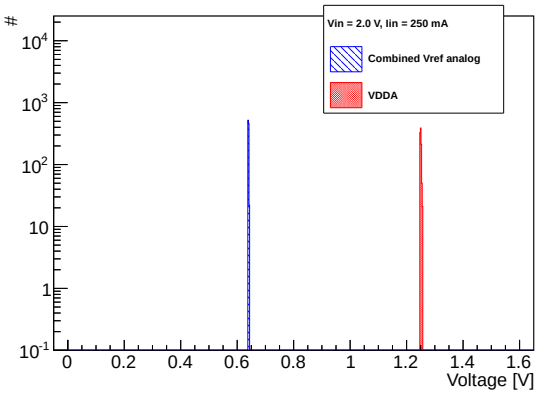


Figure 5.23: The result of the startup reliability tests at −40 °C using the IBL powering scheme.

LDO is still below 11.42 mV (0.95 %). The analog LDO has an even smaller INL of less than 2.15 mV. Also the power-up behavior is tested in this powering scheme. The reliability is proven down to temperatures as low as −60 °C. The result of the measurement at −40 °C presented in figure 5.23 demonstrates the power-up reliability of the IBL powering scheme in the full temperature range.

5.6 Production wafer probing results

The wafer level production quality assurance (QA) program concentrates on functionality tests of the chips and measures all chip characteristics that are not accessible after module assembly, such as the charge calibration. Additionally, a full functionality validation of each individual pixel and digital tests such as scan chain tests are performed for all big digital blocks in the readout chip periphery. All scan routines used in this program are implemented into the USBpix test system in the framework of this thesis. Summary results of all 43 wafers (2580 FE-I4B chips) that are probed for IBL are presented here. Additional information is given in [52].
A sophisticated data analysis and cut program[3] is used for automated chip classification. Different cuts are used for pixel level and global measurements. All pixel level tests such as digital and analog performance tests influence the pixel level cuts. The analog and digital functionality of each pixel is extensively tested. The response to digital and analog injections as well as cross-talk between neighbor pixels (see chapter 6.1.7) are measured. Threshold and noise scans measure the analog performance. The final result is a total number of pixels failing any cut. Up to 53 pixels (0.2 % of the chip) are allowed to fail in any cut for a chip suitable for IBL production. As sketched in figure 5.24 the pixel level cuts can translate to column level cuts, if the number of failing pixels exceeds the allowed number of broken pixels within one column, which is used in classifying test grade chips. In addition to pixel and column cuts, all global chip characteristics such as power consumption, charge calibration or mean noise level feed into the global chip cuts.

[3] This program called WaferAnalysis is also adapted and used for the module qualification tests.

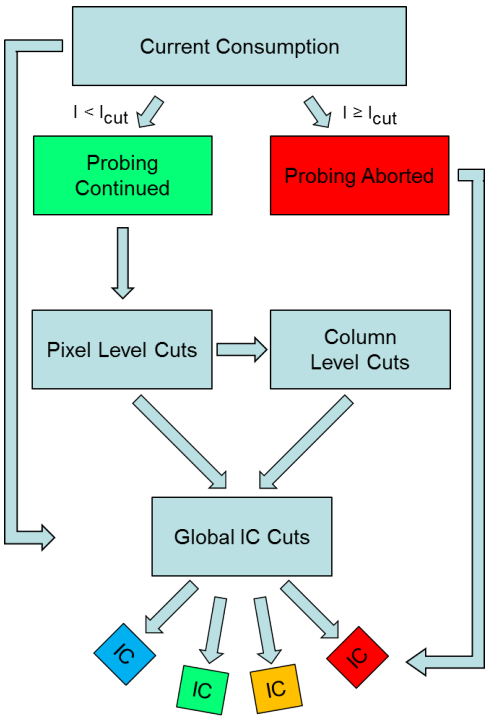
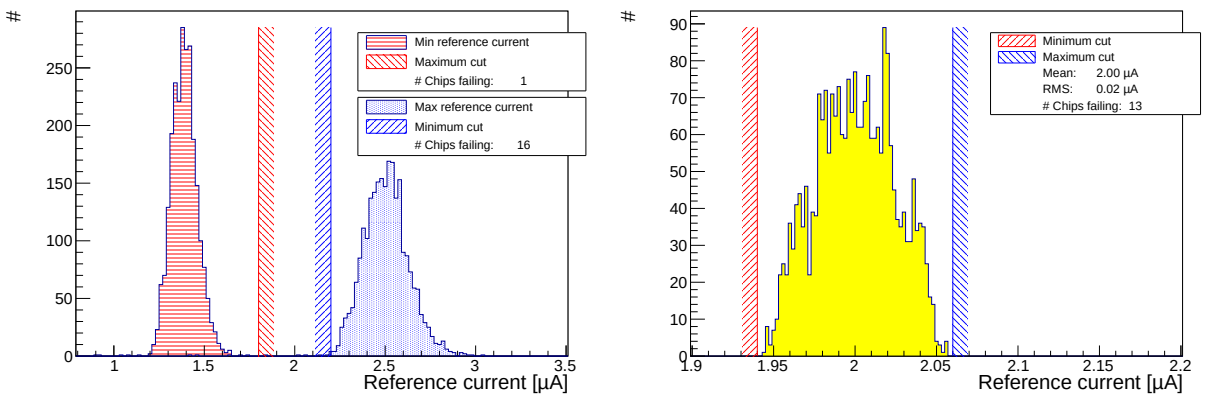


Figure 5.24: The cut flow of the wafer probing analysis program [53]. The boxes represent different cut levels and the arrows illustrate communication directions.

The only condition resulting in an abortion of the test run is a significantly high current consumption of the chip after startup. A digital supply current above 350 mA or an analog supply current exceeding 300 mA at startup aborts the probing of the chip to protect the probe needles.
Finally four different states are assigned to the chips: green chips are chips which can be used for the IBL production, yellow chips are suboptimal chips which can still be used for further R&D such as future sensor concept characterization, red chips are non-recoverable and a special state ”blue” is assigned to any chip for which the software is unable to apply reasonable cuts, and therefore interaction and data crosscheck is needed. It is possible to assign any state from ”blue” after careful data crosscheck.
Several examples of chip-to-chip distributions from the readout chip characteristics described above are presented in the following sections. These distributions contain results of all 2580 readout chips probed for the IBL production.
For all measurements of voltages at wafer level a systematic error originating from the high voltage drop across the probe needles is present. During the IBL production wafer probing this voltage drop is approximately measured using configurations with different current consumption and an extrapolation to zero current consumption. The resulting voltage drop is then used to correct the measured voltages. A systematical error of ±50 mV on all voltage measurements at wafer level still needs to be considered.

5.6.1 Reference current tuning

The reference current characteristics is measured on each chip. The dynamic range of each chip is verified using the minimum and the maximum achievable reference current. Figure 5.25a presents the chip-to-chip distribution for both. The lowest reference current must be below 1.8 µA (displayed as maximum cut) and only one chip fails this criteria. 16 chips show a maximum reference current below



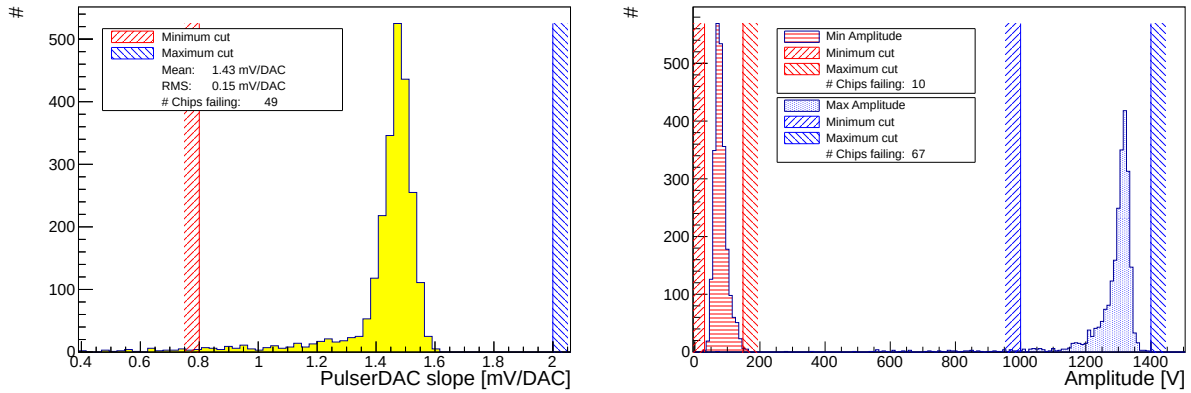
(a) (b)

Figure 5.25: chip-to-chip distributions of the minimum / maximum of the dynamic range of the reference current (a) and the reference current for the value closest to the design value of 2 µA (b) for all chips tested for the IBL production. Also the cut values used for the chip selection are also displayed. For the measurement in (a), only the minimal reference current must be below the indicated maximum cut, and the maximal reference current above the minimum cut. A reference current within the region between the minimum and the maximum cut shown in (b) is requested for selected chips.

2.2 µA and thus are excluded from IBL production.
A second quantity is used for chip selection. The reference current closest to the design value of 2.00 µA must be between 1.94 µA and 2.06 µA. The distribution of this is shown in figure 5.25b and 13 chips fail this cut. The distribution centers perfectly at 2.00 µA and has a RMS value of 0.02 µA.

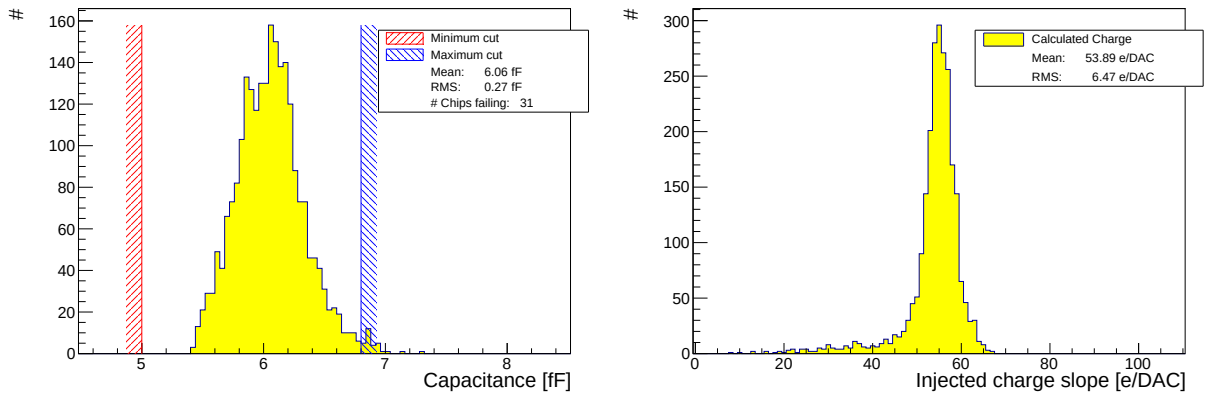
5.6.2 Test charge injection circuitry calibration

Chip-to-chip distributions of the pulser circuit calibration is summarized in figure 5.26. The distribution of the slope of the linear regression peaks at 1.43 mV/DAC with a RMS of the histogram of 0.15 mV/DAC. A tail towards low slopes is present. The cut values are also displayed below and above which the IC is excluded from the IBL production and 49 chips fail this requirement.
Also the minimum and maximum achievable voltage step amplitude is used to classify chips. Figure 5.26b shows the chip-to-chip distribution for both. Ten chips are out of the allowed minimum achievable voltage step amplitude range, and 67 chips are above the maximum specification.
Figure 5.27a presents the chip-to-chip distribution of the measured injection capacitance as discussed in chapter 5.2. All chips contain an injection capacitance between 5.2 fF and 7.4 fF. The distribution peaks at 6.06 fF with a RMS of 0.27 fF. This is in good agreement with the simulated injection capacitance of 5.7 fF. A large uncertainty on the simulated injection capacitance is expected. The accepted range is between 5.0 fF and 6.8 fF and 31 chips show an injection capacitance above this range.
The resulting injected charge per PulserDAC step is calculated for each chip and the distribution is shown in figure 5.27b. This quantity is not used for chip selection and thus no cut values are displayed. This applies also to other quantities not used for selection in the following. The mean injected charge of all chips probed for IBL is 53.89 e/DAC with a RMS of 6.47 e/DAC.



(a) (b)

Figure 5.26: The slope of the linear regression on the output characteristic of the test charge injection pulser circuit (a) and the minimal and maximal achievable voltage step amplitude (b). The cut criteria on the slope is chosen to be loose while a tight cut criteria (region for minimal as well as maximal amplitude) is used for the dynamic range.

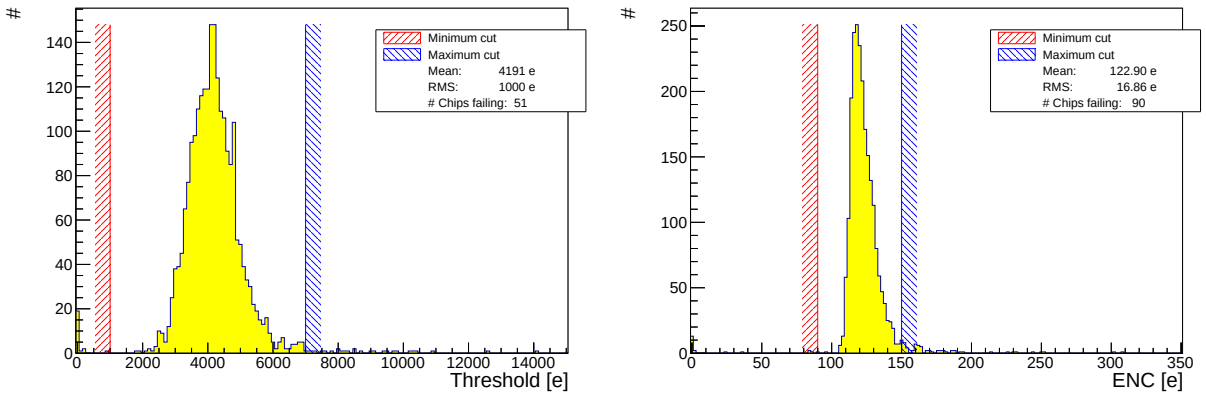


(a) (b)

Figure 5.27: Injection capacitance chip-to-chip distribution (a). All chips are accepted with a injection capacitance in the indicated region. The resulting injected charge in electrons per PulserDAC step distribution (b). This quantity is calculated offline and not used for chip selection.

5.6.3 Threshold and noise distribution at wafer level

A threshold and noise measurement is performed on each IC. The thresholds are not tuned during the wafer level tests and therefore a wide chip-to-chip distribution as seen in figure 5.28a is expected.
The noise is not expected to be considerably influenced by the mean threshold of the chip and therefore the noise distribution is expected to be centered around the mean noise value of approximately 125 e as measured on bare FE-I4A prototype chips, see chapter 5.3 and [54]. Indeed the chip-to-chip distribution



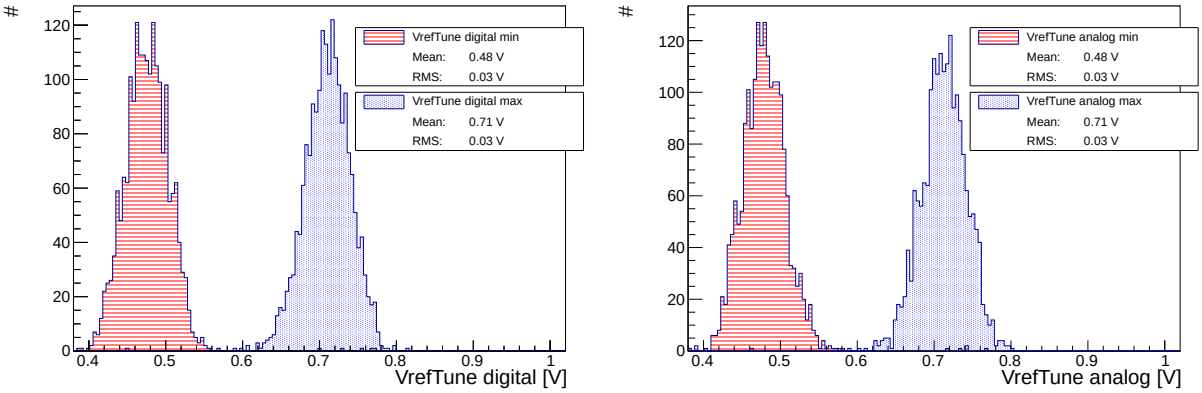
(a) (b)

Figure 5.28: The threshold (a) and noise (b) distribution in electrons for all IBL wafers. The thresholds are not tuned and broad distribution is expected. This reflects also in the very loose selection criteria. The ENC is expected around 123 e from measurements on prototype chips and must be within the shown cuts.

of the noise distribution measured on the IBL wafers has a mean of about 123 e with a RMS of 17 e. All chips with a mean ENC between 90 e and 150 e are accepted for production.

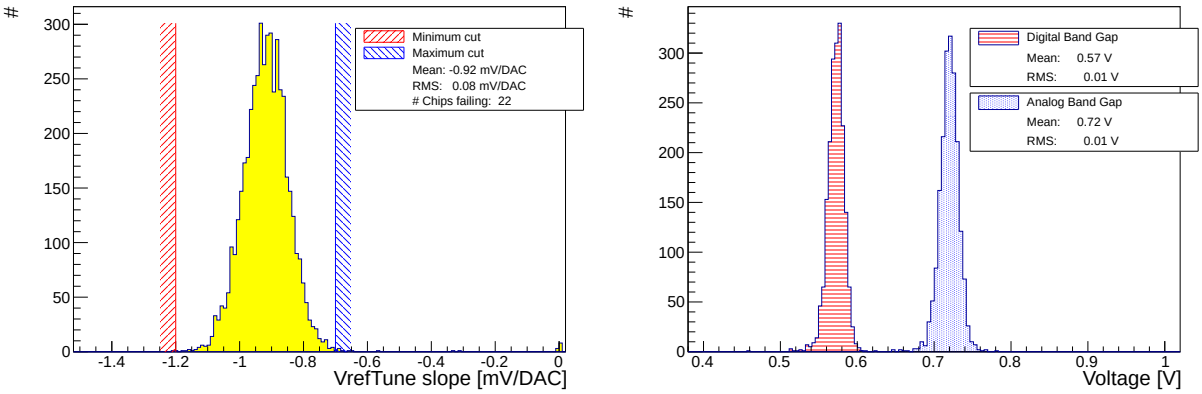
5.6.4 Characterization of powering blocks

The on-chip reference voltage blocks are characterized on wafer level as well. The chip-to-chip distributions of the minimum and maximum values for the tunable reference voltage for the digital and the analog supply voltage is shown in figure 5.29. Both reference circuits are identical and use the reference current to generate the output voltage as explained in chapter 4.3.3. Thus, no significant difference is expected in the characteristics.
The digital as well as the analog tunable reference voltage have a minimum output voltage distribution that peaks at a mean value of 0.48 V and a maximum output voltage distribution with a mean value of 0.71 V. The RMS for all four distributions is 0.03 V. Also the slope of the tunable reference voltage characteristics is similar for both circuits. In figure 5.30a the slope of a linear regression to the analog and digital tunable reference output voltage characteristics is presented in a single histogram. Eleven chips do not fulfill the selection criteria of a slope between -1.2 mV/DAC and -0.7 mV/DAC.
The fixed output voltage of the band-gap based reference voltage for digital and analog LDO is summarized in figure 5.30b. Both circuitries peak around 30 mV below the design target of 0.6 V for the digital LDO and 0.75 V for the analog LDO. However, this difference is within the above explained systematical error of voltage measurements at wafer level. The output characteristics of the LDOs are influenced by these results. The resulting output characteristics are not measured at wafer level. But



(a) (b)

Figure 5.29: Minimum and maximum output voltage of the digital (a) and analog (b) tunable reference voltage circuit. Both circuits are identical and no significant difference is expected.



(a) (b)

Figure 5.30: Chip-to-chip distribution of the slope of the linear regression fitted to the output characteristic of the tunable reference voltage (a). The histograms of the reference voltages for the digital and analog are added together. The output voltage distribution of the fixed band-gap based reference voltage for the analog and digital LDO are shown in (b).

the LDOs are tested and calibrated in the module production QA tests and results on this topic will are presented in chapter 6.

5.6.5 Summary

The fraction of chips failing is shown in figure 5.31 as a function of the tested features. The biggest influence on the yield have the cuts on the total number of failing columns and pixels. These are very

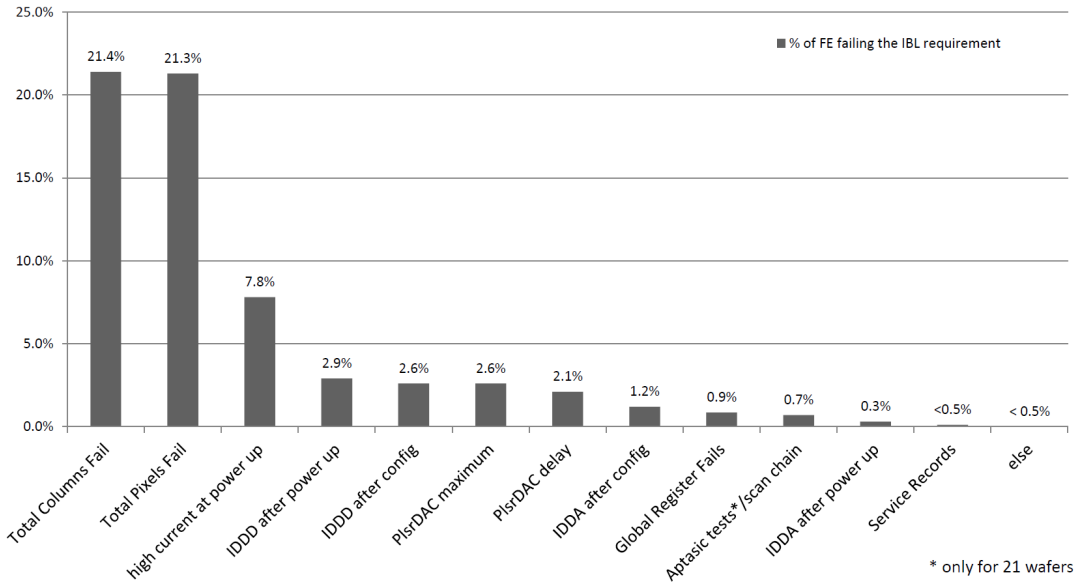


Figure 5.31: Fraction of chips failing per acceptance cut [52].

strict cuts that allow only 0.2% of the pixels to show any error in any test. The number of allowed pixels failing is inherited from the current ATLAS Pixel Detector production. The second largest amount of chips excluded from IBL production comes from high power consumption at various test stages. As a high current consumption is the only condition triggering an abortion of the test run the bin called ”high current at power up” with 7.8% of failing chips. Together with the bins ”IDDD after power up”, ”IDDD after config”, ”IDDA after config”, and ”IDDA after power up” which contain chips with completed probing runs but significantly high current consumption, the cuts on the power consumption exclude 14.8% of chips from IBL production. Note, that a chip can fail several of these cut flavors.
The mean yield of all 43 wafers tested for the IBL is $(61 \pm 2)\,\%$. The percentage of green chips per wafer is shown in figure 5.32, showing a coherent region of wafers with 46 % to 75 % of green chips. Three wafers show significantly low yield and one wafer has a yield as high as 83 % of green chips.

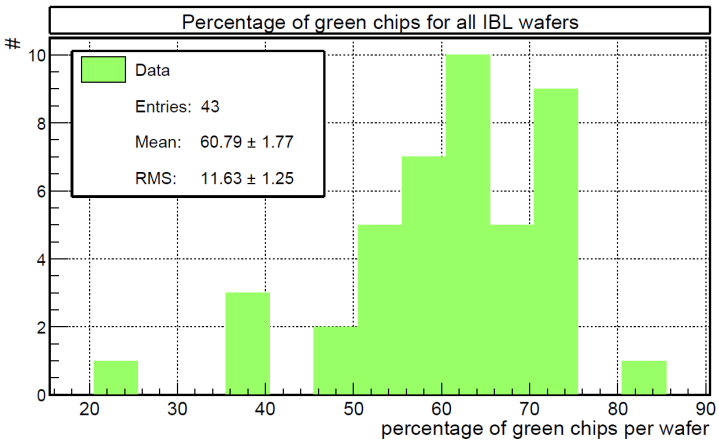


Figure 5.32: The yield per wafer distribution for 30 fully probed IBL wafers [52].

Chapter 6

Characterization and performance of IBL pixel modules

Prototype assemblies (FE-I4A readout chips connected to prototype sensors close to the production design, mounted on test printed circuit boards) using all three sensor flavors introduced in chapter 4.3 are built and irradiated to the IBL design fluence of $5 \times 10^{15} n_{eq} cm^{-2}$ using 26 MeV protons from the Karlsruhe Synchrotron and using thermal neutrons from a nuclear reactor in Ljubljana. The samples are un-powered and not cooled during the irradiation periods, as the target fluence is reached within a few minutes in both cases. Detailed pre- and post-irradiation characterizations of the prototype assembly performance in laboratory and test beam environment have been performed. A full performance validation is done on each module (FE-I4B readout chip with production design sensor and module flex) during the production QA test.

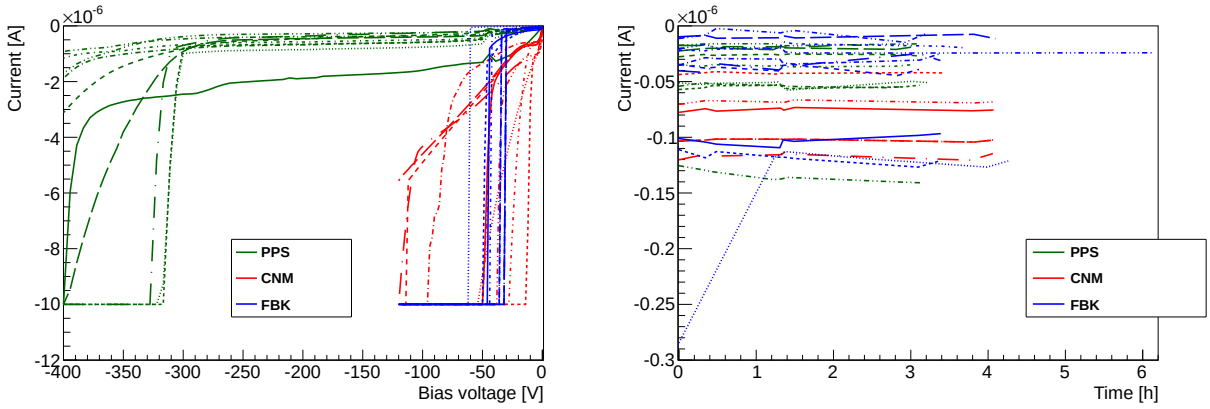
6.1 Performance measurements in laboratory environment

6.1.1 Sensor bias

The current as a function of the bias voltage is an important measure to qualify the sensor performance, before and after flip-chip as well as after module dressing. Any significant changes during the production steps indicate potential sensor damages and surface current paths. On un-irradiated modules, the measured current can be dominated by surface effects until the bias voltage exceeds the breakdown voltage. Therefore, the detection of the breakdown voltage is of major importance.
The expected breakdown voltage is significantly different for planar silicon and for 3D silicon sensors. The breakdown voltage of 3D silicon sensors is very low in comparison to planar, as shown in figure 6.1a. However, this is not a concern, because the operation voltage of the 3D silicon sensors is −20 V. All dressed IBL 3D modules must provide a breakdown voltage below −30 V to be accepted for stave loading. The planar modules have an operation voltage of −80 V and must withstand at least −150 V.
During the full module performance qualification of the IBL production the long term stability of the leakage current is also measured. The leakage current is measured at several time stamps. Randomly chosen example results for ten modules of each type are given in figure 6.1b. Additionally, the temperature is monitored at each time stamp and is stable. The leakage current fluctuations per module are in the order of 0.1 μA, except for one FBK module, on which the current settled after the first measurement point.

6.1.2 Absolute charge calibration

In the FE-I4A chip, no circuitry for direct measurement of the test charge injection capacitances is implemented. To achieve a good absolute calibration of the chip, the pulser DAC calibration as well



(a) (b)

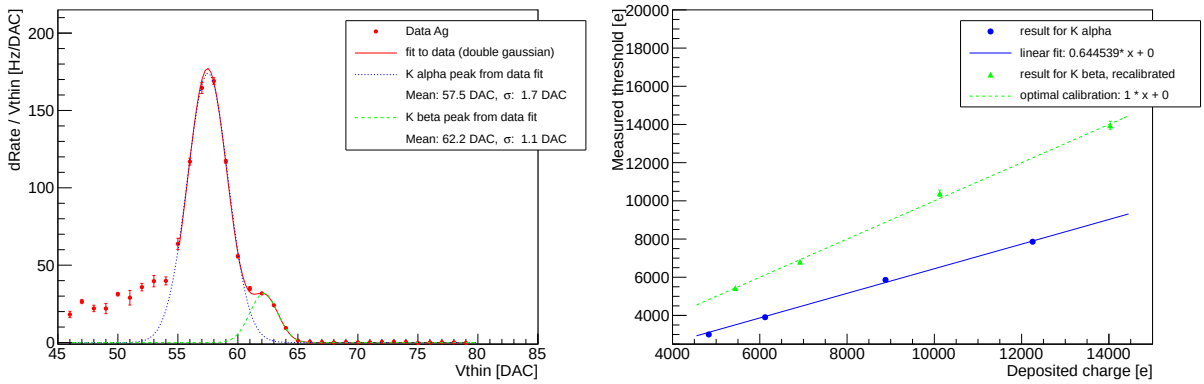
Figure 6.1: Measurement of the leakage current as a function of the bias voltage (a) for ten IBL modules of each sensor flavor. A current limit of −10 µA is used to protect the modules. The result of the long term leakage current stability measurement during the full module performance qualification at approximately −15 °C is shown in (b).

as the injection capacitance need to be known (see chapter 5.2). A method allowing to measure the injection capacitance without using the TOT information is developed and used on the first planar sensor prototype assembly.

The spectra of four x-ray sources are obtained by measuring the hit rate as a function of the threshold. The derivation of the resulting "inverted" S-shaped curve is the spectrum of each source. Figure 6.2a shows an example of the measured ^{47}Ag lines. A double gaussian fit is applied to the data points, the mean values of the fit are then correlated with the expected K_α and K_β line of the spectrum. This calibration is also performed using ^{42}Mo, ^{56}Ba and ^{65}Tb.

The measured thresholds at the mean value of the K_α line peaks using the design value for the injection capacitor is plotted as a function of the charge generated by the photons in the sensor as blue dots in figure 6.2b. A linear fit is applied and the injection capacitance can be calculated from the slope. The new calibration is then applied during the energy measurement of the K_β peak and plotted in figure 6.2b as green triangles. The dashed green linear function is not the result of a fit, but a linear function with the slope equal to one and without any offset, because this is what gives the correct calibration of the chip in this plot. Obviously the data achieved with the new calibration nicely fit the expectation. The injection capacitance when using both capacitors is measured to be 6.7 fF. The uncertainty of this measurement is expected to be in the order of 10 %. This result is in good agreement with the direct injection capacitance measurements on FE-I4B chips presented in chapter 5.

The achieved relative energy resolution of this method can be approximated from the width of the K_α peak. Converting the width of 1.7 DAC to the charge deposited in the sensor using the measured difference of the two peaks in figure 6.2a in DAC steps (4.7 DAC) and the well known energy difference of the K_α and the K_β line of ^{47}Ag (2.78 keV) results in a charge resolution of about 280 e. This is an improvement of more than an order of magnitude with respect to the energy resolution achieved using the analog hit information which is presented in chapter 6.1.6.

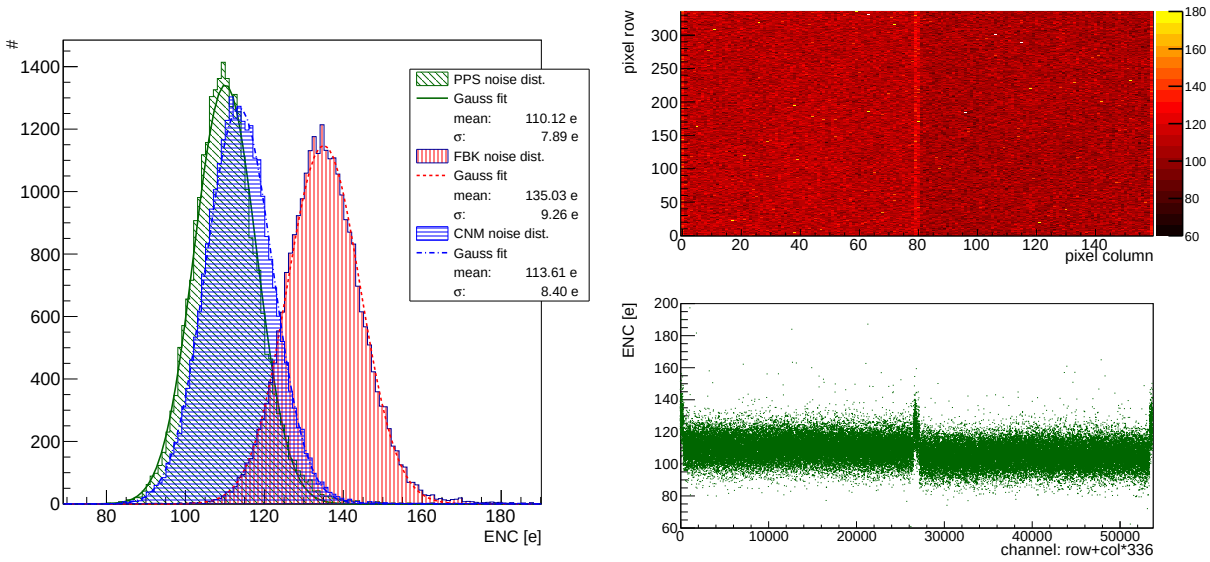


(a) (b)

Figure 6.2: The spectrum of Ag measured without using the analog hit information is shown in (a) and the measured peak energy in electrons using the design value for the injection capacitor in dependence of the charge generated in the sensor is given in (b). The measured peak energy using the re-calibrated injection capacitance is additionally depicted in (b).

6.1.3 Noise of IBL modules

The ENC of the module is expected to be influenced mainly by the capacitance at the input node of the preamplifier, which depends on the sensor type. Additionally, the ENC is affected by external influences such as flex circuit quality and power supply stability. No influence of the IBL powering mode using the on-chip LDOs is expected [55]. Figure 6.3a shows pixel-to-pixel ENC distributions for a typical sample of all three module types using the initial tuning for the IBL operation of each module. Only a single readout chip is shown for the PPS module to achieve a histogram with a similar number of entries. The ENC for all types is properly gaussian distributed. The mean ENC of the FBK module is with 135 e significantly higher than the comparable mean ENC of 110 e for a PPS module and 114 e for the CNM. The width of all three distributions is comparable in the order of 8 e to 9 e.
The ENC of the FE-I4 scales approximately linearly with the detector capacitance (as shown in chapter 5.3). A simple linear approximation using the detector capacitances measured with the PixCap chip [50] for the planar sensor (approximately (110 ± 4) fF [50]) and the CNM sensor (approximately (170 ± 2) fF [50]) and the mean ENC values of the three sensor types results in a detector capacitance of about (200 ± 8) fF for the FBK module. The given uncertainty of is the error propagation of the measurement uncertainties and does not include the uncertainty of the approximation itself.
A color coded ENC map for each pixel of a PPS double chip module and a scatter plot is presented in figure 6.3b. The noise is uniformly distributed over the full pixel matrix. The higher detector capacitance of the long pixels at the edges of the sensor and in between the two readout chips can be observed by the slightly increased noise of the corresponding pixels. The mean ENC of the edge pixels is 126 e and 120 e for the pixels in-between the readout chips. The same approximation as for the FBK module gives a detector capacitance of approximately (188 ± 8) fF for the 500 µm long pixels at the module edges and about (179 ± 8) fF for the pixels in-between the two readout chips with a length of 450 µm. Considering the size increase by a factor of about two of these pixels and subtracting the influence of the bump pad (11.6 ± 0.1) fF, see chapter 5.3), the measured detector capacitance of the long pixels is in good agreement with the expectation.



(a) (b)

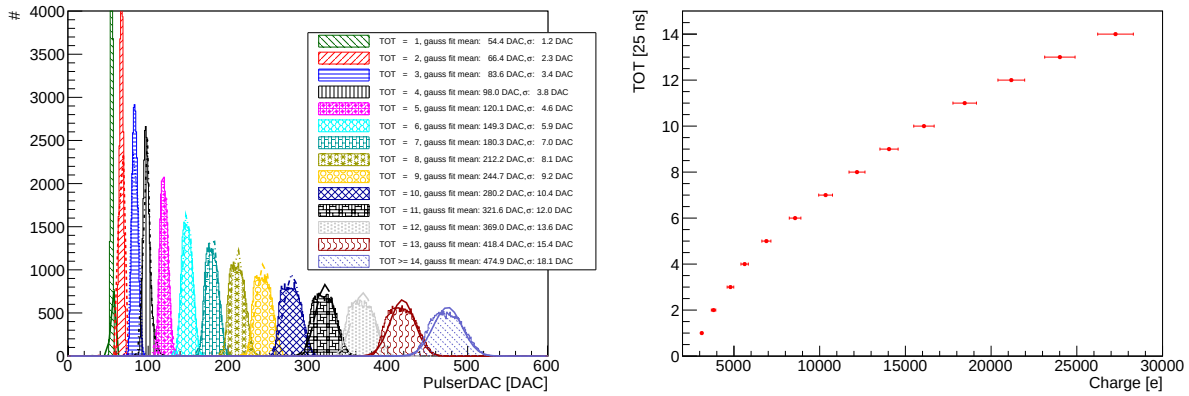
Figure 6.3: Pixel to pixel noise distributions of the three IBL module flavors (a). The noise is measured at approximately −15 °C after the tuning procedure. The PPS distribution contains the FE0 distribution only. The color coded noise map and scatter plot of the PPS module (b) contains the noise of all 53760 pixels. The 500 µm long edge pixels as well as the 450 µm long pixels between the readout chips are visible.

6.1.4 TOT to charge calibration

The limited available analog hit information due to the low number of TOT bits is a serious difficulty for the TOT to charge calibration. The simple conversion measurement used on the current ATLAS pixel modules (explained in detail in [13]) measures a TOT histogram at pixel level as a function of the injected charge. The result is then used to fit a conversion function. This method does not result in a satisfactory TOT to charge calibration using FE-I4 based modules due to the large TOT bins.
A new calibration method is developed that measures injected charge histograms in units of the PulserDAC for each TOT. For each pixel the PulserDAC value is stored for which the pixel responds with the chosen TOT. This results in a PulserDAC histogram as shown in 6.4a. The mean value and the width of the PulserDAC distributions are converted to charge and used as look up table for the TOT to charge calibration (see figure 6.4b). This new procedure benefits from the smaller step width of the injection circuitry (in terms of injected charge) in comparison with the large charge steps of the TOT information. This measurement is performed on each IBL module and the result is stored for each individual pixel. The source scan performed on each IBL module targets the measurement of the bump connectivity and not the charge calibration. The individual TOT information per pixel is not stored to limit the amount of recorded data. Therefore, here this conversion is averaged over the whole chip to be used in the source scan presented in chapter 6.1.6.

6.1.5 Hit detection timing

During detector operation, the IBL modules will be read using only a one-bunch-crossing-wide Level-1 trigger. This mode translates to a sensitive time of only 25 ns. Thus the hit timing, which is significantly influenced by the time-walk as discussed in chapter 3.3.2, is of major importance for the IBL operation.



(a) (b)

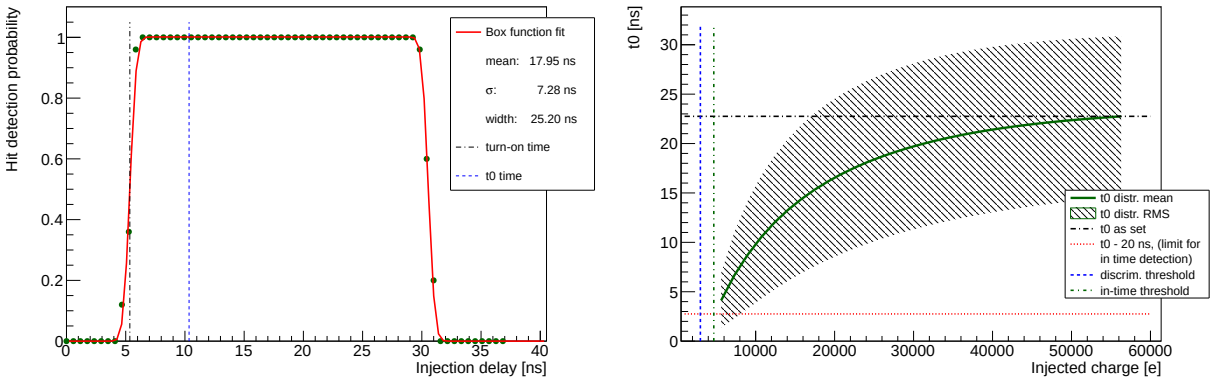
Figure 6.4: TOT to charge calibration. The mean and sigma of the pixel-to-pixel PulserDAC distributions (a) are used to obtain a TOT to charge calibration function (b).

The FE-I4 has an adjustable on-chip injection delay circuitry, which is used to tune the charge injection timing. This circuitry adjusts the injection timing globally and therefore the injection delay must be adjusted in a scan algorithm for the whole chip. This scan measures the hit detection probability as a function of the delay setting for a large injected charge and one bunch crossing read-out. This results in a box-shaped function, as presented in figure 6.5a. The detection turn-on time is defined by the 50 % hit detection probability. The difference between detection turn-off time and and detection turn-on time is known to be 25 ns and this is used by an automated algorithm to calibrate the step-width of the delay circuitry. The step-width of this particular FE-I4 is approximately 0.58 ns. The mean turn-on time of the full pixel array is measured and the injection time (t_0) is fixed to the mean turn-on time plus a safety margin of 5 ns.

Measuring the t_0 time as a function of the injected charge reveals the time-walk effect: the smaller the injected charge, the earlier the t_0 is measured. This is shown in figure 6.5b.

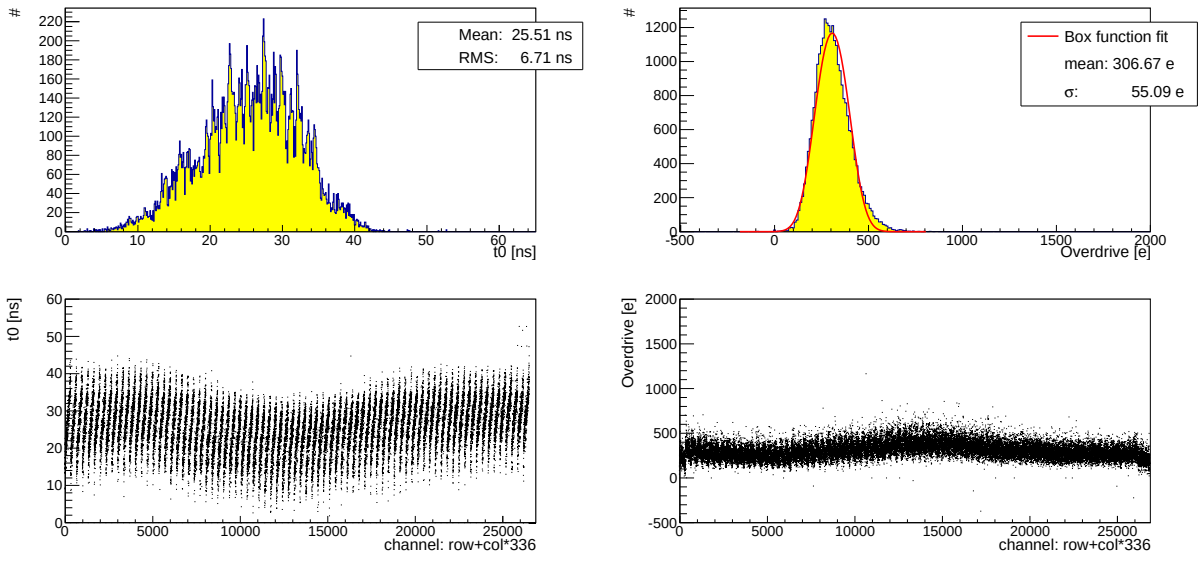
The time-walk can be measured in electrons and is defined as the charge above the discriminator threshold, at which the t_0^{tw} is measured within the same bunch crossing as the t_0 at the maximum charge. Thus, the t_0^{tw} is the t_0 minus 20 ns. All hits with a charge above the discriminator threshold plus the time-walk charge will be detected within the same bunch crossing. This threshold is commonly called in-time threshold.

The measured t_0 distribution is not uniformly distributed over the pixel array (figure 6.6a). While careful design effort is taken to ensure a synchronous trigger arrival in all four pixel digital regions, the injection signal is simply routed from pulser position inside the chip periphery to the bottom of the columns, and then upwards in the columns. In the large FE-I4 chip travel paths result which can be from a few mm to 3 cm long depending on pixel position inside the array. This leads to significantly different injection times. The signal distribution from the pulser through the periphery results in a bow visible in the scatter plot of figure 6.6a. The pulser circuitry is located close to the columns showing the minimum of the bow. Additionally, the signal travel time upwards the columns results in the column pattern within this bow. This injection time non-uniformity limits the precision of the time-walk measurements using the internal charge injection circuitry. External charge injection with precisely known hit time, as achieved by laser setups or source setups with an external trigger system, is favorable for a precise time-walk measurement.



(a) (b)

Figure 6.5: (a) Single pixel hit detection probability during a t_0 scan. Analog injections with high charge are performed as a function of the on-chip injection delay. A single consecutive bunch crossing is read. The t_0 is set to the turn-on delay plus 5 ns. (b) t_0 as a function of the injected charge for the full matrix. The effect of the time-walk for small charges is visible.



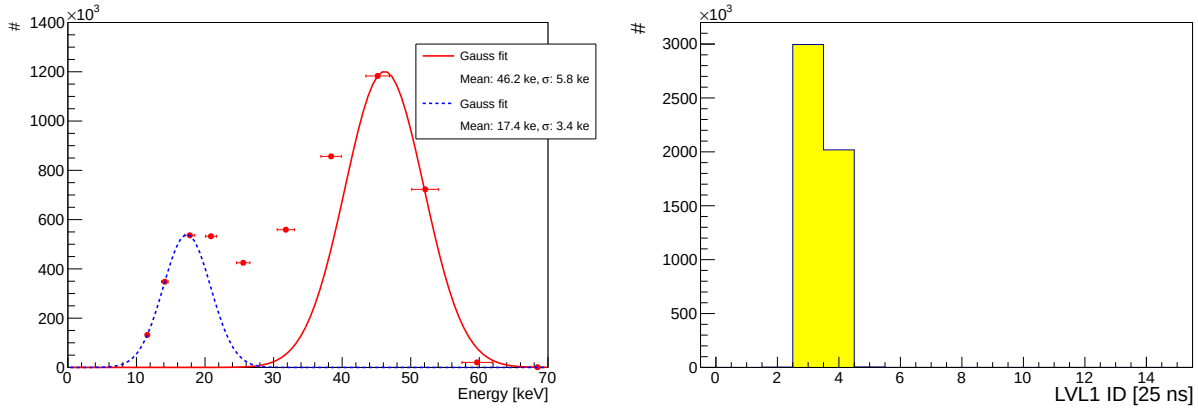
(a) (b)

Figure 6.6: Pixel to pixel t_0 distribution of the full pixel array (a) and the overdrive distribution (b).

The in-time threshold can also be conveniently measured using the normal threshold scan algorithm with single Level-1 trigger read-out after careful t_0 adjustment. The time-walk measurement as presented in 6.5b is challenging on FE-I4 based modules due to the small time-walk charge in the order of only a few hundred electrons. No significant difference between the time-walk charge measured as presented in 6.5b, and the pixel-to-pixel difference between the in-time threshold and the discriminator threshold (overdrive) is observed on FE-I3 based modules [13]. No change in this behavior is expected in FE-I4 based modules. Therefore, the time-walk is measured in the following using the overdrive. An overdrive distribution is given in 6.6b. The mean overdrive is 307 e with a standard deviation of 55 e. As the t_0 can not be adjusted at pixel level, the discussed injection time non-uniformity results in an inverted pixel position dependency of the overdrive. This is expected, because an earlier injection with respect to the t_0 time results in an increased overdrive.
The small hit discrimination circuitry (see chapter 5.4) can also correct for time-walk, if the hit is detected within the next bunch crossing and has a TOT equal or less than two. As hits with an overdrive of less than 1500 e will be assigned a TOT of two or less at this FE-I4 operation point (figure 6.4b), the measured overdrive can be compensated by the small hit discrimination.

6.1.6 Source test

A source scan is the final test assuring the possibility for each individual pixel to detect hits depositing charge in the sensor. An ^{241}Am source is used on each individual IBL module to generate hits in the sensor. The self-trigger mode of the FE-I4 is used for triggering. The main goal of the scan is the bump-connectivity validation and no clustering is used, because it is not needed for this purpose. A typical



(a) (b)

Figure 6.7: (a) Charge spectrum of the ^{241}Am source scan. (b) hit timing information (within a time window of 16 times 25 ns).

^{241}Am spectrum and hit timing distribution is shown in figure 6.7. Two peaks can be distinguished in the spectrum in figure 6.7a. The uncertainty on the charge is dominated by the width of the PulserDAC distributions, as shown in figure 6.4a, and this is drawn as error bars here. Additionally, the uncertainty of the charge injection circuitry calibration, as discussed in chapter 5.2, must be taken into account. A gaussian is fitted to both peaks. The measured charge of the peak associated to the 60 ke peak of the americium spectrum using the calibration presented above is (46 ± 6) ke. This result is slightly lower than expected. The 13.9 ke peak of the americium spectrum is nearly within the error of the measured

peak at $(17.4 \pm 3.4)\,\mathrm{k}e$. A significant improvement is expected with a charge calibration at pixel level and sophisticated clustering algorithms.
The most important result of the source scan for the IBL module production is the occupancy per pixel. The occupancy map of a PPS double chip module is shown in figure 6.8. The source is placed at

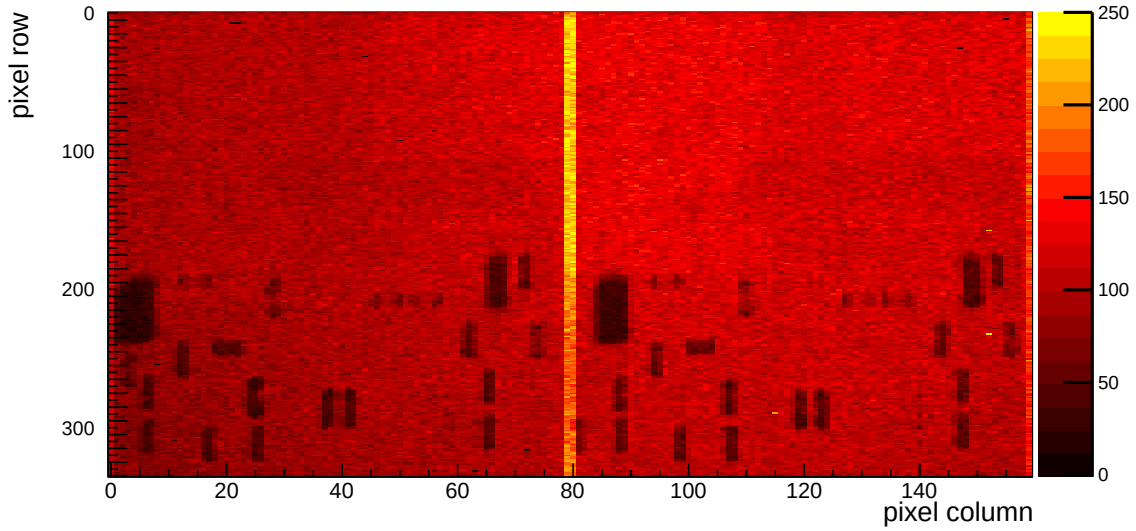


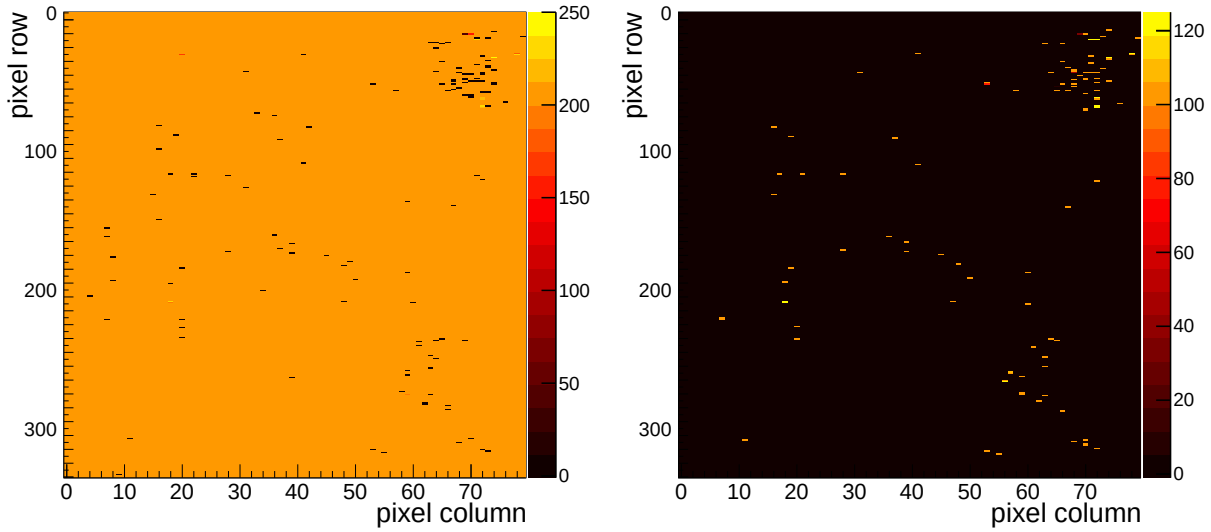
Figure 6.8: The occupancy per pixel displayed as a color coded map of the module. A decreased occupancy is expected for pixels below components on the flex and an increased occupancy is expected in long pixels.

the center of the module and illuminates the full module. The long pixels in between the readout chips as well as at the edges of the sensor are expected to have about twice the occupancy of the direct neighbors. This is well reflected in the map. The areas with decreased occupancy correlate with the passive components soldered on the module flex (to be compared to figure 4.14). A pixel with failing bump connectivity does not record any source hit and noisy pixels show an increased occupancy. The number of pixels in this module that show an occupancy below 5 % or above 450 % of the mean occupancy per pixel is only 15. Thus the bump connectivity yield of this particular module is above 99.97 %.

6.1.7 Crosstalk

Coupling between pixels can result in a hit detected in a neighboring pixel. The coupling can be either capacitative or ohmic. A scan algorithm injecting charges in the two neighboring pixels (in the long pixel direction) of the read-out pixel measures the crosstalk. The crosstalk measurement as a function of the injected charge results similarly to the threshold measurement in the crosstalk threshold. Commonly, the crosstalk is expressed (per pixel) in the fraction of charge flowing to the neighboring pixel. This is given by the fraction of the discriminator threshold and the crosstalk threshold. The maximum charge that can be injected using the internal test charge injection circuitry is in the order of 55 ke. Thus, the sensitivity of the crosstalk measurement is limited. For a threshold of 3000 e, crosstalk above 5.5 % can be measured. If no bump failure (nor any other type of failure) is present, the crosstalk cannot be measured using this method on IBL modules.
The crosstalk measurement is an important measurement for failure detection. While the source scan occupancy reveals open bump connections, shorted neighboring pixels result in one pixel with high

crosstalk (up to 100 %) and another pixel that is unresponsive to test charge injections at the preamplifier, because if two pixels are shorted, the charge at the input node of the preamplifier of one of the pixels flows into the second pixel. A serious flip-chip process issue observed on the first three flip-chip batches of the IBL production is detected due to this effect. Detailed investigations prove a low ohmic contact between neighboring pixels although the bump bonds themselves are not shorted (proven by x-ray images). One of the two affected pixels shows crosstalk of 100 %, while the other is unresponsive,



(a) (b)

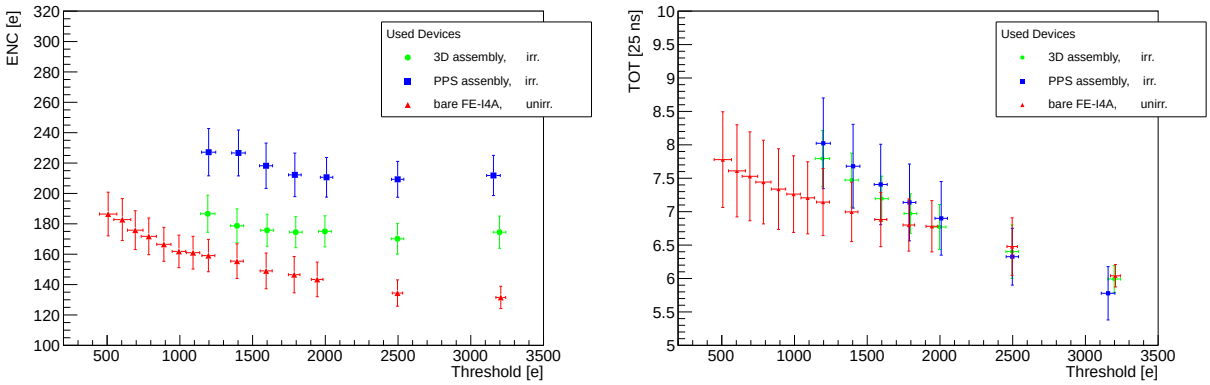
Figure 6.9: Occupancy maps used to indicate shorted pixels. The unresponsive pixels in the analog test (a) correlate with neighboring pixels with high occupancy in the crosstalk test (b).

see figure 6.9.
The investigation of this issue has been done in the framework of this thesis. The main focus is the performance characterization of the IBL modules and thus the issue is not described in detail here. From flip-chip batch four on the flip-chip process is changed. Nearly all modules accepted for the IBL production come from batch four and later. Thus modules from batch one to three are not included in the module-to-module distributions of the IBL production tests presented in chapter 6.3.

6.1.8 Low threshold operation

Low threshold operation is one of the key issues helping to achieve good hit detection efficiencies on highly irradiated sensors, when the amount of effective charge carriers seen by the preamplifier decreases. Lowering the threshold has the drawback of increasing the amount of fake hits (also called noise hits). A high amount of noise hits decreases the tracking performance of the detector. In the current ATLAS pixel detector, all pixels with a noise hit probability per 25 ns (noise hit occupancy, NOcc) higher than 10^{-7} are masked. Detailed studies are done to investigate the minimum operational threshold with a good compromise between hit detection efficiency and NOcc per pixel . In these studies prototype assemblies with 3D silicon and planar silicon sensors connected to FE-I4A readout chips, as well as a bare FE-I4A readout chip as reference, are used. Both prototype assembly flavors are irradiated to $5 \times 10^{15} n_{eq} cm^{-2}$ using 26 MeV protons, while the bare FE-I4A reference is un-irradiated.

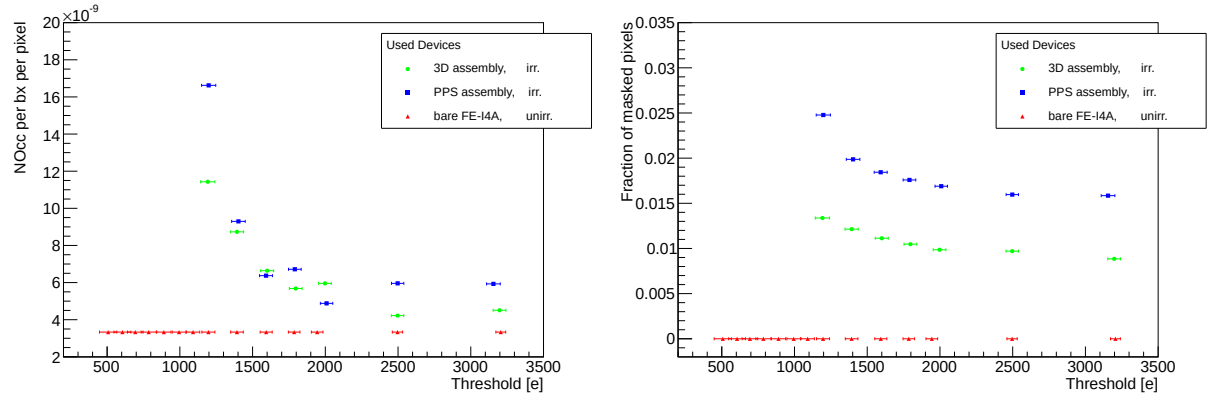
The ENC in low threshold operation is studied. Figure 6.10a shows a slight increase of the measured electronics noise when going down with threshold. Note, that due to inefficient cooling the irradiated



(a) (b)

Figure 6.10: The electronics noise (a) and TOT in units of 25 ns (LHC bunch crossing clock) in low threshold operation (b).

planar device is operated with a very high leakage current of 3 mA explaining the high noise of this device. The increase for lower thresholds is observed in the un-irradiated bare IC also, which is consistent with the influence of the operation point of the readout chip on the noise (see chapter 5).
Figure 6.11a shows the threshold dependence of the NOcc for both module flavors and for the un-irradiated bare chip. The NOcc is measured sending 5×10^8 random triggers to the chip, which correl-

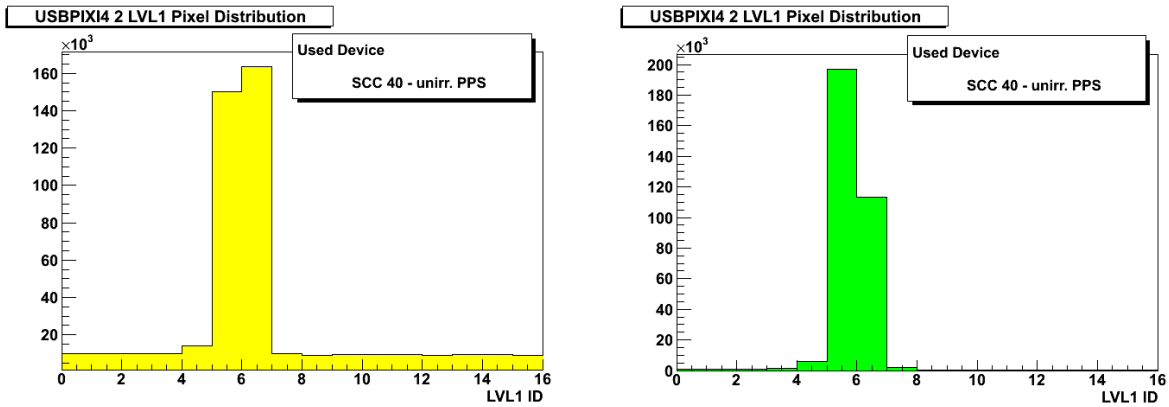


(a) (b)

Figure 6.11: Mean noise hit probability per 25 ns (a) for different thresholds. Pixels with a noise hit probability above 10^{-5} are excluded from the analysis. The fraction of masked and excluded pixels (b) as a function of the threshold.

ates to a sensitivity down to 3.34×10^{-9} noise hits per pixel and 25 ns. All digitally problematic pixels have been masked offline, whereas all pixels showing an NOcc above 10^{-5} have been masked in analysis to avoid domination of single pixels with high NOcc in the calculation of the mean NOcc. The total

amount of masked pixels as a function of the threshold is depicted in figure 6.11b. The 1-2 % unresponsive pixel fraction in the irradiated modules at high threshold is seen independently from the sensor type used. Investigations presented in chapter 6.1.9 prove that this effect is caused by the very high dose in the Front-End electronics. To achieve the high fluence in the sensor using 26 MeV protons the chip has absorbed a total ionizing dose larger then 800 Mrad, which is well above the design tolerance of the chip of 300 Mrad. Note, that for modules irradiated with neutrons the amount of unresponsive pixels is not increased with respect to the performance before irradiation.
If the pixels showing a high number of noise hits do not change with time (fixed pattern noise), these measurements prove that the chip can be operated independently of the sensor technology with a very low noise hit probability of approximately 10^{-8} down to thresholds in the order of 1600 e, without masking a large amount of pixels. Figure 6.12a shows the hit timing information, as obtained at a test



(a) (b)

Figure 6.12: Hit timing information (within a time window of 16 times 25 ns) before (a) and after (b) applying a noisy pixel mask. Obtained at a test beam using 180 GeV pions.

beam at CERN without a noisy pixel mask applied (see also chapter 6.2). Clearly the large peak of hits recognized with fixed timing relation to the particles crossing the telescope is visible, as well as a background of noise hits without fixed timing. A noisy pixel mask which disables all pixels with a noise hit probability higher than 10^{-5} obtained using a procedure similar to the measurement used for the data in figure 6.11 is applied for data acquisition in figure 6.12b. The background related to the noise hits disappears, which proves that this procedure allows operation of the module with very low noise hit probability at low thresholds.

6.1.9 Unresponsive pixels after heavy irradiation

A large fraction of unresponsive pixels is observed on irradiated prototype assemblies independent of the sensor flavor. The unresponsive pixels are only observed on samples irradiated at the Karlsruhe irradiation facility using 26 MeV protons and not on samples irradiated with neutrons. In proton irradiation, the total ionizing dose absorbed by the read out chip is much higher than during neutron irradiation. A detailed study of the analog readout chip parameter space shows, that only the feedback current setting of the second stage amplifier influences the number of unresponsive pixels. Figure 6.13 presents the fraction of unresponsive pixels as a function of the second stage feedback current setting (Amp2Vbpf, 8bit DAC) for two prototype assemblies. Both assemblies are irradiated to $5 \times 10^{15} \mathrm{n_{eq}cm^{-2}}$ at Karlsruhe and both samples show a steep decrease of the number of unresponsive pixels with increasing feedback

current setting. The decrease is independent of the test hit injection type, i.e. analog or digital. This

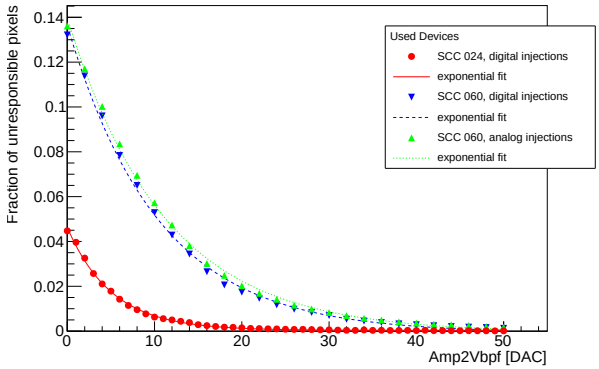


Figure 6.13: Fraction of unresponsive pixels as a function of the feedback current setting of the second stage amplifier. Both samples are irradiated to 5×10^{15} $1\,n_{eq}cm^{-2}$ with 26 MeV protons, which translates to a TID absorbed by the readout chip above 800 Mrad.

behavior is explained by a radiation induced increase of the leakage current in the second stage amplifier feedback current transistor. The leakage current increase results in a shift of the Direct Current Voltage Output (DC-level) of the second stage amplifier, which is directly connected as input to the comparator. If the output voltage exceeds the threshold voltage, the pixel is stuck and no hits can be detected, neither at the preamplifier input (analog injections), nor at the comparator output (digital injections). Adjusting the feedback current DAC compensates the leakage current and thus lowers the DC-level of the second stage amplifier output. The pixel distribution density in the DC-level parameter space of the second stage amplifier can be assumed to be gaussian. A linear adjustment of the feedback current results in a linear shift of the DC-level. Due to the gaussian pixel distribution density the number of pixels that are compensated by this linear shift below the discriminator threshold increases exponentially. So the number of unresponsive pixels decreases exponentially with a linear increase of the feedback current.
No performance degradation is observed with increased second stage feedback current and the default setting is chosen to Amp2Vbpf equal 50 based on this result.

6.2 Performance measurements in test beam environment

Several detector characteristics such as the in-pixel hit detection efficiency, the spatial resolution and inter segment charge sharing probability are measured using the well defined conditions in a test beam environment. Several IBL test beam campaigns at DESY and CERN are used to characterize the different IBL module flavors. During all campaigns the EUDET telescope and the EUDAQ software framework [56] is used. A detailed description of the setup can be found in [36]. The reconstruction and analysis of the data obtained in these test beam campaigns is not in the scope of this thesis, but the preparation and operation of all test beam campaigns was performed with a significant contribution of the author. This includes the integration of the USBpix system in the telescope framework, both software and hardware, the telescope and Device Under Test (DUT) build-up and the operation of the full system during data taking. The results presented here are taken from [36].
The DUTs are characterized with different incident angles of the beam particles. Here, results with 0° and 15° incident angle are presented. Due to the tilt of the IBL staves, an incident angle of 0° is very improbable during experimental operation, but the inefficiency sources are resolved much better with

vertical incidence of the beam. The results presented with a tilt of 15° with respect to the beam direction mimic the tilt of the IBL staves in ϕ, and thus this tilt is in the short pixel direction.

6.2.1 Cell efficiency

The in-pixel efficiency is studied to understand the inefficiency sources within the pixel cell. To increase the statistics, all pixel cells in the beam are added together for each sample. This assumes the pixels behave similarly. Figure 6.14 shows the in-pixel efficiency for a planar and a CNM 3D prototype

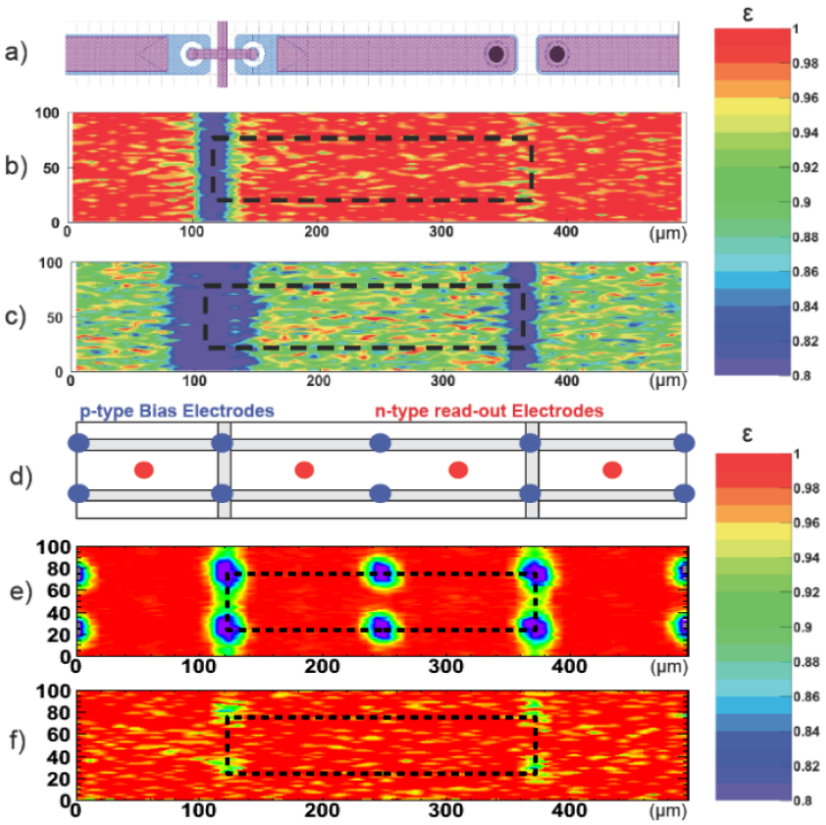


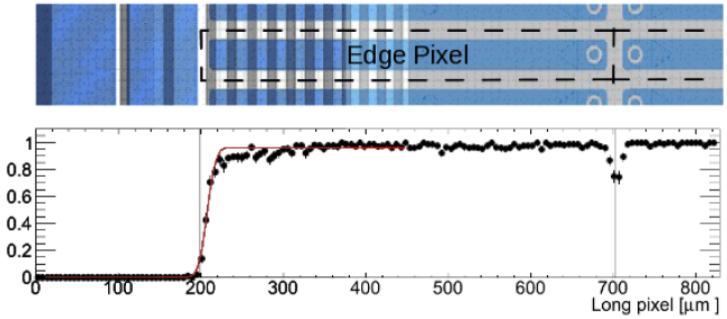
Figure 6.14: Cell efficiency maps: a) lithography sketch for PPS, b) and c) 2D efficiency maps for PPS 61 at a bias voltage of −1000 V and at −600 V using 15 degree inclined tracks, d) lithography sketch for 3D, e) the 2D efficiency map for the CNM 81 module using normal incident tracks and f) the 2D efficiency map for the CNM 34 module using 15 degree inclined tracks. Both the CNM 34 and CNM 81 are operated at a bias voltage of −160 V. All dimensions are in microns. [36].

assembly. In a) the lithography sketch of the PPS sensor design is drawn in the same scale as the inefficiency maps obtained with 15° tilt in ϕ and a bias voltage of −1000 V b) and −600 V c) on an irradiated planar sample. The bias grid implants change the field configuration and result in an area with decreased efficiency of ∼ 80 % with both bias voltages. Tracks with no incident angle in the long pixel size (η-angle) appear in IBL in the central modules only, and the inefficiency due to the bias grid implants disappear at small track angles in η (not presented here). The measured mean efficiency over the whole pixel area is 96.9 %. The spots with decreased efficiency visible in the efficiency map of the irradiated 3D sample at 0° in e) correlate with the p-type bias electrodes sketched in d), and only appear for tracks penetrating the p-doped pillar, because the pillars itself are empty and no charge is generated.

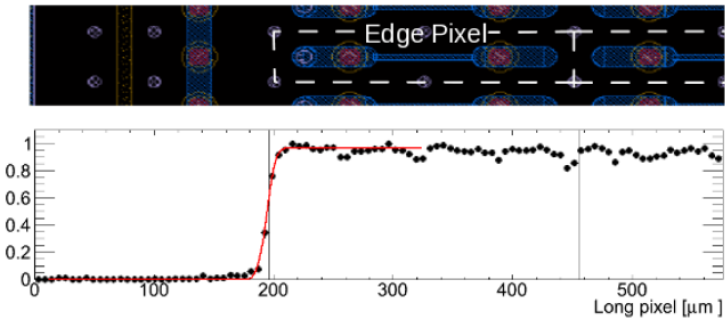
This efficiency loss is drastically reduced as soon as the tracks do not pass the pillar at the full sensor thickness, as measured with 15° incident angle.

6.2.2 Edge efficiency

The inactive edge size is one of the major and most challenging module characteristics (see chapter 4.1). The efficiency of the sensor edge is measured mounting the edge of the module in the center of the telescope sensitive region and illuminating the edge with the beam. Plotting the efficiency projection in the short pixel direction (y-direction) as a function of the long pixel direction (x-direction) results in a S-shaped efficiency curve. The inactive edge size is defined as the distance from the cutting edge of the sensor to the position with 50 % hit detection efficiency. Figure 6.15 shows the result of this



(a)



(b)

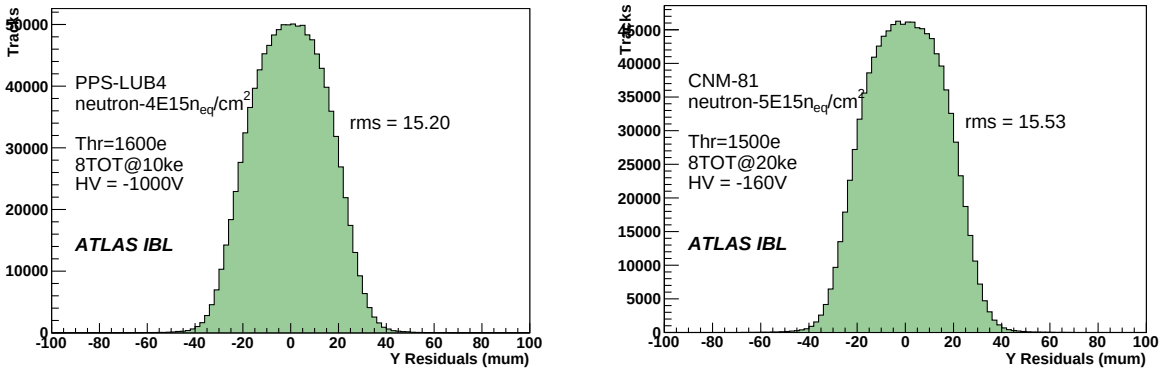
Figure 6.15: Edge efficiency measurements following irradiation. (a) A PPS edge pixel photo-lithography drawing with the efficiency projection of the PPS L2 module at a bias voltage of −1000 V. (b) A 3D CNM edge pixel photo-lithography drawing with the 1-dimensional efficiency projection of the CNM 34 module at a bias voltage of −140 V. The CNM 34 module is not fully biased in this measurement [36].

measurement for an irradiated planar and 3D sample. In figure 6.15a a sketch of the edge pixel design as explained in chapter 4.3.1 is drawn above the measured efficiency as a function of the x-direction. The inactive edge size is measured to be approximately 200 µm [36] and well below the specifications of the maximum 450 µm edge for the double chip samples. The edge efficiency of the CNM 34 sample shown in figure 6.15b also fulfills the requirement of ≤ 225 µm and is also approximately 200 µm [36].

6.2.3 Spatial resolution

The spatial resolution in the short pixel direction is expected to be 14.43 µm using equation (3.3). This neglects the charge sharing between the pixels, the threshold, as well as the incident angle. The spatial

resolution is measured in the test beam by the RMS of the residual distribution (difference between the reconstructed hit position and the measured hit position in the DUT). The charge sharing between neighboring pixels in combination with the analog hit information (TOT) is used to improve the position measurement in the DUT in case of multi-hit clusters. The hit position within the cluster is then calculated using first linear charge weighting and afterwards the eta algorithm [14].
Figure 6.16 contains the residual distributions in the short pixel direction of the planar sample PPS L4 and the 3D sample CNM 81 for the 15° incident angle mimicking the IBL stave tilt. Both samples are



(a) (b)

Figure 6.16: (a) Residual distribution of the PPS L4 module for all-hit clusters in the short pixel direction, for 15 degree beam incident angle and for a threshold setting of 1600 e. (b) Residual distribution for the CNM 81 module at the same incident angle and a threshold setting of 1500 e. The measured RMS resolution is similar for both the planar and 3D module types. [36].

neutron irradiated. The spatial resolution of both samples is approximately 15 µm [36]. This is in agreement with the simplified expectation of 14.43 µm. This analysis uses a simple clustering algorithm. A significant improvement of the spatial resolution is expected with the neural network based clustering used in ATLAS that is also foreseen for the IBL operation.

6.2.4 Summary

The hit efficiency of the DUT is defined by the number of reconstructed tracks with a matching hit in the DUT divided by the total number of tracks through the sensitive region of the DUT. A hit is considered as matching if the hit is detected in one of the eight pixels surrounding the pixel at the reconstructed hit position. Additionally, a matching hit in at least one of the simultaneously tested DUTs is required to suppress fake tracks. Noisy or known unresponsive pixels (see chapter 6.1.9) as well as the surrounding eight pixels are excluded from the analysis to assess the intrinsic effect of the radiation dose.
Table 6.1 summarizes the mean hit detection efficiency of all module flavors. The mean efficiencies of the PPS sample is close to 100 %, before irradiation. The 3D sensors show small efficiency losses due to tracks passing directly through the electrodes. The CNM sample by far exceeds 99 %, and the tested FBK 13 sensor nearly achieves 99 % hit detection efficiency. After the expected IBL end of lifetime fluence of $5 \times 10^{15} \mathrm{n_{eq}cm^{-2}}$ the PPS samples show an efficiency only slightly below 98 %, and the 3D samples exceed 98 % mean efficiency at both incident angles.
The presented results prove that all three IBL module flavors fulfill the major requirements: a geometrical inefficiency below 2.2 % and a hit detection efficiency in the sensitive region above 97 % until the

Sample ID	Bias voltage	Incident angle	Irradiation facility	Dose	Mean hit efficiency	Threshold
PPS 40	−150 V	0°	-	-	99.9 %	2700 e
PPS L4	−1000 V	0°	Lubljana	$5 \times 10^{15} n_{eq} cm^{-2}$	97.9 %	1600 e
PPS 60	−940 V	15°	Karlsruhe	$5 \times 10^{15} n_{eq} cm^{-2}$	97.7 %	1600 e
CNM 55	−20 V	0°	-	-	99.6 %	1600 e
CNM 34	−160 V	0°	Karlsruhe	$5 \times 10^{15} n_{eq} cm^{-2}$	98.1 %	1500 e
CNM 34	−160 V	15°	Karlsruhe	$5 \times 10^{15} n_{eq} cm^{-2}$	99.0 %	1500 e
FBK 13	−20 V	0°	-	-	98.8 %	1500 e
FBK 87	−150 V	15°	Karlsruhe	$5 \times 10^{15} n_{eq} cm^{-2}$	98.2 %	1500 e

Table 6.1: Summary of the mean hit detection efficiency during IBL beam test campaigns. A selection of results published in [36] is presented.

IBL end of lifetime.

6.3 Production qualification

Similarly to the wafer level production QA of the readout chips, the performance of each completely dressed IBL module is tested in great detail and automatically analyzed. Again, the test routine concentrates on calibration parameters, functionality tests at global as well as at pixel level and performance measurements. In contrast to the wafer level production QA, the module production QA is a three stage test program. It consists of the

1. Assembly test: this test is called ASSY in the following and is a short module test at room temperature right after the assembly of the module. The goal of the ASSY test is to determine and reject non operational modules as well as modules with severe bump bonding failures. The modules rejected in the ASSY test are not tested further to save testing time.

2. Thermal stress procedure: a thermal stress period consisting of ten temperature cycles between −40 °C and 40 °C with a wait-time of one hour at each temperature. The module is not operated during this procedure.

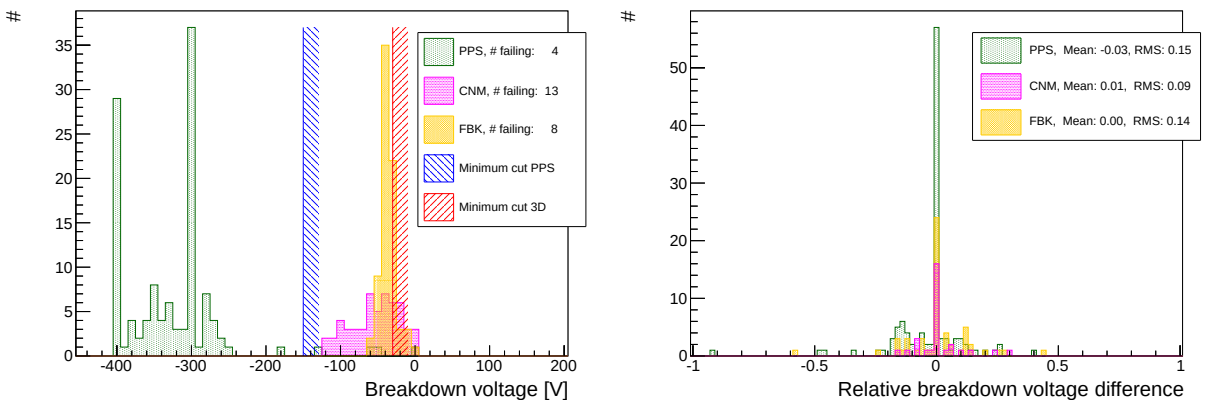
3. Final qualification test: this test stage is called FLEX in the following and is the final module performance test which is used for the module selection and ranking. The FLEX test is the full module performance measurement, including low threshold operation tests and a high statistics source test.

The module production QA is performed in equal shares at the two module dressing sites Bonn and Genoa right after the module dressing. The test setups at both sites are similar and consist of USBpix systems and several dedicated extension cards. These extension cards are custom developed high-voltage switcher boards and switcher matrices for the low voltage measurement devices. Additionally, an adapter printed circuit board (PCB) in a mixed PCB and flex technology is developed to achieve a simple and reliable connection to the test connector on the module flex, and a custom made probe needle card is used for the voltage measurements on the module flex.
At both sites, the modules are tested in batches of four modules that are connected at the same time. All modules are powered and operated simultaneously to gain operation time, but the modules are tested

one after the other. The same test routines are also used in Bonn and Genoa and no difference in the yield or any of the test results is observed. Thus, the test results of all modules, independent from the production site, are summarized. At the time of writing, the module production QA is ongoing. Results for all modules after the change of the flip-chip process (batch 4) until the time of writing (batch 10) are summarized here.
The analysis and cut program used for the wafer level production QA of the readout chips is inherited and adapted for the module production QA. The cut strategy described in chapter 5.6 is not changed for the module production, but several additional analyses are implemented.

6.3.1 Sensor characteristics

The current as a function of the sensor bias voltage is measured at both, ASSY and FLEX test stage. The breakdown voltage is used to qualify the modules in this test. Due to the different shape of the current characteristics, the result of each module is checked by the operator and not by an automated algorithm. The breakdown voltage differs for all three module flavors (figure 6.17a). The operation



(a) (b)

Figure 6.17: The module-to-module distribution of the breakdown voltage (a). The current voltage characteristics is measured at room temperature and the breakdown voltage is estimated by the user. The relative difference of the breakdown voltage measured at room temperature and at −15 °C is shown in (b).

voltage of the two 3D module types is −20 V, hence all 3D modules with a breakdown voltage below −30 V are rejected.
The sensor test procedure at wafer level is significantly different for the CNM and the FBK modules. An additional process step is used on the FBK modules to qualify the sensors at wafer level. A metal layer is applied to connect the pixel implants to GND, before the sensor is tested. After the test this metal grid is removed as this connection would be a short to all pixels. The CNM sensor characteristics is tested at wafer level using the guard ring as GND contact. The drawback of this method is the insensitivity to failures in the pixel array. Thus, the correlation between the breakdown voltage measurement at wafer level and on dressed modules is poor. This is the reason for the increased number of dressed modules failing the minimum breakdown voltage cut of the CNM modules in comparison to the FBK modules. Additionally, the value of the measured current is dominated by surface current effects on the sensor. This makes the breakdown voltage determination difficult and thus the distribution is broader than for the FBK modules. The dominance of the surface current is expected to disappear with the increased

leakage current due to radiation damage.
The planar modules fulfill the cut criteria, if the breakdown voltage is more than 70 V below the operation voltage of −80 V. Nearly all dressed modules with a planar sensor fulfill the sensor breakdown voltage criteria (with the exception of 4).
A significant change in the breakdown voltage between the ASSY and the FLEX test reveals an unexpected strong and deficient temperature dependence of the breakdown voltage or a damage that happened during the BURN-IN procedure. The relative breakdown voltage difference is presented in figure 6.17b. The relative breakdown voltage is defined as the breakdown voltage difference between ASSY and FLEX test normalized to the breakdown voltage measured in the ASSY test. All three distributions are symmetrically distributed with a mean value consistent with zero. Thus, no tendency to any direction in the breakdown voltage difference is observed.

6.3.2 Low dropout regulator calibration

The LDOs are neither tested nor calibrated at wafer level. The readout chips are operated in the IBL powering scheme for the first time during the ASSY test. The LDO characteristics is a chip feature and is tested and analyzed per readout chip, regardless of the module type.
The reference voltages of both LDOs can be tuned, as described in chapter 5.5. Dedicated test pads to measure the LDO output voltage are present on the module flex and can be contacted with probe needles. The resulting LDO output voltage dynamic range is measured, as presented in chapter 5.5.3, and the LDO output voltage is tuned to 1.2 V for the digital and 1.4 V for the analog supply voltage. The minimum / maximum distributions of the dynamic range are shown for both regulators in figure

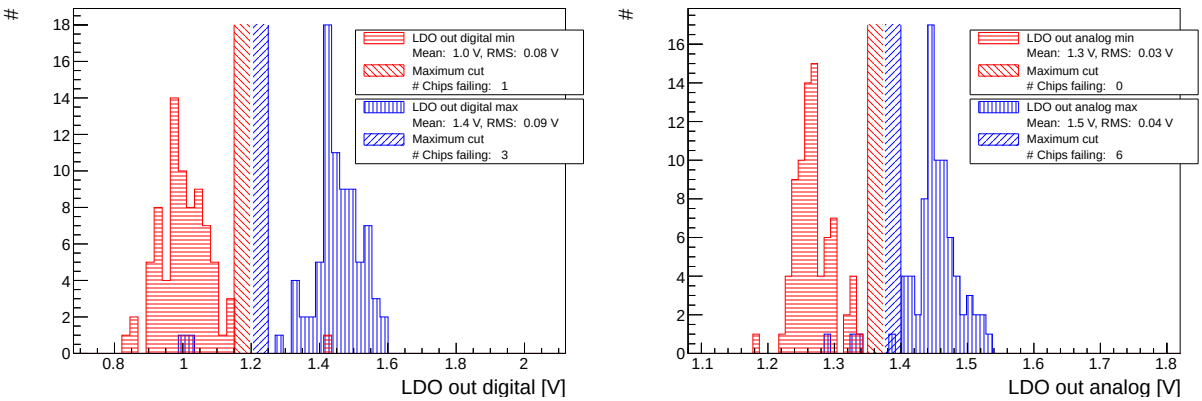


Figure 6.18: Minimum and maximum of the LDO output voltage dynamic range. The result of the analog LDO (a) and digital LDO (b), as well as the cut limits are shown.

6.18. As indicated, the minimum achievable output voltage of the digital LDO must be below 1.15 V, and the maximum digital supply voltage must be above 1.25 V. This ensures the tunability to the target of 1.2 V. The distributions peak at (1.0 ± 0.1) V in the digital minimum case and at (1.4 ± 0.1) V in the digital maximum case well below, respectively above the cut values. The similar distributions are measured for the analog LDO. Due to the combination of the band-gap based and the tunable reference voltage, the dynamic range of the analog LDO is reduced. Therefore, the safety margin for the maximum achievable analog supply voltage is removed, and all modules which achieve or exceed the analog supply

voltage target of 1.4 V are accepted for stave loading. Note, that the output voltage of the analog LDO is expected to rise with absorbed radiation dose (chapter 5.5.1). A total number of ten chips fails the criteria of the dynamic range of the digital and analog LDO.
A linear regression is applied to the LDO output voltage to measure the slope of the transfer function. The chip-to-chip distribution of the slope of both LDOs is combined in figure 6.19. This quantity is not

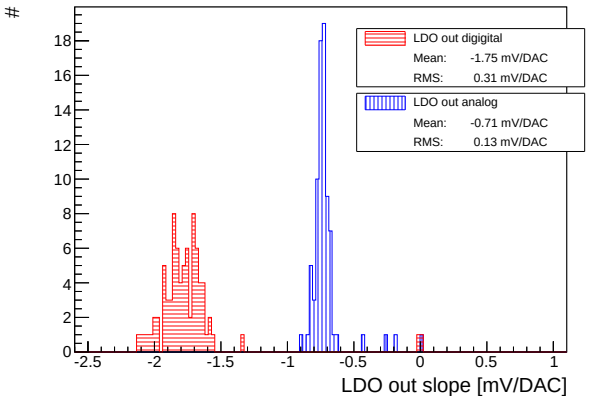
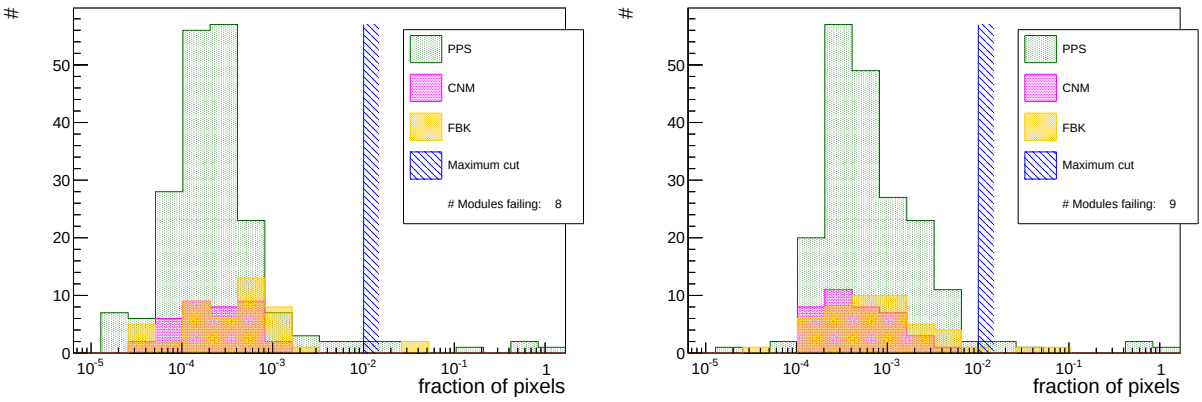


Figure 6.19: Slope distribution of the linear regression fitted to the output voltage for the digital and the analog LDO.

used for module selection and therefore no cut criteria and no number of failing chips is presented. A slope consistent with zero or far off the mean value indicates an un-tunable LDO, and is anyhow detected by the maximum and minimum cut. Six LDOs fail the tunability criteria. Also the slope reflects the fact that the dynamic range of the analog LDO is decreased. The slope distribution of the analog LDO is with (-0.71 ± 0.13) mV/DAC significantly lower than the measured (-1.75 ± 0.31) mV/DAC of the digital LDO.
The same LDO characterization is performed using the on-chip generic ADC (GADC). The GADC is not tested at wafer level and needs to be calibrated with the data collected during the module production. The only quantity accessible at module level with both, the GADC and an external measurement device, is the analog supply voltage of the readout chip. Thus, the analog LDO output characteristics is the candidate to calibrate the GADC. Additionally, the pulser circuitry input is accessible with the GADC. The pulser circuitry calibration can not be measured on dressed modules, but is measured at wafer level. A consistent pulser circuitry calibration measured at wafer level and with the calibrated GADC would confirm the successful calibration of the GADC. All possible data for this are collected in the ASSY test routine. The automated calibration routine of the GADC is addressed by the IBL collaboration at the time of writing.

6.3.3 Test hit response

The response to test hit injections at the digital readout chain input and at the preamplifier input is tested. The number of pixels which record an occupancy that differs from the number of injections are counted. This number is used to calculate the fraction of failing pixels per module. As expected, the mean fraction of pixels failing in the analog test is slightly higher (figure 6.20), because the analog test is sensitive to more error sources. Still, only nine modules with more than 1 % failing pixels do not fulfill this criteria.



(a) (b)

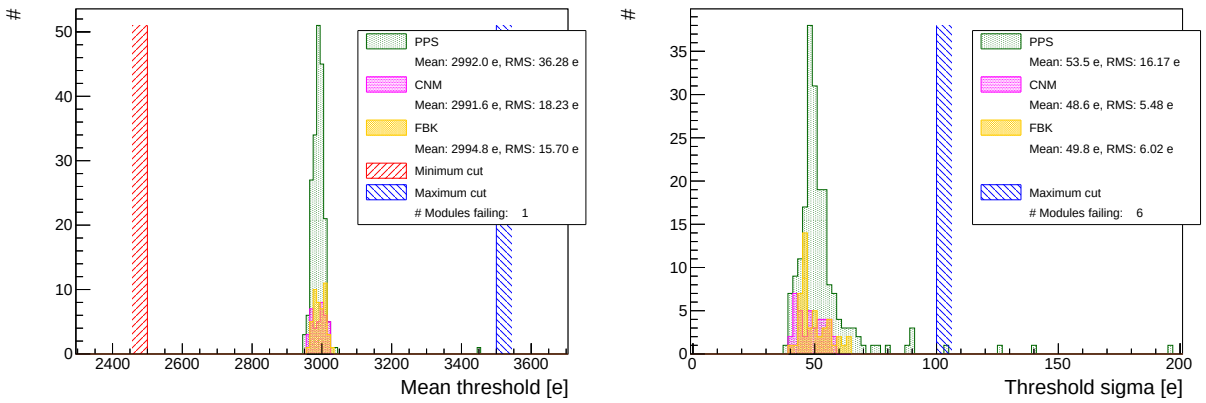
Figure 6.20: Fraction of pixels per module with an occupancy unequal to the number of digital (a) and analog (b) test hit injections. A variable bin size is used to achieve a better overview in the low fraction area in this representation with logarithmic x-axis scale.

6.3.4 Threshold tuning

The FLEX test is used to obtain a first configuration of each module, which is then used as a basis for the stave test configuration and finally for the IBL operation configuration. This configuration contains the calibration constants measured at wafer level as well as the calibration constants measured during the module tests. The module is tuned during the ASSY test to the target values of the initial IBL operation in order to obtain a tuning at room temperature. Starting from this tuning, the module is tuned again in the FLEX test at −15 °C for the initial module configuration for IBL operation. The tunability of the readout chips is in fact tested for the first time during the module tests, because the readout chips are not tuned at wafer level.
Figure 6.21 shows the mean threshold distribution after tuning (a) and the threshold sigma distribution (b) obtained in the FLEX test. One single module fails the selection criteria of a mean threshold between 2500 e and 3500 e. All other modules are tuned to the target value of 3000 e with a comparable RMS for all module types below 37 e. The threshold distribution width is also a good indicator for the tunability of the module. A width of less than 100 e is requested and all but six modules fulfill this requirement. The mean width is about 50 e, as expected.
At pixel level, the number of pixels with a threshold outside five standard deviations from the module's mean threshold are counted, as these pixels are likely to be un-tunable. Figure 6.23a displays the fraction of pixels per module, that show this failure mode.

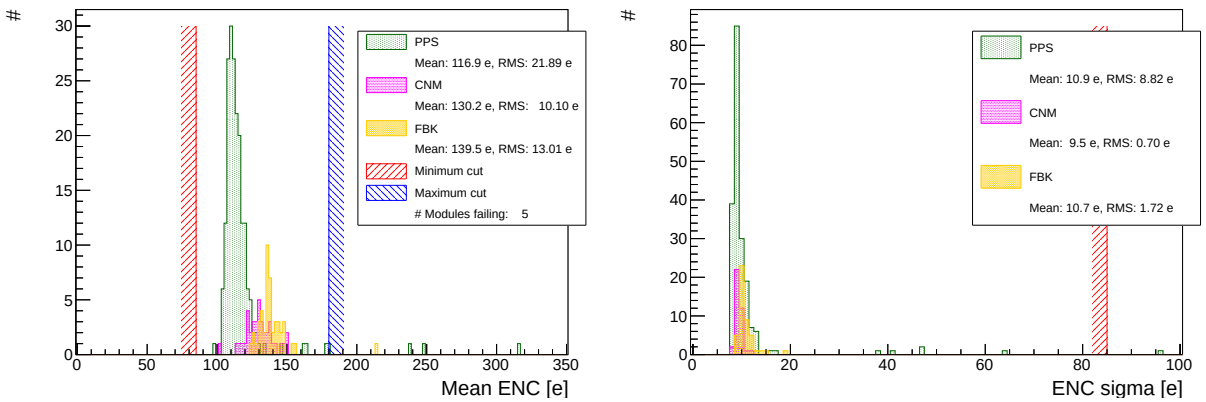
6.3.5 Noise

The ENC distribution is shown in figure 6.22a for each module flavor. As expected from the results presented in chapter 6.1.3, the planar modules' ENC distribution has the lowest mean value (117 e), while the ENC of the FBK modules has the highest mean value (140 e) reflecting their larger capacitance. The ENC distribution of the CNM modules is in between the two with a mean value of 130 e. The noise spread distributions are displayed in 6.22b. The result has a mean spread in the order of 10 e for all module types.
Similarly to the threshold of the pixels, the number of pixels with a noise difference of more than five



(a) (b)

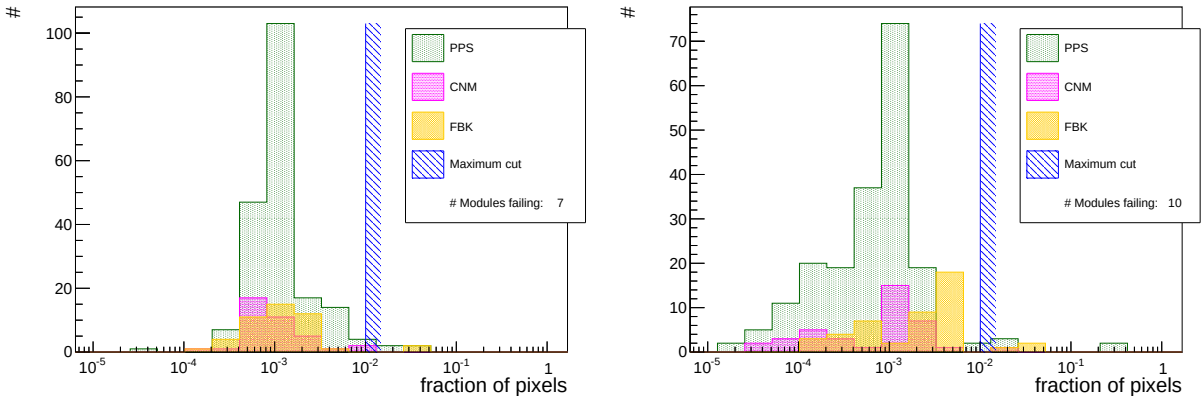
Figure 6.21: The module-to-module mean threshold (a) and threshold spread (b) distribution. All modules are tuned to 3000 e and operated at −15 °C.



(a) (b)

Figure 6.22: The module-to-module mean noise (a) and noise spread (b) distribution. All modules are tuned to 3000 e and operated at −15 °C.

standard deviations from the mean are counted. Ten modules show more than 1 % pixels that fail the pixel level noise cut (figure 6.23b).

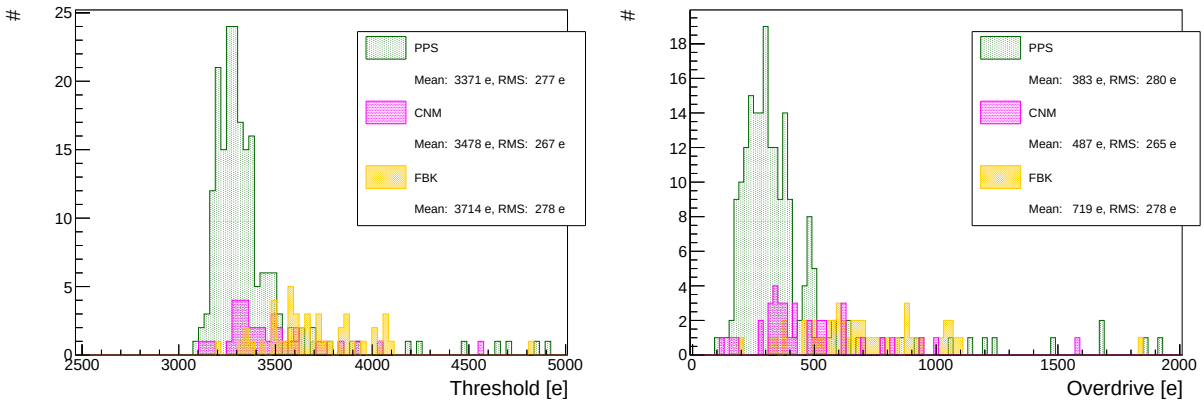


(a) (b)

Figure 6.23: Fraction of pixels with an outlying threshold (a) and noise (b) value per module.

6.3.6 In-time threshold and time-walk

The t_0 of each module is determined and stored in the module configuration during the FLEX test stage as explained in chapter 6.1.5. The in-time threshold is measured afterwards to measure the time-walk for each module. The in-time threshold distribution as well as the overdrive (calculated as difference of the mean values of the pixel-to-pixel distributions per module) are given in figure 6.24. The in-time



(a) (b)

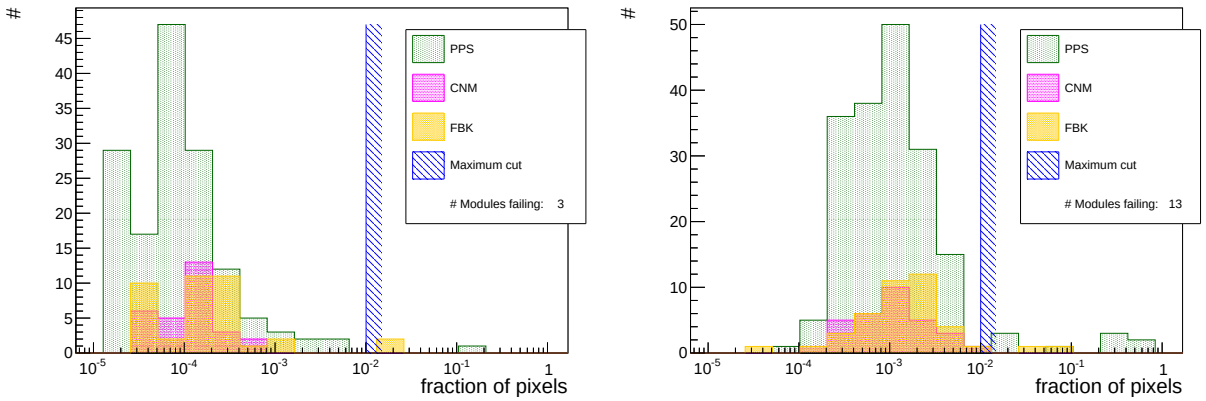
Figure 6.24: Timing scan distributions. The mean in-time threshold measured after t_0 adjustment (a) and the resulting overdrive distributions (b) for all three module flavors.

threshold distributions show the expected influence of the sensor type. The detector capacitance influences the rise-time of the preamplifier and thus the time-walk. The overdrive distribution is dominated by the in-time threshold of the modules, because all modules except for one are tuned successfully to

3000 e with a precision of approximately 2 %. Similarly to the noise distributions for the three module types, the overdrive distribution of the planar modules (383 e mean with a RMS of 280 e) is lower than the distribution of the CNM modules (487 e mean with 265 e RMS), while the FBK modules have the highest overdrive. The distribution of the FBK modules peaks at approximately 719 e and is about 278 e wide. These time-walk values are well below the time-walk correction capability of the readout chip (approximately 1500 e, see chapter 5.4.3 and chapter 6.1.5).

6.3.7 Noise occupancy and low threshold operation

The noise occupancy is measured sending 10^7 triggers with a length of 25 ns each to the tuned module. This translates to a sensitivity of the scan to a noise hit probability of 10^{-7}. The number of pixels with a noise hit probability above 10^{-7} are flagged as noisy and masked for the subsequent low threshold operation test as well as the source scan. The fraction of noisy pixels at a threshold of 3000 e is given in



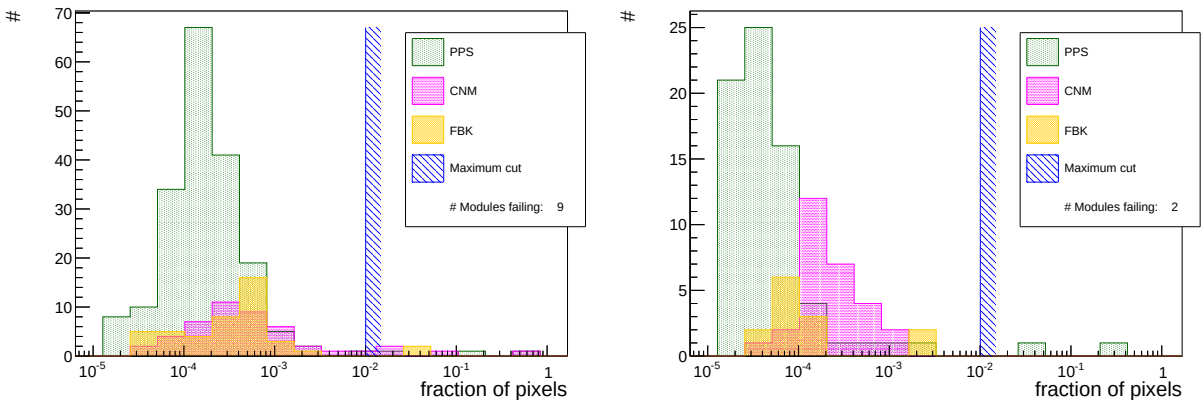
(a) (b)

Figure 6.25: Noise occupancy and low threshold operation test. The fraction of pixels with a noise hit probability above 10^{-7} using the configuration tuned at a threshold of 3000 e (a). Fraction of pixels with increased noise hit probability in any of the low threshold operation tests down to 1500 e (b).

figure 6.25a. Three modules show a number of noisy pixels above the 1 % limit.
Noise occupancy measurements at thresholds of 2500 e, 2000 e and 1500 e are performed, after the threshold is decreased globally. This procedure detects modules which are not conveniently operational at low thresholds. As expected, the number of pixels flagged as noisy at lower threshold increases (figure 6.25b). For ten additional modules the fraction of noisy pixels increases above the limit at lower thresholds.

6.3.8 Bump connectivity

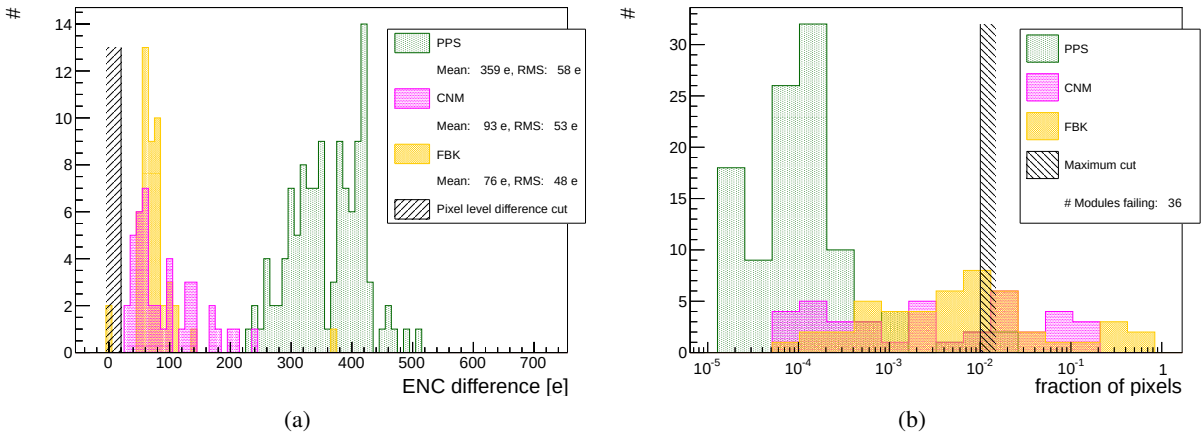
Several scans are performed to reveal the bump failures at pixel level. Several algorithms are implemented to identify the bump failure mode, either shorted (or with high coupling) or open bumps. Apart from the source scan occupancy, all of those algorithms use a combination of the result of two scans.
The number of pixels which do see crosstalk hits is counted and the fraction of shorted pixels is measured using the method described in chapter 6.1.7. Figure 6.26a shows the distribution of the fraction of pixels with crosstalk per module. A similar distribution for the number of shorted pixels is given in



(a) (b)

Figure 6.26: Fraction of pixels failing the crosstalk test (a). The fraction of potentially shorted pixels (b) is derived from the analog and the crosstalk test.

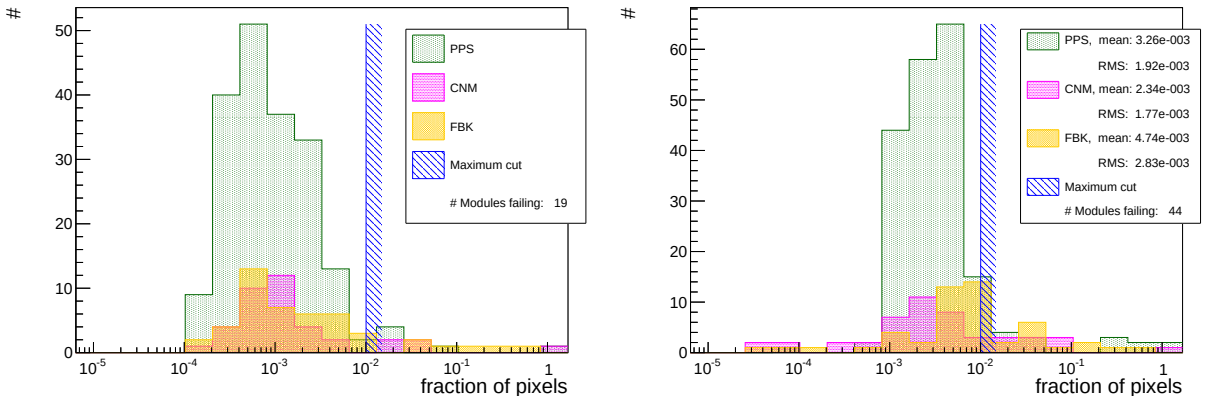
6.26b. Both failure modes occur at less than 1 ‰ of the pixels, with only very few exceptions. Nine modules have more than 1 % of pixels with crosstalk and for only two of them the algorithm searching for shorted pixels detects more than 1 % of shorted pixels.
No source scan is performed in the ASSY test stage. Another method using the difference of the preamplifier input capacitance of the un-depleted and depleted sensor is used to reveal unconnected bumps. This input capacitance difference results in a change of the ENC. The pixel-to-pixel difference in the ENC is used to estimate the number of open bump connections. This method is not exclusive and provides only a rough estimation of the number of unconnected bumps. But large areas of unconnected bumps, as typical for damages due to mechanical stress during the production steps, are in particular detectable with this method. Figure 6.27a displays the difference of the mean noise of the modules as well as



(a) (b)

Figure 6.27: The module-to-module noise difference distribution (a) which is used for the detection of open bump connections in the ASSY test. (b) shows the resulting fraction of pixels per module with unconnected bump bonds.

the cut of 20 e ENC difference that is used to flag a pixel as unconnected. Note that the cut is applied at the individual pixel noise difference, while here the mean noise difference is shown. The resulting number of pixels with potentially unconnected bump connections is counted and figure 6.27b shows the distribution of the fraction of unconnected pixels per module. A module with more than 1 % of open bumps would be rejected. In this analysis the cut is not used, as the method is not conclusive.
An ^{241}Am source scan occupancy is used for the final and conclusive open bump detection. A number of 19 modules has more than 1 % of pixels with less than 5 % or more than 450 % of the mean pixel occupancy (figure 6.28a).



(a) (b)

Figure 6.28: The module-to-module distributions of the fraction of pixels failing the occupancy criteria (a). The distribution for each module flavor of the fraction of the pixels per module that fail in any scan (b). Only the accepted modules are taken into account for the calculation of the given mean and RMS values.

6.3.9 Summary and outlook

After the test of each individual failure mode, the number of pixels which fails in any test is counted. Individual pixels are not double counted, because most of the test routines are mutually dependent on each other. For example, a digitally unresponsive pixel fails in all other tests that require the detection of charges. A required fraction of pixels that fails in any test below 1 % is the most strict cut condition used during the module production QA. The module-to-module distribution is given in figure 6.28b. This number is used as a basis for the final module selection. All 44 modules with a fraction of failing pixels above 1 % are neglected in the calculation of the given mean and RMS values. The mean number of failing pixels of the accepted PPS modules is about 0.33 %. The distribution width is approximately 0.19 %. As expected, the fraction of failing pixels distribution of the CNM and FBK modules is comparable to the planar module distribution with a mean of about 0.23 % and an RMS of 0.18 % in the CNM case and 0.47 % mean and 0.28 % RMS in the FBK case.
An additional penalty can be applied to a module in case of mechanical rework or any other disturbance in the production and testing procedure. The penalty is applied in units of failing pixels. If the resulting number of failing pixels then exceeds the 1 % limit, the module is excluded from stave loading. Table 6.2a provides a complete summary of the module production at the time of writing. The number of modules delivered by IZM per flip-chip batch and the losses due to the different failure modes are given. Modules are flagged as broken, if either mechanical damage or electrical damages, in first place

		batch number									
		1	2	3	4	5	6	7	8	9	10
# modules		46	75	100	25	58	64	33	73	92	54
breakage mode	mechanical	0.00	0.04	0.02	0.08	0.00	0.00	0.00	0.03	0.04	0.00
	electrical	0.20	0.12	0.01	0.00	0.09	0.03	0.09	0.03	0.04	0,00
reject reason	electrical	0.00	0.12	0.01	0.00	0.02	0.02	0.06	0.06	0.02	0.00
	bump yield	0.38	0.45	0.23	0.00	0.07	0.08	0.00	0.14	0.08	0.07
	sensor bias	0.09	0.00	0.08	0.00	0.02	0.00	0.03	0.01	0.00	0.07
yield		0.29	0.24	0.64	0.92	0.75	0.81	0.75	0.62	0.81	0.91

(a)

		total	1-3	4 and higher
# modules		620	221	399
breakage mode	mechanical	0.02	0.02	0.02
	electrical	0.06	0.09	0.04
reject reason	electrical	0.03	0.04	0.03
	bump yield	0.17	0.33	0.08
	sensor bias	0.02	0.05	0.01
yield		0.65	0.43	0.77

(b)

Table 6.2: Summary of module production. All completely tested batches at the 26th of September 2013 are considered. The number of delivered modules and the fraction of broken or rejected modules is given for the different failure modes. The resulting yield is calculated. The summary for each individual batch is shown in (a) and the total summary with focus on the total yield before and after the change in the flip-chip process is given in (b).

shorts and broken LDOs, are detected. The reject reason after the test procedure is divided into electrical failures, bad bump connection yield and sensor bias characteristics. In the first three batches, the major losses are due to the mentioned bump bonding issue. The laser release of the glass carrier was problematic on some modules in batch eight, which results in areas of disconnected bumps at the chip edges due to mechanical stress. A very high bump connectivity yield is achieved after the change of the flip-chip method (from batch four on). Apart from the mentioned batch eight, the bump bonding yield was almost perfect. The total yield of all batches after batch four is 77 % (table 6.2b). Batch one to three had a significantly lower yield of only 43 %.
The bare module production for IBL is finished at the time of writing. The dressing of bare assemblies to modules and the production QA tests are ongoing. The production sites deliver a rate of accepted modules which fulfills the needs of the loading of up to one stave per week. The module production and test for IBL is expected to be finished in October 2013. The stave loading is ongoing at the time of writing. Twelve staves are ready and in the stave quality assurance procedure. The obtained performance of these staves is very promising. The full staves can be tuned conveniently to a threshold as low as 1500 e. Figure 6.29 and 6.30 present a summary result for the stave qualification of stave one,

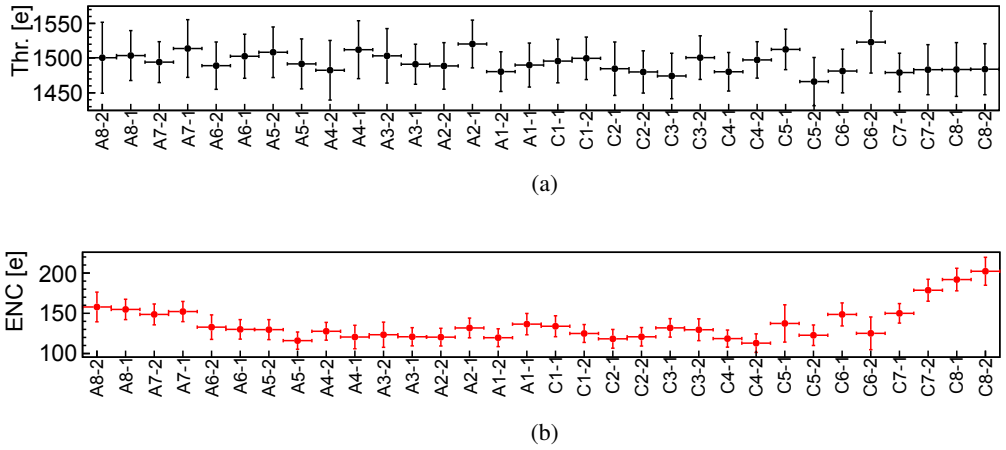


Figure 6.29: The threshold of stave one after tuning (a) and the ENC (b).

the first IBL production stave. The threshold is uniformly tuned along the stave (figure 6.29a) and the ENC is within the expectations from the module production tests (figure 6.29b). The number of failing pixels per readout chip is approximately 1 ‰ for each readout chip (not shown here). A source test using a ^{90}Sr source is performed and the resulting occupancy map of the full stave is shown in 6.30. The

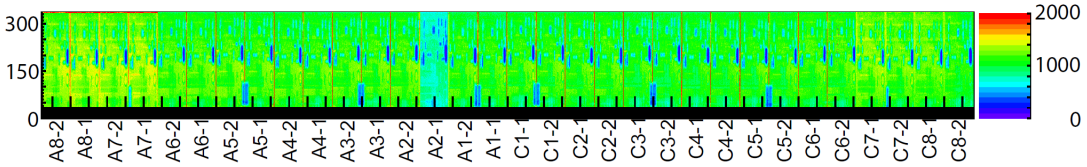


Figure 6.30: The occupancy map of the full stave one in a ^{90}Sr source scan.

integration of the IBL staves around the beam pipe is the next challenge towards the insertion of the IBL into the ATLAS detector. The commissioning phase after the insertion will provide the needed expertise to start the operation of the IBL in the LHC environment and with tracks originating from collisions the simulated ATLAS performance improvements can be validated.

Chapter 7

New pixel concepts for the LHC Phase-II

Several competitive pixel detector concepts are under research and development for the new ATLAS inner tracker needed for the LHC run Phase-II. While for the innermost layers the occupancy and radiation environment is most challenging, the price as well as the production and testing rate of modules for the huge silicon area to cover is a key issue for the outer layers. One option probed with first encouraging results is the use of a commercial high voltage CMOS technology as sensor. Due to the full CMOS functionality, the sensor could integrate the full readout logic. It could also take benefit of having a dedicated readout chip. The use of a dedicated readout chip would decouple the sensor technology from the readout chip technology and could result in an increased amount of digital functionality on the module and more electronic complexity. The first amplification stage and hit processing logic can be implemented inside the sensor. If so, the resulting signal is large enough to be capacitively coupled to the readout chip. Possibly cost of the bump connection of current hybrid pixel detector concepts can be reduced, because the sensor can be glued to the readout chip. One could also think of having a configurable sensor in terms of pixel geometry with this technology. With this solution, an adjustable pixel geometry depending on the geometrical module position within the detector is possible. The benefit could be a good physics performance with a reduced number of readout channels.
A prototype sensor in high voltage CMOS technology exists, called HV2FEI4, and is glued to the FE-I4 readout chip. In the framework of this thesis, the full integration of the HV2FEI4 support to the USBpix test system is done. This includes the configuration register support of the HV2FEI4 and the injection of test charges directly into the sensor chip. All other test setups that are used for testing of the HV2FEI4 on an FE-I4 readout chip consist of a separate DAQ system for the HV2FEI4. Thus, with the implementation of the HV2FEI4 into the USBpix system, convoluted scan routines and timing sensitive scans are possible for the first time.

7.1 The high voltage CMOS technology for particle detection

The high voltage CMOS technology is an industrial development for the application of high voltage switches. It is commonly a multi-well structure on a relatively high resistivity p-doped substrate. The resistivity of the substrate is usually above $10\,\Omega\,\mathrm{cm}^{-1}$. The entire CMOS electronics is implemented in the deep n-well. In the technology used for the HV2FEI4 sensor, the PMOS transistors are implemented directly into the deep n-well, while the NMOS transistors sit in a p-well within the deep n-well. Due to the high resistivity of the substrate, a high voltage can be applied to the substrate. The electrical field caused by the high voltage increases the depth of the depletion zone into the substrate. If this technology is used for particle detection, the simplest configuration is to use the deep n-well as charge collecting electrode. This configuration is sketched in figure 7.1. In this configuration, the collecting electrode is the only charge attracting n-well and thus no charges are lost to insensitive n-wells. The drawback is a large pixel capacitance due to the large charge collecting electrode. Additionally, the potential of the deep n-well fluctuates with the collected charge. Therefore, precautions must be taken in the use

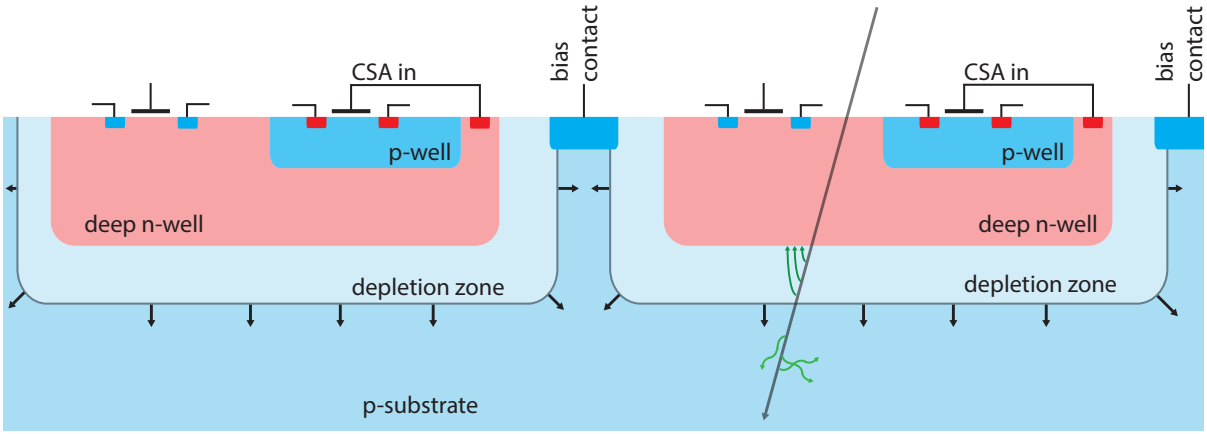


Figure 7.1: Simplified cross section of a high voltage CMOS sensor for particle detection. PMOS transistors are implemented in the deep n-well. A p-well within the deep n-well provides shielded NMOS transistors. The p-doped contacts between the deep n-wells isolate the deep n-wells and are used as bias contacts to deplete the substrate. Charges generated by ionizing particles travelling through the substrate drift towards the n-well within the depletion zone and the deep n-well can be used as charge collecting electrode.

of the PMOS transistors in the deep n-well. Within the depleted region the charge generated by ionizing particles is mainly collected by drift. This is the key feature which makes the high voltage CMOS technology a promising alternative sensor candidate also in high radiation environments and when high speed charge detection is necessary.
A collaboration has formed during 2012 which investigates the possibilities of this new concept for ATLAS. The collaborating institutes are in alphabetical order: Bonn, CCPM[1], CERN, Geneva, Göttingen, Heidelberg and LBNL[2].

7.2 The HV2FEI4 sensor

The HV2FEI4 is fabricated in the Austria Microsystems 180 nm process. This process allows a bias voltage of the substrate as high as −60 V. The depleted region depth is then approximately 15 µm. The HV2FEI4 uses the most simple configuration as shown in figure 7.1, where the deep n-well serves as charge collecting electrode and the isolation p-implants as bias contacts. The HV2FEI4 holds a charge sensitive amplifier (CSA) and a discriminator. The HV2FEI4 is designed to fit the FE-I4 bump bond footprint. The HV2FEI4 is flipped and glued to the FE-I4 readout chip. The bump pads of the readout chip and the sensor form capacitors, as shown in figure 7.2, and the discriminator output signal of the HV2FEI4 is transmitted using capacitive coupling to the preamplifier in the FE-I4 readout chip.
Although the HV2FEI4 is an early stage prototype, the sensor makes use of the configurability of the sensor and the possibilities provided by the implementation of logic into the sensor already. The pixel size of the HV2FEI4 is 33 µm × 125 µm. That is only a third of the FE-I4 pixel size. Six HV2FEI4 pixels are routed to two bump pads. Thus, six HV2FEI4 pixels are read out by two FE-I4 pixels in the same row. The connection scheme is illustrated in figure 7.3. A HV2FEI4 unit cell holds two columns and three rows of pixels. The top left, bottom left and middle right pixel are connected to one FE-I4 pixel and the three other pixels are read out by the second FE-I4 pixel. The discriminator output signal

[1] Center for Particle Physics of Marseille.
[2] Lawrence Berkeley National Laboratory.

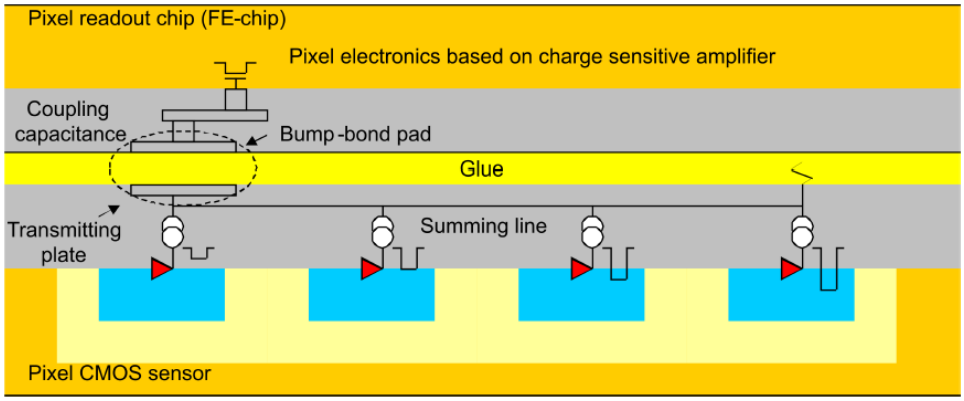


Figure 7.2: Pixel cross section of a hybrid detector concept using capacitive signal transmission between the high voltage CMOS sensor and the readout chip [57].

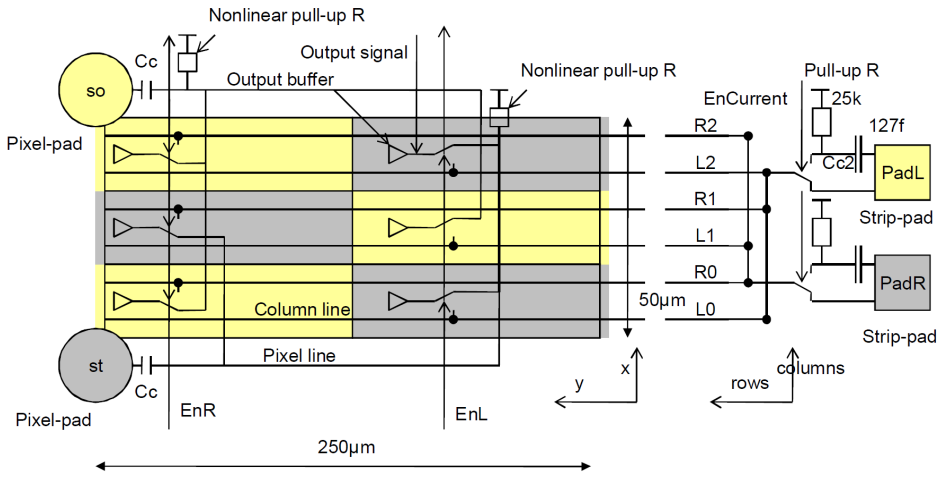
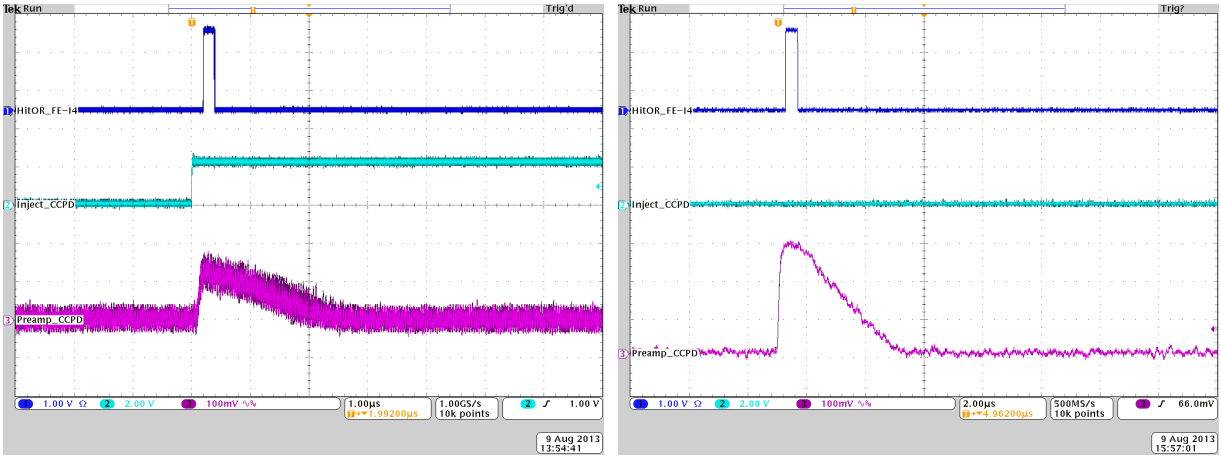


Figure 7.3: Connection scheme of a HV2FEI4 cell structure [57]. Each cell consists of six HV2FEI4 pixels which are connected to two FE-I4 pixel cells. Additionally to the pixel detector read out used in this thesis, a strip based readout option is present in the HV2FEI4 chip. This option is sketched in the logic on the right side, but is not used for the work presented here.

amplitude is adjustable. The sub-FE-I4 pixel information can be decoded using different discriminator output amplitudes for the three sub-pixels connected to the same FE-I4 pixel. The TOT information of the FE-I4 can be used to reconstruct the HV2FEI4 sub pixel instead of the collected charge as it is the case for the present passive sensor readout.
Global as well as pixel configuration registers are implemented in the HV2FEI4. These registers are used to define the pixel or the strip readout mode and to set several DACs in the sensor, for example to adjust the preamplifier bias current, which is the main current consumption driver, or to adjust the discriminator output amplitude of the three sub-pixels in the HV2FEI4 unit cell. A test charge injection capacitance is present in each HV2FEI4 pixel. A chopper circuitry with an adjustable voltage step amplitude is implemented on the support PCB for HV2FEI4 hybrid assemblies. The CSA output of a single test pixel is accessible on the PCB. Also the discriminator output of each pixel can be connected to a wire bond pad which is connected to test pins on the PCB. The needed functionality to configure the HV2FEI4 as well as to perform injections of variable charge into the sensor is implemented into the USBpix hardware and software framework. An integrated (single) test system is hence achieved to operate the readout chip as well as the HV2FEI4 sensor for the first time. This is mandatory to implement tuning algorithms using the charge injection into the sensor to tune FE-I4 parameters, or to measure the influence of HV2FEI4 parameters as a function of FE-I4 settings.

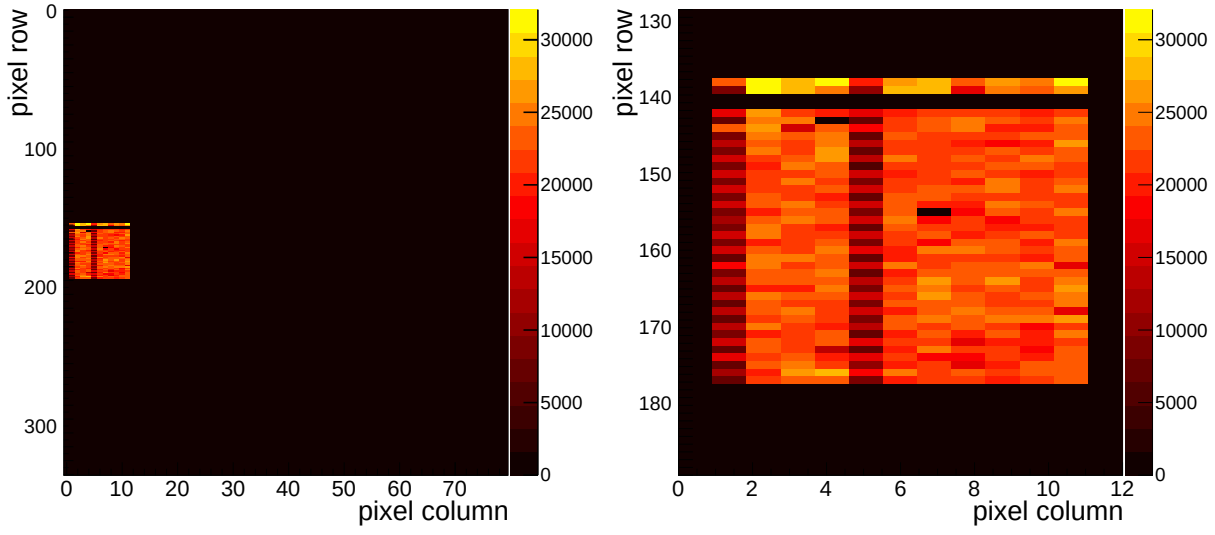
7.3 First results with HV2FEI4

The HV2FEI4 collaboration has shown the radiation tolerance of the technology to a NIEL fluence of $10^{15}\,n_{eq}cm^{-2}$ with proton irradiation and to $10^{14}\,n_{eq}cm^{-2}$ with neutron irradiation. The TID tolerance of the electronics is demonstrated up to 60 Mrad with x-ray irradiation [58].
The response of the FE-I4 HitOR signal to charges in the sensor is shown in figure 7.4. The response to two fundamentally different charge sources is presented: charge injection using the injection capacitance and charge generated by an ionizing particle.
In figure 7.4a the injection capacitance at the CSA input in the HV2FEI4 is used to issue a charge injection by the USBpix system. The injection signal of the USBpix system is shown in the middle. At the rising edge of the signal, the chopper circuitry on the support PCB generates a negative voltage step across the injection capacitance of each HV2FEI4 pixel. The bottom waveform is the CSA output of the test pixel. The top signal is the HitOR signal of the FE-I4 readout chip. The fact that the HitOR signal reacts in coincidence with the charge injection proves the functionality of the AC coupled signal transmission between HV2FEI4 and FE-I4.
The CSA of the test pixel also detects charges generated by electrons radiated by a ^{90}Sr source (figure 7.4b). No charge injections are issued by the USBpix system, so the injection signal is constant. Again, the HitOR of the FE-I4 reacts in coincidence with the CSA of the HV2FEI4, so the hybrid assembly using a HV2FEI4 sensor glued to a FE-I4 detects ionizing particles with capacitive coupling between sensor and readout chip.
Five million hits are collected in a source scan with a beta source (^{90}Sr). The discriminator output amplitude is equal for all three HV2FEI4 sub-pixels coupled to the same FE-I4 pixel. Hits are recorded by the FE-I4 in the pixels covered by the HV2FEI4 sensor (figure 7.5a). A zoom into the area of interest shows, that the HV2FEI4 is uniformly illuminated except for two columns. The HV2FEI4 pixels read out by the FE-I4 pixels in the two missing rows are implemented differently from the rest and are very noisy. Therefore the two rows of the FE-I4 pixels are masked. Also the two pixels which record no hits are masked during the scan.
The TOT information of the FE-I4 is not correlated to the charge collected in the HV2FEI4. It depends



(a) (b)

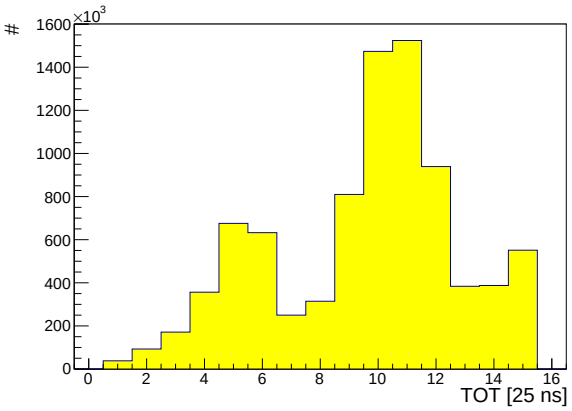
Figure 7.4: The HitOR signal of the FE-I4 readout chip (top waveform), the Strobe signal used to issue an injection (middle waveform) and the preamplifier output waveform of the HV2FEI4 operated with USBpix (bottom waveform). The response of the HitOR signal to a charge injection issued in the sensor by the USBpix system (a) as well as by a particle originating from a radioactive source (b) is shown.



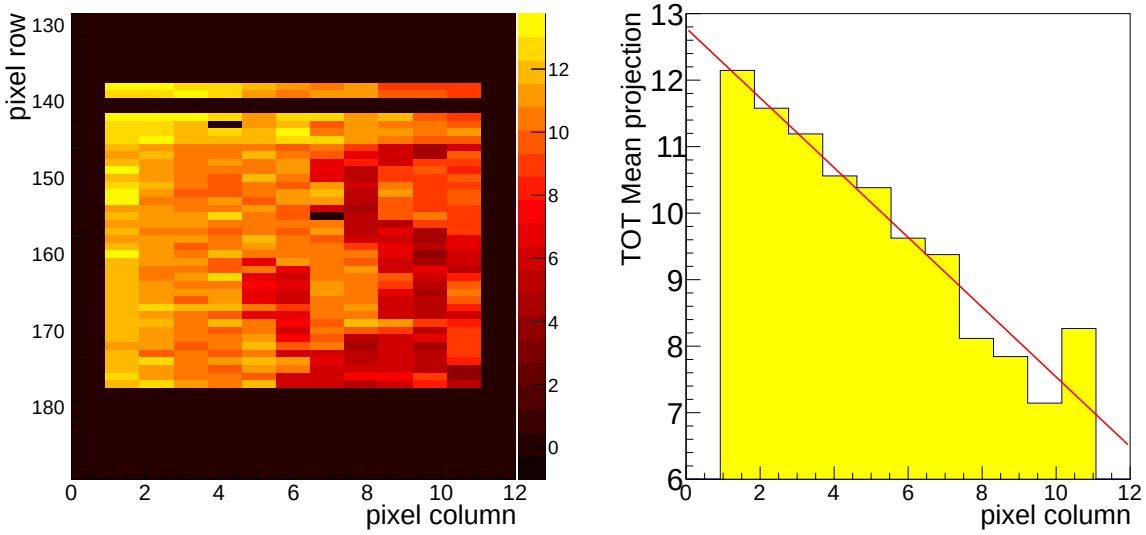
(a) (b)

Figure 7.5: Occupancy maps of the HV2FEI4 glued to an FE-I4 readout chip obtained with electrons from a ^{90}Sr source. The full FE-I4 map (a) with entries in the HV2FEI4 position and a zoom into the region of the HV2FEI4 (b).

on the discriminator output pulse height and thus can be used to get a sub-pixel resolution once the FE-I4 is appropriately tuned. Additionally, the recorded TOT is influenced by the coupling capacitance. As the plate size of the capacitors formed by the bump pads of the two chips is fixed, the coupling capacitance is mainly influenced by the thickness of the glue layer and the alignment of the chips. The TOT



(a)

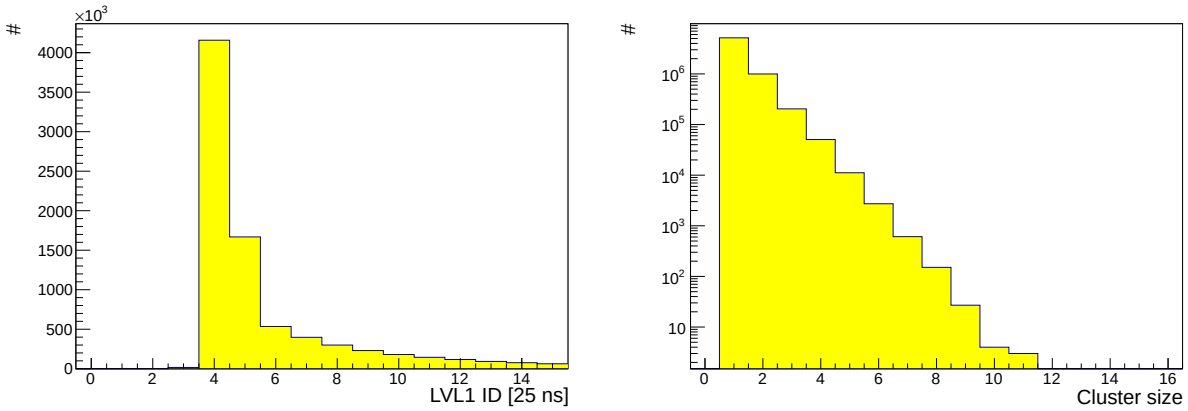


(b) (c)

Figure 7.6: The TOT information recorded by the FE-I4 (a). The TOT is not correlated to the charge collected in the sensor. The color coded mean TOT per pixel in the area covered by the HV2FEI4 (b) and the mean TOT projection along the columns (c).

spectrum recorded by the FE-I4 does not show a single peak as is expected with a uniform discriminator output pulse height (figure 7.6a). Furthermore, the calculated mean TOT per pixel presented in figure 7.6b reveals a geographical dependency. The mean TOT decreases from the left to the right. Figure 7.6c visualizes this dependency. The projection of the mean TOT along the columns decreases linearly with a slope of $-0.53\,(25\text{ ns})$/column. A very likely explanation is a slight tilt between the sensor and the readout chip. The distance between the capacitor plates increases from left to right and the capacitance decreases. The coupling strength is reduced, which results in a smaller signal recorded by the FE-I4.

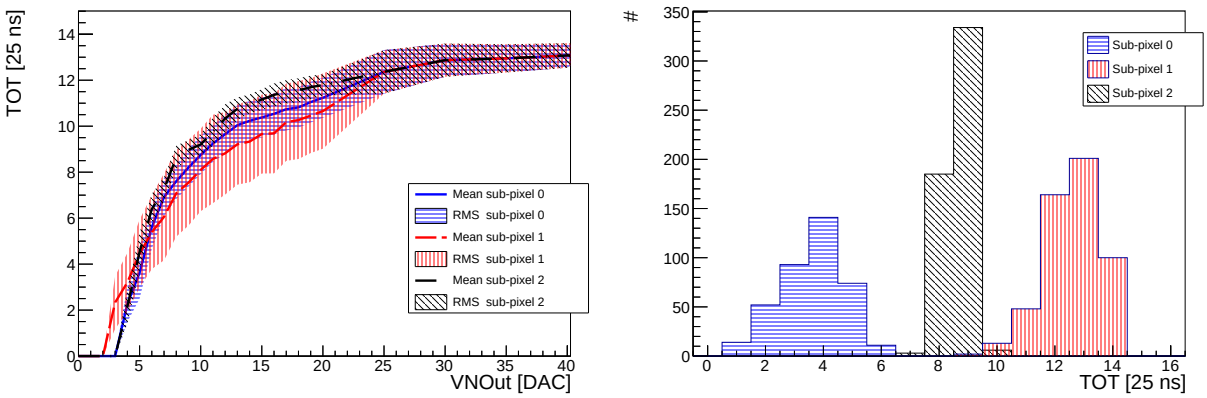
The hit detection time distribution within the sensitive time window of 16 times 25 ns is given in figure 7.7a. The FE-I4 HitOR signal is used in the scan to issue a trigger. The timing between the HitOR positive edge, which is in coincidence with the hit detection, and the trigger sent to the FE-I4 is fixed. No entries are expect in any other bin than four and five. A long tail after these is observed. This originates from hits detected in the readout chip after the hit issuing the trigger. Small hits close to big hits are expected to be detected late due to the time-walk effect. With the HV2FEI4 as sensor, the two time-walk sources introduced in chapter 3.3.2 are present twice, in the preamplifier and the discriminator of the sensor, and of the readout chip. A dedicated time-walk scan algorithm, sub-FE-I4-pixel resolution, and a cluster algorithm considering the sub-pixel connection scheme are necessary to investigate the time-walk in this configuration.
The present algorithm clusters the FE-I4 pixel information. A significant amount of multi-pixel clusters is expected to be generated by the traversing electrons from a beta source. Multi hit clusters are expected



(a) (b)

Figure 7.7: The hit timing information within a time window of 16 times 25 ns (a). The cluster size in FE-I4 pixels measured in the Sr^{90} source scan (b).

especially with the small pixel size of the HV2FEI4 pixels and the connection scheme with neighboring HV2FEI4 pixels that are connected to neighbor pixels in the FE-I4 (figure 7.3). The cluster size decreases exponentially and cluster sizes up to eleven pixels are recorded, see figure 7.7b.
To prove that the sub-FE-I4 pixel resolution is achievable, the discriminator output amplitude is scanned individually for the three sub-pixels while performing test charge injections into the HV2FEI4. The TOT response of a single FE-I4 pixel is measured. The mean of the resulting TOT distribution is given in figure 7.8a as a function of the discriminator output amplitude (set by the DAC VNOut) for all three sub-pixels connected to this FE-I4 pixel. The RMS of the TOT histograms is displayed as a band. The RMS of sub-pixel 1 is higher than for the other two sub-pixels. A repetition of this measurement on more than this single FE-I4 pixel could reveal if this is a systematic result or present in this single pixel only. Nevertheless a discriminator output amplitude can be selected from these data for each sub-pixel so that the mean and RMS of the three sub-pixels do not overlap. The TOT spectrum as measured by the FE-I4 when injecting into the HV2FEI4 with these settings is shown in figure 7.8b. Three distinct TOT peaks appear and the sub-pixel can be reconstructed from the TOT information of the FE-I4.
The pixel to pixel spread of the discriminator output amplitude smears the TOT spectrum of the FE-I4, if a large number of FE-I4 pixels is enabled at the same time. The resulting TOT spectrum does not show any distinct peaks as observed in figure 7.8b. Therefore, a tuning algorithm to adjust the TOT



(a) (b)

Figure 7.8: The TOT response of a single FE-I4 pixel as a function of the discriminator output amplitude of the HV2FEI4 and the three sub-pixels within the HV2FEI4 (a). The TOT spectrum measured by the FE-I4 with a dedicated output amplitude setting for each of the three sub-pixels.

response of each individual FE-I4 pixel while injecting charges into the HV2FEI4 is necessary. This is impossible with the setups consisting of two independent test systems for sensor and readout chip that are used so far. The implementation of this tuning algorithm into the USBpix system is work in progress at the time of writing.

7.4 Summary

The HV2FEI4 demonstrates that the high voltage CMOS technology is a promising candidate for the outer layers of the planned ATLAS pixel detector upgrade for the LHC run Phase-II. The fabrication in an industrial process and the connection of the sensor and the readout chip without the costly bump-bonding process reduces the cost. Albeit the characterization of the HV2FEI4 assemblies is in an early stage, the AC coupled signal transmission between the sensor and the readout chip, the detection of ionizing particles, as well as the reachability of a sub-pixel resolution using the TOT information of the readout chip could be demonstrated. More detailed performance investigations are simplified by the use of the USBpix test system for both layers. The basic integration of the HV2FEI4 into the hardware and software framework is finished. No difference is made within the software structure between the HV2FEI4 and the FE-I4 configuration items.

Chapter 8

Conclusions

During the next two decades the nature of the electro-weak symmetry breaking mechanism will be investigated in depth with the LHC. This implies to study the characteristics of the recently discovered Higgs boson in great detail. Additionally, the search for physics beyond the Standard Model will continue. This rich physics program requires increased collision rates. A three phase upgrade program of the LHC has started. During the long shutdown in 2013 and 2014 (LS1) the LHC is prepared to run at the design center of mass energy of 14 TeV. In the two following long shutdowns of 2018 (LS2) and 2022 to 2023 (LS3) the luminosity will be increased in two steps. The ATLAS detector will also be upgraded during these shutdowns to cope with the increased challenges. The pixel detector is upgraded during LS1 by the insertion of the IBL to ensure an excellent tracking performance until a completely new inner detector will be installed during LS3.

The presented work focuses on the development and characterization of the central sensitive elements of the pixel detector upgrades: the modules. The USBpix test system and all scan routines that are used by the collaboration for the readout chip and module characterizations, in laboratory as well as in test beam environment, and during the production tests, are developed in the framework of this thesis. As a result of the user friendliness and low price of the USBpix system in comparison with the alternatives, and the high performance in terms of speed and data quality, the USBpix system is produced in a large quantity (about 150 units) and extensively distributed within the collaboration.
Several of the results obtained on FE-I4A readout chips in this work lead to changes in the design that improve the effected circuits in the IBL readout chip, the FE-I4B. With the help of these, the FE-I4B fulfills the requirements of the IBL and of the outer layers of the baseline concept for the new pixel detector to be installed in LS3. As an example, the test charge injection circuitry in FE-I4B is improved and has a large dynamic range with good linearity.
As presented, also the analog readout chain has a very good performance. The hit detection threshold can be tuned precisely to the target threshold in a large threshold range, and the threshold dispersion across the pixel matrix is only 50 e after tuning. The operation at low thresholds is mandatory to achieve a high signal to noise ratio after irradiation of the module. It is shown in this thesis that the FE-I4 can be operated at thresholds as low as 1500 e without a significant increase of the noise hit rate. This result motivates the threshold used for the test beam campaigns as well as for the initial operation of the IBL detector in the experiment. The equivalent noise charge (ENC) of bare FE-I4 chips is characterized as well. The ENC at the IBL operation point is approximately 120 e.
The sophisticated readout architecture is based on the four pixel digital region, a common digital logic shared by four analog pixel cells. The hits are stored inside this region until the Level-1 trigger is received. With this new architecture the FE-I4 readout chip can handle very high hit rates. Even a simultaneous hit in all 26880 pixels can be processed correctly. All digital functionalities are proven to work as expected. The presented results on the powering of the FE-I4B chip lead to the powering scheme of the IBL which provides both, reliable power-up behavior at a large temperature range, and

tunability of the on-chip regulator output voltage.
During the production tests at wafer level, the full functionality of each chip is validated. Only chips with less than 0.2 % of the pixels showing any failure are accepted for the IBL production. This strict cut is the major challenge for the chips and 23 % of the chips are discarded due to this cut. The overall yield of the 43 wafers tested for IBL is (60 ± 2) %.

It is proven that the IBL modules with all three sensor flavors fulfill a number of challenging requirements. These are especially the geometrical inefficiency below 2.2 % and an efficiency above 97 % within the sensitive area until the IBL end of lifetime fluence of $5 \times 10^{15}\,\mathrm{n_{eq}cm^{-2}}$. The module performance is validated in laboratory environment. The absolute charge calibration is measured using a method that extracts the spectrum of mono-energetic x-ray sources by the derivative of the hit rate as a function of the energy. A relative charge resolution of only $280\,e$ is achieved with this method. A new TOT to charge calibration method is presented and the time-walk of the IBL modules is shown to be within the time-walk correction capabilities of the FE-I4 chip. An increase of the number of unresponsive pixels is observed after proton irradiation. The explanation of this issue and an effective counteraction is found in this thesis. The in-cell efficiency, the edge efficiency, and the overall hit efficiency are measured in test beam environments. All sensor flavors meet the 97 % efficiency requirement in the sensitive area and have an inactive edge size smaller than needed to achieve 2.2 % of geometrical inefficiency. The spatial resolution in the short pixel direction is approximately 15 µm and within the expectations for a segmentation width of 50 µm.
In addition to this, the work presented in this thesis has made a significant contribution to the production of the IBL. A complex test setup with several custom built constituents has been developed and used at both production sites for the quality assurance and the full module performance validation of each IBL module. During this program, the readout chips are operated for the first time in the IBL powering connection scheme and the on-chip regulators are calibrated. The tests include the sensor bias characteristics, the tunability of the module, the electronics noise and noise hit rate measurement, the hit detection timing, and also the measurement of the bump connectivity. Analogous to the wafer level chip tests a cut on the number of failing pixels is applied. Less than 1 % of pixels failing in any test are required for a module suitable for the IBL production. The mean fraction of failing pixels of the modules accepted for production is between 2 ‰ and 5 ‰. The module yield differs between the flip-chip batches. After some initial ramping up of the module quality, the overall module yield is 72 % from batch four on.

The experimental challenges after the LHC upgrade during the LS3 will be ambitious. In particular, the expected number of 140 pile-up events translates to increased tracking performance requirements for the inner detector. A completely new all silicon inner tracking system is mandatory. Additionally, the new tracker system should contribute to the trigger system. Research and development on new technologies for the new inner tracking system started. The demands for the innermost and outer layers of the proposed new pixel detector are very different. A new detector concept, which consists of an active sensor that is produced in an industrial high-voltage CMOS technology and coupled capacitively to the FE-I4 readout chip, is studied within this thesis. The first prototype (HV2FEI4) is used. It is shown with test charge injections that the capacitive signal transmission to the readout chip is working. The detection of ionizing particles with this concept is also proven. A sub-FE-I4-pixel resolution is achieved using different signal heights for the capacitively coupled signal. The sub-pixel information is recovered from the charge information of the readout chip.
The promising results obtained in this thesis on the first prototype using an industrial high-voltage CMOS technologies as sensor layer motivate further research and development. This should include both: a full performance measurement of the presented HV2FEI4 prototype as well as the exploration

of competitive technologies. A full performance measurement requires a number of new test and tuning algorithms, which can be implemented conveniently into the USBpix test system. Test beam campaigns to exploit the in-pixel inefficiency sources before and after irradiation are needed. Competitive technologies would allow to go one step further. The availability of a full CMOS process encapsulated in a multiple layer well structure promises to implement the logic of the readout chip into the sensor layer. If the efficiency and radiation tolerance of such a concept can be proven, the pixel detector technology for high irradiation environment might be revolutionized.

Bibliography

[1] ATLAS Collaboration. *The ATLAS experiment at CERN*. Website. http://www.atlas.ch/photos/full-detector-cgi.html. 2013.

[2] ATLAS Collaboration. *ATLAS high-level trigger, data-acquisition and controls: Technical Design Report*. Technical Design Report ATLAS. Geneva: CERN, 2003.

[3] ATLAS Collaboration. *ATLAS Experiment - Public Results*. Website. https://twiki.cern.ch/twiki/bin/view/AtlasPublic. 2013.

[4] ATLAS Collaboration. "Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC". In: *Physics Letters B* 716.1 (2012), pp. 1 –29. ISSN: 0370-2693. DOI: 10.1016/j.physletb.2012.08.020. URL: http://www.sciencedirect.com/science/article/pii/S037026931200857X.

[5] CMS Collaboration. "Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC". In: *Physics Letters B* (2012).

[6] ATLAS Collaboration. *Letter of Intent for the Phase-I Upgrade of the ATLAS Experiment*. Tech. rep. CERN-LHCC-2011-012. LHCC-I-020. Geneva: CERN, 2011.

[7] ATLAS Collaboration. *Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment*. Tech. rep. CERN-LHCC-2012-022. LHCC-I-023. Draft version for comments. Geneva: CERN, 2012.

[8] M. Capeans et al. *ATLAS Insertable B-Layer Technical Design Report*. Tech. rep. CERN-LHCC-2010-013. ATLAS-TDR-19. Geneva: CERN, 2010.

[9] V. Cindro et al. "The ATLAS beam conditions monitor". In: *JINST* 3 (2008), P02004. DOI: 10.1088/1748-0221/3/02/P02004.

[10] K. Kleinknecht. *Detektoren für Teilchenstrahlung*. 3-8351-0058-0: Teubner, 2005.

[11] W.R. Leo. *Techniques for Nuclear and Particle Physics Experiments: A How-to Approach*. 978-3540572800: Springer, 1994.

[12] J. Beringer et al. "Review of Particle Physics". In: *Phys. Rev. D* 86 (1 2012), p. 010001. DOI: 10.1103/PhysRevD.86.010001. URL: http://link.aps.org/doi/10.1103/PhysRevD.86.010001.

[13] J. Große-Knetter. "Vertex Measurement at a Hadron Collider - The ATLAS Pixel Detector". Habilitation thesis. University of Bonn. 2008.

[14] R. Turchetta. "Spatial resolution of silicon microstrip detectors". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 335.1 (1993), pp. 44–58.

[15] E. Rutherford. "The scattering of α and β particles by matter and the structure of the atom". In: *The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science* 21.125 (1911), pp. 669–688.

[16] G.R. Lynch and O.I. Dahl. "Approximations to multiple Coulomb scattering". In: *Nuclear Instr. Met. B* 58 (1991), pp. 6–10. DOI: 10.1016/0168-583X(91)95671-Y.

[17] V.L. Highland. "Some Practical Remarks on Multiple Scattering". In: *Nucl.Instrum.Meth.* 129 (1975), p. 497. DOI: 10.1016/0029-554X(75)90743-0.

[18] G.R. Lynch and O.I. Dahl. "Approximations to multiple Coulomb scattering". In: *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms* 58.1 (1991), pp. 6–10.

[19] F. Ragusa and L. Rolandi. "Tracking at LHC". In: *New Journal of Physics* 9.9 (2007), p. 336.

[20] W. Blum and L. Rolandi. *Particle detection with drift chambers*. 978-3-540-76683-4: Springer, 2008, p. 201.

[21] R.L. Gluckstern. "Uncertainties in track momentum and direction, due to multiple scattering and measurement errors". In: *Nuclear Instruments and Methods* 24 (1963), pp. 381–389.

[22] P. Rossi L. Fischer, T. Rohe and N. Wermes. *Pixel detectors: From fundamentals to applications*. Springer, 2006.

[23] N.W. Ashcroft and N.D. Mermin. *Solid State Physics*. Cengage Learning Emea, 1976. ISBN: 978-0030839931.

[24] T. Wittig. "Slim Edge Studies, Design and Quality Control of Planar ATLAS IBL Pixel Sensors". PhD thesis. University of Dortmund, 2013.

[25] C. Leroy and P.-G. Rancoita. *Silicon Solid State Devices and Radiation Detection*. 978-9814390040: World Scientific Pub Co, 2012.

[26] S.M. Sze and K.K. Ng. *Physics of semiconductor devices*. Wiley-interscience, 2006.

[27] R. Wunstorf. "Systematische Untersuchungen zur Strahlenresistenz von Si-Detektoren für die Verwendung von HEP-Experimenten". PhD thesis. 1992.

[28] J.-W. Tsung et al. "Signal and noise of Diamond Pixel Detectors at High Radiation Fluences". In: *JINST* 7 (2012), P09009. DOI: 10.1088/1748-0221/7/09/P09009. arXiv: 1206.6795 [physics.ins-det].

[29] M. Moll. "Radiation Damage in Silicon Particle Detectors - microscopic defects and macroscopic properties -". PhD thesis. University of Hamburg, 1999.

[30] T.-P. Ma and P.V. Dressendorfer. "Ionizing radiation effects in MOS devices and circuits". In: (1989).

[31] P.S. Winokur et al. "Two-stage process for buildup of radiation-induced interface states". In: *Journal of Applied Physics* 50.5 (1979), pp. 3492–3494.

[32] F.B. McLean, H.E. Boesch Jr. and T.R. Oldham. "Electron-hole generation, transport, and trapping in SiO2". In: *Ionizing radiation effects in MOS devices and circuits* (1989), pp. 87–192.

[33] T. Calin, M. Nicolaidis and R. Velazco. "Upset hardened memory design for submicron CMOS technology". In: *Nuclear Science, IEEE Transactions on* 43.6 (1996), pp. 2874–2878.

[34] T. Flick. "Overview of the Insertable B-Layer (IBL) Project of the ATLAS Experiment at the Large Hadron Collider at CERN". In: ATL-INDET-PROC-2013-006 (2013).

[35] T. Lari. "Lorentz angle variation with electric field for ATLAS silicon detectors". In: (2001).

[36] J. Albert et al. "Prototype ATLAS IBL Modules using the FE-I4A Front-End Readout Chip". In: *J. Instrum.* 7.arXiv:1209.1906 (2012). Comments: 45 pages, 30 figures, submitted to JINST, P11010. 45 p.

[37] F. Hügging. "Der ATLAS Pixelsensor - Der state-of-the-art Pixelsensor für teilchenphysikalische Anwendungen mit extrem hohen Strahlungsfeldern". PhD thesis. University of Dortmund.

[38] P. Weigell. "Recent results of the ATLAS upgrade planar pixel sensors R&D project". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 0 (2013). ISSN: 0168-9002. DOI: 10.1016/j.nima.2013.05.009. URL: http://www.sciencedirect.com/science/article/pii/S0168900213005342.

[39] A.A. Ayon, R.L. Bayt and K.S. Breuer. "Deep reactive ion etching: a promising technology for micro-and nanosatellites". In: *Smart materials and structures* 10.6 (2001), p. 1135.

[40] G. Aad et al. "ATLAS pixel detector electronics and sensors". In: *Journal of Instrumentation* 3.07 (2008), P07007.

[41] D. Arutinov et al. "Digital architecture and interface of the new ATLAS Pixel Front-End IC for upgraded LHC luminosity". In: *Nuclear Science, IEEE Transactions on* 56.2 (2009), pp. 388–393.

[42] M. Barbero et al. "Submission of the first full scale prototype chip for upgraded ATLAS pixel detector at LHC, FE-I4A". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 650.1 (2011), pp. 111–114.

[43] M. Barbero et al. "FE-I4 ATLAS pixel chip design". In: *PoS (VERTEX 2009)* 27 (2009).

[44] M.-A. Karagounis. "Analog Integrated CMOS Circuits for the Readout and Powering of Highly Segmented Detectors in Particle Physics Applications". PhD thesis. FernUniversität Hagen.

[45] L. Gonella et al. "The shunt-LDO regulator to power the upgraded ATLAS pixel detector". In: *JINST* 7.01 (2012), p. C01034. URL: http://stacks.iop.org/1748-0221/7/i=01/a=C01034.

[46] V. Gromov and R. Kluit. "A Radiation Hard Current Reference Circuit in a Standard 0.13 µm CMOS Technology." In: *Topical Workshop on Electronics for Particle Physics* (2008), pp. 494–496.

[47] V. Gromov et al. "A radiation hard bandgap reference circuit in a standard 0.13 µm CMOS technology". In: *Nuclear Science, IEEE Transactions on* 54.6 (2007), pp. 2727–2733.

[48] L. Gonella, F. Hugging and N. Wermes. "Towards minimum material trackers for high energy physics experiments at upgraded luminosities". In: *Nucl.Instrum.Meth.* A650 (2011), pp. 202–207. DOI: 10.1016/j.nima.2010.11.162.

[49] M. Backhaus et al. "Development of a versatile and modular test system for ATLAS hybrid pixel detectors". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 650.1 (2011), pp. 37–40.

[50] M. Havránek et al. "Measurement of pixel sensor capacitances with sub-femtofarad precision". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* (2013).

[51] A. Widmer and P. Franaszek. "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code". In: *IBM, J. Res. Dev.* 27 (1983), pp. 440–451.

[52] D.-L. Pohl. *Overview of the ATLAS Insertable B-Layer (IBL) Project*. Tech. rep. ATL-INDET-PROC-2013-008. Geneva: CERN, 2013.

[53] M. Backhaus. “Characterization of the FE-I4B pixel readout chip production run for the ATLAS insertable B-layer upgrade”. In: *JINST* 8 (2013), p. C03013. DOI: 10.1088/1748-0221/8/03/C03013. arXiv: 1304.4424 [physics.ins-det].

[54] M. Backhaus. “Characterization of new hybrid pixel module concepts for the ATLAS Insertable B-Layer upgrade”. In: *JINST* 7 (2012), p. C01050. DOI: 10.1088/1748-0221/7/01/C01050. arXiv: 1202.3592 [physics.ins-det].

[55] L. Gonella. “Low mass hybrid pixel detectors for the high luminosity LHC upgrade”. PhD thesis. University of Bonn, 2013.

[56] I. Rubinskiy. “An EUDET/AIDA Pixel Beam Telescope for Detector Development”. In: *Physics Procedia* 37 (2012), pp. 923–931.

[57] I. Peric. “Active pixel sensors in high-voltage CMOS technologies for ATLAS”. In: *JINST* 7 (2012), p. C08002. DOI: 10.1088/1748-0221/7/08/C08002.

[58] I. Perić et al. “High-Voltage Pixel Detectors in Commercial CMOS Technologies for ATLAS, CLIC and Mu3e Experiments”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* (2013).

Acknowledgements

At this place I want to thank the people who enabled me to complete the work presented in this thesis. This is in particular Prof. Dr. Norbert Wermes. I have highly enjoyed working in his group and with him. I want to thank him especially for the support and trust during all the time and for sharing his knowledge and experience with me.
The immense expertise in the group is also based on the people of the group who supported me on a daily basis. It would be a long list to call each of them by name. In particular, I am deeply grateful to Dr. Fabian Hügging for his great support, endurance in explanations and his trust in my work and opinion, and for staying relaxed and reasonable in turbulent times. But I may not forget Dr. Hans Krüger and Prof. Dr. Marlon Barbero for their significant contribution to the support I enjoyed and the knowledge I gained in the past four years. Thanks to all three also for proof reading this thesis.

An outstanding thank goes to my colleague, office mate and friend Dr. Laura Gonella. It was a pleasure to work with you and to have breakfast and coffee with you. I know we benefit from each other, not only during work, but also in life. I wish this continues wherever and on whatever we work on in the future.
Thanks also to the rest of the crew for the great collaboration, relaxed atmosphere, inspiring discussions, and all the social times, not at least on Wednesday evenings. It was a pleasure to collaborate with all of you. I want to call by name David-Leon Pohl and Theresa Obermann for their contribution on the wafer probing and module production tests.
A special thanks goes to Andreas Eyring for his encouraging and cheery mood, and for all the simple and honest solutions he provided, not only at work, but in particular as an life experienced friend.
I have profited and learned a lot from the collaboration with colleagues and friends from other institutes. I want to express my gratitude to all of them, in particular Silke Altenheiner, Matthias George, Dr. Jens Weingarten, and Dr. Jörn Große-Knetter.

I definitely can not thank every friend at this place who deserves it. But I want to express my exceptional thankfulness to Nils Hein and Anne Voigtländer, who catched me when I was falling, build me up when I was broken, slowed me down when I was euphoric, and last but not least, fed me when I was hungry. Long story short: thank you for being my closest friends.

My sincere and particular thanks goes to Annika Simon for accompanying me during three years of my Ph.D. and all the time before.

I want to thank also my parents, my siblings, my aunt and uncle, the whole family, for the endless support and understanding in the good as well as in the bad times. It is reassuring to know that you all are there to strengthen my back and support me if necessary. You are the basis on which I finished this work.