Evaluation of a Serial Powering Scheme and its Building Blocks for the ATLAS ITk Pixel Detector

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Abstract

The high luminosity upgrade for the Large Hadron Collider (LHC) at CERN requires a complete redesign of the current inner detectors of ATLAS and CMS. These new inner detectors will consist of all-silicon tracking detectors, combining multiple layers of silicon hybrid pixel modules and strip detectors. In the new pixel detectors conservative powering schemes are not feasible anymore. Instead serial powering has been chosen as a baseline powering scheme for both the future ATLAS and CMS pixel detectors. In serial powering, multiple detector modules are powered by a constant supply current. This new powering scheme provides challenges for the electrical and mechanical design, from the readout chip to system level considerations.

The main building block of the serial powering scheme foreseen for the ATLAS ITk pixel detector is the shunt low dropout voltage regulator (Shunt-LDO). The Shunt-LDO generates the local supply voltages for each pixel module from the constant supply current while shunting any excess current not drawn by the readout chips. In this thesis the Shunt-LDO is extensively characterised and evaluated. The expanding feature set of the Shunt-LDO has been verified over several years of development and the radiation hardness of the regulator design in the 65 nm CMOS process node used for the ATLAS ITk pixel readout chips has been proven. The operation and performance of next-generation pixel readout chips using the Shunt-LDO was demonstrated using RD53A, a technology demonstrator for the future ATLAS and CMS pixel readout chips.

An additional focus of this work is the large scale prototyping of serial powering. In the context of this work the Outer Barrel Demonstrator (OBD) program at CERN was commissioned and yielded first valuable experiences in operating a serially powered pixel detector with representative services and local supports. The OBD was the first prototype to operate multiple parallel, electrically coupled serial powering chains successfully. Finally a serial powering chain with pixel detector modules based on the next-generation readout chip, the RD53A, has been scoped, designed and set up in the context of this thesis with the goal to study low-level properties of serially powered detectors. This prototype, consisting of 8 RD53A quad chip modules with planar silicon sensors, demonstrated the ability to operate a serial powering chain with modules based on the next-generation readout chips without any performance deterioration.

Contents

Introduction

A major driving factor for humanity is the constant pursuit of knowledge, striving towards an understanding of the universe we live in - from the largest of structures in the cosmos, macroscopic phenomena in nature and society, down to the very building blocks of nature. Modern particle physics contributes to this quest, aiming to investigate the fundamental structure of matter, the (elementary) particles and their interactions.

Ironically, the investigation of the smallest particles known to exist requires experiments of unprecedented scale. In these experiments, particles are accelerated close to the speed of light and collide at tremendous energies, creating an environment similar to the immediate aftermath of the birth of the universe. In these collisions new particles are created. These particles often are not stable and decay within fractions of a fraction of a second. Nonetheless, their decay products can be detected using modern particle detectors. The properties of the particles created offer insights in the underlying physics processes and fundamental forces involved. Unfortunately interactions suited to probe and improve modern particle physics theories, most prominently the Standard Model of particle physics, are very rare and require many collisions to ever be recorded.

The most prominent example in recent times was the discovery of the Higgs boson in 2012 at the Large Hadron Collider (LHC) [1, 2]. More than 1 000 000 000 particle collisions were required on average to produce a single Higgs boson. The detectors tasked to record these rare particle signatures and their decay products need to be highly sensitive and fast, all while being exposed to a harsh environment. The two general purpose experiments are the A Toroidal LHC ApparatuS (ATLAS) and Compact-Muon-Solenoid (CMS) detectors at the LHC. They move at the forefront of technology, demanding new innovations and providing opportunities for new developments in many fields, from the design of integrated circuits to the engineering challenges of building large detectors. The next step in these developments is the upcoming luminosity upgrade of the LHC. This upgraded LHC will once again present

the experiments with unprecedented challenges, driving some of the most complex and ambitious projects in the history of particle physics. These challenges are tackled by the installation of upgraded detectors for both ATLAS and CMS. These massive projects - the ATLAS detector alone is comparable in size to roughly half the Notre Dame cathedral in Paris [3] - are undertaken by large international collaborations.

The focus in this thesis is on the upgrade of the innermost part of ATLAS - the tracking detector. The upgrade of this detector towards the new ATLAS Inner Tracker (ITk), introduced in Section 1.2.2, faces one of its most important challenges in the question of how to realize a high-performance, low material particle detector with acceptable power distribution efficiency. Conservative approaches to this very fundamental issue of delivering power to the detector will fail in the ITk pixel detector. Instead a novel approach has been chosen for the ITk pixel detector in Serial Powering, a concept introduced in Chapter 3.

Components and building blocks of this novel powering scheme have been in development over the past two decades and are reaching the maturity required for deployment in the ATLAS ITk pixel detector. One example for such a building block is the Shunt-LDO voltage regulator, a crucial part in the serial powering scheme employed by ATLAS. Chapter 4 presents contributions to this development in the characterisation and evaluation of the shunt low dropout voltage regulator (Shunt-LDO), from the first implementation in the new 65 nm technology to a mature implementation for the final application specific integrated circuit (ASIC) used in both the future ATLAS and CMS pixel detectors.

The implications of serial powering are however not limited to the scale of microelectronics. They require extensive prototyping on large scales to cover the system aspects of serial powering. These efforts are far beyond the scale of a single PhD thesis and involve large collaborations on their own. This work contributed to these efforts on mainly two aspects, both covered in Chapter 5: the Outer Barrel Demonstrator program at CERN as well as a small scale serial powering prototype, built from novel pixel detector ASICs in the SiLAB[1], as part of the larger ATLAS system test community.

1.1 The Large Hadron Collider

The LHC [4] is currently the largest and most powerful particle accelerator and largest machine ever built. It is built and operated by the European Organization for Nuclear Research (CERN) and located in the border region between France and Switzerland near Geneva. The LHC reuses the existing tunnel infrastructure of its direct predecessor LEP[2] between 45 m and 170 m underground. Figure 1.1 shows an overview of the scale and general location of

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[1] **S**ilizium **LA**bor **B**onn

[2] Large Electron-Positron Collider, constructed in 1989 and decommissioned in 2000 in favour of the LHC.
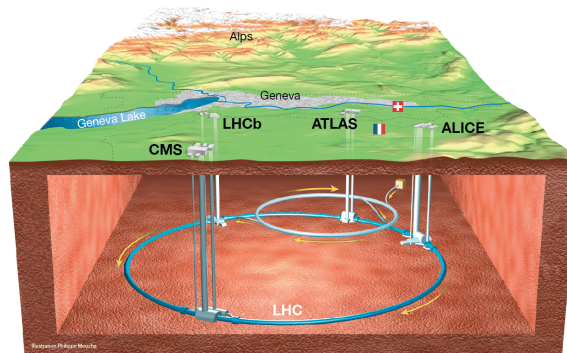
Figure 1.1: Overall view of the LHC. View of the 4 LHC detectors: ALICE, ATLAS, CMS and LHCb [5].

the LHC and the four largest experiments at the LHC. The LHC is part of the extensive accelerator infrastructure at CERN and directly supercedes the Super Proton Synchrotron (SPS). The LHC is a superconducting and symmetric proton-proton collider, accelerating and colliding protons in four different interaction regions with a design center-of-mass energy of 14 TeV at a design collision frequency of 40 MHz. At the four interaction points the four large LHC experiments are located: The two general purpose experiments ATLAS [6] and CMS [7], the heavy-ion focused ALICE [8] experiment and LHCb [9], focused on b-physics and measurements of CP violation.

The LHC has been in operation since the end of 2009, albeit with a reduced center-of-mass energy of 7 TeV at first. In this time data collected at the LHC has contributed significantly to research efforts concerning the standard model of particle physics. The most famous discovery at the LHC so far is without doubt the discovery of the Higgs boson by both ATLAS and CMS in 2012, a particle predicted in 1964.

A key figure to quantify the performance of a collider like the LHC is the *instantaneous luminosity* $\mathcal{L}$. Together with the cross section of interest σ_{exp} the total number of events N_{exp} is given as

$$N_{\text{exp}} = \sigma_{\text{exp}} \cdot \int \mathcal{L}(t)dt. \tag{1.1}$$

Today's particle accelerators accelerate beams of bunched particles instead of continuous beams. Each of these particle bunches contains a number N_p of particles and a number n_b of bunches form each of the colliding beams. Using a form factor F to describe the transverse beam profiles and incident angles in the collision point and the collision frequency f, it holds

for the instantaneous luminosity

$$\mathcal{L} \propto \frac{N_p^2 n_b f}{4\pi F},\tag{1.2}$$

assuming $N_{p,1} = N_{p,2} = N_P$. For the LHC the design peak luminosity is given as $10^{34}\,\mathrm{cm^{-2}\,s^{-1}}$ at a center-of-mass energy of 14 TeV. Both the ATLAS and CMS detectors are designed to be able to cope with this luminosity for the expected life span of the LHC of approximately 15 years, until 2025. This time span includes several long shutdown periods spanning from the months long end-of-year shutdowns to longer maintenance works. The amount of proton-proton collisions in this time-frame is usually not given as an absolute number of collisions but instead expressed in terms of the *integrated luminosity* $\mathcal{L}_{\mathrm{int}} = \int \mathcal{L}\mathrm{d}t$ in units of inverse barn[3]. As of 2020, the LHC has delivered a total integrated luminosity of approximately $190\,\mathrm{fb^{-1}}$ over its first two runs combined. Until the end of life of the LHC an additional $260\,\mathrm{fb^{-1}}$ are expected to be delivered at the LHC design center-of-mass energy of 14 TeV [10].

With rare processes and events having exceedingly small cross sections such a large number of collisions is necessary to allow any precision measurements and significant discoveries in particle physics. As an example, the total production cross section for the Higgs boson from proton-proton collisions is roughly 60 pb [11]. Following Equation 1.1 in the first two runs of the LHC only roughly $1.1 \cdot 10^7$ collisions involving Higgs bosons have been produced at the LHC. For actual data analysis only a small subset of these collisions is available however, as the acceptance and efficiency of the detector as well as the different production- and decay-channels have to be taken into consideration. As a statistical process, the error of any measurement conducted with a particle detector scales with the number of observed events as

$$\sigma_{\mathrm{stat}} \propto \frac{1}{\sqrt{N_{\mathrm{Event}}}},\tag{1.3}$$

and thus halves if the amount of data is quadrupled. Consequently for rare processes, a very large number of proton-proton collisions is necessary to achieve sufficient sensitivity. For investigations of possible beyond-standard-model physics with an even smaller cross section, even more collisions are necessary.

1.1.1 The High-Luminosity LHC

With the current luminosity a significant decrease in statistical errors at the LHC is not feasible with several years of runtime only yielding marginal improvements. Additionally especially the inner parts of the ATLAS and CMS detectors will quickly exceed their radiation

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[3] $1\,\mathrm{b} = 100\,\mathrm{fm^2}$

Figure 1.2: Project schedule for the HL-LHC taken from [10]. The upgrade to the HL-LHC will take place starting around 2026, as of January 2022.

tolerance, reducing the detection efficiency by a large margin.

In order to address this, the LHC will be upgraded to the High Luminosity Large Hadron Collider (HL-LHC) after the third run period starting in 2022 [10], increasing the instantaneous luminosity by a factor of up to 7.5 to roughly

$$\mathcal{L} \leq 10^{35} \mathrm{cm}^{-2}\,\mathrm{s}^{-1}. \tag{1.4}$$

Such an upgrade requires a major overhaul of the LHC infrastructure, including new superconducting magnets, accelerating cavities and novel technologies to further increase the luminosity in the interaction region. Research and development efforts for the accelerator upgrade have been progressing in parallel to the physics program during the past years. In Figure 1.2 an overview of the LHC schedule, including past physics runs, the accelerator upgrade progress and the future HL-LHC runs, are shown. The HL-LHC upgrade will allow the LHC to remain at the forefront of particle physics for the next decades.

1.2 The ATLAS Experiment

With a length of 45 m and a diameter of 25 m the ATLAS experiment is the largest particle detector built to this day. It is one of the general purpose particle detectors at the LHC aimed
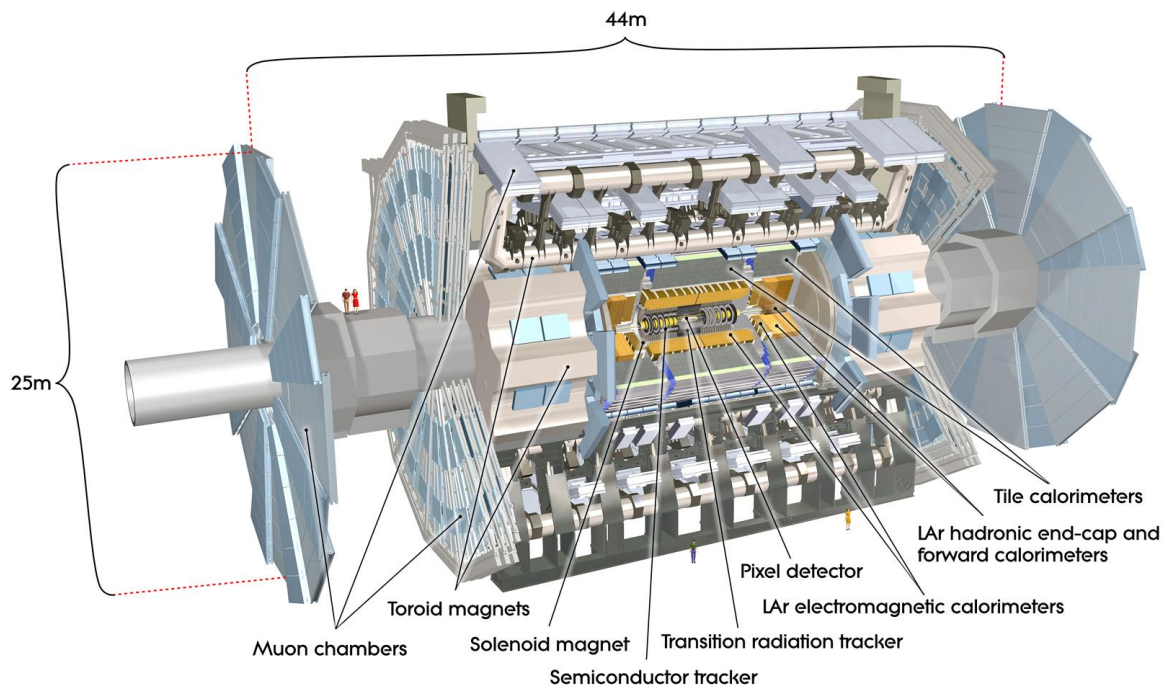
Figure 1.3: Computer generated image of the whole ATLAS detector. Two people are shown true to scale as a reference [12].

at finding as many different physics signatures as possible. A computer generated image of the ATLAS detector is shown in Figure 1.3. The ATLAS detector utilizes a large range of different particle detection techniques in different sub-detectors. These sub-detectors are deployed in multiple layers around the interaction region and can be categorized as barrel sections surrounding the beam pipe and disk layers perpendicular to the beam pipe, see also Figure 1.3. Functionally the ATLAS detector can be categorized in three different groups, starting from the interaction region.

Closest to the beam pipe is the inner detector, the ATLAS Inner Detector (ID), enclosed by a solenoid magnet system, which generates a 2 T magnetic field inside the ID volume parallel to the beam pipe. This magnet field allows the measurement of particle momentum based on track curvature for charged particles. The ID further measures particle trajectories, or tracks. With the primary and secondary interaction vertices being reconstructed from these tracks, the ID contributes significantly to event reconstruction in ATLAS.

Following the ID are the calorimeters in the ATLAS detector. The calorimeters consist of alternating and layers of absorber material and active detector layers. In the absorber layer, cascades of secondary particles, known as showers, are generated from the energy deposited

in the absorber from an incident particle. The active detector layer measures these secondary particles and their energy. Depending on the choice of absorber material and thickness, the calorimeter can be specialised for the detection of certain particles. In ATLAS, the innermost calorimeter is the Electromagnetic Calorimeter, which measures the energy of light charged particles and photons. It is followed by the Hadronic Calorimeter, which measures the energy of hadrons. Both the Electromagnetic Calorimeter and Hadronic Calorimeter are segmented to provide coarse spatial resolution. The calorimeters furthermore allow determination of the missing transverse energy, E_T, in a recorded event. E_T is a crucial quantity in a hadron collider, as only the initial transverse momentum in a collision of partons is known. This allows for the reconstruction of particles otherwise invisible for the detector, e.g. neutrinos.

Being a high-mass but not strongly interacting particle, the muon can traverse the inner layers of the ATLAS detector with most of its energy left. The unique combination of heavy mass, long lifetime and no strong interaction gives the muon a unique signature which allows the selection of events of interest for physics analyses. Therefore an additional detector layer is deployed at the outermost part of the ATLAS detector dedicated to measure traversing muons, the Muon Spectrometer. This detector consists of several layers of barrel and disc segments. In addition to the measurement of muon tracks, the momentum is measured by means of the track curvature in a toroidal magnet field surrounding the Muon Spectrometer. Depending on the location of the detector the bending field strength varies between $1.5 \leq X \leq 5.5$ T m in the barrel region of the spectrometer and $1 \leq X \leq 7.5$ T m in the disc region.

1.2.1 The ATLAS Inner Detector

The ATLAS ID consists of three subsystems. Closest to the beam pipe is the pixel detector, with the innermost layer of the pixel detector, the Insertable B-Layer (IBL), being directly attached on the beam pipe [13]. It is followed by a silicon strip detector, the SCT. The outermost part of the ID is the transition radiation tracker TRT consisting of $O(100)$ straw planes in both barrel and end-caps. A computer generated image of the original ID is shown in Figure 1.4.

The original ATLAS pixel detector consisted of three layers of pixels in both barrel and end-caps. In a major upgrade in 2013, an additional layer was introduced, the IBL [13]. Each of these layers consists of hybrid pixel detectors which offer excellent accuracy and can cope with the environment found close to the interaction region in terms of radiation tolerance and occupancy. The high granularity and performance of pixel detector comes at significant cost in both complexity, material introduced into the detector and resources required to assemble the detector.

The SCT, following the ATLAS pixel detector, consists of 4 double-sided layers of silicon strip detectors. As a strip detector, the SCT sacrifices segmentation in one dimension, thus
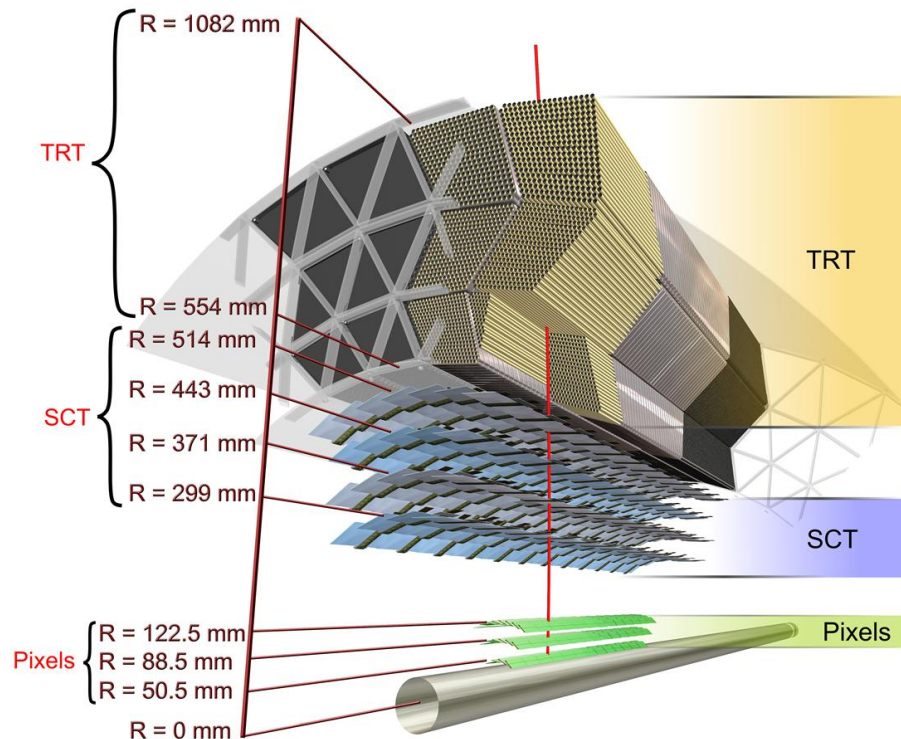
Figure 1.4: Computer generated schematic view of the original ATLAS ID without the IBL. Additionally shown in red is a charged track of 10 GeV p_T traversing the ID [14].

resolution, in favour of reduced complexity, detector material and cost. With an active area of approximately 61 m^2, the SCT is a pragmatic and cost-efficient choice compared to an extended pixel detector. Being much further away from the interaction region than the pixel detector, the requirements in terms of radiation - and occupancy tolerance for the SCT are much more relaxed compared to ATLAS pixel.

The TRT is a straw tube detector. This gaseous detector consists of more than 300 000 drift tubes 4 mm in diameter and approximately 1.5 m long. The space between the straw tubes is filled with gas with significantly different refractive index, promoting the generation of transition radiation, giving the TRT its name. The TRT enables effectively continuous tracking by providing a large number of measurement points per tracks, 36 on average, compared to 4 points in the pixel and strip detectors respectively. It provides a cost-efficient solution to cover the outer part of the ID at the cost of slightly reduced resolution and a
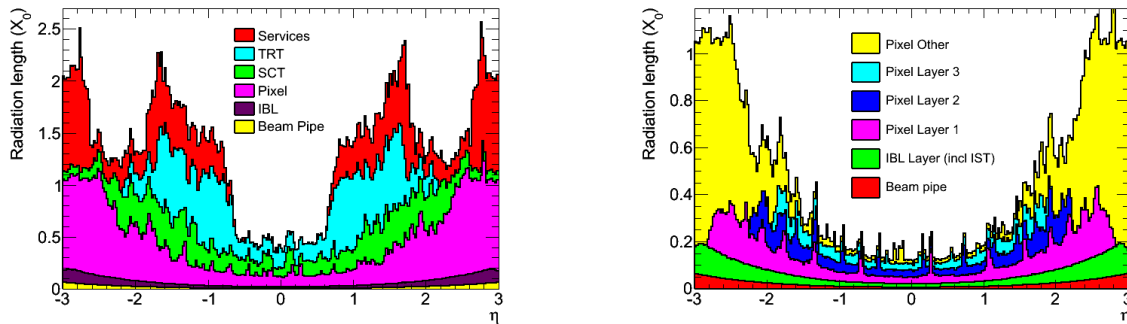
(a) Material budget of the full ATLAS ID.

(b) Material budget of the full ATLAS ID pixel.

Figure 1.5: Radiation length as a function of η for the different ID components as implemented in the ATLAS geometry model. Shown are the overall ID in Figure 1.5(a) and the pixel system in Figure 1.5(b) [13].

significantly lower tolerance to pile-up.

In Figure 1.5(a) the total material budget of the ATLAS ID including IBL is shown. Only contributions inside the detection volume are included, services and material outside the TRT is not shown. As can be seen the services of the ID provide the largest contribution to the detector material especially in the forward regions with larger η. As the services are obviously passive material in the detector they negatively impair the performance of the ID. It is thus especially important for the pixel detector to minimize the material budget, as the pixel detector offers the highest granularity on its own. In Figure 1.5(b) the material budget is shown for the pixel detector including IBL. In the forward region with approximately $|\eta| > 1.5$ the services dominate the material budget of the ATLAS pixel detector.

1.2.2 The ATLAS Phase 2 Upgrade and the ITk Project

The HL-LHC upgrade introduced in Section 1.1.1 provides two main challenges for detectors like the ATLAS detector, which are most pronounced in the inner part of the detector:

- An increase in integrated luminosity $\mathcal{L}_{int}$ corresponds to an increase in radiation dose received by the detector over the time of life.

- The increased instantaneous luminosity $\mathcal{L}$ leads to more interactions per bunch crossing, leading to higher occupancy in the detector. In Figure 1.6 the increase of particle interactions per bunch crossing in the ATLAS detector is shown over the last years. Each of these interactions results in several particles traversing the ATLAS detector. In the HL-LHC approximately 200 primary interactions are expected per bunch crossing.
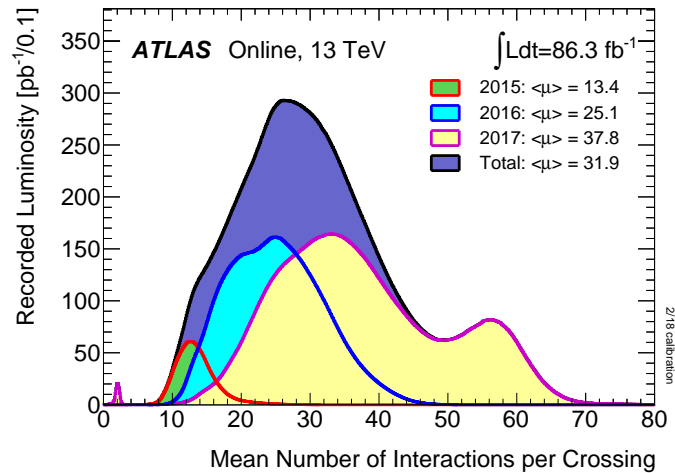
Figure 1.6: Luminosity-weighted distribution of the mean number of interactions per bunch crossing for proton-proton collisions at 13 TeV recorded between 2015 and 2018. [15].

For the inner detectors to be able to cope with such an increase in occupancy a higher granularity of the detector and larger data bandwidth is needed.

The current ATLAS ID is not able to cope with the requirements imposed by the HL-LHC. Especially the gaseous TRT is expected to be saturated at an instantaneous luminosity $\mathcal{L} < 5 \cdot 10^{34} \text{cm}^{-2} \text{s}^{-1}$. Instead the new tracking detector will be an all silicon tracker, consisting of pixels and strips. Simply expanding on the already installed pixel and SCT is not an option, as the currently installed hybrid pixel and microstrip detectors in the ATLAS ID will reach the limit of their capabilities by the end of Run 3. The requirements in terms of radiation hardness and rate capabilities can not be fulfilled by the currently employed detector technology. It is thus necessary to design a completely new inner detector with novel hybrid pixel and microstrip detectors. The new detector is referred to as the ATLAS ITk. A schematic layout of the ITk is shown in Figure 1.7.

In the current baseline layout the ITk consists of 5 layers of pixel modules and 4 layers of strip modules. The total dimensions of the ITk is constrained to the dimensions of the ATLAS ID: approximately 6 m in length with a radius of just below 1.1 m. To improve the physics performance, the ITk covers a larger range in the forward region up to $\eta < 4$ compared to $\eta < 2.5$ in the ATLAS ID. This results in an increase of the active area, resulting in approximately $200 \, \text{m}^2$ of active silicon area and more than 5 billion readout channels. The work presented in this thesis was conducted in the context of the ATLAS ITk pixel project.

In the ITk pixel detector different types of modules will be used to address the different challenges imposed by the HL-LHC. The detector will consist exclusively of hybrid pixel
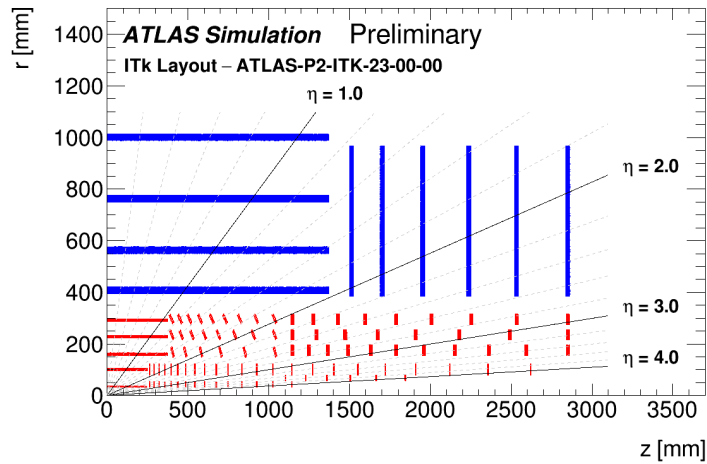
Figure 1.7: The schematic depiction of the ITk Layout, including the updated layout for the Pixel detector. Only one quadrant and only active detector elements are shown. The active elements of the strip detector are shown in blue, and those of the pixel detector are shown in red. The horizontal axis is along the beam line with zero being the interaction point. The vertical axis is the radius measured from the interaction region [16].

detector modules, see also Section 2.2. The majority of these modules will be quad chip modules, four readout chips, abbreviated as readout chip (ROC), bump bonded to a single sensor. In the innermost layer triplets of three single chip modules on a triplet flex printed circuit board (PCB) will be used. The modules in the innermost layer will utilize 3D sensors, which offer an increased radiation hardness and reduced power consumption. In the outer layers, planar sensors will be used, which are less radiation hard but easier to manufacture and more cost efficient. The complete inner system (IS) of the ITk pixel detector is designed to be replaceable after approximately half the time of life of HL-LHC. This is necessary as the projected radiation dose received after the full life time of HL-LHC exceeds the capabilities of any currently known detector technology. To reduce the pile-up in the ITk pixel detector, the granularity of the detector is increased. Compared to pixel sizes found in the ATLAS ID ranging between $50 \times 400 \, \mu m^2$ and $50 \times 250 \, \mu m^2$, the pixel size in the ITk pixel detector will be reduced to $50 \times 50 \, \mu m^2$ and $25 \times 100 \, \mu m^2$. The increased granularity and size of the pixel detector leads to a significantly larger power consumption of the full detector. A conventional parallel powering scheme as employed in the ATLAS ID pixel detector is simply impossible due to the spatial constraints in ITk. As a low-mass and power efficient alternative a Serial Powering serial powering (SP) scheme will be used for the ITk pixel detector, see Chapter 3. In Table 1.1 a comparison of key parameters of the ATLAS ID pixel detector + IBL to the future ITk pixel detector is given.

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	ATLAS Pixel + IBL	ITk Pixel
Modules	2000	8500
Pixel Size	$50 \times 400\,\mu m^2$ or $50 \times 250\,\mu m^2$	$50 \times 50\,\mu m^2$
Readout channels	80 million	5 billion
Active area	$1.7\,m^2$	$14\,m^2$
TID	$2.5\,MGy$	$10\,MGy$
Fluence	$10^{15}\,n_{eq}/cm$	$1.4^{16}\,n_{eq}/cm$
Trigger rate	$100\,kHz$	$1\,MHz$
FE data rate	$160\,Mb\,s$	$5.12\,Gb\,s$
Powering	parallel	serial
Cooling budget	$15\,kW$	$100\,kW$

Table 1.1: Comparing the current ATLAS Pixel detector including IBL with the future ITk Pixel detector.

CHAPTER 2

Silicon Pixel Detectors in High Energy Physics

Silicon is one of the most abundant and - for modern civilization - most important elements on earth. As a semiconductor it plays a crucial role in the modern electronics industry, which relies heavily on semiconductor devices to be able to fabricate integrated circuits and microelectronics. In a tracking detector like the ATLAS ITk, silicon is used both for the readout ASIC as well as the active detector volume - the sensor.

A tracking detector needs to provide sufficient spatial resolution, which is accomplished by segmenting the detector. Based on the layout of this segmentation, silicon tracking detectors can be differentiated as silicon strip detectors and silicon pixel detectors. Silicon strip detectors offer high granularity in one direction compared to silicon pixel detectors, which are finely segmented in two dimensions. Silicon strip detectors thus trade resolution and thus tracking performance for simplicity and lower cost. In a large tracking detector like ATLAS ITk with some $200\,\mathrm{m}^2$ active silicon surface, such a compromise is a necessity. Thanks to constant advances in the semiconductor industry, most importantly modern complementary metal-oxide-semiconductor (CMOS) processes with small feature sizes, pitches of a few μm between pixels or strips can be achieved.

Modern ASIC are fabricated on wafers, thin disks of crystalline silicon, which serve as the substrate for the later ASIC. From these wafers, typically 200 mm - 300 mm in diameter, the ASIC are cut after all undergoing several microfabrication process steps, e.g. doping, etching and photolithographic patterning. The resulting dies are typically only a few cm^2 in size. In the context of silicon pixel detectors, the pixel module is built from such dies. The module represents the most fundamental building block in a pixel detector.

2.1 Silicon Particle Detectors

Silicon particle detectors operate by reading out the electric signal due to the energy loss of an incident particle in the sensor volume. Such an incident particle, depending on the particle type and its energy, deposits energy in the silicon bulk, refer to Section 2.1.1. The active silicon sensor volume typically consists of a depleted space-charge region at the junction between p-doped and n-doped silicon. The energy deposited in the silicon generates free charge carriers, which immediately recombine with the silicon lattice, unless generated in the depletion region. Charge carriers freed in the depletion region instead drift in the electric field across the p-n-junction. This drift generates a signal in the readout electrodes connected to the sensor. Since the charge generated is proportional to the energy deposited in the sensor, the energy of incident particles can be measured with silicon detectors as well, provided they deplete all their energy in the active volume.

2.1.1 Particle Interaction with Matter

The interaction of particles with matter depends on the particle type and energy. For photons the dominant effects are the photoelectric effect, Compton scattering and pair production at high energies. In Figure 2.1(a) the resulting total absorption probability for photons in 300 μm silicon is shown. The photon is completely absorbed should it undergo pair production or be absorbed via the photoelectric effect. When interacting via Compton scattering the photon is instead scattered at a large angle. Consequently, the photon is completely absorbed with a certain probability when traversing through e.g. a silicon sensor.

Charged particles however continuously deposit energy in the detector material instead of being stopped immediately. Energy can be deposited in multiple ways, e.g.

- inelastic scattering with shell electrons,

- elastic scattering with atomic nuclei,

- radiation losses, e.g. bremsstrahlung, transition radiation or Cherenkov radiation,

- nuclear reactions.

The mean energy loss due to ionization per distance in an absorber material is described by the Bethe-Bloch equation [11]:

$$-\left\langle\frac{\mathrm{d}E}{\mathrm{d}x}\right\rangle = K\frac{Z}{A}\varrho\frac{z^2}{\beta^2}\left[\frac{1}{2}\ln\frac{2m_ec_0^2(\beta\gamma)^2T_{\max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right],\tag{2.1}$$

with

- $K = 4\pi N_A r_e^2 m_e c_0^2 = 0.307\,\text{MeV cm}^2\,\text{mol}^{-1}$, c_0 the speed of light in vacuum, m_e and r_e the electron mass and the classical electron radius,

- Z, A being the atomic number and nucleon number of the absorber material, ϱ the density of the absorber,

- z the charge of the incident particle,

- the Lorentz factors $\beta = \frac{v}{c_0}$ and $\gamma = \frac{1}{\sqrt{1-\beta^2}}$ describing the incident particle,

- the maximum energy transfer in a head-on collision $T_{\max} \approx 2 m_e c_0^2 (\beta\gamma)^2$,

- the Fermi density correction $\frac{\delta(\beta\gamma)}{2}$ important for incident particles with high energy.

- the material density ρ and the mean excitation energy I of the absorber material

The Bethe-Bloch equation gives a good approximation of the energy loss, or stopping power, for incident particle energies $0.1 \leq \beta\gamma \leq 1000$ with an accuracy of a few percent in different absorbers [11]. In Figure 2.1(a) the energy loss according to Equation 2.1 is shown for different absorber materials. For low particle energies with $\beta\gamma \leq 1$ the energy loss is strongly dependant on the initial energy. The energy loss reaches a local minimum around $\beta\gamma \approx 3$. For particle energies $3 \leq \beta\gamma \leq 1000$ the mean energy loss only increases moderately. Thus particles with $\beta\gamma \geq 3$ are commonly referred to as minimum ionizing particles, or MIPs. In silicon the energy loss of a MIP can be approximated [17] as

$$ -\left\langle \frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle_{\text{MIP,Si}} \approx 3.87\,\text{MeV cm}^{-1}. \tag{2.2} $$

For high energetic particles energy losses due to bremsstrahlung and other radiation effects become dominant. This is especially relevant for light leptons such as electrons, positrons and muons. Bremsstrahlung is not described by the Bethe-Bloch equation, as is the interaction of indistinguishable particles. Thus Bethe-Bloch does not describe the stopping power for electrons, which is dominated by bremsstrahlung. Energy loss by bremsstrahlung is proportional to the energy of the particle:

$$ -\left(\frac{\mathrm{d}E}{\mathrm{d}x} \right)_{\text{brems}} = \frac{E}{X_0}, \tag{2.3} $$

with the radiation length X_0 [17]. The radiation length is the mean path length in an absorber after which the incident particle's energy E_0 has been to reduced to $E = \frac{1}{e}E_0$. X_0 is a material
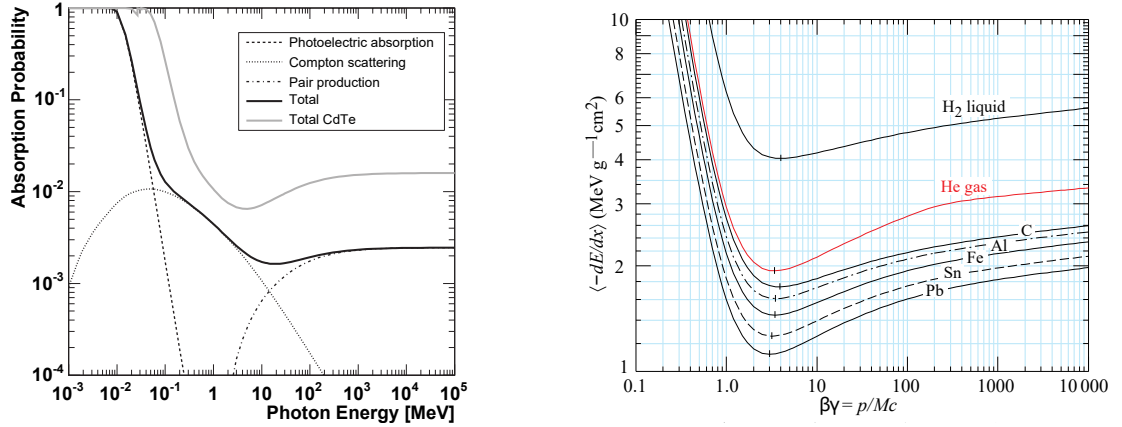
(a) Probability of photon absorption for 300 μm silicon as function of the photon energy. Contributions from different processes are indicated [18, p. 34].

(b) Mean energy loss rate of ionizing particles in matter as a function of relativistic energy $\beta\gamma$ as from Equation 2.1. Modified from [11, p. 537].

Figure 2.1: Absorption probability and energy loss rate for different particle types and energy in matter.

property of the absorber. In a mixture or compound of different materials, the total radiation length is approximated by

$$\frac{1}{X_0} = \sum \frac{\omega_j}{X_j}, \tag{2.4}$$

where X_j is the radiation length and w_j the fraction by weight of the j-th compound [11, p. 541]. In silicon the radiation length is approximately $X_{0,\mathrm{Si}} \approx 9.36$ cm [17, p. 65]. The radiation length is a common unit of measurement of the material budget of components in a particle detector.

2.1.2 Signal Generation and Detection

In a typical silicon pixel detector the active volume is the depletion region at the junction between p-doped and n-doped silicon. Considering as an example a typical n-in-p-type planar sensor, a weakly doped p-type silicon is chosen as the bulk material. The readout electrodes are implemented as segmented, highly doped n-silicon. Due to the different doping concentration in p-type and n-type silicon, when applying a reverse bias voltage, the depletion region at the p-n-junction can grow several 100 μm into the p-type bulk, effectively filling the full bulk of the sensor. In this example, the n-doped electrodes are kept at ground potential and the negative bias voltage is applied to the sensor backside. The sensor backside does not need to be segmented and only requires a metal interface to connect to the bias voltage.

Incident particles generate free charge carriers in the depletion region by exciting electrons from the valence band to the conduction band. This way two charge carriers are created: an free electron in the conduction band and a defect electron or hole in the valence band. The
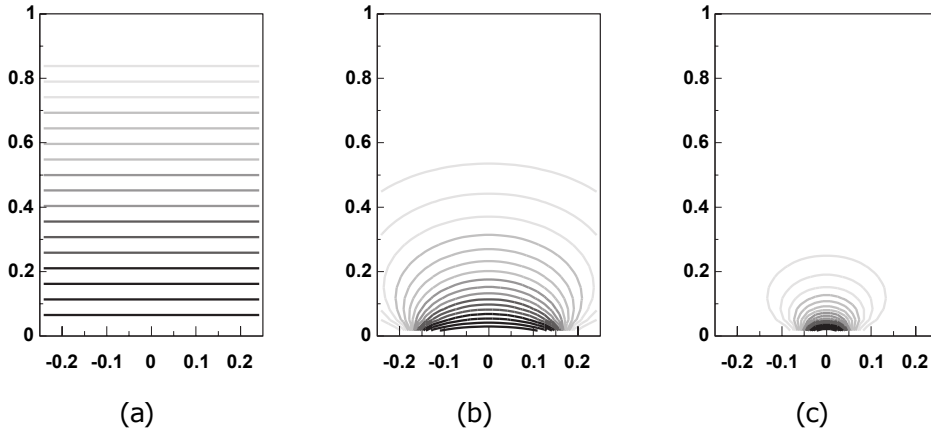
Figure 2.2: Weighting potential between two parallel electrodes of varying width on the X-axis, compared to the vertical bulk thickness on the Y-axis. The electrodes in (a) are of infinite size, 1/3 of the distance between the electrodes in (b) and 1/10 of the distance between the electrodes in (c) [18, p. 61].

average number of electron-hole pairs generated at room temperature is given by

$$N_{e^-h} = \frac{E}{\omega},\tag{2.5}$$

with the deposited energy E and the mean energy ω required to create an electron-hole pair. For silicon $\omega \approx 3.65\,\text{eV}$ [17].

The electric field present in the depletion region causes these charges to drift apart. The signal in the readout electrode is dominated by the current induced from the movement of charges in this electric field according to the Shockley-Ramo theorem [19]. The induced current is given as

$$i = e\vec{E}_\text{W}\vec{v},\tag{2.6}$$

with the charge carrier charge e, velocity $\vec{v}$ and the weighting field $\vec{E}_\text{W}$ [17, p. 135]. The weighting field for different electrode sizes is shown in Figure 2.2. For infinitely large electrodes a moving charge carrier will induce the same signal in the readout electrode for any part of its drift path. For small electrodes only charges drifting close to the electrode contribute meaningfully to the signal read out. In a pixel detector with several neighbouring readout electrodes the weighting fields of each electrode overlap. A charge created in one pixel cell can thus also induce a signal in neighbouring pixel in an effect referred to as charge sharing.

The silicon pixel sensor itself is typically characterized by its diode-like IV curve. The most important figures are the leakage current and the breakdown voltage. The leakage current is the amount of current flowing through the sensor as a function of the reverse bias voltage

applied. As the reverse bias voltage of a sensor is increased, the depletion zone in the sensor volume grows and the leakage current increases slightly. This increase in leakage current saturates once the sensor volume is fully depleted until the reverse bias voltage exceeds the breakdown voltage of the sensor, at which point the leakage current increases drastically. Such a breakdown can lead to irreversible damage to the sensor and is thus to be avoided. The breakdown voltage is strongly influenced by the sensor design. The pixel sensors used in the ITk pixel detector will utilize either planar sensors or 3D sensors. These sensor types have different internal structures, with the planar sensor having its readout electrodes parallel to the sensor surface, thus planar, and the 3D sensor electrodes being perpendicular to the sensor surface. 3D sensors offer a much increased radiation hardness due to the reduced drift length in the sensor, however are much more expensive to produce. Additionally breakdown occurs much quicker for 3D sensors compared to planar sensors, which needs to be considered in the design of the ITk pixel detector.

2.1.3 Spatial Resolution

A pixel detector with binary read out, i.e. no charge information is available, has a spatial resolution according to [17, p. 843]

$$\sigma_i = \frac{a_i}{\sqrt{12}}, \tag{2.7}$$

with a_i referring to the pixel pitch and σ_i to the resolution in x or y direction. For small pixels the charge signal can be registered by several neighbouring pixels. This leads to clusters in the hit data. If charge information is available the center of gravity of the cluster can be used as the mean hit position. This significantly improves on the spatial resolution. The spatial resolution when considering charge sharing follows as

$$\left(\frac{\sigma_i}{a_i}\right) = \frac{1}{2\pi^2} \sum_{m=0}^{\infty} \frac{1}{m^2} \cdot e^{-4\pi^2 m^2 \left(\frac{\sigma}{a}\right)^2}, \tag{2.8}$$

assuming gauss shaped signal distribution at the readout electrodes and neglecting noise. $\frac{\sigma}{a}$ denotes the width of the gaussian charge distribution in units of the width of the readout electrode. Assuming a gaussian charge distribution a near perfect reconstruction can be obtained for $\sigma \geq \frac{a}{2}$. In the limit of small signals $\frac{\sigma}{a} \rightarrow 0$, Equation 2.8 simplifies to Equation 2.7 [17, p. 844].
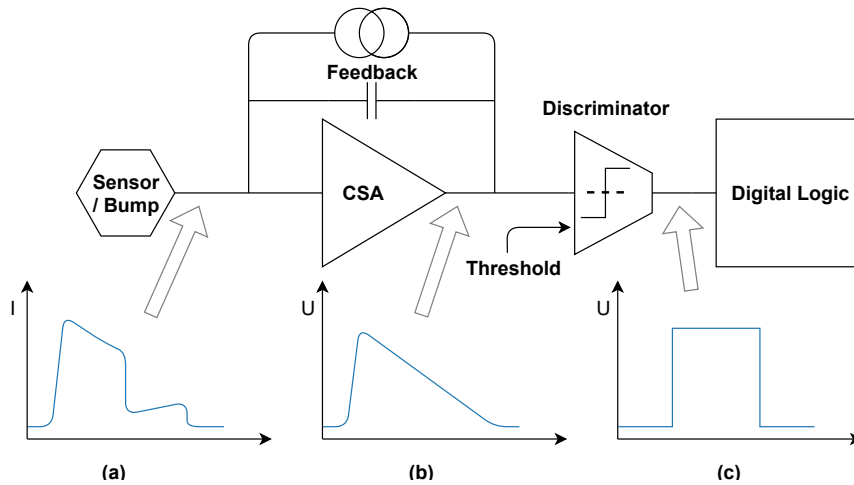
Figure 2.3: Generic pixel detector front-end electronic circuit. The signal shape is depicted as a current pulse coming from the sensor (a), the voltage pulse generated by the charge sensitive amplifier (CSA) in (b) and the discriminator output in (c). Taken from [20].

2.1.4 Signal Processing

The charge signal induced on the readout electrodes requires further processing and digitization. This is typically achieved by the analog front-end electronics (AFE) of a pixel detector as shown in Figure 2.3. The charge collection electrode of each sensor pixel is connected to the input node on the left hand side. Usually each sensor pixel is connected to its own dedicated readout electronics. The input signal is a charge pulse induced on the readout electrode of the sensor pixel as shown in Figure 2.3 (a). The first stage in the typical signal processing chain is a CSA, which converts the induced charge pulse into a voltage pulse by integrating the input signal. The amplitude of the CSA output signal is proportional to the integrated charge, while the slope of the falling edge depends on the feedback current. When using a constant current feedback as is done here, the falling edge of the CSA is linear as shown in Figure 2.3 (b). With a sufficiently steep rising edge, the width of the CSA output signal is thus proportional to the integrated charge as well. The CSA can be followed by additional amplification stages to increase the signal gain or shape the signal further.

The output signal of the amplification stage is fed into a discriminator, which compares the CSA output signal to a given threshold voltage. As the signal exceeds this threshold voltage the discriminator switches its output from low to high and vice versa, digitizing the output signal of the CSA. In an ideal case the discriminator output would be described by a step function, corresponding to the signal shown in Figure 2.3 (c). The width of the rectangular output signal of the discriminator corresponds to the duration for which the CSA output is above the threshold voltage of the discriminator and is referred to as time over threshold (ToT). As the width of the CSA output signal is approximately proportional to the input charge, the

19
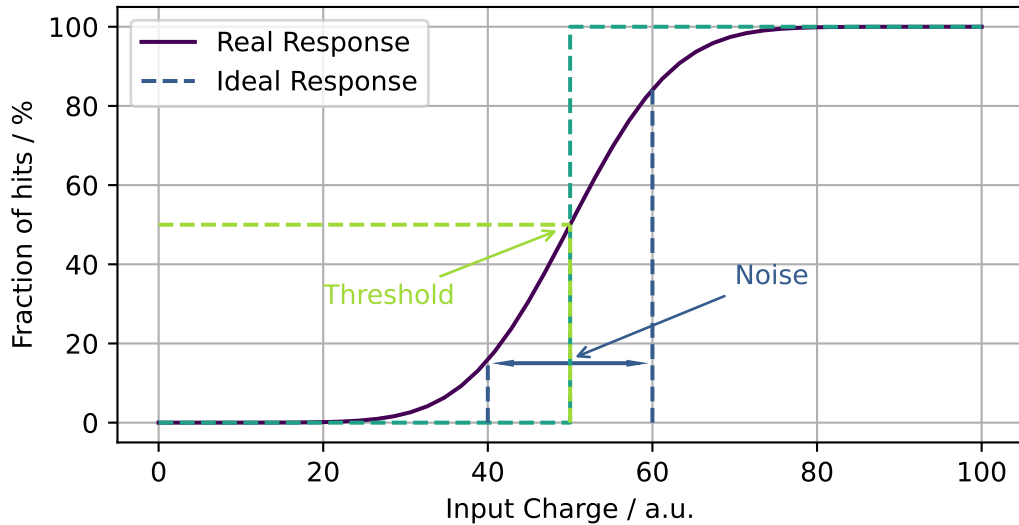
Figure 2.4: Arbitrary S-curve as defined in Equation 2.9. In addition the response of an ideal discriminator is given. The threshold is defined as the input charge for which 50 % of hits are recognized. The noise is derived from the width of the S-curve.

ToT is a measure of the energy deposited in the sensor. In the digital logic of the front-end the ToT is counted in units of clock cycles.

Due to electrical noise the response function of a discriminator does not follow an ideal step function but instead is described using the error function as [17, p. 753]

$$P_{\text{hit}}(Q_{\text{in}}) = 1 - \text{erf}\left(\frac{Q_{\text{in}} - \mu}{\sigma\sqrt{2}}\right). \tag{2.9}$$

Here, $P_{\text{hit}}(Q_{\text{in}})$ denotes the probability for a given charge Q to result in a high discriminator output level. μ is the threshold of the discriminator and σ denotes the noise. The resulting S-curve is shown in Figure 2.4. The threshold of the discriminator is then defined as the input charge Q_{in}, for which the probability of the discriminator output being high is 50 %. The noise contribution to the signal processing can be extracted from the width of the S-curve. Assuming gaussian distributed noise the relevant reference points for the width of the S-curve are $P_{\text{hit}}(Q_1) = 16\,\%$ and $P_{\text{hit}}(Q_2) = 84\,\%$. The resulting width corresponds to $1\,\sigma$ of the full noise.

2.2 Hybrid Pixel Detector Modules

In high energy physics applications silicon pixel detectors are the detectors of choice for the innermost layers of tracking detectors at particle colliders due to their excellent spatial and timing resolution. In addition pixel detectors can cope with the harsh environment present in the interaction points of particle colliders like the LHC. The pixel system in a detector like ATLAS plays a fundamental role in particle identification and reconstruction of primary and secondary vertices. The basic building block of the pixel system is the pixel module. For pixel modules two general design approaches can be used. Combining the active sensor and the readout electronics in the same silicon bulk yields a pixel module classified as a Monolithic Active Pixel Sensor, or MAPS. Alternatively the readout electronics and active volume can be realized in two independent silicon dies, which are then interconnected to form a hybrid pixel module. Both approaches have their inherent advantages and disadvantages [21]. In the ATLAS ID as well as the future ATLAS ITk hybrid pixel modules are used exclusively.

2.2.1 Modules

The hybrid pixel detector module traditionally consist of a silicon sensor connected to one or more readout chips using a flip chip process. Modern pixel detectors provide significant challenges for this flip chip process due to the very small pixel pitch and the large amounts of pixels per ASIC. While the high-density bump bonding process is a very expensive and error prone process, the hybrid pixel module offers significant advantages as the readout chip and sensor can be designed and optimized individually. A schematic view of a hybrid pixel module is shown in Figure 2.5. Here, the pixelated readout chip is on the bottom and bump-bonded to the sensor tile on the top. Typically the bump bonds are deposited on either the sensor tile or the readout chip before the sensor is placed on top of the readout chip face-down, thus flip chip. After necessary alignment the stack of sensor and readout chips is heated up until the bump bonds melt and form an electrical and mechanical connection between both chips. Wire bonding pads on the readout chip periphery, which is not covered by the sensor, provide connectivity to the services of the pixel detector.

Connection of the hybrid pixel module to the detector services, including power, data and control signals, is done using high density interconnect circuits, typically on a flexible PCB or module flex. Figure 2.6 shows the full module stack for a barrel module of the current ATLAS pixel detector.

The sensor in this ATLAS pixel module features 47232 pixels arranged in 144 columns and 328 rows for a total active surface of $6.08 \times 1.64 \mathrm{cm}^2$. Connected to this sensor are 16 readout chips with 2880 pixel cells each [23]. Glued to the sensor backside is the module flex, an approximately 100 µm thin PCB to route signals and power. Bias voltage for the sensor is
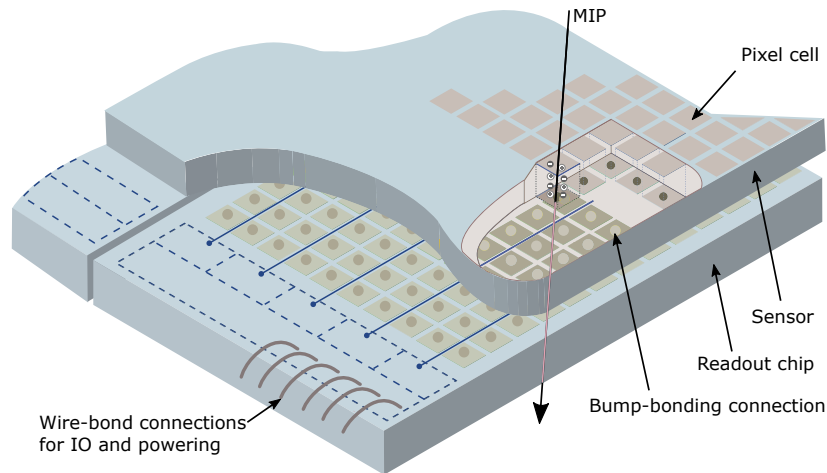
Figure 2.5: Schematic view of a hybrid pixel detector with square pixels. A MIP is shown to traverse through a single sensor pixel. Wire bond connections of the readout electronics are shown. Modified from [22].

applied via a dedicated hole in the sensor. Depending on the location of the pixel module, the module flex is directly connected to the Type-0 services or connected via an additional thin foil, called pigtail [23]. The material budget of a barrel layer pixel modules used in the ATLAS detector and perpendicular to the incident particle is $1.2\,\%X_0$, to which the different components contribute [24]:

- sensor: $0.32\,\%X_0$,

- bump bonds and readout chip: $0.27\,\%X_0$,

- flex hybrid: $0.39\,\%X_0$,

- pigtail: $0.22\,\%X_0$.

2.2.2 Services

The high granularity of a pixel detector directly translates into the need for a large amount of cables to service the detector in terms of power supply, data acquisition (DAQ) and control signals. This makes the services one of the most significant contributors to the overall material budget of a pixel tracking detector, see also Figure 1.5(b). Especially in the forward region, where cables leave the detector volume, the contribution from services to the material budget far exceeds the contribution from the actual detector. This degrades the performance of all following subdetectors in this region. Additionally such a large concentration of cables can make routing difficult as only limited space is available.
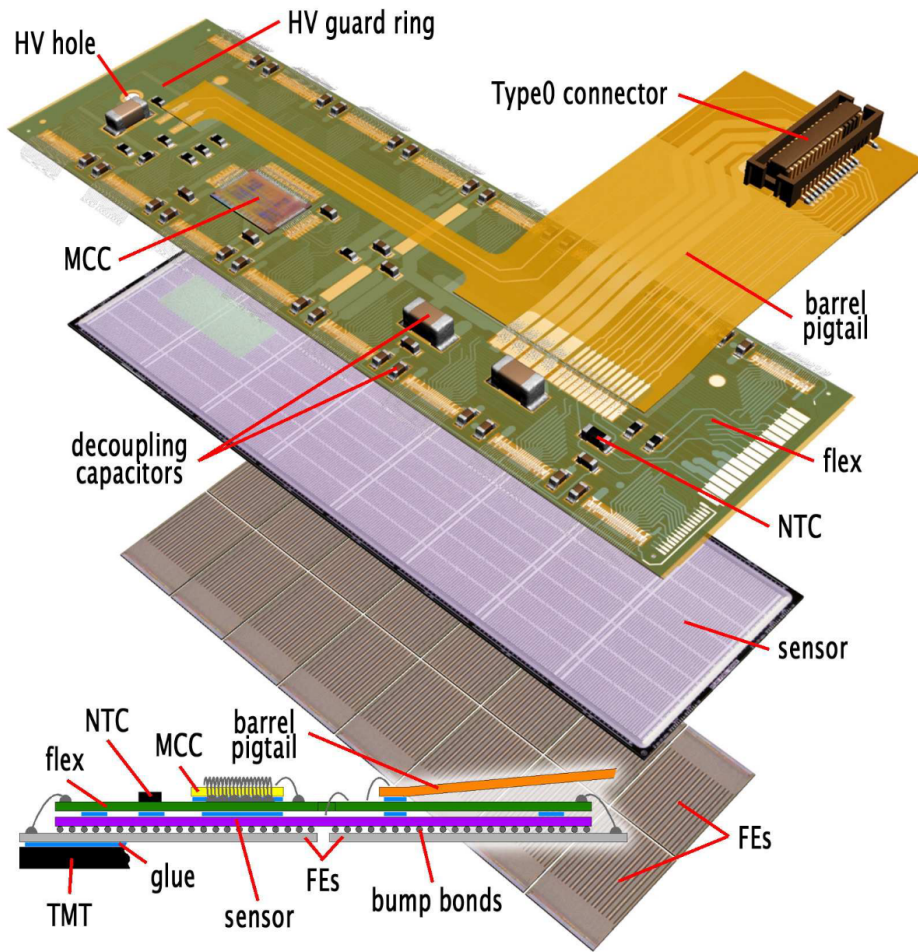
Figure 2.6: The elements of a pixel barrel module of the ATLAS ID pixel detector. The thermal management tile on which the module is glued is suppressed [23].

To mitigate these difficulties the services for the ATLAS pixel detector use a modular design as shown in Figure 2.7. The services can be disconnected at intermediate locations between the detector and the services cavern using patch panels. There are a total of 4 patch panels. Readout chip power low voltage (LV) and sensor bias voltage high voltage (HV) are routed from the power supplies to PP4. The HV is directly routed to PP1 via the Type IV HV cables. The LV is routed via Type IV, PP2 and Type II cables to PP1. From PP1 power is supplied to the module via the Type I and Type 0 services with the intermediate PP0. The Type 0 services connect directly to the module flex. Data transmission is done electrically from the module to PP0, as the high radiation levels do not allow optical data transmission. Initially from PP0 data is transmitted optically to the service room [25]. However due to radiation damage to the electro-optical converters, the conversion to optical signals now takes place in a better serviceable location outside the ID volume [26].
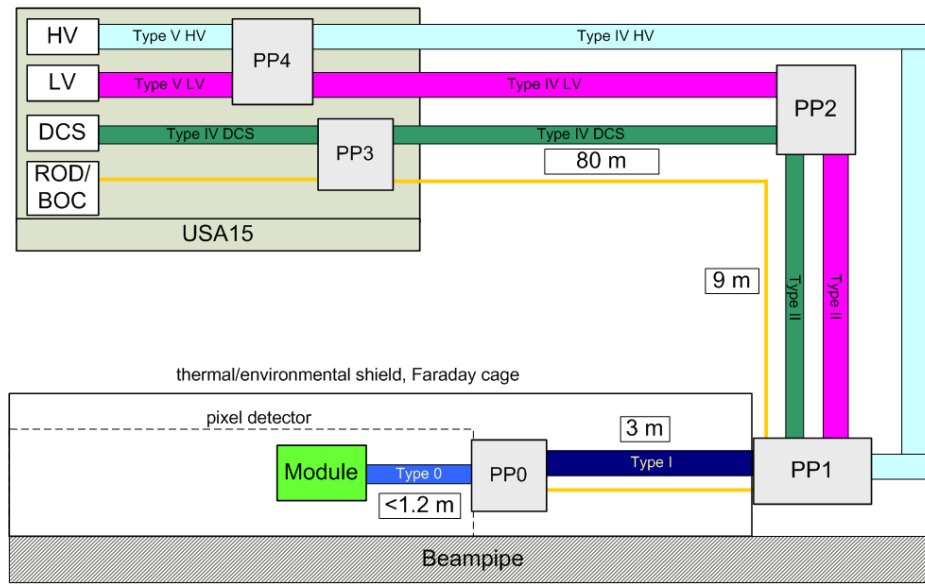
Figure 2.7: Simplified schematic view of the layout of the services for the ATLAS ID pixel detector [25].

Of these services a dominant fraction by mass is contributed by the LV cables. The ATLAS pixel detector with its millions of readout channels has a current consumption of approximately 3.7 kA [6, p. 82]. In traditional powering schemes as used for ATLAS pixel, power is either supplied directly from the power supply to the module in a direct or independent powering scheme or alternatively multiple modules are connected in parallel to a common LV line. Such powering schemes allow a high level of control over the pixel detector, as even single modules can be powered off at will. However with the large amount of pixel modules in a detector like ATLAS pixel, they introduce a large amount of material into the detector. To mitigate the contribution of these LV cables to the material budget of the detector, cables with a small cross section can be chosen. Of course depending on the cable material and the cross section A of the cables, a current dependent voltage drop V

$$A = l \cdot \frac{I}{V} \cdot \frac{1}{\sigma} \tag{2.10}$$

occurs with the current flow I and the conductivity of the cable σ. Minimizing A thus leads to an increase in V, as the total cable resistance increases. This increases the power losses on the cables $P = V \cdot I$. Not only does this reduce the power efficiency of the system, costing money, but also this power dissipation generates heat which needs to be removed, requiring massive cooling plants. For safety reasons, the voltage drop V on the cables is constrained to prevent possible over voltages on the modules. As a result the LV cable cross section can not be minimized and presents major contributions to the services material budget and

effectively fills the cable channels in the detector. In the current ATLAS pixel detector the total services dominate the total pixel material budget. The Type 0 services in particular account for approximately 0.13 %X_0 split between [24]

- LV cables: 0.10 %X_0,

- HV cables: 0.02 %X_0,

- data transmission: 0.01 %X_0.

The future ITk pixel detector with its larger size, more modules and readout channels as well as higher power consumption per module due to the increased granularity will only make this issue more pressing. A traditional approach as used in ATLAS pixel will simply not be possible anymore and a new, efficient powering scheme needs to be employed.

Serial Powering - A Novel Powering Scheme for the ITk Pixel Detector

In the current ATLAS pixel detector, a large contribution of the total material budget consists of detector services especially in the forward direction as shown in Section 1.2.1. Of these services, the power cables are the most significant contributor, as each detector module is powered by an independent set of cables. In order to minimize the material budget, the power cable diameter needs to be as small as possible. As a smaller diameter results in a larger cable resistance and thus increased power loss, the achievable cable dimensions are limited by the available cooling budget and acceptable detector power efficiency. During initial operation of the current ATLAS pixel detector, the power efficiency was expected to be as low as 25 %. For a total power consumption of 6 kW in the readout chips, a total of 24 kW had to be provided to the detector to account for the power losses in the services, totalling to 18 kW [6].

In the ITk pixel detector the per module current consumption per active area was expected to increase by a factor 2 to 4 with respect to IBL modules in order to meet the requirements set for a pixel detector in the HL-LHC environment, especially the increased granularity. Using the same cables as in the current ATLAS pixel detector the power efficiency would drop below 10 %. Since the new ITk pixel detector will be significantly larger as well, more cables are needed to service the detector, which results in more inactive material inside the detector volume. While the low power efficiency is already undesirable, the increased material inside the ITk would be unacceptable from a physics performance view. Ultimately, a different low-mass, high-efficiency powering scheme is required to service the future ITk pixel detector.

The two most promising candidates are DC-DC conversion and Serial Powering serial powering (SP) [27–29]. Both ATLAS ITk pixel as well as the future CMS pixel detector have decided to use SP as a baseline powering scheme. The core element of the used SP

schemes will be the Shunt-LDO regulator, a voltage regulator with shunt capabilities designed explicitly for use in a serially powered pixel detector.

As SP is a completely novel powering scheme for large scale pixel detectors, it requires a significant amount of prototyping to verify design choices for ITk. These efforts range from component prototyping, as for example the different iterations of the Shunt-LDO circuitry outlined in Chapter 4, to large scale prototyping like the Outer Barrel Demonstrator (OBD) in Chapter 5.1. Such large scale programs are invaluable, as they offer needed insights on system level aspects of SP, which may not be accessible during inital prototyping stages, like chip testing.

3.1 Serial Powering Concept

In an SP scheme, a number n of modules is powered in series by a constant current. Within a SP chain, the local ground of each module is the input potential of the following module. In the following the *first* module in a serial powering chain refers to the module with the highest local ground potential, while the *last* module in the serial chain has the lowest local ground potential, typically the same as the system ground. A sketch of a SP chain can be seen in Figure 3.1. Here, every module consists of four readout chips connected in parallel to provide redundancy in case of failure of a single chip. The required current I_0 for the SP chain is defined by the module with the largest current draw. Naively assuming a constant current draw for each module, the voltage drop V_m would remain unchanged compared to parallel powering. With the additional assumption of the

Figure 3.1: Simplified serial powering scheme consisting of quad-chip pixel modules.

same type of cable being used such that the power loss on each individual cable P_Cable is constant, the power dissipation for an SP chain of length n would be

$$P_{Module} = V_\mathrm{m} \cdot I_0,$$
$$P_{Cable} = R_\mathrm{Cable} \cdot I_0^2,$$
$$P_{Chain} = n \cdot P_\mathrm{Module} + P_\mathrm{Cable},$$
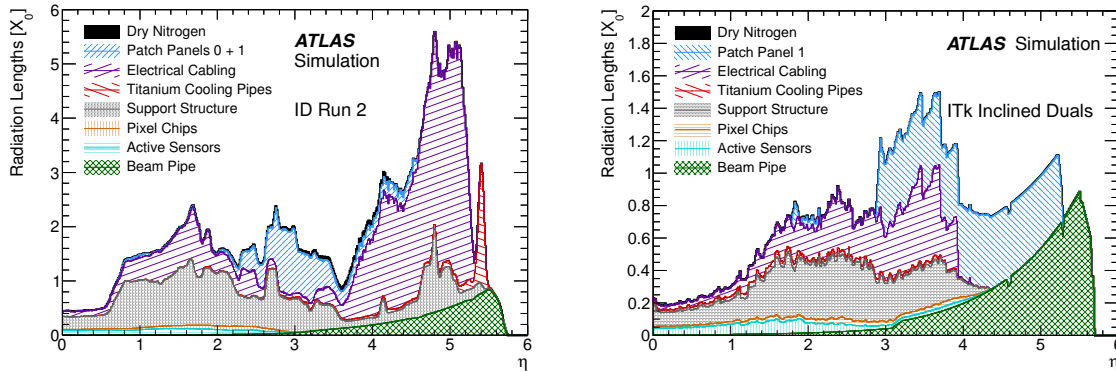
(a) Radiation length X_0 versus the pseudorapidity η for the current ATLAS ID pixel detector [30].

(b) Radiation length X_0 versus the pseudorapidity η for the ITk pixel detector [16].

Figure 3.2: Simulated material budget of the current ATLAS pixel detector during Run 2 (a) and the ITk (b). Contributions from different components are shown. The figures only show positive η; negative η is expected to look the same. The serially powered ITk pixel detector shows a significantly lower material budget, especially in the forward region.

compared to a parallel powering scheme consisting of n modules

$$P_{\text{Parallel}} = n \cdot (P_{\text{Module}} + P_{\text{Cable}}).$$

A comparison of such key figures in serial and parallel powering schemes can also be seen in Table 3.1. It can be seen that, depending on the contribution of the detector services to the total power budget, an SP scheme can offer a significant increase in power efficiency. At the same time SP can bring a significant reduction in the material budget used in the detector. Figure 3.2 shows a comparison of the simulated material budget of the current pixel detector during Run 2 data taking and the future ITk, as proposed in [30]. The overall material budget of serially powered ITk is significantly smaller, especially in the forward region, where the cables leave the detector alongside the beam pipe. Using a conventional parallel powering scheme, the material budget especially in the forward direction would be unacceptable. Additionally the required cables would not fit in the volume available for services in ITk pixel.

The approach does not consider the fact that a pixel readout chip actually behaves more akin to a variable ohmic load instead of a resistor. For a SP scheme to operate reliably the pixel modules need to display the electric characteristic of an ohmic resistor instead. In order to address this, the supply voltage for each readout chip is generated by dedicated voltage regulators on the module. As the powering scheme is based on a constant current supply which needs to cover the maximum possible current draw, there is always an excess current

Parallel and serial powering of n modules					
Scheme	Total module current	PSU voltage	Cable cross section	Power loss	Powering efficiency
Parallel	$n \cdot I$	V_{Mod}	A	$R \cdot I^2$	$\frac{V \cdot I}{V_{\mathrm{Mod}} \cdot I + R \cdot I^2}$
Serial	I	$n \cdot V_{\mathrm{Mod}}$	A/n	$R \cdot I^2/n$	$\frac{V \cdot I}{V_{\mathrm{Mod}} \cdot I + R \cdot I^2/n}$

Table 3.1: Key figures of parallel and serial powering schemes with n modules being powered. Compared are the total current input in the system I, the power supply (PSU) terminal voltage V, the voltage drop over a pixel module V_{Mod}, the cable cross section A, which is inversely proportional to the cable resistance R, needed to service the modules, power losses on the cables and the powering efficiency. In an SP scheme, the reduced power losses on cables lead to a significant improvement in power efficiency.

that needs to be shunted. A constant current supply is used opposed to a constant voltage supply, as it is inherently more resistant to load transients: with a high output inductance, a constant current supply has a high transient impedance. Thus in the case of fast load changes, e.g. if a chip in the serial chain fails, the output current of the power supply remains very stable [31]. Both objectives are covered by the Shunt-LDO, see also Section 3.2, a voltage regulator specifically designed for serially powered pixel detectors. Although the inherent current draw of these regulators is almost negligible, they increase the average power consumption of the pixel modules. This is caused by an additional voltage drop in the Shunt-LDO, the dropout voltage V_{do}. For a typical Shunt-LDO as will be discussed in this work, V_{do} is typically in the order of 300 mV. As can be seen from Figure 3.6 and Equation 3.13, this additional voltage drop reduces the power efficiency of a single regulator by $O(20\,\%)$ on its own. This provides a non negligible challenge for the design of the local supports of the ITk pixel detector, as the power dissipation of the pixel modules is increased significantly and requires a more potent cooling system. Ultimately the saved material budget in an SP scheme and the significantly reduced total power consumption of the system more than compensate for this added inefficiency.

However the serial connection of pixel modules brings additional risks and challenges at the system level, which are not present in parallel powering.

Within each SP chain, all modules are on different local ground potentials, which makes AC-coupling of all data links mandatory, see Section 3.1.1. The varying ground potentials in a SP chain also need to be considered for the HV distribution, see Section 3.1.2, scheme. With the HV leakage current I_{leak} being returned via the LV line, the HV must be distributed in a way that does not short the serial powering chain.

Noise can propagate on the power lines, adversely affecting the full serial chain unless

filtered properly, e.g. within the Shunt-LDO. Should a module in an SP chain fail high ohmic, thus interrupting the chain, the full chain would be put out of operation. Such a failure may be the result from a malfunction on the ROC or on the services. Similarly, no individual module can be switched on or off. Some of these risks can be mitigated by redundancy on the module level. Should the readout chip fail electrically open, the chain current can be shunted by the Shunt-LDO. Each readout chip is equipped with two separate Shunt-LDO regulators connected in parallel. This allows fine tuning of the Shunt-LDO to the current consumption of the analog and digital domains of the ROC, which generally require different supply currents. In principle using two Shunt-LDO per ROC also allows e.g. the digital domain to be operated at a lower core voltage than the analog domain, as is the case in the FE-I4, and provides some redundancy against failure of a single Shunt-LDO. In addition the majority of ITk Pixel module will consist of 4 ROC connected in parallel, such that 8 parallel Shunt-LDO distribute the chain current on module level. If a Shunt-LDO fails on such a module, the remaining Shunt-LDO can take over the additional current, keeping the serial chain operational. This capability comes at the cost of an increased power dissipation in such a faulty module. If too many regulators fail on a single module, the full chain needs to be switched off. Thus the average number n of modules in a serial powering chain is a trade-off between reliability of the detector system and the efficiency of longer serial chains. In a real detector like ITk pixel the feasible length of a serial powering chain is additionally constrained by the layout of the local supports and monitoring systems. In the ITk pixel detector there will be 912 serial powering chains between 3 and 14 modules in length with an average length of 9 modules.

Another set of risks to be addressed are potential overvoltages in a serial chain. These can for example occur if a module fails low ohmic and the PSU can not regulate its output voltage fast enough. If the resulting transients are too large, meaning they exceed the voltage capabilities of the Shunt-LDO or ROC, they can destroy some of the remaining modules in the chain. These can be mitigated, for example, by an active element like the Pixel Serial Powering Protection (PSPP) or a passive, fast voltage clamp to provide overvoltage protection. A different valid approach would be to target the causes and prevent over voltages from occurring in the first place, as it is done in the latest generation of Shunt-LDO, see also Section 4.3.

3.1.1 AC-Coupling of Data Signals

In a serial powering chain, all modules have their own local ground potential LV_{out}. Only the last module in a chain shares the same ground as the serial powering chain itself, which is also used for the PSU and the readout system. The ROC receives its clock (CLK) and command (CMD) signals from the DAQ, while sending output data to the DAQ. This communication
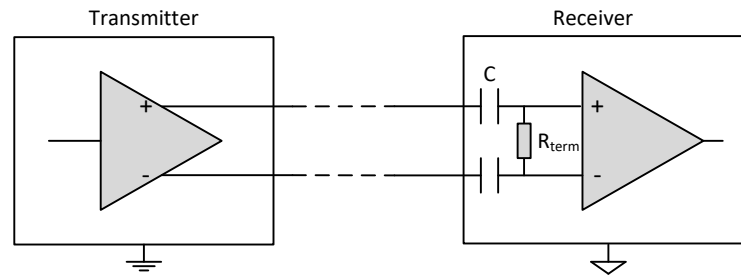
Figure 3.3: Simplified schematic of AC-coupled low voltage differential signaling (LVDS) data links. Capacitors are placed in series on both lines of the differential pair prior to the termination resistor. These filter any DC component in the LVDS signal, which is necessary, as transmitter and receiver in a serially powered detector usually have different ground potentials [24].

usually is done via LVDS links to cope with longer signal paths and mitigate pickup of unwanted noise, e.g. crosstalk between separate links. Similar to single ended signalling, each LVDS link is referenced to the local transmitters ground potential. This DC potential of the LVDS lines is called the common mode voltage V_{cm}. The common mode voltage includes ground shifts between transmitter and receiver and is typically in the order of a few V [32]. Due to the serial connection of modules, V_{cm} will increase for modules more upstream in the chain as the local module ground potential increases with respect to the system ground. Once V_{cm} shifts out of the operational range of the receiver, link integrity is not anymore guaranteed. For long serial chains with large voltage drops over the full chain V_{cm} quickly grows large enough to damage receiver inputs.

This issue can be solved using AC-coupled data links. In an AC-coupled termination scheme, as shown in Figure 3.3, capacitors are connected in series with the LVDS transmission lines. These block all DC components in the LVDS link. The V_{cm} is then not anymore set by the transmitter, but by the receiver, which needs self biased receiver inputs. In this scheme, current can only flow through the capacitors and the termination resistor R_{term} during signal transitions. If these transitions are not frequent enough, charge can not flow through the coupling capacitors. The charge on the two receiver terminals will then slowly decay towards the same value, which reduces noise margin of the LVDS link [32]. To ensure frequent transitions, a DC-balanced signal needs to be used when using AC-coupling. DC-balance here refers to the number of ones and zeros, or HI and LO signal levels, which has to be 0 over the full data set, as is the case e.g. in a CLK signal. For CMD and data, DC-balance is achieved by use of an appropriate encoding, e.g. the 8B/10B encoding used for the FE-I4.

The capacitors used in AC-coupling need to be dimensioned properly to avoid unwanted filtering of data. Here the run length (RL), the number of consecutive equal bits is important, as the maximum RL defines the lowest effective frequency component in the LVDS data
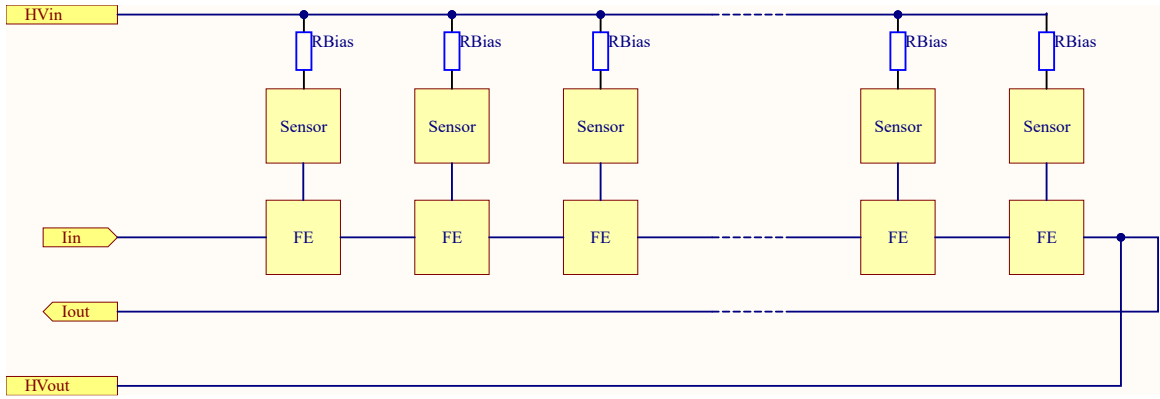
Figure 3.4: Schematic of a common HV supply for a full serial powering chain. All modules are connected in parallel to the HV supply line. The HV return is returned via the LV return line.

stream. The attenuation of the data stream can be kept below 0.25 dB, if the capacitor is chosen according to

$$C = \frac{7.8 \cdot RL \cdot T}{R_{\text{term}}}, \tag{3.1}$$

with the bit period T and the termination resistor R_{term} [32]. Typical capacitor sizes for high speed applications are 0.1 μF and 0.01 μF.

3.1.2 High Voltage Distribution

The HV return line of pixel detector modules as they can be found in the current ATLAS ID or in ITk is connected to the local module ground, the HV distribution scheme must be chosen in a way that does not short the serial powering chain. The straightforward solution, connecting each module to its own HV PSU, is not feasible in a detector as large as ITk and violates the grounding and shielding requirements. Another option is connecting a full serial chain to one HV PSU. A schematic implementation is shown in Figure 3.4. In such a scheme, all modules in a serial powering chain are connected in parallel to the same HV input. The HV return is realised via the LV return of the serial chain. Consequently, the HV is referenced to the chain ground, while the n-th module upstream has a local ground potential $n \cdot V_{\text{Mod}}$ larger than the reference potential. The bias voltage seen by this n-th module is thus

$$HV_n = HV_{\text{supply}} + (n - 1)V_{\text{mod}}. \tag{3.2}$$

Considering a serial powering chain 8 modules long and $V_{\text{mod}} = 1.5$ V, similar to the setup described in Chapter 5.2, this voltage difference ΔHV between the sensor reverse bias voltage seen by the first and last module in the serial chain is 12 V. Such a difference in the bias

voltage becomes an issue, if the breakdown voltage V_{bd} of the sensors used is small compared to HV_{supply}, such that $n \cdot V_{mod} \approx V_{bd} - HV_{supply}$. For planar sensors as will be used in most of ITk this is not a concern, as $V_{bd} - HV_{supply}$ is typically an order of magnitude larger than $n \cdot V_{mod}$. After the sensor has been irradiated, breakdown is even less of a concern. For 3D sensors however, which will be used in the innermost layer of ITk, this can quickly become a problem, as breakdown occurs much earlier. Depending on the chain length in the innermost layer, it would be necessary to utilize more than one HV group per SP chain. Furthermore, at the end of life of the detector, the leakage current of the irradiated sensors will increase to the order of 2 mA. For a chain of 14 modules this would result in a total leakage current in the order of 30 mA, which is very challenging for typical off the shelve HV PSU and provides a risk for the long-term availability of the detector. Thus in addition to the system reliability aspects, using multiple HV groups in a serial chain is also a more cost efficient approach. In ITk pixel this is achieved in two different ways, depending on the subsystem: in the innermost layer of the ITk IS, each module is connected to a dedicated HV supply and return line, with the HV return line being floating. In the other layers two HV groups are implemented per serial chain. Each of these groups is connected to a dedicated HV supply line and referenced to the system ground. Additional HV groups also contribute to system reliability. If a failure in a serial chain would cause thermal runaway in one module, the corresponding HV group will be switched off. If there are two or more of these groups per serial chain, less modules will be put out of operation - provided the SP chain itself can still be operated.

Grouping the HV supplies together within a SP chain can have further unintended implications with respect to the interplay between PSU. It is common during beginning of data taking in an experiment like ATLAS for the pixel modules to be powered, but the HV being switched off until stable beam conditions are achieved. With the HV input of each module in this situation pulled to system ground, the differing local grounds in the SP chain cause a small bias voltage occuring for all but the last modules in a HV group within the SP chain. The behaviour of the leakage current caused by this small bias depends on the properties of the HV PSU. If the PSU has a low ohmic off mode, the leakage current can return through the PSU and nothing of note happens to the last module in the group. For a high impedance PSU off mode however, when comparing to the series connection of sensor and bias resistor, a more attractive current path for the leakage current is the last module of the HV group. The leakage current will then be returned through the sensor of the last module in forward direction, which is unintended behaviour. Depending on the amount of leakage current, more than one module will experience this forward bias. This is due to the HV line floating to higher potentials if larger leakage currents flow in the chain. If then the voltage drop over a single bias resistor, returning the collected leakage current, exceeds the potential difference between the HV line and local ground potential, some of the leakage current has to be returned through the $(n-1)$th module in the HV group. This phenomenon became

prominently known in the context of the OBD and initiated further studies investigating if this behaviour is potentially harmful to the detector, see for example [33] and Section 5.3.5. The mitigation strategy would be specifying the off mode of the HV PSU to be low ohmic. Since typical commercially available HV PSU utilize high ohmic off modes, this additional requirement would come at a potentially significant financial cost.

3.2 Voltage Regulation with the Shunt-LDO Regulator

As mentioned in Section 3.1, the conversion of constant chain supply current to local ROC supply voltage in the serial powering scheme intended for the ITk pixel detector will be done using the Shunt-LDO [34] regulator. The Shunt-LDO is at its core a combination of a low dropout voltage regulator (LDO) and a shunt regulator which was first introduced in the FE-I4. In Figure 3.5 the simplified schematics of a Shunt-LDO can be seen. The LDO consists here of the PMOS transistor M_1, the error amplifier A_1 and the resistive divider formed by R_1 and R_2. In all implementations of the Shunt-LDO discussed in the context of this thesis R_1 and R_2 are of equal size. The output voltage of A_1 will be steered such that the fractional voltage drop over R_2 is equal to V_{ref}, such that for $R_1 = R_2$

$$V_{out} = 2 \cdot V_{ref}. \tag{3.3}$$

The desired output voltage V_{out} is then generated with respect to the local ground potential I_{out}. The load, in this case the ROC, draws its required supply current from the available I_{in} via the V_{out} terminal.

The transistor M_4 offers an additional current path parallel to the load and provides the shunt capabilities to the Shunt-LDO. In order to steer this transistor, additional circuitry to sense the current flowing through the regulator is needed. To this end a fraction of the current flowing through the Shunt-LDO, defined by the current mirror formed by M_1 and M_2, is drained into the gate-drain connected transistor M_5. The amplifier A_2 and transistor M_3 are added to improve on the accuracy of the current mirror. This mirrored current is compared to a reference current I_{ctrl} flowing through resistor R_{shunt} and the gate-drain connected transistor M_6, which is defined by the input potential V_{in}, by the amplifier A_3. This reference current can be approximated as

$$I_{ctrl} \approx \frac{V_{in} - V_{M6}}{R_{shunt}}, \tag{3.4}$$

where V_{M6} denotes the threshold voltage of transistor M_6. If the current flowing through M_5, being a fraction of the current flowing through M_1, is not equal to I_{ctrl}, A_3 steers M_4 to draw more or less current, until the current fraction through M_5 equals the reference current I_{ctrl}.
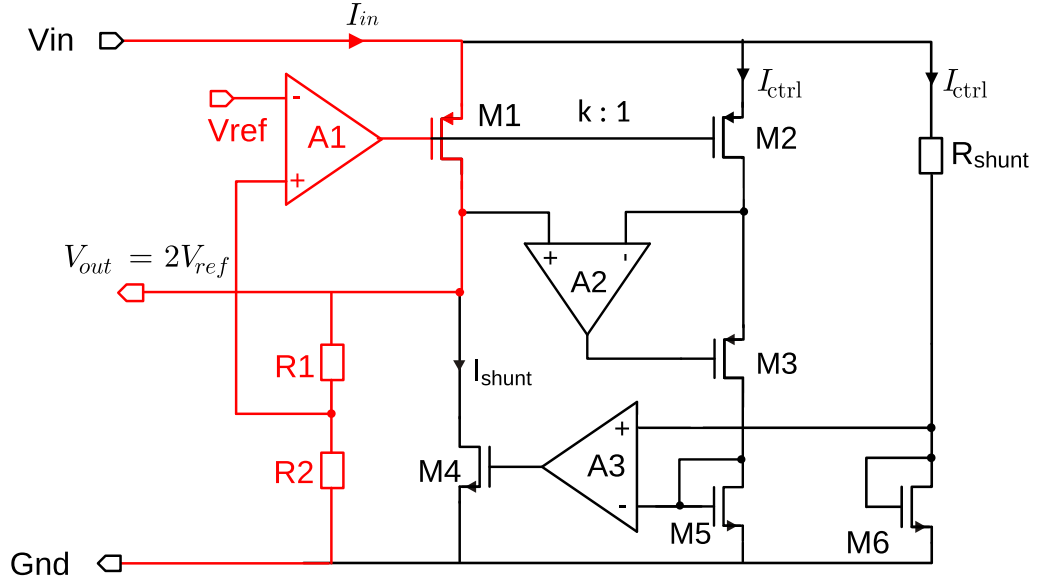
Figure 3.5: Simplified schematic of the Shunt-LDO as implemented in the FE-I4 ROC [35]. The regulator is supplied with I_{in}, the ROC power rails are connected to V_{out}. Gnd corresponds to the local ground potential. The LDO is marked red, the shunt regulator in black.

As a result, the current difference

$$I_{shunt} = I_{in} - I_{load} \tag{3.5}$$

is shunted through M_4 and a constant current flows through M_1. This constant current's value can be approximated using Equation 3.4 as

$$I_{in} \approx (k + 2) I_{ctrl} = (k + 2) \frac{V_{in} - V_{M6}}{R_{shunt}} \tag{3.6}$$

with the current mirror ratio k. Rearranging for V_{in} then yields

$$V_{in} \approx R_{shunt} I_{ctrl} + V_{M6} = \frac{R_{shunt}}{k + 2} I_{in} + V_{M6}. \tag{3.7}$$

This mode of operation with a constant current flowing through M_1 is referred to as Shunt-LDO mode, or shunt mode for short. The Shunt-LDO offers the possibility for the current regulation loop to be switched off, leaving only the LDO part of the regulator active, turning the Shunt-LDO into an LDO.

From Equation 3.6 and Equation 3.7 it can be recognized that the Shunt-LDO behaves

like an ohmic resistor in series with a voltage offset V_{M6}. More specifically, neglecting the threshold voltage V_{M6}, the effective input resistance of the Shunt-LDO is given as

$$R_{in} \approx \frac{V_{in}}{I_{in}} = \frac{R_{shunt}}{k}. \tag{3.8}$$

As a consequence, if several Shunt-LDOs with the same R_{in} and V_{M6} are connected in parallel, they each receive an equal share of the input current I_{in}, allowing stable parallel operation of multiple regulators on a single front-end (FE) or detector module. As the output voltage V_{out} has no influence on the input characteristics of the Shunt-LDO, these parallel regulators can also operate with different target output voltages. In the FE-I4 the two Shunt-LDOs are operated with output voltages of 1.5 V and 1.2 V respectively without issues.

The ability of a voltage regulator or power supply to keep its output voltage V_{out} constant over a range of input voltages V_{in} or load currents I_{load} is referred to as the *line regulation* and *load regulation* of the device. The line regulation is typically defined as:

$$Line\ Regulation = \frac{\Delta V_{out}}{\Delta V_{in}} \cdot 100\,\%, \tag{3.9}$$

and is measured for a constant load current. A low line regulation is usually preferred. For commercially available power supplies and LDOs, the typical line regulation is in the order of 0.1 %. Since the Shunt-LDO operates based on a constant current supply instead of a constant voltage supply, the line regulation is instead referred to as

$$Line\ Regulation = \frac{\Delta V_{out}}{\Delta I_{in}} \cdot 100\,\%\,\mathrm{V\,A^{-1}}. \tag{3.10}$$

The load regulation is similarly defined as

$$Load\ Regulation = \frac{\Delta V_{out}}{\Delta I_{load}}, \tag{3.11}$$

for a constant V_{in} and given in units of Ω. Sometimes the load regulation is also referred to as output impedance. Similar to the line regulation, a low load regulation is usually desired.

The inherent robustness of the Shunt-LDO comes at the price of power efficiencies. For all implementations of the Shunt-LDO discussed in this thesis, the design value for the current mirror ratio k is 1000 : 1, thus the losses in the reference current path are negligible. Whenever current is shunted, the Shunt-LDO burns extra power $P_{shunt} = I_{shunt} \cdot V_{out}$ compared to the stand-alone ROC. An additional source of inefficiency is the transistor M_1, where even more power $P_{do} = V_{do} \cdot I_{in}$ is dissipated, with the dropout voltage of the Shunt-LDO V_{do}
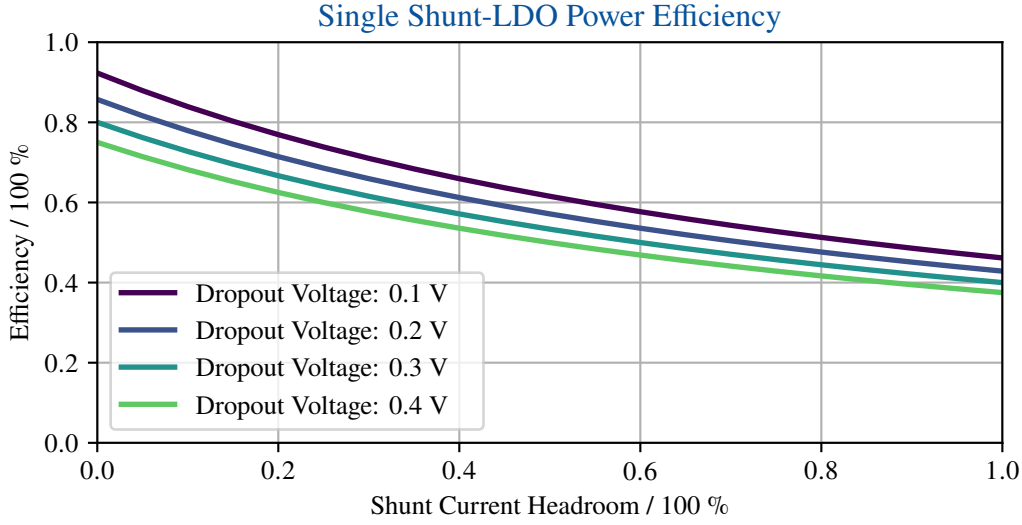
Figure 3.6: Efficiency of a single Shunt-LDO for different values of V_{do} and different shunt headrooms. The headroom is given as $\frac{I_{\text{shunt}}}{I_{\text{load}}}$, the regulator output voltage is $V_{\text{out}} = 1.2\,\text{V}$.

being defined as

$$V_{\text{do}} = V_{\text{in}} - V_{\text{out}}. \tag{3.12}$$

The total power efficiency of the Shunt-LDO is then given as

$$\eta = \frac{1}{\left(1 + \frac{V_{\text{do}}}{V_{\text{out}}}\right)\left(1 + \frac{I_{\text{shunt}}}{I_{\text{load}}}\right)} \tag{3.13}$$

and plotted in Figure 3.6 as a function of the current headroom $\frac{I_{\text{shunt}}}{I_{\text{load}}}$ for different V_{do}. As can be seen a low V_{do} and more importantly a low current headroom are desired to maximize power efficiency of the Shunt-LDO. The dropout voltage is mostly driven by M_1, thus M_1 is the only transistor not cascoded in the circuitry in Figure 3.5. The shunt current headroom is driven by the parallel operation of several Shunt-LDO on a module. Here, process variations in the Shunt-LDO and services like the module flex PCB will cause different R_{in}, and thus current consumption, for each regulator, while the threshold voltage V_{M6}, effectively an offset in Equation 3.7, may vary between Shunt-LDO due to process variations and especially radiation damage. This results in an uneven current sharing, which needs to be compensated by providing extra current headroom to the serial chain, such that the regulator with the largest effective R_{in} still receives enough current to cover the needs of the FE. Such an extra headroom adds to the power losses in M_1 and M_4 on a module level. As a mitigation strategy for current imbalances caused by differing V_{M6}, a controllable offset voltage V_{ofs} can be
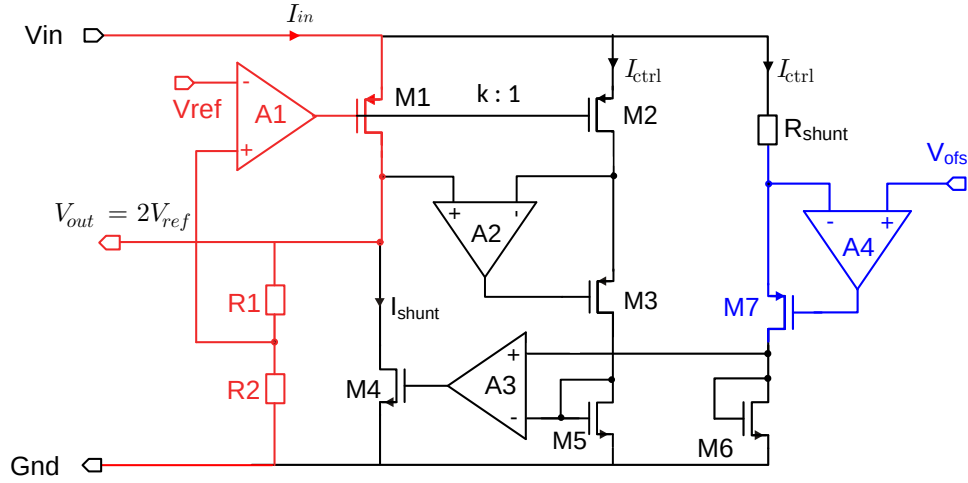
Figure 3.7: The Shunt-LDO with an additional offset generating circuit in the reference current path. The LDO is marked red, the shunt regulator black and the offset generating circuit in blue. Adapted from [35].

introduced into the Shunt-LDO reference path as shown in Figure 3.7. On a single ROC V_{ofs} can be shared between the two parallel Shunt-LDO, minimizing the mismatch between the offset voltages and improving the current sharing. Similarly on a multi-chip module the offset voltage can be shared between the different ROC. The amplifier A_4 applies V_{ofs} to the lower terminal of R_{shunt}, while the upper terminal of R_{shunt} remains tied to V_{in} as before. As soon as $V_{\text{in}} > V_{\text{ofs}}$ the reference current I_{ctrl} starts flowing through R_{shunt} and is drained into M_6. Equation 3.7 now becomes

$$V_{\text{in}} \approx \frac{R_{\text{shunt}}}{k+2} I_{\text{in}} + V_{\text{ofs}}. \tag{3.14}$$

This scheme offers several potential advantages: V_{ofs} can be chosen larger than V_{M6}, which allows smaller values for the slope resistor R_{shunt}, allowing more efficient operation at currents larger than the target I_{in} as the total power burned is

$$P_{\text{tot}} = I_{\text{in}}^2 R_{\text{eff}} + I_{\text{in}} V_{\text{ofs}}, \tag{3.15}$$

as can be seen in Figure 3.8. This is important when considering modules with multiple parallel Shunt-LDO, which will have an imperfect current sharing between the regulators. The benefits of a smaller R_{shunt} become especially clear once on such a module one or more Shunt-LDO become faulty and are not available anymore. Since now the remaining regulators
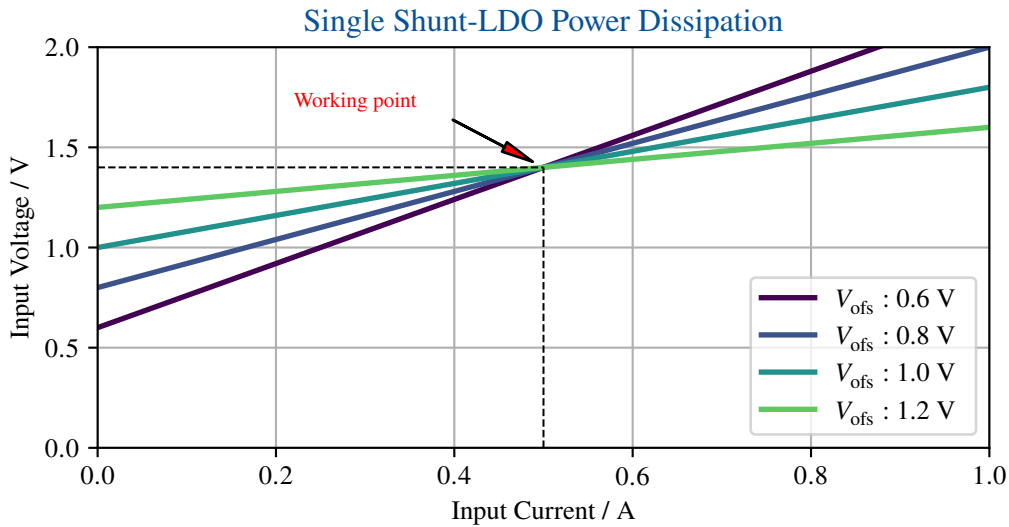
Figure 3.8: Different configurations of V_{ofs} and R_{eff} to reach a target working point I_{in} = 0.5 A, V_{in} = 1.4 V. For larger V_{ofs} and smaller R_{eff}, the Shunt-LDO is more efficient for higher I_{in}.

would have to shunt significant excess currents, a small slope resistor allows acceptable operating points V_{in} for more failing regulators compared to the initial regulator design. This makes the SP chain more reliable, as a larger number of single point failures on a module is required to cause failure of the chain. On the other hand a small R_{shunt} amplifies the effects of a mismatch in V_{ofs} on the current balancing of a system with multiple parallel Shunt-LDOs, as more current is needed to equalize V_{in} for the different regulators. Since V_{ofs} is not provided from the Shunt-LDO itself but externally, the different V_{ofs} of parallel Shunt-LDO on a module can be tied together. This significantly reduces any variation in the offset component in Equation 3.14, improving the input impedance matching of parallel regulators and thus the current balancing, being beneficial for power efficiency.

The Shunt-LDO for a new Generation of Pixel Readout Chips with Serial Powering Capability

The RD53 Collaboration was formed between ATLAS and CMS in 2013 in order to develop a new generation of pixel ROC for the future ATLAS and CMS detectors in the HL-LHC. This new ASIC was chosen to be manufactured in a 65 nm CMOS process. The main factor behind this choice is the required tolerance to the unprecedented radiation levels in HL-LHC, for which the 65 nm node has shown promising results. Furthermore this node meets more specific requirements, such as a sufficient logic density, low power consumption and long term commercial availability [36].

The main goals of the RD53 collaboration were qualification of the chosen technology node, especially in terms of radiation hardness, as well as development of the necessary foundations needed to design a ROC for future ATLAS and CMS pixel detectors. This extends to the development and evaluation of the building blocks needed for these later production ASICs, such as the Shunt-LDO. Designs like the Shunt-LDO, a design tested and proven in the 130 nm node used for the FE-I4, required translation and re-qualification in the new node. For this purpose, a series of prototype chips have been developed and within the context of this thesis extensively characterized. An overview of the results of these efforts can be found in Section 4.1.

The development within RD53, which included a number of smaller demonstrator chips like the FE65-P2 [37] and Chipix [38], culminated after many years in the RD53A [39], a large scale ASIC fabricated in a 65 nm CMOS technology. The RD53A ASIC was intended as a technology demonstrator and as such includes two different digital buffer architectures as well as three different AFE designs, referred to as the SYNC, LIN and DIFF AFE. At the

same time many key features of a later production chip were already available in RD53A, such as the reduced pixel pitch, serial powering capabilities and high speed data links. Up to this day, the RD53A is widely used in prototyping and pre-production campaigns, including but not limited to hybridisation market surveys and large scale serial powering system tests as for example in Section 5.2. In Section 4.2 the Shunt-LDO used in RD53A is discussed.

Following the reception and characterisation of the RD53A, a decision on the actual AFE architecture to be used had to be made by both ATLAS and CMS. In early 2019, the ATLAS collaboration decided to move forward using the so-called Differential AFE [40], while CMS decided to use the so-called Linear AFE. By request of both ATLAS and CMS, the RD53 collaboration was extended in this context, now also covering the design and fabrication of the final production chips for both experiments, the ITk Pixel ROC (ITkPix) and CMS ROC (CROC) [41]. While ITkPix and CROC use substantially different AFEs and will differ in physical size, both chips will share the same fundamental design library, referred to as RD53B [42]. This library contains the digital core design, sensing and monitoring as well as power management, including the Shunt-LDO.

The experiences made with RD53A as well as in system test campaigns with the FE-I4 in the OBD program raised new requirements for the Shunt-LDO in RD53B. The new Shunt-LDO for RD53B is not only a significant improvement over the design in RD53A, but also includes a variety of new features requested by the experiments. The key specifications of the RD53B Shunt-LDO, the operational range, line- and load regulation, are listed in Table 4.1. In order to verify these design improvements and new features, an additional series of Shunt-LDO prototype chips became necessary. The new Shunt-LDO design, as well as the characterisation and verification of these new prototypes conducted in the context of this work are covered in Section 4.3.

4.1 Prototyping and Characterization of a Shunt-LDO in a 65 nm Node for the RD53A Readout Chip

The adaptation of the existing Shunt-LDO design for the new 65 nm node was conducted in three steps. At first the existing design used in the FE-I4 was translated to the new node, without adding any additional features. The resulting prototype chip did not include any on-chip bandgap reference circuit, meaning V_{ref} had to be provided externally, and was rated to the same shunt current as the FE-I4 Shunt-LDO, 500 mA. After verifying the basic functionality of the prototype, the radiation hardness of the design was tested in an X-ray irradiation campaign. This prototype was followed by a second iteration. Not only was this new regulator rated for a shunt current of up to 2 A, but it also included a bandgap reference circuit to provide reference voltages on-chip as well as a series offset in the current reference

Technical Specifications of the Shunt-LDO	
Input Voltage (LDO)	$1.4\,\text{V} \leq V_{\text{in}} \leq 2\,\text{V}$
Input Current (Shunt-LDO)	$I_{\text{in}} \leq 2\,\text{A}$
Load Current I_{load}	$I_{\text{load}} \leq 1\,\text{A}$
Output Voltage	$0.7\,\text{V} \leq V_{\text{out}} \leq 1.32\,\text{V}$
Dropout Voltage	$0.2\,\text{V}$
Line Regulation	$\leq 10\,\text{mV}/I_{\text{in}}$
Load Regulation	$\leq 10\,\text{mV}/I_{\text{load}}$
Load Transient Response	$\pm 30\,\text{mV}$

Table 4.1: Specifications of the Shunt-LDO for the final production chips ITkPix and CROC [43]. The Specifications for line- and load regulation are referenced to the full range I_{in} and I_{load}.

path as shown in Figure 3.7, which serves to shift the Shunt-LDO working point and allows using smaller slope resistors, as mentioned in Section 3.2.

Based on the experiences made with the first two prototypes in the new technology node, the Shunt-LDO was implemented on the RD53A. In RD53A, the 65 nm Shunt-LDO was first connected to a realistic and representative load with respect to application in the future ATLAS and CMS detectors, which offered a new perspective for characterisation. As shown in Section 4.2.1, the Shunt-LDO in RD53A showed generally promising performance, but came with a few caveats, especially related to the on-chip bandgap reference circuit, which had to be addressed for the future production chips. Despite these shortcomings, RD53A with its Shunt-LDO has been succesfully used in a first serial powering prototype using new-generation ROCs and Shunt-LDOs, treated in depth in Section 5.2, and will be used in the upcoming large-scale system tests outlined in Section 5.1.3.

4.1.1 500 mA prototype

As mentioned the first adaptation of the Shunt-LDO in the new 65 nm node was in essence a copy of the design used in FE-I4. Similar to FE-I4, this Shunt-LDO was designed for a maximum shunt current of 500 mA. A bandgap reference circuit was not included in this first prototype, such that the reference voltage V_{ref} could not be generated on-chip and needed to be provided externally instead. The silicon, mounted on a test PCB[1], can be seen in Figure 4.1. This prototype chip includes three parallel Shunt-LDO regulators on the same die, sharing

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[1] Designed by M Karagounis, M Krause, FH Dortmund

common wirebonding pads for I_{in} and ground reference. For each of the three Shunt-LDO the reference voltage $V_{\text{ref,i}}$ is derived from a common supply voltage V_{CC} using variable resistors. The slope-defining resistor in the reference circuit, R_{shunt} in Figure 3.5, can be chosen to be either a $2\,\text{k}\Omega$ resistor inside the silicon, an surface-mounted device (SMD) resistor on the PCB or a parallel connection of both for each of the three Shunt-LDO. In the measurements presented here the internal resistor was used. Dedicated connectors allow direct access of $V_{\text{out,i}}$ of all regulators and can be used to connect external loads. Parallel to this path power transistors are placed, which can be steered to simulate load transients. Sensing lines are provided for measurement of $V_{\text{out,i}}$ in order to compensate for the voltage drop on wirebonds and PCB traces caused by $I_{\text{load,i}}$.

It should be noted that all voltages on this PCB are referenced to the PCB ground, not the Shunt-LDO ground, as the internal Shunt-LDO ground is not accessible. The current flowing from Shunt-LDO ground to PCB ground through the wirebonds connecting both planes can cause a significant shift in the Shunt-LDO's ground potential with respect to the main reference. This shift is directly proportional to I_{in} and decreases with I_{load}, as this current is returned directly to the PCB ground. Since V_{ref} is generated with respect to the Shunt-LDO ground, it will thus always include a small shift δV_{GND} given as

$$\delta V_{\text{GND}} = R_{\text{wb}} \cdot I_{\text{in}} \qquad (4.1)$$

Figure 4.1: Test PCB with the $500\,\text{mA}$ Shunt-LDO prototype chip. Each chip included 3 individual instances of the same Shunt-LDO design connected in parallel. The PCB allows configuration of the Shunt-LDO operation mode, monitoring of input- and output currents and voltages and studying of transient response.

with R_{wb} denoting the combined resistance of wire bonds and copper traces on the PCB. For a typical aluminium wirebond with a diameter of $25\,\mu\text{m}$ and a length of $5\,\text{mm}$ the ohmic resistance would be in the order of $0.3\,\Omega$. In case of the chip discussed here the ground connection is achieved using 15 wirebonds. For an input current $I_{\text{in}} = 500\,\text{mA}$, the resulting shift would be $\mathcal{O}(10\,\text{mV})$. The shift on V_{out} is expected to be twice the shift on V_{ref}. Key figures obtained from measurements with this prototype chip can be found in Table 4.2.

The input I-V characteristic of this Shunt-LDO is shown in Figure 4.2. It is obtained by ramping up the input current, which can be provided by a current source or a voltage source

Line- and load regulation results of the 500 mA Shunt-LDO prototype chip.	
R_{eff}	$2.1\,\Omega$
V_{ofs}	$0.38\,\mathrm{V}$
$\dfrac{V_{\mathrm{out}}}{V_{\mathrm{ref}}}$	1.99 ± 0.01
Line Regulation	$0.027\,\mathrm{V\,A}^{-1}$
Load Regulation	$< 0.015\,\Omega$
Load Transient Response	$130\,\mathrm{mV}$

Table 4.2: Overview of results from the 500 mA Shunt-LDO test chip.

operated in its current limit, and recording V_{in} and V_{out} at every step. For this measurement, no load is drawn from the Shunt-LDO. The expected linear characteristics can be seen once the input current I_{in} is large enough to saturate the Shunt-LDO. V_{ref} is chosen as 600 mV to provide an output voltage V_{out} of 1.2 V. The regulator is designed to have a minimum dropout voltage V_{do} of 200 mV, the lowest design working point is thus at a V_{in} of 1.4 V. For further evaluation, only working points with $V_{\mathrm{do}} \geq 200\,\mathrm{mV}$ are considered.

To determine the effective input resistance of the Shunt-LDO, a line fit on V_{in} in the region of interest $1.4\,\mathrm{V} \leq V_{\mathrm{in}} \leq 2\,\mathrm{V}$ is used, 2 V being the highest voltage to be safely applied to the circuitry. From Equation 3.8, an input resistance of $2\,\Omega$ would be expected given the value of R_{shunt}. As can be seen from Table 4.2 the measured R_{eff} slightly disagrees with the expectation. The line regulation of the Shunt-LDO can be determined from this measurement using Equation 3.10 and is listed in Table 4.2 for the region of interest, or 1.3 % when referenced to V_{in}, which is large compared to commercial voltage sources. For the full region of interest however this only corresponds to an acceptable difference ΔV_{out} of $\leq 6\,\mathrm{mV}$. Figure 4.3 shows the output voltage steering precision, that being the ratio of V_{out} and V_{ref}, for different values of V_{ref} both in Shunt-LDO mode as well as LDO mode. From Equation 3.3 it is expected that

$$V_{\mathrm{out}} = \lambda V_{\mathrm{ref}}, \tag{4.2}$$

with $\lambda \approx 2$. This is well satisfied in both Shunt-LDO mode and LDO mode, however an offset $\Delta\lambda$ can be seen between both cases. This offset is caused by the shift δV_{GND} discussed before. With no load applied in this measurement, the current flowing through the regulator in LDO mode is negligible, while in Shunt-LDO mode a current of 500 mA is flowing through the regulator. Based on the approximation given above, the observed difference of $\approx 15\,\mathrm{mV}$ is in agreement with the expectation.

Figure 4.4 shows the load regulation behaviour of the Shunt-LDO. In order to obtain this
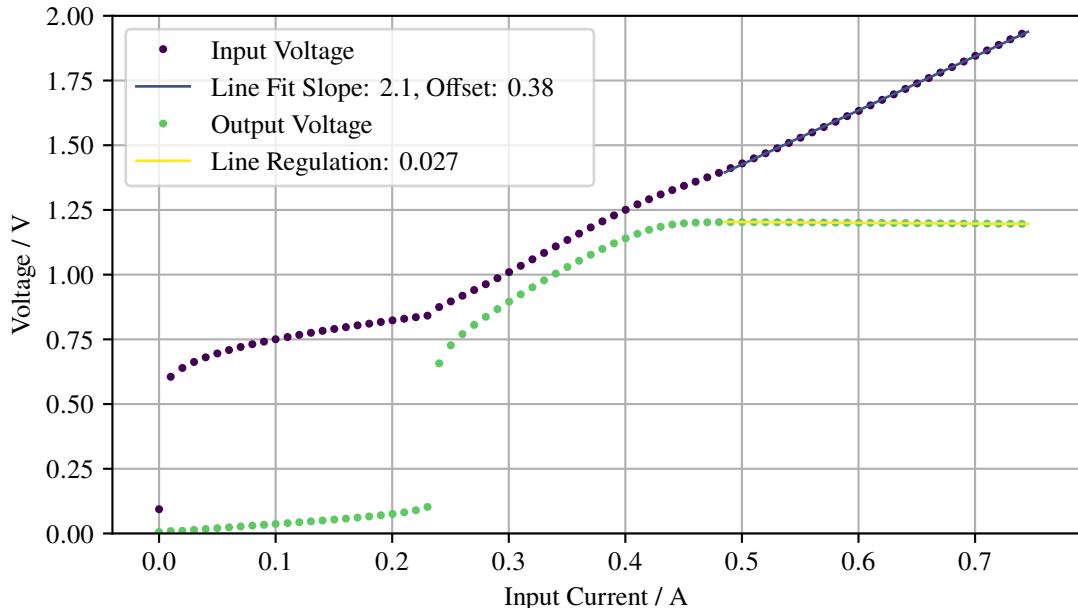
Figure 4.2: I-V characteristics of the 500 mA Shunt-LDO prototype chip. V_{ref} was chosen to be 600 mA. A line fit on V_{in} yields the effective input resistance of the Shunt-LDO $R_{in} \approx 2.1\,\Omega$. The fit range is constrained by the necessary dropout voltage $V_{do} = 200$ mV. The line regulation for a constant load $I_{load} = 0$ A is approximately 0.029 V A^{-1}

measurement, the regulator is set to a working point with a constant input current, in this case $I_{in} = 500$ mA. I_{load} is then increased stepwise while recording V_{in} and V_{out}. Unintuitive at first, V_{in} decreases during this measurement over the full range of I_{load}. This can again be explained the ground shift δV_{GND}: as the load current increases, less current needs to be returned from the Shunt-LDO ground to the PCB ground, but is instead returned directly on the PCB. This causes a decrease in δV_{GND} according to

$$\delta V_{GND} = -R_{wb} \cdot I_{load}. \tag{4.3}$$

The black line in Figure 4.4 illustrates the effect of this ground shift based on the approximation discussed above and is in good agreement with the observed behaviour. The resulting load regulation is listed in Table 4.2. As this measurement includes the mentioned ground shift, the load regulation performance is underestimated: with a reduction in δV_{GND}, V_{out} decreases, due to V_{ref} being referenced to the PCB ground. This effect amplifies the expected decrease in V_{out} from the increased load current. For the 15 parallel wire bonds connecting the Shunt-LDO ground to the PCB ground a shift $\Delta V_{out} \mathcal{O}(5$ mV$)$ is expected for the full range of I_{load}. As a consequence the load regulation performance of the Shunt-LDO can be considered
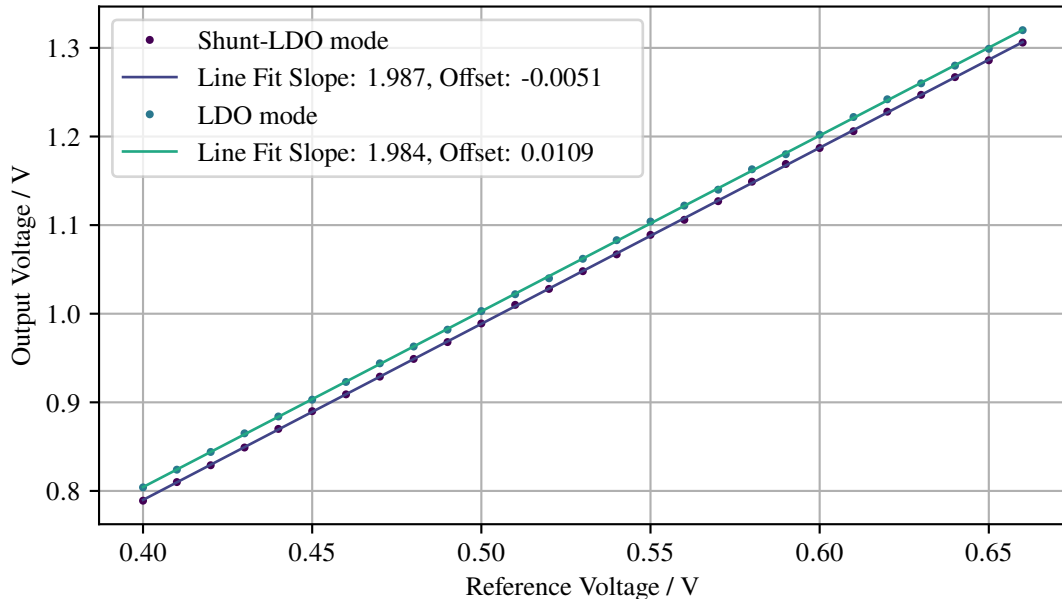
Figure 4.3: Relation of V_{ref} and V_{out} at a constant working point of $V_{\text{in}} = 1.42\,\text{V}$, corresponding to $I_{\text{in}} = 500\,\text{mA}$ in Shunt-LDO mode, measured in both LDO mode and in Shunt-LDO mode. No load was drawn from the regulator.
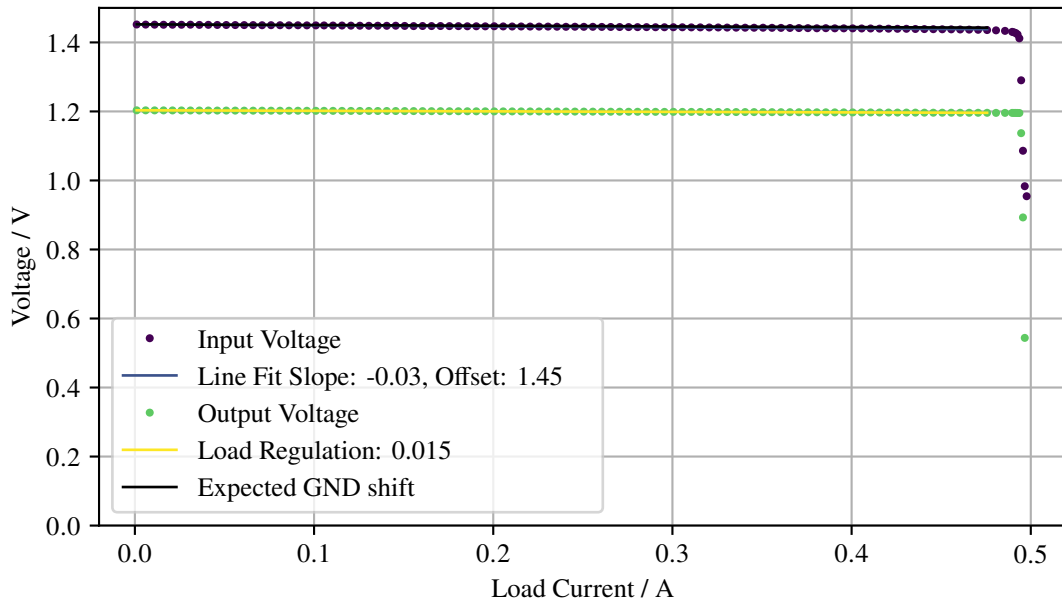
Figure 4.4: Load Regulation of the Shunt-LDO with a constant input current $I_{\text{in}} = 500\,\text{mA}$. Once I_{load} approaches I_{in}, the Shunt-LDO gets starved of current and can not keep its working point up.

very good with a total change in V_{out} of $\lesssim 2\,\text{mV}$. Once I_{load} approaches the input current I_{in}, both V_{in} and V_{out} decrease rapidly, as the load attempts to draw more current from the Shunt-LDO than is supplied to the regulator. This manifests itself in a vanishing shunt current $I_{\text{shunt}} \to 0\,\text{A}$. In the example shown in Figure 4.4 this is the case for $I_{\text{shunt}} \leq 10\,\text{mA}$. Due to its origin this phenomenon is referred to as *undershunt current condition*, or alternatively as *overload* of the Shunt-LDO. Such an overloaded Shunt-LDO appears to have a lower R_{in} compared to a Shunt-LDO in stable operation. Since such a rapid change in V_{in} can directly translate to a transient on V_{mod} in a SP chain, it is necessary to protect the SP chain against possible Shunt-LDO overloads. Different mitigation strategies will be discussed in Section 4.3 and Chapter 5.

As each ROC will be equipped with two Shunt-LDO, powering the analog and digital domain respectively, the behaviour of Shunt-LDO connected in parallel needs to be considered, too. In addition to the single Shunt-LDO characteristics this includes the current sharing between regulators. Considering two parallel Shunt-LDO with the same working point, a perfect current balancing between both regulators is desired. Imperfect current sharing would require additional current to be provided to the system, which increases I_{shunt} and thus the current headroom on the Shunt-LDO drawing more current. The power efficiency of such a regulator would decrease as shown in Equation 3.13 and Figure 3.6. An example for the parallel operation of multiple Shunt-LDO regulators is shown in Figure 4.5(a). Here, two regulators on the same die have been operated with differing reference voltages $V_{\text{ref},1} = 600\,\text{mV}$ and $V_{\text{ref},2} = 500\,\text{mV}$ respectively. The combined slope of the two-regulator system is roughly half the slope of a single regulator - contributions to the effective input resistance from wirebonds or the PCB are not affected, as the two parallel regulators are on the same silicon die. The line regulation for both regulators used are $0.012\,\text{V}\,\text{A}^{-1}$ and $0.023\,\text{V}\,\text{A}^{-1}$ respectively.

It needs to be noted that due to the limited range of available input currents, the fit range for Shunt-LDO$_{\#1}$ is much smaller compared to Shunt-LDO$_{\#2}$. Thus the determined line regulation of Shunt-LDO$_{\#1}$ is less accurate and not as susceptible to e.g. thermal effects, resulting in a artificially lowered line regulation. Prior to saturation, V_{out} of a Shunt-LDO follows V_{in} until V_{in} exceeds $V_{\text{out}} + V_{\text{do}}$. Thus Shunt-LDO$_{\#2}$ with a target output voltage $V_{\text{out}} = 1\,\text{V}$ saturates before Shunt-LDO$_{\#1}$, which in turn requires $V_{\text{in}} \geq 1.4\,\text{V}$ to saturate. The load regulation of the two-Shunt-LDO-system is shown in Figure 4.5(b). Both regulators show a load regulation of $\leq 0.02\,\Omega$, being compatible with single regulator measurements. The current balancing between parallel Shunt-LDO can not be easily measured using the PCB shown in Figure 4.1, as the individual current paths are not accessible. To offer the possibility for accurate studies of the current sharing between regulators, a dedicated test PCB was available. The board can be seen in Figure 4.6(a). On this PCB, the input current trace is split in two traces of matched impedance, the current flowing through each trace can be

(a) Input IV curve.

(b) Combined load regulation.
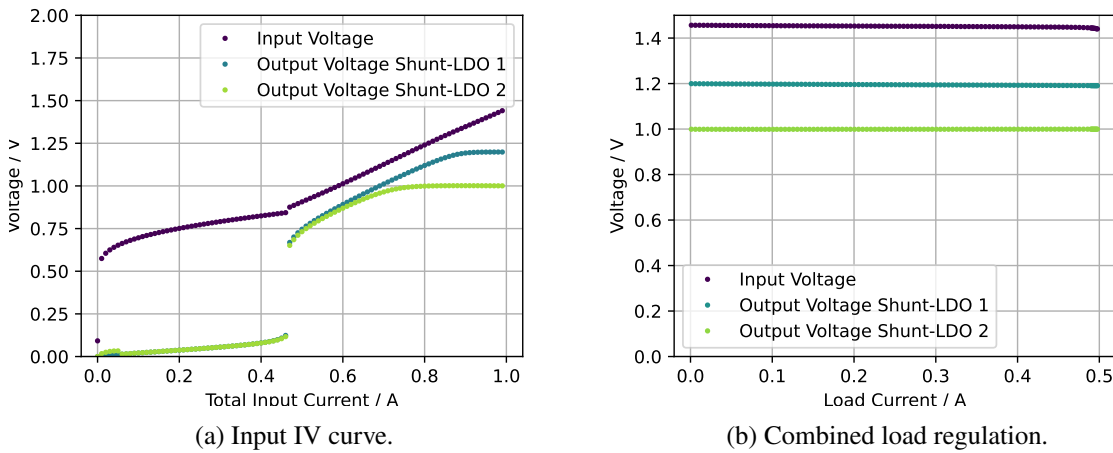
Figure 4.5: Combined input IV 4.5(a) and load regulation 4.5(b) of two parallel Shunt-LDO. $V_{\mathrm{ref},1} = 600\,\mathrm{mV}$ and $V_{\mathrm{ref},2} = 500\,\mathrm{mV}$ respectively. During the line regulation measurement, no load current was drawn from the Shunt-LDO. The load regulation measurement was performed for $I_{\mathrm{in}} = 1\,\mathrm{A}$.

measured using a $10\,\mathrm{m\Omega}$ resistor. To improve the current sensing accuracy, the resistors used have a specified accuracy of $\leq 0.1\%$. These current sharing studies were part of a bachelor thesis supervised in the context of this thesis [44]. The measurement shown in Figure 4.6(b) indicates a good current sharing between parallel Shunt-LDO, operated with the same target working point, in the relevant range of I_{in}. In general the Shunt-LDO performs well in parallel operation with line- and load regulation figures compatible with the stand-alone case.

Changes in the digital activity of the ROC can lead to fast changes in the load current drawn from the Shunt-LDO. In order to simulate the Shunt-LDO response to such load transients, an additional path for the load current is provided in the shape of an NMOS transistor which is steered by fast voltage pulses. During the transient, V_{out} is expected to decrease for increasing load currents and vice versa, until after a short time the regulator stabilises again. According to simulations of the Shunt-LDO design, the transient response of V_{out} is expected to be up to $\pm 30\,\mathrm{mV}$ for load changes on a time scale of a few ns. With both analog and digital domain of the ROC being powered by their own Shunt-LDO, a transient on the digital Shunt-LDO should not affect the analog Shunt-LDO, which is connected in parallel. In Figure 4.7 the response of the Shunt-LDO to a load pulse with a rise time of $100\,\mathrm{ns}$ and $5\,\mathrm{ns}$ is shown. Here two Shunt-LDO are operated in parallel, one with a constant load current of $200\,\mathrm{mA}$, while for the second Shunt-LDO a load transient $\Delta I_{\mathrm{load}} = 200\,\mathrm{mA}$ is applied on top of a constant load current of $200\,\mathrm{mA}$. For slower rise times, the behaviour is as expected. Once an additional load current is drawn, the output voltage of the Shunt-LDO drops rapidly before recovering within $10\,\mathrm{\mu s}$. As the additional load current is switched off, the output voltage spikes to
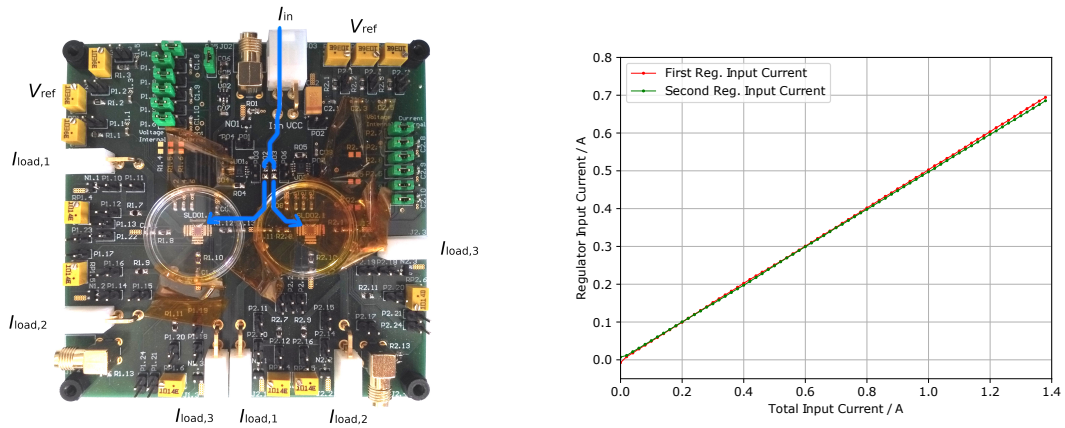
(a) Test PCB with two 500 mA Shunt-LDO prototype chips used for current sharing studies.

(b) Current sharing between two parallel Shunt-LDO during ramp-up of I_{in}.

Figure 4.6: Test PCB for current sharing studies with the 500 mA prototype chip (4.6(a)) and example measurement of current sharing between two parallel Shunt-LDO (4.6(b)). Adapted from [44].

larger values and then recovers on a similar time scale. The output voltage of the Shunt-LDO changes by less than 20 mV, which is well within the specifications. The regulator placed in parallel, which does not see a load transient, shows no significant response. For faster load pulses with a rise time of 5 ns, the Shunt-LDO shows a more pronounced response. As listed in Table 4.2, large transients on the output voltage of up to 130 mV can be seen. The output voltage stabilizes again within 10 μs, but shows significant, high frequency oscillations during this time. The load current drawn by the power transistor, as sensed over an 100 mΩ resistor, shows an unexpected superimposed oscillation. The Shunt-LDO connected in parallel is affected as well with its output voltage showing oscillations with an envelope of 50 mV. The observed oscillations could not be reproduced in simulations of the Shunt-LDO but showed sensitivity to the measurement setup, pointing towards them being caused by parasitics in the measurement setup. On the rising edge of the load pulse the response of the Shunt-LDO shows a much more stable response, as shown in Figure 4.7(e) and is in good agreement with simulations of the Shunt-LDO.

In order to verify the radiation hardness of this first Shunt-LDO design in 65 nm, a prototype chip was irradiated with X-rays at CERN to a target total ionising dose (TID) of 600 Mrad, including some headroom to account for uncertainties in the dose rate provided by the X-ray cabinet. This irradiation campaign was conducted by a small collaboration with significant contributions in the context of this thesis. Initially, the dose rate per hour was chosen small, starting at $10\,\mathrm{krad\,h^{-1}}$, as during the first few Mrad most radiation effects were expected. With increasing TID, the dose rate was increased to $3.43\,\mathrm{Mrad\,h^{-1}}$, the maximum achievable dose rate in the setup, to reach the target TID in a reasonable time. During the irradiation,

(a) Rise time 100 ns, rising - and falling edge shown

(b) Rise time 5 ns, rising - and falling edge shown

(c) Rise time 100 ns, zoom in on falling edge shown

(d) Rise time 5 ns, zoom in on falling edge shown

(e) Rise time 5 ns, zoom in on rising edge shown
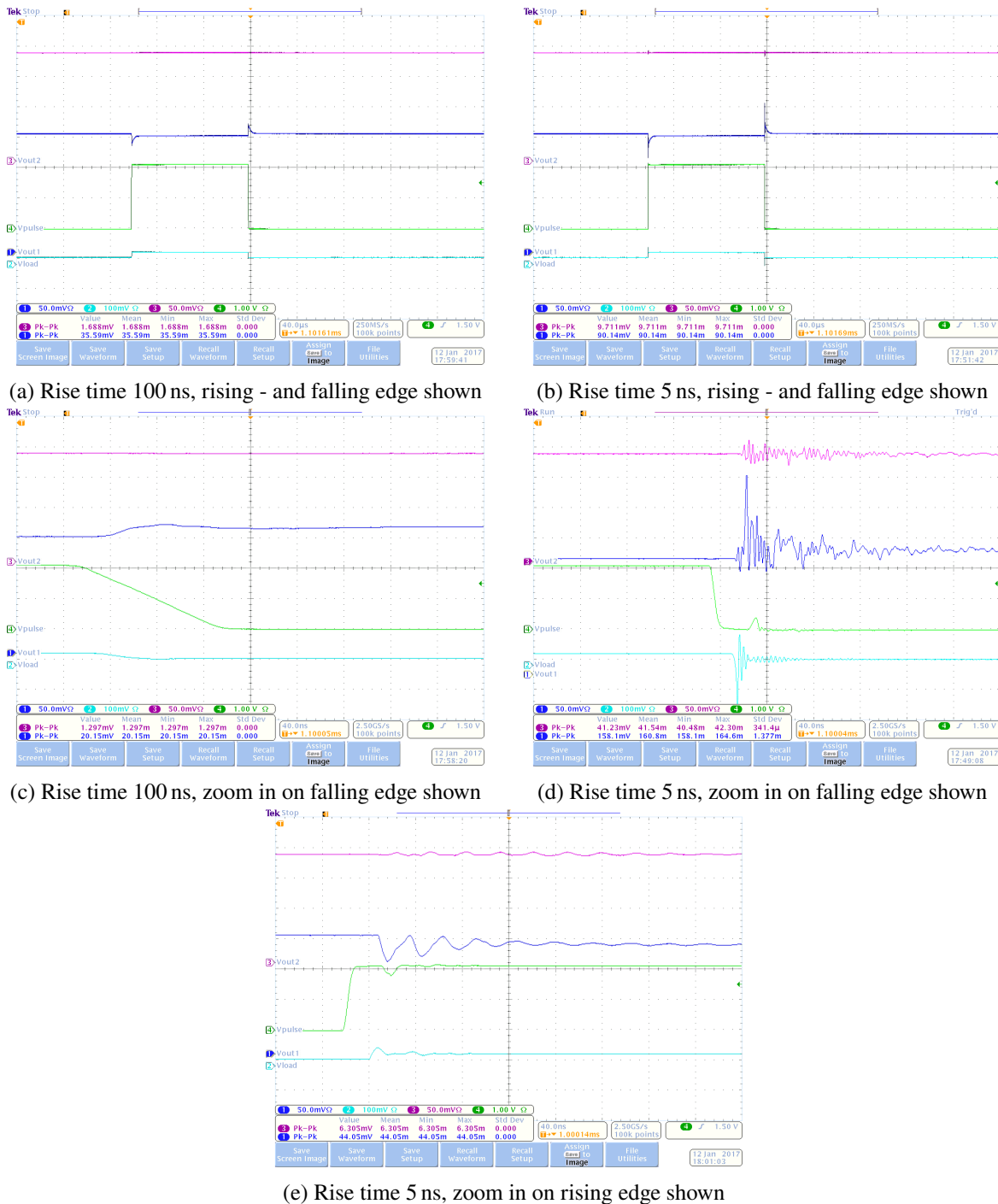
Figure 4.7: Two parallel Shunt-LDO, one is subjected to a load pulse of 200 mA. The voltage pulse causing the transient is shown in green, the load pulse as sensed using a 100 mΩ resistor in cyan. The output voltage of the regulator experiencing the load change is shown in blue, the output of the second regulator is shown in purple. In Figure 4.7(a) and Figure 4.7(c), the rise time of the load pulse is 100 ns. In Figure 4.7(b) and Figure 4.7(b), the rise time is 5 ns.
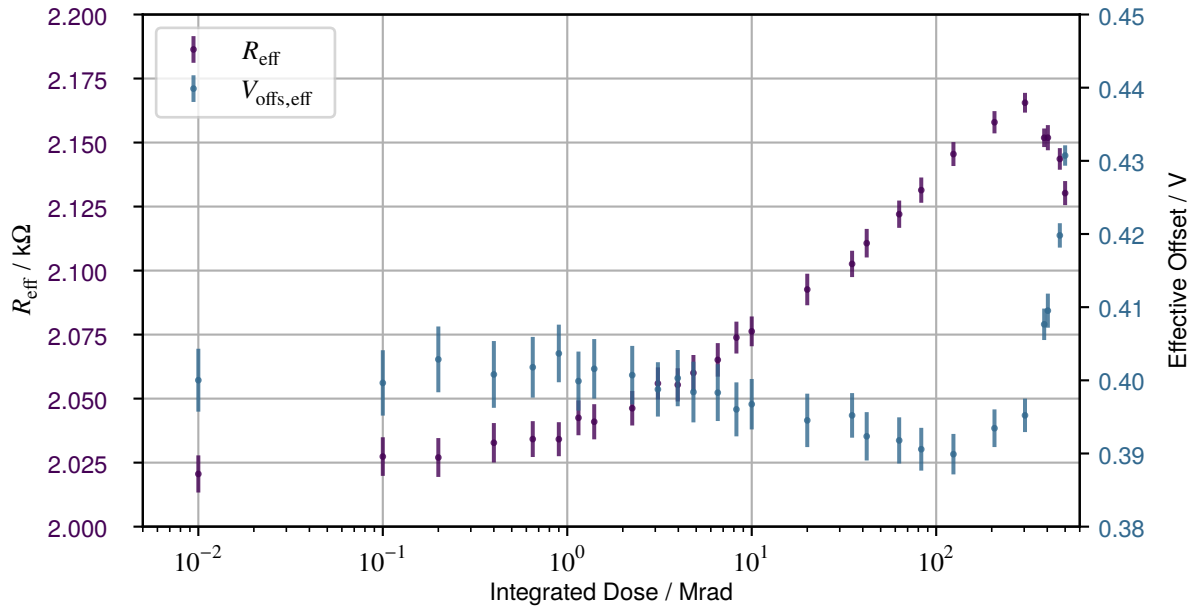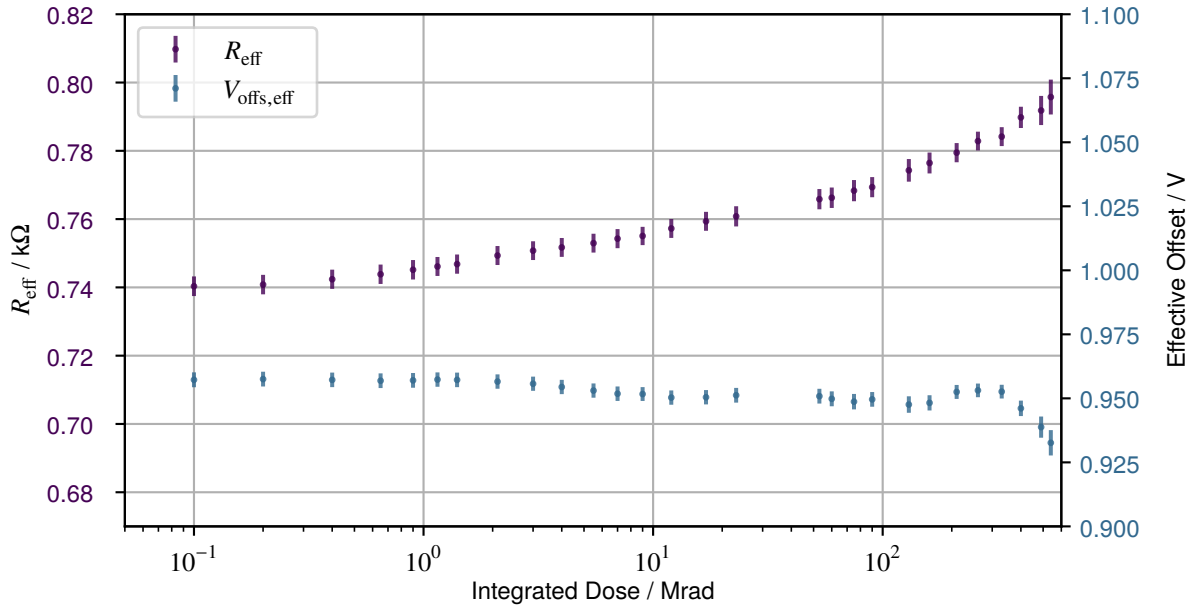
Figure 4.8: Effective input resistance R_{in} and offset voltage V_{ofs} of the 500 mA Shunt-LDO prototype during the X-ray irradiation campaign. Error bars give the fit uncertainty from the covariance matrix.

two Shunt-LDO on the PCB were operated in parallel: $SLDO_1$ in Shunt-LDO mode and $SLDO_2$ in LDO mode. The working point for $SLDO_1$ during the irradiation was chosen as $I_{in} = 0.5$ A with a constant load $I_{load} = 0.25$ A drawn. $SLDO_2$ was operated without any applied load, resulting in a negligible current consumption. At each intermediate TID step the input IV curve, line- and load regulation of $SLDO_1$ was measured. The response to load transients was recorded at the end of the campaign, as the setup did not allow tracking transient measurements during the irradiation.

The R_{in} of the Shunt-LDO extracted from the input IV measurements as a function of TID is shown in Figure 4.8 together with the effective offset voltage given by V_{M6}. Error bars represent the uncertainties on the fit parameters. A drift in either R_{in} or offset of the Shunt-LDO input IV is undesirable, as this can lead to unbalanced current sharing between parallel Shunt-LDO, which in turn requires more current headroom and reduces power efficiency. The effective offset remains largely constant during irradiation and only increases for very large TID, which is understood to be caused by an increase of the threshold voltage of transistor M_6 and expected from simulation. The effective slope shows an increasing trend as well, potential causes are radiation damage to the internal R_{shunt} or the current mirror. For the largest TID, the extracted slopes decrease again. To better understand this behaviour, dedicated monitoring of the current mirror and usage of a more radiation hard R_{shunt} are
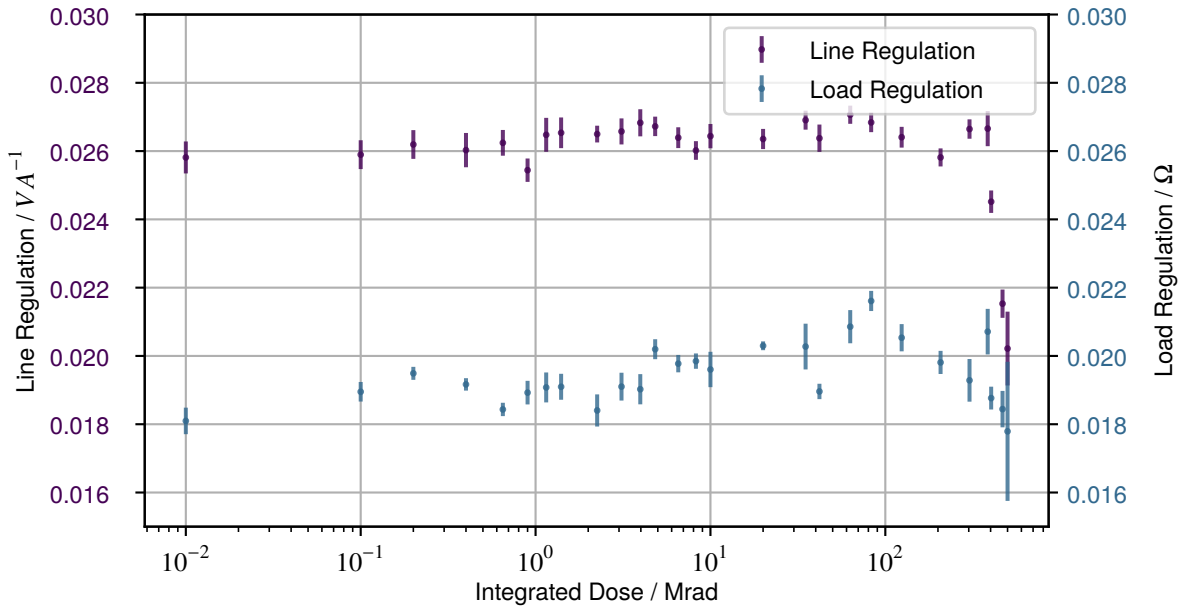
Figure 4.9: Line regulation of the 500 mA Shunt-LDO prototype during the X-ray irradiation campaign. Error bars give the fit uncertainty from the covariance matrix.

necessary, both of which were not considered for this radiation campaign. The shift in the threshold voltage of M_6 on the other hand can be controlled by introduction of an actively steered offset, see Figure 3.7. The line- and load regulation as a function of TID are shown in Figure 4.9. For the line regulation measurement, the same fit constraints as for the input IV measurement apply, while for the load regulation the full range of $I_{\text{load}} = [0 - 500]$mA can be utilized as the Shunt-LDO was not driven into overload. Up to an absorbed dose of a few $O(100\,\text{Mrad})$, the line regulation stays mostly constant and is in agreement with the measurement presented in Figure 4.2. For large doses, the line regulation decreases by some margin, however this is only covered by the last measurement points. For the shifts in operating point at larger TID, this corresponds to a better regulation of V_{out} and is beneficial. The load regulation on the other hand remains largely constant during irradiation. The effect of the absorbed radiation dose on the working point of the Shunt-LDO during irradiation can be seen in Figure 4.10. As can be expected from Figure 4.8, V_{in} increases significantly with increasing TID for a constant working point. Following expectation, V_{in} decreases once a load current is drawn from the Shunt-LDO. The output voltage V_{out} decreases significantly for large TID. Possible reasons for this behaviour are the line regulation, as the operating point shifts to larger V_{in} as well as a degrading output steering precision: since the reference V_{ref} was provided by a dedicated voltage supply it remained constant during the campaign. The
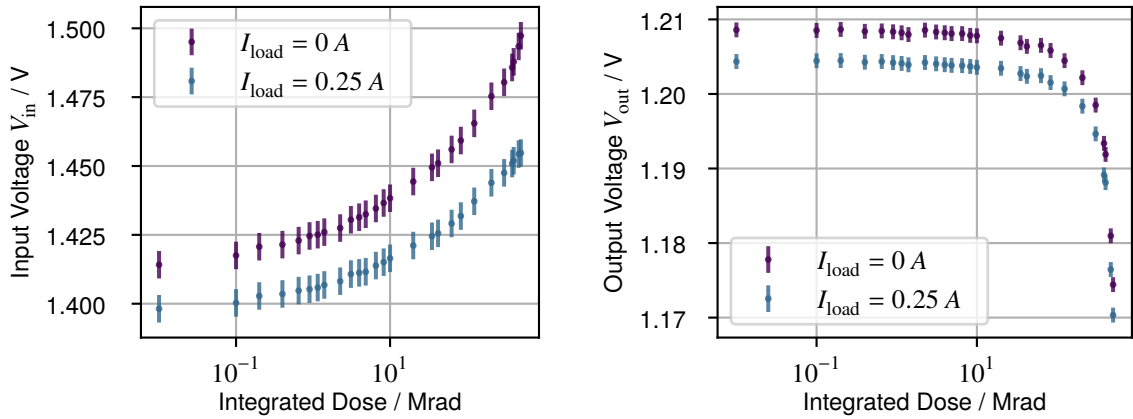
(a) Input voltage V_{in} as function of TID

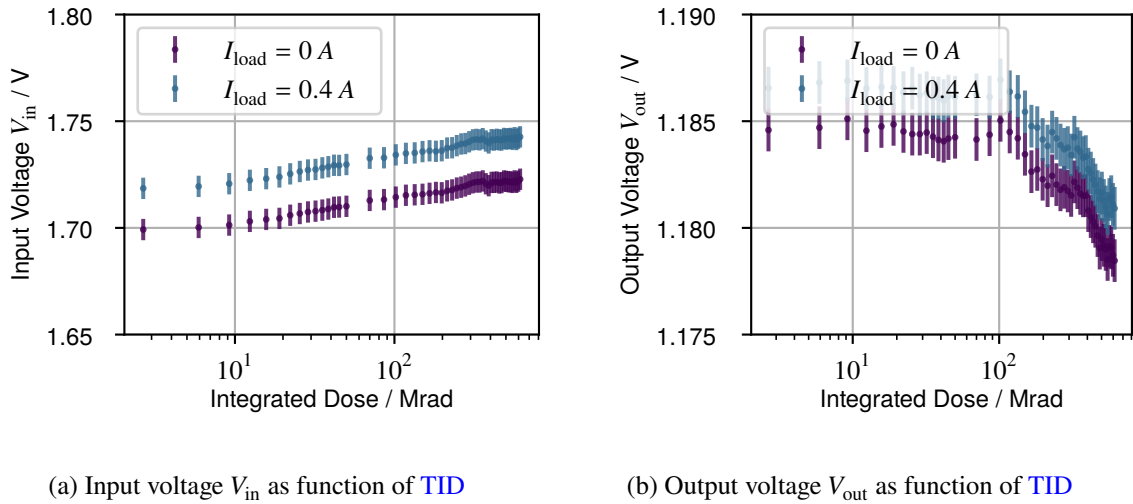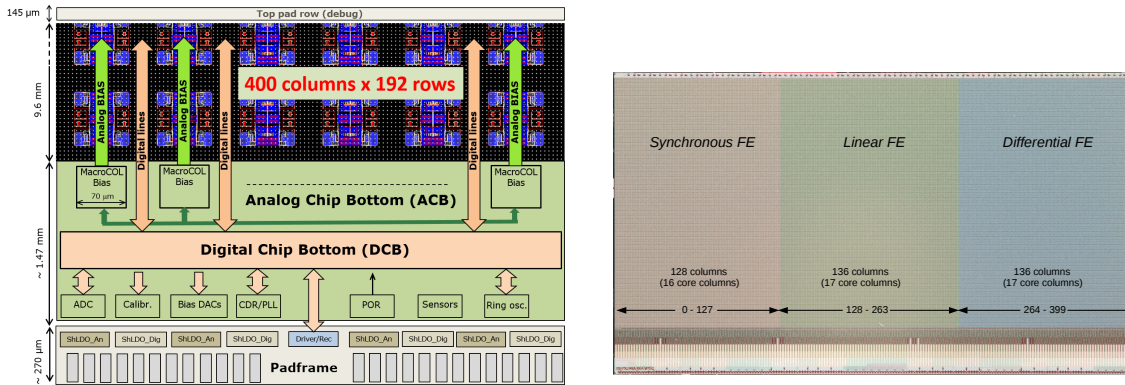(b) Input voltage V_{out} as function of TID

Figure 4.10: V_{in} and V_{out} as function of TID at an operating point $I_{in} = 0.5$ A with both no load current drawn and a load current of 0.25 A, the default working point during irradiation.

load transient response of the Shunt-LDO, shown after irradiation in Figure 4.11, is degraded comparing to Figure 4.7. This is especially the case for the parallel regulator in LDO mode, which ideally should not respond to load transients at all. Again the Shunt-LDO responds better to the rising edge of the load pulse compared to the falling edge. As discussed before, the superimposed oscillations are understood to be largely driven by parasitics and not actual Shunt-LDO behaviour. After annealing for 24 h at room temperature, the regulator transient response does not change significantly, the exception being the response of the regulator in LDO mode.

(a) Rise time 5 ns, zoom in on rising edge shown

(b) Rise time 5 ns, zoom in on falling edge shown

(c) Rise time 5 ns, zoom in on rising edge shown

(d) Rise time 5 ns, zoom in on falling edge shown
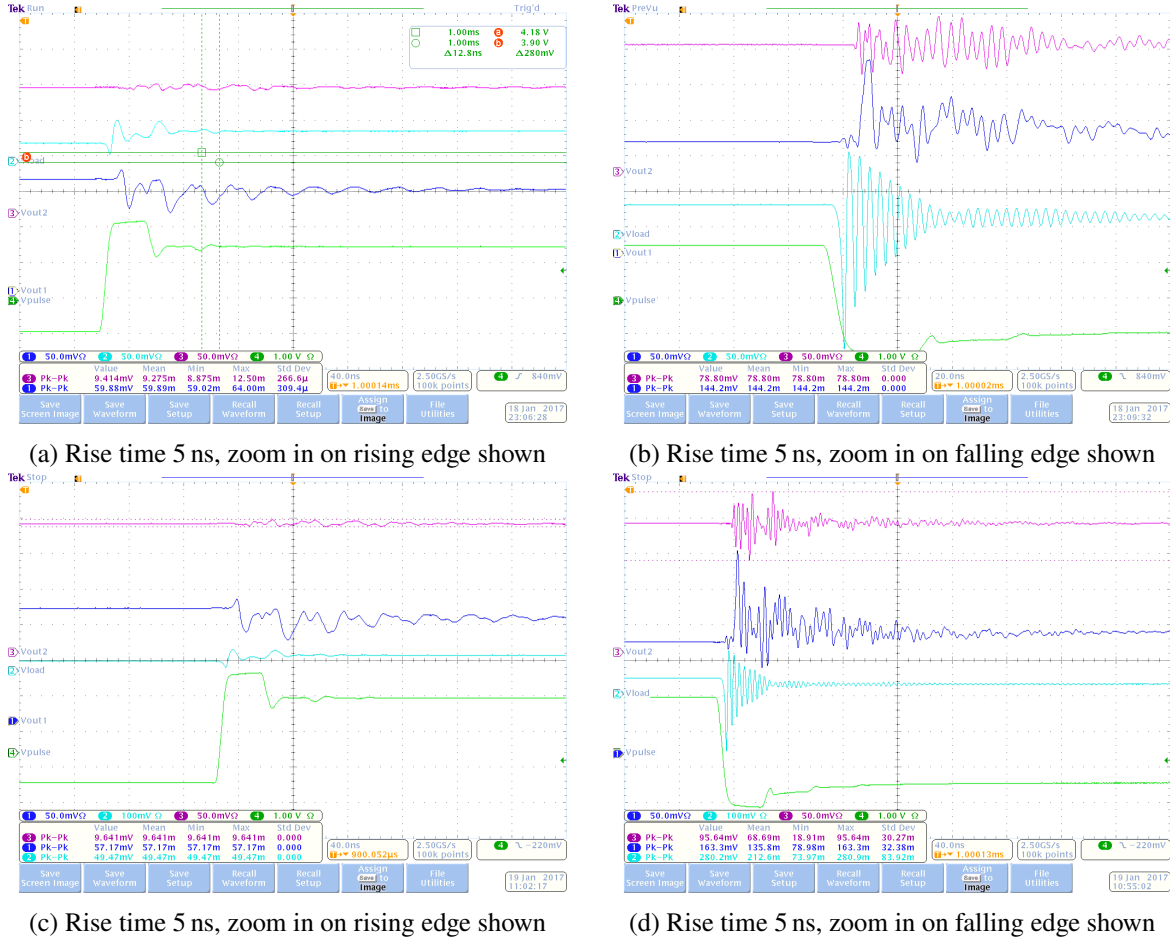
Figure 4.11: Load response measurement as shown in Figure 4.7. The voltage pulse causing the transient with a rise time of 5 ns is shown in green, the load pulse as sensed using a 100 mΩ resistor in cyan. The output voltage of the regulator experiencing the load change is shown in blue, the output of the second regulator is shown in purple. In Figure 4.11(a) and Figure 4.11(a), the transient response after reaching the target TID is shown, while Figure 4.11(c) and Figure 4.11(c) reflect the behaviour after annealing at room temperature for 24 h.

4.1.2 2 A prototype

The 500 mA prototype was followed by an up-
scaled design featuring a first implementation
of an actively steered offset voltage V_{ofs} and an
internal bandgap reference circuit to generate V_{ref}
and V_{ofs}. Alternatively both V_{ref} and V_{ofs} can be
generated by an external bandgap on the PCB or
using variable resistors and the common supply
voltage V_{CC} similar to the 500 mA prototype. In
addition this Shunt-LDO is rated for shunt cur-
rents up to 2 A. Since the voltage rating of the
Shunt-LDO is unchanged, the internal resistor
R_{shunt} is reduced to 600 Ω. According to Equa-
tion 3.8 this would correspond to $R_{\mathrm{eff}} = 600$ mΩ.
As the increased current rating for this prototype
requires significantly more space on the die as
well as more wirebonds, only one regulator is
implemented per die, compared to the three reg-
ulators per die in the previous iteration. The
test PCB, shown in Figure 4.12, expands on the

Figure 4.12: The 2 A Shunt-LDO on a test
board.

features of the 500 mA prototype by providing dedicated sensing lines for e.g. V_{in}, V_{out} and
the regulator ground potential I_{out}, which significantly reduces the impact of wirebonds and
trace resistance of the PCB on measurement accuracy. The characterization of this chip
followed the procedure outlined for the 500 mA prototype and was extended by dedicated
investigations of the temperature behaviour of the Shunt-LDO and the current mirror ratio k.
To proof the radiation hardness of the updated regulator, two X-ray irradiation campaigns
were conducted with the regulator being at room temperature first followed by a second
regulator irradiated at −10 °C. The detailed characterization of this prototype chip was part
of a bachelor thesis supervised in the context of this thesis [44] and only key points will be
covered here. The irradiation campaigns were performed by the same collaboration as for the
500 mA prototype, with key results being published as a conference proceeding [45].

The input IV curve and load regulation of the 2 A Shunt-LDO measured at room temperature
can be seen in Figure 4.13. In both cases the offset voltage V_{ofs} was chosen as 800 mV and
the reference voltage V_{ref} as 600 mV. As the bandgap reference in this prototype was not
working reliably, both V_{ref} and V_{ofs} were generated from V_{CC} using variable resistors. The
load regulation was measured at $I_{\mathrm{in}} = 0.86$ A to ensure $V_{\mathrm{do}} = 200$ mV. All voltages are
measured using the provided sensing lines and referenced to the chip ground potential I_{out}.

Line- and load regulation results of the 2 A Shunt-LDO prototype chip.	
R_{eff}	$0.77\,\Omega$
V_{ofs}	$0.73\,\text{V}$
$\frac{V_{\text{out}}}{V_{\text{ref}}}$	1.97 ± 0.01
Line Regulation	$0.022\,\text{V\,A}^{-1}$
Load Regulation	$0.002\,\Omega$
k-factor	863 ± 8

Table 4.3: Overview of results from the 2 A Shunt-LDO test chip. The transient response of this chip was not measured.
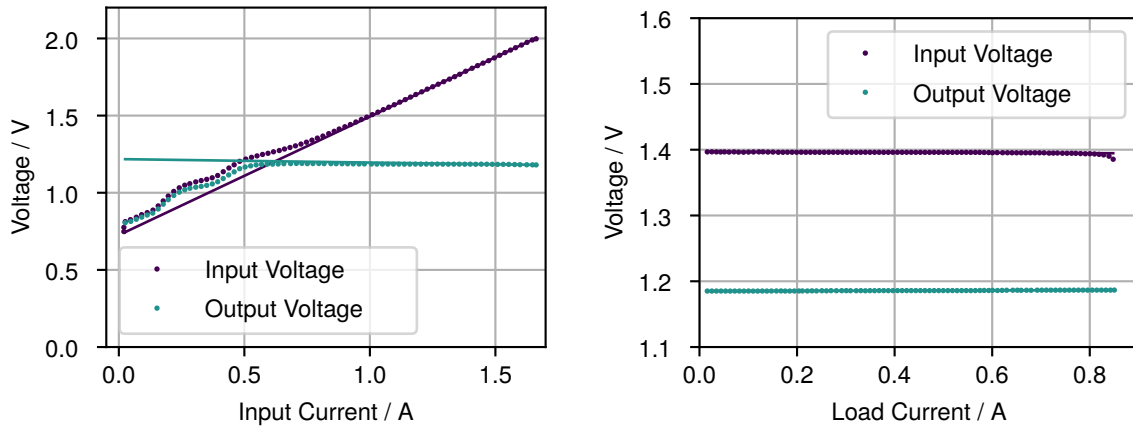
(a) Input IV curve and line regulation.

(b) Load regulation.

Figure 4.13: Input IV curve, line regulation 4.13(a) and load regulation 4.13(b) of the 2 A Shunt-LDO prototype chip.

Key results from the measurements are listed in Table 4.3.

The input resistance and effective offset from the input IV curve in Figure 4.13(a) can be found in Table 4.3. The line regulation performance is compatible with the 500 mA prototype with a change in the output voltage corresponding to $0.022\,\text{V\,A}^{-1}$. For the chosen slope and offset parameters this results in a ΔV_{out} of approximately 16 mV over the full operational range. While exceeding the targeted value $\Delta V_{\text{out}} \leq 10\,\text{mV}$ this performance is still considered acceptable. The output voltage steering shown in Figure 4.14 is slightly lower than expected and not constant over the full range, displaying a behaviour very similar to the 500 mA prototype. A small bump in the output steering can be seen in Figure 4.14.
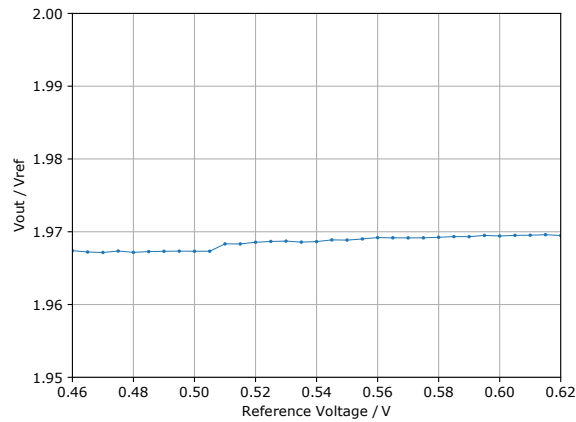
Figure 4.14: V_{out} steering precision for constant V_{ref} for different V_{ref} at a constant working point with
no load current drawn from the Shunt-LDO [44].

While the origin is not understood, this behaviour was observed to be independent of the
choice of the working point and load current of the Shunt-LDO [44]. The start-up behaviour
of this regulator differs significantly from the previous prototype, see Figure 4.2, which is
caused by the newly introduced offset regulation. As long as amplifier A_4 in Figure 3.7 is
saturated, no current can flow through the regulator for $V_{\text{in}} < V_{\text{ofs}}$. With the Shunt-LDO being
provided an input current this forces V_{in} to be larger than V_{ofs}. This condition depends on the
initial state of the then floating transistor M_7 however: should M_7 be sufficiently conductive,
A_4 can not be immediately saturated, the resulting input IV curve being comparable to the
500 mA prototype. The load regulation, as measured in Figure 4.13(b), is showing excellent
performance. As the load regulation is measured with the chip ground as reference, a ground
shift contribution similar to the 500 mA prototype is not observed.

While line- and load regulation and output steering performance are comparable with the
500 mA prototype, the extracted R_{eff} and V_{ofs} are in disagreement with the expectations. For
V_{ofs} only a small discrepancy is to be expected given by the ground shift between Shunt-LDO
and PCB, as V_{ofs} is set with the PCB ground as reference. The IV curve measurement however
uses the Shunt-LDO local ground as reference, so a shift $O(10\,\text{mV})$ caused by wire bond and
trace resistance is expected. The observed difference between measurement and expectation
exceeds this, indicating additional issues present in the implementation, e.g. parasitic effects.
In order to account for potential process variations between different chips, the effective V_{ofs}
was measured on 5 available chips, each of them being supplied the same 0.8 V offset voltage.
The average effective offset was measured to be $V_{\text{ofs}} = (0.734 \pm 0.008)$ V, indicating a small
statistical spread and a systematic shift, likely based on the offset circuit implementation. The
extracted slope from Figure 4.13(a) is significantly larger than expected, with a measured R_{in}
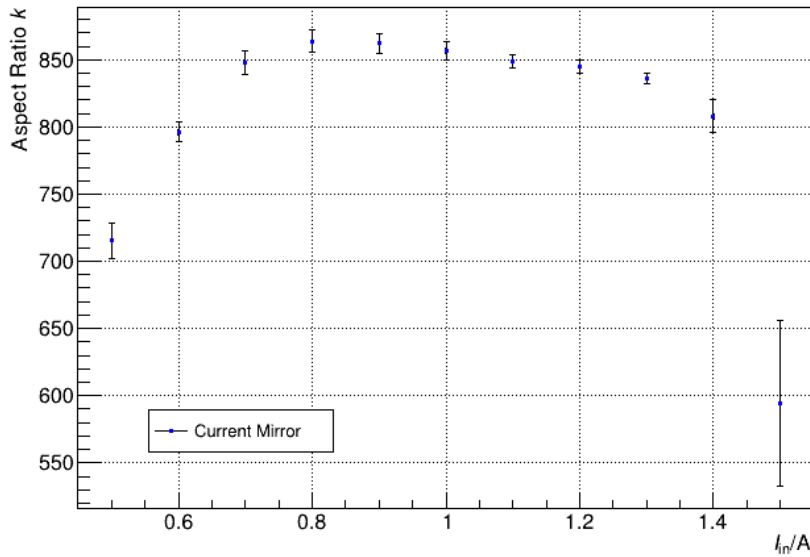
Figure 4.15: Current mirror ratio k at different working points of the 2 A Shunt-LDO, as averaged over 5 different chips [44].

of $0.77\,\Omega$ compared to an expected R_{in} of $0.6\,\Omega$. The two most likely sources of this deviation, see also Equation 3.8, are the current mirror ratio k and R_{shunt}. In the measurements presented here, a $0.6\,k\Omega$ resistor integrated on the silicon die was used as R_{shunt}. The k-factor can not be measured directly, as the transistors forming the current mirror can not be accessed. Instead it can only be obtained indirectly by measurement of I_{ctrl} and rearranging Equation 3.6. I_{ctrl} can be measured directly using an ammeter or by measuring the voltage drop over R_{shunt}, if a known resistor is used. As the internal R_{shunt} is not known with sufficient precision, I_{ctrl} is measured with an ammeter. k is then given as

$$k \approx \frac{I_{in}R_{shunt}}{V_{in} - V_{ofs}} = \frac{I_{in}}{I_{ctrl}}, \tag{4.4}$$

with $I_{ctrl} = \frac{V_{in}-V_{ofs}}{R_{shunt}}$. In Figure 4.15 a measurement of the k-factor is shown for different working points, averaged over the 5 available chips. For $I_{in} \leq 0.8\,A$ the regulator is not in the required operating range. Especially for very low currents the Shunt-LDO is not fully saturated and can exhibit unexpected behaviour. For $I_{in} \geq 0.8\,A$ k can be seen to decrease with increasing I_{in}, a behaviour expected to be caused by heat generation on the chip. For very large I_{in} the measured k-factor deviates significantly from chip to chip. At the operating point used for the load regulation measurements in Figure 4.13(b), the resulting average current mirror ratio is $k = 863 \pm 8$. Using the k-factor measurement and the effective R_{in} of the

regulator, the internal shunt resistor R_{int} can be obtained as $R_{int} = R_{eff} \cdot (k+2) = (658 \pm 7)\,\Omega$. As a comparison, R_{int} was measured directly by applying a voltage over R_{int} and measuring the resulting current, while the Shunt-LDO was not operated. Again averaged over 5 chips this yields $R_{int} = (621 \pm 3)\,\Omega$, which includes contributions such as trace resistances on the PCB and wire bonds and is not in agreement with the current mirror ratio measurement. A possible explanation for the discrepancy are parasitic impedances contributing to the R_{eff} measurement, e.g. from transistor M_6, but could ultimately not be fully understood in the context of this work. As R_{eff} of the Shunt-LDO is an important contributor to the power efficiency of a system with multiple parallel regulators, external high-precision SMD resistors will be used in the final experiment instead of on-chip resistors.

The radiation hardness of this Shunt-LDO prototype was again verified during an extensive X-ray irradiation campaign. In this campaign two chips were irradiated to the target TID of 500 Mrad: one chip at room temperature and one chip cooled down to $-10\,^\circ$C. The results presented here refer to the measurements at room temperature to provide a direct comparison to the predecessor prototype while the measurements at cold temperatures are shown in Figure 4.19 - Figure 4.21. The general procedure and figures of interest follow the procedure outlined in Section 4.1.1: the Shunt-LDO was operated at a constant working point $I_{in} = 1$ A, $I_{load} = 0.4$ A during irradiation with input IV curves and load regulation measurements at each TID step. V_{ofs} and V_{ref} were provided using dedicated voltage supplies with $V_{ofs} = 1$ V and $V_{ref} = 0.6$ V respectively. These TID steps were again chosen roughly on a logarithmic scale, providing more resolution at lower dose rates.

The effective input resistance R_{eff} and the effective V_{ofs} extracted from the input IV curves are shown in in Figure 4.16. In a similar observation compared to Figure 4.8, R_{eff} increases with the TID received. Unlike with the irradiation of the 500 mA prototype, there is no decrease in R_{eff} observed for the largest TID. The total observed increase in R_{eff} remains below 10 %, but with neither the k-factor nor R_{shunt} being monitored the exact cause can not be determined. The effective offset shows a much better response to the received TID, with the final V_{ofs} differing by ≤ 4 % compared to the unirradiated case. With V_{ofs} being provided by an external voltage supply and a negligible current being drawn from the V_{ofs} supply, no significant shift in V_{ofs} is expected. The causes for the shift in V_{ofs} presumably are either radiation damage in A_4, which should not occur to a significant extend, or the aforementioned issues of the implementation of the offset steering circuitry. The Shunt-LDO irradiated at $-10\,^\circ$C shows similar behaviour, as can be seen in Figure 4.19, but to a somewhat lesser extend. The line- and load regulation of the irradiated chip are shown in Figure 4.17. As seen before both parameters show better performance compared to the 500 mA prototype. For large received TID the relative decrease in regulation performance is significantly more pronounced, the previously unexpected increase in line regulation performance for large TID is not observed anymore. Since the baseline regulation performance of the unirradiated

Figure 4.16: Effective input resistance R_{in} and offset voltage V_{ofs} of the 2 A Shunt-LDO prototype during the X-ray irradiation campaign at room temperature. Error bars give the fit uncertainty from the covariance matrix.
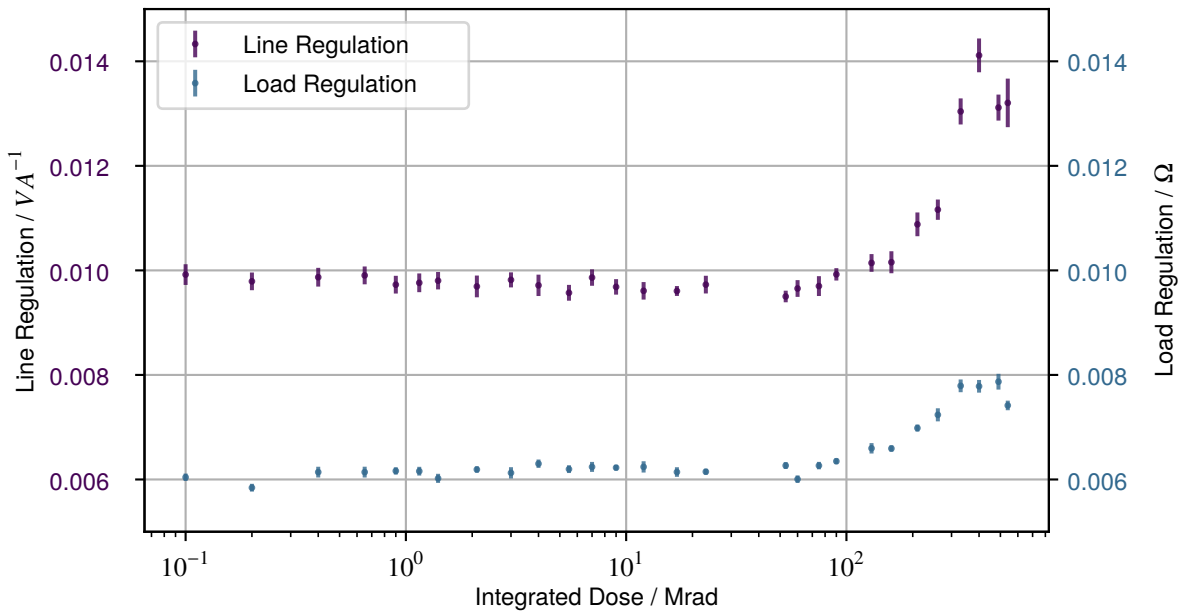
Figure 4.17: Line regulation of the 2 A Shunt-LDO prototype during the X-ray irradiation campaign at room temperature. Error bars give the fit uncertainty from the covariance matrix.
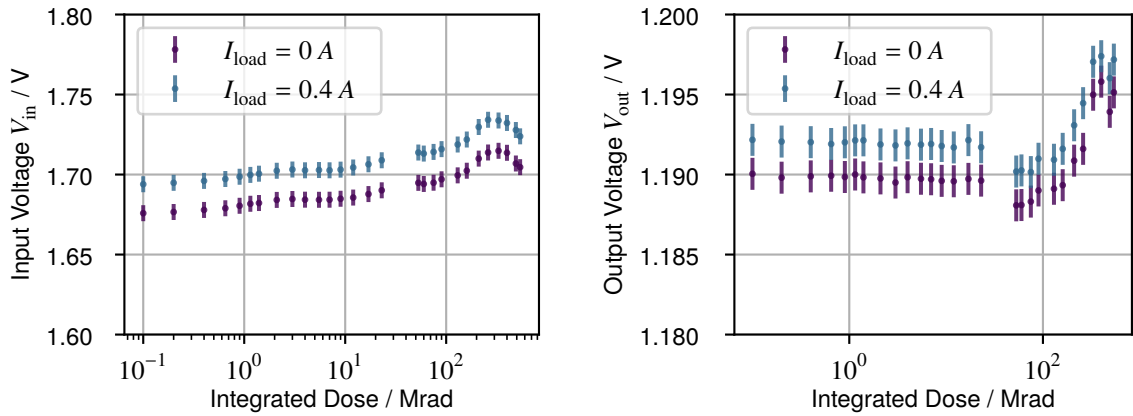
(a) Input voltage V_{in} as function of TID

(b) Output voltage V_{out} as function of TID

Figure 4.18: V_{in} and V_{out} as function of TID at an operating point $I_{in} = 1\,A$ with both no load current drawn and a load current of 0.4 A, the default working point during irradiation at room temperature.

Shunt-LDO improved so significantly this translates to very small absolute changes, resulting in the the fully irradiated regulator significantly outperforming the 500 mA prototype before irradiation. Comparing this to the Shunt-LDO irradiated at cold temperatures yields some more important differences. The cold Shunt-LDO, see Figure 4.20, shows in general a better line- and load regulation. In addition, the regulation performance does not seem to degrade significantly for high TID compared to the Shunt-LDO irradiated at room temperature.
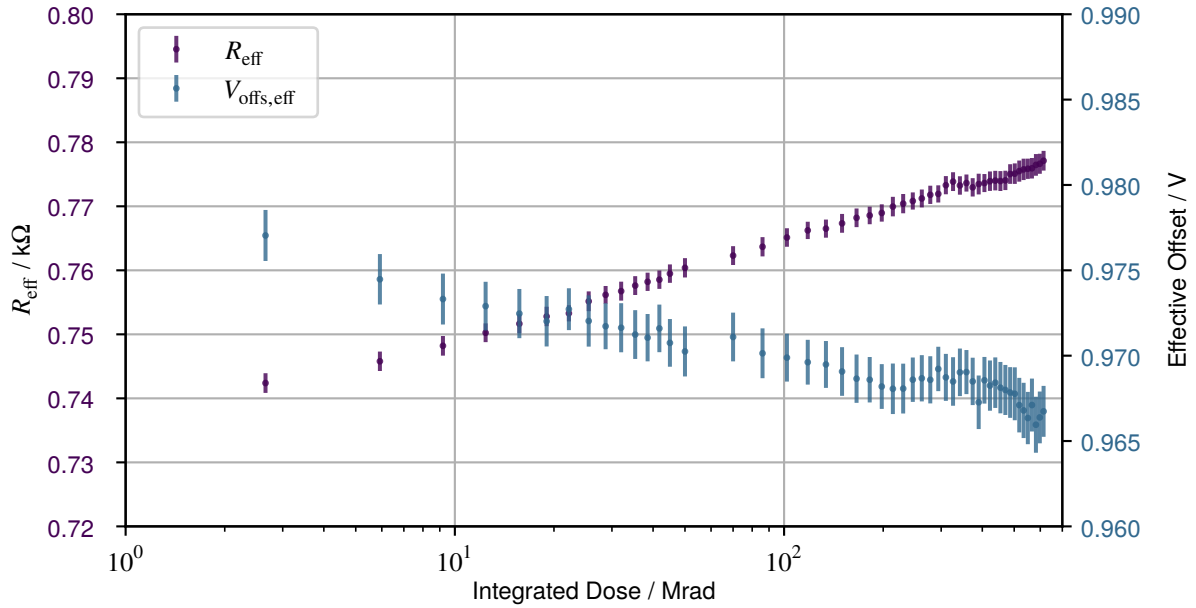
Figure 4.19: Effective input resistance R_{in} and offset voltage V_{ofs} of the 2 A Shunt-LDO prototype during the X-ray irradiation campaign at $-10\,°\mathrm{C}$. Error bars give the fit uncertainty from the covariance matrix.
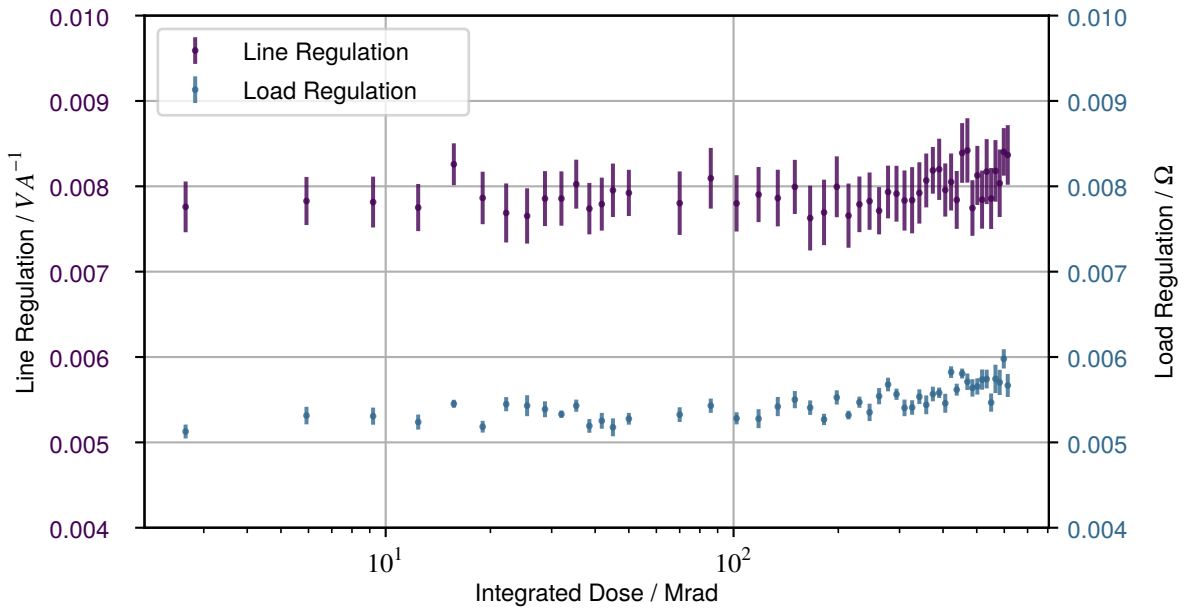
Figure 4.20: Line regulation of the 2 A Shunt-LDO prototype during the X-ray irradiation campaign at $-10\,°\mathrm{C}$. Error bars give the fit uncertainty from the covariance matrix.

(a) Input voltage V_{in} as function of TID

(b) Output voltage V_{out} as function of TID

Figure 4.21: V_{in} and V_{out} as function of TID at an operating point $I_{in} = 1$ A with both no load current drawn and a load current of 0.4 A, the default working point during irradiation at $-10\,°C$.

Finally, the effect of the irradiation on the working point of the 2 A prototype can be seen in Figure 4.18. Fitting to the observed increase in R_{eff}, V_{in} increases slightly for a constant I_{in} with increasing dose. Only for very large doses V_{in} decreases again, this corresponds in magnitude to the decrease in V_{ofs} seen in Figure 4.16. For the Shunt-LDO irradiated at cold temperatures, this decrease in V_{in} can not be resolved as visible in Figure 4.21(a), as the decrease in V_{ofs} is significantly smaller for high TID as seen comparing Figure 4.16 with Figure 4.19. V_{out} stays nearly constant for smaller TID and increases by a few mV for larger TID. This behaviour corresponds to the decreased performance in line regulation in Figure 4.17. With the regulation performance not showing a significant decrease at high TID for the Shunt-LDO irradiated at cold temperatures, V_{out} in Figure 4.21(b) is instead decreasing for large doses. This decreasing tendency can be seen in Figure 4.18(b) as well just below a TID of 100 Mrad. In addition, V_{out} is smaller by $\approx 5\,mV$. While the change in line regulation is relatively large as discussed, the change in the resulting V_{out} is almost negligible with $\Delta V_{out} \leq 1\,\%$. The presented behaviour does not change significantly when drawing a load current from the regulator with the exception of a small, almost constant offset to lower voltages. Recalling V_{ofs} and V_{ref} being referenced to the PCB GND and not to I_{out}, but both V_{in} and V_{out} measured with respect to I_{out}, this can be explained by the reduced δV_{GND} shift, which an increase in I_{load} causes as discussed in Section 4.1.1.

(a) Functional view of the RD53A floorplan. The physical dimensions of the ASIC are 20 mm × 11.6 mm with a pixel matrix of 400 × 192 pixel. The *bottom* of the chip includes the main pad frame and power distribution blocks as the Shunt-LDO.

(b) Different AFE flavors of the RD53A. *Synchronous AFE* covers columns 0 - 127, *Linear AFE* in columns 128 - 263 and *Differential AFE* in columns 264-400.

Figure 4.22: Functional overview of the RD53A floorplan and the different AFE flavours in RD53A. Taken from [39].

4.2 RD53A - A Prototype Readout ASIC with Serial Powering Capability

The RD53A is a next generation hybrid pixel readout chip [39]. designed in a commercial 65 nm CMOS node featuring a higher integration density of digital logic, rate capabilities and radiation hardness compared to ROC used in the current ATLAS and CMS experiments. The functional layout of the chip can be seen in Figure 4.22(a). With the final production chips for ATLAS and CMS being expected to be at least 20 mm in width, RD53A has a width of 20 mm which allows the chip bottom and padframe to be reused for the production design. The chip height is restricted by the available space on the wafer reticle, leading to a matrix of 400 × 192 pixel with a pixel size of 50 μm × 50 μm. For the production chips an increase in the row count is expected. The power - and bias distribution are designed for a larger matrix of up to 384 rows. RD53A is intended as a technology demonstrator to prove the suitability of the chosen 65 nm technology for a large ASIC in the context of the HL-LHC upgrades of ATLAS and CMS. Because it is not intended as a final production ASIC, RD53A contains design variations for testing purposes, most notably three different AFE designs leading to a non-uniform pixel matrix. Detailed information on the design of RD53A are available in [39], characterisation results of the RD53A can be, amongst others, found in [20, 46].

Different from previous pixel ROC, RD53A is designed specifically for serial powering operation with connections from the chip bottom only. The chip core is powered via two internal voltage rails, V_{DDA} and V_{DDD} for the analog and digital domains of the chip

Power Supply Limits		
Parameter	Typ.	Max.
Core supply voltage	1.2 V	1.32 V
Shunt-LDO input voltage	1.5 V	2 V
Per pixel analog current	4 µA	8 µA
Per pixel digital current	4 µA	6 µA
Periphery analog	30 mA	60 mA
Periphery digital	30 mA	60 mA
Output drivers (each)	20 mA	30 mA
Total current (4 outputs)	0.75 A	1.3 A
400×384 pixel periphery analog	30 mA	60 mA
400×384 pixel periphery digital	30 mA	60 mA
400×384 pixel total current (4 outputs)	1.4 A	2.3 A

Table 4.4: Overview of the design current draw and voltage supplies for RD53A. Taken from [39].

respectively. These voltage rails in turn are supplied by 2 on-chip Shunt-LDO regulators. The pass device and shunt transistors of these regulators are each split in four blocks along the chip bottom to prevent single hot spots in favor of a more even power dissipation along the chip bottom, yet there is only a single control circuit per regulator. Each of these regulator blocks is supplied by *active power pads*. These pads can be switched to control the on-chip voltage rails for V_{DDA} and V_{DDD}: in passive mode, the core voltages V_{DDA} and V_{DDD} can be provided externally, referred to as direct powering. In active mode, the regulator output voltages are used to supply V_{DDA} and V_{DDD} instead [39]. The local analog and digital ground potentials are separated on the ASIC and tied together with low impedance off-chip. The current rating of each active power pad has to account for the power draw of RD53A including some headroom. In Table 4.4 the estimated power draw for RD53A and a hypothetical chip with a full 400×384 pixel matrix is shown. For the full size chip, an absolute maximum current consumption of 1.5 A each digital and analog is assumed, corresponding to 375 mA per pad. Including headroom each pad has therefore been designed for a maximum current of 500 mA, yielding a maximum rated current of 4 A per ROC and 2 A per Shunt-LDO [39].

4.2.1 The Shunt-LDO in RD53A

The regulator layout is functionally very similar to the layout implemented in the previously discussed 2 A testchip and shown in Figure 4.23, including input and output pads. The typical values of control voltages and pin assignments of the Shunt-LDO in RD53A are listed in Table 4.5. The offset voltage V_{ofs} is generated by means of a current source generating a reference current $I_{\text{ofs}} = 2\,\mu\text{A}$. This current is drained to an external resistor to ground. The resulting voltage is amplified by a factor 2 by A_5 and fed into A_4. The multiplication in A_5 is necessary as target values for V_{ofs} exceed the voltage provided by the bandgap reference. Accordingly the offset voltage for RD53A is given as

$$V_{\text{ofs}} = 2I_{\text{ofs}}R_{\text{ofs}}. \tag{4.5}$$

The internal resistor R_3 is again designed as 600 Ω. In RD53A this is an inefficient choice for reasonable offset voltages of around 1 V, as the set current to operate the Shunt-LDO at its typical working point $V_{\text{in}} = 1.5\,\text{V}$ would be much larger than the nominal analog or digital currents. Thus, and due to the higher precision achievable with external SMD resistors, an external resistor R_{shunt} will be connected between V_{in} and R_{ext}, leaving R_3 in Figure 4.23 floating. The choice of both R_{shunt} and R_{ofs}, defining the working point of the Shunt-LDO, are driven by the power consumption of the RD53A ROC. In first estimation the operation range of the Shunt-LDO could be defined by the minimum and maximum required current of RD53A. Thus, with a dropout voltage of 200 mV and a core supply voltage of 1.2 V, the supply voltage of the Shunt-LDO should exceed 1.4 V for the current drawn by RD53A, see Table 4.4. The maximum allowed input voltage of the Shunt-LDO however should never be exceeded. In this example, an effective resistance of $R_{\text{eff}} = 185\,\text{m}\Omega$ would be required for RD53A. The necessary offset voltage V_{ofs} can then be calculated as

$$V_{\text{ofs}} = V_{\text{in}} - I_{\text{in}} \cdot R_{\text{eff}} = 1.4\,\text{V} - 0.75\,\text{A} \cdot 185\,\text{m}\Omega \approx 1.25\,\text{V}. \tag{4.6}$$

The resulting values for R_{shunt} and R_{ofs} are 370 Ω and 312.5 kΩ respectively. Alternatively, one can determine R_{ofs} and R_{shunt} by setting a desired V_{ofs} and determining the required slope from a single working point. Assuming a target offset $V_{\text{ofs}} = 1\,\text{V}$ and a typical current draw of 500 mA per regulator, which includes ample headroom, the resulting R_{shunt} is around 800 Ω. This configuration is used in most measurements presented here as well as during RD53A waferprobing [20]. The control voltages of the Shunt-LDO, namely V_{ref} and the supply voltage for I_{ofs} generation are provided by the RD53A core bandgap, which is in turn supplied by the output voltage of the digital Shunt-LDO, V_{DDD}. This circular dependency between regulator output and generation of reference voltages and currents can be problematic for operation of RD53A as will be explained in this chapter. Both the analog and digital reference voltage V_{ref}

Pin	Type	Min.	Typ.	Max.	Descr.
V_{in}	Power	1.4 V	–	2 V	Input voltage
I_{in}	Power	0.5 A	–	2 A	Input current
V_{Shunt}	Power	1.4 V	–	2 V	Shunt circuitry supply voltage
GND	Ground	–	–	–	Local ground
V_{DD}	Power	1 V	1.2 V	1.32 V	Shunt-LDO output
V_{ref}	Analog	0.5 V	0.6 V	0.66 V	Reference voltage
R_{int}	Analog	–	V_{in}	–	Enable R_{int}
R_{ext}	Analog	300 Ω	–	–	External R_{shunt} to V_{in}
I_{ofs}	Analog	–	200 kΩ	–	External R_{ofs} to GND
COMP_{ENB}	Digital	–	GND	–	GND to enable compensation

Table 4.5: Assignment and typical orders of magnitude of Shunt-LDO circuit pins [39].
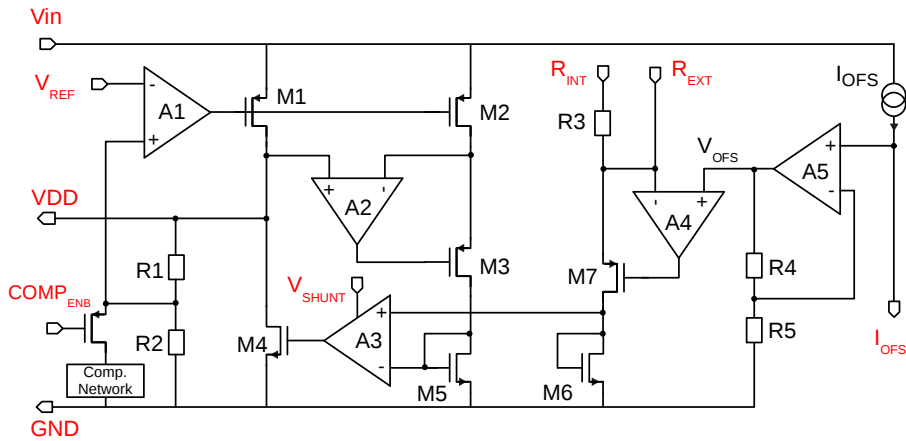
Figure 4.23: Shunt-LDO as integrated in RD53A. Input and output pads are marked in red. R_{shunt} can be either chosen as an internal resistor R_3 or an external resistor on the module flex PCB [39]

	0x074b		5 chip average		wafer probing	
	Analog	**Digital**	**Analog**	**Digital**	**Analog**	**Digital**
R_{eff}	$0.93\,\Omega$	$0.89\,\Omega$	$(0.95 \pm 0.04)\,\Omega$	$(0.93 \pm 0.05)\,\Omega$	$(0.86 \pm 0.03)\,\Omega$	$(0.87 \pm 0.02)\,\Omega$
V_{ofs}	$0.9\,\text{V}$	$0.92\,\text{V}$	$(0.93 \pm 0.02)\,\text{V}$	$(0.91 \pm 0.02)\,\text{V}$	$(0.95 \pm 0.04)\,\text{V}$	$(0.95 \pm 0.04)\,\text{V}$
V_{Rofs}	$0.94\,\text{V}$	$0.96\,\text{V}$	$(0.96 \pm 0.02)\,\text{V}$	$(0.97 \pm 0.02)\,\text{V}$	$-$	$-$
V_{DD}	$1.1\,\text{V}$	$1.16\,\text{V}$	$(1.15 \pm 0.07)\,\text{V}$	$(1.11 \pm 0.04)\,\text{V}$	$(1.11 \pm 0.17)\,\text{V}$	$(1.16 \pm 0.08)\,\text{V}$
$\frac{V_{\text{DD}}}{V_{\text{ref}}}$	2.024 ± 0.002	2.015 ± 0.004	2.009 ± 0.015	2.011 ± 0.003	1.996 ± 0.012	2.005 ± 0.010
$I_{\text{in, min}}$	$0.49\,\text{A}$	$0.41\,\text{A}$	$(0.49 \pm 0.09)\,\text{A}$	$(0.48 \pm 0.14)\,\text{A}$	$-$	$-$

Table 4.6: Shunt-LDO key figures from input IV measurement on RD53A 0x074B as well as average over 5 sample chips and results from wafer probing. V_{ofs} denotes the offset as per line fit on V_{in}. $I_{\text{in, min}}$ is the current for which the regulator saturates, i.e. the startup current. V_{DD} and V_{Rofs} denote the regulator output voltage and the voltage drop over R_{ofs} for $I_{\text{in}} = I_{\text{in, min}}$ respectively.

can be trimmed using a 5-bit on-chip register, which requires an established link between chip and DAQ. The regulator offset can not be trimmed as result of a trade-off between increased efficiency and robustness with respect to single event effect (SEE): implementing a trimming register for V_{ofs} could lead to abrupt changes in the Shunt-LDO working point. Such abrupt changes would disturb the current sharing between parallel Shunt-LDO, potentially leading to overload conditions in parts of the module and hence transients in the supply line of the serial chain.

The integration of the Shunt-LDO on RD53A has a few implications on operation of the regulator. The Shunt-LDO can not be operated without load anymore, as the RD53A can not be disconnected from the Shunt-LDO output. Furthermore the load current itself can not be accurately determined, as the load current is not accessible from outside the chip. This makes repeated performance studies of the proven Shunt-LDO design less feasible and shifts the focus towards operation of a RD53A using the Shunt-LDO. Compared to bench tests of Shunt-LDO prototype chips this makes additional considerations necessary, as the RD53A sets new boundary conditions for the Shunt-LDO operation. Upon supplying the chip with the target operating current, all reference voltages and currents need to be generated by the bandgap reference such that the Shunt-LDO can operate as intended. Both V_{DDA} and V_{DDD} need to be sufficiently large upon regulator startup to power analog and digital domains of the chip. With V_{DD} trimming implemented by on-chip registers, communication with RD53A needs to be established before V_{DD} can be trimmed to a target value.

In Figure 4.24 an example measurement of the input IV curves of the Shunt-LDO on an RD53A is displayed. In this example, both regulators are powered by separate power supply channels and do not share a common input current. Both regulators are configured for
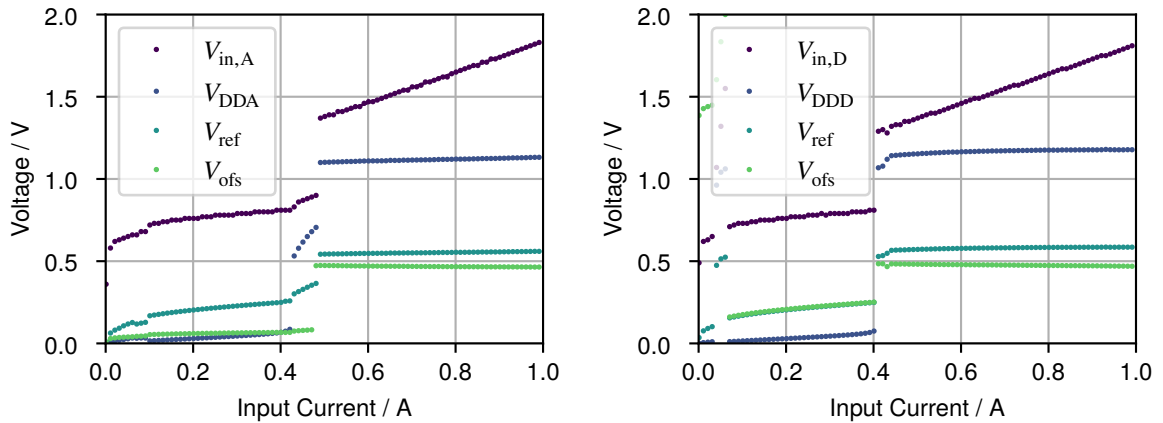
(a) Input IV curve of RD53A 0x074B, analog Shunt-LDO.

(b) Input IV curve of RD53A 0x074B, digital Shunt-LDO.

Figure 4.24: Input IV curve of RD53A 0x074B with parallel analog and digital Shunt-LDO. Each regulator is powered individually. V_{ofs} denotes the voltage drop over R_{ofs}.

an offset $V_{\mathrm{ofs}} = 1\,\mathrm{V}$ and loaded with $R_{\mathrm{ext}} = 806\,\Omega$, implying an effective Shunt-LDO input impedance of $R_{\mathrm{eff}} = 0.806\,\Omega$ for a k-factor of 1000. The measured V_{ofs} is the voltage drop over R_{ofs} and fed into A_5 in Figure 4.23. The effective offset of the Shunt-LDO is to first order $2 \cdot V_{\mathrm{ofs}}$. From the shown measurement several key points for the operation of RD53A can be taken. Most importantly these cover the working point of the RD53A by means of R_{eff} and V_{ofs}, the minimum working point $I_{\mathrm{in,\,min}}$ to reach regulator saturation and the regulator output voltage V_{DD} at this working point. Due to the initial limited availability of RD53A, these measurements were limited to a sample of 5 chips with working Shunt-LDO. Only with the later finalized wafer probing procedures most of these figures could be tracked for a large number of RD53A chips [20]. In Table 4.6 an overview of these figures is given for the example chip presented here, the average of the 5 chip sample as well as the corresponding averages from wafer probing. Notably the 5 chip sample does not represent the collective wafer probing data very well. As a small sample compared to the ≈ 9000 RD53A tested in wafer probing this is not unexpected. Comparing the behaviour of V_{in} to Figure 4.13(a), the late startup of the regulator in RD53A becomes clearly visible. This is a consequence of the current source driving I_{ofs} being powered by the bandgap reference, which in turn depends on the regulator output. Once V_{ofs} saturates, the regulator shows the known linear behaviour. In some cases the required current to reach the linear regime of the Shunt-LDO is *larger* than the targeted working point for both digital and analog Shunt-LDO. From chip to chip, the required startup current varies significantly and is additionally sensitive to the chip temperature as can be seen in Figure 4.25: at lower temperature, startup occurs generally

(a) Analog Shunt-LDO.

(b) Digital Shunt-LDO.
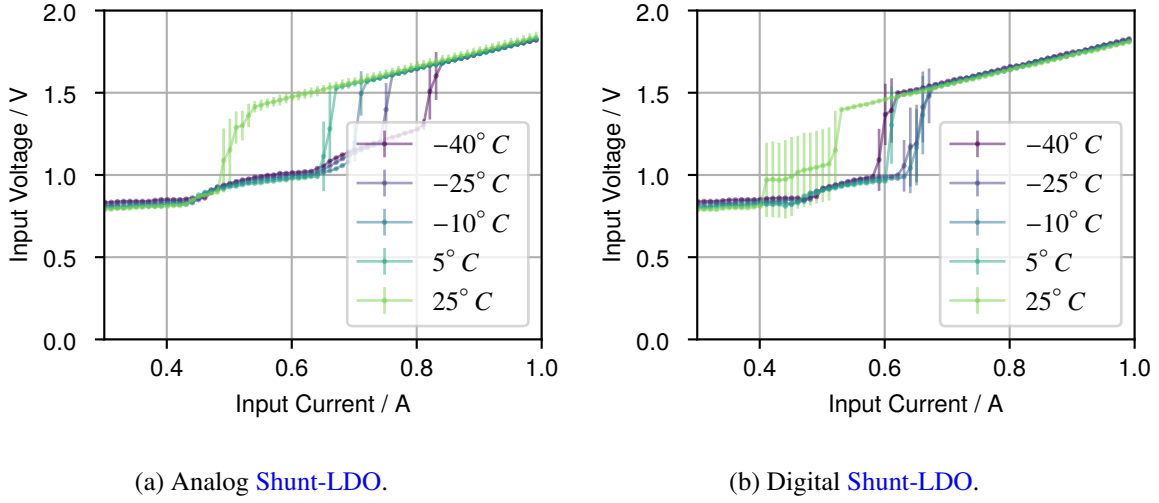
Figure 4.25: Input IV curve of RD53A 0x074B at differing temperatures in a climate chamber, averaged over 10 measurements. Errors denote the standard deviation of the measurement set.

later, i.e. at higher I_{in}. For the example chip 0x074B this is particularly visible for the analog Shunt-LDO, startups of the digital Shunt-LDO are less separated. Startup of the regulator occurs immediately once any current is supplied to the chip, if V_{ofs} is provided by an external power source. The late startup of some Shunt-LDO became clearly visible during initial wafer probing, where for many Shunt-LDO only few measurement points in saturation are available [20]. Once the regulator startup is achieved, the regulator remains in saturation even if I_{in} is lowered, as long as no overload occurs. This is beneficial when considering multiple parallel Shunt-LDO e.g. on a multichip module. Here, a regulator not in saturation has an effectively lower impedance compared to a saturated regulator, thus drawing more current share from the total supply current. This unbalanced current sharing helps starting up all regulators, while no regulator will drop out of saturation once reached unless the total supply current cannot supply all involved loads.

Once the Shunt-LDO is saturated more features become apparent. Firstly, the voltage drop measured over R_{ofs}, expected to be $500\,\text{mV} \approx 249\,\text{k}\Omega \cdot 2\,\mu\text{A}$, is lower than expected. With R_{ofs} well known this indicates the offset generating current to be smaller than expected, in the presented case $1.93\,\mu\text{A}$ and $1.97\,\mu\text{A}$ respectively. Additionally the offset voltage generated by I_{ofs} is slightly larger than the effective offset obtained by the fit on V_{in}. The results obtained from the available sample is consistent with the results obtained during RD53A wafer probing and shows a generally too small V_{ofs} in RD53A. Similarly, the observed R_{eff} does not match with the expected $R_{eff,\,exp} = 0.806\,\Omega$. Similar to the 2 A prototype chip, this is due to a mismatch in the Shunt-LDO k-factor. To verify this, the k-factor of the Shunt-LDO has been measured on RD53A. Following the same procedure as outlined in Section 4.1.2, the
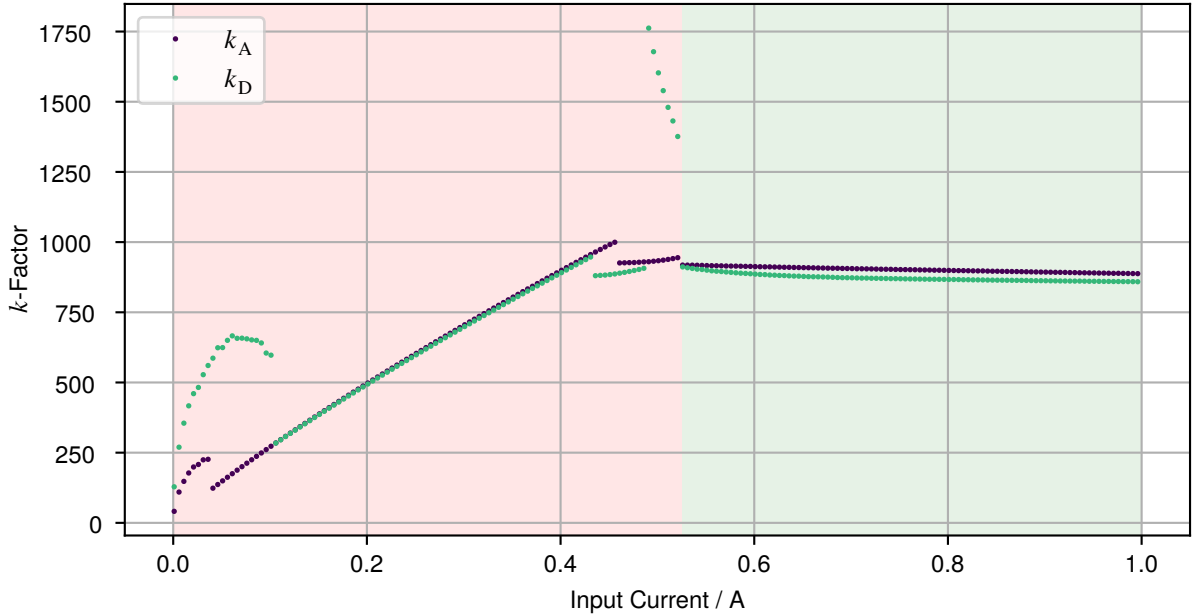
Figure 4.26: Measurement of the k-factor of analog and digital Shunt-LDO on an RD53A. The unsaturated operation region is shaded in red, while saturated operation is marked in green.

Shunt-LDO reference current was measured as voltage drop over R_{ext}. Being an external SMD resistor, the value of R_{ext} is well known as $806\,\Omega$ with a precision of $0.1\,\%$. Additional contributions, e.g. trace impedance or soldering contacts, can be neglected as they are typically of the order of $0.1\,\Omega$. The then measured reference current is then compared to the input current supplied to the Shunt-LDO and gives an upper estimate for the k-factor assuming the Shunt-LDO has a negligible leakage current:

$$I_{ctrl} = \frac{I_{in} - I_{bias}}{k + 2} \approx \frac{I_{in}}{k}. \tag{4.7}$$

The result of such a measurement is shown in Figure 4.26. Neglecting the behaviour of the unsaturated regulator, a dependency $k(I_{in})$ can be noted, which can be approximated as linear in first order with an average slope of $-75\,A^{-1}$. In Table 4.7 the results of such a k-factor measurement are listed for the chip used in Figure 4.26 as well as the average of the available 5 chip sample. Given are the the minimum and maximum value of k as well as the slope of k in the saturation region as shown in Figure 4.26. Additionally an expected range for R_{eff} using the obtained k-factors is given. This range for R_{eff} is in sufficient agreement with the measured R_{eff} in Table 4.6. From wafer probing data k can only be estimated using the effective R_{eff} obtained from the input IV curve. The distribution of the measured R_{eff} shown

	0x074B		5 chip mean	
	Analog	**Digital**	**Analog**	**Digital**
k_{min}	888	859	884 ± 10	865 ± 11
k_{max}	918	909	952 ± 42	894 ± 15
k-factor, slope	$-65\,\mathrm{A}^{-1}$	$-84\,\mathrm{A}^{-1}$	$(-103 \pm 44)\,\mathrm{A}^{-1}$	$(-67 \pm 20)\,\mathrm{A}^{-1}$
R_{eff} range / Ω	$(0.90 \pm 0.02)\,\Omega$	$(0.92 \pm 0.03)\,\Omega$	$(0.87 \pm 0.05)\,\Omega$	$(0.91 \pm 0.03)\,\Omega$

Table 4.7: Shunt-LDO k-factor upper estimate based on Equation 4.7 measured on RD53A, averaged over 5 chips. Only saturated operation of the Shunt-LDO is considered. k_{min} and k_{max} refer to the lowest and highest value for k in the saturation region of Figure 4.26 respectively.

in Figure A.3 [20] support the observation of a mismatched k-factor in RD53A on a larger scale.

As a final point of observation, the output voltages V_{DD} have to be considered. The line regulation of the Shunt-LDO itself is very good with only a few $\mathrm{mV\,A}^{-1}$, as has been shown with the prototype chips. On RD53A however the line regulation performance is significantly worse. In the measurement shown in Figure 4.24, the line regulation performance in comparison is decreased by a factor of 3. This is driven by the dependency of the bandgap reference output voltage on I_{in}. This dependency causes a slope of $0.03\,\mathrm{V\,A}^{-1}$ on V_{ref}, which already exceeds the line regulation of the 2 A prototype chip. If V_{ref} is provided by an external power supply, the line regulation of RD53A is again in good agreement with the prototypes investigated before, however this is not a realistic scenario. In addition, the default values for V_{DD} upon Shunt-LDO startup are very low. As was confirmed also from wafer probing, average values for V_{DDA} and V_{DDD} are 1.1 V and 1.16 V respectively. The digital domain of RD53A does require a supply voltage $V_{DDD} \geq 0.9\,\mathrm{V}$ to provide full digital functionality, including data transmission and register operations like trimming of V_{ref}. Thus the smaller value for V_{DDD} is of no concern. For V_{DDA} the situation is different, as the clock and data recovery (CDR) [47], which is powered by V_{DDA}, has been shown to require $V_{DDA} \geq 1.15\,\mathrm{V}$ to reliably lock onto an incoming command signal. Without a successful lock, communication with the chip is not possible, which includes writing of V_{ref} trimming registers. As a preliminary solution, most RD53A are fitted with a pull-up resistor between V_{refA} and V_{DDA}. With a typical size of $150\,\mathrm{k\Omega}$, this leads to a typical increase of 100 mV for V_{DDA}.

With the pull-up resistor in place, operation of the RD53A with active Shunt-LDO is generally possible without any issues or impact on performance, as will be shown in Section

5.2. However the characteristics discussed here have implications for multi-chip modules, which are the basic building block of the future ITk pixel detector. Parasitics in the circuitry cause the working point of the individual Shunt-LDO to shift away to larger R_{eff} and smaller V_{ofs}. As the working point needs to be carefully chosen to provide an optimal trade-off between robustness of the multi-chip module and power efficiency and is further constrained by boundary conditions, e.g. the available local cooling power, optimisation is necessary. The late startup point of the bandgap reference generally leads to large current sharing imbalances for parts of the possible operation region and need to be addressed. Furthermore the bandgap reference needs to provide a more narrow distribution of output voltages to reduce the width of the distributions of V_{ofs} and V_{DD}. In an attempt to address these issues, the design of the Shunt-LDO has been overhauled for RD53B and expanded by several crucial features which will be covered in Section 4.3

4.3 An Updated Shunt-LDO Design for RD53B

Characterisation of the Shunt-LDO in RD53A and operation of RD53A chips in serial powering configurations have revealed points of concern in the Shunt-LDO design. While the general performance of the regulator was deemed sufficient, the implementation of the Shunt-LDO in RD53A was not without issues as has been discussed in Section 4.2.1. These feature most prominently the bandgap reference in RD53A, which did not perform up to expectation. With the continued development of the ITk pixel detector design, further requirements were raised for the Shunt-LDO: As a dedicated bypass chip to protect modules from voltage transients on the LV line was dropped from the design, the Shunt-LDO needs to be expanded by a protection mechanism against current transients on its input. This is achieved by the addition of a voltage clamp parallel to the Shunt-LDO, the over voltage protection (OVP). During large scale serial powering system tests with FE-I4 pixel modules it became clear that a typical source of these transients are overload conditions of the Shunt-LDO. A dedicated protection mechanism was added to the Shunt-LDO to mitigate the effects of Shunt-LDO overloads on the module, the Under-shunt current protection (UCP). During the production phase of the ITk pixel detector, it will become necessary to test pixel modules already loaded on their local support structure with no or very limited active cooling available. Considering the lightweight nature of these support structures, operation of a multi-chip module at nominal power would lead to unacceptable heat generation, thus an option for low power operation of both the ROC and the Shunt-LDO was foreseen. A new prototype chip campaign was launched to verify the newly added features in terms of general performance and radiation hardness. The campaign spanned over 3 prototype chips, which are referred to as RD53B Shunt-LDO test chip A, B and C. Between the first two iterations, all new features

were implemented in the Shunt-LDO prototype:

- **Test chip A** includes the revised bandgap scheme and the UCP to mitigate effects from Shunt-LDO overload.

- **Test chip B** expands on test chip A with an auxiliary startup circuit, a voltage clamp OVP and integrates a low power mode (LPM) for low power operation. As an improvement upon test chip A external resistors are used for reference current and voltage generation to provide better radiation hardness and temperature stability.

- **Test chip C** includes minor modifications to the bandgap scheme and startup circuit to improve Shunt-LDO stability.

In the context of this thesis, the main focus was put on test chip B as the first prototype with all new features implemented. This prototype was characterized in depth, including an irradiation campaign to a TID of 800 Mrad as a bachelor thesis supervised within this work [48]. Test chip C is not a focus of the efforts presented here. This is partly due to a design bug in test chip C, which was expected to negatively impair the radiation hardness of the offset generating circuitry. This bug introduced parasitic current paths in the offset generation, which were expected to be dependent on the chip temperature and thus I_{in}.

Revised Bandgap Scheme, Reference Generation and Startup Circuit

In a serial powering chain, each Shunt-LDO must become operational immediately once any significant supply current is provided and be reliable over wide temperature ranges from room temperature down to temperatures of −40 °C. In RD53A, neither was satisfied sufficiently. In the RD53B implementation, a bandgap reference scheme without the circular dependencies present in RD53A was realised. In Figure 4.27 the bandgap reference schematic for a full RD53B pixel chip is shown. This scheme is fundamentally different from RD53A, as no Shunt-LDO output is used to supply any reference. Instead, a new linear regulator, the *Pre-Regulator* is connected in parallel to the Shunt-LDO. The pre-regulator draws its reference voltage from a low precision, 2 V tolerant bandgap[2], making no adjustments to the input voltage safety limits necessary. The pre-regulator output V_{DDPre} then supplies a high-precision core bandgap which generates the main reference current I_{ref} using an external SMD resistor, as external resistors are less susceptible to self heating of the Shunt-LDO and available in higher precision and radiation hardness. I_{ref} can be trimmed to account for process variations and equalize I_{ref} between different chips. The main reference current is then mirrored and used to generate all reference voltages V_{ref} and V_{ofs} using dedicated, external

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[2] A 2 V-tolerant bandgap with enough steering precision for this application is not achievable [35].
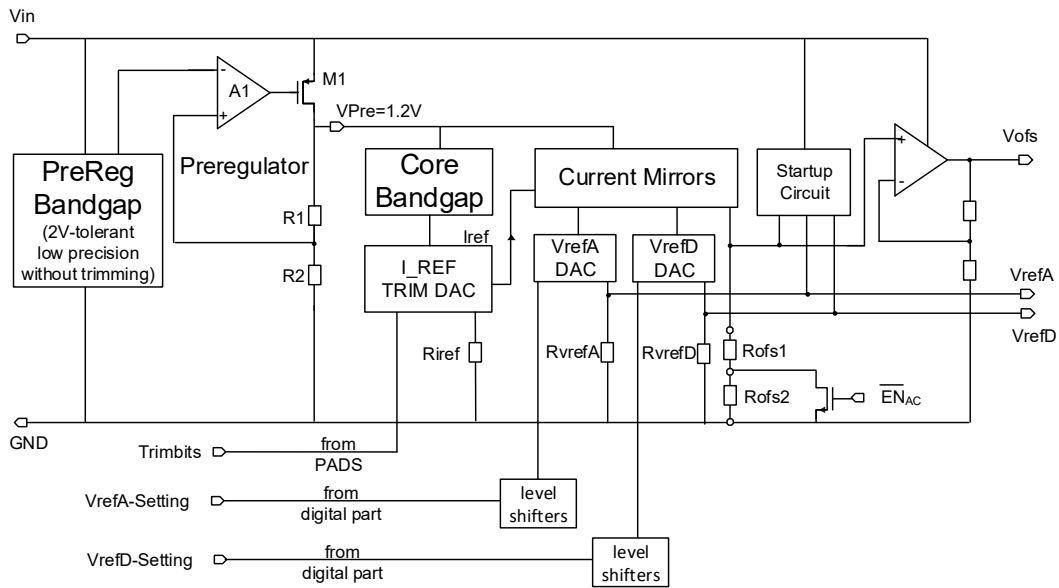
Figure 4.27: Bandgap reference scheme used in the RD53B Shunt-LDO. Shown is the scheme for a full RD53B ROC including startup circuit and LPM switch [35].

resistors R_{VrefA}, R_{VrefD}, R_{ofs}. Similar to RD53A, V_{ref} can be trimmed, as the regulator output has no effect on the IV characteristics of the Shunt-LDO. Just as in RD53A V_{ofs} can not be trimmed, as sudden changes in V_{ofs} would be an issue in serial operation. The pre-regulator itself draws very little current such that its effect on the Shunt-LDO IV characteristics can be neglected. Without the circular connections present in RD53A the offset voltage V_{ofs} requires
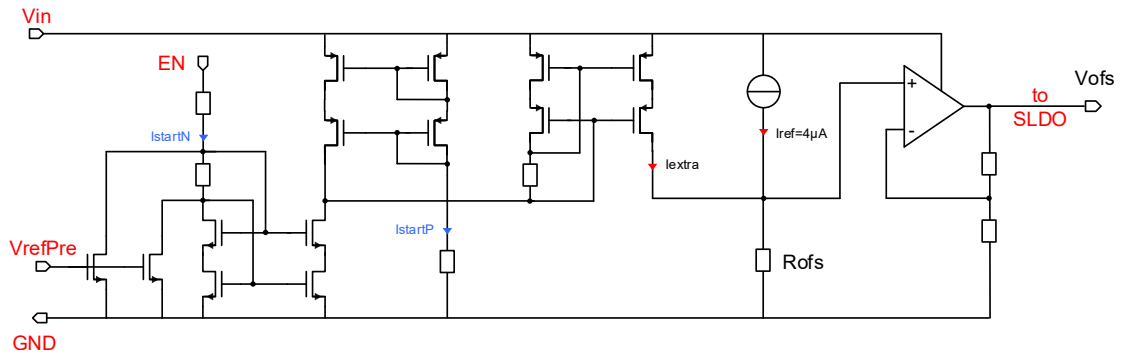
Figure 4.28: V_{ofs} startup circuit in RD53B, taken from [42].

a dedicated startup circuit, especially when considering LPM operation of the Shunt-LDO. This is due to a low offset causing the shunt transistor M_4 in Figure 3.7 to be fully open, which clamps V_{in} to low values even for high currents. The chosen solution, shown in Figure 4.28, is designed to boost V_{ofs} close to the value of V_{in} until a large enough V_{in} is available to operate the pre-regulator by injecting additional current in R_{ofs}. Once the pre-regulator reference

V_{refPre} is large enough, this injection is shut off.

A notable difference in Figure 4.27 compared to the offset generation in RD53A is the presence of two external resistors, R_{Ofs1} and R_{Ofs2}, with a center tap switch in RD53B, effectively acting as a 1-bit variable resistor. The switch, which is internal to the Shunt-LDO, in practice implements a LPM for the regulator as shown in Figure 4.29. In normal operation the switch is closed, bypassing the second resistor R_{OfsL}. Thus V_{ofs} is only generated as the voltage drop over $R_{\text{ofs}} = R_{\text{Ofs,H}}$. If the switch is opened, R_{ofs} becomes $R_{\text{OfsH}} + R_{\text{OfsL}}$, leading to a larger total V_{ofs} as I_{ref} does not change. In this state a much smaller current can be sufficient to achieve a working point $V_{\text{in}} \geq 1.4\,\text{V}$, allowing the regulator outputs to exceed 1.2 V.

Such a LPM requires the power-up or default configuration of a ROC to draw very little power to avoid immediate regulator overload, which is the case for both ITkPix and CROC. The switch itself can be controlled by a dedicated AC signal called LP_{En}. An AC signal was chosen to steer the switch, as in a serial chain either all modules are to be operated in LPM or none. Thus all modules are steered by the same signal, which needs to be AC coupled to avoid unwanted current paths. This signal is input into a rectification circuit, converting it into a logic level which is then

Figure 4.29: Schematic view of the LPM switch in RD53B [35].

applied to the switching transistor. If no signal is present, or amplitude or frequency of the AC signal are too low, the switch stays closed, leaving the Shunt-LDO in high power operation. Testing yielded a required AC frequency $\geq 10\,\text{kHz}$ for a rectangular voltage pulse with an amplitude of $\approx 1\,\text{V}$ at the input for the test chip. The resulting voltage drop V_{ROfs} then corresponds to half the offset voltage $V_{\text{Ofs,Half}}$ and is multiplied by two before being fed into the Shunt-LDO, see also A_4 in Figure 3.7. This is necessary as V_{ofs}, especially in LPM operation, can exceed the pre-regulator output voltage V_{DDPre}.

Undershunt Current Protection

The variable shunt current I_{shunt} through M_4 in Figure 3.7 serves to keep the total current $I_{\text{in}} = I_{\text{shunt}} + I_{\text{load}}$ flowing through the regulator constant, which is a fundamental condition for serial chain operation. As has been seen in e.g. Section 4.1.1, the situation changes once I_{load} approaches I_{in}. In this situation the shunt current approaches 0 A and the regulator input voltage V_{in} drops sharply, similar to a short circuit failure. On a multi-chip module with multiple parallel regulator this can impair the operation of all chips on the module: If a single regulator becomes low-ohmic as described, it will draw additional current from
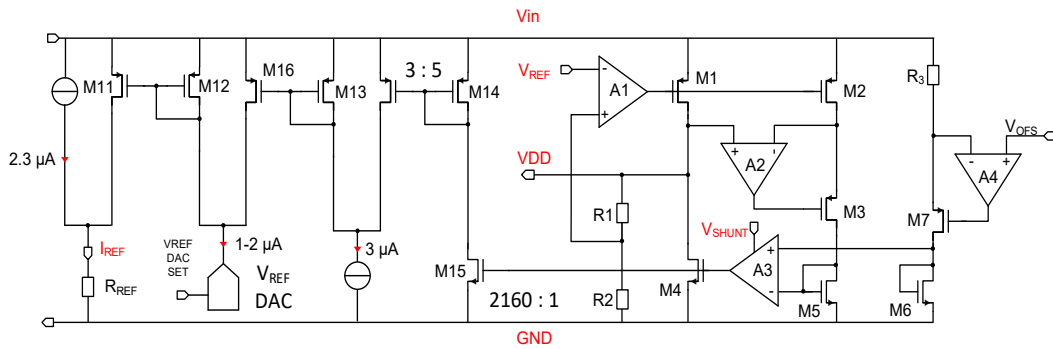
Figure 4.30: Schematic of the Shunt-LDO with additional UCP circuit taken from [42].

the neighbouring regulators. If the impedance of a single Shunt-LDO decreases drastically, this can drive more chips into an overloaded state and prevent the module from functioning properly, e.g. leading to oscillations in the current sharing on a module. There are several possible causes for such a behaviour. One is an insufficient margin in the module supply current which can not account for the imperfect current balancing between regulators. During operation itself, various fault conditions can cause excessive I_{load} drawn from the Shunt-LDO, e.g. hardware failures due to radiation damage and electromigration as well as temporary effects like SEE or bad configurations sent to the chip. To mitigate the effects of an overload condition on the Shunt-LDO, the UCP has been added to the regulator. The schematic of the RD53B Shunt-LDO with the added UCP is shown in Figure 4.30. This UCP operates by comparing the current I_{shunt} flowing through M_4, via the current mirror M_4:M_{15}, to a reference current. Once I_{shunt} is below the threshold defined by the UCP, the reference voltage V_{ref} of the Shunt-LDO is lowered, which leads to less current drawn by the load. However, V_{ref} can not be lowered below a threshold of 0.35 V. As the pass device is not cascoded to improve Shunt-LDO efficiency by minimizing the dropout voltage, the voltage drop over M_1 is limited to 1.32 V. Larger voltage drop can permanently damage M_1. V_{in} is allowed to reach up to 2 V during operation. The voltage drop over M_1 is given as $V_{in} - V_{out}$, thus a lower limit of 700 mV was set for V_{out} [42].

The UCP implemented as described effectively makes internal shorts in the chip invisible as long as the effective remaining impedance of the load is greater than 0.7 V/I_{in}. A failure mode with a lower effective impedance would require V_{ref} to be reduced further and, since this is not possible, lead to a collapse in V_{in} after all. A possible undesired consequence of using this UCP are oscillations in V_{out} of the regulator. If a condition causing a Shunt-LDO overload disappears once V_{ref} is lowered, the V_{ref} will recover again to its target value. Should the overload condition still be present once V_{ref} is raised again, the regulator will oscillate. For the affected chip this is obviously problematic, as it can not be operated properly. For neighbouring chips however this poses no problem, as V_{in} of the chip with internal oscillations
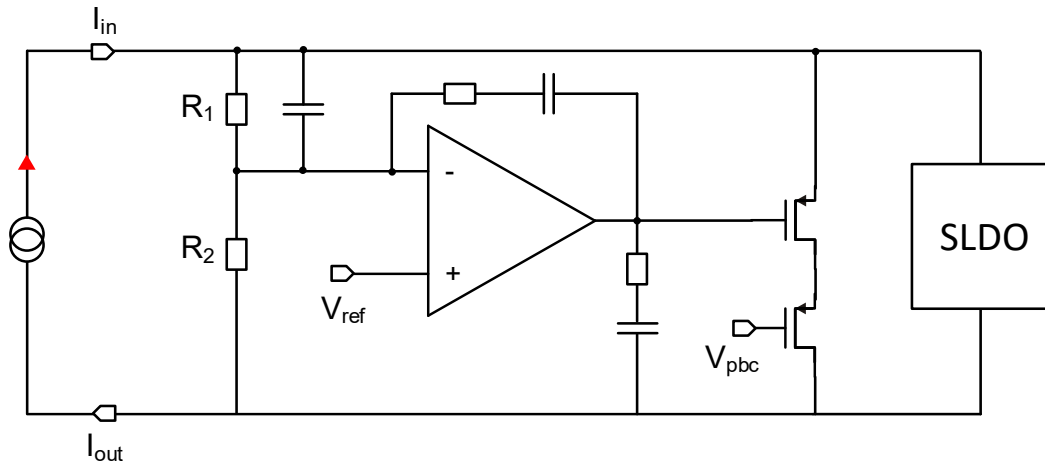
Figure 4.31: OVP with current clamp as implemented for the RD53BShunt-LDO. Taken from [42]

would stay constant. Without UCP V_{in} itself would oscillate, which would seriously affect neighbouring chips and potentially could damage other modules in the serial chain by causing voltage transients on the LV line.

Over Voltage Protection

To protect against voltage transients in V_{in} exceeding 2 V, an OVP as shown in Figure 4.31 is added to the Shunt-LDO. The total ability of the regulator to draw current is limited by the pass device M_1 in Figure 3.7, no current above this limit can be shunted by the regulator. Thus the implemented OVP contains a current clamp in parallel to the Shunt-LDO.

The OVP needs to become active if V_{in} is close to 2 V. The threshold of the clamp is defined by V_{refOVP} as $V_{OVP} \approx N_{OVP} \cdot V_{refOVP}$, with the design scaling factor $N_{OVP} = 3.33$. As a reference for the OVP an internal copy of the pre-regulator reference voltage V_{refPre} is used, which is around 0.6 V, resulting in a threshold voltage $V_{OVP} \approx 2$ V. In addition it is possible to override the OVP reference with an externally provided voltage. Since V_{in} is common for both Shunt-LDO on a ROC, only one OVP is implemented per ROC. Since no balancing mechanism is implemented, any overvoltage on a multi-chip module will cause the chip with the lowest effective V_{OVP} to clamp most of the current. For a static overload this could lead to damage to the Shunt-LDO by excessive current. Such a static overload could e.g. be caused by high-ohmic failures of multiple Shunt-LDO on a multi-chip module and can ultimately lead to loss of the full serial chain. However this is a hypothetical scenario as such a failure has yet to be observed.

4.3.1 Characterisation of the new Shunt-LDO Prototype

For characterisation the RD53B Shunt-LDO test chip B was mounted on a dedicated test PCB as shown in Figure 4.32. It offers the core functionality known from the test PCB for the 500 mA and 2 A prototype chips. Improving over the previous design, each monitoring pin is equipped with its own connections to either the PCB GND or the Shunt-LDO GND potential. Dedicated sense points for sensing of V_{in}, I_{in}, V_{out} and I_{out} are available. The external resistors to set V_{ref} and V_{ofs} as well as the slope resistor R_{shunt} are available as variable resistors, the reference current is set by the fixed precision resistor R_{Iref}. A negative temperature coefficient resistor (NTC) monitors the temperature of the cooling backplate of the PCB, to which a heatsink can be attached. V_{ref} and I_{ref} can be trimmed to their target values using jumpers.

Similar to the previous prototypes, a power transistor is placed parallel to the V_{out} measurement path to simulate load transients. The working point of the Shunt-LDO prototype chip was chosen to be the same working point as for the RD53A Shunt-LDO in Section 4.2.1: The slope resistor R_{shunt} was chosen to achieve $R_{\text{eff}} = 0.806\,\Omega$ with an offset of 1 V. For centered V_{ref} trim bits, the reference voltage was set by fine tuning of R_{Vref}. As the variable resistors used for trimming of V_{ofs} and V_{ref} are very sensitive mechanically, the trimming precision was limited to $\Delta V \approx 20\,\text{mV}$. Due to a production error the OVP reference voltage was wrongly connected to the pre-regulator bandgap output voltage, which is only approximately 500 mV, instead of the pre-regulator reference voltage V_{refPre}. As this would clamp V_{in} earlier than intended, most measure-

Figure 4.32: PCB designed and provided by FH-Dortmund, loaded with a RD53B Shunt-LDO test chip B.

ments used an externally provided V_{refOVP}. All measured voltages are obtained via the dedicated sense pads, referenced to I_{out} instead of the PCB GND. A summary of the obtained results is given in Table 4.8.

An example input IV curve is shown in Figure 4.33. I_{ref} is monitored as the voltage drop over the I_{ref} generating resistor R_{Iref}. With $R_{\text{Iref}} = 150\,\text{k}\Omega$ and a target $I_{\text{ref}} = 4\,\mu\text{A}$ the voltage drop over R_{Iref} is expected as 0.6 V, which is equal to V_{ref}. During the shown measurement all voltages except the OVP reference voltage are derived from the bandgap reference, which is different from previous prototype chips like the 2 A prototype.

Compared to Figure 4.24 the much improved start up characteristic is clearly visible. The

Line- and load regulation results of RD53B Shunt-LDO test chip B	
R_{eff}	$0.93\,\Omega$
V_{ofs}	$0.98\,\text{V}$
$\dfrac{V_{\text{out}}}{V_{\text{ref}}}$	2.02 ± 0.01
Line regulation	$0.02\,\text{V\,A}^{-1}$
OVP reference multiplier	3.36 ± 0.02
Load regulation	$0.004\,\text{V\,A}^{-1}$
UCP threshold	$I_{\text{shunt}} \leq 0.01\,\text{A}$
I_{ref} slope	$0.045\,\mu\text{A\,A}^{-1}$

Table 4.8: Overview of results from the RD53B Shunt-LDO test chip B.
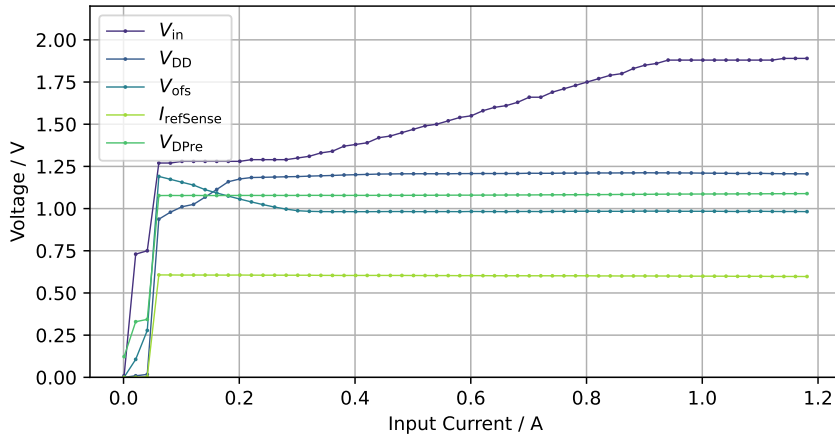
Figure 4.33: Full input IV curve measured with an RD53B Shunt-LDO test chip B. I_{ref} is measured as a voltage drop across a $150\,\text{k}\Omega$ resistor.

effect of the startup circuitry introduced in Section 4.3 can be seen in V_{ofs}: for small I_{in}, V_{ofs} follows V_{in} and increases beyond its target value. Once V_{in} exceeds the target V_{ofs}, the startup circuit injects increasingly less current into R_{ofs}, lowering V_{ofs}. In this range of I_{in}, V_{in} remains constant while V_{ofs} decreases linearly. Once the startup circuit switches off the linear characteristic of the Shunt-LDO shows on V_{in}. During this startup process V_{ofs} exceeds V_{DDPre}, which is only possible due to the pre-regulator only generating $V_{\text{Ofs,Half}}$. Subtracting V_{ofs} from the measured V_{in} yields the expected linear behaviour over the full measurement range as can be seen in Figure 4.34. When correcting V_{in} by V_{ofs}, the extracted R_{eff} can vary based on the slope of V_{ofs} itself. In the case of the measurement shown here V_{ofs} increases over the full measurement range with a slope of $0.005\,\text{V}\,\text{A}^{-1}$, which has only a negligible effect on R_{eff}.
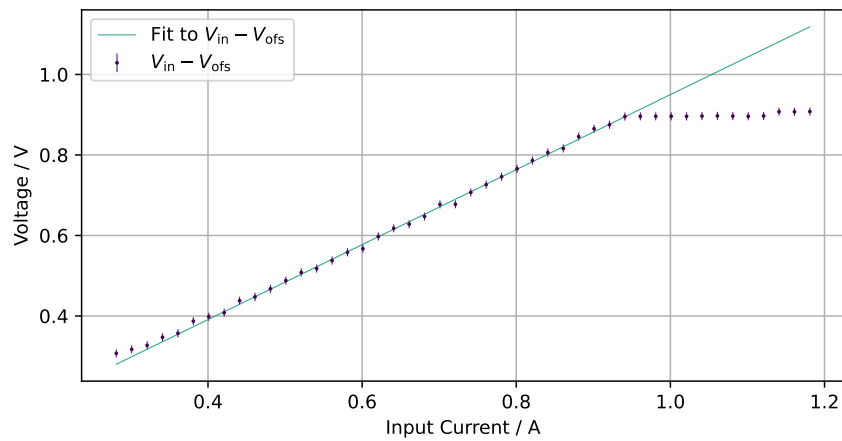
Figure 4.34: Input IV curve of the RD53B Shunt-LDO. V_{in} is corrected by V_{ofs} to account for the varying V_{ofs} due to the startup circuit.

The offset voltage extracted from the fit on the corrected V_{in} is listed in Table 4.8 and is in good agreement with the a direct measurement using the V_{ofs} sensing pin on the PCB, yielding $V_{\text{ofs}} = 0.979\,\text{V}$. The resulting slope of V_{in} in Table 4.8 does not match the expected input impedance given as $\frac{R_{\text{shunt}}}{k}$. This is expected as the current mirror ratio k is known to be smaller than the targeted $1000:1$ ratio from previous measurement campaigns.

For the RD53B Shunt-LDO test chip B the k-factor was measured using different strategies in [48] and is shown in Figure 4.35. For a range of different values for R_{shunt}, the input IV curve of the Shunt-LDO was measured. The k-factor was obtained by comparing the current flow through R_{shunt}, I_{ctrl}, to the input current. This was done both at specific working points as well as over the full range I_{in}. As a comparison the ratio $\frac{R_{\text{eff}}}{R_{\text{shunt}}} \approx k$ is given. The measurements relying on the measurement of I_{ctrl} are mostly in good agreement. The ratio $\frac{R_{\text{eff}}}{R_{\text{shunt}}}$ however shows a strong dependency on R_{shunt}, as the resulting k depends on the choice
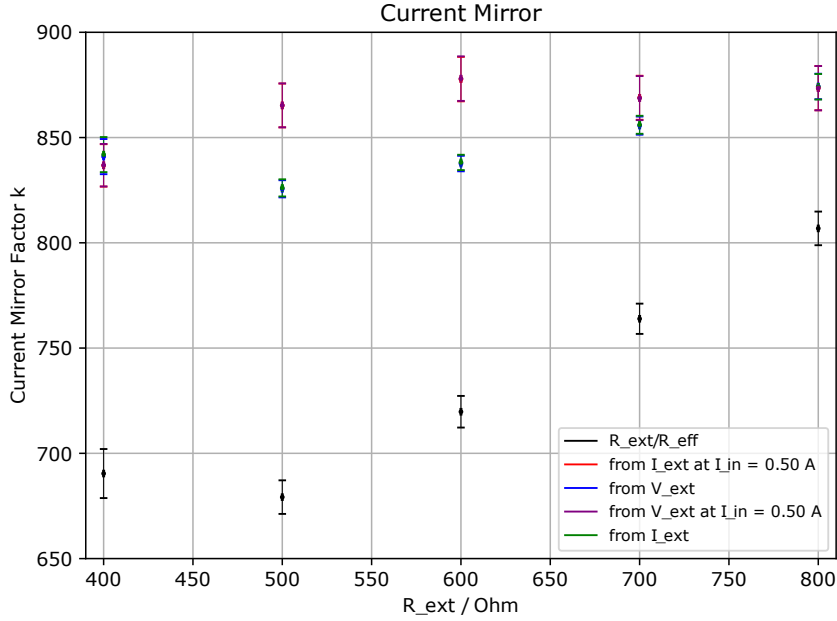
Figure 4.35: Measurement of the RD53B Shunt-LDO test chip B current mirror ratio k [48].

of R_{shunt}, which is unexpected. As expected from previous prototype chips and RD53A, the resulting average $k \approx 870 \pm 10$ is below the target value. Followup investigations revealed the cause of the k-factor mismatch to be an impedance mismatch in the current paths towards M_1 and M_2 in Figure 4.23. This leads to a different effective potential applied at the source of M_1 and M_2 respectively, shifting the resulting current mirror ratio. Subsequently this design bug was fixed for the Shunt-LDO implementation in ITkPix and CROC.

The main reference I_{ref} is sufficiently stable for the full operation range as can be seen from Table 4.8. For a operation range of 1 A for I_{in} this corresponds to a change in the order of 1 % in I_{ref}. As a comparison, the LSB step size of the I_{ref} trim bits is almost twice as large with approximately $0.08\,\mu\mathrm{A}$. The line regulation and output steering precision listed in Table 4.8 are in good agreement with the previous measurements done on RD53A and the predecessor prototype chips. The line regulation is mostly driven by a change in V_{ref} over the measurement range, $\Delta V_{\mathrm{ref}} \approx 0.04\,\mathrm{V\,A^{-1}}$.

For high I_{in} in Figure 4.33, V_{in} is seen to reach a plateau. This is due to V_{in} exceeding the threshold voltage of the Shunt-LDO OVP circuit. With a reference voltage $V_{\mathrm{refOVP}} = 0.55\,\mathrm{V}$ as applied during the measurement and a design scaling factor of $N_{\mathrm{OVP}} = 3.33$ of the OVP, the threshold voltage is expected to be $V_{\mathrm{OVP}} \approx 1.84\,\mathrm{V}$. To test the scaling factor N_{OVP}, the input IV curve is measured for different applied V_{refOVP}. As additional reference the input for V_{refOVP} on the PCB is connected to the regulator reference V_{ref}. Such a measurement is shown in Figure 4.36 and the calculation of the corresponding scaling factor N_{OVP} is
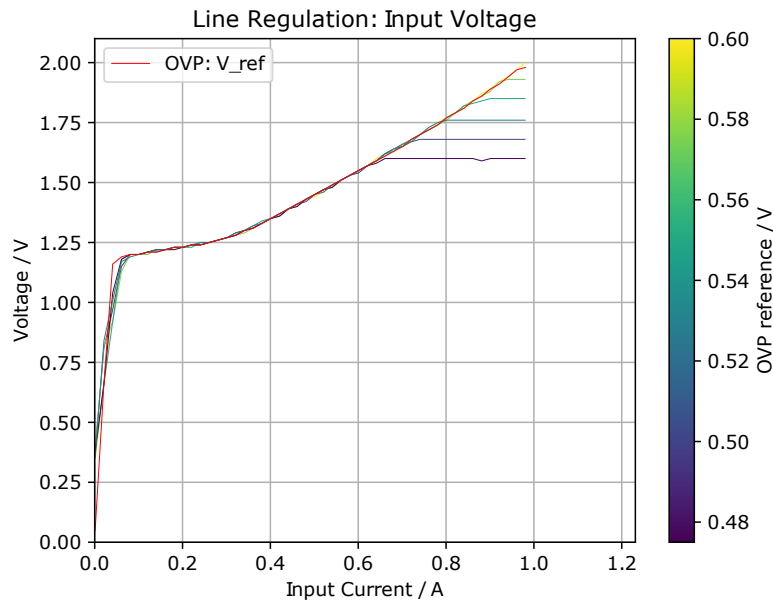
Figure 4.36: Input IV for different V_{refOVP}. The red curve results from connecting V_{refOVP} directly to V_{ref}. Taken from [48].

listed in Table 4.9. The mean N_{OVP}, also listed in Table 4.8, is slightly exceeding the target value $N_{\text{OVP,target}} = 3.33$, however the difference is acceptable for the application. With the given factor the OVP threshold given by a reference voltage $V_{\text{refOVP}} = 0.6\,\text{V}$ follows as $V_{\text{OVP}} = 2.02\,\text{V}$. Considering the actual voltage tolerance of the Shunt-LDO circuit will be slightly larger than 2 V since there is some safety margin included, this threshold is considered sufficiently close to the ideal case $V_{\text{OVP}} = 2\,\text{V}$. With the exception of V_{in}, V_{refOVP} has shown no impact on the Shunt-LDO during normal operation.

Similar to the line regulation measurement, an example of a load regulation measurement is shown in Figure 4.37. This measurement was performed with the UCP switched on. The working point was chosen as $I_{\text{in}} = 0.6\,\text{A}$. The general behaviour is very similar to the observations made with the previous prototype chips with an good load regulation, listed in Table 4.8, which is largely dominated by a change in V_{ref} by $(0.004 \pm 0.001)\,\text{V A}^{-1}$. This did not contribute to the 500 mA - and 2 A prototype chips, as all reference voltages for these chips were provided by an external power supply. Once I_{load} approaches I_{in}, the UCP is shown to work by reducing the available V_{ref} and thus V_{DD}. However V_{in} stays nearly constant as intended. With no UCP active, the behaviour is more reminiscent of the previous prototype chips with a collapse of all Shunt-LDO voltages. From load regulation measurements without active UCP the minimum difference $I_{\text{shunt}} = I_{\text{in}} - I_{\text{load}}$ required for the Shunt-LDO to operate can be extracted to be of the order of 10 mA, giving a lower limit for feasible UCP activation

V_{refOVP} / V	V_{OVP} / V	N_{OVP}
0.475 ± 0.001	1.6 ± 0.01	3.368 ± 0.023
0.500 ± 0.001	1.68 ± 0.01	3.360 ± 0.022
0.525 ± 0.001	1.76 ± 0.01	3.352 ± 0.020
0.550 ± 0.001	1.85 ± 0.01	3.364 ± 0.020
0.575 ± 0.001	1.93 ± 0.01	3.356 ± 0.019
0.600 ± 0.001	≥ 2	–

Table 4.9: Measurement of OVP scaling factor N_{OVP} [48]. For OVP threshold voltages above 2 V no scaling factor was obtained, as the power supply was limited to an output voltage of 2 V to protect the regulator.
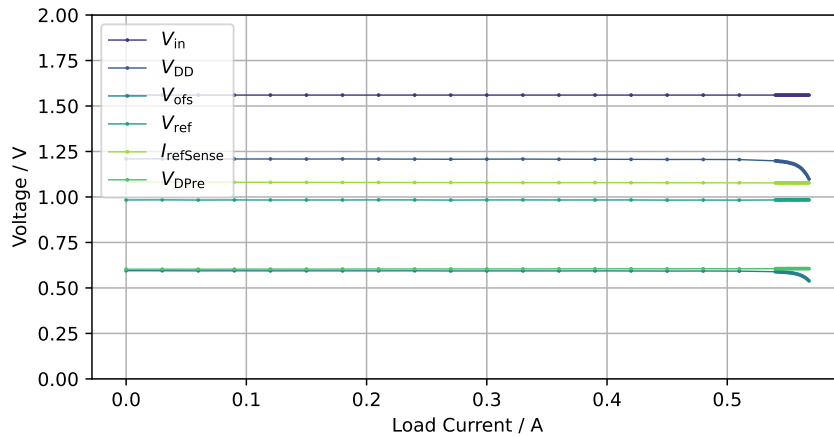
Figure 4.37: Full load regulation curve measured with an RD53B Shunt-LDO test chip B. I_{ref} is measured as a voltage drop across a 150 kΩ resistor.

(a) Load transient applied with UCP off.

(b) Load transient applied with UCP on.

(c) Minimum load pulse to cross UCP threshold.
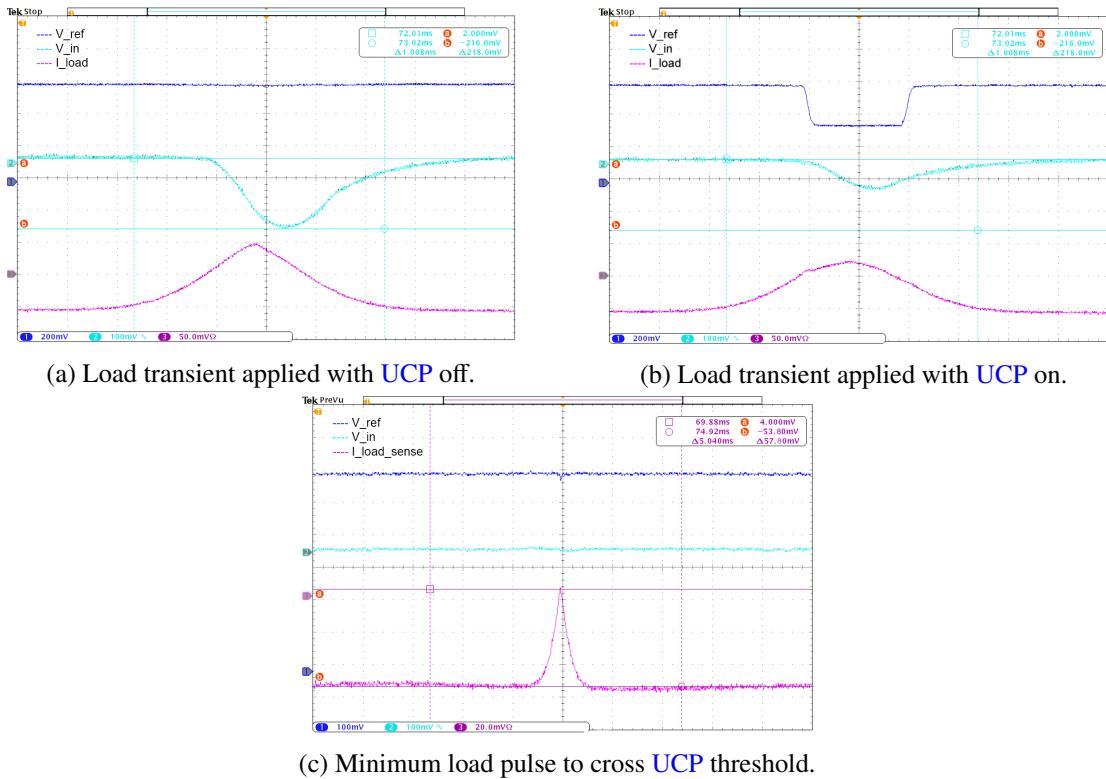
Figure 4.38: Load transients applied to RD53B Shunt-LDO with UCP switched off and on respectively. Shown are V_{in}, V_{ref} and the load pulse measured as voltage drop over a $0.1\,\Omega$ resistor.

thresholds.

To further test the UCP, the regulator is kept at a constant working point. Load transients are applied using the a power transistor. These load pulses can be sensed using a $100\,\text{m}\Omega$ resistor in the current path. Fast load transients are obtained by applying voltage pulses with a short rise time to the gate of the power transistor. An example with both UCP off and on is shown in Figure 4.38. In Figure 4.38(a), the load transient ΔI_{load} is too large for the regulator to remain stable. Instead, V_{in} starts to collapse once I_{load} increases too much. The peak load current $I_{\text{load}} = 1\,\text{A}$ far exceeds the input current $I_{\text{in}} = 0.6\,\text{A}$. In Figure 4.38(b) the same voltage pulse is applied to the gate of the power transistor, the effective load remains unchanged. With the UCP active, the behaviour is changed significantly. Once the load pulse causes I_{shunt} to drop below the UCP threshold, V_{ref} is seen to be lowered as expected down to the lower limit $V_{\text{ref}} \geq 0.35\,\text{V}$. If I_{load} is increased further at this point, the regulator starts to display the same behaviour as before. With V_{ref} being reduced significantly, the resulting peak load current is much smaller as well, roughly consistent with the drop in V_{ref}. As a result the transient in V_{in} decreases both in width and amplitude. In Figure 4.38(c) the minimum load pulse amplitude to trigger the UCP is shown. Minding the different scale compared to

the previous images, the load pulse corresponds to a peak $I_{load} = 578$ mA. This is roughly consistent with the results from the static load regulation measurement which implied a lower limit for UCP activation of 10 mA. The observed limit is much higher, thus the UCP is triggered before the Shunt-LDO would collapse without any UCP, giving some safety margin. The presented measurement is not a perfect representation of the Shunt-LDO in RD53B however, as the voltage pulse defining the load current drawn by the power transistor does not change with V_{DD}. In a real pixel ROC, the load drawn by the chip is of course dependent on its supply voltage. In fact this is essential for the UCP to work as intended. A full overload condition is thus very unlikely to occur, with the exception of electrical failures, e.g. a short circuit.

Irradiation of the new Shunt-LDO Prototype

The radiation hardness of the new Shunt-LDO implementation was verified in two X-ray irradiation campaigns in the context of this thesis. The first of these campaigns in summer 2019 covered TID up to 800 Mrad at cold temperature[3] and was performed with focus on the novel features of the Shunt-LDO design. Based on the experiences made during previous irradiation campaigns additional data, e.g. constant measurements of the k-factor, were performed during the irradiation. This campaign was followed by an additional campaign at christmas 2019. The second campaign was performed at a higher operating temperature[4] and, due to the constraints set by the timing of the campaign, was conducted up to a target TID of 2 000 Mrad, far exceeding the specifications of the Shunt-LDO. In the following the main focus will be put on the first campaign conducted, supplementary material covering the second irradiation campaign can be found in Section A.3.

The general procedure of the irradiation campaigns discussed here follows the previous examples with the 500 mA and 2 A test chips respectively. The Shunt-LDO is mounted on a cooling plate and kept at low temperature. The chip temperature is not actively controlled but the temperature of the cooling liquid is instead kept at -17 °C. During the irradiation, the Shunt-LDO is kept at a working point $I_{in} = 0.6$ A, $I_{load} = 0.5$ A. In regular intervals, the temperature of the Shunt-LDO is recorded via the NTC and a measurement of the k-factor is performed by measuring I_{ctrl} and comparing to I_{in}. The NTC temperature plotted against time during the irradiation is shown in Figure 4.39. At each measurement point, a line- and load regulation measurement was performed. This was followed by application of a load pulse to test the UCP similar to Figure 4.30. During these measurements the X-ray cabinet was switched off to reduce uncertainty on the TID. Any TID listed in plots in the following only refer to the target TID of that measurement step: since the X-ray beam

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[3] Target temperature of -10 °C

[4] Around 0 °C
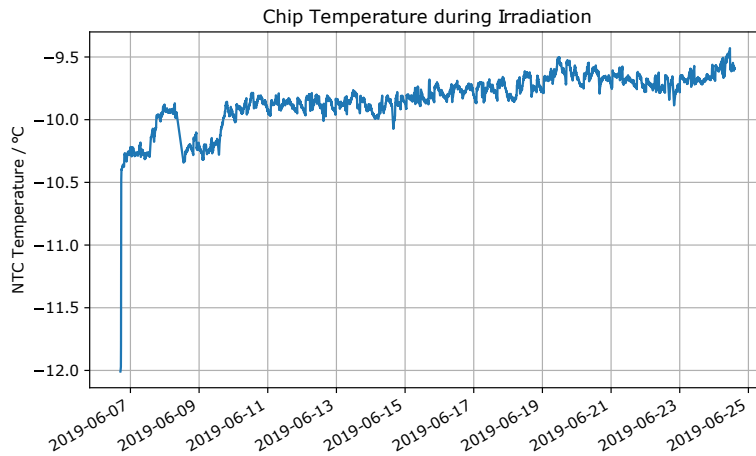
Figure 4.39: Temperature log during RD53B Shunt-LDO irradiation campaign at cold temperature

TID / Mrad	V_{OVP} / V
0	1.89 ± 0.01
10	1.88 ± 0.01
100	1.88 ± 0.01
500	1.88 ± 0.01
800	1.87 ± 0.01

Table 4.10: Measurement of OVP voltage threshold V_{OVP} during Shunt-LDO irradiation.

profile was significantly inhomogeneous [49], the actually received TID is assumed to be $0.75 \cdot \mathrm{TID}_{\mathrm{target}} \leq \mathrm{TID} \leq \mathrm{TID}_{\mathrm{target}}$. During each input IV curve measurement, the same quantities as in Figure 4.33 were measured. In Figure 4.40 shows an example measurement of V_{in}. From the collected V_{in} measurements, the effective slopes and offsets, R_{eff} and V_{ofs} are determined and shown in Figure 4.41. Over the full range of TID, R_{eff} and V_{ofs} remain fairly consistent. Only after reaching the required target TID of 500 Mrad V_{ofs} is increasing. In general the input IV characteristic of this implementation of the Shunt-LDO is more consistent with respect to the measurements shown in Figure 4.8 and Figure 4.19. The current mirror ratio remains effectively constant during irradiation as shown in Figure 4.42. This is consistent with the minimal changes observed in R_{eff}.

From Figure 4.40 a change in the behaviour of the OVP can be seen with increasing TID. In Table 4.10 the OVP voltage threshold V_{OVP} is listed. In general a lower clamp voltage
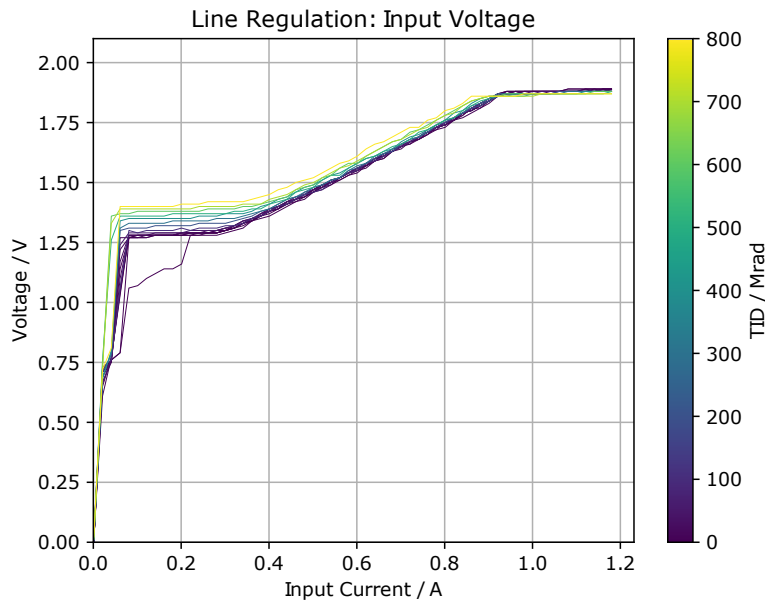
Figure 4.40: Shunt-LDO V_{out} during line regulation measurement over the course of the irradiation campaign at $-10\,°C$. Taken from [48].

for higher TID would be not problematic assuming the difference ΔV_{OVP} is small, as it does not open the possibility for operating the Shunt-LDO at unsafe V_{in}. A significant decrease in V_{OVP} combined with an increase in R_{eff} or V_{ofs} would be potentially problematic, if the resulting drift of the regulator's working point exceeds the OVP threshold. The campaign indicates a slight decrease in N_{OVP}, as for a constant V_{refOVP} the clamp voltage decreases slightly with TID but is barely resolved given the measurement accuracy of V_{in}, thus showing a sufficient radiation hardness of the OVP circuitry.

The line- and load regulation performance are shown in Figure 4.43. The line regulation performs similar to the test bench measurement shown in Figure 4.33. For low TID it remains mostly unchanged and improves with TID. The load regulation in turn performs worse for large TID but is close enough to the specifications for TID $\leq$ 600 Mrad, while the line regulation exceeds the specifications as seen before.

Considering Figure 4.41 a small shift in the working point of the Shunt-LDO is expected: with V_{ofs} increasing by approximately 50 mV during irradiation and R_{eff} remaining largely constant, the working point should follow the change in V_{ofs}. This can be seen in Figure 4.44(a), where an increase in V_{in} for a defined $I_{\text{in}} = 0.6\,A$ during irradiation is seen. This shift in V_{ofs} is in good agreement with the seen shift in I_{ref} during irradiation. Since V_{ref} is generated using a copy of I_{ref} as well, V_{DD} should show a qualitatively similar behavior to I_{ref} which can be seen comparing Figure 4.44(b) with Figure 4.44(c). Furthermore, the output V_{DD} does not
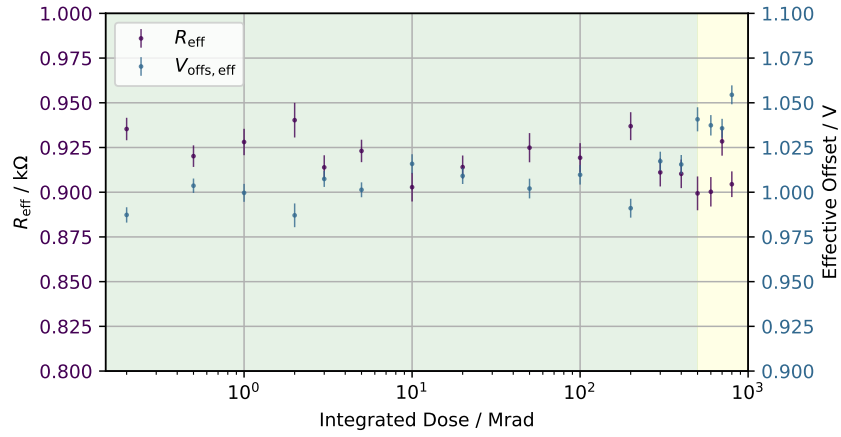
Figure 4.41: R_{eff} and V_{ofs} extracted from input IV measurement during cold irradiation of the RD53B Shunt-LDO test chip B. The TID limit required by the Shunt-LDO specifications is color coded *green*.
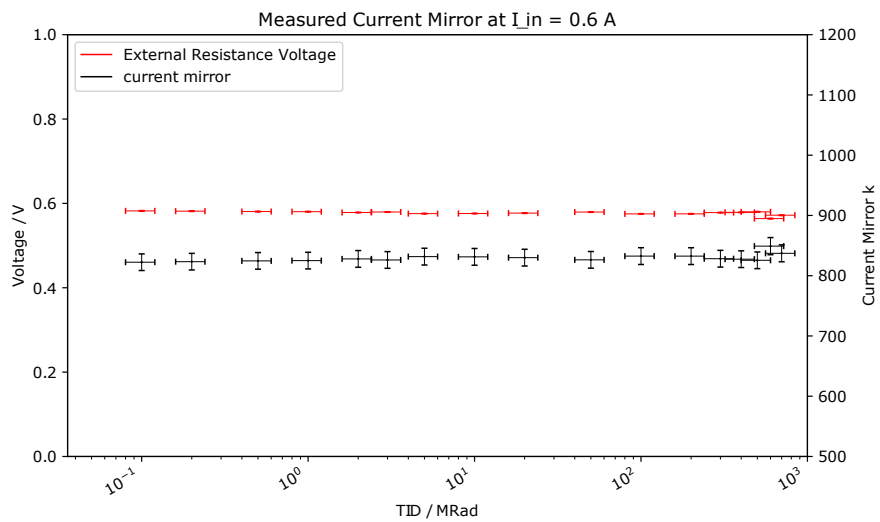
Figure 4.42: R_{eff} and V_{ofs} extracted from input IV measurement during cold irradiation of the RD53B Shunt-LDOtest chip B. The TID limit required by the Shunt-LDO specifications is color coded *green*.
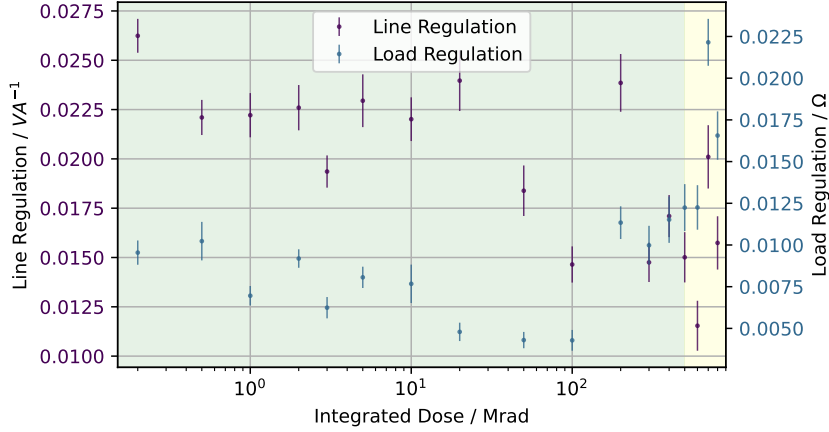
Figure 4.43: Line- and load regulation extracted during cold irradiation of the RD53B Shunt-LDOtest chip B. The TID limit required by the Shunt-LDO specifications is color coded *green*.

exactly follow the reference voltage V_{ref} exactly. This is due to a shift in the output steering at the working point as shown in Figure 4.44(d) which corresponds to a $\Delta V_{\text{DD}} \approx 10\,\text{mV}$.

After each of the discussed IV curve measurements, the UCP of the Shunt-LDO was tested by applying a load pulse to the regulator. For these measurements, the regulator was kept at the working point of the irradiation $I_{\text{in}} = 0.6\,\text{A}$ with a constant load drawn $I_{\text{load}} = 0.5\,\text{A}$. To provide a better resolution the voltage signal applied to the power transistor's gate was chosen as a linear ramp instead of a rectangular voltage pulse. As spatial constraints did not allow connection of voltage probes directly to the PCB, V_{in} and V_{ref} were measured using the sense lines for IV curve measurements. When V_{ref} and V_{in} were connected to the oscilloscope for UCP measurements, the reference voltage V_{ref} dropped by approximately $80\,\text{mV}$, as the scope input impedance of $1\,\text{M}\Omega$ formed a resistive current divider with the V_{ref} generating resistor R_{Vref}. This effectively reduces the current flow I_{RVref} through R_{Vref} such that

$$V_{\text{ref}} = \frac{I_{\text{RVref}}}{R_{\text{Vref}}} = \frac{4\,\mu\text{A} \cdot \frac{R}{R_{\text{Vref}}}}{R_{\text{Vref}}}, \tag{4.8}$$

with R being the impedance of R_{Vref} and the oscilloscope connected in parallel. With $R_{\text{Vref}} \approx 150\,\text{k}\Omega$ this yields an expected V_{ref} of approximately $520\,\text{mV}$, which is in good agreement with the measurement. The exact value of V_{ref} does not matter for the UCP operation however, as long as $V_{\text{ref}} \geq 350\,\text{mV}$. During IV curve measurements the oscilloscope was disconnected.

In Figure 4.45 results from the UCP measurements during irradiation are shown. The voltage pulse applied to the power transistor gate was chosen in amplitude such that V_{ref} would be decreased down to the lower limit of $350\,\text{V}$. Monitoring of the actual load pulse

(a) Input voltage V_{in} as function of TID

(b) Reference current I_{ref} as function of TID

(c) Output voltage V_{DD} as function of TID

(d) Output steering at working point as function of TID
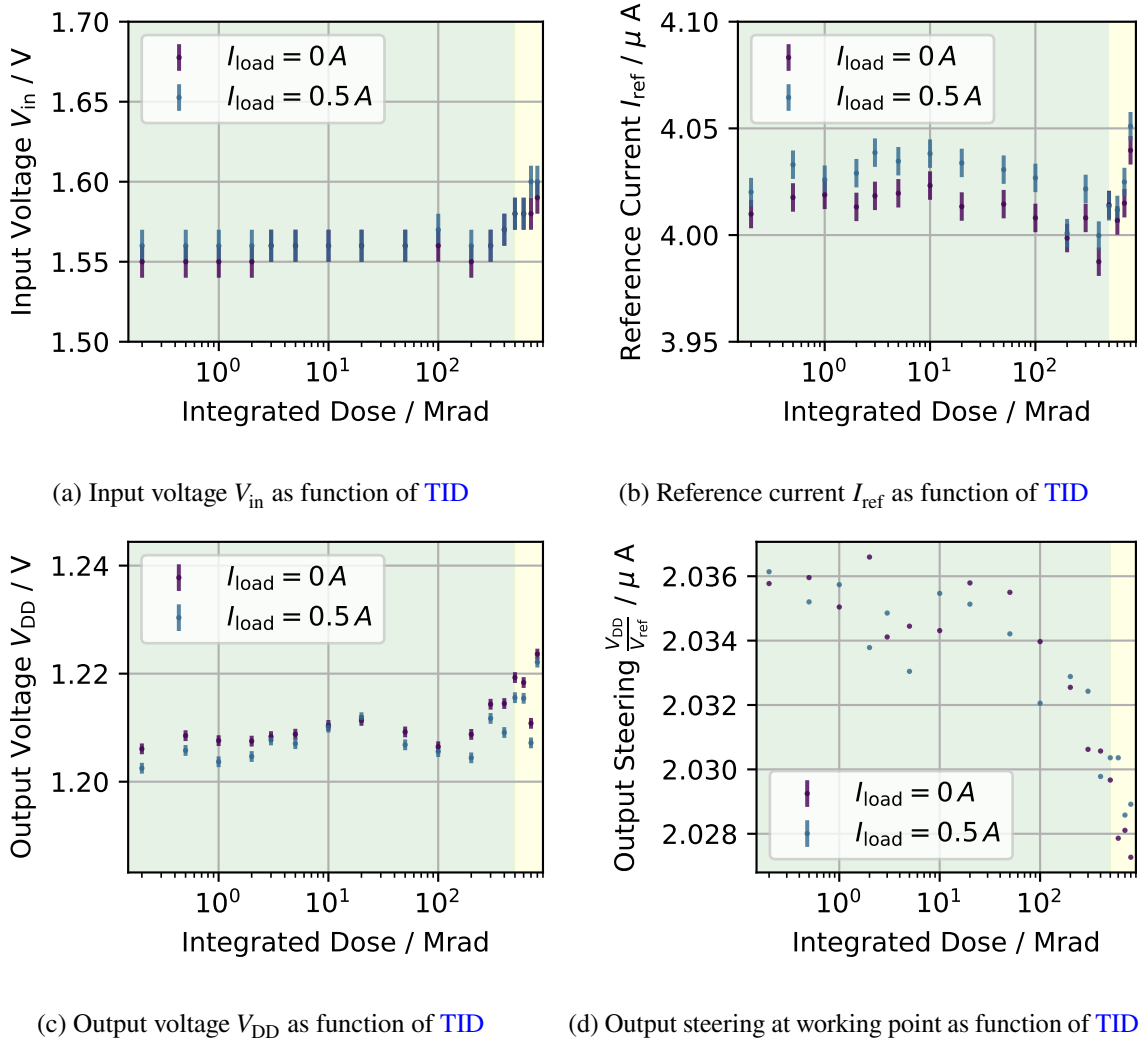
Figure 4.44: V_{in}, V_{out} and the references V_{ref} and I_{ref} as function of TID at an operating point $I_{in} = 0.6\,\mathrm{A}$ with both no load current drawn and a load current of 0.5 A.

itself was not possible in the setup. Initially, before any irradiation takes place, the UCP behaves as shown in Figure 4.45(a). As expected a transient on V_{in} only develops once V_{ref} reaches the limit of the UCP. With higher TID the UCP performance appears to be degrading. In Figure 4.45(c) V_{ref} is always lowered by the UCP even if no load pulse is applied. The circuitry recovers once the voltage pulse amplitude is decreased slightly. This combined with the UCP being active even with very little voltage applied to the power transistor gate strongly hints at the cause not being a degradation of the UCP but rather radiation damage to the power transistor, which was not sufficiently shielded during the irradiation. As can be seen from Figure 4.46, the threshold voltage of the power transistor is lowered significantly. For the same gate voltage pulse applied, the current drawn from a Shunt-LDO increases by 200 mA. As the power transistor is an NMOS transistor it is expected to be more conductive for a given gate voltage with larger TID. The default voltage pulse applied to the power transistor gate in Figure 4.45 was 1.04 V as in Figure 4.46. An unirradiated Shunt-LDO showed the same UCP performance as Figure 4.45 when loaded with the irradiated power transistor. Given in the measurements presented above the Shunt-LDO shunt current was $I_{shunt} \leq 100$ mA, it was thus concluded that the observed UCP behaviour was completely driven by radiation damage to the power transistor. Unfortunately this could not be verified by using the irradiated Shunt-LDO with an unirradiated power transistor as the regulator was damaged during a follow-up measurement.
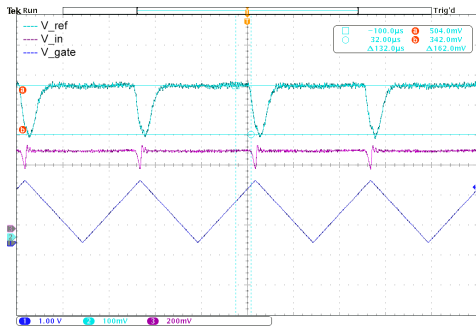
(a) Load transient applied with UCP on before irradiation.
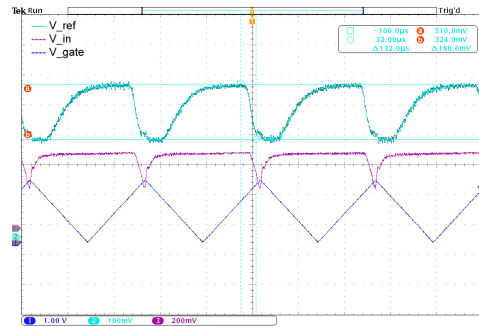
(b) Load transient applied with UCP on at a TID of 400 Mrad.
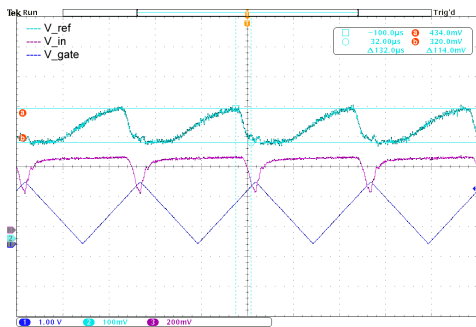
(c) Load transient applied with UCP on at a TID of 500 Mrad.
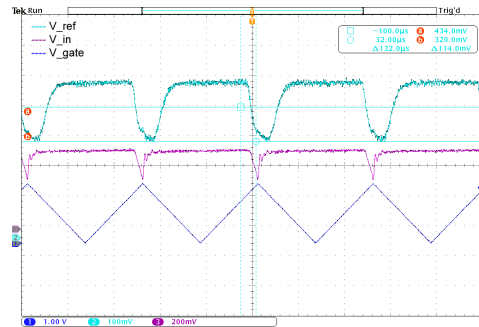
(d) Load transient applied with UCP on at a TID of 500 Mrad with a lowered pulse voltage.

Figure 4.45: Load transients applied to RD53B Shunt-LDO with UCP switched on during irradiation. Shown are V_{in}, V_{ref} and the voltage pulse controlling the power transistor which draws additional load from the Shunt-LDO.

4.4 Conclusion and Outlook Towards the ATLAS Production Chip

The development of pixel ROC for the next generation ATLAS and CMS experiments at the HL-LHC foresees serial powering as the baseline powering mode for the pixel detector of both experiments. Thus the Shunt-LDO is a core element of the future pixel chips which needs to be characterized and studied in depth. While a large part of the verification work is done in simulation of the analog circuits, ultimately bench testing with prototype chips is necessary especially considering the requirements for radiation tolerance in RD53. In the context of this thesis, the development of the Shunt-LDO has been followed closely within the RD53 collaboration over the course of nearly 3 years. The results presented here cover the characterisation of the Shunt-LDO circuitry starting from the first implementation in the new 65 nm CMOS technology up to the regulator prototypes for RD53B. All of these results have been obtained in close collaboration with the chip designer and cover 6 generations of

(a) Load current drawn by an unirradiated power transistor for a gate pulse amplitude of 1.04 V, just triggering the UCP. The peak I_{load} drawn is approximately 580 mA
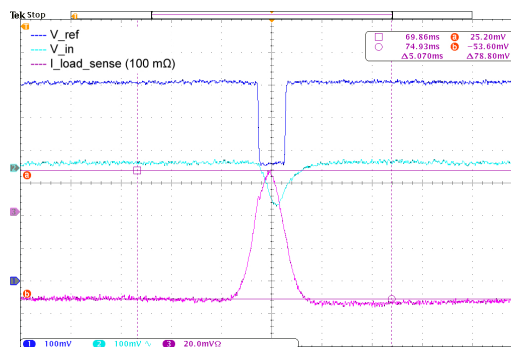
(b) Load current drawn by the irradiated power transistor for a gate pulse amplitude of 1.04 V. The peak I_{load} drawn is approximately 780 mA
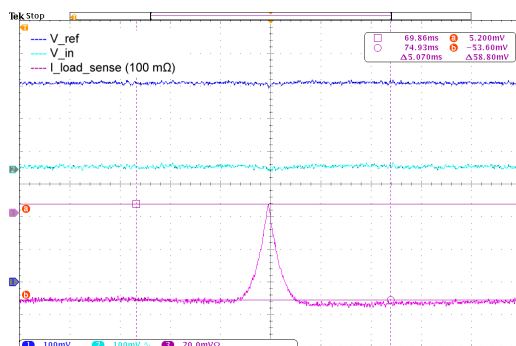
(c) Load current drawn by the irradiated power transistor for a gate pulse amplitude of 0.942 V, just triggering the UCP. The peak I_{load} drawn is again approximately 580 mA

Figure 4.46: Comparison of the load current drawn by the power transistors used on the Shunt-LDO test PCB for a given gate pulse amplitude.

the Shunt-LDO circuit.

Starting with the first prototypes, the 500 mA and 2 A prototype chips, the functionality of the Shunt-LDO was verified in the novel technology node used within RD53 in section 4.1, key results are listed in Table 4.2 and Table 4.3. In two irradiation campaigns the radiation hardness of the core regulator was proven sufficiently. The unreliable bandgap reference was reworked for implementation in RD53A. Comparing the performance to the regulator specifications set for RD53B these first prototypes do not match the specifications fully. Both line- and load regulation is generally too large, especially considering the externally provided reference voltages V_{ref} have a positive impact on regulator performance. Parasitics in the regulator circuitry show a serious impact on the Shunt-LDO working point which can quickly become an issue when combining multiple Shunt-LDO on multi-chip pixel modules in serial

powering chains with a tight power budget.

The Shunt-LDO in RD53A was the first realistic implementation in the new technology node, being tightly intertwined with the pixel ROC on the same chip. By design the RD53A should in principle be operational in a HL-LHC environment in a serially powered detector. Due to issues with the new bandgap reference circuit design the performance of the Shunt-LDO in RD53A was lacking: late start-up of the bandgap reference prevents operation of RD53A at otherwise feasible working points for many chips and a lower than expected output voltage of the bandgap can render RD53A essentially not operational if core blocks such as the CDR are not sufficiently supplied. Since RD53A was still very much a prototype chip, all of the encountered issues could be tackled with fixes in procedure or testing hardware. The mature core design of the Shunt-LDO in turn performs well, enabling operation of serially powered pixel detectors with RD53A pixel modules without any performance impact compared to a direct powering scheme. This will be demonstrated in the following in Section 5.2. Key results from measurements with RD53A are listed in Table 4.6 and Table 4.7.

Based on the experiences made with RD53A significant improvements were made to the Shunt-LDO design for use in the RD53B based pixel ROC. The most prominent improvement is the implementation of a redesigned bandgap reference scheme and an auxiliary startup circuit to ensure proper Shunt-LDO startup even at very low currents. Driven by new requirements from the experiments, additional features were included in the Shunt-LDO. Spanning 3 iterations of prototype chips, this finalized Shunt-LDO design including the full feature set was verified and tested for irradiation hardness. Key points of the characterisation efforts with test chip B can be found in Table 4.8 and Table 4.9. Ultimately the last remaining larger issue discovered in the Shunt-LDO prototyping phase, the mismatch of the current mirror k, could be successfully traced back to a bug in the regulator design and was fixed.

At the time of writing the first prototype versions of the final ITkPix and CROC are becoming available in larger numbers for final verification efforts. The Shunt-LDO in these chips is expected to be very well performing. A first look into the performance of the Shunt-LDO in the ITkPix pixel chip can e.g. be found in [50].

Large Scale Serial Powering Prototypes for the ITk Pixel Detector

Qualification of SP does not only require verification efforts of the core building block of the current SP design on the scale of single chips, the Shunt-LDO, as was elaborated in Chapter 4. It also necessitates setting up representative prototypes for the full scale system. These span from short SP chains consisting of only a few modules up to large prototypes with several SP chains and dozens of modules involved. Naturally these setups provide the most valuable insights when utilizing the most recent ROC and Shunt-LDO available. This is
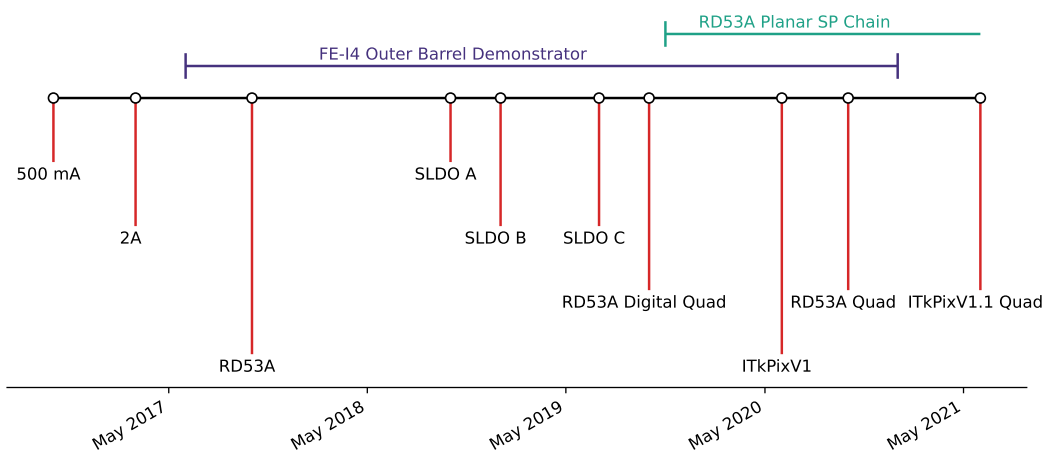
Figure 5.1: Approximate timeline showing large scale SP system test setups directly covered in this thesis and as a reference relevant milestones in R&D phase within RD53. RD53A and ITkPix (digital) quads refer to the module design used in the prototype covered in section 5.2.

not always feasible, as especially large scale system tests require hardware commitments not possible in early R&D stages. Here the amount of available ROC or modules is usually the limiting factor. As a consequence SP prototype setups tend to lag behind the parallel ongoing hardware developments, utilizing older generation ROC instead, which are often more readily available. In Figure 5.1 an approximate timeline of selected SP prototypes is compared to development milestones with respect to the RD53 collaboration.

First large scale SP prototypes, intended to build upon initial efforts e.g. by [24, 51], were conceived with a planned population with FE-I4 pixel modules in mind, the most recent ROC available at the time which also featured an integrated Shunt-LDO, similar to the circuitry discussed in Section 4.1.1: at the time the design for RD53A was not yet submitted for production. One of these large prototypes is the OBD at CERN, consisting of 6 SP chains loaded on a common local support and is introduced in Section 5.1. This prototype campaign featured a smaller precursor prototype: the Small Electrical Prototype. This setup consisted of only a single section of the later OBD, a single SP chain populated with 7 FE-I4 quad chip modules. This prototype campaign was designed to be as mechanically representative as possible for the future ITk pixel detector in order to qualify detector design choices and preparing infrastructure for future prototypes and production of the ITk pixel detector. Additionally, the behaviour of the used FE-I4 modules in serial powering chains in a more realistic framework could be studied. On the other hand the FE-I4 limited the achievable knowledge gain, as it does not represent certain features of the upcoming ROC, e.g. the high-speed data transmission, increased power consumption and redesigned Shunt-LDO. Over the course of this thesis there was constant involvement in the OBD program, with emphasis on the commissioning phase of the Small Electrical Prototype. An overview of the Small Electrical Prototype is given in Section 5.1.1.

To address the limitations of FE-I4 based prototypes, follow-up experiments were scoped and designed. These setups were intended to utilize pixel modules based on the newly available RD53A ROC. Within the ATLAS collaboration the planned prototypes include a large scale system similar to the OBD for each of the ITk pixel subsystems and serial powering test benches loaded with 3D- or planar modules. Both *3D* and *planar* are referring to the design of the sensor, where a planar sensor has a planar readout electrode parallel to the sensor backside. In a 3D sensor the readout electrodes are realized as columns drilled into the sensor bulk. In the context of this thesis such a prototype consisting of RD53A quad modules with planar sensors has been set up and characterized. This prototype, covered in Section 5.2, was designed with a different focus compared to the OBD. The setup was intended to be electrically representative of the future ITk pixel, featuring a novel current source prototype, while not considering the mechanical constraints present in setups like the OBD. The focus was put on the electrical characteristics and performance of current generation pixel modules in a SP chain. Results obtained with this prototype are covered in Section 5.3 and have been

shared and discussed in the ATLAS system test community. The system was designed to be compatible with ITkPix pixel modules once available, which allows a fast setup of an SP prototype with the final production ROC. In Section 5.3.6 an outlook on the most recent developments, an SP chain with 13 digital[1] ITkPix quad modules, is given.

5.1 The Outer Barrel Demonstrator Program

The OBD program was launched to verify the various aspects of the new ITk pixel detector layout. Being launched before the first RD53A ROC were available, most components have not been finalized at the time, however the OBD program still allowed gaining invaluable experience in integrating and operating large system tests as are required for ITk pixel.

Several prototypes have been built within the OBD program to focus on the different system aspects. Prototypes of functional local supports have been built to demonstrate the mechanical and thermal performance of the support structures and prepare equipment needed for the shipping of loaded support from loading sites to integration sites, as the assembly and integration of ITk pixel will be a decentralized effort. In addition to the mechanical efforts a
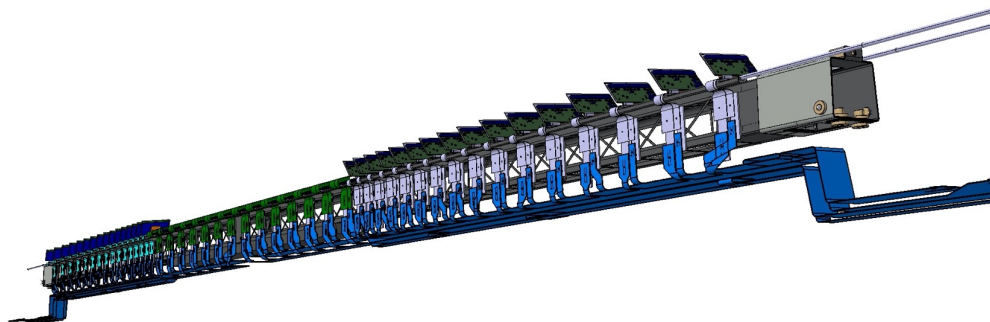
Figure 5.2: CAD drawing of the OBD concept. On a half loaded longeron 64 FE-I4 modules, quad modules in the flat region and dual chip modules in the inclined region, are integrated. The modules are organized in 4 SP chains, each with 7 quad modules or 16 dual chip modules. Alternatively a configuration with 6 SP chains can be chosen, consisting of 2 SP chains with 7 quad modules each and 4 SP chains with 8 dual chip modules each [52].

large program has been launched to demonstrate the electrical aspects of operating multiple SP chains on a common, representative local support with representative services and power supplies. This prototype, referred to as the demonstrator, consists of 46 FE-I4 based pixel modules, 14 quad chip modules in a flat section and 32 inclined dual chip modules, totalling

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[1] A module without a sensor tile bump bonded to the ROC.
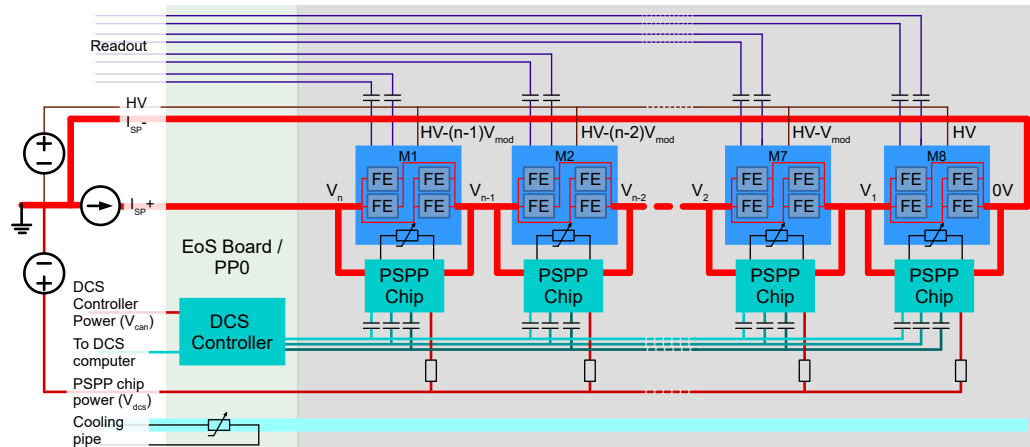
Figure 5.3: Powering scheme of the OBD following [30].

120 ROC, on a longeron of 1.6 m length. The longeron is a carbon truss structure, offering mechanical support for the detector while introducing little mass into the detector. A single cooling pipe is attached to each side of the surface the longeron. The modules are loaded on pyrolitic graphite tiles which are directly connected to the cooling pipe. This allows for two rows of modules, slightly offset with respect to each other, to be integrated on a single longeron. A CAD drawing of the full demonstrator is shown in Figure 5.2.

The powering scheme of the OBD follows the scheme suggested in [30] and is shown in Figure 5.3. At the time a dedicated chip was foreseen as part of the detector control system (DCS) for each module, which provided monitoring and bypass functionality: the PSPP chip [53, 54]. A maximum SP chain length of 16 modules was foreseen. The full system was to be supplied using the same types of power supply units currently in use for the ATLAS pixel detector including a comparable services inventory.

A project of such scale like the OBD program of course requires significant person power and involves many people and institutes from the ATLAS system test community and and far exceeds the scope of a single PhD thesis. In the context of this thesis, significant contributions have been made to the OBD program, with a focus on the small electrical prototype.

5.1.1 A Small Electrical Prototype

The demonstrator was preceded by the Small Electrical Prototype consisting of only a single flat section of the full demonstrator with 7 FE-I4 quad modules. The Small Electrical Prototype allowed verification of the full integration procedure and detector operation on a smaller scale. The DCS for the later demonstrator was developed and commissioned with the Small Electrical Prototype. Results obtained with the Small Electrical Prototype are e.g.

(a) CAD drawing of the Small Electrical Prototype [58].

(b) Photograph of the Small Electrical Prototype. Modules are separated by thin pieces of kapton tape to ensure electrical insulation [55].
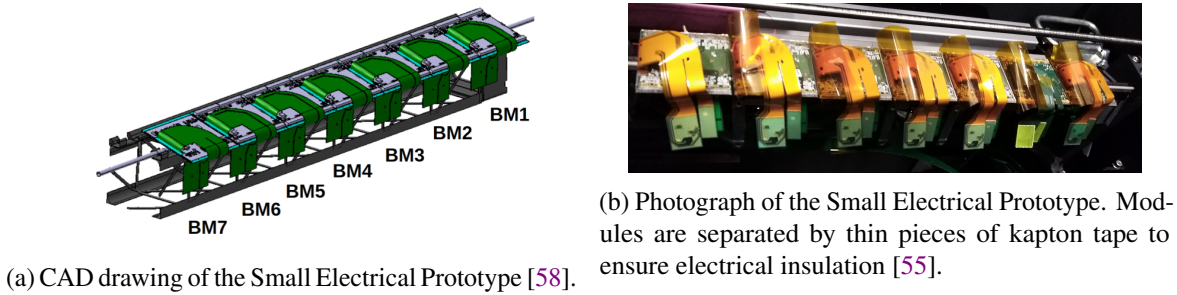
Figure 5.4: CAD Drawing and picture of the fully assembled Small Electrical Prototype.
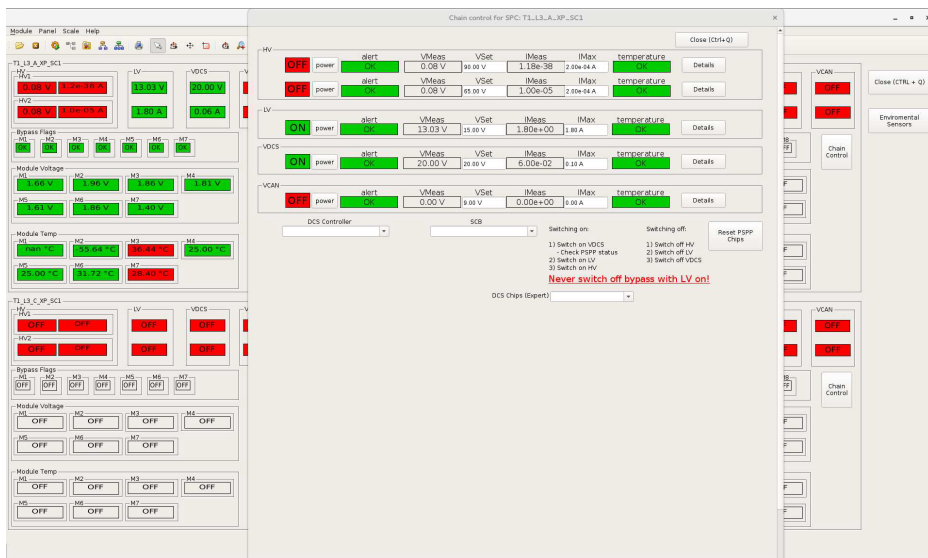
Figure 5.5: View of the slow control user interface for the OBD and Small Electrical Prototype.

published in [53, 55–57]. A CAD drawing and photograph of the fully assembled Small Electrical Prototype can be seen in Figure 5.4.

The DCS includes all elements as described in [53] and is integrated in a supervisory control and slow control DAQ tool based on SIMATEC WinCC OA [59]. An example view of the user interface is shown in Figure 5.5. This interface gives an overview of the current status of the prototype, including access to all monitoring parameters, and allows control of the full setup.

During the commissioning phase the pixel modules loaded on the Small Electrical Prototype were read out using the pyBAR [60] DAQ. Following the immediate commissioning the Small Electrical Prototype and later the OBD served as a test bed for large scale DAQ developments for ITk pixel [57].

(a) Digital scan.

(b) Analog scan.
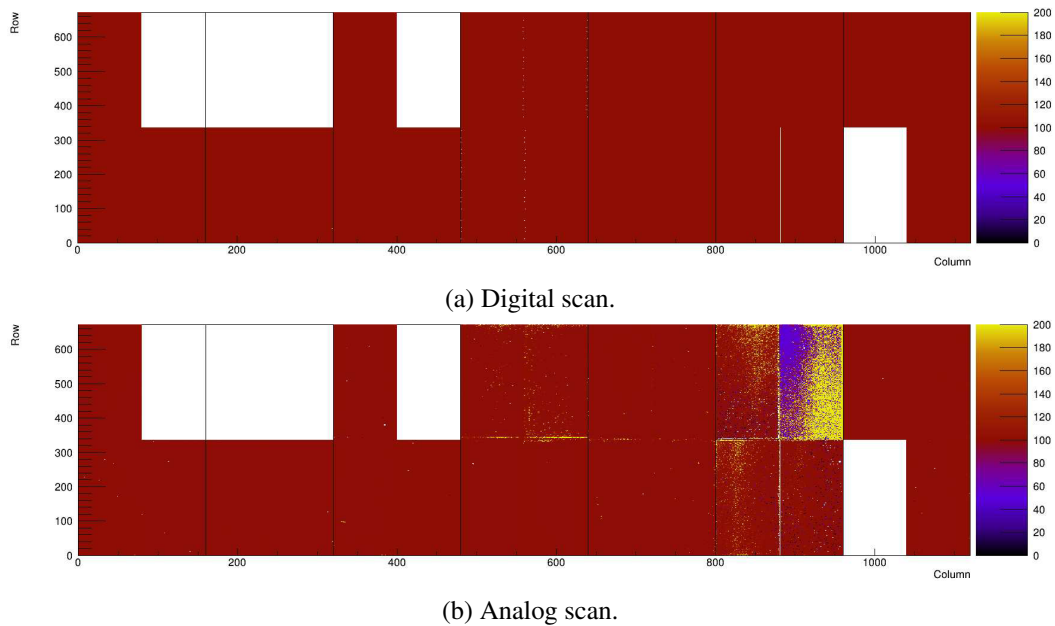
Figure 5.6: Digital and analog test injections for all ROC integrated in the Small Electrical Prototype. Modules 4-6 are not connected to HV and show a inhomogeneous response.

Results and Lessons Learned from the Small Electrical Prototype

Although some of the ROC integrated in the Small Electrical Prototype were not fully operational, the SP chain is in principle fully functional. All modules were tested extensively during the integration steps. The testing procedure and results can be found in [61]. 2 out of the 7 modules integrated in the setup, M4 and M5, have damaged sensors. Modules M1, M2 and M3 share a common HV supply and return line. Modules M4, M5 and M6 are not connected to HV and module M7 is connected to the second HV supply and return line. As can be seen in Figure 5.6 most ROC are working as expected in terms of digital and analog injection tests. As part of the evaluation of the module performance in the SP chain, the modules were tuned to a target detection threshold of $3\,000\,e^-$ with a ToT target code of 10 for the reference injection used in analog scans. The resulting threshold and Equivalent Noise Charge (ENC) distribution is shown in Figure 5.7. A scan with a radioactive Sr90 source is shown in Figure 5.8. Here large areas of disconnected bump bonds between sensor and ROC become visible. From reception tests of the modules used in the Small Electrical Prototype such poor quality was expected, as no high-grade modules were available for this first prototype. Considering the module quality as such, the Small Electrical Prototype performs well within expectation.

The monitoring capabilities of the DCS used in the OBD program allowed further insights in a serially powered detector system. Monitoring of the input voltage V_{in} of each module
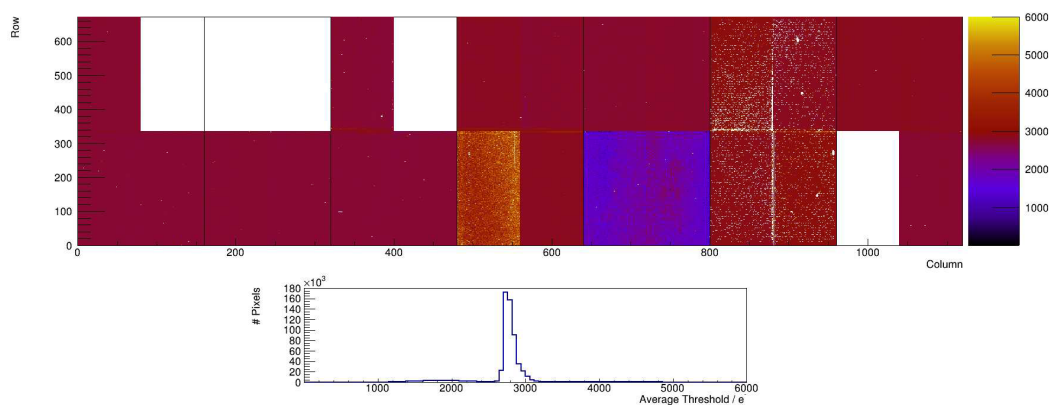
(a) Threshold distribution.
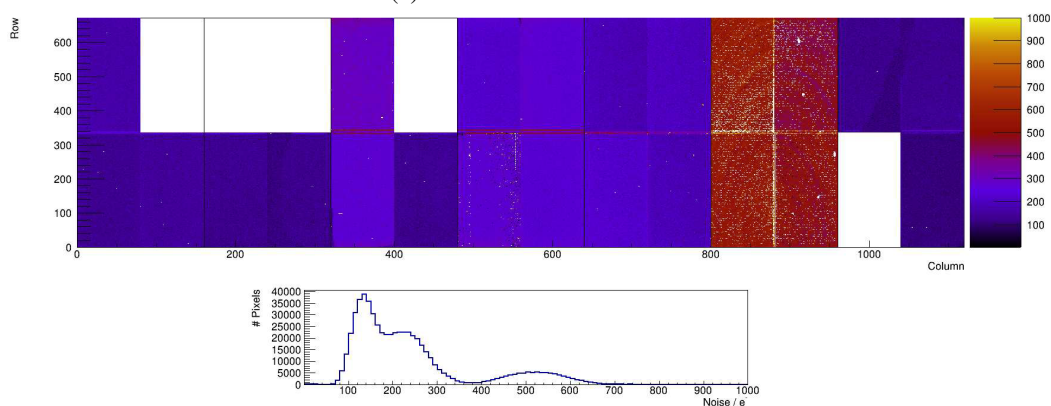
(b) ENC.

Figure 5.7: Threshold distribution and ENC after tuning to $3\,000\,e^-$ with a target ToT code of 10 for reference injections. Modules M4, M5 and M6 show larger ENC due to the lack of a bias voltage applied to the sensor.

during the power up of the structure or during tests with DAQ systems as shown in Figure 5.9 can reveal unexpected behaviour of the system.

In Figure 5.9(a) the input voltage of the FE-I4 is shown not to be constant upon start up. This is understood to be the consequence of a not well defined power-on configuration of the ROC, which can draw too much load current from the Shunt-LDO regulators, leading to a regulator overload. According to follow-up investigations this is dominated by a single register, setting the supply current for the main CSA in the ROC, the pre-amplifier bias. As discussed in Section 4, overloading a Shunt-LDO regulator leads to a significant drop in that regulator's R_{in}, which is visible as a drop in V_{in}. In Figure 5.9(b) a different example for dynamic overloading of Shunt-LDO regulators on a pixel module is shown. Here a DAQ system based on a gigabit transceiver (GBT) was used. In its power-on state, this DAQ system was sending arbitrary bits on the CMD lines connected to the SP chain while also
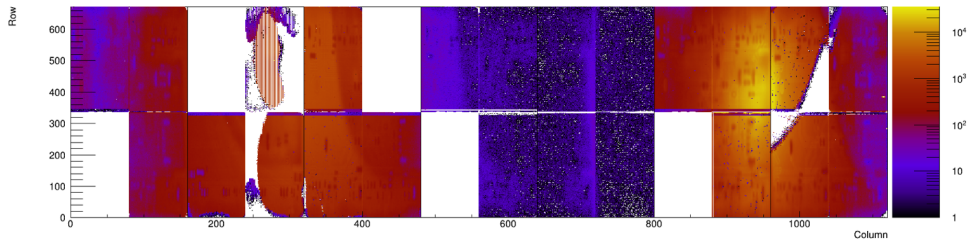
Figure 5.8: Radioactive source scan with a Sr90 source on the Small Electrical Prototype after repairing the HV connection of M6. Large regions of disconnected bump bonds are visible. Not all ROC functional for source scans. The overall lacking yield is expected, as the modules were seen to be not fully functional during first reception tests [55].
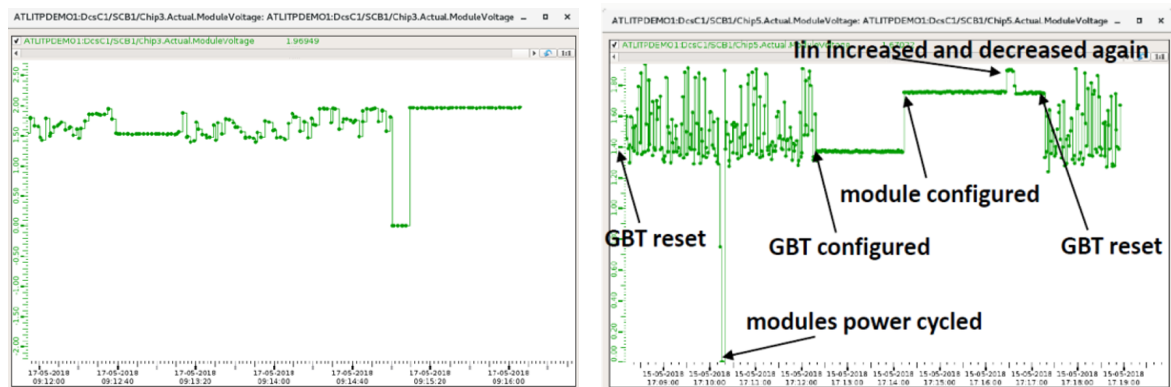
(a) V_{in} as measured for one module during power up sequence of the Small Electrical Prototype. Until the module is configured properly, V_{in} does not settle to a constant value, which would be expected from the Shunt-LDO.

(b) V_{in} as measured for one module during power up and configuration sequence of a GBT based [57] DAQ. For a not-configured readout system V_{in} is highly unstable. Only after configuration of both the DAQ and the ROC can a stable working point be reached.

Figure 5.9: Dynamic overload of the Shunt-LDO in FE-I4 modules in an SP chain. In Figure 5.9(a) the FE-I4 module upon startup in is not in a sufficiently defined configuration, leading to an excessive current consumption. This overloads the Shunt-LDO, leading to a sudden decrease in V_{in} of the module. In Figure 5.9(b) a misconfigured DAQ system is sending random bits on the CMD lines to the FE-I4 module. These random bits can correspond to valid commands interpreted by the ROC, changing its configuration. Here this leads to configurations which draw too much current, resulting in a regulator overload.

providing a valid CLK. It is expected that some of these arbitrary bit patterns will form a valid command for the FE-I4. This can then result in random changes in the configuration of the ROC. While most of these changes would remain undetected, sometimes the FE-I4 is put into a high-power state which can overload the Shunt-LDO regulators, a behaviour similar to the start-up behaviour of the serial powering chain described above. Once the DAQ has

been configured no random bit patterns are sent anymore and the ROC remains in its current configuration. In the example shown in Figure 5.9(b) the ROC ends up in a configuration overloading at least one of the Shunt-LDO regulators. After proper configuration of the full module no regulator overload is visible and the module remains in the targeted working point. Upon resetting the DAQ, random patterns are again sent to the ROC, resulting in dynamic overloading of Shunt-LDO regulators on the module. In a serial chain these overloads can manifest themselves as transients on the LV line seen by neighbouring modules in the chain, if the power supply can not regulate its output voltage fast enough. Such transients can cause damage to the Shunt-LDO, if the input voltage seen by any Shunt-LDO is too large. In the OBD, PSPP chips monitor V_{in} of each module and activate a low impedance bypass if V_{in} exceeds a threshold value. In effect bypassing a module can have a similar effect as a regulator overload: due to the sudden drop in module voltage, as the bypass has a low impedance, transients will occur on the LV line if the power supply regulation is too slow. In combination this can lead to a chain reaction in which SP chain which is switched off by the DCS, once the first module bypass is switched on. In the new generation ROC measures have been taken to mitigate such unwanted behaviour. A robust power-on reset has been implemented in RD53A which ensures the ROC is in a well defined configuration upon startup. Furthermore, RD53A can only decode and execute commands if the CDR can lock onto the incoming bit stream, which requires a frequency of approximately 160 MHz. For a random command pattern this lock will fail and the ROC can't be configured arbitrarily. The PSPP chip has been dropped from the ITk pixel detector design, removing potential chain reactions as described above. Without a PSPP chip however the serial chain is more vulnerable to transients on the LV line, e.g. caused by module failure. These vulnerabilities are addressed by the overhauled Shunt-LDO found in the ITk pixel production ROC, in particular using the OVP and UCP, see also Section 4.3 and Section 4.3.

During power up of the Small Electrical Prototype measurable leakage currents have been observed on the HV line monitoring although no bias voltage was applied. When switched off the HV power supply was in a high-impedance state with some $10\,M\Omega$ between its terminals. As discussed in Section 3.1.2, the module in a given HV group with the lowest local GND potential with respect to the system GND is a lower impedance return path for the leakage current, if the off-mode impedance of the power supply exceeds the bias resistor on the HV line, which is typically in the order of $10\,k\Omega$. Depending on the total amount of leakage current, the last n modules in the HV group can then be subjected to a significant forward bias. This raised concerns as it could be potentially damaging to the ROC and triggered further studies as in Section 5.3.5 and [33].
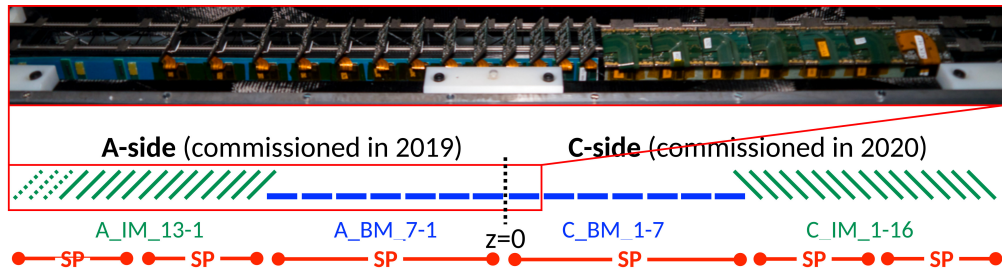
Figure 5.10: Schematic overview of the final demonstrator. A photograph of the *A*-side of the longeron shows the quad modules in the flat section as well as the inclined duals. The different powering units, i.e. SP chains, are denoted. The SP chains for the inclined dual chip modules can be combined to a single, up to 16 modules long SP chain [63].

5.1.2 The Outer Barrel Demonstrator

The Small Electrical Prototype provided a lot of valuable experiences for the operation of a SP chain with representative services and infrastructure. However with the smaller setup the operation of multiple SP chains on a common local support could not be demonstrated sufficiently. This had to be done using a larger prototype to verify the grounding and shielding scheme of the outer barrel (OB), which electrically couples the local supports to the modules. Consequently the Small Electrical Prototype was followed up on by the full demonstrator. The demonstrator consists of a single longeron structure which, according to the designs for the OB available at the time, would be populated with six independent SP chains. Each of the two sides of the longeron is divided into a flat section consisting of 7 quad chip modules grouped in a SP chain and an inclined section consisting of 16 dual chip modules, which can be grouped together in a single powering chain or alternatively in two chains with 8 modules each. As mentioned the flat section is identical in layout to the Small Electrical Prototype. The longeron in the demonstrator program is half loaded, with only A- and C-side populated. The *A*-side is not fully populated with only 13 dual chip modules as the number of suitable modules available was not sufficient. In Figure 5.10 the corresponding schematic overview of the demonstrator together with a photograph showing the *A*-side of the longeron is shown. Together this resulted in not only the first prototype utilizing multiple parallel SP chains on a common local support, but also the largest SP prototype with the longest SP chains built to date. In the context of this work, the commissioning and subsequent measurement program of the final demonstrator was accompanied. With a stand-alone publication still in progress, some results obtained with the final demonstrator have been published in e.g. [62–64] and are cited here to give some impressions of the outcome of this large project.

In the full demonstrator modules of higher quality have been used compared to the Small

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(a) Threshold distribution.

(b) ENC.
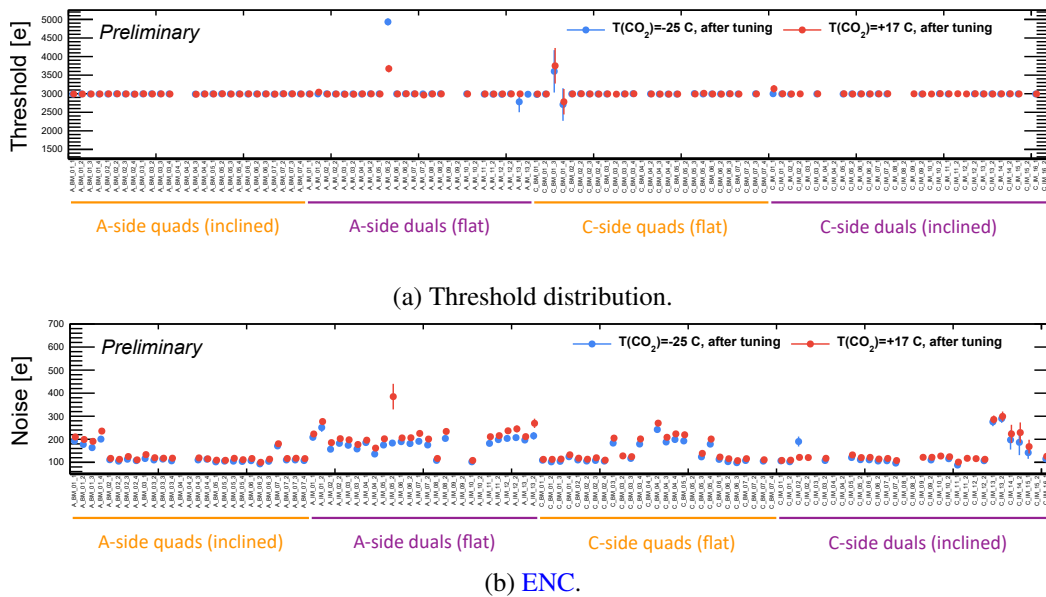
Figure 5.11: Threshold distribution and ENC of the full demonstrator after tuning to $3\,000\,e^-$. Taken from [63].

Electrical Prototype. Accordingly a better module performance also with respect to overall functionality is expected. A measurement program similar to the Small Electrical Prototype, yet larger in scale due to the increase in modules on the prototype, has been conducted. As expected, the module yield in the full demonstrator is significantly better compared to the Small Electrical Prototype. In Figure 5.11 the threshold distribution and ENC of all functional ROC are shown after all modules have been tuned to a detection threshold of $3\,000\,e^-$. As can be seen only a limited number of ROC could not be operated, as data from these chips is missing. For the remaining ROC the resulting threshold distribution is homogeneous with only a few chips not reaching the target threshold values. The ENC levels are less homogeneous yet in agreement with previous module testing. As expected a general shift to lower ENC can be seen when operating at lower temperatures, while the threshold tuning is not impacted by a change in module temperature. Measurements using radioactive sources are inherently more complicated with a structure as large as the demonstrator. Using mounts for radioactive sources on motor stages, source scans could be performed for the full demonstrator using only two Sr90 sources moved along the full longeron over several hours. In Figure 5.12 the resulting occupancy map is shown for the A-side dual chip modules. The corresponding measurement for the C-side quad chip modules can be found in [63]. These measurements were obtained with the largest SP prototype to date, utilizing 6 parallel SP chains, giving the closest representation of the future ITk pixel detector in a system test context so far.
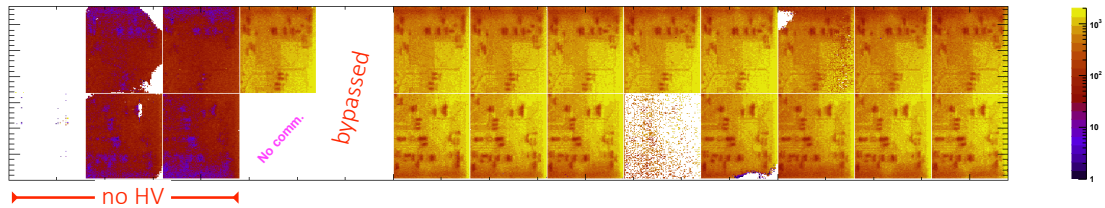
Figure 5.12: Source scan with a Sr90 radioactive source of the *A*-side double chip modules of the final demonstrator [63].

5.1.3 Conclusion and Outlook

The OBD program was a large scale effort for prototyping all the required steps in assembly, integration and operation of a serially powered pixel detector as will be found in the ITk pixel detector. Despite the limitations implied by the outdated ROC architecture, which is not representative for the future ITk pixel detector, significant lessons could be learned from the campaign.

The Small Electrical Prototype was the predecessor of the OBD demonstrator and was used to commission the infrastructure, DCS and DAQ of the OBD. A promising concept for the integration of modules on local support structures could be tested and verified. The accessibility of the smaller scale of the prototype allowed a more fluent development of the DCS and the prototype as a whole, which was highly beneficial to the final OBD integration. Although limited in its size, the Small Electrical Prototype was at the time the largest scale SP test setup considering the significant infrastructure attached to the prototype. This enabled the system test community to learn many valuable lessons about integrating and operating a serially powered pixel detector with all its bells and whistles. Many of these lessons had a direct influence on the development within the RD53 collaboration. Most prominently the required feature list of the Shunt-LDO for ITkPix was extended significantly to tackle several issues discovered in the Small Electrical Prototype. Additional measurement campaigns were conducted to follow up on experiences gained with the Small Electrical Prototype, especially concerning the HV distribution and potential requirements for a low-ohmic HV off mode.

The full OBD expanded on the numerous lessons learned already while bringing system test for ITk pixel to a scale suitable for exercising the later production stages, culminating in the largest serial powering prototype built to date. For such a project to succeed it is vital that all pieces are coming together. Confirming and expanding upon measurements performed with the Small Electrical Prototype, the OBD presented a unique test bed for many efforts related to ITk pixel, from DCS development to DAQ qualification. The infrastructure developed around the demonstrator will be further used in the near future on the path towards
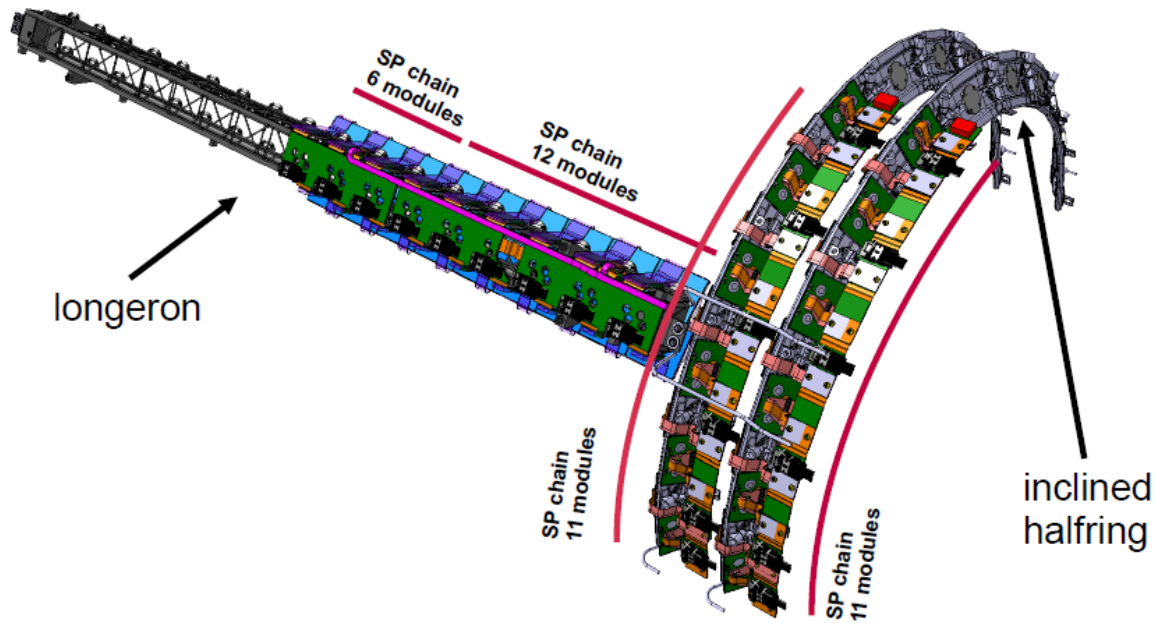
Figure 5.13: CAD drawing of the planned ATLAS ITk pixel Combined Slice system test. The combined slice will consist of a flat section on a longeron and two half rings with inclined modules [52].

the next step in ATLAS ITk OB pixel system test, the Combined Slice.

The Combined Slice will be an up-to-date, full-scale prototype including loaded local supports of the OB subsystem and will be initially loaded with RD53A modules. Similar to the concept introduced in section 5.2, the ability to replace RD53A modules with ITkPix modules once available in sufficient quantities is foreseen. A CAD drawing of the planned Combined Slice is shown in Figure 5.13. Based on the proven procedures developed in the OBD program, the integration chain for the OB in ITk Pixel will be prototyped and finalized in the scope of the Combined Slice system test.

5.2 Setup of a Serial Powering Prototype with RD53A Modules

In order to study low level serial powering system aspects, such as HV distribution or the Shunt-LDO supply current headroom, a small prototype with representative, current generation RD53A pixel modules has been scoped, set up and characterized in the context of this thesis. This prototype consists of up to 8 RD53A modules connected in series on a support structure, multiple of which can be daisy-chained to achieve longer SP chains. A single stave loaded with 8 quad chip modules is shown in Figure 5.14. To allow for better monitoring of the modules and a more flexible readout, dedicated services are used in this prototype, which, while electrically representative, do not have to comply with ITk pixel production services. The services, design goals and the DAQ scheme are covered in Section 5.2.2.

The indicator of the performance of a SP chain is the performance of the modules. This module performance is judged based on certain figures of merit including, but not limited to, the detection threshold dispersion after tuning, amount of noisy pixels as well as the electrical noise of the AFE. For RD53A, a detailed study of the performance of the three different AFE is found in [20]. In Section 5.2.1 the RD53A modules used in the scope of this prototype are introduced.

Finally in Section 5.3 the performance of the full SP chain is evaluated and put into context of stand-alone module operation by means of module performance measurements and studies of the electrical behaviour of the module, focused on the Shunt-LDO. Limitations of the system with RD53A modules and potential improvements in a future prototype using ITkPix modules are discussed in Section 5.3.6.

5.2.1 An RD53A Quad Module for Serial Chain Operation

The results presented in this chapter have all been obtained from measurements of RD53A quad modules with a dedicated serial powering flex covered in the following. The modules themselves can be loosely categorized as digital modules and fully functional modules. A fully functional quad module consists of four ROC bump bonded to a common silicon sensor tile, while a digital module is electrically mostly identical to a fully functional module but lacks a Si sensor. Both flavours of modules are assembled using the same module flex PCB.

Performance and characterization measurements of RD53A ROC were for the most part performed in LDO mode. In this mode of operation, the ROC is supplied by the on-chip Shunt-LDO. The shunt regulator of the Shunt-LDO can be deactivated by pulling a dedicated shunt enable pin to the regulator ground. The Shunt-LDO then effectively becomes a typical LDO regulator. Without the shunt regulator this requires the full chip to be supplied by
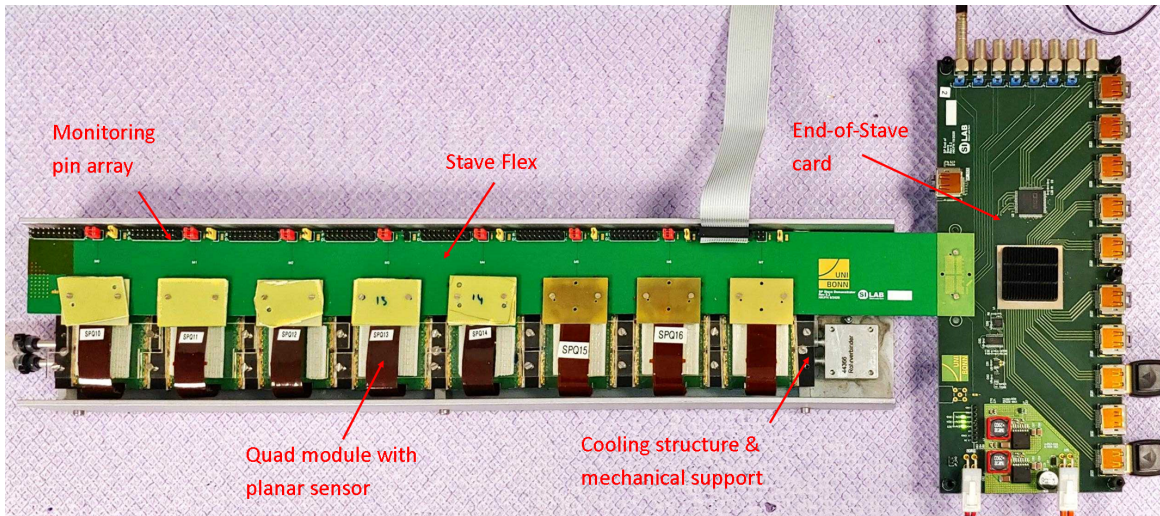
Figure 5.14: RD53A planar serial powering chain loaded with RD53A quad modules on dedicated flex PCBs.

a constant supply voltage $V_{\text{in}} = V_{\text{DD}} + V_{\text{do}}$ compared to the constant current used in a SP chain. Such a voltage based operation is more reliable though, as the issues observed with the RD53A Shunt-LDO, see Section 4.2.1, are tied to the necessity of creating a sufficiently large voltage drop V_{in} over the regulator.

A first step towards the evaluation of RD53A modules in serial chain operation is thus a comparison of chip performance between LDO and Shunt-LDO modes of operation, expecting a very similar performance. Any impact on the module performance in shunt mode can be identified this way. For example the increased power dissipation of the ROC in the shunt regulator can lead to an increased chip temperature, which would directly translate to an increase in noise. Such studies should be performed with digital modules or bare ROC, as a Si sensor connected to the AFE has a significant impact on the module performance figures, typically resulting in significantly increased noise of the AFE. The full picture of the module performance can then be achieved by comparing the performance of a fully functional module in both LDO and Shunt-LDO mode. Here the additional power dissipation in the Shunt-LDO should have a more pronounced effect on the noise of the AFE: in addition to the direct contribution to the AFE ENC, the increase in temperature would lead to a larger sensor leakage current, which in turn further increases the ENC.

The RD53A Serial Powering Quad Module Assembly

The typical stack up of the quad modules used in the context of this thesis can be seen in Figure 5.15. The bare module, consisting of four ROC bump bonded to a large Si sensor tile.

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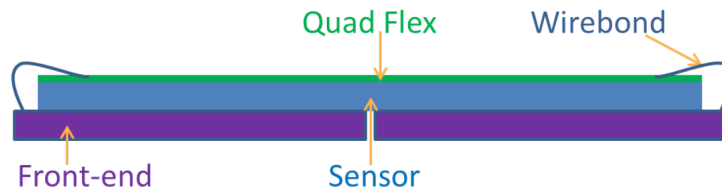
Figure 5.15: Schematic cross section of an assembled RD53A quad module as used in the context of this thesis. The flex is glued to the bare module. Wire bonds provide interconnection between ROC and the flex PCB, which provides an interface for the DAQ.

The sensor tile is dimensioned for full size readout chips compared to the half sized RD53A chips and thus cover an area of roughly $4\,\mathrm{cm} \times 4\,\mathrm{cm}$. The RD53A dies bump bonded to such a sensor are typically cut to the final chip size, approximately $2\,\mathrm{cm} \times 2\,\mathrm{cm}$, in order to exercise the flip chip and module assembly process with more realistic module sizes. The resulting quad module has the same dimensions as are expected for the ITkPix production modules. As an additional benefit the larger dies provide a greater surface area for the cooling system which is required to keep the module at an acceptable temperature in Shunt-LDO mode of operation. On the other hand, half of the module surface area is not covered by active readout electronics. The digital quad module imitates this stackup, replacing the bare module with four single ROC glued to a glass dummy with approximate sensor dimensions and thermal expansion coefficient. Consequently the digital quad is mechanically and electrically very similar to the fully functional module while being less resource intensive. It is thus very well suited for commissioning of the SP prototype and its services. The core part of these services is the module flex shown in Figure 5.16.

This three layer flex PCB is a descendant of the dual chip flex PCB used in the hybridization market survey, see [20], yet offers a different feature set due to the different scope of the prototype. Different from the dual chip module flex, this PCB offers a multitude of monitoring lines to allow the important electrical characterisation of the module. These lines include sense lines for the module input potential V_{in} and the local module GND as well as the NTC mounted on the flex. For each of the four chips a sense line for V_{DDA} and the on-chip voltage multiplexer V_{Mux} is available. V_{DDD} is not routed out of the module in favour of V_{Mux}. This design choice was deemed reasonable as RD53A operation has been shown to be more sensitive to V_{DDA} and since V_{DDD} is still available via the voltage multiplexer. Furthermore the low terminal of each of the 8 slope resistors R_{ext} on the module is accessible with sense lines. With these sense points an accurate measurement of the offset voltage V_{ofs} of any Shunt-LDO can be performed, as it reflects the actual V_{ofs} present in the circuit, see Figure 4.23. The amount of monitoring lines comes at the cost of routing space and connector pins, limiting the available data links for each of the 4 ROC on the module. Out of the 4 available high

Figure 5.16: Flex PCB used for the RD53A quad chip assembly for the SP prototype.

speed data lanes per ROC, only one lane is routed per ROC, which is completely sufficient for this prototype. This further fits the readout system of choice, BDAQ53 [20, 65], which offers up to 7 high speed links. In addition none of the HitOr lines, 4 of which are available per chip as LVDS, is routed from the flex. This limits the feasibility of tests with radioactive sources significantly, but is an acceptable trade-off given the different focus of these modules. The large amount of monitoring lines was not feasible with the original flex connector used on the dual chip module flex and was replaced with a compression interposer[2]. This new connector choice additionally offered a much better mechanical reliability compared to the connectors used on the dual chip module flex. To test individual quad chip modules on a desktop test bench, a dedicated adapter card was designed in [50] and used extensively for module testing.

Working Point of the Shunt-LDO

The working point of quad modules in a SP chain needs to be chosen carefully to achieve a balance between realistic conditions and reliability. As shown in Figure 3.6 the powering efficiency of the Shunt-LDO suffers significantly if a large current headroom is chosen. Since analog and digital domain of the RD53A have different current consumptions, choosing the same value for R_{shunt} is not efficient and would lead to an unnecessarily large current headroom in the Shunt-LDO drawing less current. A module voltage of 1.5 V should not be undercut as RD53A operation in Shunt-LDO mode has shown to be unreliable at lower voltages. The offset generating resistors R_{ofs} were chosen to reach a target offset voltage of $V_{\mathrm{ofs}} = 0.9$ V. Based on measurements of the current consumption of both analog and digital domain a total supply current of $I_{\mathrm{in}} = 1.1$ A is targeted. This current includes a headroom of 20 % and is approximated best by loading slope resistors R_{shunt} for the analog and digital Shunt-LDO as 1 170 Ω and 1 080 Ω respectively, restricted by the actually available resistor sizes with a sufficiently high precision ≤ 0.1 %.

Ideally this would equate to an effective module input impedance $R_{\mathrm{eff}} = 0.14$ Ω, however, with the known deviation in the Shunt-LDO current mirror ratio k, the actual R_{eff} of such a module will be larger. Using the average k values from wafer probing for both analog and

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[2] Samtec Z-Ray ZA1 Series

Parameter	Target
$I_{\text{Module, Min}}$	3.67 A
V_{ofs}	0.9 V
R_{eff}	0.14 Ω
I_{Module}, SP chain	5 A
V_{Module}, SP chain	1.6 V

Table 5.1: Working point of the RD53A quad modules used in the context of this thesis. $I_{\text{Module, Min}}$ refers to the estimated current consumption of an RD53A quad module with no current headroom. I_{Module} and V_{Module} denote the working point used for measurements presented in this thesis.

digital domain, $k_{\text{A}} \approx 938$ and $k_{\text{A}} \approx 931$, such a module is expected to have an effective input resistance $R_{\text{eff}} \approx 0.145\,\Omega$. Ultimately, since R_{eff} is very sensitive to the k factors of each of the 8 involved Shunt-LDO and k shows a rather wide distribution in the order of 5 %, a more precise estimate of R_{eff} can only be made on module level with wafer probing data of the four ROC forming the quad module.

The working point chosen for the quad modules used in this work includes an additional current head room. As the majority of measurements of RD53A chips in LDO mode were performed at a module input voltage of 1.6 V, the nominal chain current was increased to 5 A to achieve the same module input voltage. The target parameters for module offset and input impedance, the estimated baseline current consumption of the quad chip module and the ultimately set working point of the RD53A quad modules are listed in Table 5.1.

Module Performance in Shunt-LDO Mode

The performance of the RD53A modules is quantified based on the threshold performance of the module after tuning to a target threshold. Prior to such a threshold tuning, the Shunt-LDO reference voltages need to be trimmed such that $V_{\text{DDA}} = V_{\text{DDD}} \approx 1.2$ V. For all modules used in the context of this work, the available wafer probing data provided the optimal settings for V_{refA} and V_{refD}. Afterwards the general functionality of the module is ensured by means of a digital and analog scan. An example of this shown in Figure 5.17. In both scans 100 test injections were performed in the digital and analog part of the ROC respectively. The figure of merit in this measurement is the response of the ROC. In case of a fully functioning chip, 100 detected hits per pixel are expected. For analog test injections this is only the case if the amount of charge injected into each pixel is significantly larger than the detection threshold. For an RD53A quad module this corresponds to a total of 30 720 000 hits. As

(a) Digital scan.
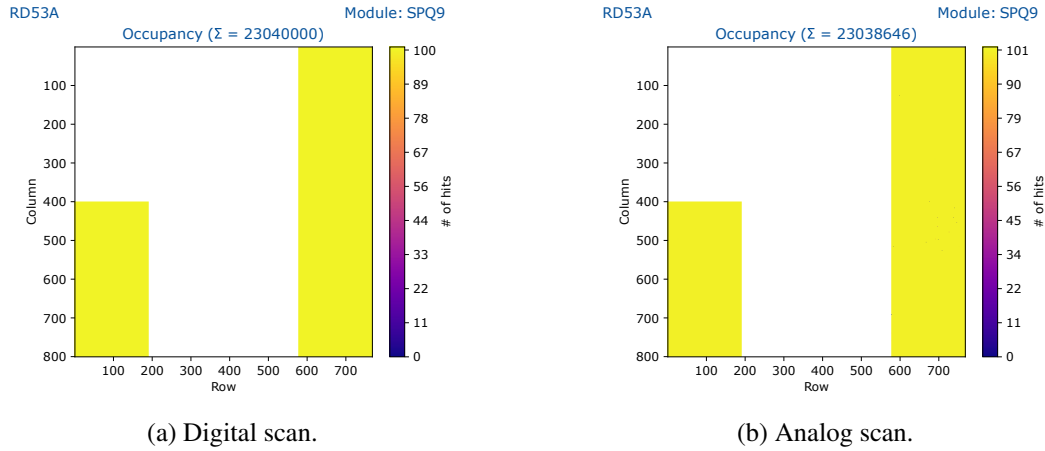
(b) Analog scan.

Figure 5.17: Digital and analog scan of digital quad SPQ9.

discussed before, the sensor covers an area roughly twice as large as the ROC. With the sensor sized plotting used, which conserves the aspect ratio and module geometry, this leads to an empty region in the center 384 rows of the module. In Figure 5.17(a) and Figure 5.17(b) an additional faulty area can be seen in the top left corner of the module. Due to a production error in the first production run of the module flex this chip was not operational and could not be read out: due to a missing connection the power-on-reset of this ROC was not triggered, leaving the chip unusable. This leaves 230400 active pixels on this module. The digital scan shows a perfect response with every pixel recording a total of 100 hits. In the analog scan only 28 pixel recorded less than 100 hits, yielding an overall good operating performance of the module. Following these measurements the module is tuned to a detection threshold of $1\,000\,e^-$ in the LIN and DIFF AFE. The SYNC AFE is omitted here. This is based on the front-end choices for the future ITkPix and CROC, which will use only the DIFF and LIN AFE respectively. Figure 5.18 shows the threshold distribution of SPQ9 after tuning, the ENC can be seen in Figure 5.19. Both AFE can be tuned nicely to the target threshold with only a limited number of pixels failing the tuning procedure, denoted as failed fits. In agreement with the expectation [20], the DIFF AFE shows both a smaller threshold distribution and lower ENC compared to the LIN AFE. The visible tail in the noise distribution of the DIFF AFE is a consequence of a design bug in the DIFF AFE which negatively impacts the performance of the AFE, refer also [20, 46].

Compared with test results during RD53A chip characterization, the threshold performance of SPQ9, operated in Shunt-LDO mode, shows promising results. The threshold performance and ENC are compared in Table 5.2 and Table 5.3 respectively. As a reference measurements published in [20] of both LIN and DIFF AFE are used. These measurements were performed on single RD53A chips operated in LDO mode. As an additional reference point measurements
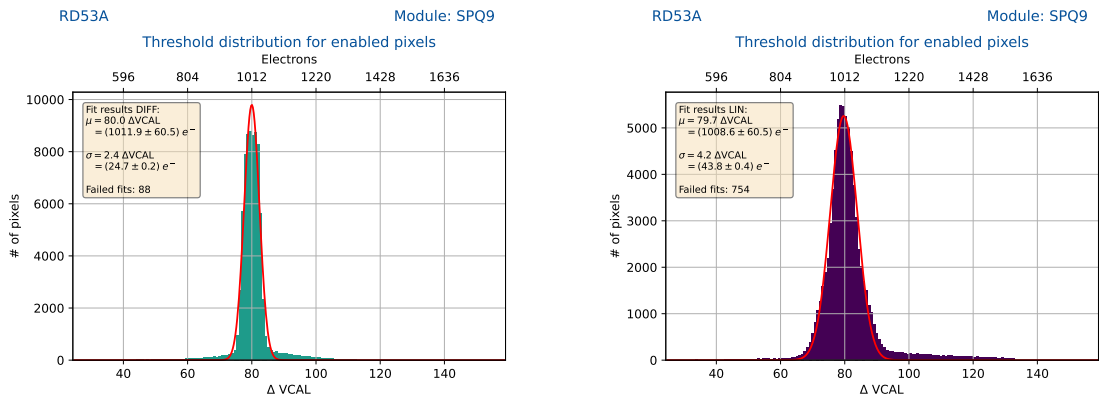
(a) Threshold distribution of digital quad SPQ9, DIFF AFE, after tuning to a target threshold of $1\,000\,e^-$.

(b) Threshold distribution of digital quad SPQ9, LIN AFE, after tuning to a target threshold of $1\,000\,e^-$.

Figure 5.18: Threshold distribution for all enabled pixels in SPQ9, LIN and DIFF flavours, after tuning to $1\,000\,e^-$

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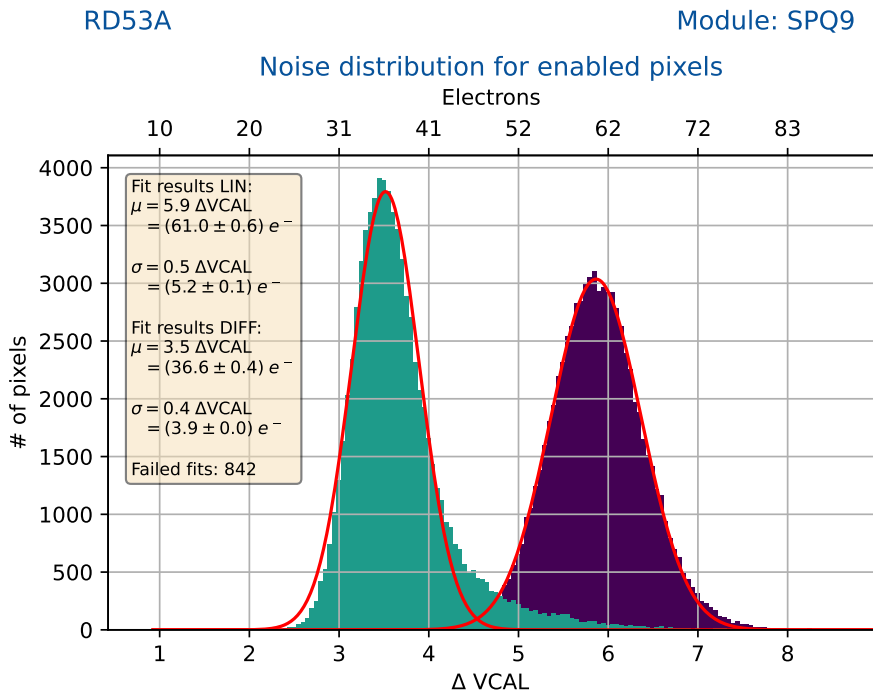
Figure 5.19: ENC distribution of digital quad SPQ9, LIN and DIFF AFE, after tuning to a target threshold of $1\,000\,e^-$.

	Reference LDO[20]	SPQ9 Shunt-LDO	Q4 Shunt-LDO[66]
Threshold mean LIN AFE	$(1\,008 \pm 61)\,e^-$	$(1\,009 \pm 61)\,e^-$	$(1\,009 \pm 61)\,e^-$
Threshold width LIN AFE	$(43.0 \pm 0.4)\,e^-$	$(42.0 \pm 0.4)\,e^-$	$(42.9 \pm 0.4)\,e^-$
Threshold mean DIFF AFE	$(1\,014 \pm 61)\,e^-$	$(1\,012 \pm 61)\,e^-$	$(1\,013 \pm 61)\,e^-$
Threshold width DIFF AFE	$(26.0 \pm 0.4)\,e^-$	$(25.0 \pm 0.2)\,e^-$	$(25.8 \pm 0.2)\,e^-$

Table 5.2: Threshold performance comparison of RD53A digital quad module SPQ9 in Shunt-LDO mode with reference measurements in LDO mode performed in [20]. As an additional reference measurements of an RD53A digital quad module with a different flex PCB, also operated in Shunt-LDO mode and performed in [66], is given. All chips tuned to a detection threshold of $1\,000\,e^-$.

	Reference LDO[20]	SPQ9 Shunt-LDO	Q4 Shunt-LDO[66]
Noise mean LIN AFE	$(56 \pm 1)\,e^-$	$(61.0 \pm 0.6)\,e^-$	$(59.3 \pm 0.6)\,e^-$
Noise width LIN AFE	$(3.0 \pm 0.1)\,e^-$	$(5.3 \pm 0.1)\,e^-$	$(4.45 \pm 0.04)\,e^-$
Noise mean DIFF AFE	$(39.0 \pm 0.4)\,e^-$	$(36.6 \pm 0.4)\,e^-$	$(38.6 \pm 0.4)\,e^-$
Noise width DIFF AFE	$(4.0 \pm 0.4)\,e^-$	$(3.90 \pm 0.04)\,e^-$	$(4.29 \pm 0.04)\,e^-$

Table 5.3: ENC comparison of RD53A digital quad module SPQ9 in Shunt-LDO mode with reference measurements in LDO mode performed in [20]. As an additional reference measurements of an RD53A digital quad module with a different flex PCB, also operated in Shunt-LDO mode and performed in [66], is given. All chips tuned to a detection threshold of $1\,000\,e^-$.

from the module testing site qualification performed in [66] are given as well. These measurements were performed with a digital RD53A quad, Q4, which was assembled with the ATLAS RD53A common hybrid flex PCB, an early prototype of the later production design for ITkPix. The corresponding results from SPQ9 and Q4, both operated in Shunt-LDO mode, are in good agreement with the reference measurement. The threshold performance can be considered equal between the three different candidates. The ENC comparison shows good agreement as well with small differences between the different ROC. Due to the significant increase in power dissipation when operating a module in Shunt-LDO mode, an increase in ENC due to self heating would be expected. With both SPQ9 and Q4 being operated on large heat sinks the temperature difference with respect to single chip measurements in LDO mode is in the order of $10\,^\circ$C. For temperature differences in this order of magnitude measurements[66] suggest a barely resolvable increase in ENC. All in all operating an RD53A in Shunt-LDO mode yields a very comparable performance compared to available references

(a) Digital scan.
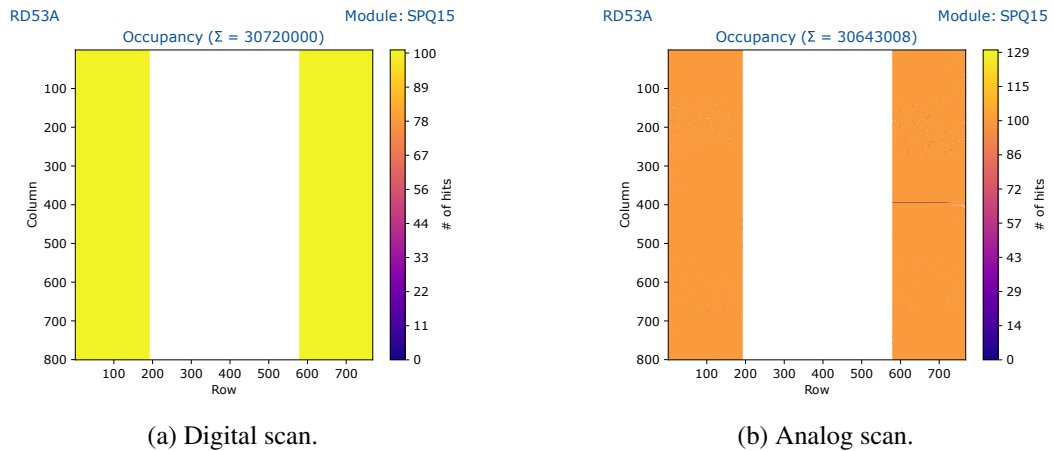
(b) Analog scan.

Figure 5.20: Digital and analog scan of digital quad SPQ15.

and experience.

As a next step the performance of a fully functional module can be put into context. These modules use planar n-in-p Si sensors, a proven sensor technology also in use in the current ATLAS pixel detector. During operation of these modules a reverse bias voltage $\geq 70\,\mathrm{V}$ is applied to ensure full depletion of the sensor. As a sensor adds additional capacitance at the input pad of each pixel the ENC of the AFE is expected to increase. The threshold performance is expected to be compatible with the performance of digital modules. Digital and analog scans of module SPQ15, operated in Shunt-LDO mode, are shown in Figure 5.20. The analog scan shown in Figure 5.20(b) was performed with the Leakage Current Compensation (LCC) of the DIFF AFE being used. If no LCC is used, the DIFF AFE is largely dysfunctional in the peripheral rows as shown in Figure B.1. This was unexpected as the LCC is only required to prevent saturation of the pixel inputs in the DIFF AFE for per pixel leakage currents exceeding $10\,\mathrm{nA}$, which corresponds to a total leakage current of $3\,\mathrm{mA}$ for the full module. In contrast the actual leakage current of such a module is in the order of $100\,\mathrm{nA}$ as can be seen from Figure 5.21.

Even with the LCC enabled the analog scan of SPQ15 still shows a faulty column in the SYNC AFE of one ROC. Disregarding this exception the module shows a mostly homogeneous response as can also be seen in Figure 5.22.

In Figure 5.23 the threshold performance, ToT response and ENC of SPQ15 is shown. As expected the threshold performance is in good agreement with measurements of digital quad modules. The very high noise especially in the LIN AFE is a consequence of the sensor design and the multiple different AFE included in RD53A. Due to the usage of a bias resistor in the bias grid of the sensor, an additional leakage current can flow from the pixel inputs of one AFE. This interplay between sensor design and RD53A is also the reason for the
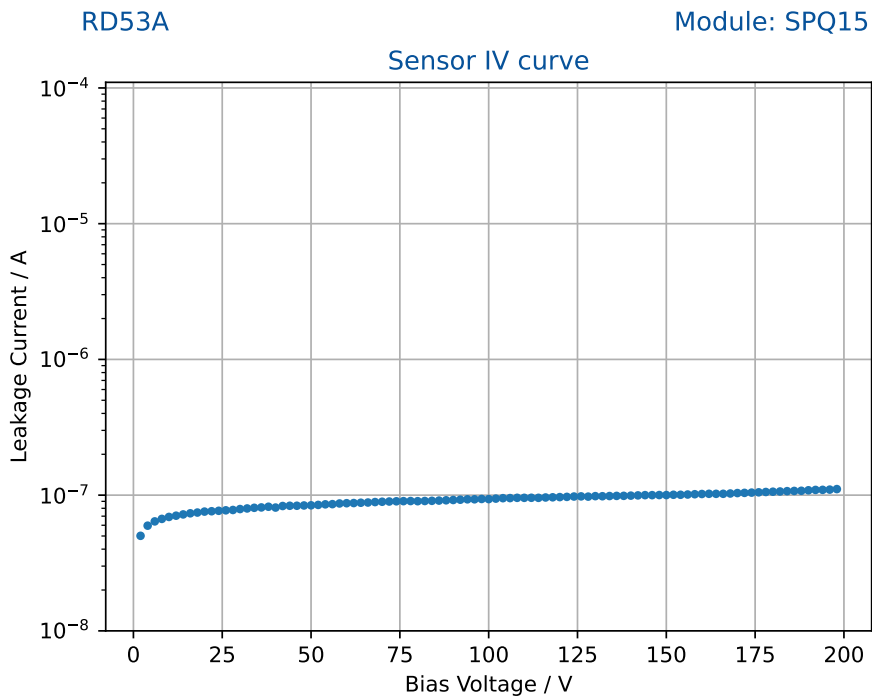
Figure 5.21: SPQ15 sensor IV curves measured during reception tests.

necessity of using the LCC in the DIFF AFE [67].

   In general it can be said that for both digital and fully functional modules the Shunt-LDO does not cause a performance degradation, which allows the modules in a serial powering chain to be benchmarked with respect to widely available experience with single RD53A chips operated in LDO mode which will be further pursued in Section 5.3.

5.2.2 Services and Periphery

Next to the modules used the services and periphery of the SP chain are an integral part of the prototype. These include the module flex covered before, the stave flex and End-of-Stave (EoS) card, the power supplies, cabling and DAQ. For a stave loaded with 8 quad modules, a single adapter card with connections to all modules, which provides interfaces to the DAQ, would quickly become unwieldy and inflexible. Instead a similar approach to the design of large pixel detectors like ATLAS pixel is chosen. In this approach, the modules are connected to a stave flex, also referred to as type-0. This stave flex provides routing of all module up- and downlinks and distributes LV and HV to the SP chain. Without direct interfaces to the DAQ the stave flex can be comparably compact. For each module the stave flex offers a set of
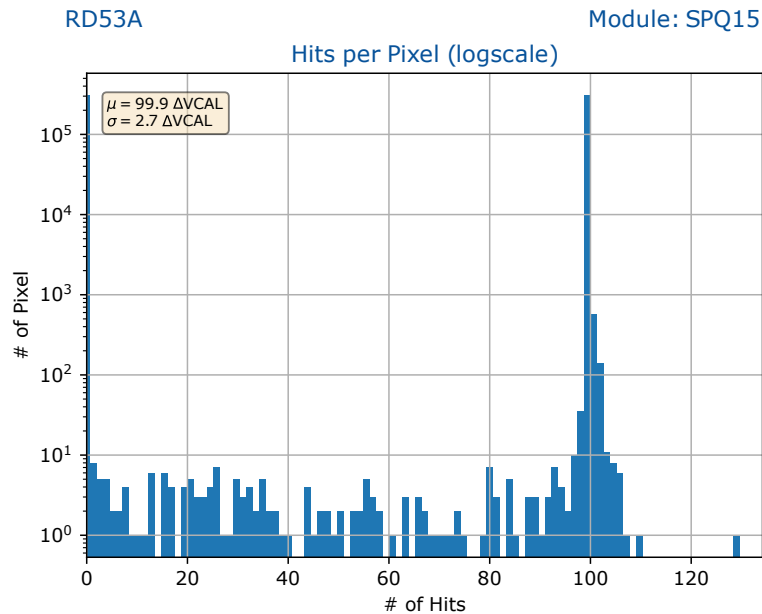
Figure 5.22: 1-D occupancy histogram of Figure 5.20(b). Module dimensions are defined by the sensor, 768×800 pixel. The center 384 rows not covered by any ROC are included in the 0-bin.

monitoring pins for all sense lines discussed in Section 5.2.1. An additional line distributes the $\mathrm{LP_{En}}$, see Section 4.3, signal to all modules, but is not used for RD53A modules. A photograph of the stave flex used in this prototype can be seen in Figure 5.24.

Using the same connector as the module connector, the stave flex can be connected to the EoS card, loosely corresponding to PP0 in ATLAS pixel. This EoS card acts as the interface between the quad modules, the DAQ and power supplies and defines the system GND potential and is shown in Figure 5.25. The system GND can be directly connected to the LV return line, ensuring the module with the lowest local GND having the system GND as the reference potential. Alternatively the system GND can remain decoupled from the LV return, which allows daisy chaining of multiple of these SP chains. As studies of different HV schemes and their impact on the SP chain performance is a focus of this prototype, the HV distribution can be customized on the EoS card using dedicated jumpers. Between a common HV supply line and return line and dedicated HV connections for each modules any configuration can be chosen. By default the HV is referenced to the EoS GND potential. With every module's local GND available on the stave flex however any local module GND can be used as a reference for a HV supply group instead.

With a design SP chain length of 8 quad chip modules, each with a single data link per ROC, the DAQ would need to be able to handle 32 high speed data links in parallel, which
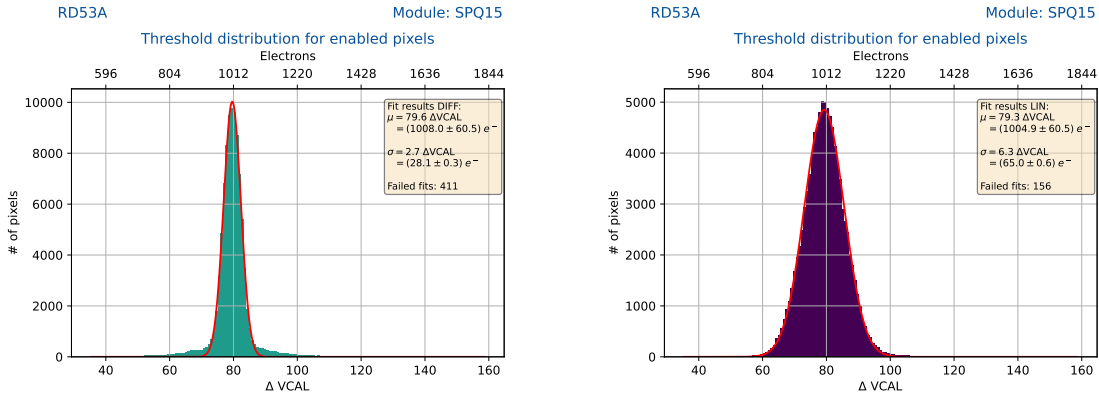
(a) Threshold distribution of SPQ15, DIFF AFE, after tuning to a target threshold of $1\,000\,e^-$.

(b) Threshold distribution of SPQ15, LIN AFE, after tuning to a target threshold of $1\,000\,e^-$.
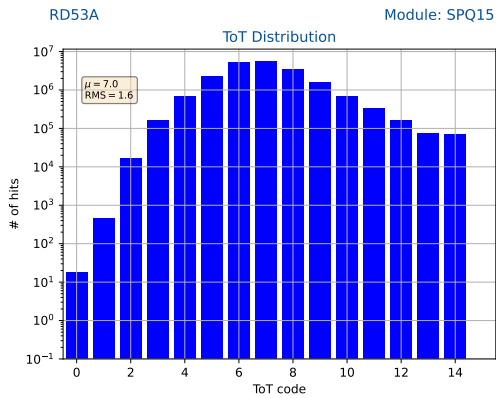
(c) ToT distribution of both LIN and DIFF AFE after tuning to a target threshold of $1\,000\,e^-$. Target ToT of 7.
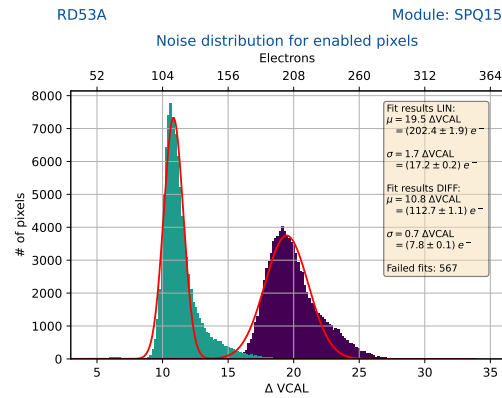
(d) ENC distribution of SPQ15, LIN and DIFF AFE, after tuning to a target threshold of $1\,000\,e^-$.

Figure 5.23: Threshold distribution and ENC for all enabled pixels in SPQ9, LIN and DIFF flavours, after tuning to $1\,000\,e^-$. Furthermore, ToT response to a reference charge injection after tuning to $1\,000\,e^-$ and a ToT target of 7.

poses a significant challenge. During the design phase of the prototype, no readout system able to handle such a large amount of ROC was available for use. Using several small scale DAQ systems in parallel was deemed not economical while providing little benefit. Instead a more modular approach, based on the BDAQ53 system, was chosen. As mentioned above, BDAQ53 can reasonably support a single quad module with 4 data links operating at a speed of $1.28\,\mathrm{Gb\,s^{-1}}$. Using two digital crosspoint switches [68, 69] the up- and downlinks of the SP chain are dynamically routed on the EoS card. A 16×16 switch takes up to 16 different CMD inputs and distributes them fully configurable to the 8 modules via the stave flex. The usual configuration consists of a single CMD input which is either routed to only one module

Figure 5.24: Stave flex of the RD53A serial powering prototype.
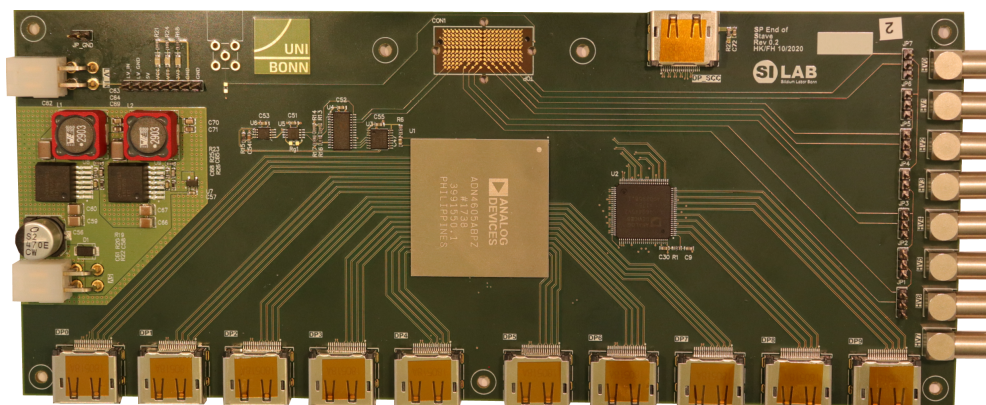
Figure 5.25: EoS card of the RD53A serial powering prototype.

or copied and distributed to all modules in parallel. An additional 40×40 switch has all 32 data links as inputs and can route any 4 data links through one DisplayPort connector as an output to the DAQ system. In usual operation the data links from a single module are forwarded to the DAQ whilst the remaining data links are terminated in the crosspoint switch. Additional outputs are available as well, allowing e.g. the usage of multiple BDAQ systems in parallel or observation of the data links forwarded to the DAQ on an oscilloscope, which is very helpful for debugging purposes. Both crosspoint switches are controlled using the I^2C interface embedded in the BDAQ53 hardware. In Figure 5.26 a schematic overview of the routing on the EoS card and the connection to the readout system is shown.

In order to monitor module voltages as needed e.g. for Shunt-LDO related measurements, a set of four small 4-channel 16 bit analog-to-digital converter (ADC)[70] is used. These ADC are controlled via I^2C by a Raspberry Pi. This approach is advantageous as it allows the I^2C reference voltage to be equal to any reference voltage instead of the system GND, since the ADC are limited to an input voltage $\leq 6\,\mathrm{V}$ with a lower input voltage range providing better resolution. A 20-pin ribbon cable is used to connect the pin header of any module on the stave flex to a breakout board populated with the ADC.

The LV is supplied by a prototype candidate for the future ITk pixel current sources. Thus this setup is the first serial powering prototype supplied by a dedicated current source optimised for operation in a serially powered pixel detector. The design requirements for this current source are listed in Table 5.4 Preliminary tests with RD53B Shunt-LDO prototype
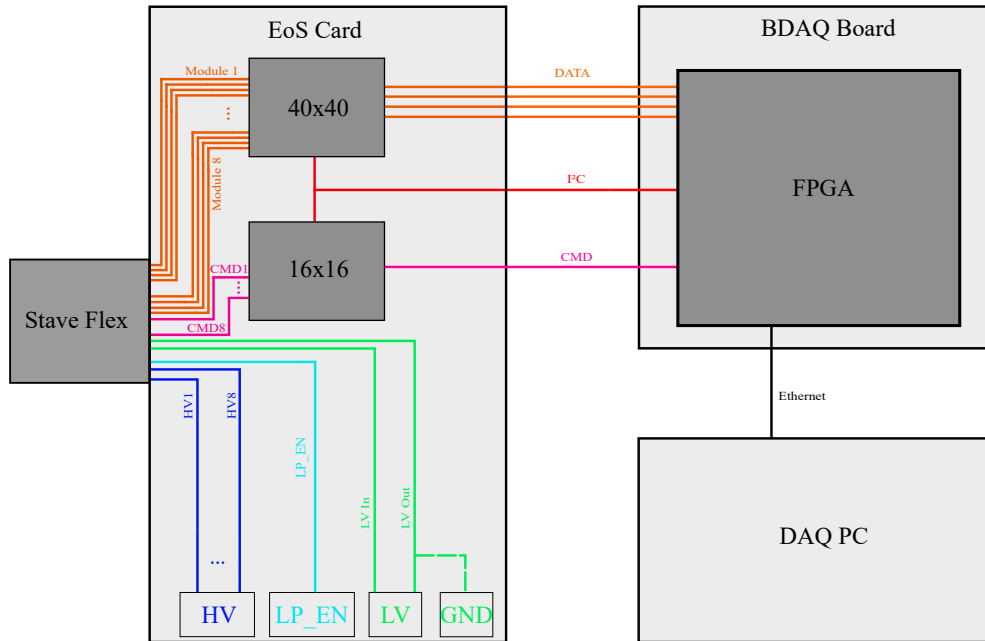
Figure 5.26: Functional overview of the EoS card in the context of the SP prototype including readout scheme. The EoS card distributes LV, HV and LP$_{EN}$ to the SP chain. Module readout is accomplished using two digital crosspoint switches. A 16×16 switch distributes a CMD input towards any combination of modules. A 40×40 switch selects any 4 ROC from the SP chain and forwards their data links to the DAQ. Auxiliary interfaces to power the EoS card are not shown.

DC Output Current	0.4 A - 10 A
DC Output Voltage	0 V - 50 V
DC Output Power	300 W
Current Ramp Rate	$1\,\mathrm{A\,s}^{-1}$ - $10\,\mathrm{kA\,s}^{-1}$
Noise	< 0.7 % PP @ 8 A
Current Regulation ± 0.25 % load	< 0.5 ms

Table 5.4: Specifications of the current source prototype supplying the SP prototype.

chips showed some initial issues with the performance of the current source, especially concerning higher than expected output noise. These were quickly rectified, yielding a power supply largely fulfilling the initial requirements set for an ITk pixel current source.

5.3 Characterisation of a Serial Powering Chain with Planar RD53A Quad Modules

Before a module is integrated into the SP stave it is subjected to a series of reception test measurements to ensure general functionality and get first impressions of the performance figures of the module. These tests are typically done in a dedicated setup and potentially different environmental conditions. The reception tests for the modules used in the SP prototype discussed here have been performed in the context of a master thesis [50], as such only a brief overview of core results is given here.

A first set of measurements covered here are the electrical characteristics, driven by the Shunt-LDO, of the quad modules in the serial powering chain. These cover the module IV characteristic, current sharing between the different Shunt-LDO and studies of the current headroom required for module operation in order to verify the choice of the Shunt-LDO working point for RD53A modules in a SP chain.

Following the performance of the SP chain is evaluated with respect to the baseline performance figures established in this chapter. Based on this evaluation, different schemes for the HV distribution are considered.

5.3.1 Quad Module Reception Tests

After module assembly and wire bonding, initial testing was performed for each quad module in a dedicated test setup [50]. After a first power up and general functionality test to establish successful communication with all involved ROC, the Shunt-LDO reference voltages V_{DDA} and V_{DDD} are trimmed to the target values using input from wafer probing. The global reference current I_{ref} of the AFE is set during the module wire bonding instead. Following measurements of the Shunt-LDO input IV curves and the sensor IV curves, the LIN and DIFF AFE of all ROC are tuned to detection thresholds of $1\,000\,e^{-}$. The threshold performance of the modules is measured as outlined before and can be seen in Figure 5.27.

With these measurements in place a preliminary yield assessment of the available quad modules can be made. While all modules are assembled using probed chips, the chip yield during wafer probing was determined without consideration of the Shunt-LDO [20]. Thus it is not necessarily expected that all Shunt-LDO of all modules considered here are fully

functional. Modules SPQ11, SPQ15 and SPQ18 showed very promising results. For the remaining 5 modules the following issues were found:

- **SPQ10** has one faulty Shunt-LDO, FE0 is not operational. The remaining chips are very noisy, such that tuning to the target threshold $1\,000\,e^-$ is not possible.

- **SPQ12** showed one not-responsive ROC, FE3, during reception testing.

- **SPQ13** has a sensor with very large leakage current. Module failed after tuning to a target threshold $\leq 1\,000\,e^-$.

- **SPQ14** showed one not-responsive ROC, FE2, during reception testing. LIN AFE has very high ENC.

- **SPQ16** showed one not-responsive ROC, FE3, during reception testing. Additionally the voltage multiplexer for FE0 and FE1 can not be read out. LIN and DIFF AFE have very high ENC.

No issues were found with SPQ11, SPQ15 and SPQ18 and the threshold performance of all functional ROC is within expectations. During integration of the quad modules in the SP chain it became clear that some of these observed issues were driven by the test system used. In the reception tests, a typical voltage source was used as a power supply. With a capability to provide an output current of 5 A this was deemed sufficient given the target working point of the RD53A quad modules of approximately 1.5 V for a module current of 4.4 A. However further testing showed a larger module current was needed to start up these chips. As the current source prototype used to supply the SP chain can supply currents of up to 10 A this issue can be overcome by an adapted startup procedure, which increases the SP chain current to 6 A before setting the nominal chain current of 5 A. Due to this all ROC except modules SPQ10 and SPQ13 could be fully utilized in the SP chain.

5.3.2 Electrical Characteristics of Modules

The electrical characteristics of the RD53A quad modules in the SP chain are driven by the on-chip Shunt-LDO. Using the on-chip voltage multiplexer and the measurement setup discussed in Section 5.2.2 the input IV curves of all Shunt-LDO on a module can be measured. Compared to the procedures used in Section 4.2 a somewhat different approach is necessary. Since the voltage multiplexer of RD53A is a crucial part of this measurement, with most voltages not available on dedicated sense lines, the ROC needs to be operational during the measurement. Thus the input current is ramped down from the previously mentioned startup current of 6 A to 4 A. While it has been established that any ROC would require a supply
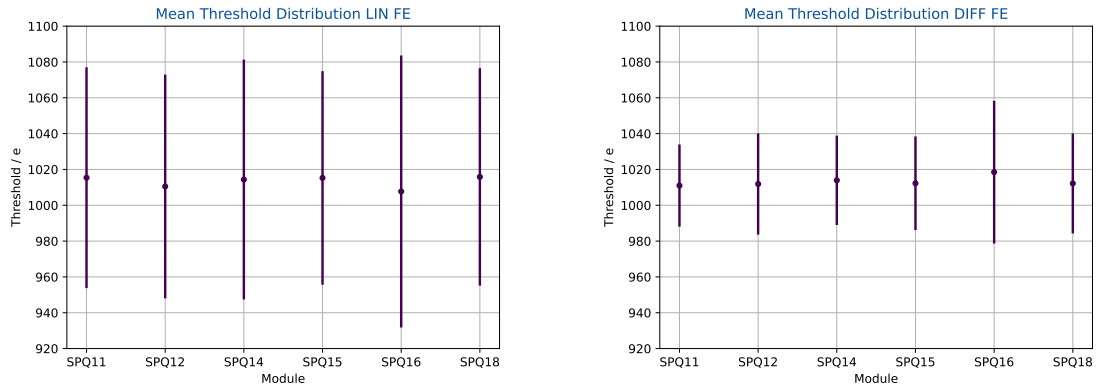
(a) Quad module reception: threshold distribution of LIN AFE, after tuning to a target threshold of $1\,000\,e^-$.

(b) Quad module reception: threshold distribution of DIFF AFE, after tuning to a target threshold of $1\,000\,e^-$.
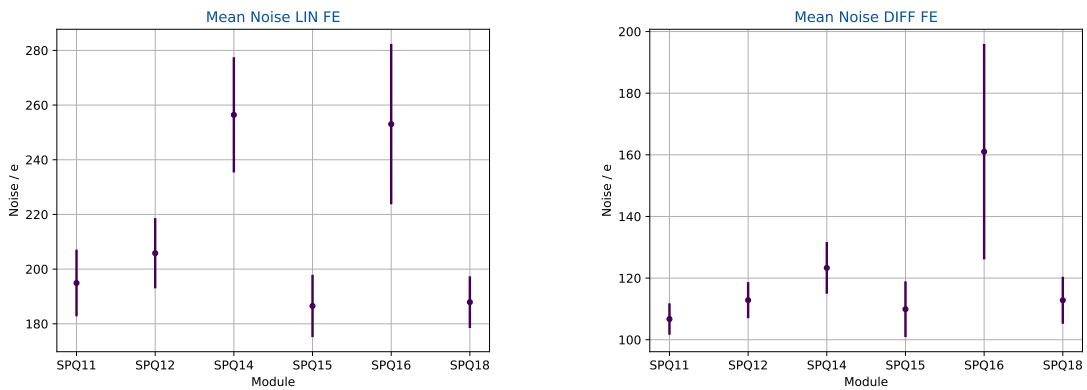
(c) Quad module reception: ENC of LIN AFE, after tuning to a target threshold of $1\,000\,e^-$.

(d) Quad module reception: ENC of DIFF AFE, after tuning to a target threshold of $1\,000\,e^-$.

Figure 5.27: Threshold distribution and ENC, LIN and DIFF flavours, after tuning to $1\,000\,e^-$. Modules SPQ10 and SPQ13 are not shown, as they could not be tuned to a threshold of $1\,000\,e^-$ successfully.
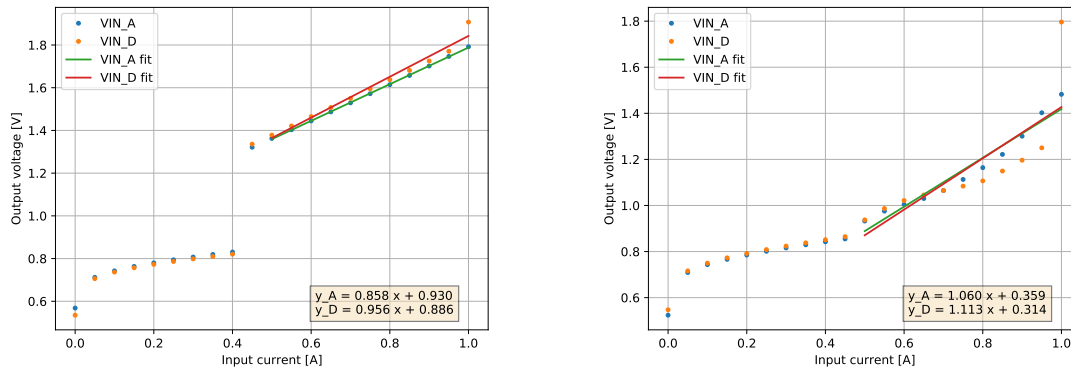
(a) Example of a good IV curve measurement from wafer probing. With proper selection of fit ranges R_{eff} and V_{ofs} can be determined.

(b) Example of a bad IV curve measurement from wafer probing. Extraction of R_{eff} and V_{ofs} is not possible, as no feasible working point is reached.

Figure 5.28: Examples for Shunt-LDO IV curves obtained from wafer probing.

current of approximately 1.1 A, this is only the case for a ROC configured for operation, with e.g. the full pixel matrix enabled. The actual current drawn during these IV curve measurements is lower.

Measurement of the Shunt-LDO IV curves using the on-chip multiplexer also offers advantages. V_{in} and GND, usually measured at the power connector of the test PCB or close to the wire bond pads, can now be measured as direct copies of the internal chip voltages. This provides a more accurate reference potential GND as well as voltage readings generally closer to the voltages actually seen by the Shunt-LDO. Furthermore this allows for a slightly more accurate trimming of V_{DDA} and V_{DDD}, which was performed prior to the Shunt-LDO IV curve measurement.

As mentioned before, an accurate estimate of the Shunt-LDO characteristic can only be given for any module at a time, provided wafer probing data is sufficient. With no direct measurements available for either the effective offset voltage or the current mirror ratio k in the wafer probing data set, an indirect approach is chosen similar to the procedure outlined in Section 4.2.1. In this approach both k and the offset voltage are obtained from the line fit on the input IV from wafer probing. The effective slope of analog and digital Shunt-LDO is then used to determine an estimate for k, referred to as k_{eff} in the following. The effective offset voltage gained from the wafer probing data is used to determine I_{ofs}, as R_{ofs} is well known. k_{eff} and I_{ofs} of all 8 Shunt-LDO are then used to model the expected input IV curve of the quad module. Unfortunately though the wafer probing data set is not complete for all modules available. This is mostly due to the aforementioned startup difficulties encountered for some of the Shunt-LDO. An example for such a behaviour is shown in Figure 5.28. For a ROC as shown in Figure 5.28(b) it is not possible to extract the effective slope R_{eff} or the
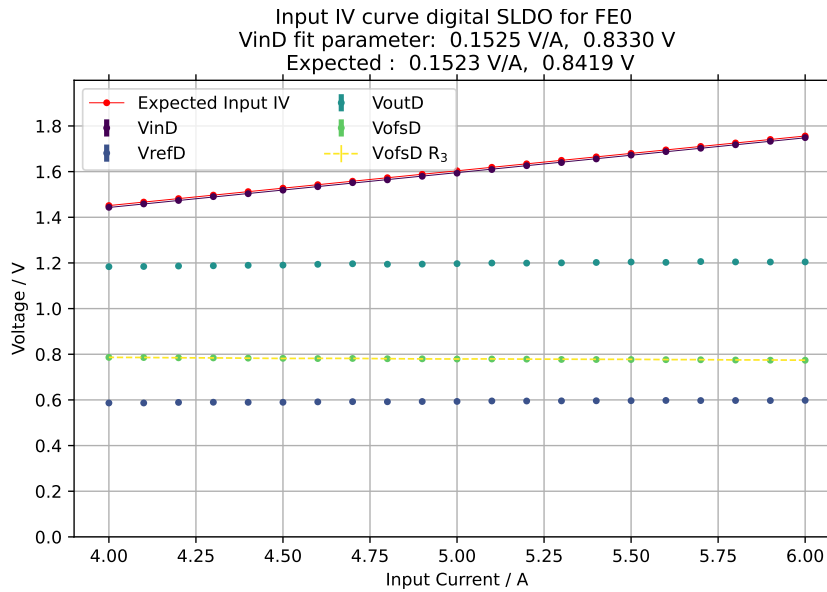
Figure 5.29: Shunt-LDO IV curve of the digital Shunt-LDO on SPQ14 FE0. Overlayed is the expected IV curve from wafer probing data. VofsD R_3 is the voltage measured at the lower terminal of R_{shunt} and is thus the offset voltage seen by the Shunt-LDO.

offset voltage V_{ofs} from the available data in a meaningful way. Assuming the Shunt-LDO are functional, it is expected for both R_{eff} and V_{ofs} to be described by the distributions found in Appendix A.2 and missing values are drawn from these distributions instead.

Such a resulting Shunt-LDO IV curve is shown in Figure 5.29. Shown is the Shunt-LDO IV curve of the digital regulator on SPQ14 FE0. For the remaining data sets the IV curves can be found in Section B.3. In these measurements, V_{in}, V_{DD}, V_{ref} and V_{ofs} are each measured using the on-chip voltage multiplexer. V_{in} for each of these plots corresponds to the V_{in} rail of the ROC. For each ROC the V_{in} rails of digital and analog Shunt-LDO are tied together on the chip, while the V_{in} of each ROC are tied together on the module flex. The differences in V_{in} between the different ROC, driven by impedance mismatches on the module flex, are negligible as can be seen. The offset voltage V_{ofs} measured using the voltage multiplexer is again a copy of the voltage input in A_5 in Figure 4.23, while the actual offset voltage seen by the Shunt-LDO is the potential at the lower terminal of R_{shunt}. In the measurement, both voltages are directly compared as the lower terminal of R_{shunt} is available on the monitoring pins for each Shunt-LDO.

In Table 5.5 the different R_{eff} and V_{ofs} for each module are listed as an average of the available data points per module. Additionally the difference between measured and expected R_{eff} and V_{ofs} are plotted in Figure 5.30 A prominent exception to the general good agreement between measurement and expectation is found in SPQ18. Here the measured R_{eff} significantly

	$R_{\text{eff}} + V_{\text{ofs}}$	Expected
SPQ11	$0.15\,\Omega + 0.81\,\text{V}$	$0.15\,\Omega + 0.85\,\text{V}$
SPQ12	$0.15\,\Omega + 0.82\,\text{V}$	$0.15\,\Omega + 0.83\,\text{V}$
SPQ13	$0.15\,\Omega + 0.82\,\text{V}$	$0.14\,\Omega + 0.84\,\text{V}$
SPQ14	$0.15\,\Omega + 0.83\,\text{V}$	$0.15\,\Omega + 0.84\,\text{V}$
SPQ15	$0.15\,\Omega + 0.83\,\text{V}$	$0.14\,\Omega + 0.86\,\text{V}$
SPQ16	$0.16\,\Omega + 0.78\,\text{V}$	$0.15\,\Omega + 0.85\,\text{V}$
SPQ18	$0.17\,\Omega + 0.77\,\text{V}$	$0.15\,\Omega + 0.81\,\text{V}$

Table 5.5: Overview of Shunt-LDO IV curve fits of modules in SP chain. The expected IV curve based on wafer probing data is given as well.
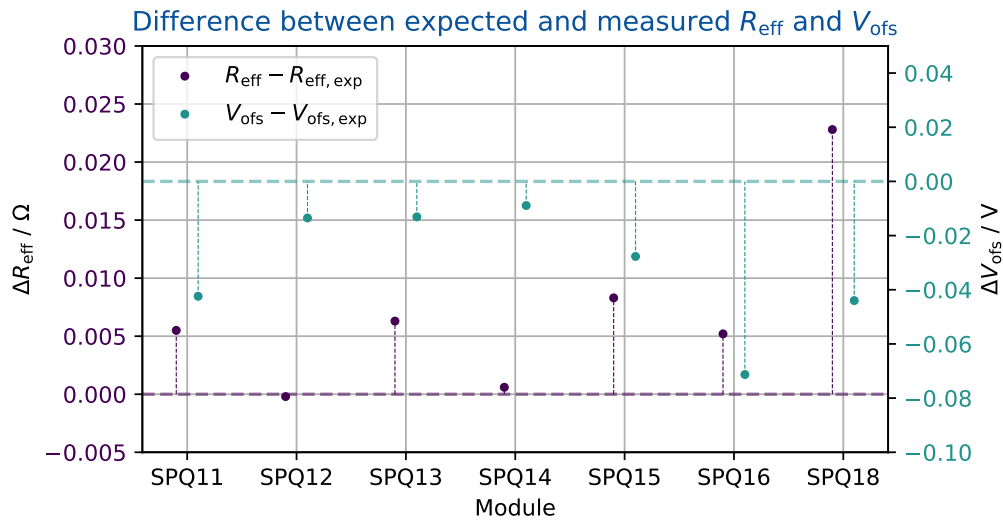
Figure 5.30: Discrepancy between measured R_{eff} and V_{ofs} and expected Shunt-LDO IV curve for modules in SP chain.

exceeds the expectation by approximately 15 %. With a full set of IV curves available from wafer probing data for this module such a difference is not expected. During reception tests SPQ18 was seen to have a larger R_{eff} compared to its peer modules as well [50]. While the underlying mechanism is not understood the origin for this behaviour is expected to be on the module itself. For SPQ16, the measured V_{ofs} is approximately 9 % lower than expected.

During each IV curve measurement, the voltage applied to the lower terminal of R_{shunt} is measured at each step of I_{in}. As shown in Equation 3.6 this voltage can be used to estimate the current flowing through the Shunt-LDO if k is known, with V_{M6} being equal to the offset voltage seen by the regulator. Using the estimates for the k-factor outlined above this allows a measurement of the current distribution on the module. Since the current sharing on a module has a direct impact on the required current headroom, which needs to be provided to the module. From the loading of the module flex, and thus the configuration of the Shunt-LDO, an almost even current sharing is expected between analog and digital Shunt-LDO, in which the digital Shunt-LDO would draw approximately 13 % of the total module current each and the analog Shunt-LDO each 12 %. A systematically different current sharing between analog and digital Shunt-LDO would warrant a reconsideration of the choices for R_{shunt} for the analog and digital Shunt-LDO. Should a single or multiple regulators draw significantly more current than their share, this would indicate an overload of the respective Shunt-LDO. In such case the current headroom provided to the module would be considered insufficient.

As a first step in determining the current sharing on a module, the voltage drop over R_{shunt} is measured as $V_{\mathrm{in}} - V_{\mathrm{ofsR_3}}$. These currents are then added up for each module and compared to the input current I_{in}. In Figure 5.31 the resulting calculated module currents are shown. Considering the significant implicit inaccuracies in obtaining the k-factor from R_{eff} alone, this procedure works well for all modules except SPQ18. The steeper slope on V_{in} measured for SPQ18 has a direct impact on this measurement and causes a very significant discrepancy with respect to the remaining modules. All modules show an approximately linear increase in the difference between I_{Mod} and I_{in}. This can be explained by the already observed dependency of k on I_{in} in Figure 4.26: For higher I_{in}, the k factor decreases, which causes a larger current through R_{shunt}.

As a next step the relative current share of each Shunt-LDO can be determined by comparing the calculated current I_{ctrl}, scaled by k, with the calculated on-module current sum. A good example for such a measurement is shown in Figure 5.32. Plots for the remaining modules are found in Section B.3. Despite the innate uncertainties in the determination of the k-factor, the on-module current sharing fits the design current distribution nicely. Of course a constant current sharing would initially be expected between all ROC in the working region of the Shunt-LDO. However the aforementioned dependency of k from I_{in} is not the same for each Shunt-LDO but instead differs in strength. Thus a change in the relative current sharing with a change in I_{in} can be expected.
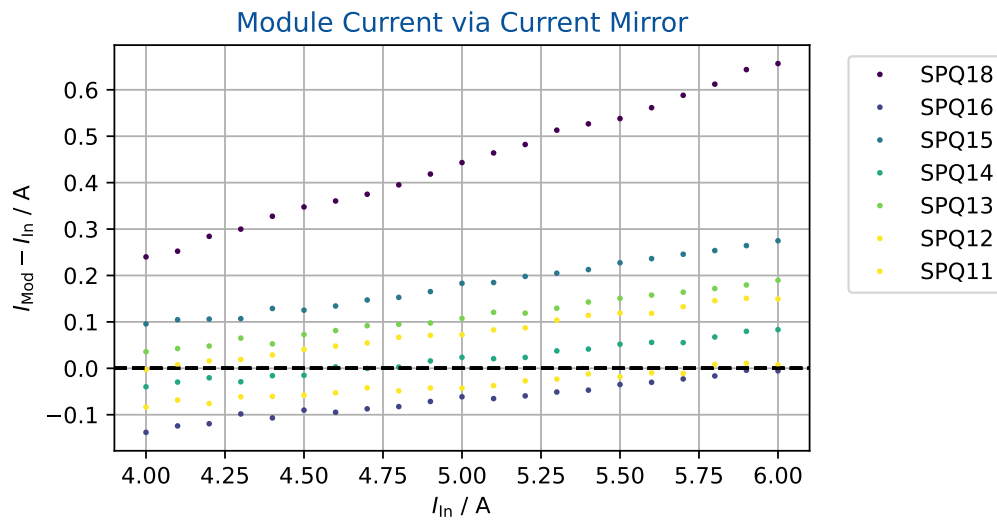
Figure 5.31: Difference between calculated module current and I_{in}.
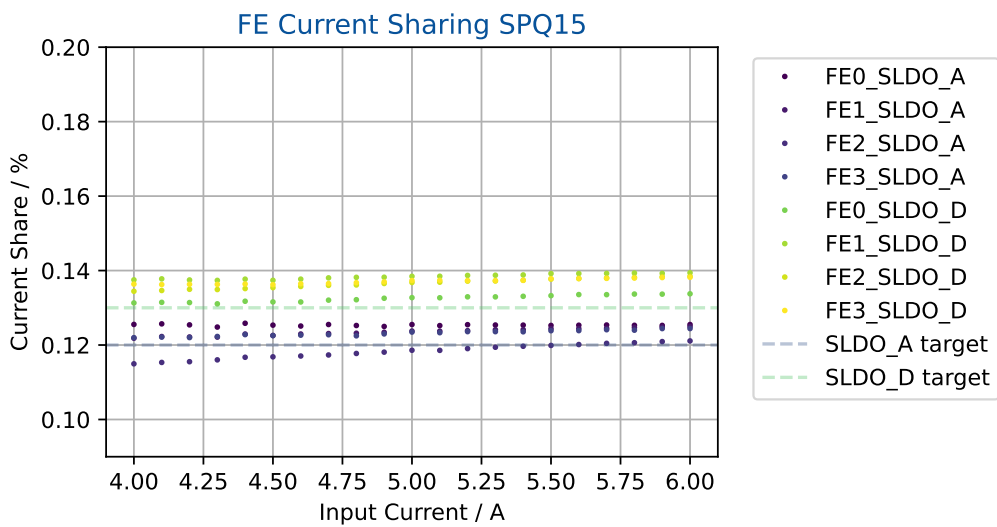
Figure 5.32: Current sharing between different Shunt-LDO on SPQ15. Both analog and digital regulators draw similar shares of the total current close to the ideal 12 % and 13 % respectively. The x-axis denotes the current supplied to the module, while the y-axis denotes the relative current share with respect to the calculated module current as per Figure 5.31.

5.3.3 Shunt-LDO Current Headroom

The working point of the RD53A quad modules introduced in Section 5.2.1 includes an operational current headroom of 20 % to account for the expected uneven current sharing between the different Shunt-LDO on the module. Based on the results shown in Section 5.3.2 an attempt can be made to estimate the required current headroom for operation of the RD53A quad modules. To this end the effective available current headroom can be changed by reducing the provided input current I_{in}. As long as the module voltage seen by the Shunt-LDO exceeds 1.4 V any resulting working point would be valid. In normal operation as in Section 5.3.4 the RD53A modules are usually not configured to draw the maximum current possible. Most importantly the SYNC AFE was usually disabled, which significantly reduces the current drawn by the module.

Estimates for the RD53A current consumption are based on a default chip configuration in which most internal biases are set to their default values according to [39]. With the analog current consumption mostly fixed the current consumption of the digital part of RD53A remains variable with a strong dependence on the chip activity. A simple way to increase the current consumption of the digital part of RD53A is sending readout trigger commands with a high frequency, which need to be processed by the chip. For the ITk pixel detector, an average trigger rate in the order of 1 MHz is expected. Actual hit data, e.g. from a radioactive source or analog test injections, are not needed. This is convenient as the DAQ used is not able to cope with such data rates. With this a procedure was developed to estimate the current headroom required for RD53A quad modules in the serial powering chain.

Starting at a working point I_{in} = 6 A with large current headroom, after establishing communication with the full module, the full pixel matrix is enabled. Using a variation of a scan developed for use with radioactive sources or in test beam environments, trigger commands are send to the RD53A module with a rate in the order of 1 MHz. Tracking the module V_{in} on an oscilloscope allows observation of an overload of single Shunt-LDO, as such an overload would lead to a drop in the regulators input impedance. The module input current is then reduced and the scan repeated until an overload is visible on the oscilloscope. Ideally this overload should also be visible when measuring the current sharing on the module, as an overloaded Shunt-LDO is expected to draw much more current than a not overloaded regulator. Figure 5.33 shows such a measurement on module SPQ11. From this measurement a clear overload of the module can be seen at input currents of 3.4 A, while no overload is seen for an input current of 4 A. When disabling parts of the matrix, e.g. the SYNC AFE, the overload even at low input currents disappears, as the total current consumption of the ROC is significantly reduced. With multiple parallel Shunt-LDO such an overload occurs gradually, making it difficult to accurately estimate the point of overload: a partially overloaded Shunt-LDO can draw current from the neighbouring regulators. Only once the
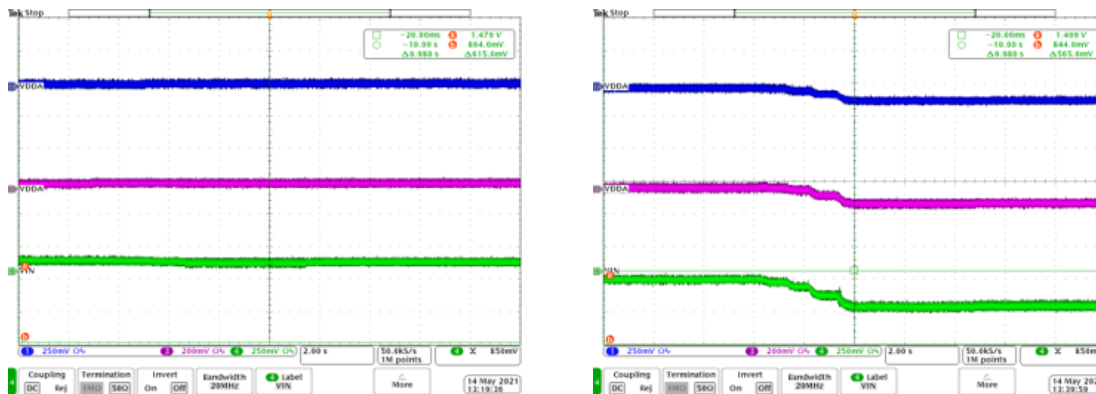
(a) $I_{in} = 4$ A, full matrix enabled. Shown are V_{in} and two V_{DDA}.

(b) $I_{in} = 3.4$ A, full matrix enabled. Shown are V_{in} and two V_{DDA}.

Figure 5.33: Module overload measurement with an oscilloscope. The module voltage V_{in} is shown in green, the two measured V_{DDA} are displayed in blue and purple. For different input currents, a repeated scan procedure aims to potentially cause an overload on one or more Shunt-LDO. Such an overload should manifest itself as a significant drop in V_{in}. In Figure 5.33(a) a measurement of SPQ11 for an input current of 4 A is shown with no clear overload taking place. Figure 5.33(b) shows the same measurement of SPQ11 for an input current of 3.4 A. A clear overload of the module is visible.

available current headroom is not sufficient to supply enough current to all Shunt-LDO, an overload will be visible. In Table 5.6 overload threshold estimates are given for modules in the SP chain. The given current headroom percentage refers to the required module current listed in Table 5.1. For all quads the estimated thresholds for overload conditions are well below the target headroom of 20 %. With the given configuration of the Shunt-LDO, an overload during normal operation could not be provoked for any feasible working point $V_{in} \geq 1.4$ V. All observed overloads occured at module voltages 1.4 V $\leq V_{in} \leq V_{ofs}$. The module response to an overload is slow enough and low in amplitude, such that the current source supplying the chain can compensate in time by changing its output voltage. As shown in Figure 5.34 such an overload can not be seen on the input voltage lines of direct neighbours in the serial chain. With the FE-I4 modules in the OBD program, powered by a voltage source, the behaviour was different: a local overload on a single module was clearly visible on neighbouring modules. This caused the PSPP chips of these neighbouring modules to switch on the module bypass. The resulting chain reaction bypassed the full powering chain.

The high uncertainty of the current mirror ratio k makes detection of an overload by measurement of the current distribution very difficult. In Table 5.7 such a current distribution during the overload shown in Figure 5.33(b) is measured. The measured distribution is consistent with the current distributions shown in Figure B.15(a) and Figure B.16(a), an overload of the Shunt-LDO can not be resolved. Nonetheless the general approach looks promising and more accurate results are expected from measurements with ITkPix, as ITkPix

Quad	I_{in}	Headroom Rounded up
SPQ11	$(3.8 \pm 0.1)\,A$	$(6 \pm 3)\,\%$
SPQ12	$(3.7 \pm 0.1)\,A$	$(3 \pm 3)\,\%$
SPQ13	$(3.8 \pm 0.1)\,A$	$(6 \pm 3)\,\%$
SPQ14	$(3.7 \pm 0.1)\,A$	$(3 \pm 3)\,\%$
SPQ15	$(3.7 \pm 0.1)\,A$	$(3 \pm 3)\,\%$
SPQ18	$(3.7 \pm 0.1)\,A$	$(3 \pm 3)\,\%$

Table 5.6: Estimated overload threshold for modules in SP chain. Current headroom given with respect to the base current consumption given in Table 5.1. A clear overload is often only visible for $I_{in} \leq 3.67\,A$, which is the expected module current consumption with no headroom. The module voltage for each of these thresholds is below $1.4\,V$.
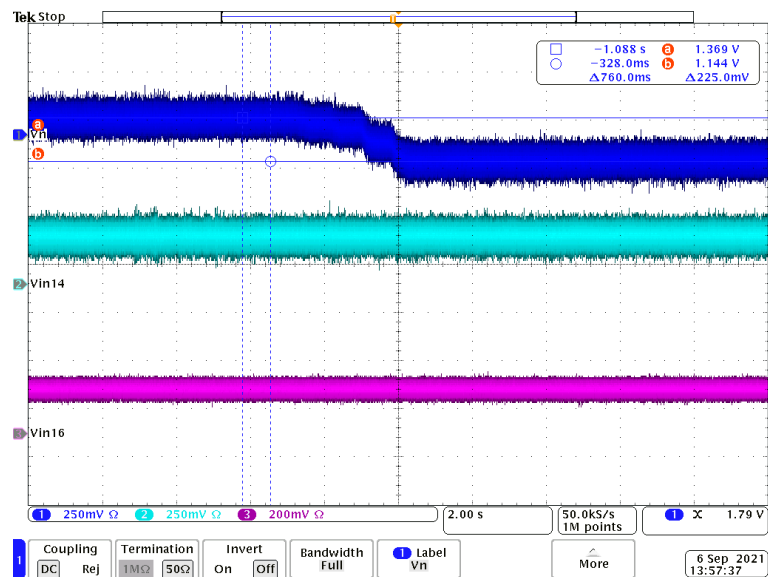
Figure 5.34: Effect of a module overload on neighbouring modules. Shown are the input voltages V_{in} for modules SPQ14 in cyan, SPQ15 in blue and SPQ16 in purple. SPQ15 is driven into overload, while SPQ14 and SPQ16 are kept at a lower power consumption. No effect of the overload on the direct neighbours in the serial chain is visible.

SPQ11	Current share analog	Current share digital
FE0	$(0.128 \pm 0.022)\,\%$	$(0.128 \pm 0.022)\,\%$
FE1	$(0.113 \pm 0.019)\,\%$	$(0.127 \pm 0.022)\,\%$
FE2	$(0.114 \pm 0.020)\,\%$	$(0.130 \pm 0.023)\,\%$
FE3	$(0.121 \pm 0.021)\,\%$	$(0.138 \pm 0.024)\,\%$

Table 5.7: Current sharing between Shunt-LDO in overload condition for SPQ11.
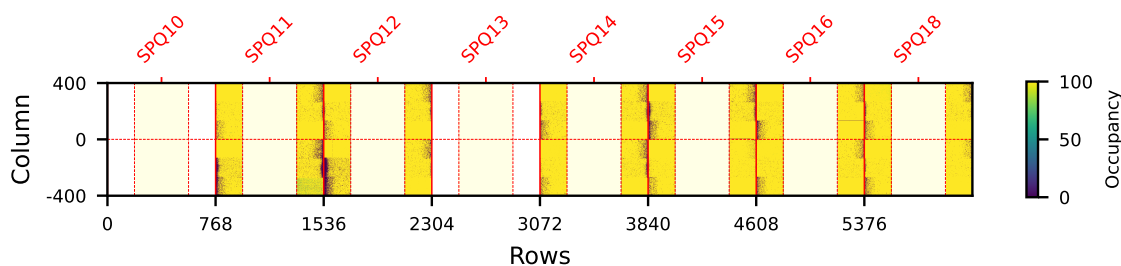
Figure 5.35: Analog test injections for all fully functional ROC in the SP chain after tuning to a target threshold of $2\,000\,e^-$. SPQ10 and SPQ13 are masked since they are not considered in any further evaluations. Sensor sized plotting is used, areas covered by the sensor but not connected to any ROC pixel are shaded in yellow.

offers the possibility to measure each regulator's input current I_{in} and shunt current I_{shunt}, which allows a very direct measurement of the local current headroom.

5.3.4 Module Performance in Serial Powering chain

Based on the results from the module reception tests the performance of the RD53A quad modules in an SP chain can be evaluated. As a first step, the general functionality of the ROC is tested. Afterwards the LIN and DIFF AFE of the ROC are tuned to detection thresholds of $2\,000\,e^-$ and $1\,000\,e^-$ in serial chain operation. Measuring the threshold performance and ENC of modules in the chain and comparing them with the reference gained from reception tests allows judging the module performance.

As known from the module reception tests, SPQ10 and SPQ13 fail to be operated at a detection threshold of $1\,000\,e^-$. Since this is the main performance benchmark, these modules are excluded in the following. In Figure 5.35 an analog scan of the remaining modules at a threshold of $2\,000\,e^-$ is shown with sensor sized plotting. All unmasked modules show a largely homogeneous response with only few failing pixels. Only the SYNC AFE on single
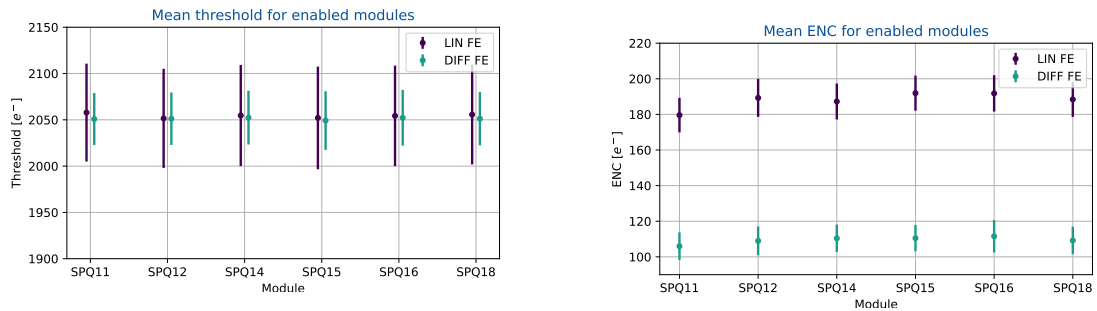
(a) Example of a good IV curve measurement from wafer probing. With proper selection of fit ranges R_{eff} and V_{ofs} can be determined.

(b) Example of a bad IV curve measurement from wafer probing.

Figure 5.36: Threshold distribution and ENC for LIN and DIFF AFE of all modules in serial chain operation after tuning to a target threshold of $2\,000\,e^-$.
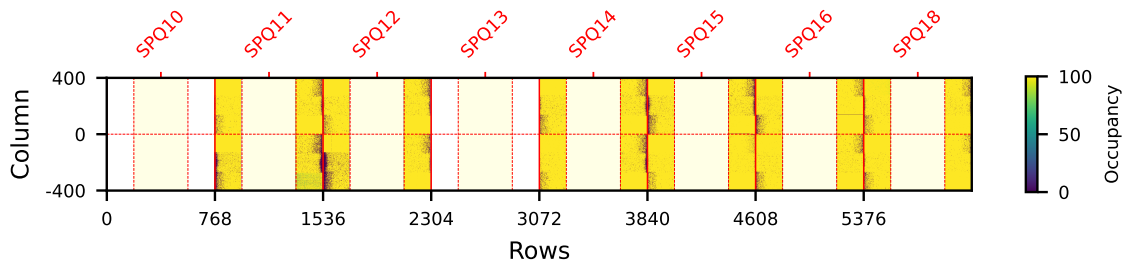
Figure 5.37: Analog test injections for all fully functional ROC in the SP chain after tuning to a target threshold of $1\,000\,e^-$. SPQ10 and SPQ13 are masked since they are not considered in any further evaluations. Sensor sized plotting is used, areas covered by the sensor but not connected to any ROC pixel are shaded in yellow. Noisy pixels are shown in purple with no apparent response to analog injections, as they are masked by the tuning procedure.

ROC of modules SPQ11, SPQ15 and SPQ16 show larger amount of non-ideally responding pixels. With only LIN and DIFF AFE being a subject of this prototype, the worse performance of the SYNC AFE is of no concern. The distribution of the mean threshold and mean noise after tuning to $2\,000\,e^-$ can be seen in Figure 5.36.

After tuning to a threshold of $1\,000\,e^-$, pixels in the periphery region of the LIN and DIFF AFE become increasingly noisy. This is caused by the interplay between sensor and AFE as discussed before and varies in effect as can be seen in Figure 5.37, where all noisy pixels are masked. The effect is more pronounced in the periphery of the ROC, closer to the Shunt-LDO. This is observed both in LDO and Shunt-LDO mode, implying the Shunt-LDO is not responsible for this uneven distribution. As can be seen in Figure 5.38 the amount of noisy pixel per module varies significantly after tuning to $1\,000\,e^-$, while after tuning to $2\,000\,e^-$ only a very limited number of noisy pixels can be observed. In Figure 5.39 the
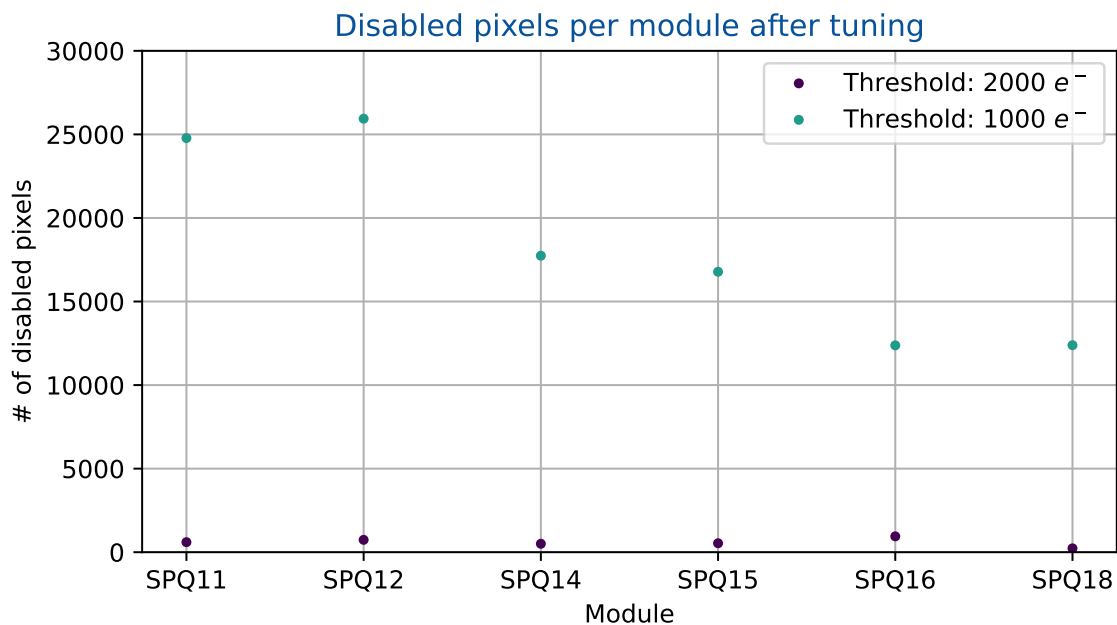
Figure 5.38: Amount of noisy pixel on quad modules after tuning to $2\,000\,e^-$ and $1\,000\,e^-$. As a reference the sum total of all pixel in the LIN and DIFF AFE is given.
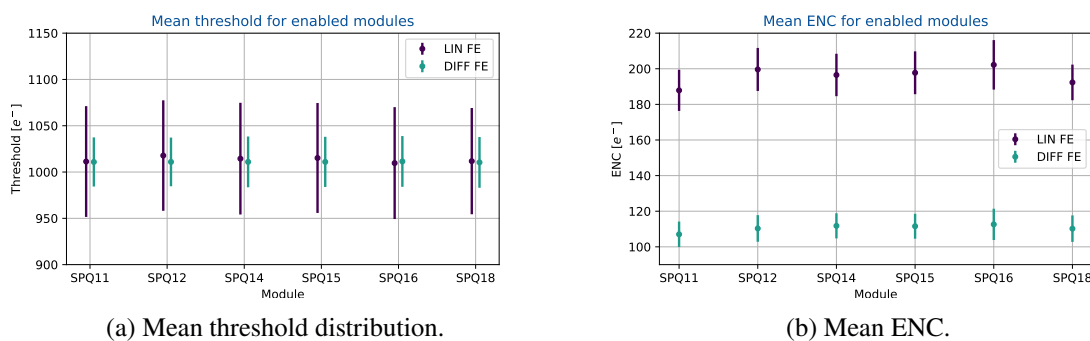
(a) Mean threshold distribution.

(b) Mean ENC.

Figure 5.39: Threshold distribution and ENC for LIN and DIFF AFE of all modules in serial chain operation after tuning to a target threshold of $2\,000\,e^-$.

mean threshold and ENC is plotted for the LIN and DIFF AFE for each module in serial chain operation. As can be seen from comparing Figure 5.36 with Figure 5.39, the threshold performance and ENC remains largely unchanged after tuning the ROC to a threshold if $1\,000\,e^-$, as would be expected.

The threshold performance of the tuned modules in the SP chain can now be compared with the reception test measurements shown before. In Table 5.8 and Table 5.9 the threshold distribution and ENC is shown for the LIN and DIFF AFE respectively. As can be seen

LIN AFE	SP chain		Reception tests	
	Threshold	ENC	Threshold	ENC
SPQ11	$(1\,011 \pm 60)\,e^-$	$(188 \pm 12)\,e^-$	$(1\,015 \pm 62)\,e^-$	$(194 \pm 12)\,e^-$
SPQ12	$(1\,018 \pm 60)\,e^-$	$(200 \pm 12)\,e^-$	$(1\,010 \pm 63)\,e^-$	$(206 \pm 13)\,e^-$
SPQ14	$(1\,014 \pm 61)\,e^-$	$(197 \pm 12)\,e^-$	$(1\,014 \pm 67)\,e^-$	$(256 \pm 21)\,e^-$
SPQ15	$(1\,015 \pm 60)\,e^-$	$(198 \pm 12)\,e^-$	$(1\,015 \pm 60)\,e^-$	$(187 \pm 11)\,e^-$
SPQ16	$(1\,010 \pm 62)\,e^-$	$(202 \pm 14)\,e^-$	$(1\,007 \pm 76)\,e^-$	$(253 \pm 29)\,e^-$
SPQ18	$(1\,012 \pm 58)\,e^-$	$(192 \pm 10)\,e^-$	$(1\,016 \pm 61)\,e^-$	$(188 \pm 10)\,e^-$

Table 5.8: Threshold distribution and ENC of the LIN AFE for all modules in SP chain operation. Results from reception tests are listed as reference. All chips tuned to a detection threshold of $1\,000\,e^-$.

LIN AFE	SP chain		Reception tests	
	Threshold	ENC	Threshold	ENC
SPQ11	$(1\,011 \pm 27)\,e^-$	$(107 \pm 7)\,e^-$	$(1\,011 \pm 23)\,e^-$	$(107 \pm 5)\,e^-$
SPQ12	$(1\,011 \pm 27)\,e^-$	$(110 \pm 7)\,e^-$	$(1\,012 \pm 28)\,e^-$	$(113 \pm 6)\,e^-$
SPQ14	$(1\,011 \pm 28)\,e^-$	$(112 \pm 7)\,e^-$	$(1\,014 \pm 25)\,e^-$	$(123 \pm 8)\,e^-$
SPQ15	$(1\,011 \pm 28)\,e^-$	$(112 \pm 7)\,e^-$	$(1\,012 \pm 26)\,e^-$	$(110 \pm 9)\,e^-$
SPQ16	$(1\,011 \pm 30)\,e^-$	$(113 \pm 9)\,e^-$	$(1\,019 \pm 40)\,e^-$	$(161 \pm 35)\,e^-$
SPQ18	$(1\,010 \pm 28)\,e^-$	$(110 \pm 7)\,e^-$	$(1\,012 \pm 28)\,e^-$	$(113 \pm 8)\,e^-$

Table 5.9: Threshold distribution and ENC of the DIFF AFE for all modules in SP chain operation. Results from reception tests are listed as reference. All chips tuned to a detection threshold of $1\,000\,e^-$.
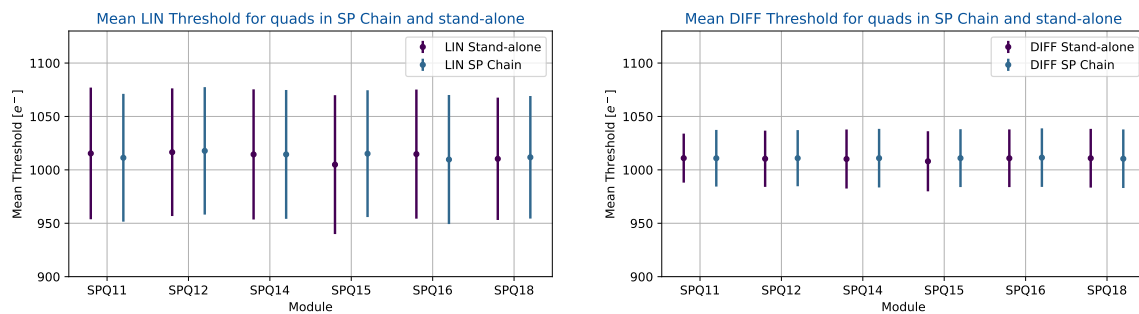
(a) Threshold distribution for all active pixel in the SP chain, LIN AFE only.

(b) Threshold distribution for all active pixel in the SP chain, DIFF AFE only.

Figure 5.40: Threshold distribution for all active ROC in SP chain after tuning to a target threshold of $1\,000\,e^{-}$. Shown are measurements in SP chain operation as well as each module stand-alone on the stave.

the performance of the modules does not degrade in serial chain operation. The very high ENC observed for some of the modules during reception tests, refer to Figure 5.27, could not be reproduced. The active cooling available for all modules in the SP chain compared to the reception tests is expected to have further impact on the measured ENC, but could not explain this difference. Since the modules are retuned in the SP chain, the threshold distribution should not be sensitive to the different setups as long as modules are not too noisy. In summary this makes judging the module performance based on the reception tests more difficult, however it still allows to conclude no significant impact of the SP operation.

In order to mitigate contributions from the different setups used, an additional set of reference measurements is performed on the stave. In these measurements only a single module was powered at any time. Active cooling was used to ensure a stable module temperature comparable to SP chain operation, while the same bias voltage is applied to the sensor as during reception tests. The resulting comparison of threshold performance and ENC is shown in Figure 5.40 and Figure 5.41. A very good agreement between stand-alone and serial chain operation can be seen. The number of disabled pixels in SP operation compared to the stand-alone operation is shown in Figure 5.42. No clear tendency towards an increase or decrease in the number of noisy pixels can be observed. For most modules the relative change in the number of noisy pixel is negligible. The DIFF AFE contributes approximately 60 % of noisy pixels in both stand-alone and SP operation for all modules. For modules SPQ11 and SPQ12, the number of noisy pixel after tuning to $1\,000\,e^{-}$ exceeds 10 % of the full matrix size. For the module with the smallest number of noisy pixel, SPQ18, approximately 6 % of the combined matrix of LIN and DIFF AFE are disabled. Such orders of magnitude for disabled pixels are unacceptable for detector operation. However it is known this behaviour is a consequence of the module design and is not caused by the SP scheme.
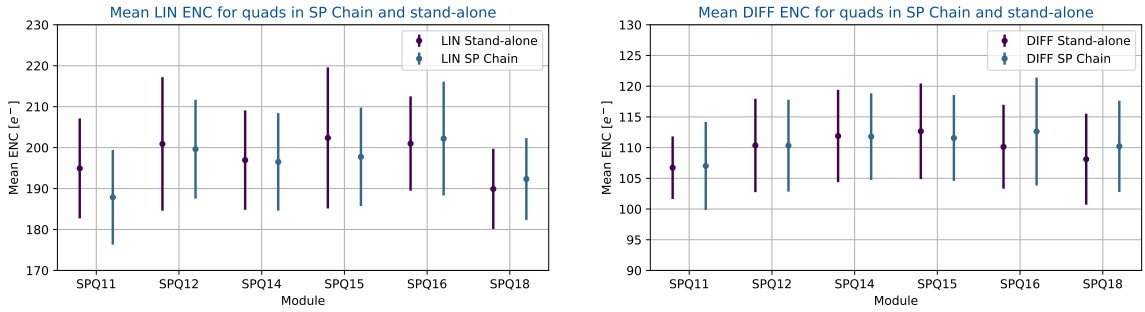
(a) ENC for all active pixel in the SP chain, LIN AFE only.

(b) ENC for all active pixel in the SP chain, DIFF AFE only.

Figure 5.41: ENC distribution for all active ROC in SP chain after tuning to a target threshold of $1\,000\,e^-$. Shown are measurements in SP chain operation as well as each module stand-alone on the stave.
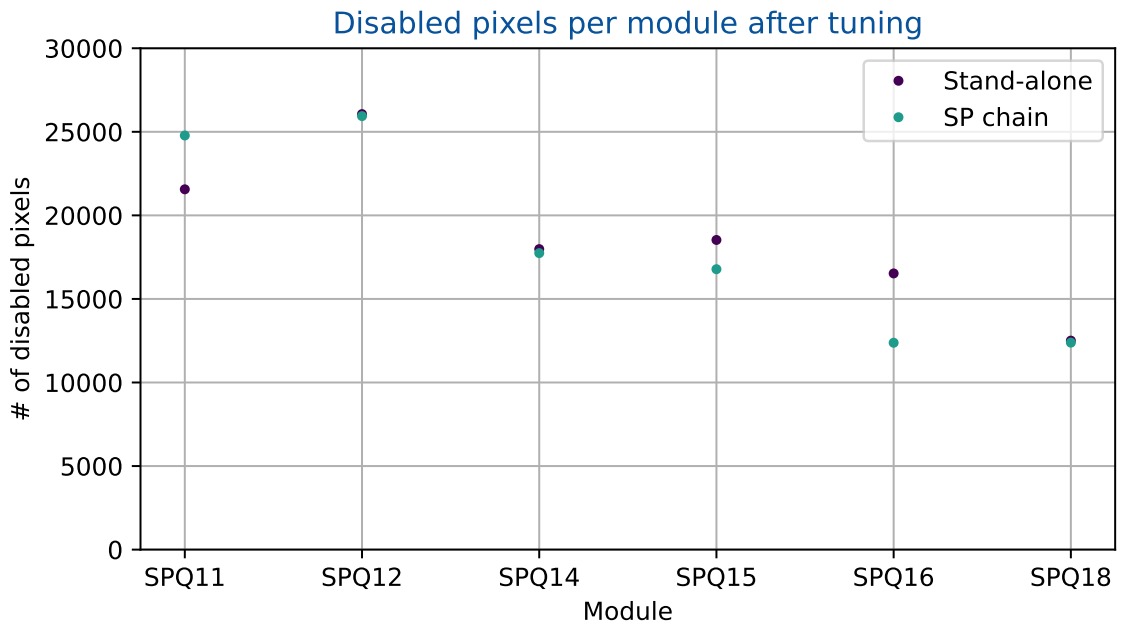
Figure 5.42: Comparison of number of noisy pixels in SP operation and stand-alone.
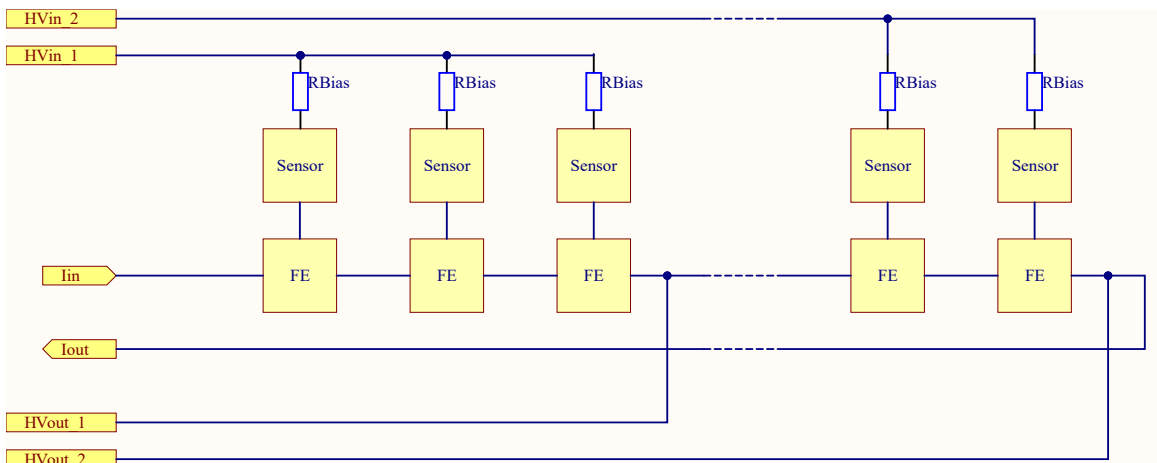
Figure 5.43: Schematic view of the initial HV distribution scheme baseline for the ITk OB and EC. Modules in a serial chain are grouped in two HV groups. Within each group all sensor backsides are supplied in parallel by the same HV output channel. The leakage current is returned via the LV line to the HV power supply. This scheme is not in agreement with the most recent grounding and shielding rules, which require each HV supply channel to be directly referenced to the system ground.

For future ITkPix production modules or modules with a different sensor architecture less than 1 % noisy pixels are expected for detection thresholds in the order of $1\,000\,e^-$, with both LIN and DIFF AFE being optimized for operation at low thresholds.

5.3.5 Studies of the HV Distribution

As discussed in Section 3.1.2 the HV distribution in a serially powered detector is not trivial and requires some considerations. Two main approaches form the current baseline for the ATLAS ITk Pixel detector. In the OB and end caps (EC) two HV supply channels will be used per SP chain, depending on the chain length. In such a configuration, typically 6-8 modules are supplied by HV in parallel. Initially the return line of each of these HV groups was to be connected to the module with the lowest local GND potential with respect to the system GND as shown in Figure 5.43. This corresponds to the HV scheme treated in the following. However after a revision of the grounding and shielding rules for the ITk Pixel detector, each HV supply line needs to be directly referenced to the system ground. This is not compatible with the scheme shown in Figure 5.43. As a solution a single common HV return is used instead for both HV supply channels similar to Figure 3.4. The default operation mode of the RD53A SP prototype discussed here is a common HV distribution scheme with a single HV return line for 8 modules. This represents one HV group in the future ITk OB and EC pixel detectors.

The innermost layer of the IS in ITk pixel is populated with modules using 3D-sensors
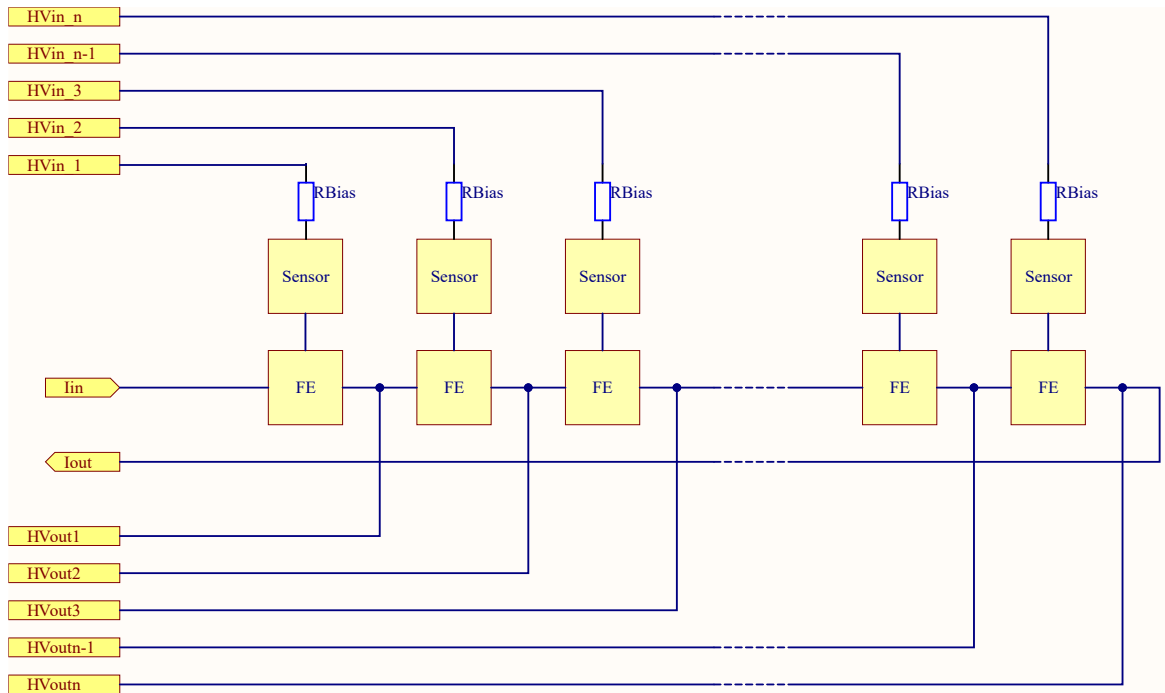
Figure 5.44: Schematic view of the HV distribution scheme baseline for the innermost layer of the ITk IS. Each module in the SP chain is connected to its dedicated HV supply and return line.

compared to the planar sensors used in the rest of ITk pixel. These sensors have a significantly lower breakdown voltage which will be well below 20 V. According to Equation 3.2 only very short SP chains could be realized for such modules to prevent potential damage to the sensors and ensuring full depletion at the same time, given the maximum LV voltage drop for an ITkPix module of 2 V. It is thus more feasible to change the HV distribution scheme to a scheme with a dedicated HV return line for each module while retaining the same SP chain lengths as in other parts of the detector. Such a scheme is shown in Figure 5.44. The scheme used in the IS is in violation of the grounding and shielding rules just as the initial OB scheme discussed above. As it is not feasible to use a HV distribution scheme in the IS which is in agreement with these rules, an exception was made for the IS.

In each scheme utilizing more than one HV group for a single SP chain it is important to provide sufficient isolation between the HV return line and the system GND to suppress parasitic current paths. With the SP prototype characterised here, the different HV distribution schemes can be compared with respect to any potential impact on the module performance. Tested are as most representative cases a common HV return line for the serial chain, two HV supply channels as is the default for the majority of ITk pixel and a single HV supply and return for each module in serial chain operation. The performance evaluation follows the procedure outlined before.
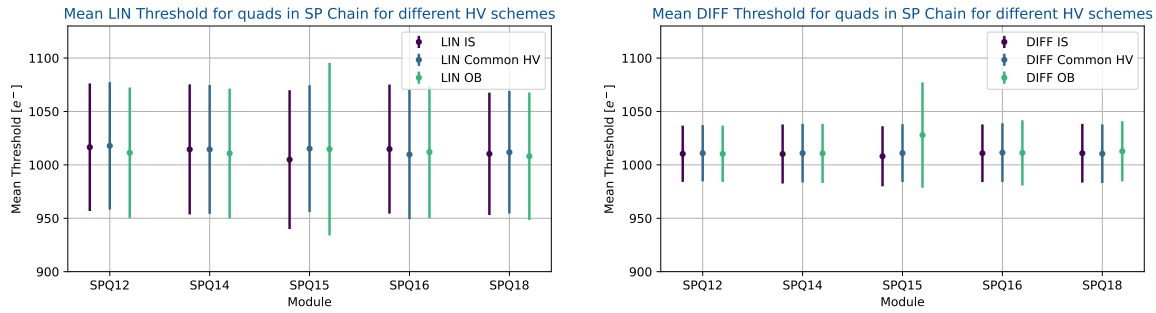
(a) Threshold distribution for all active pixel in the SP chain, LIN AFE only.

(b) Threshold distribution for all active pixel in the SP chain, DIFF AFE only.

Figure 5.45: Threshold distribution for all active ROC in SP chain after tuning to a target threshold of $1\,000\,e^-$. Shown are measurements with a single shared HV return line labelled (Common HV), two HV return lines labelled OB and a dedicated HV return line per module labelled IS.
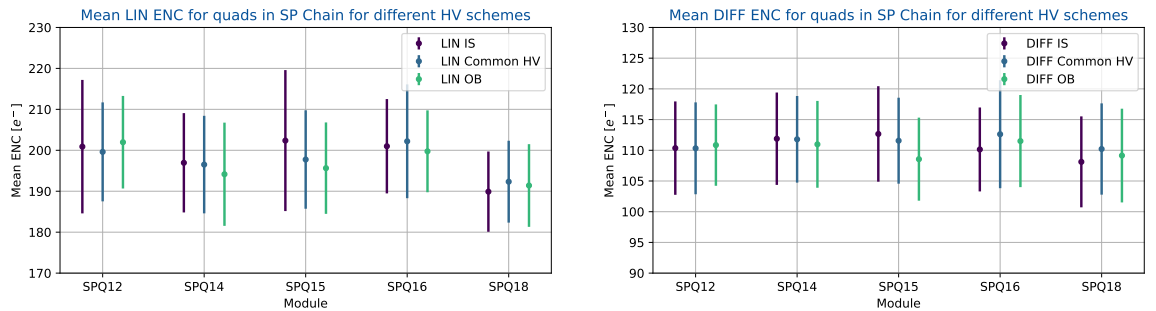
(a) ENC for all active pixel in the SP chain, LIN AFE only.

(b) ENC for all active pixel in the SP chain, DIFF AFE only.

Figure 5.46: ENC distribution for all active ROC in SP chain after tuning to a target threshold of $1\,000\,e^-$. Shown are measurements with a single shared HV return line labelled (Common HV), two HV return lines labelled OB and a dedicated HV return line per module labelled IS.

In Section 5.3.4 the SP chain uses a HV configuration in which all modules except SPQ13 are grouped in the same HV group. SPQ13 is not included due to its excessive leakage current. Switching to a different HV distribution scheme should not have any impact on the module performance. To evaluate any change in module performance, repeated threshold scans are performed in different HV configurations without prior re-tuning of the module. The resulting threshold distributions and ENC for a single HV return line, a scheme with two HV return lines, representing the initial OB approach, and operation with dedicated HV return lines for each module, representing the IS, are shown in Figure 5.45 and Figure 5.46. In case of the OB HV scheme, modules SPQ10−SPQ12 and SPQ14−SPQ18 are grouped together respectively. SPQ11 is missing in this data set as a result of mechanical failure during operation. Due to a mechanical failure of the glue used in module building, the module

flex detached from the bare module, severing a large number of wire bonds and rendering the module unusable. From the remaining module population only SPQ15 shows a noteable change in threshold performance in the DIFF AFE when using the OB HV scheme. While not finally understood the threshold distribution can be narrowed after re-tuning the AFE, bringing SPQ15 again perfectly in line. Given the unchanged ENC, temperature effects are not likely to be causing this behaviour. In the IS configuration no remarkable effects could be observed. Overall, no systematic effect on the module performance could be provoked using different HV grouping schemes.

HV Off-Mode Considerations

An important question raised from previous SP prototyping is the issue of potentially harmful current paths through the module sensors in a SP chain, if the HV is switched off but all modules are powered. This is typically the case during the switch-on procedure of a pixel detector, e.g. after the annual end-of-year shutdown of the LHC, or during filling of the LHC accelerator ring with protons. The behaviour of the SP system in such a case is driven by the impedance of the HV power supply when switched off, the underlying mechanism is outlined in Section 3.1.2. In an effort to add to studies performed in parallel on RD53A single chip modules on single chip card (SCC) and a ITkPix single chip, published in [33], the effect of the different options for a HV off mode on the SP chain stability is investigated. Furthermore any effect the different HV configurations may have on the SP chain when LV is switched on or off is to be covered.

Firstly the effect of a high-ohmic HV off-mode on the RD53A is to be quantified. To this end the leakage current flowing through any sensor can be sensed using a $1\,\text{k}\Omega$ series resistor on the HV supply line on the stave flex. All modules are connected in the same HV group, the LV is ramped up to the nominal operating current of the SP chain $I_{\text{in}} = 5\,\text{A}$ and the leakage current for each module is measured using the series resistor. For this measurement a large leakage current is desirable. To maximise the leakage current, SPQ13 was included in the HV group. SPQ11 was replaced by the spare module SPQ17, which suffers from an increased leakage current similarly to SPQ13.

In Figure 5.47 the absolute value of the leakage current for each module is shown as a function of the serial chain current. In this measurement, the HV off mode was chosen as low ohmic. The measured leakage current is very sensitive to the module temperature and the amount of ambient light incident on the sensor. As expected from known module properties, all modules except SPQ13 and SPQ17 show a negligible leakage current. If now a high-ohmic off mode is chosen for the HV power supply, the leakage current for all modules except module SPQ18 will be returned through SPQ18, applying an effective forward bias. This behaviour is shown in Figure 5.48, where the absolute value of the sum of
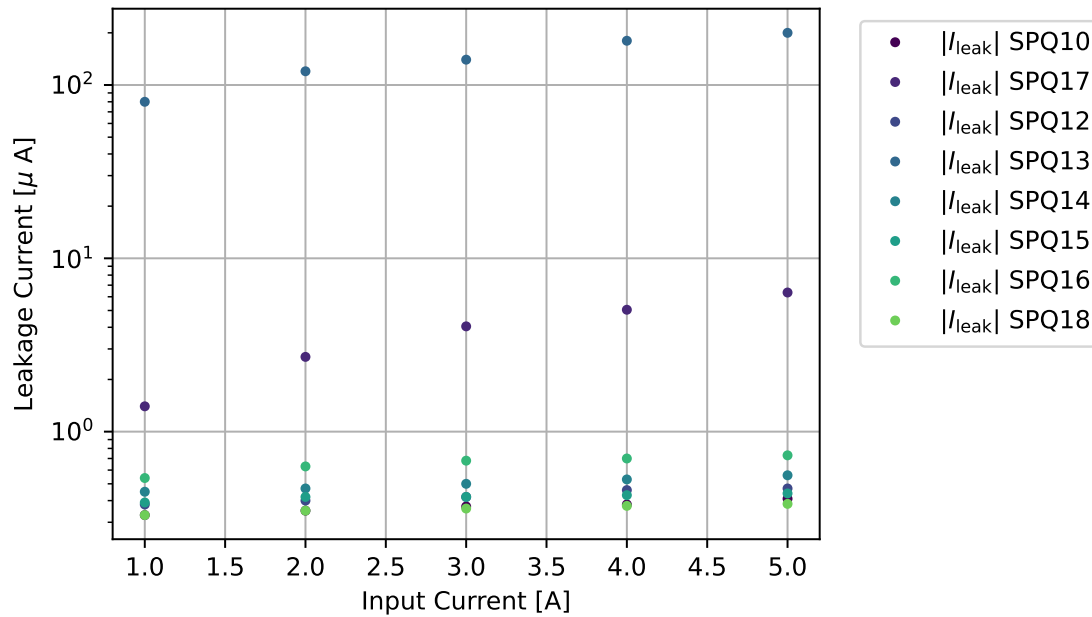
Figure 5.47: Reverse bias leakage current for each module generated by LV voltage drop over each module. LV supply switched off with a low-ohmic off mode.

all leakage currents except SPQ18 is compared with the current flowing through SPQ18. The current flow through the sensor of SPQ18 is in forward bias direction and corresponds to a leakage current of approximately 0.67 nA per pixel. No immediate adverse effect from this forward biasing could be observed. After reaching the nominal chain current, establishing communication with SPQ18 and leaving the chain powered on in this configuration for several hours, SPQ18 was still fully functional. This is in accordance with similar observations made with irradiated RD53A modules [33]. Differing from the observations in [33] a forward leakage current was only observed for the last module in the SP chain, SPQ18. This is due to the smaller HV bias series resistor in this serial chain, which totals to 6 kΩ compared to 10 kΩ on the SCC used in [33], as well as a much lower total leakage current. The resulting voltage drop over the bias resistor, which is limited to the voltage drop over a single module, is smaller. A measurement of the AFE pixel input potential, similar to the measurement on an ITkPix single chip in [33], would give further insights on potential harmful voltages inside the ROC. This can happen if the voltage of the pre-amplifier input of the AFE exceeds the core voltage V_{DDA} due to forward bias flow. Measurements with ITkPix suggest this is not of concern for per pixel leakage currents of up to 6.5 nA. Such a leakage current is well above the estimates for ITk pixel at end of life and an order of magnitude above the leakage current that could be generated with the RD53A prototype in this work.

As a second point the behaviour of the HV lines when switching the chain current on or
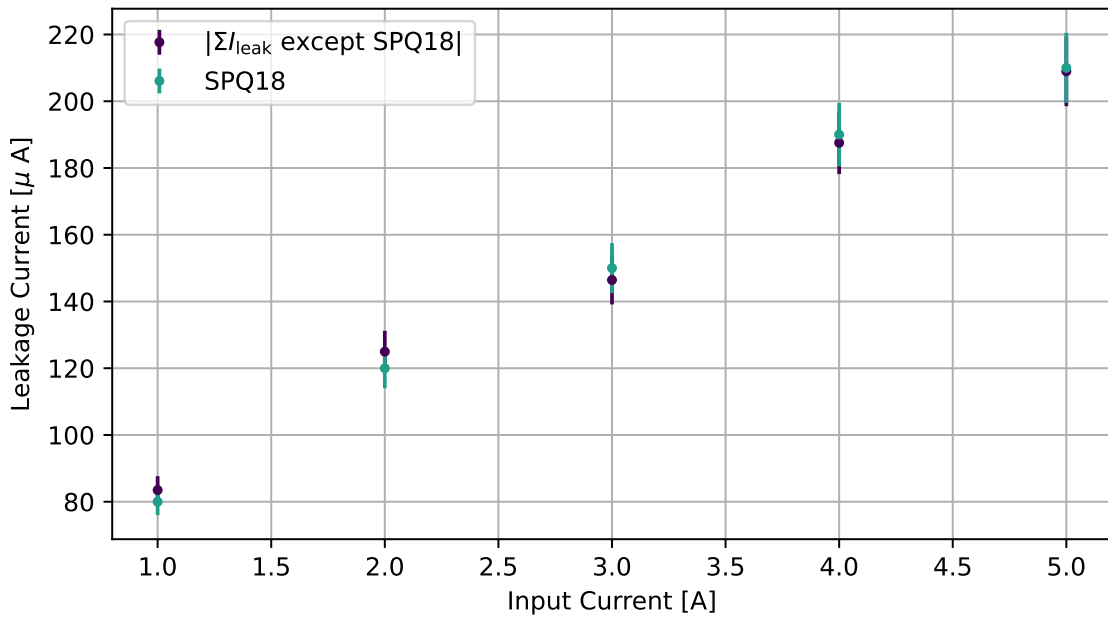
Figure 5.48: Sum of the leakage currents of all modules except SPQ18 and forward leakage current measured for SPQ18 as function of input current. As the leakage currents and the current returned through SPQ18 have different signs, the absolute value of the sum of leakage currents is shown.

off is to be checked. During these LV transients, potentially harmful currents may flow on the HV line depending on the HV off mode. In Figure 5.49 the observed transients on the HV line are shown for one module when the LV is switched on. With an input current ramp rate of $1\,\mathrm{kA\,s^{-1}}$, the input current reaches its nominal value after 5 ms. The sensed current on the HV line settles after approximately 2.5 s. The transients coincide with the transients visible on the LV line when switching the chain on. These observed current spikes are expected to be driven by a filter capacitor on the module flex, which is connected in parallel to the sensor to filter out high frequency noise on the HV line. Any current flow to charge and discharge this capacitor, which does not flow through the module itself, can be seen at the point of measurement. As expected a low-ohmic off mode of the HV power supply largely mitigates this effect.

5.3.6 Conclusion and outlook

Summarizing the previous sections, a serial powering chain with 8 RD53A quad modules and dedicated services has been successfully set up and evaluated. The results presented here show that a serial powering scheme for the ITk pixel detector with current generation pixel ROCs is feasible and performing well.

As expected the performance of RD53A ROC is not at all impacted by the usage of the
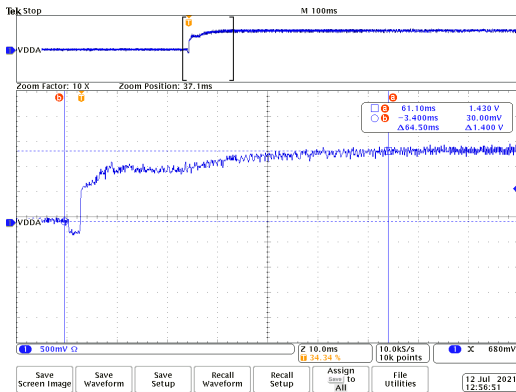
(a) Module LV during input current ramp.
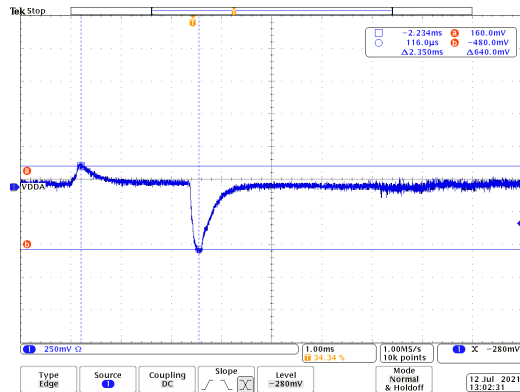
(b) High-ohmic HV off mode.
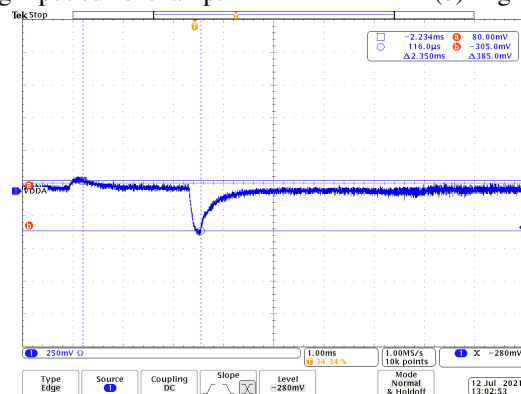
(c) Low-ohmic HV off mode.

Figure 5.49: Transient on the HV line when LV is switched on. Measured on SPQ10. HV power supply is in an high-ohmic off state in Figure 5.49(b) and in an low-ohmic off state in Figure 5.49(c). 1 division corresponds to a current of 250 μA. Sign indicates current flow direction with negative currents flowing in reverse bias direction. As reference the module LV for the same current ramp is shown in Figure 5.49(a).

Shunt-LDO to supply power to the ROC. The dedicated services used for the quad modules in the context of this work yield a module with comparable performance with respect to collaboration standards for module testing [66]. All services used in the serial powering prototype are designed with a focus on flexibility and accessibility, allowing more insights on the electrical behaviour of the used quad modules than usually available.

Powered by a representative current source a serial powering chain consisting of 8 RD53A quad modules was set up. Each module has been characterised before integration on the stave as well as in the serial powering chain. No failures relatable to the serial powering chain could be noted, but module performance in good agreement with reception tests and expectations specific to RD53A. The Shunt-LDO circuitry in RD53A, despite its known flaws, performs well in a realistic scenario, providing a stable power supply to the ROC. Measurement procedures were successfully tested which will allow valuable input to fine tuning of the module current headroom, which contributes significantly to the power efficiency of a serially powered detector.

Different HV distribution schemes have been tested for the ITk pixel detector. The choice of the HV distribution scheme does not influence the performance of the serial powering chain in any meaningful way. Measurements aiming at the interplay between the HV power supply properties and the serial powering chain, with focus on the question of a potentially unsafe high-ohmic off mode, do not raise any cause of concern.

As a next step, the SP chain is populated with digital ITkPix quad modules. No changes to the services and infrastructure of the prototype are required, as the setup was designed with compatibility to ITkPix in mind. At the time of writing a measurement campaign is taking place to provide data required for the LV power supply market survey for ITk pixel.

CHAPTER **6**

Summary and Outlook

The LHC will be upgraded to the HL-LHC in the coming years. The challenges imposed by this upgrade in turn require upgrades of the particle detectors at the LHC in order for them to cope with the conditions in the HL-LHC. In particular large parts of the ATLAS detector have to be completely rebuilt - the complete inner detector will be exchanged in favour of an all-silicon tracking detector, the ITk. The pixel detector in ITk has to resort to a completely novel power distribution scheme in high energy physics in order to comply with the constraints set by the ITk in terms of space, performance and power efficiency. This new scheme is the Serial Powering scheme. The work presented in this thesis was closely involved in the prototyping and system test related to serial powering.

The development of the Shunt-LDO voltage regulator from the first prototype in the new 65 nm node to the integration in a first large-scale pixel readout chip in the new technology node has been closely accompanied. Crucial characterisation measurements have been performed to add to the verification of the Shunt-LDO. The results obtained with the 500 mA and 2 A prototype chips are in good agreement with simulations of the design. While the line regulation of these first prototypes does not quite reach the design target, the load regulation performance is shown to be excellent. Further core features of the Shunt-LDO show satisfying performance, including the output voltage steering and new offset generating circuitry in the 2 A prototype. Parallel operation of Shunt-LDO as will be exercised in the future pixel ROC was demonstrated as well as serial operation. The radiation hardness of these first Shunt-LDO prototypes in 65 nm has been demonstrated in several X-ray irradiation campaigns, reaching TID in excess of 500 Mrad. Starting with the 2 A prototype a deviation in the current mirror ratio k could be observed. k is together with the Shunt-LDO offset voltage responsible for defining the working point of the Shunt-LDO and by extension of the pixel detector module. Large deviations from the design value can quickly lead to a misconfiguration of the Shunt-LDO working point, resulting in a decreased power efficiency of the pixel module.

With power efficiency being one of the main challenges for ITk pixel, such outcomes need to be avoided.

These first prototypes culminated in the implementation of the Shunt-LDO in the RD53A ASIC, a first prototype of the future pixel ROC for the ATLAS and CMS experiments, designed to be operated in a serially powered detector. The Shunt-LDO in RD53A suffers from some teething problems, which limits the performance of RD53A in Shunt-LDO operation. Most of these issues could be traced back to the bandgap reference providing lower-than-expected output voltages. The consequences of these issues included problems with the start up of the Shunt-LDO circuitry at otherwise feasible working points. A more critical possible outcome was a too small value of the output voltage of the Shunt-LDO responsible for the analog domain, V_{DDA}. This voltage is responsible for supplying the CDR of RD53A, which has tight voltage requirements for operation. In effect this often could render RD53A not operational. The core design of the Shunt-LDO was shown to be much more mature in turn and - as shown by system test campaigns following the initial testing of RD53A - allows stable and reliable operation of RD53A in serially powered systems.

Accompanying the development and initial testing of RD53A, first large scale prototyping campaigns have been launched to verify serial powering from a system perspective for ATLAS ITk pixel. One of these campaigns is the Outer Barrel Demonstrator program. The Small Electrical Prototype, essentially a prototype of the final demonstrator, was commissioned with significant contributions in the context of this work. At the time, the Small Electrical prototype was the largest serial powering prototype to be built until eclipsed by the final demonstrator. Having to rely on older FE-I4 pixel modules limited how representative the demonstrator ultimately could be for ITk pixel, however, due to its impressive scale it offered perspectives not in reach for small scale prototypes. The demonstrator program not only yielded invaluable input in terms of the assembly, integration and operation of large serially powered detectors. In addition it raised awareness to features of a serially powered detector, which need to be investigated and addressed to ensure reliable operation of the detector. This input ultimately led to an expansion of the required feature set of the Shunt-LDO.

The Shunt-LDO for the final ATLAS and CMS production chips, commonly referred to as the RD53B Shunt-LDO, was in many regards a completely new circuit, which was prototyped in a series of three prototype chips, each integrating more features and improving on the previous versions. This new regulator design was characterised within the RD53 collaboration with significant contributions from this work. All new features of the Shunt-LDO could be verified, the performance of the core regulator improved upon the design in RD53A and the full circuit could be shown to be radiation hard well beyond the required TID of 500 Mrad by two X-ray irradiation campaigns to target TID of 800 Mrad and 2 Grad respectively.

The final project covered in this thesis was the integration and characterisation of a first serial powering prototype consisting of RD53A quad chip modules, powered by a

representative current source prototype. This prototype, much smaller in scale compared to the demonstrator with only a single serial powering chain 8 modules long, was aimed at low-level properties of serially powered pixel detectors and part of a larger effort within the ATLAS system test community, aiming to cover all aspects of serial powering. The prototype was fully developed and assembled at the Physics Institute of the University of Bonn. Using this prototype the performance of RD53A in a serial powering concept was demonstrated successfully. Experiences made with previous prototypes on FE-I4 basis could be verified. Despite its issues the Shunt-LDO offers a stable platform for a serially powered detector with no performance degradation compared to QA/QC tests [20]. Different schemes for the HV distribution in the ITk pixel detectors have been tested and showed no impact on the module performance. Investigations of the interplay between power supplies in a serial powering chain, especially focusing on the off-mode of the HV power supply, have been conducted. These investigations, to be understood in the context of the OBD and [33], provide no evidence for potential harmful interactions between the HV supply and the serial powering chain. The prototype showed its potential use in refining the Shunt-LDO configuration in the terms of its working point. This will allow for additional optimisations of the power efficiency in the upcoming ITkPix modules. This is aided by the design of the prototype services, which are compatible to ITkPix modules to allow a quick transition to the most recent ROC.

At the time of writing, the RD53A serial powering stave has transitioned to a serial powering chain of digital ITkPix quad modules. A measurement program has started which will provide immediate input for the specifications of the LV power supplies for ITk pixel. In the near future the setup will be loaded with fully functional ITkPix quad modules and represent an important part in the final serial powering system tests for ITk pixel.

Appendix - Shunt-LDO Characterization

This appendix contains additional measurements expanding on the results presented in Section 4. In Section A.1 additional results from measurements with the 2 A Shunt-LDO prototype chip are shown. Section A.2 contains additional material and results concerning the measurements performed with the RD53A Shunt-LDO presented in Section 4.2. In Section A.3 additional material for the characterization of the RD53B Shunt-LDO prototype chip B can be found. Supplementary plots for two irradiation campaigns conducted with the RD53B Shunt-LDO prototype chip B are found in Section A.4.

A.1 2 A Prototype

Figure A.1 shows measurements of the Shunt-LDO at different ambient temperatures performed in a climate chamber. The temperatures were measured at a heat sink mounted to the backside of the PCB. In Figure A.1(a) line regulation measurements over the full temperature range are shown. Figure A.1(b) shows the load regulation measurements at different temperatures. As all measured voltages are referenced to the PCB GND, V_{out} shows a negative impedance behaviour due to GND shifts. Figure A.1(c) shows the Shunt-LDO output voltage working point at different temperatures for static load currents of $I_{\text{load}} = 0\,\text{A}$, $I_{\text{load}} = 0.4\,\text{A}$ and $I_{\text{load}} = 0.8\,\text{A}$. For these measurements the Shunt-LDO was supplied with a constant input current $I_{\text{in}} = 0.86\,\text{A}$, $V_{\text{ref}} = 0.6\,\text{V}$ and $V_{\text{ofs}} = 0.8\,\text{V}$. For higher load currents the temperature drift is smaller.
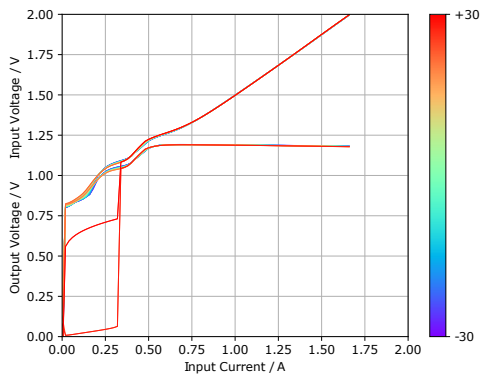
(a) Line regulation of the 2 A Shunt-LDO prototype chip at different temperatures
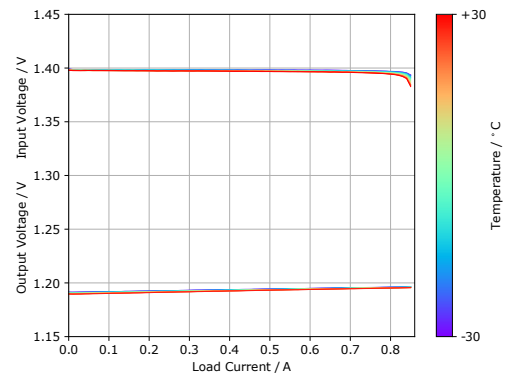
(b) Load regulation of the 2 A Shunt-LDO prototype chip at different temperatures
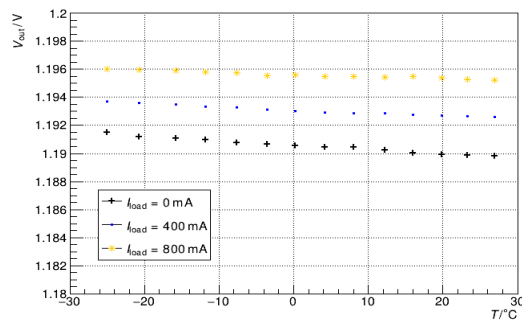
(c) V_{out} of the 2 A Shunt-LDO prototype chip at different temperatures and load currents

Figure A.1: Measurements of the temperature behaviour of the Shunt-LDO in a climate chamber with ambient temperatures ranging from $-30\,°\text{C} \leq T \leq 30\,°\text{C}$.

A.2 RD53A

Figure A.2 shows the schematic of the bandgap reference circuit used in RD53A. This circuit itself is powered by the output voltage of the digital Shunt-LDO V_{DDD}. Additionally shown is the principle schematic for the generation of the reference voltage for RD53A's on-chip analog-to-digital converter, which is essential for monitoring purposes. Both R_3 and R_4 can be either adjusted by configuration bits on-chip or defined by using off-chip resistors, e.g. SMD on a module flex, instead. With a typical bandgap output voltage of 400 mV a gain of approximately 2.25 is needed to achieve $V_{refADC} = 900$ mV.
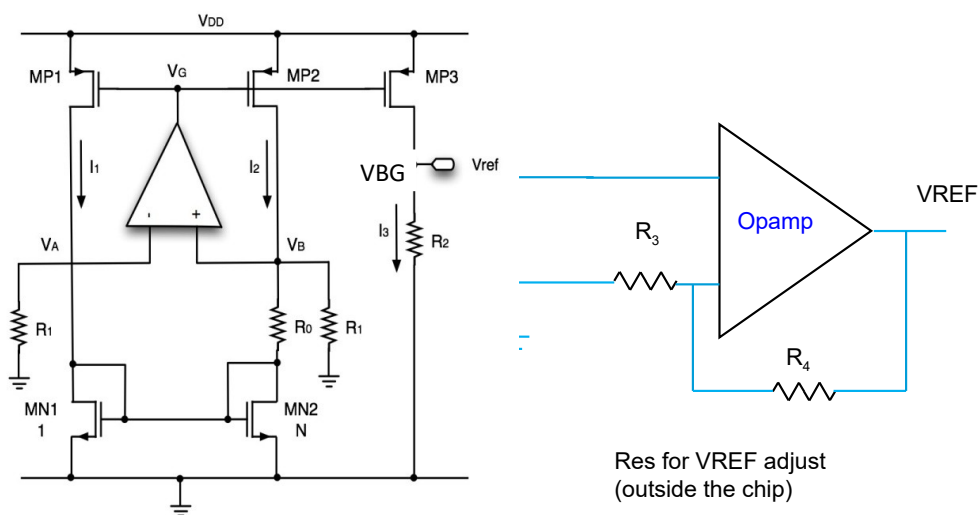
Figure A.2: On the left: bandgap reference of the RD53A providing reference voltages for critical components, e.g. the Shunt-LDO. On the right the general principle for the generation of the on-chip analogue-digital-converter is shown. Taken from [39].

In Figure A.3 and Figure A.4 the collected results from line fits to the input IV curves of the RD53A Shunt-LDO from wafer probing are shown as are published in [20]. Color coding gives the preliminary binning of chips with respect to the measured quantity. To circumvent issues with a delayed bandgap startup, the IV curves for this measurement were measured starting from high input currents and ramping down, increasing the linear range available for analysis. Nonetheless not all RD53A chips started up properly, leading to fit results far off from acceptable values.

Figure A.5 shows the default values for V_{DDA} and V_{DDD} upon startup of RD53A. Naturally only chips with a successful bandgap startup are included. By design both V_{DDA} and V_{DDD} should be centered around 1.2 V. Trim bits for the regulator output voltages allow fine tuning

(a) $R_{\text{eff,A}}$

(b) $R_{\text{eff,D}}$
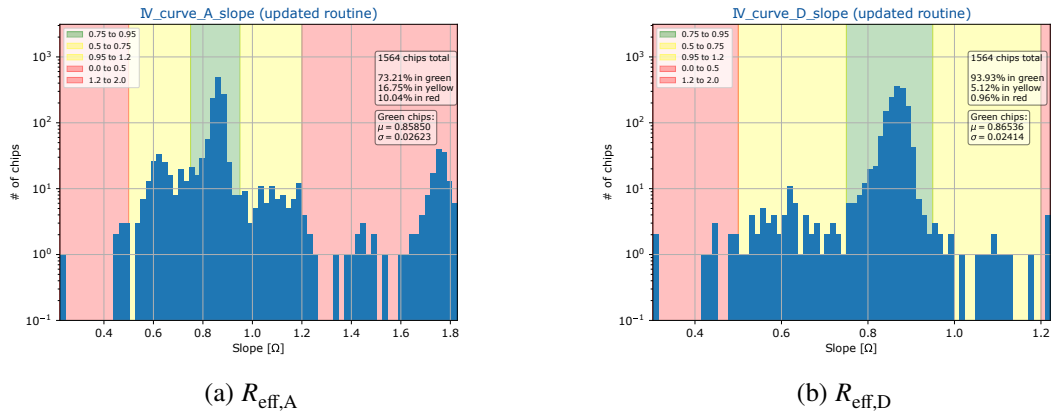
Figure A.3: Distribution of R_{eff} for analog and digital Shunt-LDO from wafer probing taken from [20].

(a) $V_{\text{ofs,A}}$

(b) $V_{\text{ofs,D}}$
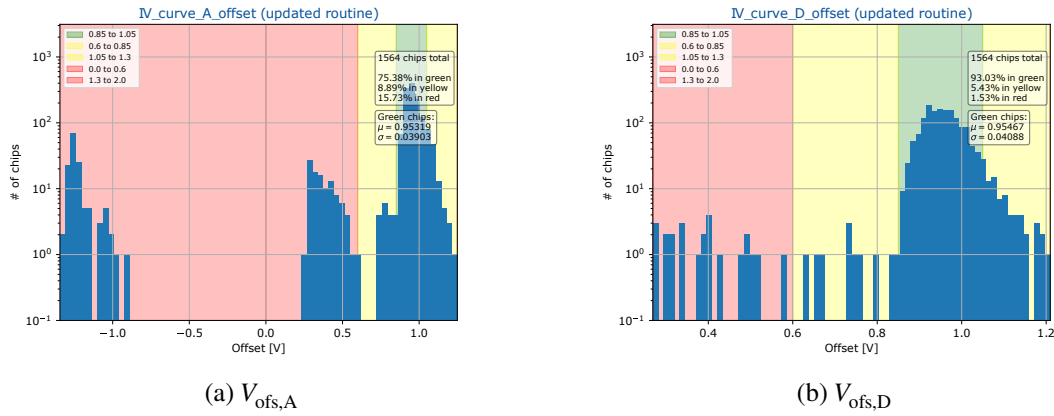
Figure A.4: Distribution of V_{ofs} for analog and digital Shunt-LDO from wafer probing taken from [20].

of V_{DDA} and V_{DDD} once communication with the ROC is established.

In Figure A.6 and Figure A.7 the voltage steering precision for V_{DDA} and V_{DDD} determined using wafer probing data is shown. Ideally both distributions should be centered around a ratio $\frac{V_{\text{DD}}}{V_{\text{Ref}}} = 2$.

(a) V_{DDA} (b) V_{DDD}
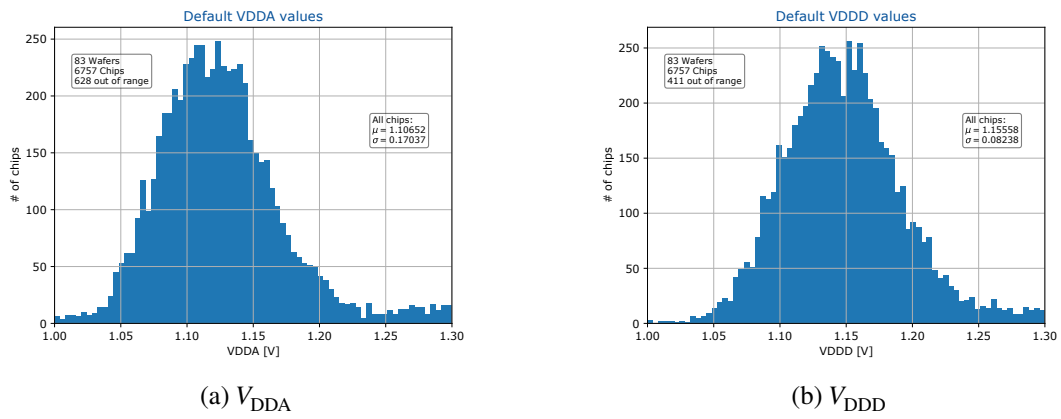
Figure A.5: Distribution of untrimmed V_{DDA} and V_{DDD} upon regulator startup as recorded during wafer probing taken from [20].
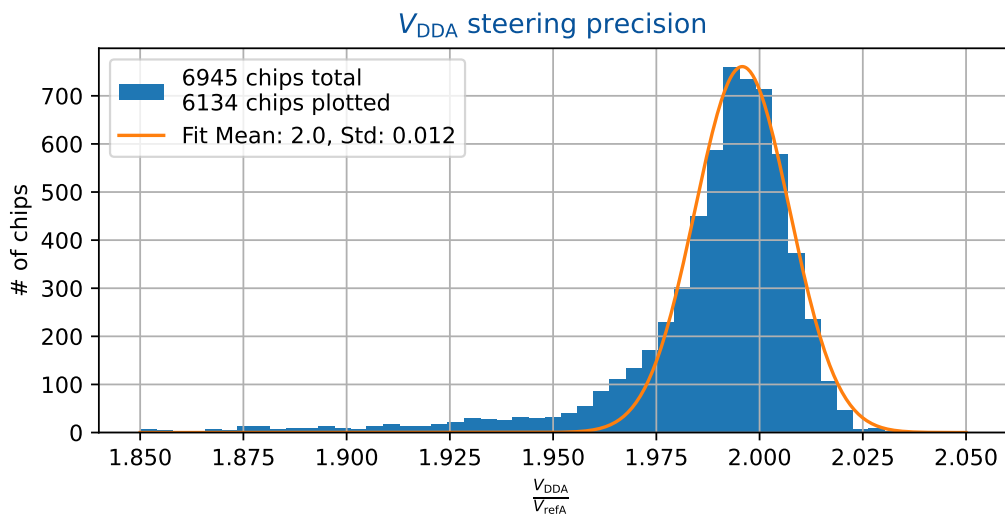
Figure A.6: Analog output voltage steering precision in RD53A from wafer probing data.
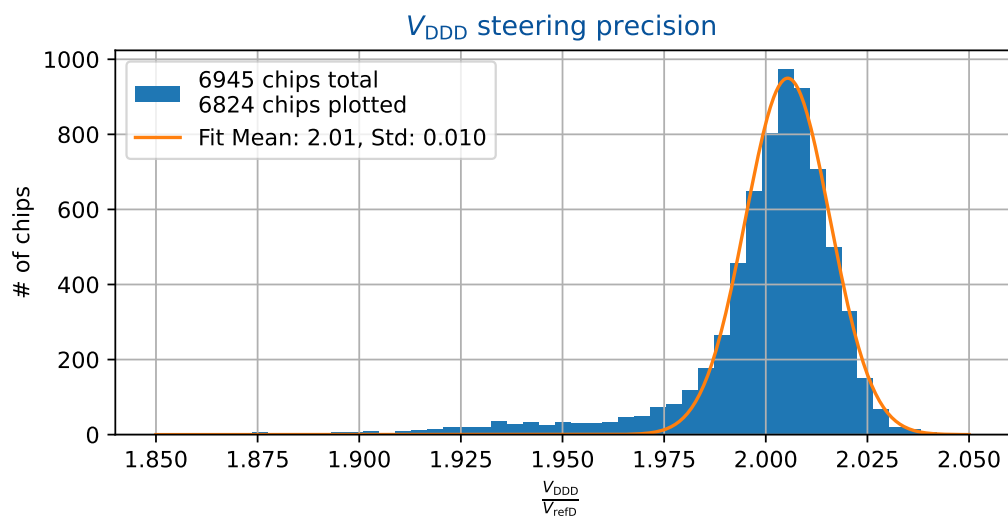
Figure A.7: Digital output voltage steering precision in RD53A from wafer probing data.
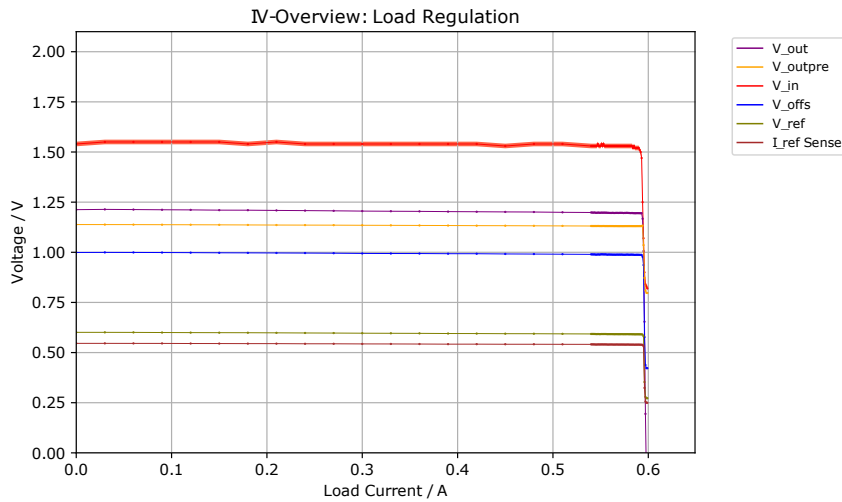
Figure A.8: Full load regulation curve measured with an RD53B Shunt-LDO test chip B, taken from [48]. I_{ref} is measured as a voltage drop across a $150\,\text{k}\Omega$ resistor.

A.3 RD53B Test Chip B

Figure A.8 shows a load regulation measurement with an RD53B prototype Shunt-LDO with the UCP switched off. Without the UCP mitigating overload situations, a complete collapse of all Shunt-LDO voltages can be seen.

In Figure A.9, Figure A.10 and Figure A.11 some measurements of the temperature dependence of the RD53B Shunt-LDO performed in [48] are shown. A significant dependence of V_{ofs} on the chip temperature can be seen, which translates into differing input IV curves at different temperatures.
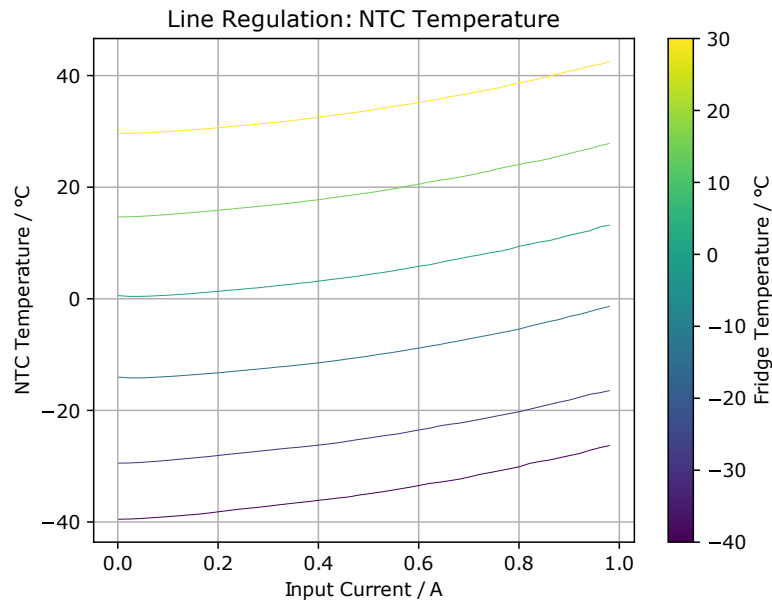
Figure A.9: Shunt-LDO chip temperature from NTC in line regulation measurement in different ambient temperatures. Taken from [48].
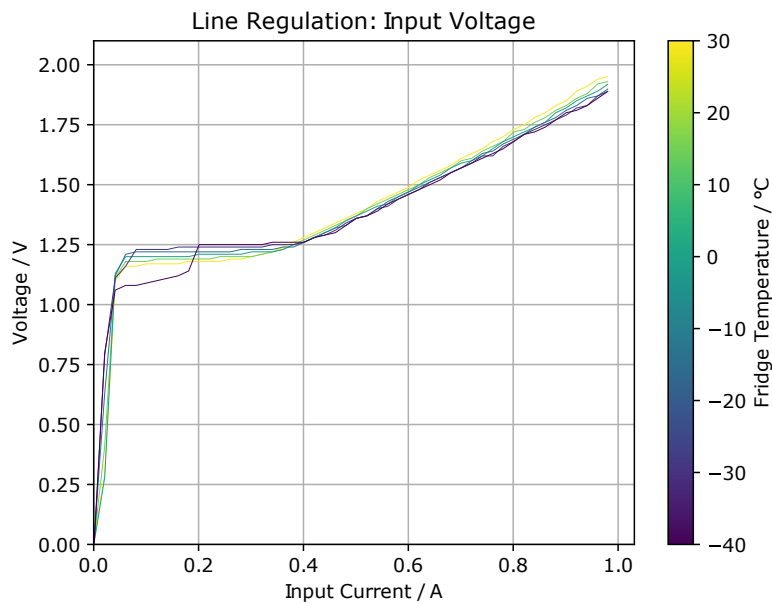
Figure A.10: Shunt-LDO V_{in} during line regulation measurement in different ambient temperatures. Taken from [48].
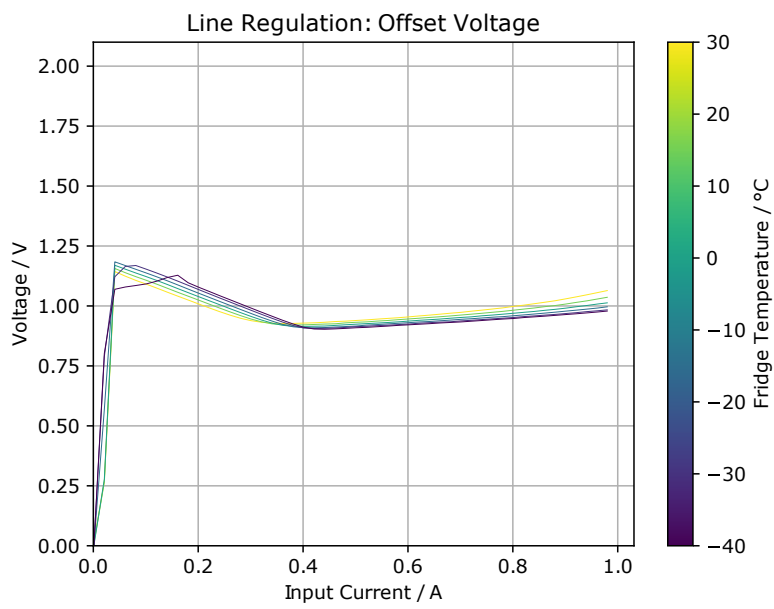
Figure A.11: Shunt-LDO V_{ofs} during line regulation measurement in different ambient temperatures. Taken from [48].
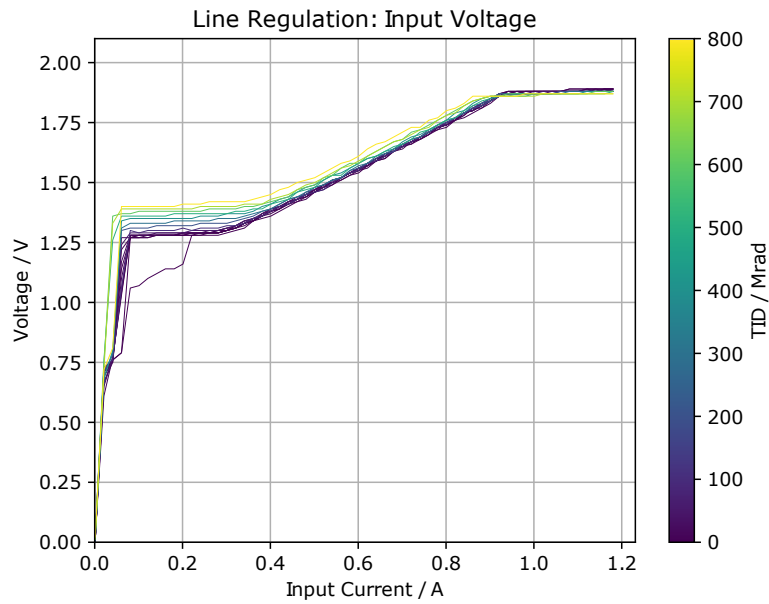
Figure A.12: Shunt-LDO V_{out} during line regulation measurement over the course of the irradiation campaign at $-10\,°C$. Taken from [48].

A.4 RD53B Test Chip B Irradiation

In the following sections supplementary plots with data from the two X-ray irradiation campaigns conducted with the RD53B Shunt-LDO in the context of this thesis.

A.4.1 Cold Irradiation Campaign

In Figure A.13 - Figure A.23 plots of the various quantities measured in line- and load regulation measurements during the RD53B Shunt-LDO irradiation at $-10\,°C$ are shown as a function of TID.
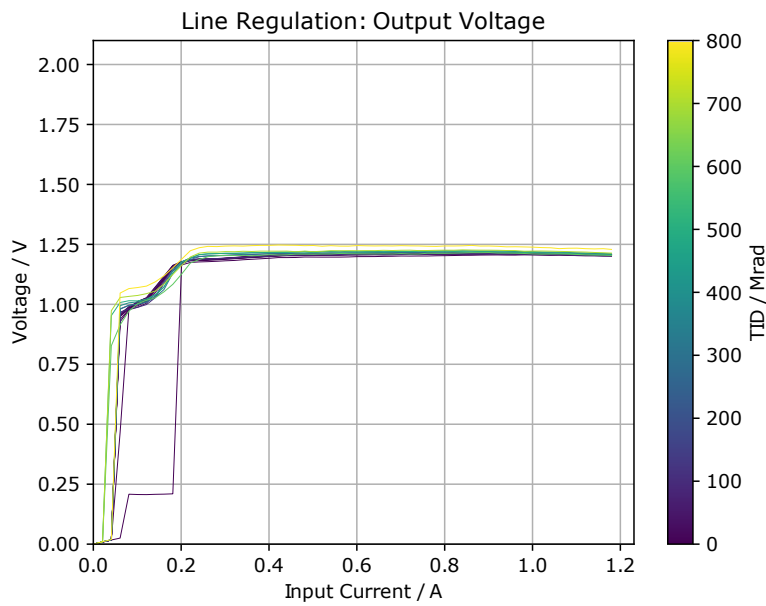
Figure A.13: Shunt-LDO V_{ref} during line regulation measurement over the course of the irradiation campaign at −10 °C. Taken from [48].
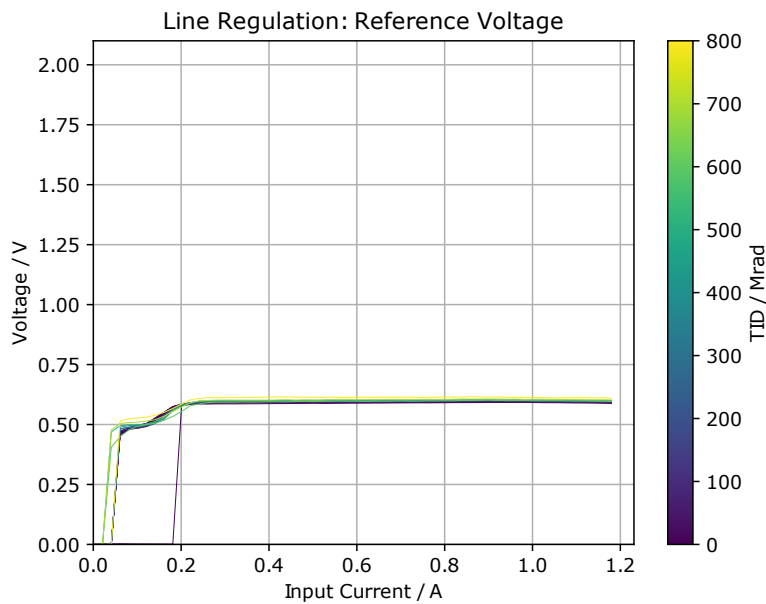
Figure A.14: Shunt-LDO V_{ref} during line regulation measurement over the course of the irradiation campaign at −10 °C. Taken from [48].
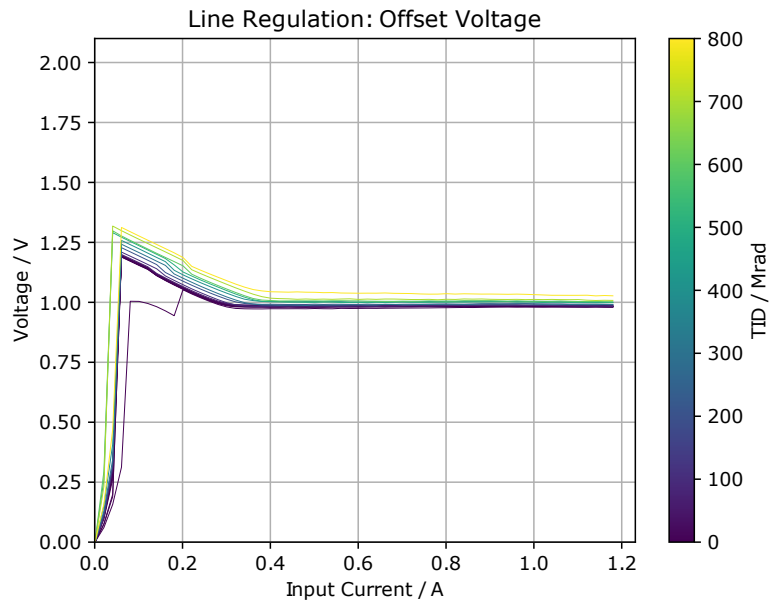
Figure A.15: Shunt-LDO V_{ofs} during line regulation measurement over the course of the irradiation campaign at $-10\,°\mathrm{C}$. Taken from [48].
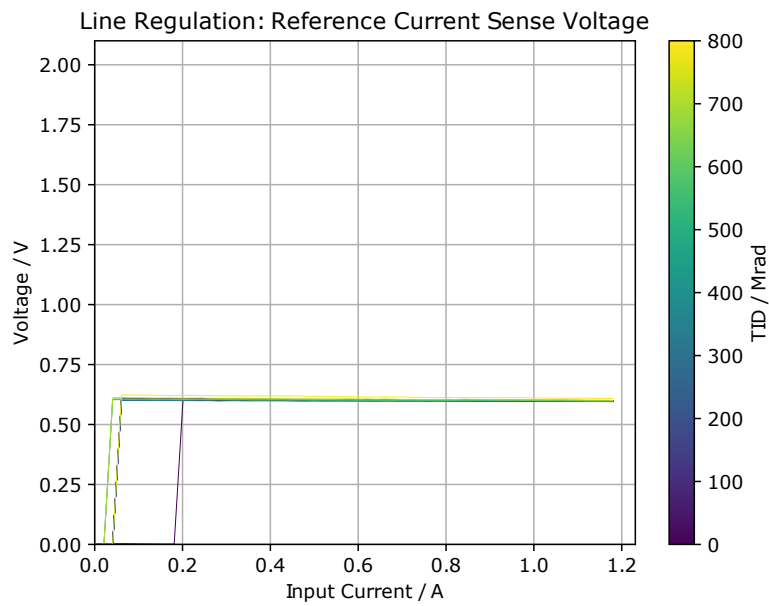
Figure A.16: Shunt-LDO I_{ref} during line regulation measurement over the course of the irradiation campaign at $-10\,°\mathrm{C}$. I_{ref} is measured as a voltage drop across a $150\,\mathrm{k\Omega}$ resistor. Taken from [48].
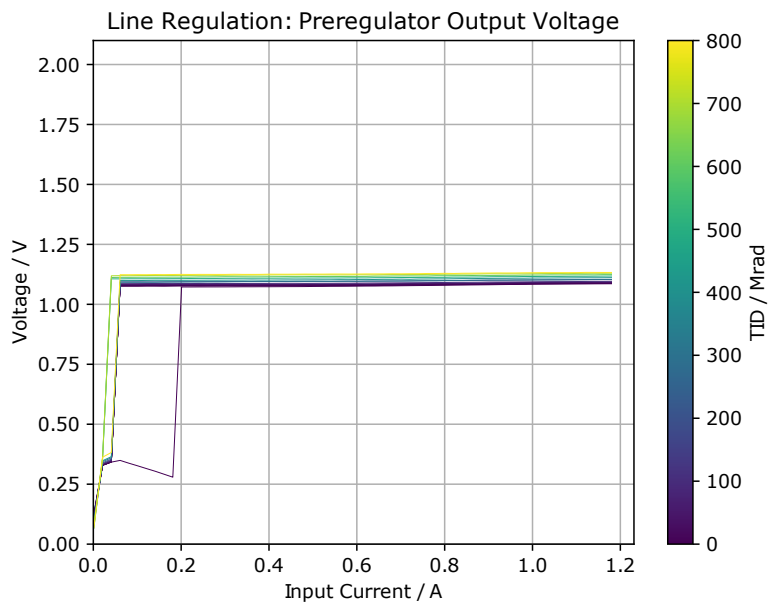
Figure A.17: Shunt-LDO V_{DDPre} during load regulation measurement over the course of the irradiation campaign at −10 °C. Taken from [48].
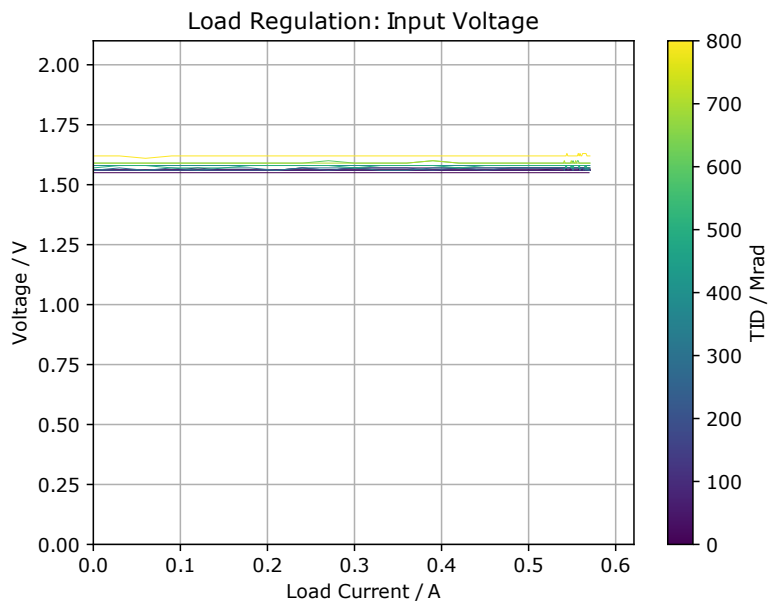
Figure A.18: Shunt-LDO V_{in} during load regulation measurement over the course of the irradiation campaign at −10 °C. Taken from [48].
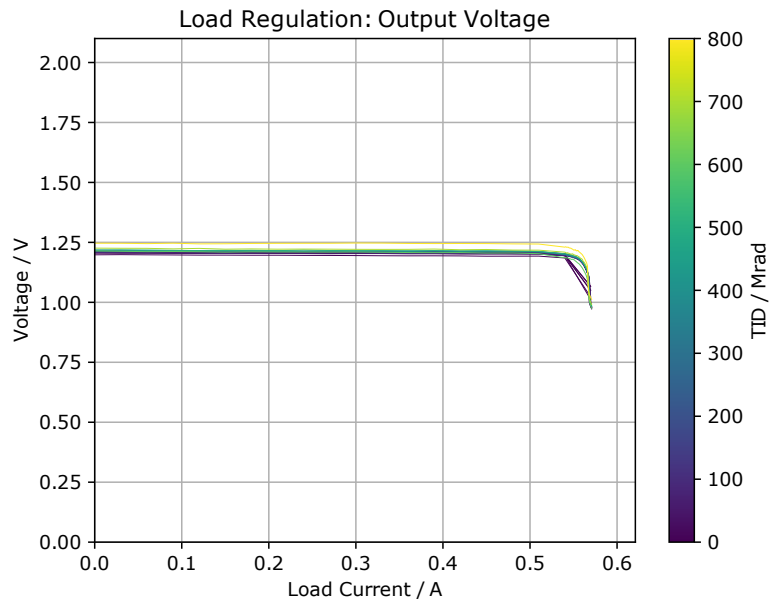
Figure A.19: Shunt-LDO V_{out} during load regulation measurement over the course of the irradiation campaign at $-10\,°\text{C}$. Taken from [48].
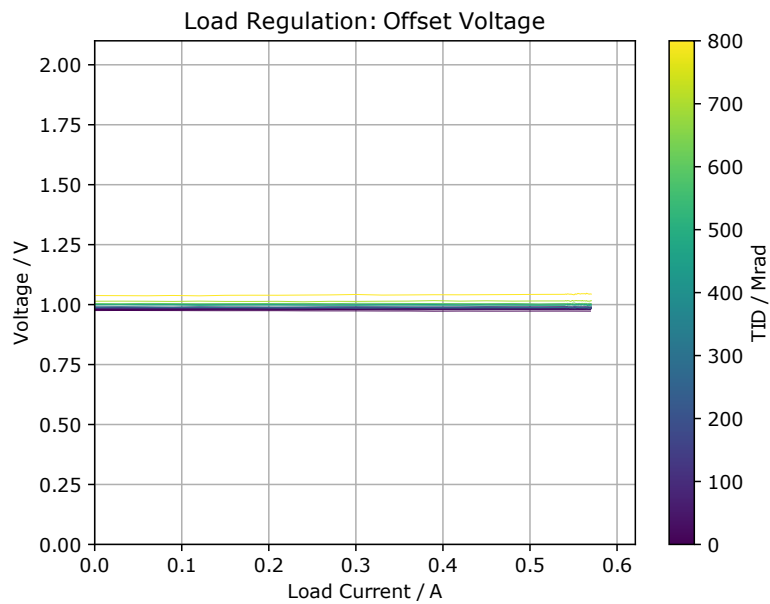
Figure A.20: Shunt-LDO V_{ofs} during load regulation measurement over the course of the irradiation campaign at $-10\,°\text{C}$. Taken from [48].
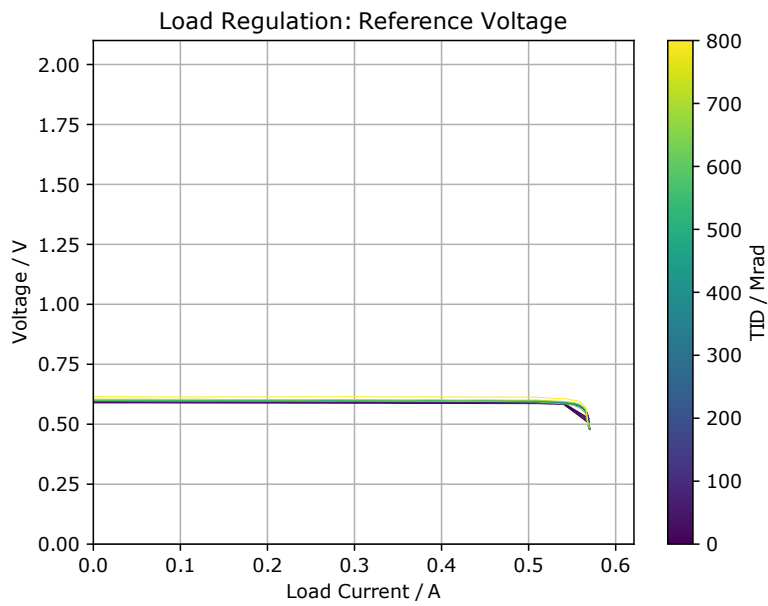
Figure A.21: Shunt-LDO V_{ref} during load regulation measurement over the course of the irradiation campaign at $-10\,°C$. Taken from [48].
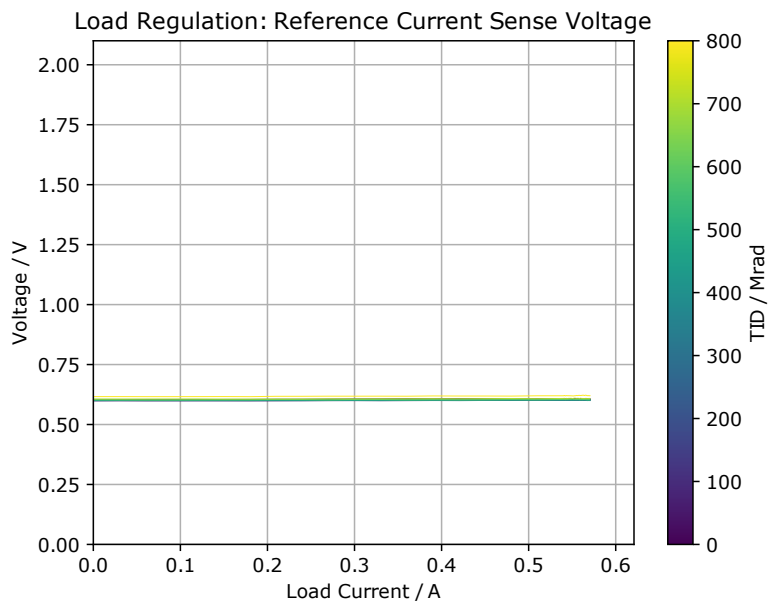
Figure A.22: Shunt-LDO I_{ref} during load regulation measurement over the course of the irradiation campaign at $-10\,°C$. I_{ref} is measured as a voltage drop across a $150\,k\Omega$ resistor. Taken from [48].
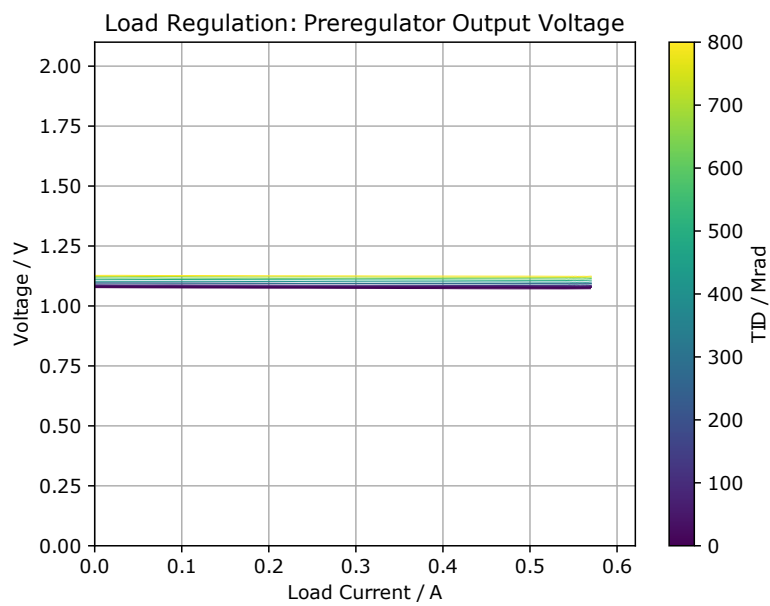
Figure A.23: Shunt-LDO V_{DDPre} during line regulation measurement over the course of the irradiation campaign at $-10\,^\circ\mathrm{C}$. Taken from [48].
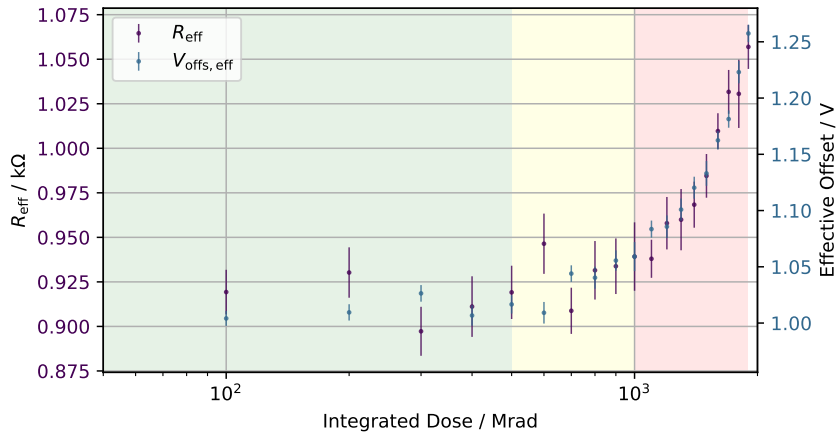
Figure A.24: R_{eff} and V_{ofs} extracted from input IV measurement during warm irradiation of the RD53B Shunt-LDO test chip B. The TID limit required by the Shunt-LDO specifications is color coded *green*.

A.4.2 Warm Irradiation Campaign

The procedure of the irradiation campaign at warm temperatures, referring to a chip temperature of $0\,°\text{C}$, is mostly identical to the irradiation campaign discussed in Section 4.3. Measurement setup and infrastructure are identical between the different irradiation campaigns. Due to timing constraints during this campaign a reduced measurement program was followed: the TID steps between measurements were set at $100\,\text{Mrad}$ and all measurements needed to be possible to be done remotely. As such, the UCP was not followed during this campaign, as the oscilloscope would have to be (dis)connected before and after each measurement as mentioned in Section 4.3. The maximum target TID of this campaign was $2\,000\,\text{Mrad}$, exceeding the design radiation hardness of the Shunt-LDO.

From the collected V_{in} data from line regulation measurements, the effective slopes and offsets, R_{eff} and V_{ofs} are determined and shown in Figure A.24. Over the initial range of TID, R_{eff} and V_{ofs} remain fairly consistent. Only after reaching the required target TID of $500\,\text{Mrad}$ V_{ofs} is increasing. For very large TID exceeding $1\,000\,\text{Mrad}$ both R_{eff} and V_{ofs} start to increase significantly. In Figure A.25 the temperature measurement performed on the NTC as well as a log of the k factor over the course of the irradiation campaign is shown. For large TID the current mirror ratio k starts to decrease more and more significantly, corresponding to the observed increase in R_{eff}. The line- and load regulation performance are shown in Figure A.26. Both are performing slightly worse compared to the irradiation campaign discussed in Section 4.3. Nonetheless even for very large TID the Shunt-LDO shows acceptable line- and load regulation performance.

In Figure A.27 the development of the Shunt-LDO working point during the irradiation campaign is shown. For TID below $1\,000\,\text{Mrad}$ the working point remains largely constant
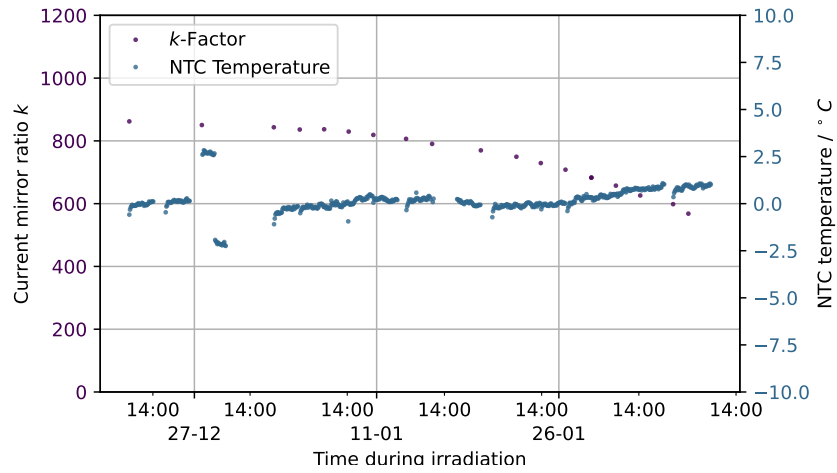
Figure A.25: Temperature and k-factor logging during warm irradiation of the RD53B Shunt-LDO test chip B. Each measurement point of the k-factor coincides with one 100 Mrad irradiation step.
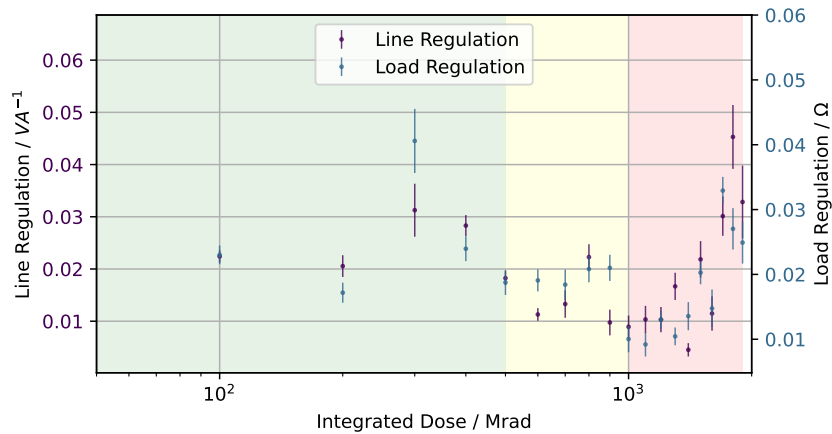
Figure A.26: Line- and load regulation extracted during warm irradiation (at 0 °C) of the RD53B Shunt-LDOtest chip B. The TID limit required by the Shunt-LDO specifications is color coded *green*.

as expected from Section 4.3. Only for very large TID the working point starts drifting significantly. As the Shunt-LDO is not intended to be accumulating TID in excess of 1 000 Mrad at any point during the operation of ITk pixel, this is not of concern.
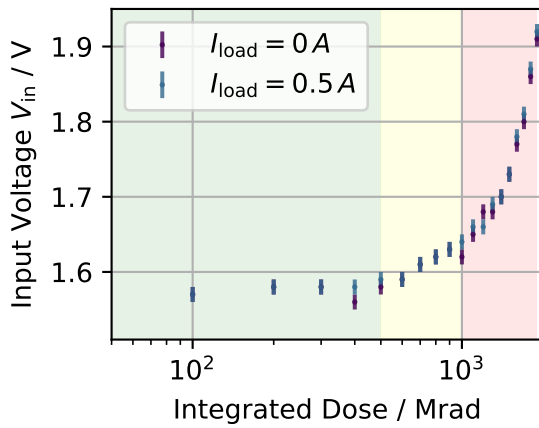
(a) Input voltage V_{in} as function of TID
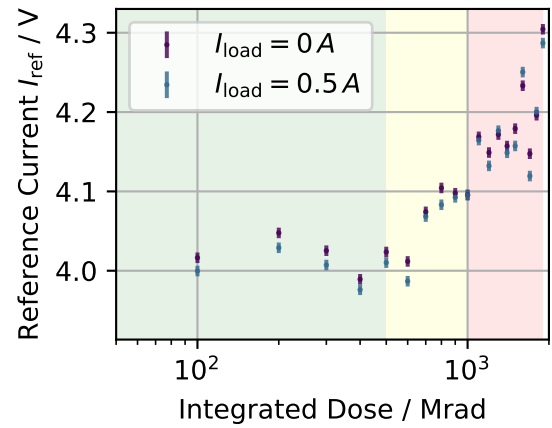
(b) Reference current I_{ref} as function of TID
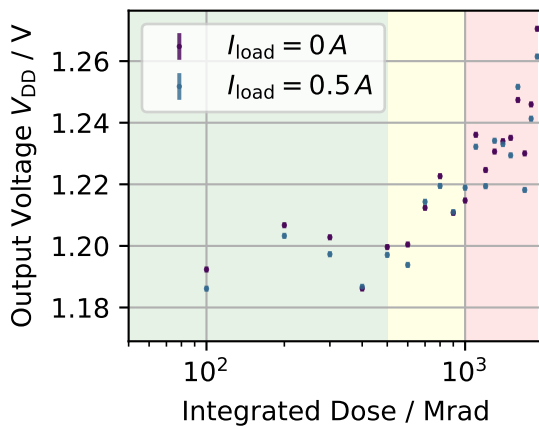
(c) Output voltage V_{DD} as function of TID
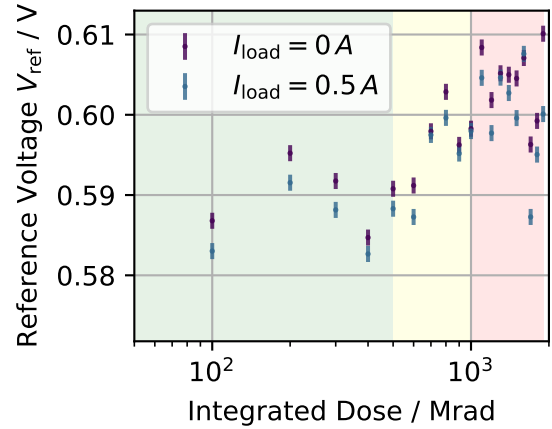
(d) Reference voltage V_{ref} as function of TID
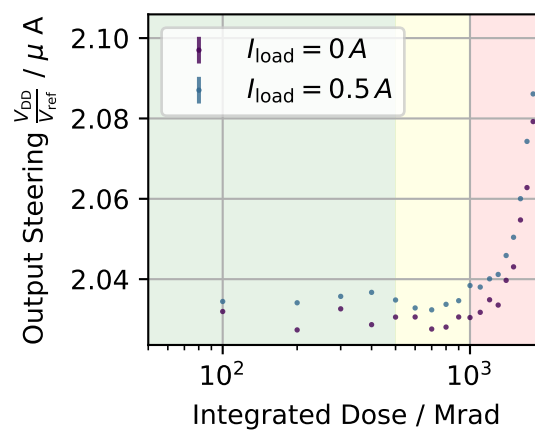
(e) Output steering at working point as function of TID

Figure A.27: V_{in}, V_{out} and the references V_{ref} and I_{ref} as function of TID at an operating point $I_{in} = 0.6$ A with both no load current drawn and a load current of 0.5 A.

Appendix - Large Scale Serial Powering Prototypes for the ITk Pixel Detector

In this section supplementary material for the serial powering prototype with RD53A modules, discussed in Section 5.2. Section B.1 expands on the module performance measurements presented in Section 5.2.1. Section B.2 contains the sensor IV curves obtained during the reception tests for the RD53A quad modules loaded on the serial powering stave. In Section B.3 supplementary plots from the characterisation of the RD53A quad modules in serial powering operation can be found.

B.1 An RD53A Quad Module for Serial Chain Operation

In Figure B.1 an analog scan of module SPQ15 with leakage current compensation disabled is shown. Due to the sensor design in conjunction with the different AFE on RD53A, pixel in the periphery of the DIFF AFE are stuck, no hits are recorded.
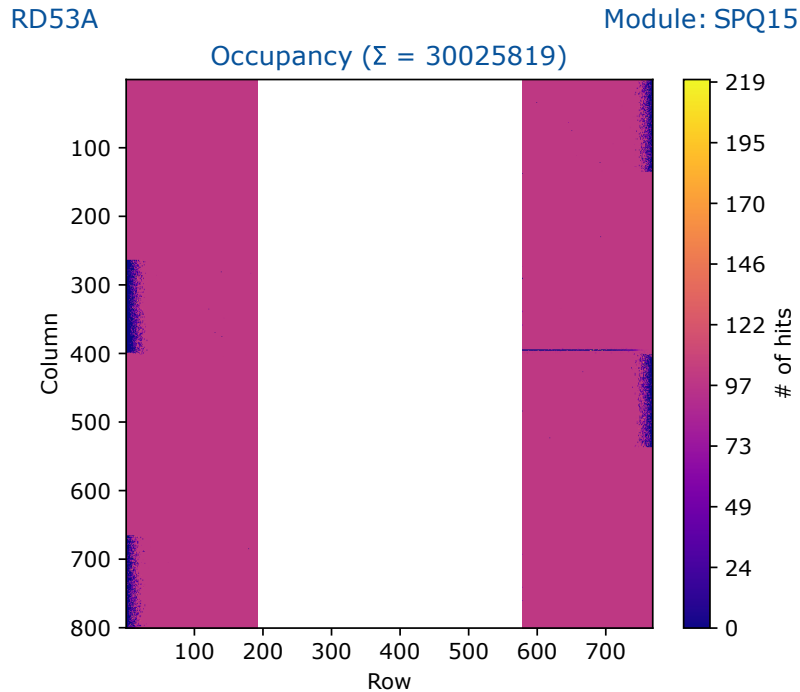
Figure B.1: Analog scan of quad module SPQ15 with LCC disabled.

A comparison of the threshold performance and ENC of SPQ15 between Shunt-LDO mode and LDO mode of operation can be found in Table B.1 and Table B.2. The corresponding mean threshold and ENC distributions measured in LDO mode are shown in Figure B.2 and Figure B.3.   In agreement with the measurements with digital quad modules discussed in Section B.1 no performance difference can be observed between different modes of operation. In particular the observed noise levels and noisy periphery of the DIFF AFE do not significantly depend on the powering mode.
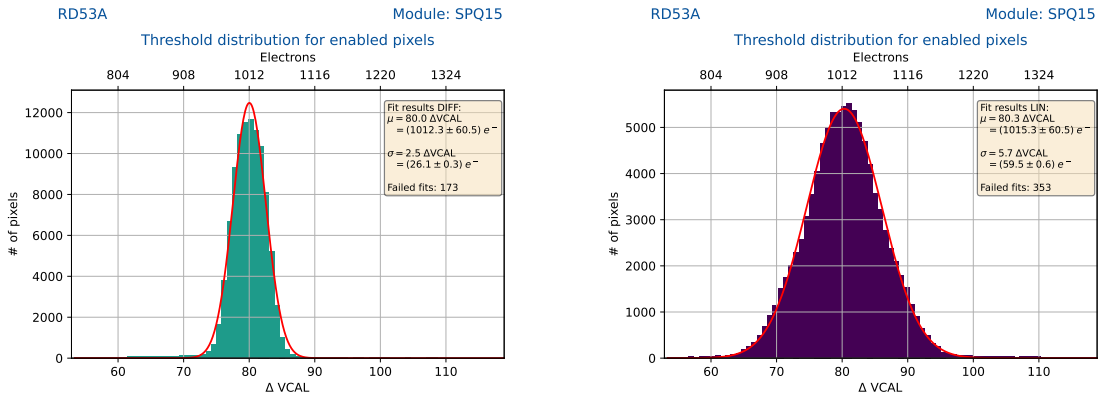
(a) Threshold distribution of SPQ15, DIFF AFE, after tuning to a target threshold of $1\,000\,e^-$.

(b) Threshold distribution of SPQ15, LIN AFE, after tuning to a target threshold of $1\,000\,e^-$.

Figure B.2: Threshold distribution for all enabled pixels in SPQ9, LIN and DIFF flavours, after tuning to $1\,000\,e^-$

.
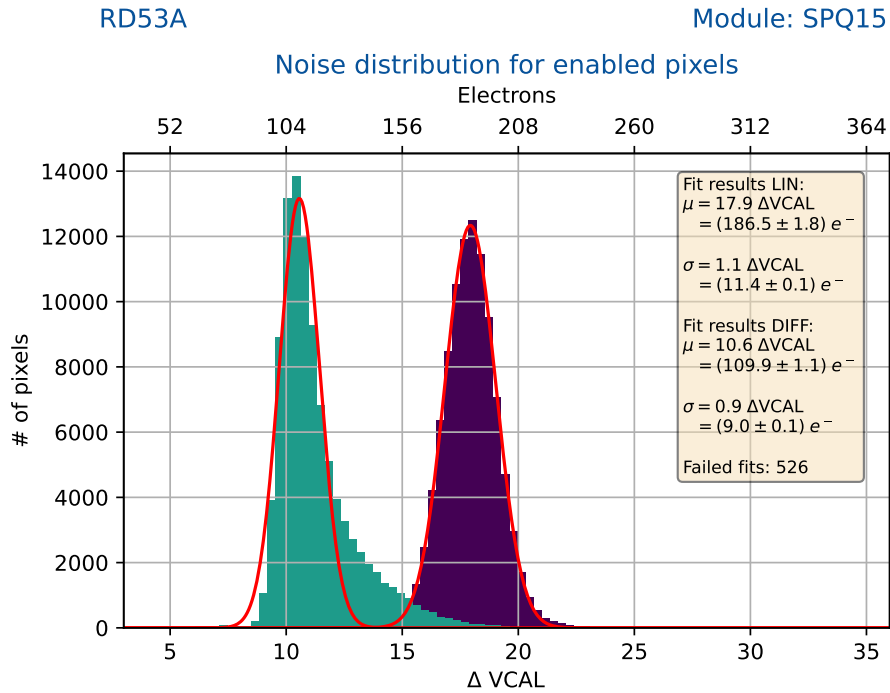
Figure B.3: ENC distribution of SPQ15, LIN and DIFF AFE, after tuning to a target threshold of $1\,000\,e^-$. Module operated in LDO mode.

	SPQ15 Shunt-LDO	SPQ15 LDO
Threshold mean LIN AFE	$(1\,004.9 \pm 60.5)\,e^-$	$(1\,015.3 \pm 60.5)\,e^-$
Threshold width LIN AFE	$(65.0 \pm 0.6)\,e^-$	$(59.5 \pm 0.6)\,e^-$
Threshold mean DIFF AFE	$(1\,008.0 \pm 60.5)\,e^-$	$(1\,012.3 \pm 60.5)\,e^-$
Threshold width DIFF AFE	$(28.1 \pm 0.3)\,e^-$	$(26.1 \pm 0.3)\,e^-$

Table B.1: Threshold performance comparison of RD53A digital quad module SPQ15 in Shunt-LDO mode with measurements of SPQ15 in LDO mode. All chips tuned to a detection threshold of $1\,000\,e^-$.

	SPQ15 Shunt-LDO	SPQ15 LDO
Noise mean LIN AFE	$(202.4 \pm 1.9)\,e^-$	$(186.5 \pm 1.8)\,e^-$
Noise width LIN AFE	$(17.2 \pm 0.2)\,e^-$	$(11.4 \pm 0.1)\,e^-$
Noise mean DIFF AFE	$(112.7 \pm 1.1)\,e^-$	$(109.9 \pm 1.1)\,e^-$
Noise width DIFF AFE	$(7.8 \pm 0.1)\,e^-$	$(9.0 \pm 0.1)\,e^-$

Table B.2: ENC comparison of RD53A digital quad module SPQ15 in Shunt-LDO mode with measurements of SPQ15 in LDO mode. All chips tuned to a detection threshold of $1\,000\,e^-$.

B.2 Reception Tests

Figure B.4 and Figure B.5 shows the sensor IV curves measured for all RD53A quad modules loaded on the serial powering stave.
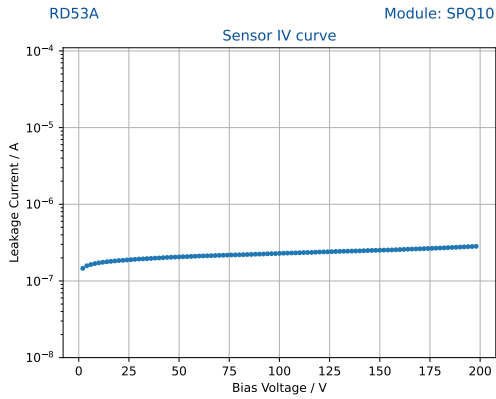
(a) SPQ10 Sensor IV curve.
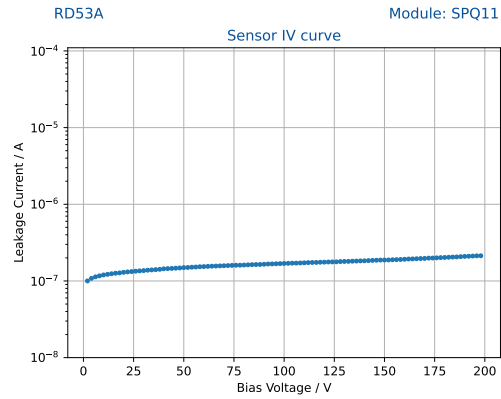
(b) SPQ11 Sensor IV curve.
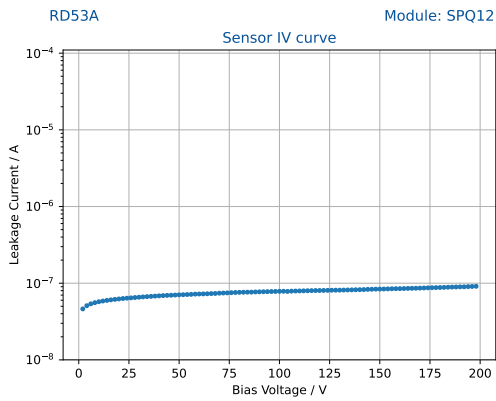
(c) SPQ12 Sensor IV curve.
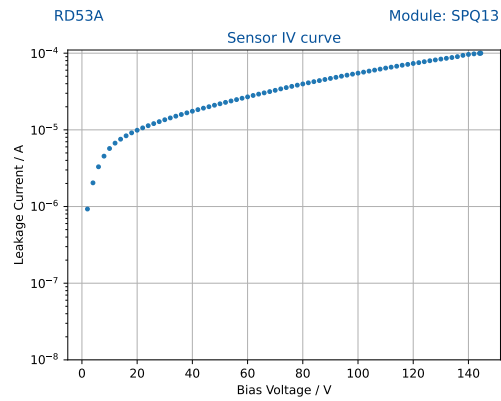
(d) SPQ13 Sensor IV curve.

Figure B.4: Quad module sensor IV curves for modules SPQ10-SPQ13 measured during reception tests.
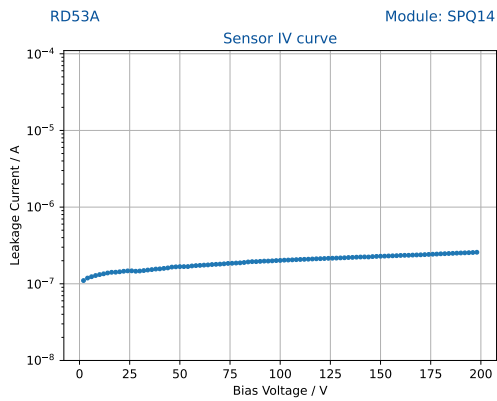
(a) SPQ14 Sensor IV curve.
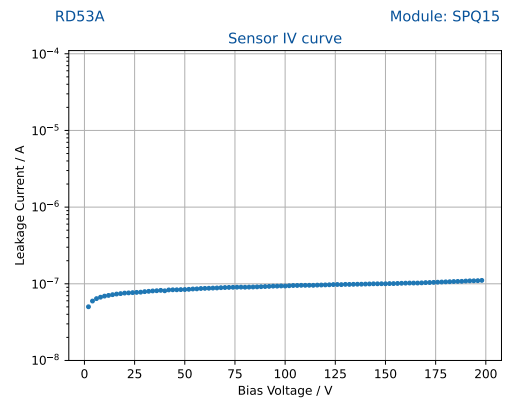
(b) SPQ15 Sensor IV curve.
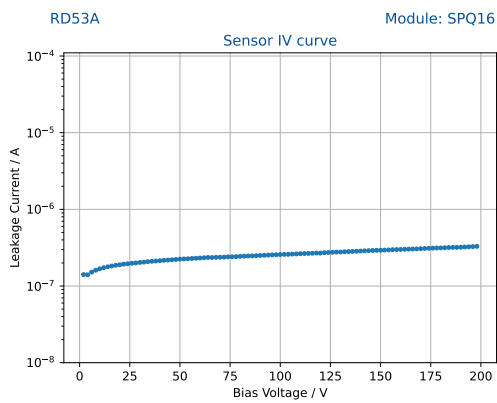
(c) SPQ16 Sensor IV curve.
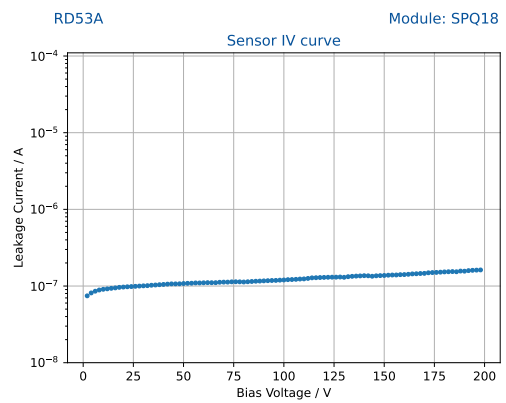
(d) SPQ18 Sensor IV curve.

Figure B.5: Quad module sensor IV curves for modules SPQ14-SPQ18 measured during reception tests.

B.3 Characterisation of an RD53A Serial Powering Chain: Shunt-LDO Measurements

The following Figues B.6 - B.12 show all Shunt-LDO input IV curves measured on the RD53A serial powering stave using the on-chip voltage multiplexer. V_{in} is measured using sense pins on the module flex. Additionally the expected input IV curve is marked in red, which is extracted from available wafer probing data. SPQ10 has faulty Shunt-LDO and is thus not shown. SPQ16 has faulty voltage multiplexer for two ROC, thus reading out only near-zero values for all local voltages.

(a) FE0, analog Shunt-LDO.
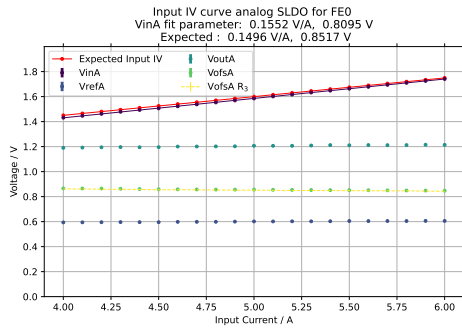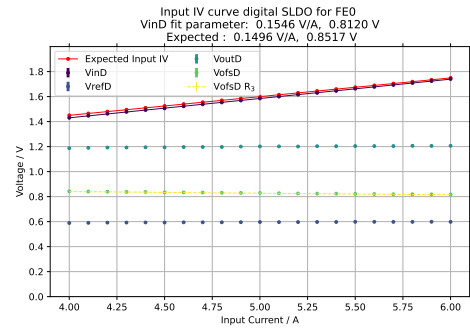
(b) FE0, digital Shunt-LDO.
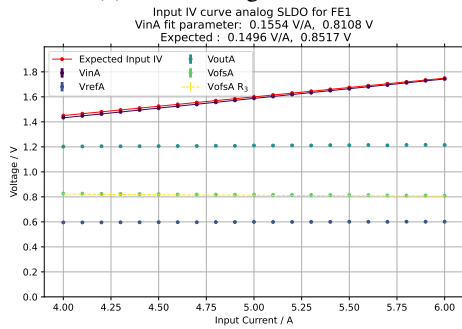
(c) FE1, analog Shunt-LDO.
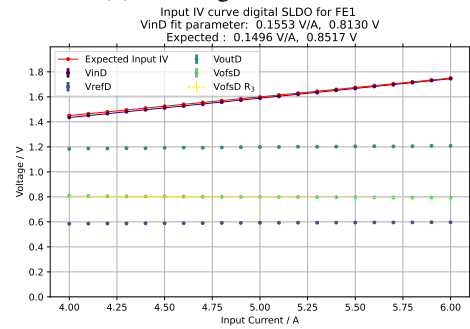
(d) FE1, digital Shunt-LDO.
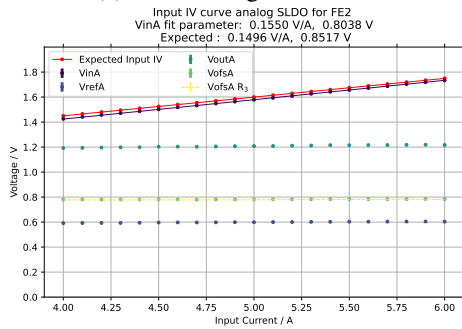
(e) FE2, analog Shunt-LDO.
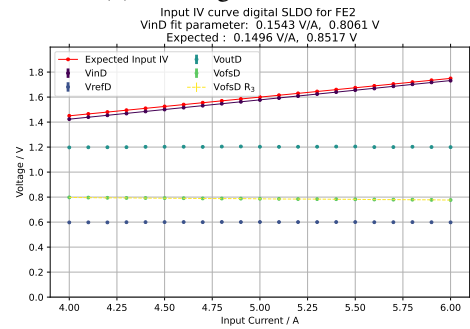
(f) FE2, digital Shunt-LDO.
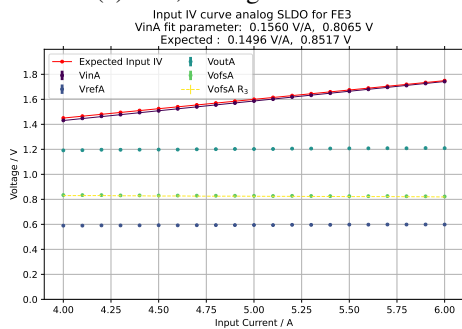
(g) FE3, analog Shunt-LDO.
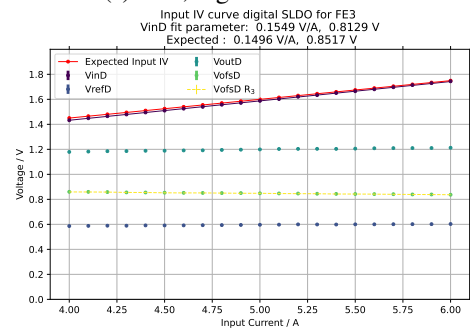
(h) FE3, digital Shunt-LDO.

Figure B.6: Shunt-LDO Input IV curve measurements of SPQ11.

(a) FE0, analog Shunt-LDO.

(b) FE0, digital Shunt-LDO.

(c) FE1, analog Shunt-LDO.

(d) FE1, digital Shunt-LDO.

(e) FE2, analog Shunt-LDO.

(f) FE2, digital Shunt-LDO.

(g) FE3, analog Shunt-LDO.

(h) FE3, digital Shunt-LDO.

Figure B.7: Shunt-LDO Input IV curve measurements of SPQ12.

(a) FE0, analog Shunt-LDO.
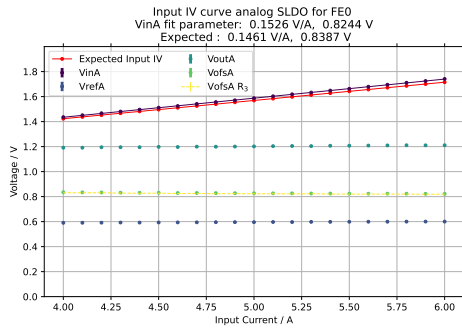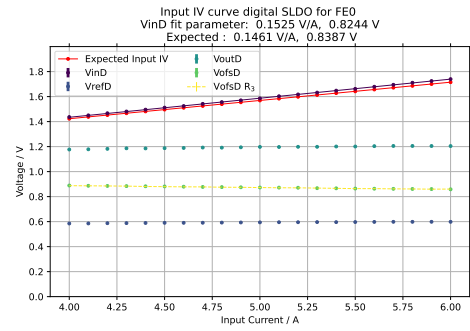
(b) FE0, digital Shunt-LDO.
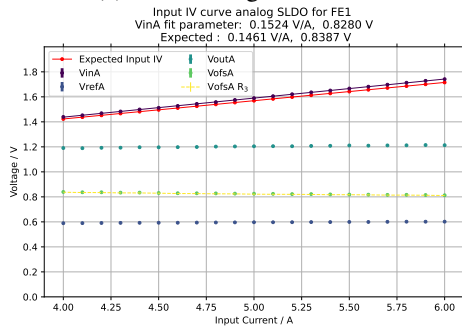
(c) FE1, analog Shunt-LDO.
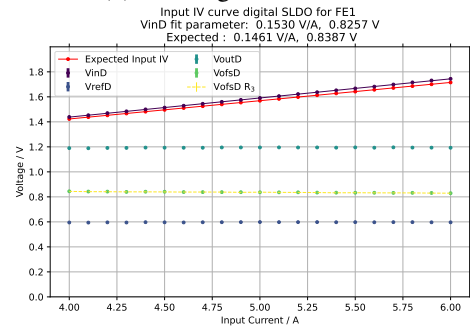
(d) FE1, digital Shunt-LDO.
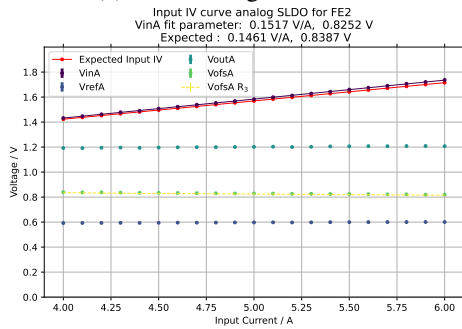
(e) FE2, analog Shunt-LDO.
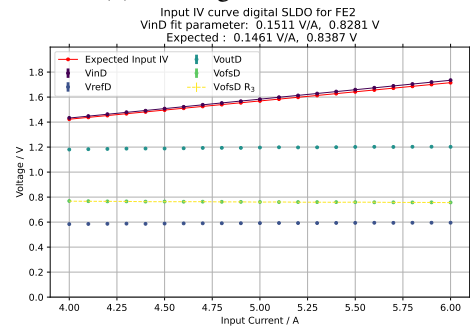
(f) FE2, digital Shunt-LDO.
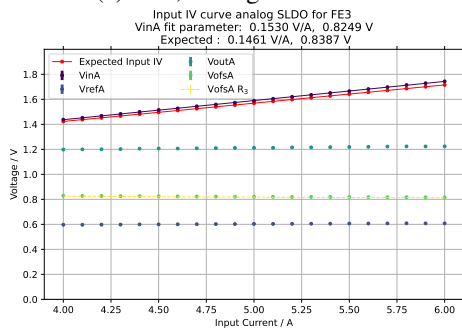
(g) FE3, analog Shunt-LDO.
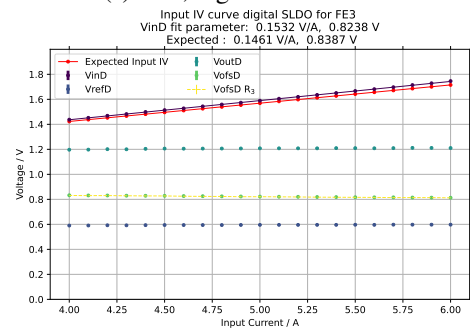
(h) FE3, digital Shunt-LDO.

Figure B.8: Shunt-LDO Input IV curve measurements of SPQ13.

(a) FE0, analog Shunt-LDO.

(b) FE0, digital Shunt-LDO.

(c) FE1, analog Shunt-LDO.

(d) FE1, digital Shunt-LDO.

(e) FE2, analog Shunt-LDO.

(f) FE2, digital Shunt-LDO.

(g) FE3, analog Shunt-LDO.

(h) FE3, digital Shunt-LDO.

Figure B.9: Shunt-LDO Input IV curve measurements of SPQ14.

(a) FE0, analog Shunt-LDO.
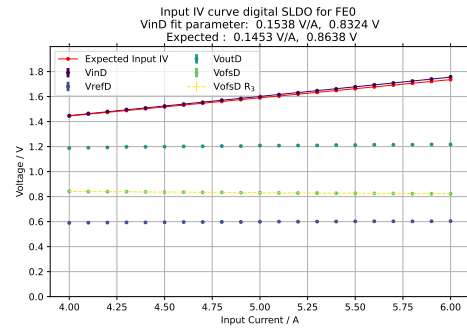
(b) FE0, digital Shunt-LDO.
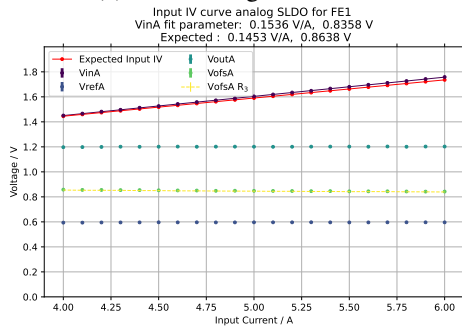
(c) FE1, analog Shunt-LDO.
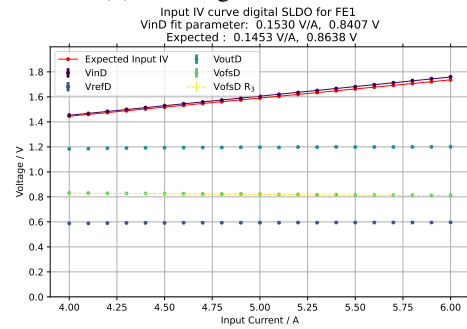
(d) FE1, digital Shunt-LDO.
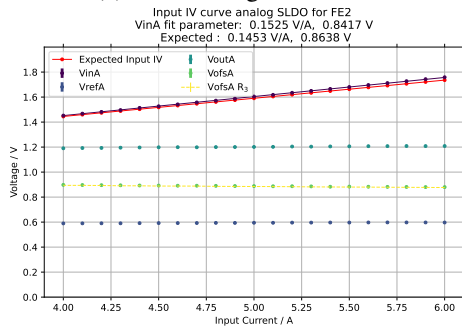
(e) FE2, analog Shunt-LDO.
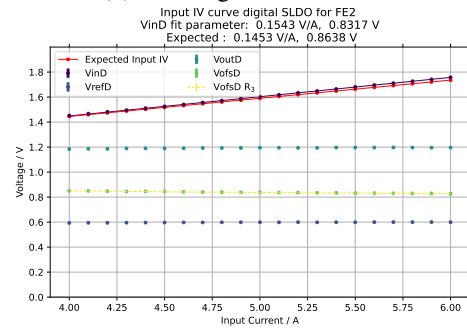
(f) FE2, digital Shunt-LDO.
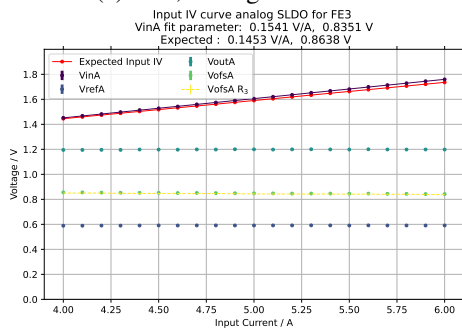
(g) FE3, analog Shunt-LDO.
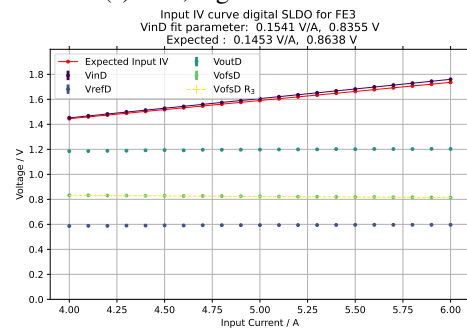
(h) FE3, digital Shunt-LDO.

Figure B.10: Shunt-LDO Input IV curve measurements of SPQ15.

(a) FE0, analog Shunt-LDO.

(b) FE0, digital Shunt-LDO.

(c) FE1, analog Shunt-LDO.

(d) FE1, digital Shunt-LDO.

(e) FE2, analog Shunt-LDO.

(f) FE2, digital Shunt-LDO.

(g) FE3, analog Shunt-LDO.

(h) FE3, digital Shunt-LDO.

Figure B.11: Shunt-LDO Input IV curve measurements of SPQ16. FE0 and FE1 of SPQ16 have a faulty voltage multiplexer, leading to faulty readings in Figure B.11(a) - Figure B.11(d).

(a) FE0, analog Shunt-LDO.
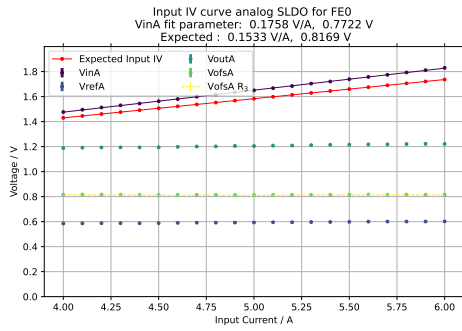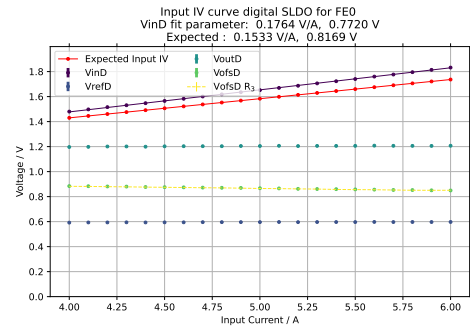
(b) FE0, digital Shunt-LDO.
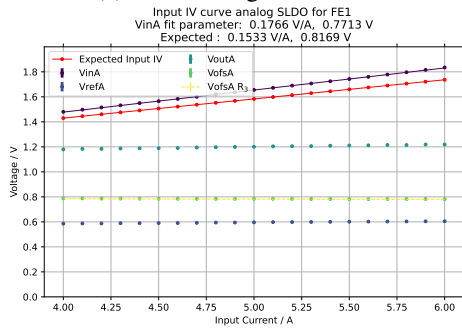
(c) FE1, analog Shunt-LDO.
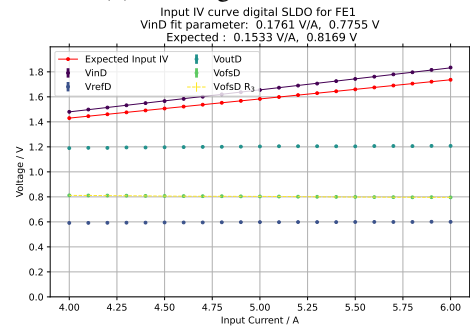
(d) FE1, digital Shunt-LDO.
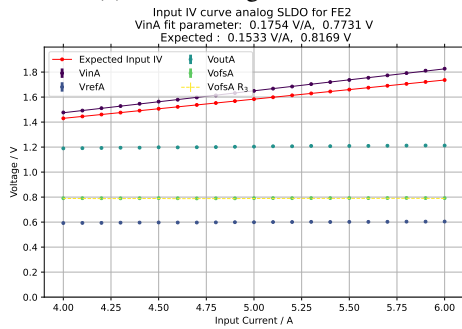
(e) FE2, analog Shunt-LDO.
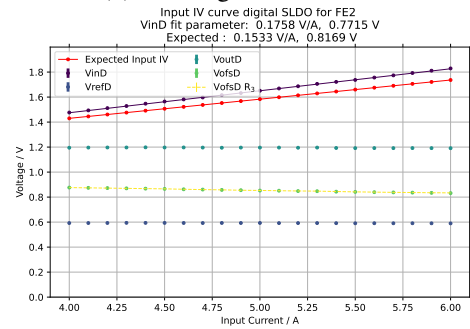
(f) FE2, digital Shunt-LDO.
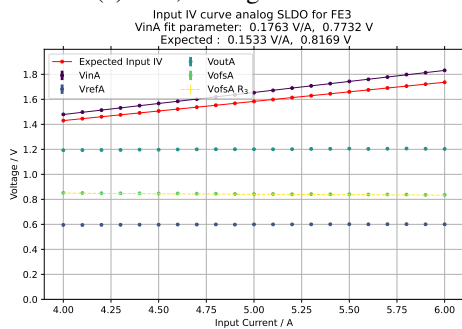
(g) FE3, analog Shunt-LDO.
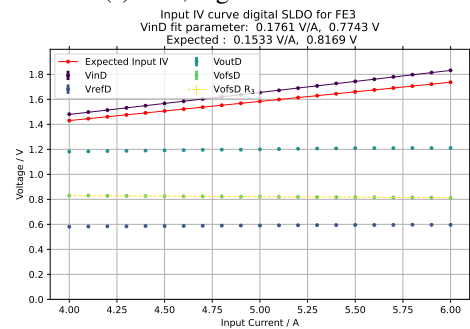
(h) FE3, digital Shunt-LDO.

Figure B.12: Shunt-LDO Input IV curve measurements of SPQ18.

In Figure B.13 and Figure B.14 the calculated current sum for each RD53A quad in the serial powering chain is shown. The total current is calculated using the R_{ext} sense pins on the module flex. Together with the k-factor estimate from wafer probing this yields the total module current. The uncertainty on I_{Mod} is driven by the uncertainty of the k-factor, while R_{ext} is given as a precision resistor with 0.1 % accuracy. For the following measurements an uncertainty on k of 5 % was chosen, which is a rather optimistic estimate. The plots include a reference corresponding to the supplied input current: ideally, the calculated module current on average corresponds to this reference. For all modules an increase in $I_{\text{Mod}} - I_{\text{in}}$ can be seen. This is due to k being a function of I_{in}, decreasing with the supplied current. This leads to an overestimate of I_{Mod} for higher I_{in}.

(a) SPQ11.

(b) SPQ12.
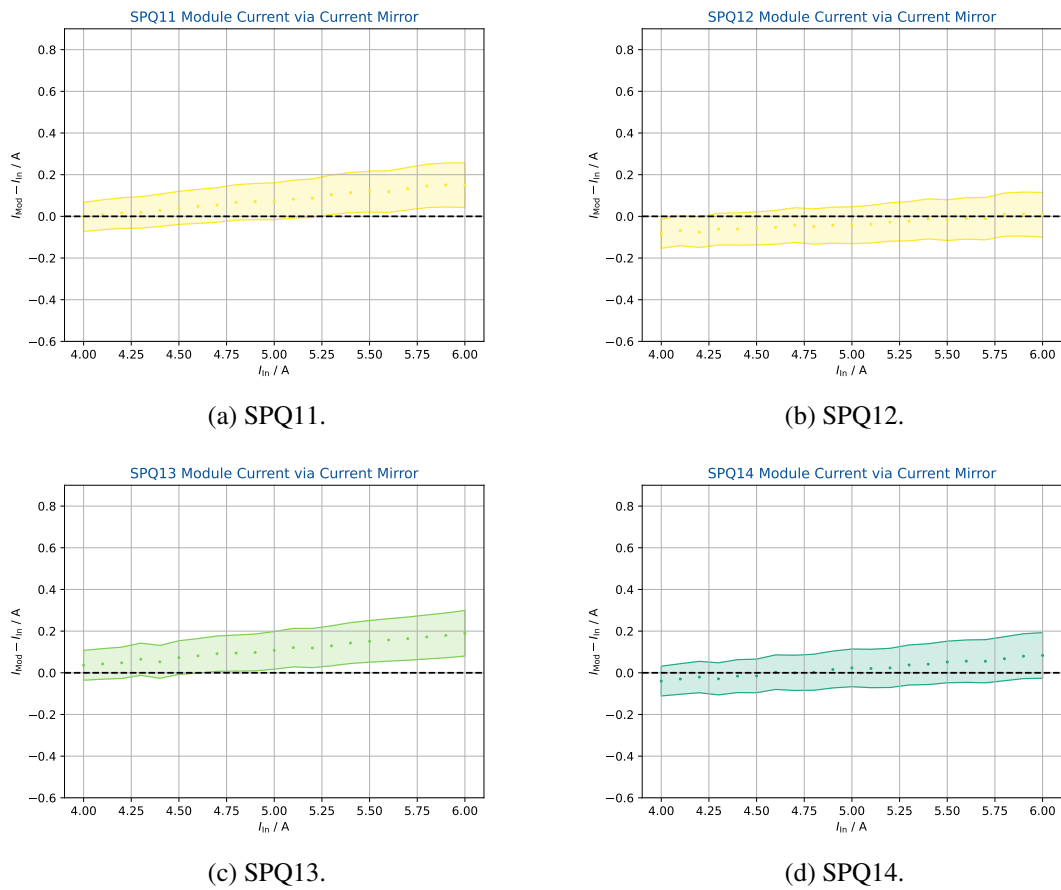
(c) SPQ13.

(d) SPQ14.

Figure B.13: Calculated on-module current for quad modules SPQ11-SPQ14 based on the k-factor. Uncertainties dominated by the k-factor determination.
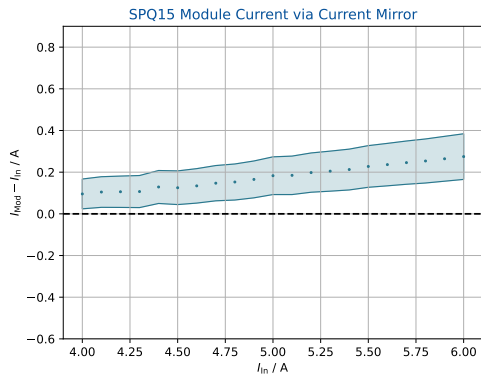
(a) SPQ15.
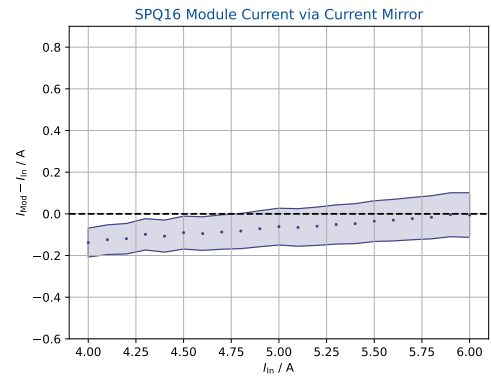
(b) SPQ16.
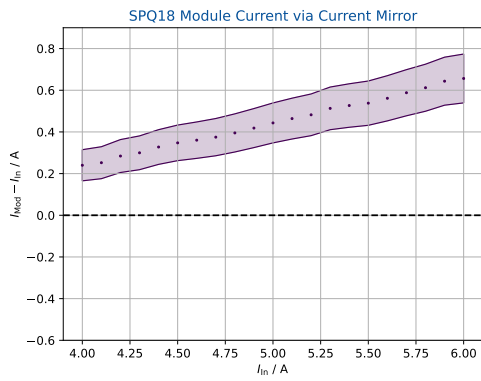
(c) SPQ18.

Figure B.14: Calculated on-module current for quad modules SPQ15-SPQ18 based on the k-factor. Uncertainties dominated by the k-factor determination.

Figure B.15 and Figure B.16 show the on-module current split between analog and digital Shunt-LDO. Marked is in addition the targeted current assuming equal V_{ofs} for all Shunt-LDO, which follows from the choice of R_{ext}. Again the uncertainties are driven by the estimate of the k-factor.

(a) SPQ11.

(b) SPQ12.

(c) SPQ13.

(d) SPQ14.

(e) SPQ15.

(f) SPQ16.

(g) SPQ18.
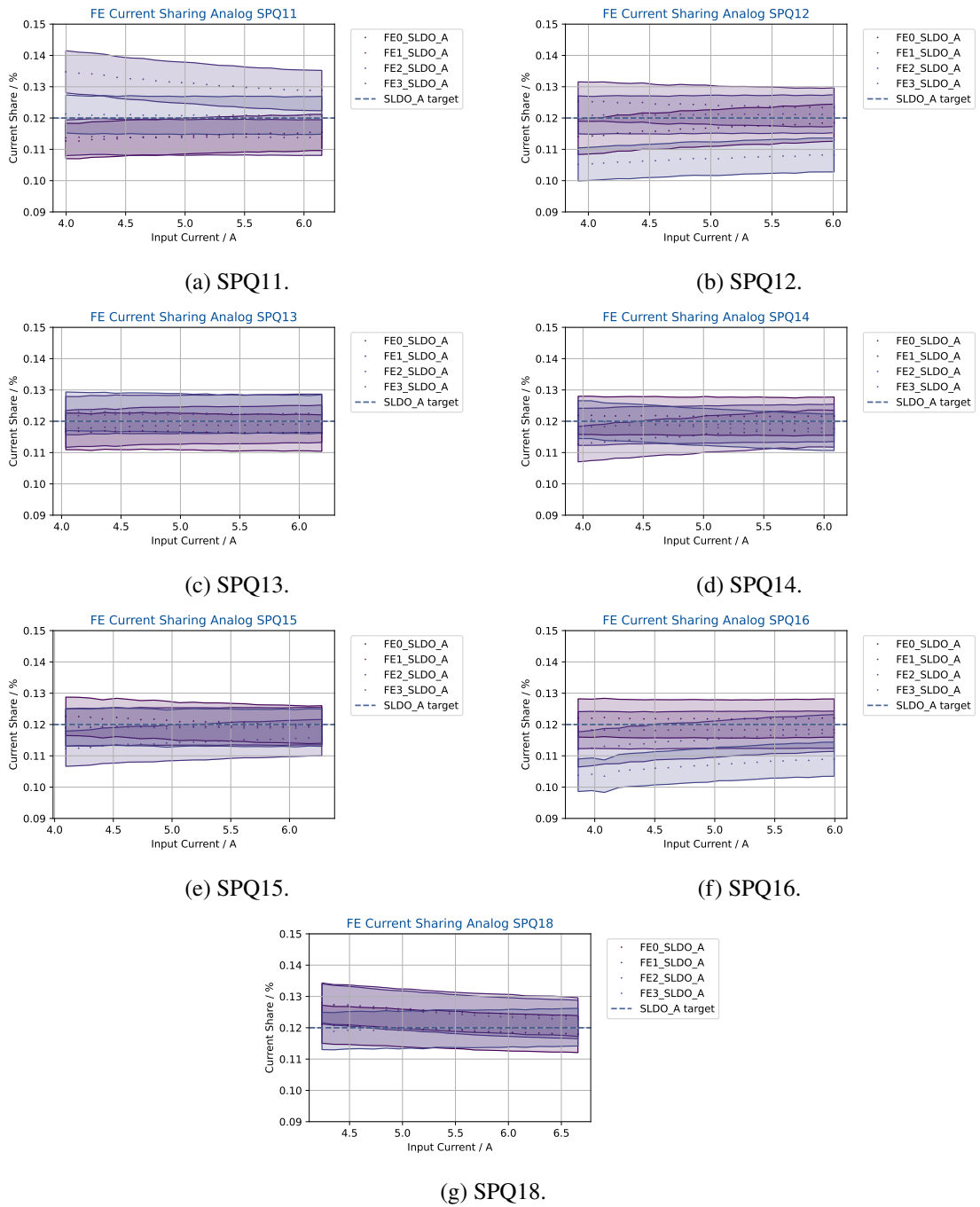
Figure B.15: Calculated on-module current sharing for each quad module based on the k-factor. Only contributions of the Shunt-LDO powering the analog domain shown. Uncertainties dominated by the k-factor determination.

(a) SPQ11.

(b) SPQ12.

(c) SPQ13.

(d) SPQ14.

(e) SPQ15.

(f) SPQ16.

(g) SPQ18.
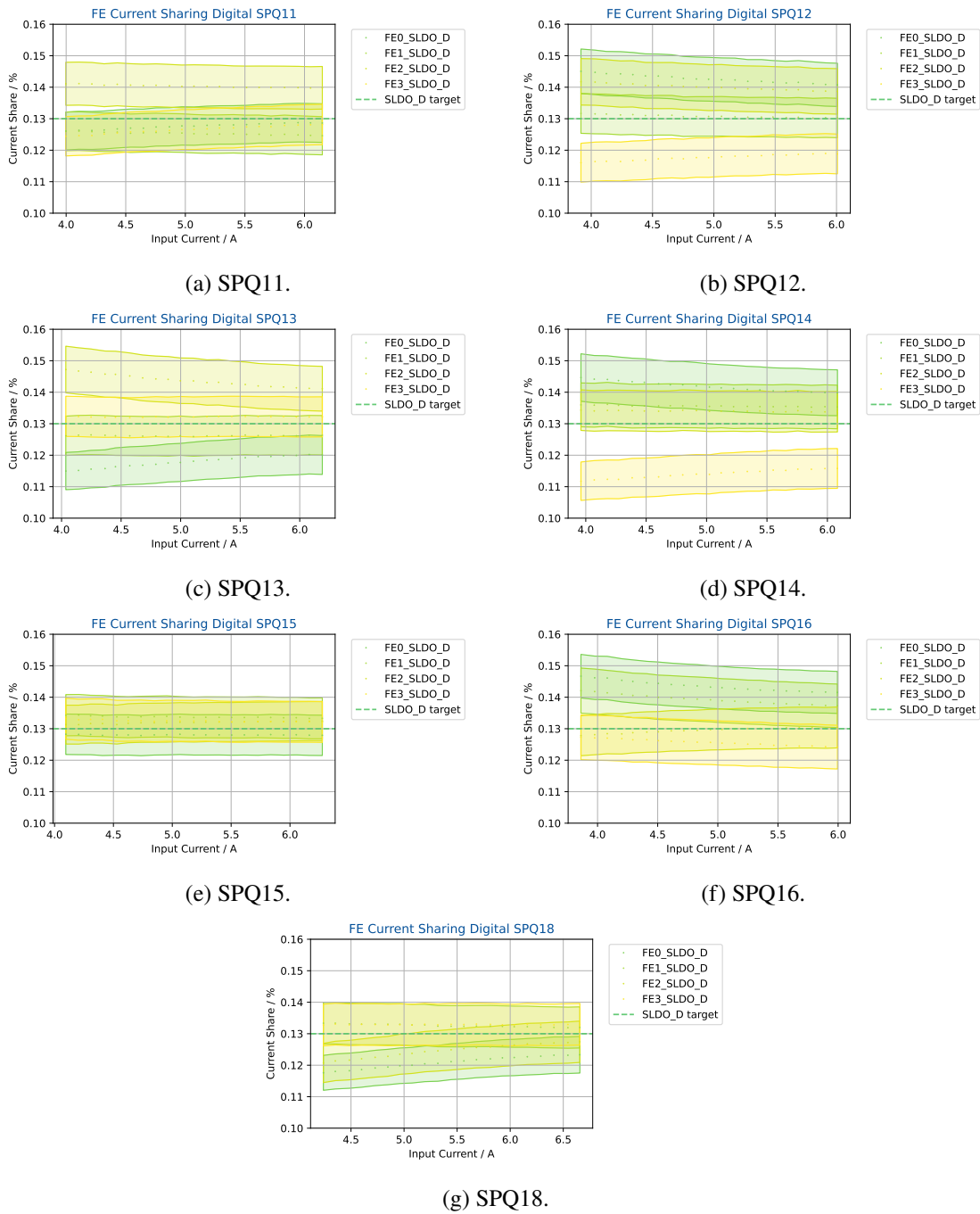
Figure B.16: Calculated on-module current for each quad module based on the k-factor. Only contributions of the Shunt-LDO powering the digital domain shown. Uncertainties dominated by the k-factor determination.

Based on the preceding measurements of the on-module current sum the relative current sharing on each module is calculated. As discussed an even current sharing is desired, as this decreases the required headroom of the Shunt-LDO, increasing the power efficiency of the module. The resulting relative current sharing is shown in Figure B.17 together with the target current share for digital and analog Shunt-LDO. SPQ10 is missing as it does not have a full set of operational Shunt-LDO. The corresponding plot for SPQ15 is found in Figure 5.32 in the main text body.

(a) SPQ11.

(b) SPQ12.

(c) SPQ13.

(d) SPQ14.

(e) SPQ16.

(f) SPQ18.
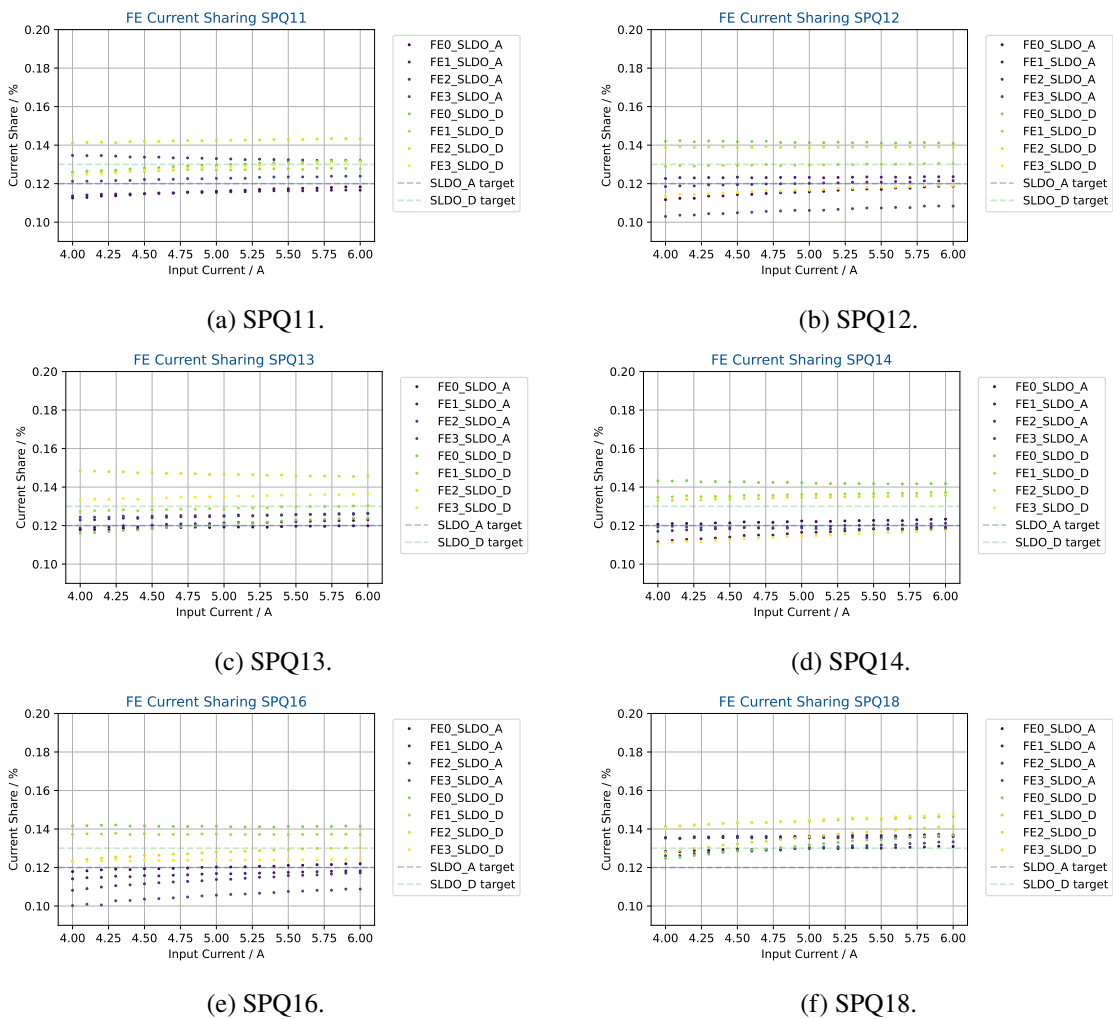
Figure B.17: Current sharing between different Shunt-LDO on different quad modules. Both analog and digital regulators draw similar shares of the total current close to the ideal 12 % and 13 % respectively. The x-axis denotes the current supplied to the module, while the y-axis denotes the relative current share with respect to the calculated module current as per Figure 5.31.

B.4 Characterisation of an RD53A Serial Powering Chain: Module Performance in a Serial Powering Chain.

2-D plots of the threshold- and ENC distribution measurements of all RD53A quad modules in the serial powering chain can be found in Figure B.18 (tuning to $2\,000\,e^-$) and Figure B.19 (tuning to $1\,000\,e^-$). Modules SPQ10 and SPQ13 as well as the SYNC AFE of all modules are not included in these plots.
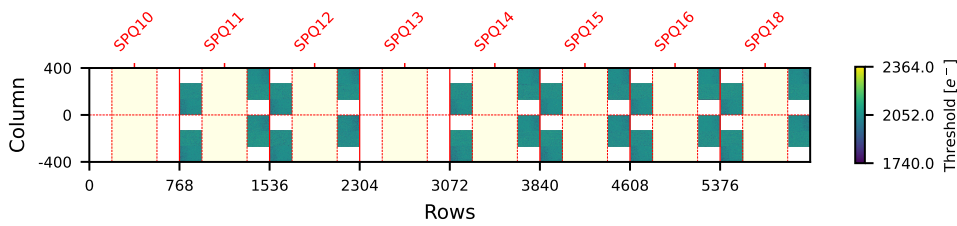
(a) Threshold distribution for all active pixel in the SP chain.
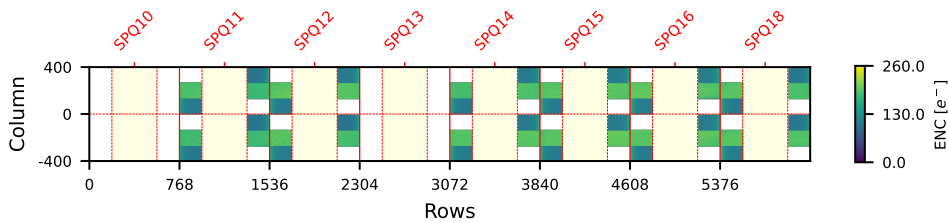
(b) ENC for all active pixel in the SP chain.

Figure B.18: Threshold and ENC distribution for all active ROC in SP chain after tuning to a target threshold of $2\,000\,e^-$. SPQ10 and SPQ13 are masked, SYNC AFE of all modules is masked. Sensor sized plotting is used, areas covered by the sensor but not connected to any ROC pixel are shaded in yellow.
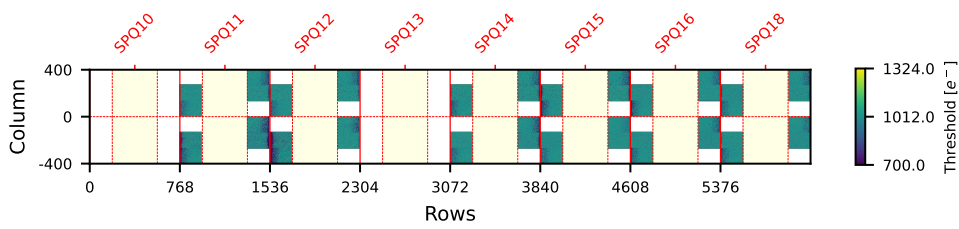
(a) Threshold distribution for all active pixel in the SP chain.
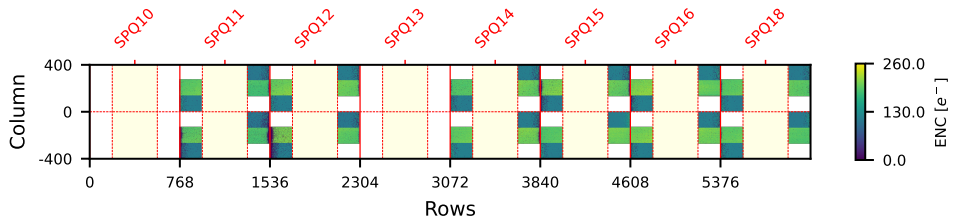
(b) ENC for all active pixel in the SP chain.

Figure B.19: Threshold and ENC distribution for all active ROC in SP chain after tuning to a target threshold of $1\,000\,e^-$. SPQ10 and SPQ13 are masked, SYNC AFE of all modules is masked. Sensor sized plotting is used, areas covered by the sensor but not connected to any ROC pixel are shaded in yellow.

B.5 High Voltage Off Mode Studies

Figure B.20 shows the transients measured on the HV line when switching off the supply current I_{in} for module SPQ18, the module with the lowest local ground in the powering chain. In Figure B.20(a) the switching of I_{in} is shown. Figure B.20(b) and Figure B.20(c) display the observable current transients on the HV line for different off-states of the HV power supply. The transients are measured as voltage drops over a 1 kΩ resistor in the HV path for each module. In Figure B.21 the same measurement is performed while switching on I_{in}.
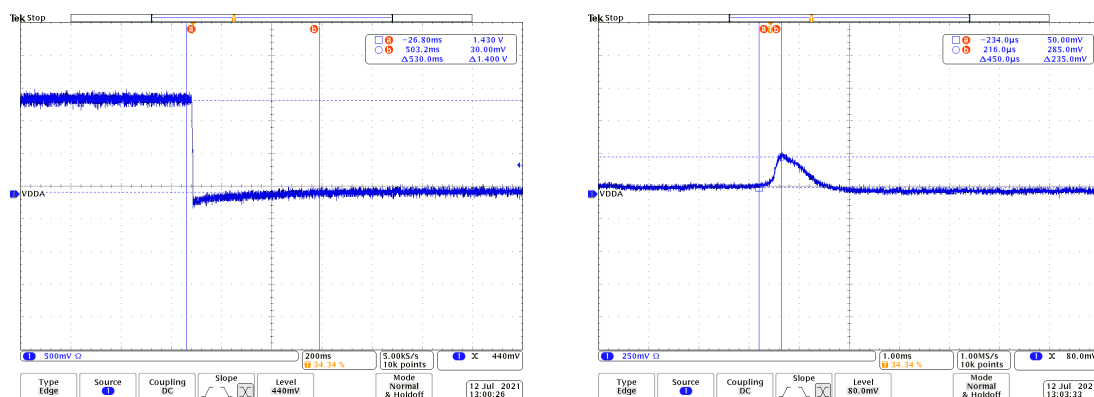
(a) Module LV during input current ramp.

(b) High-ohmic HV off mode.
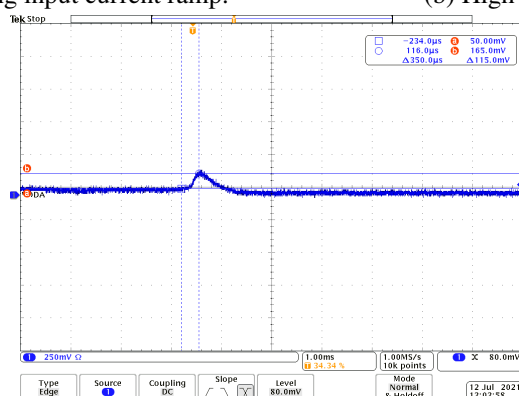
(c) Low-ohmic HV off mode.

Figure B.20: Transient on the HV line when LV is switched off. Measured on SPQ10. HV power supply is in an high-ohmic off state in Figure B.20(b) and in an low-ohmic off state in Figure B.20(c). 1 div corresponds to a current of 250 μA. Sign indicates current flow direction with negative currents flowing in reverse bias direction. As reference the module LV for the same current ramp is shown in Figure B.20(a).

(a) High-ohmic HV off mode.

(b) Low-ohmic HV off mode.
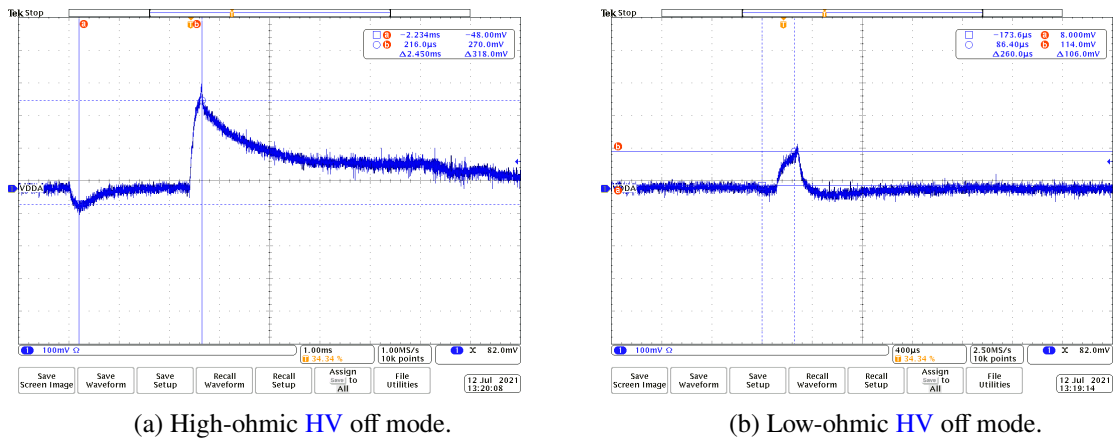
Figure B.21: Transient on the HV line when LV is switched on. Measured on SPQ18. HV power supply is in an high-ohmic off state in Figure B.21(a) and in an low-ohmic off state in Figure B.21(b). 1 div corresponds to a current of 250 μA. Sign indicates current flow direction with negative currents flowing in reverse bias direction.

Bibliography

[1] G. Aad et al., *Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC*, Physics Letters B **716** (2012) 1, ISSN: 0370-2693, URL: https://www.sciencedirect.com/science/article/pii/S037026931200857X (cit. on p. 1).

[2] S. Chatrchyan et al., *Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC*, Physics Letters B **716** (2012) 30, ISSN: 0370-2693, URL: https://www.sciencedirect.com/science/article/pii/S0370269312008581 (cit. on p. 1).

[3] ATLAS Outreach, *ATLAS Fact Sheet: To raise awareness of the ATLAS detector and collaboration on the LHC*, 2010, URL: https://cds.cern.ch/record/1457044 (cit. on p. 2).

[4] L. Evans and P. Bryant, *LHC Machine*, Journal of Instrumentation **3** (2008) S08001, URL: https://doi.org/10.1088/1748-0221/3/08/s08001 (cit. on p. 2).

[5] P. Mouche, *Overall view of the LHC. Vue d'ensemble du LHC*, (2014), URL: https://cds.cern.ch/record/1708847 (cit. on p. 3).

[6] G. Aad et al., *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST **3** (2008) S08003. 437 p, URL: https://cds.cern.ch/record/1129811 (cit. on pp. 3, 24, 27).

[7] S. Chatrchyan et al., *The CMS experiment at the CERN LHC. The Compact Muon Solenoid experiment*, JINST **3** (2008) S08004. 361 p, URL: https://cds.cern.ch/record/1129810 (cit. on p. 3).

[8] K. Aamodt et al., *The ALICE experiment at the CERN LHC. A Large Ion Collider Experiment*, JINST **3** (2008) S08002. 259 p, URL: https://cds.cern.ch/record/1129812 (cit. on p. 3).

[9]   A. A. Alves et al., *The LHCb Detector at the LHC*, JINST **3** (2008) S08005,
        URL: https://cds.cern.ch/record/1129809 (cit. on p. 3).

[10]   *Schedule for the LHC and the HL-LHC*,
        https://hilumilhc.web.cern.ch/content/hl-lhc-project,
        Accessed: 2022-02-12 (cit. on pp. 4, 5).

[11]   Particle Data Group, *Review of Particle Physics*,
        Progress of Theoretical and Experimental Physics **2020** (2020), ISSN: 2050-3911,
        URL: https://doi.org/10.1093/ptep/ptaa104 (cit. on pp. 4, 14–16).

[12]   J. Pequenao, *Computer generated image of the whole ATLAS detector*, 2008,
        URL: https://cds.cern.ch/record/1095924 (cit. on p. 6).

[13]   M. Capeans et al., *ATLAS Insertable B-Layer Technical Design Report*, tech. rep.,
        2010, URL: https://cds.cern.ch/record/1291633 (cit. on pp. 7, 9).

[14]   J. Pequenao, *Computer generated image of the ATLAS inner detector*, 2008,
        URL: https://cds.cern.ch/record/1095926 (cit. on p. 8).

[15]   ATLAS Collaboration, *ATLAS experiment public results*, https://twiki.cern.
        ch/twiki/bin/view/AtlasPublic/LuminosityPublicResultsRun2,
        URL: https://twiki.cern.ch/twiki/bin/view/AtlasPublic/
        LuminosityPublicResultsRun2 (cit. on p. 10).

[16]   ATLAS Collaboration, *The schematic depiction of the ITk Layout.* https:
        //atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/ITK-2020-002/,
        Accessed: 2022-02-12 (cit. on pp. 11, 29).

[17]   H. Kolanoski and N. Wermes, *Teilchendetektoren: Grundlagen und Anwendungen*,
        Springer, 2016, ISBN: 978-3-662-45349-0 (cit. on pp. 15–18, 20).

[18]   N. Wermes et al., *Pixel Detectors, From Fundamentals to Applications*,
        Springer-Verlag, 2006, ISBN: 3-540-28332-3 (cit. on pp. 16, 17).

[19]   W. Shockley, *Currents to Conductors Induced by a Moving Point Charge*,
        Journal of Applied Physics **9** (1938) 635,
        URL: https://doi.org/10.1063/1.1710367 (cit. on p. 17).

[20]   M. Daas, *Characterization and Quality Control of RD53A Readout Chips and
        Modules for the ATLAS ITk Pixel Detector*,
        PhD thesis: Rheinische Friedrich-Wilhelms-Universität Bonn, 2021,
        URL: https://hdl.handle.net/20.500.11811/9487
        (cit. on pp. 19, 65, 67, 70, 71, 73, 110, 112, 113, 115, 117, 124, 151, 155–157).

[21] N. Wermes, *Pixel detectors ... where do we stand?*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment **924** (2019) 44, 11th International Hiroshima Symposium on Development and Application of Semiconductor Tracking Detectors, ISSN: 0168-9002, URL: https://www.sciencedirect.com/science/article/pii/S016890021830826X (cit. on p. 21).

[22] D.-L. Pohl, *3D-Silicon and Passive CMOS Sensors for Pixel Detectors in High Radiation Environments*, PhD thesis: Rheinische Friedrich-Wilhelms-Universität Bonn, 2020, URL: https://hdl.handle.net/20.500.11811/8743 (cit. on p. 22).

[23] G. Aad et al., *ATLAS pixel detector electronics and sensors*, Journal of Instrumentation **3** (2008) P07007, URL: https://doi.org/10.1088/1748-0221/3/07/p07007 (cit. on pp. 21–23).

[24] L. Gonella, *Low mass hybrid pixel detectors for the high luminosity LHC upgrade*, Presented 23 Sep 2013, 2013, URL: https://cds.cern.ch/record/1633150 (cit. on pp. 22, 25, 32, 98).

[25] J. Weingarten, *System Test and Noise Performance Studies at The ATLAS Pixel Detector*, 2007, URL: http://cds.cern.ch/record/1099748 (cit. on pp. 23, 24).

[26] K. Lantzsch, Internal Communication (cit. on p. 23).

[27] D. B. Ta et al., *Serial powering: Proof of principle demonstration of a scheme for the operation of a large pixel detector at the LHC*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment **557** (2006) 445, ISSN: 0168-9002, URL: https://www.sciencedirect.com/science/article/pii/S016890020502214X (cit. on p. 27).

[28] T. Stockmanns et al., *Realisation of serial powering of ATLAS pixel modules*, (2004), URL: https://cds.cern.ch/record/915954 (cit. on p. 27).

[29] T. Stockmanns et al., *Serial powering of pixel modules*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment **511** (2003) 174, Proceedings of the 11th International Workshop on Vertex Detectors, ISSN: 0168-9002, URL: https://www.sciencedirect.com/science/article/pii/S016890020301787X (cit. on p. 27).

[30] ATLAS Collaboration,
      Technical Design Report for the ATLAS Inner Tracker Pixel Detector, tech. rep.,
      CERN, 2017, URL: http://cds.cern.ch/record/2285585 (cit. on pp. 29, 100).

[31] A. Luengo, Internal Communication (cit. on p. 30).

[32] *LVDS Owner's Manual*, https://www.ti.com/lit/ug/snla187/snla187.pdf?
      ts=1649747465509&ref_url=https%253A%252F%252Fwww.google.com%252F,
      Accessed: 2022-04-12 (cit. on pp. 32, 33).

[33] *Description of and Results from Testing a Serial Powering Chain of Irradiated RD53A
      Modules*, tech. rep., CERN, 2022, URL: https://cds.cern.ch/record/2808444
      (cit. on pp. 35, 105, 144, 145, 151).

[34] M. Karagounis et al.,
      "An integrated Shunt-LDO regulator for serial powered systems",
      2009 Proceedings of ESSCIRC, 2009 276 (cit. on p. 35).

[35] M. Karagounis, Internal Communication (cit. on pp. 36, 39, 75–77).

[36] J. (Chistiansen and M. (Garcia-Sciveres, *RD Collaboration Proposal: Development
      of pixel readout integrated circuits for extreme rate and radiation*, tech. rep.,
      CERN, 2013, URL: https://cds.cern.ch/record/1553467 (cit. on p. 41).

[37] Carney, R. et al.,
      "Results of FE65-P2 Pixel Readout Test Chip for High Luminosity LHC Upgrades",
      *Proceedings of 38th International Conference on High Energy Physics —
      PoS(ICHEP2016)*, vol. 282, 2017 272 (cit. on p. 41).

[38] Pacher, L. et al., "Results from CHIPIX-FE0, a Small-Scale Prototype of a New
      Generation Pixel Readout ASIC in 65 nm CMOS for HL-LHC", *Proceedings of
      Topical Workshop on Electronics for Particle Physics — PoS(TWEPP-17)*, vol. 313,
      2018 024 (cit. on p. 41).

[39] M. Garcia-Sciveres, *RD53A Integrated Circuit Specifications*, tech. rep., CERN, 2015,
      URL: https://cds.cern.ch/record/2113263
      (cit. on pp. 41, 65, 66, 68, 132, 155).

[40] ATLAS Collaboration, *Internal communication: Analog FE Decision (Access
      restricted to ATLAS collaboration)*, https://indico.cern.ch/event/804139/,
      URL: https://indico.cern.ch/event/804139/ (cit. on p. 42).

[41] F. Arteche Gonzalez et al., *Extension of RD53*, tech. rep., CERN, 2018,
      URL: https://cds.cern.ch/record/2637453 (cit. on p. 42).

[42] M. Garcia-Sciveres, F. Loddo and J. Christiansen, *RD53B Manual*, tech. rep., CERN, 2019, URL: https://cds.cern.ch/record/2665301 (cit. on pp. 42, 76, 78, 79).

[43] J. Kampkötter, Internal Communication (cit. on p. 43).

[44] M. Frohne, *characterization of the ShuntLDO-regulator in 65 nm process for the new ATLAS ITk pixel detector readout chip*, 2017 (cit. on pp. 49, 50, 56, 58, 59).

[45] S. Orfanelli, *Serial Powering Optimization for CMS and ATLAS Pixel Detectors within RD53 Collaboration for HL-LHC: System Level Simulations and Testing*, **313** (2018) 055 (cit. on p. 56).

[46] M. Standke, *Characterization of the Joined ATLAS and CMS RD53A Pixel Chip*, Presented 28 Feb 2019, 2019, URL: https://cds.cern.ch/record/2717863 (cit. on pp. 65, 115).

[47] P. Rymaszewski, *Design and characterization of pixel IC electronics and sensors for new pixel detector generations*, PhD thesis: Rheinische Friedrich-Wilhelms-Universität Bonn, 2022 (cit. on p. 73).

[48] M. Schüßler, *characterisation of a RD53b ShuntLDO Prototype for the Atlas ITk Pixel Detector Readout Chip*, 2019 (cit. on pp. 75, 82–85, 89, 159–168).

[49] M. Vogt, *Development of the Readout System BDAQ53 and Verification and Characterization of the Hybrid Pixel Readout Chip RD53A (In preparation)*, PhD thesis: Rheinische Friedrich-Wilhelms-Universität Bonn, 2022 (cit. on p. 88).

[50] C. Perry, *Towards Shunt-LDO characterisation in ITkPixV1*, 2021 (cit. on pp. 96, 113, 124, 130).

[51] V. Filimonov, *Development of a serial powering scheme and a versatile characterization system for the ATLAS pixel detector upgrade*, PhD thesis: Rheinische Friedrich-Wilhelms-Universität Bonn, 2017, URL: https://hdl.handle.net/20.500.11811/7265 (cit. on p. 98).

[52] D. A. Feito, Internal Communication (cit. on pp. 99, 109).

[53] N. Lehmann, *Control and Monitoring for a serially powered pixel demonstrator for the ATLAS Phase II upgrade*, tech. rep., CERN, 2018, URL: https://cds.cern.ch/record/2644706 (cit. on pp. 100, 101).

[54] N. Lehmann, *Development of a Detector Control System Chip*, Presented 02 Sep 2019, 2019, URL: https://cds.cern.ch/record/2701808 (cit. on p. 100).

[55] S. Kuehn, *Results of larger structures prototyping for the Phase-II upgrade of the pixel detector of the ATLAS experiment*, tech. rep., CERN, 2019, URL: https://cds.cern.ch/record/2663382 (cit. on pp. 101, 104).

[56] M. Hamer, *Phase-II upgrade of the ATLAS Pixel Detector*, tech. rep., CERN, 2019,
URL: https://cds.cern.ch/record/2665116 (cit. on p. 101).

[57] E. Buschmann, *ATLAS Phase-II-Upgrade Pixel Demonstrator Read-out*,
PoS **TWEPP2018** (2019) 046 (cit. on pp. 101, 104).

[58] S. Kühn, Internal Communication (cit. on p. 101).

[59] *SIMATIC WinCC Open Architecture*, http://www.etm.at/,
URL: http://www.etm.at (cit. on p. 101).

[60] J. Janssen, D.-L., Pohl, et al., *pyBAR - Bonn ATLAS Readout in Python, 2018*,
https://github.com/SiLab-Bonn/pyBAR,
URL: https://github.com/SiLab-Bonn/pyBAR (cit. on p. 101).

[61] *ITk Pixel SR1 System Test Module Qualification*, https://twiki.cern.ch/twiki/
bin/view/Atlas/ITkPixelSR1SystemSetupModuleQualification,
Accessed: 2022-04-25 (cit. on p. 102).

[62] L. Meng and ATLAS Collaboration, *ATLAS ITk Pixel Detector Overview*, tech. rep.,
CERN, 2021, URL: https://cds.cern.ch/record/2767329 (cit. on p. 106).

[63] S. Zambito, *ATLAS Inner Tracker Pixel Outer Barrel Demonstrator*, (2021),
URL: https://cds.cern.ch/record/2752953 (cit. on pp. 106–108).

[64] F. Hinterkeuser,
Development and evaluation of prototypes for the ATLAS ITk pixel detector, tech. rep.,
CERN, 2020, URL: https://cds.cern.ch/record/2743490 (cit. on p. 106).

[65] M. Daas et al., *BDAQ53, a versatile pixel detector readout and test system for the
ATLAS and CMS HL-LHC upgrades*,
Nuclear Instruments and Methods in Physics Research Section A: Accelerators,
Spectrometers, Detectors and Associated Equipment **986** (2021) 164721,
ISSN: 0168-9002, URL: https:
//www.sciencedirect.com/science/article/pii/S0168900220311189
(cit. on p. 113).

[66] L. Schall, *Tests and Characterization of RD53A Modules for the High-Luminosity
Upgrade of the ATLAS Pixel Detector at the LHC*, 2021 (cit. on pp. 117, 148).

[67] K. Nakamura, Internal Communication (cit. on p. 119).

[68] *Analog Devices ADN4604, 4.25 Gb s, 16×16, Digital Crosspoint Switch*,
Accessed: 2022-03-08, URL: https://www.analog.com/media/en/technical-
documentation/data-sheets/ADN4604.pdf (cit. on p. 121).

[69]   *Analog Devices ADN4605, 4.25 Gb s,* 40×40*, Digital Crosspoint Switch*,
        Accessed: 2022-03-08, URL: https://www.analog.com/media/en/technical-
        documentation/data-sheets/ADN4605.pdf (cit. on p. 121).

[70]   *ADS111x Ultra-Small, Low-Power, I2C-Compatible, 860-SPS, 16-Bit ADCs With
        Internal Reference, Oscillator, and Programmable Comparator*,
        Accessed: 2022-03-08, URL:
        https://www.ti.com/lit/ds/symlink/ads1114.pdf?ts=1649121926946&
        ref_url=https%5C%253A%5C%252F%5C%252Fwww.google.com%5C%252F
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