Hybrid Pixel Readout Chip Verification, Characterization and Wafer Level Testing for the ATLAS-ITK Upgrade at the HL-LHC

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CHAPTER 1

Introduction

Throughout history, fundamental questions about the constituents of matter and the universe have preoccupied mankind for a long time. It started with the cosmogonic theory of the four classical elements by Empedocles in 450 BC [1], among others, followed by the introduction of the atom by John Dalton in 1808 [2] and the discovery of subatomic constituents as described by Joseph Thomson in his plum pudding model in 1903 [3]. In modern times, particle physics has evolved. Among others on the basis of the findings of Ernest Rutherford, who discovered the atomic nucleus and the neutron [4] in 1911 and the gauge theory introduced by Yang and Mills in 1954 [5] leading to the formation of the standard model first mentioned by Pais and Treiman in 1975 [6]. The standard model summarizes sub atomic constituents of matter in elementary- and interacting- particles [7]. Research, investigating the standard model, relies on particle accelerators to probe the constituents of matter at ever smaller scales. The largest particle accelerator built to date is the Large Hadron Collider (LHC) in Geneva, Switzerland. According to Equation (1.1) [8] some of the kinetic energy E of the colliding particles is transformed into mass m in the form of particles, proportional to the inverse squared speed of light c^2.

$$E = m \cdot c^2 \tag{1.1}$$

Particle collisions help refine our understanding of the fundamental forces and the makeup of matter. Some particle reactions are extremely rare and require the aggregation of many collisions. The most famous discovery of the LHC, the Higgs particle [9], for example required on average one billion proton collisions to produce one Higgs particle. Therefore the two drivers for more accurate answers to the question: "What is matter made of?" are:

1. **Higher Energy:** To probe increasingly smaller scales and produce increasingly massive sub atomic constituents

2. **Higher Rates:** To probe rare events

For all of the produced particles, their properties, such as mass, charge and momentum need to be measured. This necessitates large, general-purpose detectors, such as the ATLAS [9] and CMS [10] detectors, which employ a variety of detection systems to measure the aforementioned properties for each generated particle. Those detectors operate at the forefront of engineering, pushing existing technologies to their limits. Especially with increasing rate, as for seen after the HL-LHC upgrade, introduced in Section 1.2, the radioactive exposure of the detectors increases. This

leads to technological challenges involving single event upsets [11] and silicon bulk damage [12] in modern integrated circuits. The content presented in this thesis focuses on the development of novel, radiation-tolerant ATLAS detector, introduced in Section 1.3, components, the hybrid pixel detector readout chip, introduced in Section 2.2. A short description of the physics involved in particle detector building and hybrid pixel detectors can be found in Chapter 2. Followed by a detailed description of the tested readout chip in Chapter 3. Chapter 4 and Chapter 5 focus on the introduction of the readout and simulation framework as developed in the scope of this thesis. Chapter 6 summarizes the general performance of the tested readout chip, while Chapter 7 summarizes statistical test results acquired during bulk testing of the readout chip, as well as the process and software, which was developed in the scope of this thesis, including the roll-out to multiple global collaborating sites. This Chapter will give a quick introduction into the LHC and its detectors.

1.1 The Large Hadron Collider (LHC)

The Large Hadron Collider (LHC) is the largest particle accelerator to date. Since 2008 [13] the LHC has used the tunnel dug for LEP with a circumference of 27 km at the border between France and Switzerland close to Geneva [14]. Figure 1.1 shows the underground ring with its four main experiments: ATLAS [15], CMS [10], ALICE [16] and LHCb [17], as well as its pre-accelerator, the Super Proton Synchrotron (SPS) [18].

The LHC's novel superconducting magnets allowed the accelerator to keep not only electrons and positrons, as previously used by LEP, but also protons on its ring trajectory. Protons, which are 1836 times heavier than electrons, gain therefore significantly more energy, due to less emitted synchrotron radiation. This increased the LHC's acceleration energy to 13.6 TeV today [20]. In 2012 the LHC contributed to the discovery of the Higgs Boson [9], completing Peter Higgs, François Englert and Robert Brouts theory [21][22], resulting in the Nobel Prize for François Englert and Peter Higgs in 2013 [23], fulfilling one of the LHC's primary research goals. In 2015 an upgrade of the LHC to the High Luminosity LHC (HL-LHC) was approved. High luminosity refers to an increase of the particle collisions per time, which is as mentioned before, one of the main drivers for more accurate particle physics measurements. The luminosity is expected to increase 5-7.5 compared to its original value from 2014, to a peak luminosity of 10^{31} cm^{-2}s^{-1} [24] [25]. The instantaneous luminosity ($\mathcal{L}$) is defined as shown in Equation (1.2) [26] and proportional to N_p^2, with N_P referring to the number of particles per bunch, n_b the number of bunches, f the bunch-revolution frequency, which is 40 MHz at the LHC and HL-LHC, and F a form factor describing the shape of the beam and incident angle at the interaction point. A bunch is defined as a packet of particles inside the accelerator, with many bunches forming the beam. To identify individual bunches, each bunch has an assigned bunch crossing ID, to differentiate consecutive interactions.

$$\mathcal{L} \propto \frac{N_p^2 n_b f}{4\pi F} \tag{1.2}$$

An accelerator's event rate $\frac{dN(\sigma)}{dt}$ can be determined by its luminosity and total proton-proton scattering cross section σ as shown in Equation (1.3) [26].

$$\frac{dN}{dt} = \mathcal{L} \cdot \sigma \tag{1.3}$$

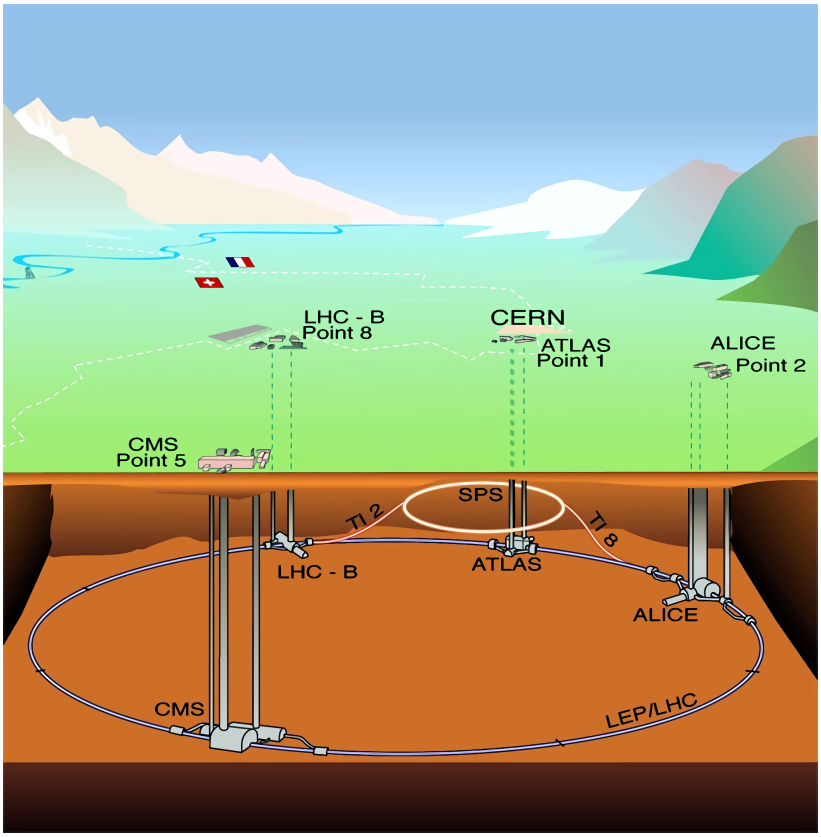


Figure 1.1: A schematic view of the Large Hadron Collider at the French-Swiss border in Geneva, with its four main experiments: ATLAS, CMS, ALICE and LHCb[19].

From Equation (1.2) and (1.3) it is easy to see that the event rate can be increased by:

1. Increasing the interaction frequency f
2. Increasing the number of protons per bunch N_p
3. Decreasing the form factor F

For the HL-LHC it was decided to optimize all three factors, by increasing the filling factor, which defines how many 40 MHz bunches are actually filled, with how many particles. In addition to a change of the beam form-factor F as described in Reference [27]. One subsequent benefit of this is that the recovery time of the readout electronics will remain unchanged at 40 MHz . The optimized filling- and form-factor F lead to an increased interaction rate as described in Equation (1.3), allowing the experiment to detect rare events significantly more often, offering a more precise measurement of the standard model and, if they exist, increasing the potential for detecting e.g. supersymmetry or Dark Matter [28].

1.2 The High Luminosity Large Hadron Collider (HL-LHC)

As discussed in Section 1.1 an intuitive way to increase the collisions per time is to optimize the beam filling- and form-factor. Therefore the new HL-LHC project was born, the project timeline is shown in Figure 1.2. The HL-LHC project plan with LS 1-3 indicating long shutdowns for construction and EYETS indicating extended year-end technical stops. Experimental runs are interspersed with shut downs for system upgrades. At the time of writing, the LHC is in Run 3, with the next long shutdown, LS3, being planned for 2026. During this period the LHC will be upgraded to the HL-LHC, with subsequent experimental Runs 4 and 5 taking advantage of the improvements. Further information about the upgrade can be found in Section 1.4.

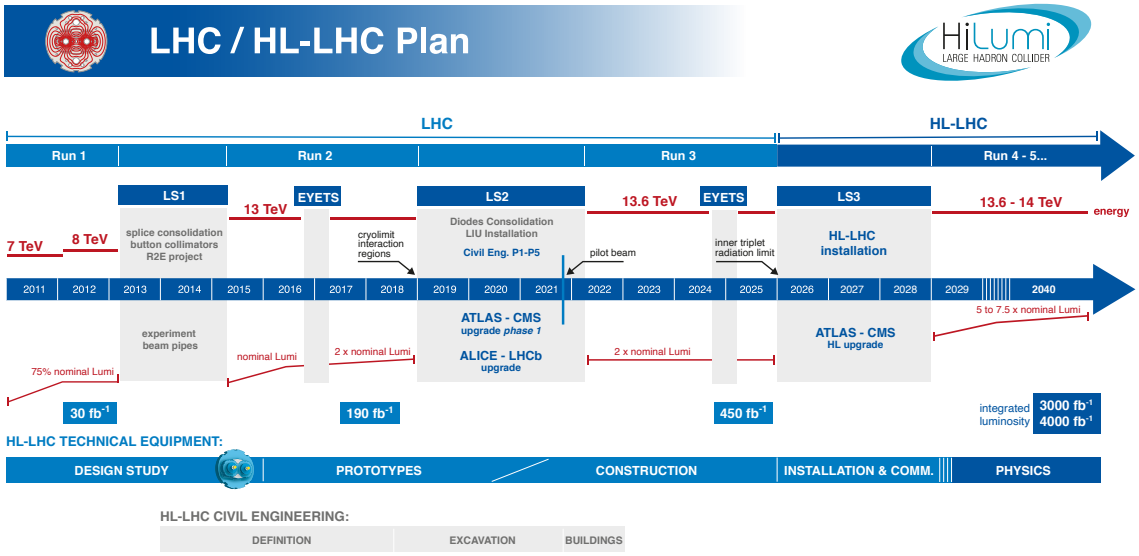


Figure 1.2: The HL-LHC project timeline. The ATLAS and CMS upgrades will take place in Long Shutdown 3 (LS3) [25]

1.3 A Toroidal LHC Apparatus (ATLAS)

ATLAS, short for "A Toroidal LHC Apparatus" [15], is the largest general-purpose particle detector at the LHC. General-purpose is a reference to its suitability for a broad spectrum of particle physics measurements. Many of its scientific goals are shared with the Compact Muon Solenoid (CMS) detector [10], despite its different detector design. Each detection layer is sensitive to different particle types and particle properties. In the following each detection layers technical buildup and sensitivity is explained. Figure 1.3 shows a full view of ATLAS with its 25 m diameter and 44 m [29] length it is CERNs largest detector. The particles collide in the center of the detector, where the Pixel detector is referenced in Figure 1.3. The newly produced particles then propagate out from the center of the detector. A few, long lived particles also reach the outermost detection layer.

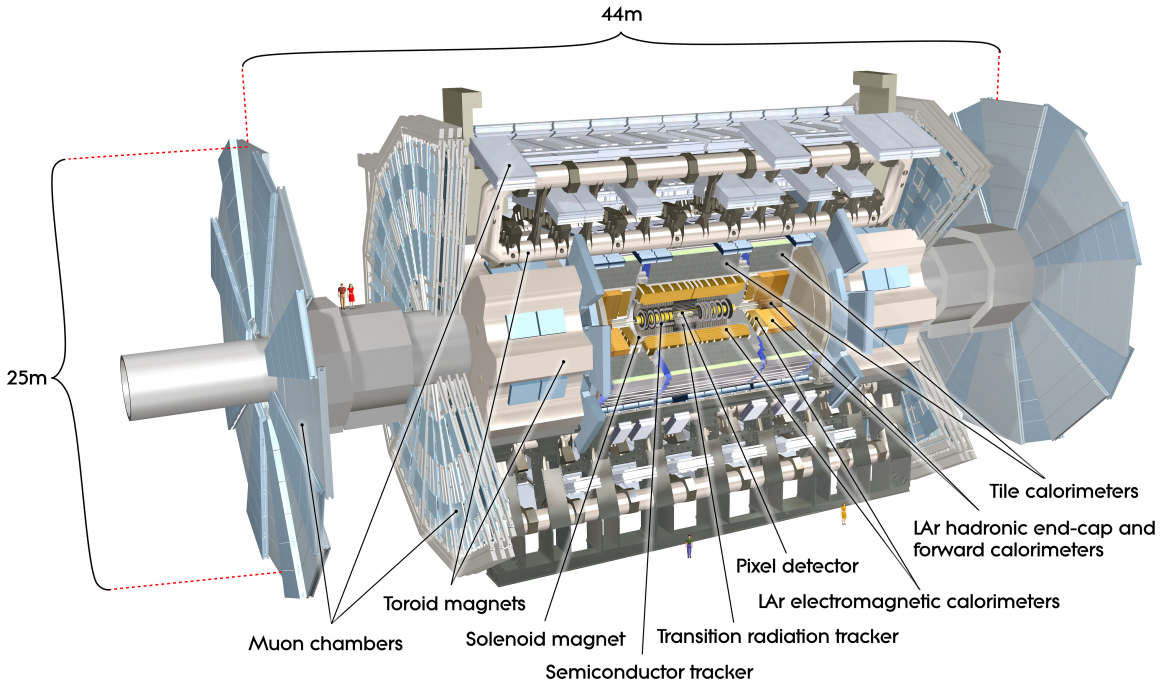


Figure 1.3: A computer-generated image of the ATLAS detector [30]

The different detection systems are elaborated in the following Sections.

1.3.1 Muon Spectrometer

The outermost detection system is the Muon Spectrometer [31]. Muons are leptons, just like electrons, but 207 times more massive. Their large mass, compared to the electron, leads to low energy deposition in the detector and allows them to traverse the whole ATLAS detector mainly undisturbed. Therefore the outermost detection layer is designed to detect muons and measure their momentum, energy and path with increased precision. The muon chambers consist of a toroidal magnetic field, created by eight air-core barrel magnets, spanning 26 m by 20 m diameter [31]. This magnetic field bends the traversing muon's tracks according to the Lorentz force, with the curvature giving information about the muon momentum. Such tracks are reconstructed using Monitored Drift Tubes (MDTs), Cathode Strip Chambers (CSCs) and Resistive Plate Chambers (RPCs) [31].

1.3.2 Calorimeter Systems

The Calorimeter Systems are surrounded by the Muon Chambers. Calorimeter Systems are designed to measure a particle's energy. This is achieved by using thick material, which offers a high interaction probability to, ideally, stop a particle inside the calorimeter. Since most particles interact electromagnetically and/or hadronically, ATLAS employs two different calorimeters. The outer calorimeter is the hadronic calorimeter, stopping most hadronically interacting particles in a hadronic shower, using

predominantly stainless steel as absorber-material and scintillating tiles as active material [32]. The inner, electromagnetic calorimeter, stops electro-magnetically interacting particles such as electrons, photons, etc. in an electromagnetic shower using lead as the passive component and liquid argon as the active detection medium [33]. Both calorimeters are designed as sampling calorimeters, with an active material, which generates a signal for detection. In both cases the absorber and active material are arranged in an alternating, accordion-like structure. Hereby the showers are generated in the absorber material, while each shower's energy and position is measured in the corresponding active medium.

1.3.3 Inner Detector

The Inner Detector (ID) [34] is surrounded by the calorimeters. The Inner Detector, as currently employed in ATLAS, utilizes three different tracking technologies. The four innermost layers use hybrid pixel detectors, which will be explained in Section 2. The next four layers detect traversing particles using strip detectors, which offer slightly less resolution and readout speeds than hybrid pixel detectors, but at significantly reduced cost per square meter. The strip detector of the Inner Detector features 6 million channels. The largest part of the Inner Detector uses a transition radiation detector to cover a large volume of 12 m^3 with a resolution of 0.17 mm and 350 thousand channels [35].

1.4 ATLAS ITk Upgrade

The ATLAS ITk (Inner Tracker) upgrade is a replacement of the Inner Detector for the HL-LHC. The replacement will take place during Long Shutdown 3 as shown in Figure 1.2. The upgrade is necessary due to the increased luminosity of the HL-LHC, as stated in Section 1.2, which leads to a significantly higher vertex density per collision. A vertex is the point, where at least two protons collide. Due to the optimization of the filling- and form-factor F the number of vertices per bunch crossing increase, which leads to a higher track density in ATLAS at the HL-LHC. The effect, of multiple vertex generation in the same bunch is called pile-up. Figure 1.4 shows the increased track density before and after the HL-LHC upgrade inside ATLAS. It is visible, that the track density at the center of ATLAS, where ITk will be located, increases significantly more, than further out. This is related to the inverse square law, which states that the radiation intensity, radially emitted by a point like source, is inversely proportional to the square of the distance.

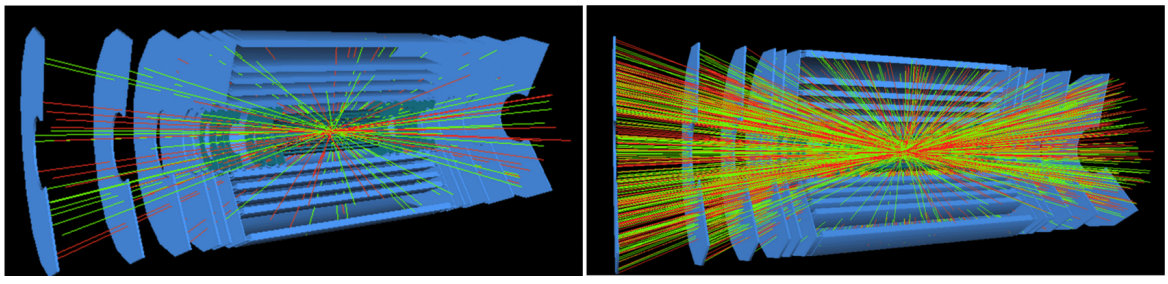
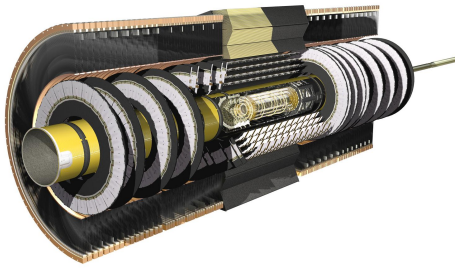
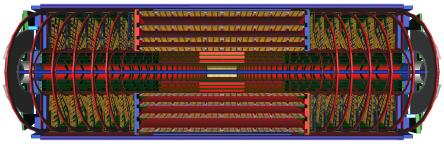


Figure 1.4: Simulations of different luminosities, at the LHC with current Inner Detector (left) and HL-LHC and with new ITk (right) [36]

A higher track density presents multiple challenges for a new detector:

- Higher spatial resolution to differentiate interaction vertices close to each other
- Higher radiation tolerance, necessitated by more traversing particles
- Higher readout speed to process the increased track density

Inner Detector (ID)	Inner Tracker (ITk)
 Figure 1.5: An ID CAD cross-section[37]	 Figure 1.6: An ITk CAD cross-section[38]

Pixel Detector	
4 barrel layers with 1736 modules [35]	5 barrel layers with 5000 modules [39]
3 disks in each end-cap with 288 sensor modules [35]	11 disks in each end-cap with 4164 modules [39]
Barrel radius 3.3 cm to 14 cm [35]	Barrel radius 3.3 cm to 27.4 cm [39]
1.9 m^2 of active area [35]	12.83 m^2 of active area [39]
92 million pixels [35]	5.1 billion pixels [39]

Strip Detectors	
4 barrel layers [34]	4 barrel layers [40]
9 wheels in each end-cap [34]	6 disks in each end-cap [40]
Barrel radius 30 cm to 52 cm[34]	Barrel radius 40 cm to 100 cm [40]
60 m^2 of active area [35]	165 m^2 of active area [41]
6 million readout channel [35]	60 million readout channel [41]

Transition Radiation Detector	
Barrel radius 55 cm to 107 cm [34]	Covered by Pixel and Strip Detectors
12 m^3 active volume [35]	
350000 read-out channel [35]	

Table 1.1: Comparison of Inner detector and ITk.

These challenges can only be met with a redesign of the readout chip of the current inner pixel detector. The current chips employed in the ATLAS inner detector are called FEI3 [42] and FEI4 [43].

The new readout chip, ITkPix, and its purpose in ITk is described in Chapter 3 [44].

Table 1.1 compares the current ATLAS inner detector with the new ITk detector, including the new ITk pixel readout chip. Figure 1.5 shows a computer generated image of the inner detector, with the pixel detector in the center, followed by the silicon strip detector, and the transition radiation detector. Figure 1.6 shows the layer structure of ITk. The first five layers in the center are pixel detector layers, while the next four outer layers in red, are strip detector layers. This will result in a factor fifty increase of readout channels in the pixel detector, with the amount of strip readout channels increasing tenfold. A transistion radiation detector is no longer employed in ITk. To ensure the qualification of all necessary components and processes needed to build ITk, the building of the ATLAS ITk pixel detector can be subdivided into two phases:

1. ITk pre-production (until 2023): ITk pre-production is the phase before production, where all components and processes will be qualified and defined, to scale up for production.

2. ITk production (until Run4): ITk production is the actual phase where final components for the ITk detector are built and put into the final ITk.

The contents of this thesis will mainly refer to topics related to ITk pre-production and the preparation of the ITk production.

CHAPTER 2

Tracking Detector Prerequisites

In general a tracking detector is defined as a measurement device, which measures the trajectory of a traversing particle, without deflection. In high energy physics it is common to measure a particle's trajectory in a magnetic field, to determine its charge and momentum. Both values are proportional to the radius of the circular flight trajectory of the particle, in the transverse plane, according to the Lorentz force [45]. Up until the 1980s, mainly bubble chambers [46] were used to track charged particles. Formerly, images from multiple bubble chamber perspectives were taken on film, to read out large volumes. Figure 2.1 shows an exemplary image, taken in the Big European Bubble Chamber in 1979, with curled tracks being visible induced by a D-meson decay. On the right, the manual analysis, of a CERN employee is visible, identifying all related particles and tracks.

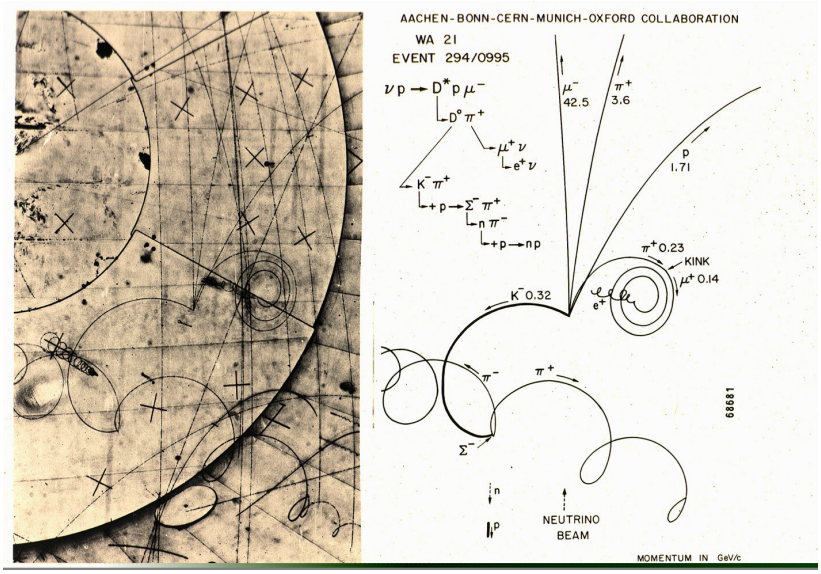


Figure 2.1: On the left an original photo taken by the Big European Bubble Chamber (BEBC) in 1978 is visible, on the right, the manually-analyzed tracks of a D-meson decay is visible [47]

It is evident, that this manual procedure has its limitations for statistically driven research, as particle physics is today. Gas-filled detectors, with modern electronic readout, are still used today

in the form of for example Gas Electron Multiplier detectors (GEMs) [48] and still employed, for example in the peripheral tracking of modern detectors, such as ALICE [49]. However, due to the development of accelerators with increasing luminosity, gas-filled detectors are rarely used close to the interaction point. Reasons for that are gain drops in gas-filled detectors, at high rates, expected close to the interaction points at the HL-LHC [50], as well as high pixel and readout electronic densities achievable in silicon microchips. Therefore, today particle tracking, in high density track areas, is addressed by pixel silicon particle detectors. They offer high precision, 3D-information of charged particles, while withstanding high radioactive doses, at high readout speeds with high spatial resolution. The low atomic number of silicon (Z=14) is ideal, for minimal energy loss of charged particles in the material, to minimize multiple scattering [45]. In the following the basic signal generation mechanisms, applicable for ITk, as well as the silicon-hybrid-pixel-detector design is explained.

2.1 Signal Generation

All tracking detectors require a signal in order to determine the position of a traversing particle. The signal is a current spike generated by an ionising particle in, for example, a silicon lattice. Signal generation mechanisms must be differentiated in photon and charged particle interactions. In the following Section 2.1, silicon is assumed as sensor material.

2.1.1 Photons

Photons interact with matter according to the Lambert-Beer law, as described in Equation (2.1) [45]. The law describes the probability of a photon traversing matter of the thickness x. Each photon of the incoming intensity I_0, with energy E, has an absorption probability depending on the materials absorption coefficient $\mu(E)$.

$$I(x) = I_0 e^{-\mu(E)x} \tag{2.1}$$

The absorption coefficient $\mu(E)$ is photon-energy and material dependent. The absorption coefficient for silicon is shown in Figure 2.2.

It is visible, that the total absorption coefficient μ includes three effects, depending on the photon energy.

- **Photoelectric Effect**: The photoelectric effect is dominant at low photon energies in silicon up to 0.1 MeV. Here the interacting photon transfers its entire energy to the interacting atom. This full absorption of the photon leads to the emission of a single electron. The electron energy is hereby equivalent to the initial photon energy minus its original binding energy in the atom. Figure 2.2 indicates, that the photoeffect cross section decreases rapidly with increasing photon energy. Not shown in the Figure is that the photoeffect cross section increases with increasing atomic number Z of the traversed medium at constant photon energy. In the top left a drop, followed by a rapid rise in the cross section is visible, which is related to the photon exceeding the binding energy of an inner shell electron, the so called absorption edge [45].
- **Compton Scattering**: Compton Scattering is dominant at photon energies between 0.1 MeV and 10 MeV in silicon and appears, when the photon energy significantly exceeds the binding

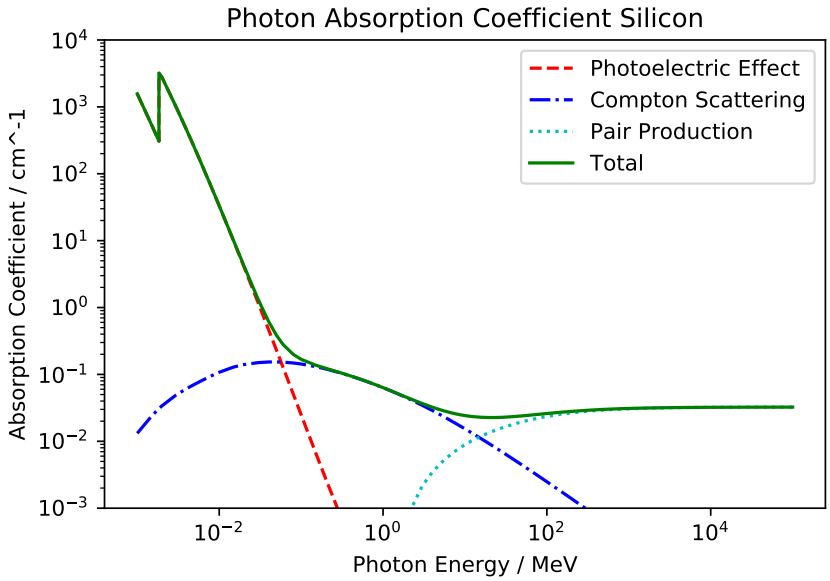


Figure 2.2: The absorption coefficient μ for Silicon [51]

energy of the interacting electron. In this case the photon transfers some of its kinetic energy T to the electron according to $T = E_\gamma - E'_\gamma$. The energy E'_γ is hereby the recoil energy of the scattered photon, given by Equation (2.2) [45].

$$E'_\gamma = \frac{E_\gamma}{1 + \frac{E_\gamma}{m_e c^2}(1 - \cos\theta_\gamma)} \tag{2.2}$$

E_γ is the initial photon energy, m_e the electron mass, c the speed of light and θ_γ the angle between the incoming and scattered photon. The maximal electron energy is detected at θ_γ=180°, this is the so called Compton edge. The energy of the scattered photon, as well as the freed electron is continuously distributed.

- **Pair Production**: Pair production is dominant at photon energies above 10 MeV, as a photon is converted into an electron-positron pair in the Coulomb field of a nucleus. The rest energy of an electron or positron is 511 keV, which explains, why pair production only occurs at energies starting at ≈1 MeV. In addition to the energy, necessary to create an electron and a positron, some of the photon energy is transferred to the nucleus as recoil. The pair production cross section σ_{pair} in to the high-energy approximation is given by Equation (2.3) [45].

$$\sigma_{pair} \approx \frac{7}{9}\frac{1}{X_0}\frac{A}{N_a \rho} \tag{2.3}$$

The radiation length X_0 [45] is hereby a characteristic property of the material.

2.1.2 Charged Particles

Charged particles interact in many collisions, with matter, transferred through the electromagnetic interaction. In the penetrated medium, this leads to ionisation and excitation of electrons [52]. Every single collision leads to a small energy loss W of the traversing particle, on the order of <100 eV [52]. The Bethe Bloch Equation (2.4) [52] describes the mean energy loss per penetration length for particles, which are heavier than electrons.

$$-\left\langle \frac{dE}{dx} \right\rangle = K \frac{Z}{A} \frac{z^2}{\beta^2} \left[\frac{1}{2} ln \left(\frac{2m_e c^2 \beta^2 \gamma^2 W_{max}}{I^2} \right) - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right] \tag{2.4}$$

K is hereby defined as $K = 4\pi N_A r_e^2 c^2 m_e = 0.307\,\text{MeV}\,\text{cm}^2\,\text{mol}^{-1}$ [45] with r_e the classical electron radius and m_e the electron mass, z being the charge of the traversing particle, β being the velocity of the traversing particle, Z & A being the atomic number and mass of the penetrated medium, $W_{max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1+2\gamma m_e/M+(m_e/M)^2}$ being the maximum transferable energy in a single collision, I being the mean excitation energy $I = 173\,\text{eV}$ for silicon [52] and $\delta(\beta\gamma)$ being the density correction factor. Figure 2.3 shows the Bethe Bloch Equation (2.4) for a proton and electron with $\beta\gamma = \frac{p}{mc}$ between 0.1 and 100.

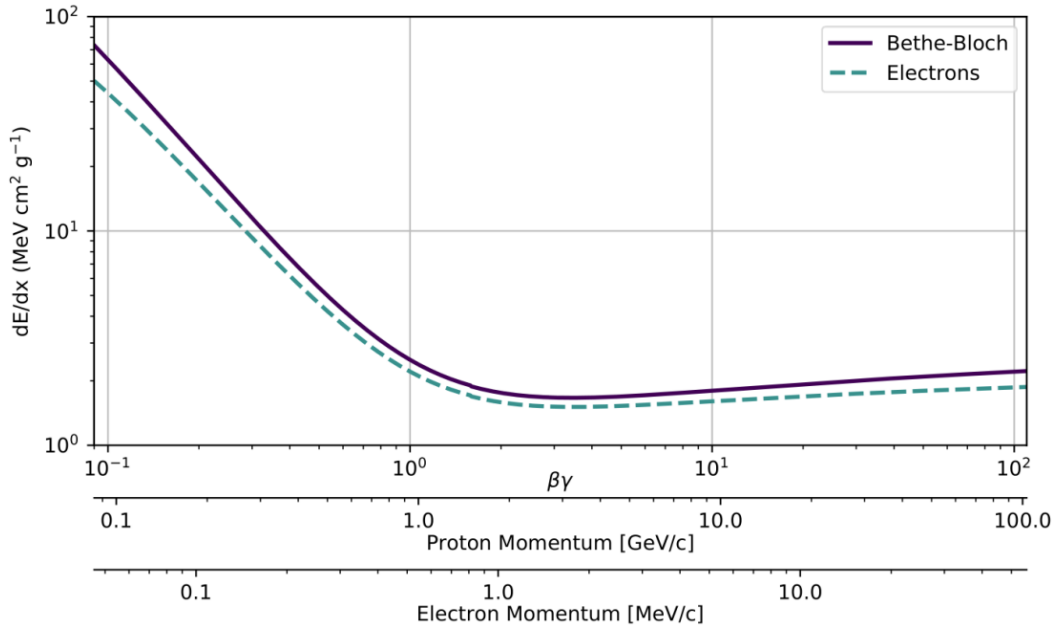


Figure 2.3: Specific energy loss of protons and electrons [53].

It is visible that for low energies the $\frac{1}{\beta^2}$ term dominates and that at $\beta\gamma \approx 3$, $\left\langle \frac{dE}{dx} \right\rangle$ reaches its minimum. Particles, with minimal energy loss, per penetration depth are toughest to detect by a detector, since they free minimal charge. Therefore these particles are called minimum ionising particles (MIPs). For $\beta\gamma > 3$, the logarithmic term starts to dominate, because of the increasing W_{max}, as well as the transverse electric field increase due to relativistic effects, which is expressed by the explicit $\beta^2\gamma^2$ dependence of the logarithmic term. The $\delta(\beta\gamma)$ term in Equation (2.4) is the

density-effect correction term. It appears due to the polarization of the medium by the traversing particle, which lowers the logarithmic rise at high energies. The density-effect correction term is parameterized for different energies as shown in Equation (2.5) [54]:

$$\delta(\beta\gamma) = \begin{cases} 2\zeta \ln 10 + C_D & \text{for} \quad \zeta \geq \zeta_1 \\ 2\zeta \ln 10 + C_D + a(\zeta_1 - \zeta)^k & \text{for} \quad \zeta_0 \leq \zeta < \zeta_1 \\ \delta_0 10^{2(\zeta - \zeta 0)} & \text{for} \quad \zeta < \zeta_0 \end{cases} \tag{2.5}$$

The material constant C_D for silicon can be assumed to be $2\ln(\hbar\omega_p/I) - 1 = -4.4351$ [54] and $\zeta = \log(\beta\gamma)$. Please note that the energy loss of electrons is dominated by additional effects, such as bremsstrahlung and multiple scattering, as discussed in e.g. [45].

2.1.3 Langau Distribution

The total energy loss of a charged particle along its trajectory in the detector material is the sum of multiple discrete energy transfers, with the energy loss being subject to statistical fluctuation. The deposited energy distribution can be described by a Landau-Vavilov function [55] [56]. The shape of the Landau-Vavilov distribution is skewed to higher energies, due to rare high energy δ-electron energy transfers [45]. Detectors with finite sensor thicknesses often cannot measure the complete tail of the Landau-Vavilov distribution, which biases the measured mean energy loss. Therefore the most probable value is used to describe the deposited particle energy. Figure 2.4 shows the energy loss distribution of 500 MeV pions in silicon.

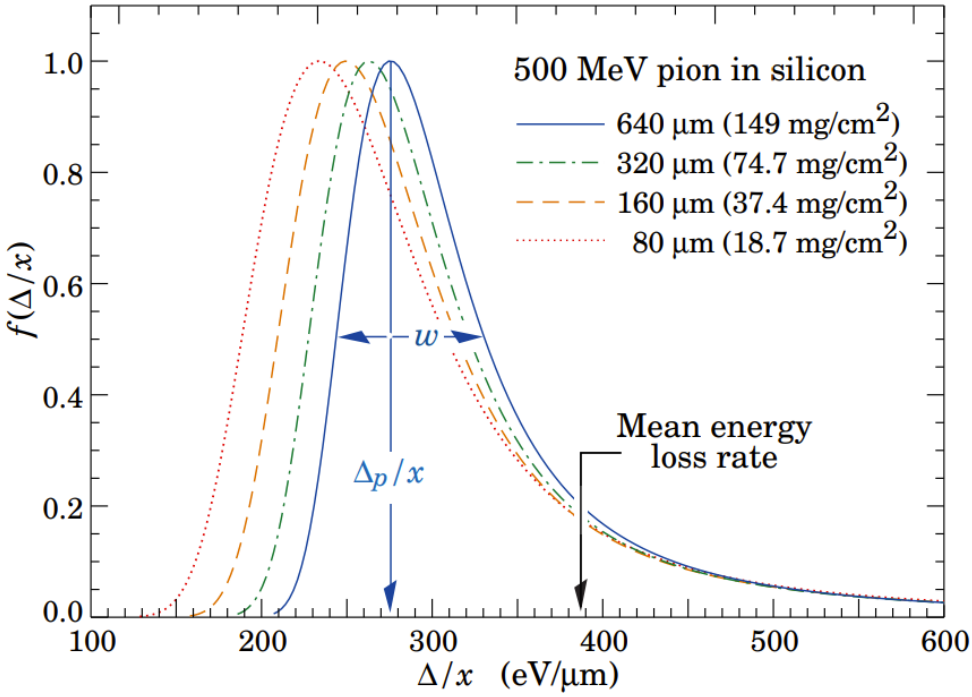


Figure 2.4: Energy loss Δ per thickness x normalized to the most probable value Δ_p/x for 500 MeV pions in silicon for multiple sensor thicknesses [57].

It is visible, that the most probable energy loss shifts to the right for increasing sensor thicknesses. The variable parameter w describes the full width at half maximum. With a sensor thickness of ≈ 160 µm, as used in ATLAS the most probable deposited energy Δp per thickness is ≈ 250 eV µm^{-1}, extracted from Figure 2.4. According to Equation (2.6) the number of generated electron-hole pairs N_{eh} in silicon can be calculated. Electron-hole pairs appear in the silicon lattice, where electrons in the valance band are excited into the conduction band, leaving behind holes (positively charged charge carrier equivalents) in the lattice [58]. This charge in the conduction band can be measured by the readout electronics, if it exceeds a certain detection threshold.

$$N_{eh} = \frac{\Delta p}{E_{eh}} \tag{2.6}$$

The energy in silicon, to generate one electron-hole pair is $E_{eh} = 3.65\,\text{eV}$. Therefore the most probable amount of generated electron-hole pairs in silicon by 500 MeV pions in a 160 µm thick sensor is $N_{eh} = (250\,\text{MeV} \cdot d)/3.65\,\text{eV} \approx 70 \cdot d$ with the sensor thickness d.

2.2 Silicon Hybrid Pixel Detector

From Chapter 2 and Section 1.4 the requirements for the ITk tracking chip, and the decision to use a pure silicon tracker for ITk are known. Section 2.1 introduces the physical processes responsible for signal generation in silicon detectors. The technology chosen for pixel ITk upgrade is the Silicon Hybrid Pixel Detector technology. This design features an independent sensor and readout chip design, produced separately and later connected pixel to pixel. The pixel to pixel connection process is called bump bonding, which uses microscopic solder balls to establish a pixel-to-pixel connection. The benefit of independent sensor and readout electronics manufacturing is the possibility to optimize each component according to its requirements. Readout chips for example use radiation-hard CMOS processes with small feature sizes (65 nm), enabling the implementation of fast signal amplification and complex digital logic for rapid data readout. Silicon sensors, on the other hand, are rarely produced in a CMOS process. They utilize high-resistivity silicon bulks with designs sustaining high bias voltages allowing for efficient charge collection after high levels of irradiation. Figure 2.5 shows a sensor as the top chip and the readout chip as the bottom chip. The pixelated structure of both chips is indicated by the small squares on both chips. A connection between each sensor pixel and readout chip pixel is established using bump bonds, indicated by the small circular balls. A traversing, minimum ionizing particle is also visible, injecting electrons and holes into the sensor pixel. The holes are guided to the top of the sensor, while the electrons are guided to the readout chip. Inside the readout chip, the charge is digitized, sent along the blue traces to the end of column logic, and then transmitted via a standard protocol and wire bonds to the ATLAS periphery.

2.2.1 Hybrid Pixel Sensor

The Hybrid Pixel sensor (short sensor) is designed to collect electron-hole pairs, generated by the processes discussed in Section 2.1. To obtain information about the location of the hit, the sensor features a pixel matrix with many diodes. All diodes are operated in reverse bias, to generate a large depletion zone. Inside the depletion zone, electric fields guide the induced electrons and holes to the readout and biasing electrodes, where the charge is removed. During the time, between the traversal of

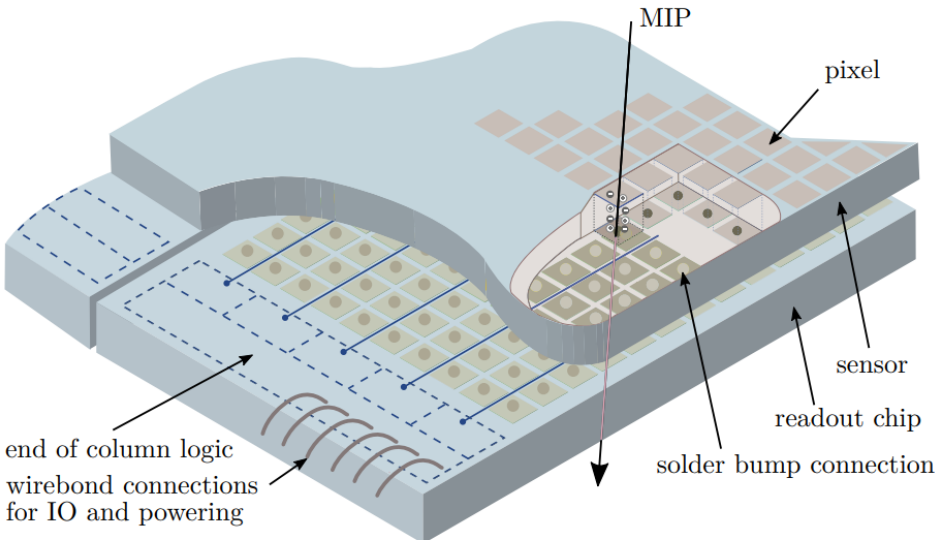


Figure 2.5: 3D render of a hybrid pixel detector being hit by a minimum ionizing particle (MIP). [53]

the particle until the complete drift of holes and electrons to their corresponding electrodes, a signal can be measured on the readout electrode, connected to a readout chip.

2.2.2 Hybrid Pixel Readout Chip

A hybrid pixel detector readout chip is a mixed signal chip, referring to its mix of analog and digital logic on one dye. The analog part of the readout chip receives the signal from a sensor using a solder bump connection as shown in Figure 2.5. This charge is then digitized and prepared for digital readout. One major advantage of pixel sensors compared to, e.g. strip sensors is their high density of readout channels per surface area. This allows a pixel chip to monitor a large surface, with high spatial resolution and high hit density, while necessitating a high-bandwidth data connection and complex digital architecture to read out all digital channels in as little time as possible. Luckily this architecture can be achieved using standard CMOS processes used in consumer electronics. Therefore, standardized design tools, especially for the digital part of the readout chip, can be used. In case of ATLAS the readout chip for its hybrid pixel detector is called ITkPix, discussed in the following Chapter.

CHAPTER 3

ITkPix - Hybrid Pixel Readout Chip

In this Chapter the components of a readout chip, as well as the novel readout chip for the ITk upgrade will be discussed. Figure 3.1 shows a readout chip picture, overlayed with markings for the two main

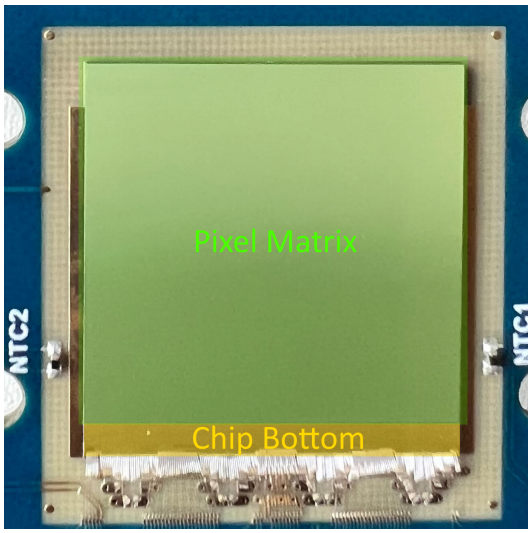


Figure 3.1: An image of ITkPixV1 indicating the ratio between pixel matrix and chip bottom.

components of a readout chip. The pixel matrix is overlayed in green and accompanying periphery, marked as chip bottom is overlayed in yellow.

1. **Pixel Matrix**: The pixel matrix contains many pixels, containing analog and digital logic, responsible for detecting a hit. From there the hit signal is digitized and processed by the pixel periphery. The pixel periphery takes care of encoding hit information, such as amount of detected charge, time of charge detection and which pixel was hit.

2. **Chip Bottom**: The chip bottom contains all blocks relevant for chip operation, for example, analog powering circuits, internal hit data processing, digital circuits for external communication, and many more explained in Section 3.2

One particular implementation of a readout chip is ITkPixV1.1. ITkPixV1.1 is short for ITk pixel

chip Version 1.1. Its full scale predecessor readout chips are summarized in Table 3.1. ITkPix is the general term for a class of readout chips developed by the RD53 Collaboration. The RD53 Collaboration is the reasearch and development group at CERN responsible for designing and producing the next generation of readout chips for the ATLAS and CMS pixel detector upgrades at the HL-LHC [59] [60].

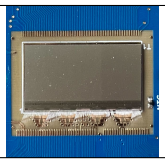
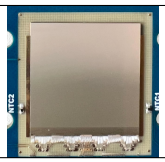
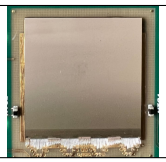
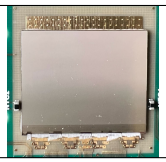
					Not Yet Submitted
Name	RD53A	ITkPixV1	ITkPixV1.1	CROCV1	ITkPixV2
Submission	May 2017	March 2020	Sept 2020	June 2021	TBD
Array Size	400 x 192	400 x 384	400 x 384	432 x 336	400 x 384
Dimensions	20 mm x 11.6 mm	20 mm x 19.2 mm	20 mm x 19.2 mm	21.6 mm x 16.8 mm	20 mm x 19.2 mm
Analog Front End	Sync [61], Lin [62], Diff [63]	Diff [63]	Diff [63]	Lin [62]	Diff [63]
Purpose	Large scale demonstrator and analog front end evaluator	First full scale ATLAS chip	Fixing high-current bug of ITkPixV1	First full scale CMS chip	Final ATLAS chip to be used in the detector

Table 3.1: A summary table of all large-scale chips developed by RD53 Collaboration.

From left to right, the chips appear in chronological order of submission. With subsequent submission, additional features were implemented which leads to an increased feature list and increased chip complexity from left to right. RD53A was the first large-scale demonstrator chip of the RD53 Collaboration. It was designed to test different buffer architectures, a novel design philosophy, which integrated manually designed analog front end islands into a fully synthesized digital sea, while testing three different analog front end designs. The three successor chips ITkPixV1, ITkPixV1.1 and CROCV1 are based on the RD53B design framework. Those three chips therefore only feature minor differences summarized in Table 3.1. In this thesis RD53B is used instead of e.g. ITkPixV1.1 in combination with common features of the three aforementioned chips. RD53A's successor is ITkPixV1, to demonstrate the successful enhancements of the analog front end performance, as well as proving the periphery being able to support the chip in its full scale, while adding additional digital features, such as isolated hit removal, data-merging or scan chain. Shortly after ITkPixV1.1 was submitted due to the high-current bug. The high-current bug relates to a storage cell, which was unintendedly used in the pixel matrix leading to high digital current consumption and data loss under certain conditions. This feature made characterization measurements for ITkPixV1 difficult. Appendix A offers more information concerning the high-current bug. ITkPixV1.1 was followed by CROCV1, for the first time verifying the new and improved linear analog front end [62] for CMS. ITkPixV2 is yet to be submitted and expected to be the final chip for the ITk upgrade. It incorporates

fixes for the high-current bug, as well as improvements based on many of the measurements presented in this thesis.

3.1 ITkPixV1.1 - Pixel Matrix

The pixel matrix constitutes the largest part of a readout chip, and is the active area on the chip, capable of measuring the charge injected by a sensor. Figure 3.2 shows the schematic construction of the ITkPixV1.1 pixel matrix. The whole matrix is contained inside the yellow surface and consists of 50 x 48 matrix cores, which is an identical group of pixels, that is copied over the whole pixel matrix. One matrix core is the smallest building block on the digital level, while all matrix cores share the same digital routing. The next smaller entity within a matrix core is a pixel quad. A pixel quad is an entity of four pixels, which share the same analog island for its analog front ends, surrounded by the synthesized digital sea. The analog front end is described in Section 3.1.1. The next smaller entity is a single pixel. One matrix core consists of 8x8 pixels. One pixel consists of the digital pixel logic, processing and storing, responsible for part of the hit and trigger data processing and storing each pixel's configuration, as well as the analog front end, which digitizes the analog charge signal received by a sensor.

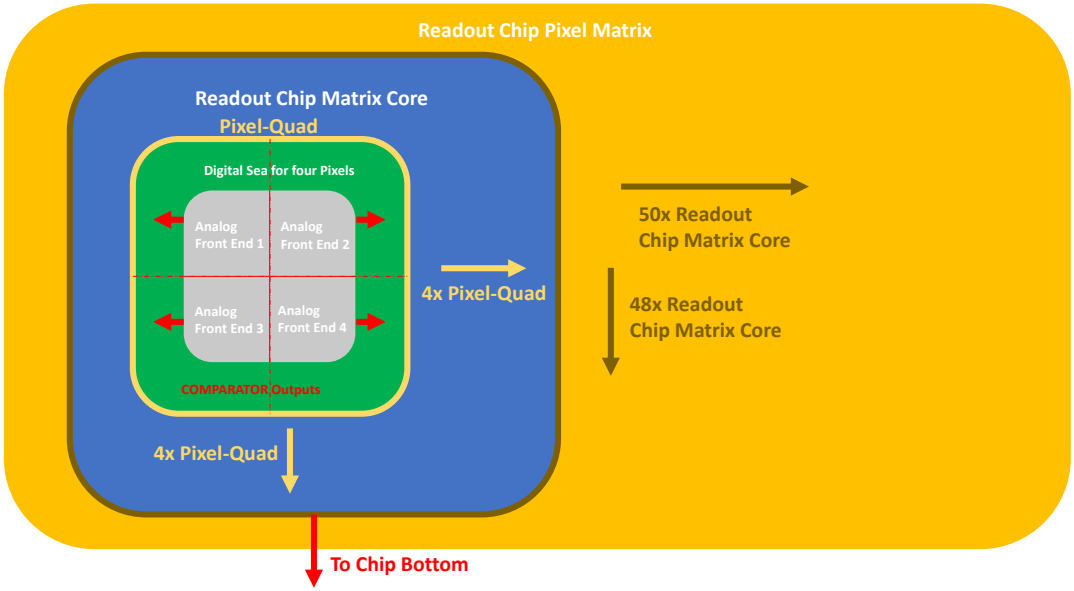
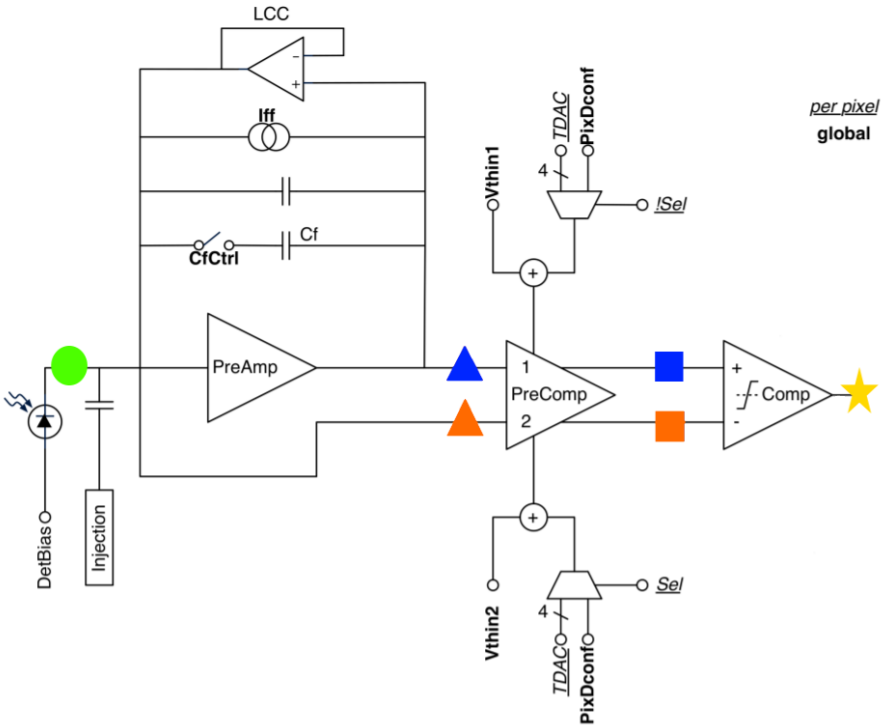


Figure 3.2: Schematic view of the main components inside ITkPixs pixel matrix.

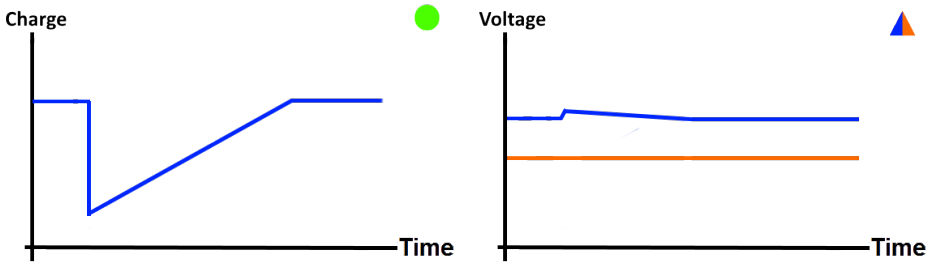
3.1.1 Analog Front End

The analog circuitry in the pixel matrix is called analog front end. The analog front end is responsible for the integration of the charge and the conversion of a signal that is proportional to the injected

charge into a time-proportional signal, which is measured digitally. Figure 3.3 shows the process of charge conversion to digital signal in the differential analog front end.

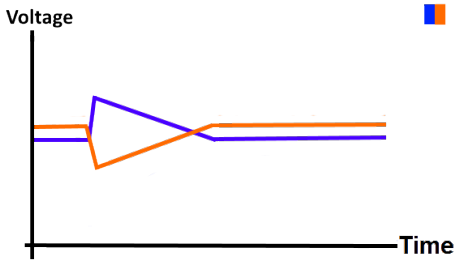


(a) Differential Front End Schematics [63]

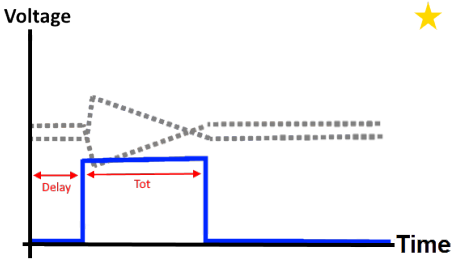


(b) Injection Signal [63]

(c) Pre-amplifier Output [63]



(d) Pre-comparator Output [63]



(e) Comparator Output [63]

Figure 3.3: Schematic view of charge conversion to digital signal via the differential analog front end [63]

Figure 3.3 shows the working principle of the differential analog front end. It starts with the

quick arrival of many electrons, as shown by the charge drop in Figure 3.3(b). This charge is supplied by a sensor or an injection capacitance, which simulates the steep drop in charge by instantly discharging a capacitance and injecting its charge into the amplification circuit. The pre-amplifier (PreaAmp) recognizes this charge deposited on the charge-integrating capacitance Cf and raises its output proportional to the voltage change at its input. The charge, however, is continuously removed by the constant current source Iff, which is responsible for the rising slope in Figure 3.3(b) and following Figures. The leakage current compensation circuit (LCC) is designed to compensate for DC leakage current coming from the sensor introduced by, e.g. radiation damage. In Figure 3.3(c) the input and output of the preamplifier are visible, which go into the pre-comparator (PreComp). This pre-comparator has another stage for amplification. In addition to that it compares the voltage levels of the preamplifier input, with the preamplifier output. The advantage of comparing the unamplified preamplifier input and amplified preamplifier output is the cancelation of DC offsets, which influence either branch of the precomparator. Figure 3.3(d) shows the signal after the precomparator. The two signals hint at a differential output, which is proportional to the input signal of the precomparator input. The DC offset of the two signals can be defined by two global threshold voltages, called vthin1 and vthin2, as well as one local threshold voltage, called TDAC. vhthin1 and vthin2 are displayed in blue and orange in Figure 3.3(d). An increase in vthin1, or TDAC for example, would increase the y-axis intercept of the blue signal, and vice versa for vthin2 and the orange signal (in Figure 3.3(d)). The two triangular precomparator outputs are forwarded to the final comparator as shown in Figure 3.3(e). This compares the two signals with each other and as soon as the blue signal is higher than the orange signal, outputs a digital one and zero other wise. The length of this signal is proportional to the depth of the charge signal seen in Figure 3.3(b), due to the constant discharging current Iff. Figure 3.3(e) defines two properties of the analog front end circuit, depending on, e.g., its supplied bias currents, analog front end delay and ToT vary. The analog front end delay defines the time, it takes the injected charge signal after injection to cross the threshold defined by vthin1 and vthin2. This depends on two factors:

- The drop rate of the initial charge signal. High charges have a more steeply falling slope (compare with Figure 3.3(b)).
- DC offset of the orange and blue signal (Figure 3.3(d)), referring to the threshold voltages vthin1 and vthin2.

ToT is short for time over threshold and refers to the width of the comparator output. The width of this signal is known to be proportional to the depth of the charge signal in Figure 3.3(b) at constant discharge currents Iff. This signal is a charge measure and depends on two factors:

- The drop depth (charge) of the initial charge signal. High charges have a deeper minimum (Figure 3.3(b)).
- The discharge current Iff. The higher the discharge current Iff, the faster the charge-integrating capacitance Cf is discharged and the faster it returns to the baseline and the shorter its ToT.

All of the above amplifiers and comparators are active components and require biasing. Table 3.2 summarizes all the biases with their names and functionality.

The rectangular signal output of the comparator (Figure 3.3(e)) is sampled with a 25 ns clock and stored in the hit buffer of the corresponding region. At this point, the signal is completely digitized

Text Name	Register Name [44]	Description
Preamplifier bias	DAC_PREAMP_DIFF	Pre-amplifier input stage current
Precomparator bias	DAC_PRECOMP_DIFF	Precomparator tail current
Comparator bias	DAC_COMP_DIFF	Comparator total current
Constant current Source Iff	DAC_VFF_DIFF	Preamp feedback current
Thresholdvoltage 1	DAC_TH1_DIFF	Negative threshold voltage branch offset
Thresholdvoltage 2	DAC_TH2_DIFF	Positive threshold voltage branch offset
Leakage current compensation	DAC_LCC_DIFF	Leakage current compensation current

Table 3.2: Table with a list of all bias currents according to the differential front end manual [63].

and will be read out with the arrival of a corresponding trigger. Please note that this circuitry is repeated many times on a single readout chip. Therefore, this set of circuits is called a pixel. In ITkPix there are, for example, $1.5 \cdot 10^5$ pixels per chip, and inside ITk there are $5 \cdot 10^9$ pixels in total.

3.2 ITkPixV1.1 - Chip Bottom

The chip bottom, combines analog and digital circuits. It is designed to be as small as possible, to maximize the active pixel matrix area, while leaving enough space for all blocks necessary for chip operation. The chip bottom is mainly responsible for the communication with the outside world, such as decoding commands, or encoding data generated by the pixel matrix. In addition to that the following features are incorporated in the chip bottom and shown in Figure 3.4:

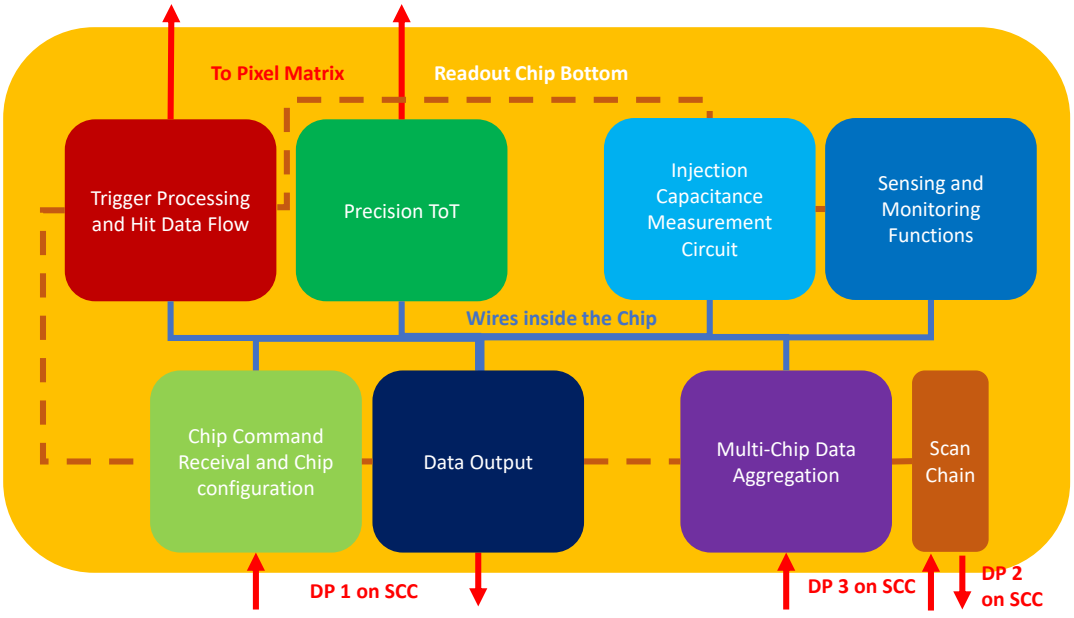


Figure 3.4: Schematic view of the main components inside RD53Bs chip bottom.

- **Sensing and Monitoring** consists of a multiplexer and ADC, to measure chip internal voltages and currents. This block is tested in Section 6.2.1.
- **Injection Capacitance Measurement** circuit is based on a charge pump, which is capable of measuring multiple copies of the injection capacitance indicated in Figure 3.3. This circuit is used and further explained in Section 7.2.5.
- **Precision Tot** is a ToT measurement circuit in the chip bottom which can be connected to individual pixels in the matrix by a multiplexer network. It features a timing resolution of 640 MHz instead of 40 MHz in the regular ToT. This circuit is used in many scans to circumvent the high-current bug. It is further explained in Appendix A.
- **Trigger Processing** ensures that the corresponding triggered hits are correctly recorded and assembled in the correct data-format, to be forwarded to the Data-Output. This block is further tested in Section 5.2.
- **Chip Command Receival** is responsible for the receival of commands form the DAQ-system and making changes to the chip operating parameters. This block is tested in Section 5.1.1.
- **Data Output** encodes and sends out all data according to the Xilinx aurora66 protocol [64]. This feature is initially tested in Section 5.2.5.
- **Multi-Chip Data Aggregation** or data-merging, receives and encodes data from a secondary ITkPixV1.1 into its own data stream. This feature is tested in Section F.2.48.
- **Scan Chain** technique used in testing. The objective is to make testing easier by providing a simple way to set and observe every flip-flop in an IC. All flip-flops of the aforementioned blocks are tested, except the ones for precision Tot, since it is not considered a critical feature of ITk. The scan chain is investigated in Appendix D.

All blocks are embedded in the yellow background in Figure 3.4, which represents the chip bottom, along with all its biasing and power distribution network. The blue line indicates metal traces, which connect all of the aforementioned blocks. In addition, the dashed brown line indicates all blocks, that are part of the scan chain. The scan chain is an alternative operating mode of all connected circuits, which connects them in a long shift register, making fast testing on flip flop level possible. Apart from the digital blocks in Figure 3.4, also biasing components are incorporated in the chip bottom, which are treated in more detail here.

The most important reference voltages and currents are summarized in Figure 3.5. All currents and voltages in the chip bottom and pixel matrix are derived from the main reference current, which is nominally 4 µA. This main reference current is called IREF. Figure 3.5 shows a schematic view on how IREF is generated and distributed. Initially a voltage of roughly 490 mV is generated by a silicon core bandgap, which is fine-tuned by a 4 bit DAC and distributed by a current mirror through RD53B. One of the voltages, which is proportional to IREF, is the offset voltage of the shunt regulator (VOFS). The voltage drop over a 24 900 Ω resistor (R_OFS) at 20 µA is expected to be 498 mV, which is the value, the 4 bit DAC is trimmed to. In addition to VOFS, the reference voltages for the LDO regulators VREFA, VREFD, as well as the ADC reference voltage VREF_ADC are generated, by sending mirrored currents through R_VREFD, R_VREFD, R_VREF_ADC.

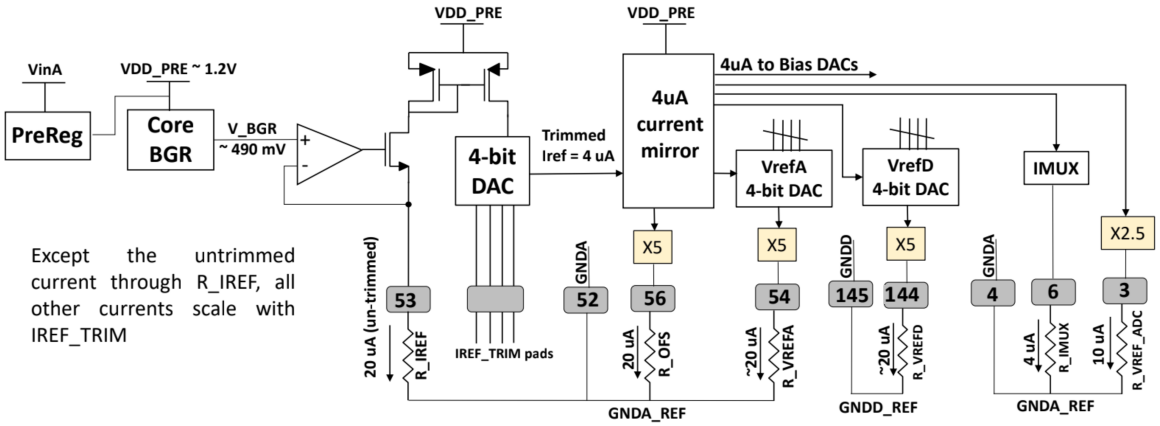


Figure 3.5: IREF generation and its dependants [44]

The LDO regulators are low drop out regulators, which are responsible for supplying the VDDD and VDDA power rails with 1.2 V at all times. LDO regulators regulate an output voltage that is powered from a higher voltage input [65].

In the following Chapter 4, the data acquisition system (DAQ), which is developed in part during this thesis is introduced, along with its hard and software components.

CHAPTER 4

Testing Environment

Building a reliable chip requires a reliable testing environment. The chip testing of ITkPixV1.1 proceeds in three stages in this thesis:

1. **Verification:** Verification occurs pre-submission and requires simulating ITkPixV1. Pre-submission verification ensures that readout system and chip work well together. During this stage it is important to adjust the readout system to the needs of the chip and verify end to end, that ITkPixV1.1 only sends expected data.

2. **Characterization:** Characterization occurs post-submission in actual hardware. In this stage it is important to qualitatively analyze the performance of individual chips. Especially analog chip components are known to have divergence between simulation and reality.

3. **Wafer probing:** This stage is aimed to bulk-test large quantities of ITkPixV1.1 on wafer level and quantitatively determine whether each individual chip works or not.

Looking at above requirements, a testing environment is needed, which can operate the chip not only in in hardware, but also simulate it pre-submission and allow versatile testing during characterization and fast, scale able testing during wafer probing. The readout system and simulation environment, fulfilling most of the requirements, called BDAQ53 will be explained in Section 4.1. In addition, chip testing requires interface boards between chip and BDAQ53 hardware. For RD53B the two most important desings with regard to this thesis will be explained in Section 4.2.

4.1 BDAQ53 Testing Environment

A readout system or data acquisition system (DAQ), developed in Bonn, called BDAQ53 [66] is used and further developed to fulfill the above criteria. In the following Sections the DAQ components, such as hardware, firmware, software and quality control measure for BDAQ53, called continuous integration (CI), will be discussed.

4.1.1 Hardware

BDAQ53 hardware consists of a custom-designed base board, hosting all relevant connectors for ITkPixV1.1 operation, as well as a consumer-grade FPGA board, as shown in Figure 4.1. The custom

base board mainly features connectors for the FPGA with different testing setup components. The power connector delivers power to the base board and FPGA. It requires a 5 V, 2 A power source. The USB port is used to flash new firmware to the FPGA, while the RJ-45 port is used to send TCP packages between BDAQ53 and computer. The general-purpose input-output (GPIO) display ports (DP), comprise a full-size display port, as well as a mini display port. Those ports are used to supply additional signals to ITkPixV1.1 during specific tests, discussed in the corresponding chapters. The aurora receiver display ports are connected to the FPGA's high-speed MGT lines. Three display ports feature one high-speed MGT line each, while the display port on the left features four high-speed MGT lines, allowing the chip to be read out at 4 x 1 280 Gbit s^{-1}. The same four display ports are used to transmit command data to the chip at 160 Mbit s^{-1} .

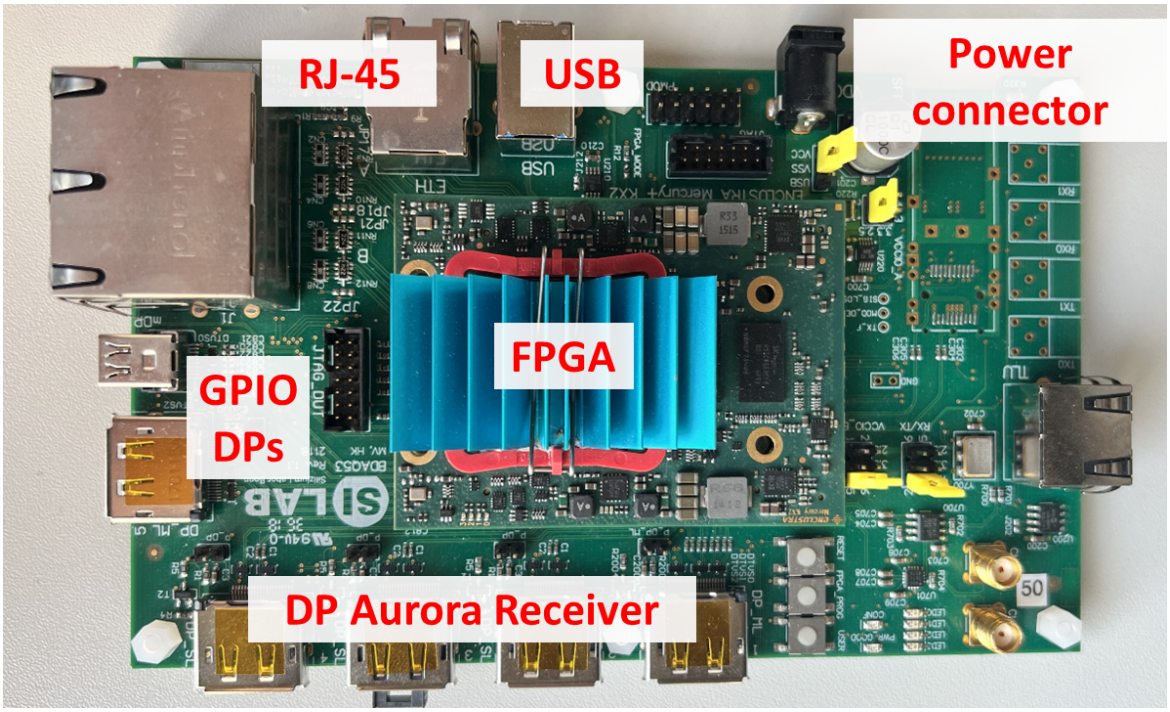


Figure 4.1: An image of the BDAQ53 board, with the main components labeled.

4.1.2 Firmware

Firmware defines the low-level control of BDAQ53 hardware. In contrast to software, which executes commands sequentially, firmware is used to define parallel logic blocks, which interact with each other under strict timing. The firmware is flashed to the BDAQ53 FPGA and among others, used to forward the data transmitted by the computer or chip to the corresponding receiver. Reading a register from ITkPixV1.1 would involve the BDAQ53 firmware in the following way:

1. BDAQ53 software sends a read register command via TCP to the firmware, running on the BDAQ53 board.

2. BDAQ53 firmware receives the TCP data at a different frequency than 160 MHz, which is the

RD53B command frequency.

3. A clock domain crossing to 160 MHz is performed.
4. Command is send out via display port to ITkPixV1.1.
5. BDAQ53 firmware waits for response of the chip on one of the MGT receivers.
6. Firmware receives response at 1 280 Mbit, stores it in a buffer and interleaves it with other data, to be transmitted to the computer.
7. A clock domain crossing is performed and the received data is sent out to the DAQ computer, using TCP, running BDAQ53 software.

One key feature for the development and testing of the test system itself, as well as the testing of its compatible chips, is simulation. During the development of ITkPixV1, the simulation of BDAQ53 was used to develop firmware and software for BDAQ53, without producing the chip. This is not only a key to rapid and in-time chip testing after the arrival of physical chips, but also allows for an in-depth analysis of erroneous Verilog code, both on the BDAQ53 and RD53B side.

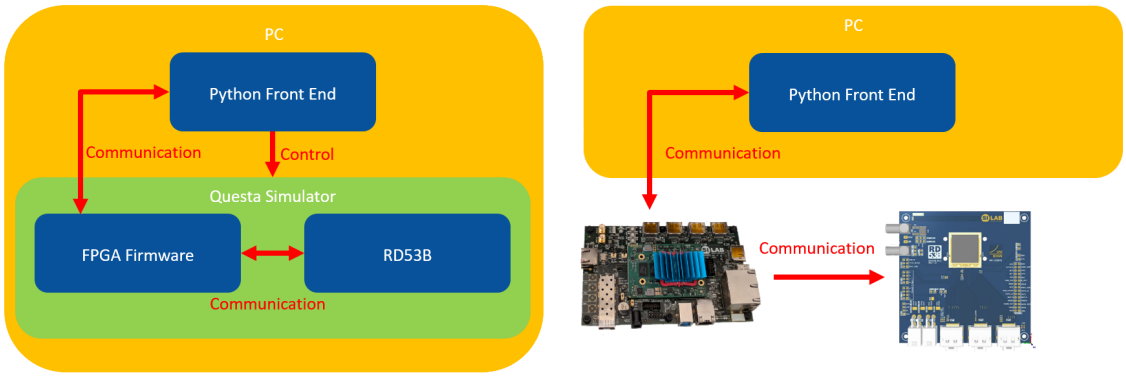


Figure 4.2: Two schematics for BDAQ53 operation. On the left in simulation mode or CI, which simulates the BDAQ53 firmware and RD53B. On the right with physical hardware.

Figure 4.2 shows the philosophy behind the BDAQ53 simulation framework. It is as simple as replacing the BDAQ53 hardware and device under test (in this case, a RD53B chip) with a Verilog simulator. The left part of Figure 4.2 shows that no hardware is required to run these tests. The yellow box indicates that everything takes place inside the computer. The computer runs the regular Python front end, exactly the same way as it would run with regular hardware, but instead of connecting to the BDAQ53 board via TCP, in this case it connects to the Questa simulator, which runs the Verilog code, defining the BDAQ53 firmware and the RD53B chip. The Python front end has some additional control over the Questa simulator, to mimic e.g. the injection of hits into the pixel matrix. During simulation, waveforms are used to study how each logic block behaves. Figure 4.4 shows the waveforms that are used to study the logic interaction between the logic blocks in the firmware or in the silicon logic blocks inside RD53B.

```
self.write_ecr()
self.registers['GCR_DEFAULT_CONFIG'].write(0xac75)   # Write Magic numbers to disable constant reset
self.registers['GCR_DEFAULT_CONFIG_B'].write(0x538a)   # Write Magic numbers to disable constant reset
```

Figure 4.3: An image of the python commands used to send data to the RD53B simulation in Figure 4.4

The signals shown in Figure 4.4 are generated through the standardized python front end. The peak marked in red on the top left of Figure 4.4 is generated by the *self.write_ecr()* command as shown in Figure 4.3, while the two "write register" commands in the yellow box in Figure 4.4 are generated by the *self.write[{register_name}].write({register_value})* commands in Figure 4.3. The simulation conserves not only the information written to the register, but also the timing relation between the *send clear* command and *register write* commands. With these base functions, it is possible to address any register and functionality on the chip to configure it and run it as defined in the RD53B manual[44].

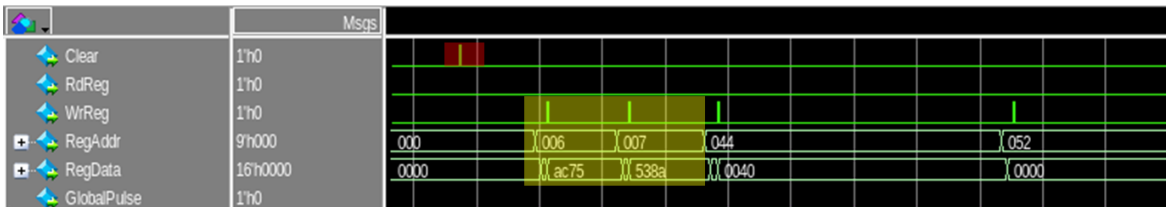


Figure 4.4: An image of the signals generated inside the chip based on the python code from Figure 4.3 in simulation.

This complete integration of the Python front end, BDAQ53 firmware, and chip simulation was useful not only for readout system development but also for chip verification at the logic level. Therefore, in addition to regular chip verification in system verilog the chip was continuously verified against its BDAQ53 integration, increasing the discovery potential for logic bugs. Shortly before submission, a multitude of scans was conducted, as discussed in Chapter 5.

4.1.3 Software

BDAQ53 software is written in Python [67], with versatility and code modularity in mind. Figure 4.5 summarizes the BDAQ53 code classes, as of the beginning of this thesis. Classes in red, depict main classes, white and blue classes depict base classes, with the one purple class referring to the basil framework, which is also developed in Bonn, providing basic hardware interfaces. Goal of BDAQ53 software is to allow the user to focus on the development of tests for ITkPixV1.1 with the configuration of DAQ hardware, initialization of data and file handling taken care of automatically.

Figure 4.5 summarizes the modular concept of BDAQ53. From Section 4.1.2, it is clear, that BDAQ53 is a translator between computer and RD53 Collaboration chips. Therefore hardware drivers for the BDAQ53 firmware, as well as every chip supported by BDAQ53 are necessary. The BDAQ53 firmware driver depends on basil, as well as custom command transmitter modules, that transmit data to the chip and custom aurora receiver modules, that buffer data received from the chip. This software and firmware part was extended by adding data-merging test modules, as explained in Section 6.2.2 and a scan chain module as explained in Section D. The chip driver, labelled RD53A in Figure 4.5, is replaced with new chip classes, one of which is the ITkPixV1 driver class, depending on ITkPixV1 register class, as well as ITkPixV1.1 calibration, chip base and mask object. Please note, that the

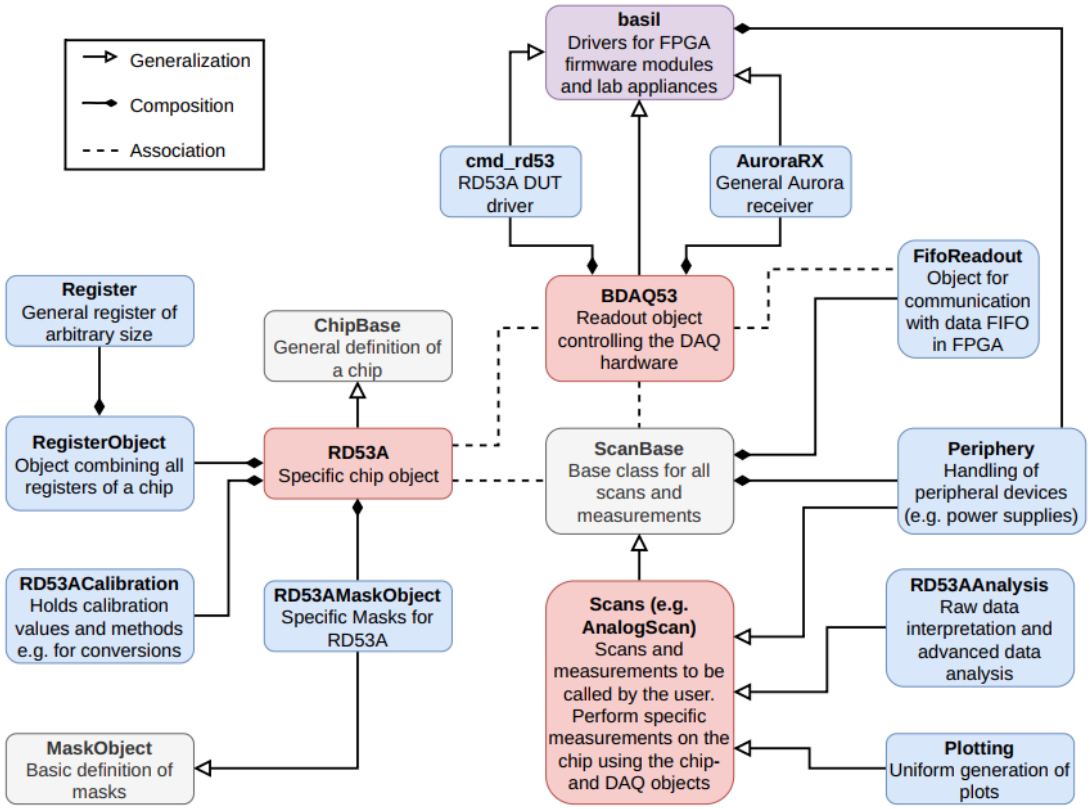


Figure 4.5: BDAQ53 software class diagram [66]. Main classes are depicted in red, base classes in white. The basil framework in purple provides basic hardware interface classes.

ITkPixV1 driver class inherits from all those classes, with ITkPixV1 characteristics stored only in the ITkPixV1 driver class itself, keeping the modularity of BDAQ53 intact. Both driver classes are initialized in the ScanBase class, which takes care of procedures, that are necessary in every scan, such as BDAQ53 firmware initialization, ITkPixV1 initialization, generation of files, to store data and many other thing. All scans inherit from ScanBase, which allows users to step in after the software has verified, that BDAQ53 firmware, chip and computer communicate successfully and begin its test script from a known chip state. The data received from the chip is then analyzed by a custom analysis class, decoding the chip data and preparing the data for plotting. A test script or scan is typically designed to test individual chip components. Three of the most common scans to test the pixel matrix are summarized in the following Sections.

Digital Scan

A digital scan is a scan that tests the processing of digital hits at a single-pixel level. For this purpose, a rectangular signal is injected behind the comparator in Figure 3.3. This rectangular signal replaces the signal sent by the analog front end and has a well known signal width, which is then digitized. An ITkPixV1.1 digital scan injects in 400 pixels at a time one hundred times and measured whether all

hits are received properly. A resulting hit map with all pixels working is shown in Figure 4.6.

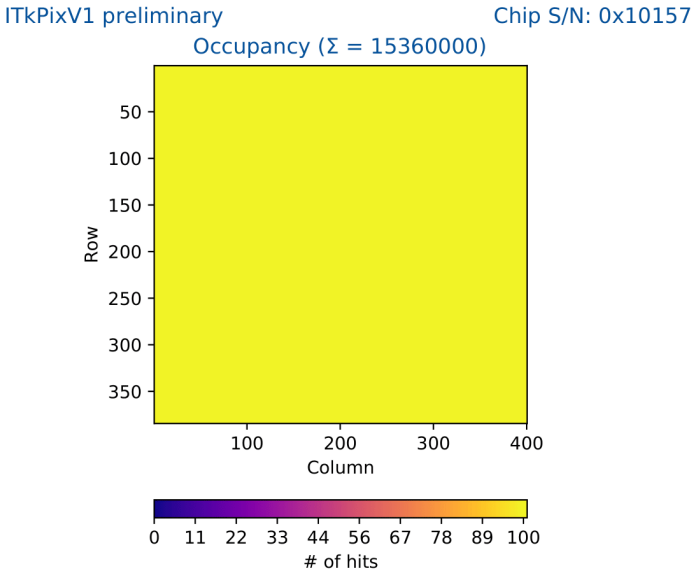


Figure 4.6: Digital hit map with 100 % occupancy

Figure 4.6 shows an ITkPixV1.1, with the columns on the x-axis and the rows on the y-axis. The color indicates the number of detected injections. In this case, the number of received digital injections corresponds to 100 for all pixels, which translates to a fully working digital matrix.

Analog Scan

An analog scan works just like a digital scan, except that it injects a known charge into the analog front end at the green dot in Figure 3.3. The hit map output of an ideal analog scan looks just like an ideal digital scan as shown in Figure 4.6. It may be noted that due to the high current bug, described in Section A, in ITkPixV1 and the single ToT feature in ITkPixV1.1, introduced by the metal fix, this test is conducted in precision Tot mode.

Threshold Scan

A threshold scan measures the charge detection threshold of each pixel. Section 3.1.1 describes the way signals are processed inside the analog front end. It is therefore known, that increasing injected charges yield an increasing ToT value, if they are above a pixel's analog front end's detection threshold. This threshold is defined globally by the threshold voltage and locally on a per-pixel base via TDAC. Which threshold voltage corresponds to which detection threshold is measured by injecting increasingly large charges into the analog front end. Another way of executing a threshold scan is to run multiple analog scans with increasing charge. Figure 4.7 shows this scan for a single pixel.

The y-axis of Figure 4.7 shows the number of hits detected in the output of the analog front end comparator. During this example, each charge was injected 100 times. Along the x-axis, the increasing injected charge is displayed in delta vcal. Each point on this graph is its own analog scan for a

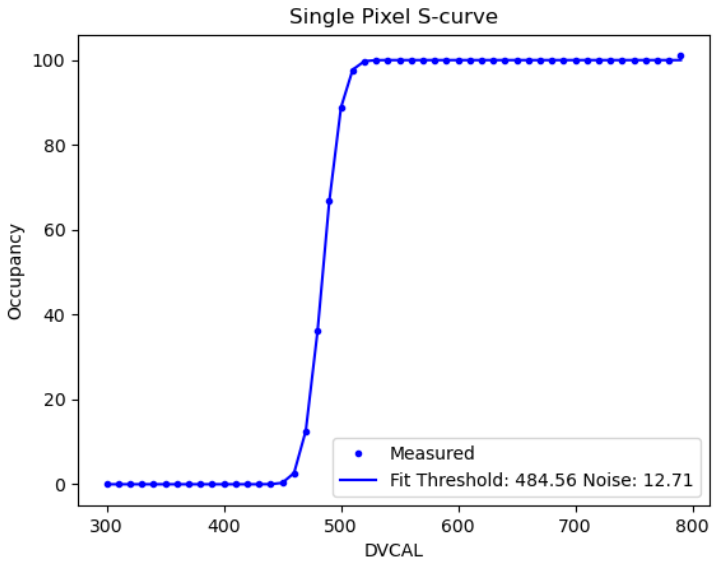


Figure 4.7: S-curve from a threshold scan for a single pixel.

single pixel. The resulting S-curve starts with zero occupancy at low charges and then transitions to one-hundred around 500 delta vcal (DVCAL). An S-curve can be described using the cumulative distribution function of the Gaussian distribution, as shown in Equation (4.1):

$$R(q) = \frac{N_{inj}}{2}\left(1 + erf\left(\frac{q-\mu}{\sqrt{2}\sigma}\right)\right) \tag{4.1}$$

Equation (4.1) has three parameters, which can be fit to the function displayed in Figure 4.7. N_{inj} describes the number of injections per pixel. The μ parameter describes the pixel's detection threshold, which is the charge, for which the measured pixel receives 50 % of N_{inj}. The parameter σ is proportional to the region where the measured occupancy is > 0 % and < 100 %. For an ideal pixel, the σ would be zero and the S-curve would be represented by a step function with infinite gradient at the detection threshold. For example the pixel in Figure 4.7 has a N_{inj} of 100, detection threshold μ of 485 delta vcal, with a noise intensity σ of 12 delta vcal. A conversion between delta vcal and electrons can be found in Section 7.2.5. In addition to the detection threshold, a threshold scan can also measure the in-time threshold of each individual pixel. This is achieved by considering only hits, that arrive less than 25 ns after analog injection. This effect is charge dependent, since larger injected charges have a steeper rising edge and are therefore detected within earlier bunch crossing IDs than smaller charges. This delay effect is further explained in Section 3.1.1. The in-time threshold scan, considering only a subset of the received hits, has a right shifted S-curve with a higher detection threshold than the regular threshold scan.

4.1.4 Continuous Integration (CI)

In academia, reproducibility of results is critical. To ensure that BDAQ53 has a stable and reproducible behavior, continuous integration practices are introduced. Continuous integration (CI) is a practice of

software development, that helps ensure the longevity and functionality of code written by a multitude of developers. It is a common problem that features contributed to a repository by one developer are overwritten or broken by following commits. Therefore, it is a key objective of CI to define tests for each feature or function in the repository. BDAQ53 CI tests hadrware, firmware and software on four levels.

- **Codeing style:** The code style CI monitors the code formatting according to PEP8. This is to proper searchability and readability of all uploaded code. Since Python allows for multiple formatting styles and, e.g., ignores white spaces, it is crucial for a team of developers to adhere to a consistent set of coding rules to enhance readability and understanding of the code, preventing code errors already in an early stage. If all changes adhere to the PEP8 standard, the test is passed.
- **Software:** Software tests are fast and parallelizable, testing the functionality of all major classes and scans in BDAQ53. Therefore, the BDAQ53 repository includes not only the code to test the chips, but also the code that tests the code and compares the result with a predefined set of reference outputs. It is quite common that a change in one base function has an effect on many functions that rely on this method, breaking a large chunk of the repository. If all functions are callable and all scan outputs are consistent with a set of reference files, this CI is passed.
- **Simulation:** Simulation is rare in CI, due to its long execution times and the need for proprietary software. BDAQ53 nevertheless uses this class of CI by hosting its own simulation servers and accessing the group licenses via internal license servers. The simulation deployed there is still one hundred percent containerized and paralellized. This set of CI tests not only the Python side of BDAQ53, but also the verilog code (firmware). Capturing the compitability changes at the verilog and chip level. This is a key feature for the long-term support of a multitude of chips. If the simulation output is consistent with a set of reference files, this CI passes.
- **Hardware:** The most complex test that covers most of the features of BDAQ53 is the so-called hardware test. As the name implies, it utilizes actual BDAQ53 hardware with a real RD53A and ITkPixV1.1 chip, located inside our laboratory, called SILAB. It tests the complete installation, firmware build and scanning process, copying the latest BDAQ53 repository to a SILAB testing server, building the latest firmware, and running a set of predefined scans. If the scan output is consistent with a set of reference files, this CI passes.

If all the tests in CI are successful, the changes are ready to be merged into the development branch, ensuring that no breaking changes are added to the repository and that BDAQ53 results are reproducible at all times.

4.2 RD53B Interface Cards

When a chip arrives, it resembles a piece of silicon, which has no easy way of connecting to the outside world. In Section 4.1.1, display port connectors are introduced as connectors between the BDAQ53 board and the chip. The display port on the chip side is mounted on an interface card, which features multiple connectors for power, measuring and data. For RD53B two types of interface cards are used in this thesis, one called Single-Chip Card and one called probe card. One key difference

between the two cards is the way they establish electrical contact with the chip. The Single-Chip Card uses a permanent, wire-bonding [68] connection between chip and Single-Chip Card, while the probe card uses a nonpermanent, tungsten needle connection. The nonpermanent connection is especially important during wafer probing, which is a quality assurance step executed on wafer level, after which the chips are further processed and later assembled. Table 4.1 shows a comparison between probe card and Single-Chip Card. The probe card features an additional I2C bus, to control its active components. The I2C bus is included in one of the Display Ports on the bottom of the probe card (See also Figure 6.1 DP2).

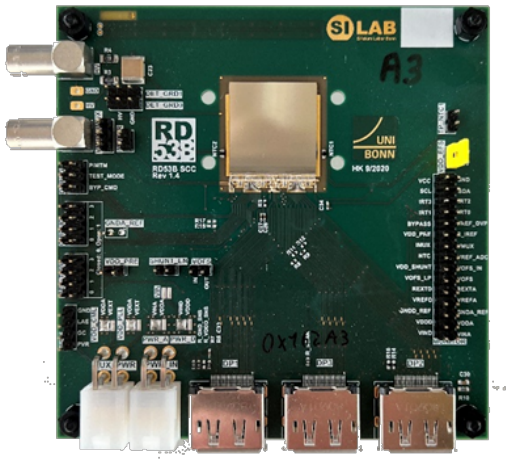
	
Single-Chip Card	probe card
10 cm x 10 cm	10 cm x 10 cm
2 x Chip Power, 3 x Chip Data	2 x Chip Power, 3 x Chip Data
2 x SMA (readout chip MUX, sensor Bias) 11 x GPIO Jumper Pads	1 x SMA (probe card MUX), 8 x PMOD GPIO
Passive components only	1 x MUX, 3 x I2C to GPIO, 2 x Levelshifter, 1 x Eeprom
194 x Wirebond Pads	194 x Tungsten Needles, including two edge sensors

Table 4.1: Comparing Single-Chip Card and probe card

The edge sensors of the probe card are used to determine whether a contact is established between ITkPixV1.1 and probe card. Therefore, each edge sensor has two needles. The first needle, is oriented vertically, like all the others shown in Figure 7.2(b). The second needle is horizontally oriented, on which the said first needle is suspended and in contact when the probe card does not touch the wafer. In the case where the needle card is touching the wafer, the said first needle is suspended by the wafer, while the said second needle remains in its original position, separating the two needles. A simple circuit is used to determine the resistance between the two needles and therefore determine whether the wafer and probe card are in contact. The Single-Chip Card is used for bench testing and characterization in chapter 6 and the probe card is used for wafer probing and large scale testing in Chapter 7.

CHAPTER 5

ITkPixV1.1 Verification

In Section 3 the main components of a readout chip are summarized. During ITkPixV1 verification, prior to arrival of the chips, both components, namely the chip bottom and the pixel matrix, are tested. The simulation and verification environment is described in Section 4.1.2. For the Verilog simulation, Questa is used together with cocotb [69] as Python interface.

5.1 Chip Bottom

The chip bottom as explained in Section 3.2 is responsible for all peripheral tasks, such as command decoding, data processing, data encoding, temperature measurement, power distribution, and many more. The type of simulation utilized in the scope of this thesis is especially suited for the testing of digital components. Therefore, command decoding, data processing, and data encoding is tested. Usual RTL tests are conducted in multiple stages, with ever-increasing block complexity and occasional external input to signals that are not exposed on the physical chip. During the following simulation ITkPixV1 is simulated as a whole, without interfering with the chip on a gate or cell level. During verification as described, only chip pads, that will also be accessible on the final chip are used to transmit data to the readout chip or receive data in the BDAQ53 system. For data transmission, it is possible to use the existing BDAQ53 command encoders for RD53A with minor modifications. The command encoder module receives the commands to be transmitted to the readout chip in 8 bit blocks, serializes them and transmits the data with 160 Mbit s^{-1} to the chip. The reader may be reminded that the actual data rate is lower, since RD53B uses a 5 bit to 8 bit encoding to minimize transmission errors in the high radiation environment.

For reliable testing, it is essential to define a proper initialization sequence to establish communication with the chip. According to the manual [44], the connection to the chip is established in the following steps:

1. RD53B reset
2. PLL lock (phase-locked loop)
3. Frame boundary locking
4. Communication lock

To ensure that the chip is in a well-defined state before starting the initialization sequence, a slow clock of 1 MHz is applied to the chip command input for 10,000 cycles or 1 ms. This slow clock leads to the chip resetting to its default state with a known register and pixel configuration. This signal is shown in Figure 5.1. This Figure displays a waveform, with the signal state[1] on the y-axis and the time on the x-axis.

Figure 5.1: Slow clock command applied to the command input of RD53B for initial reset.

From here a faster 80 MHz clock is applied to the chips command input, for the PLL to lock. Since there is no dedicated clock line supplied to RD53B the reference clock is recovered from the command stream, by the PLL. The signal is applied again for 1,000 cycles or 0.1 ms, as shown in Figure 5.2.

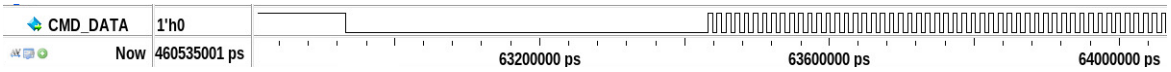


Figure 5.2: Fast clock command applied to the command input of RD53B for correct PLL lock.

As mentioned in the above enumeration, this signal is followed by 2,000 sync commands over 0.2 ms for the channel to synchronize and complete its frame boundary locking, as shown in Figure 5.3. Now the chip is ready to receive commands, as indicated by the lower signal "Locked" rising in Figure 5.4.

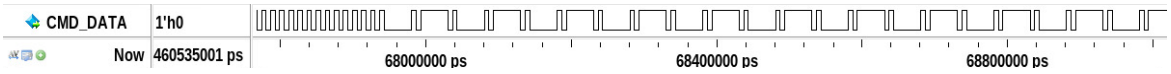


Figure 5.3: Multiple sync commands being send to the command input of RD53B for correct frame alignment.

The ability to receive commands is necessary for the chip to be configured to establish aurora communication with the BDAQ53 board and software. Therefore, Figure 5.4 shows the configuration of 18 registers, telling the chip, which aurora lanes are active on the BDAQ53 board, as well, as which data frequency is expected, in addition one of the first registers to be written is the so-called "GCR_DEFAULT_CONFIG"-register, which acts as a key to multiplex between the hardwired default configuration of the chip, and the adjustable configuration, written via register write commands. The 64 bit key is usually the first register write command to be sent. This process is shown in Figure 4.3 and Figure 4.4. Figure 5.4 also summarizes the whole initialization procedure, with the slow clock on the left, the channel synchronizer locking with the rising "Lock" command, as well as the register writing in the bottom four rows of the Figure. The row RdReg and WrReg indicate, whether a read or write command for the register address currently visible in line RegAddr was received. In case of a write command, the data currently displayed in RegData is written to the corresponding chip register. and finally the BDAQ53 board indicating that it received valid aurora frames and a successful aurora channel configuration is established, as shown in lines RX_LANE_UP and RX_CHANNEL_UP in Figure 5.5.

[1] high for logic one, low for logic zero

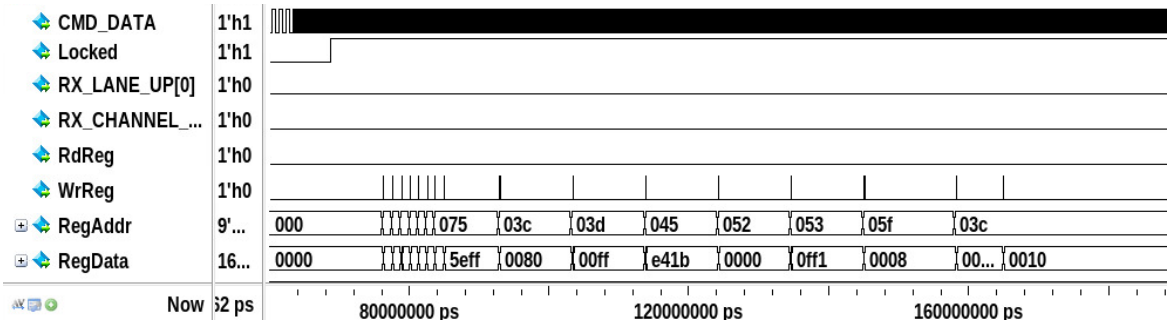


Figure 5.4: Configuration for communication establishment written to RD53B.

This procedure is the initial proof that not only RD53B is capable of receiving commands from the DAQ site, but also that BDAQ53 is capable of operating RD53B chips. This initialization sequence is performed at the beginning of every simulation and physical scan.

5.1.1 Register Write and Read Test

After establishing a reliable procedure to communicate with RD53B chips, it is important to ensure that all registers can be written and read within their expected range. Therefore, the Register Write and Read Test is performed, which tests each individual bit of each register. In terms of concreteness, the test first writes a binary $0b01010101$, followed by a read-back, then a binary $0b10101010$ to each register, again followed by a read-back. This test ensures that both states of each bit in each register are working. Therefore, this test proves the correct connection of each register, while ensuring that the register reading and register writing works reliably between DAQ and RD53B. Figure 5.5 shows the test procedure in simulation. The signal "CMD_DATA" at the very top shows the command stream sent from the BDAQ53 board to the RD53B. Followed by the Channel-Synchronizer "Lock" bit. The "RX_LANE_UP" and "CHANNEL_UP" indicate successful receipt of aurora frames on the BDAQ53 side. The four lowest signals are signals inside RD53B, which indicate the reception of a read command, write command, the register address to be read or written, such as the value to be written to/ read from the corresponding register address. The full test sequence starts as shown in Figure 5.4, then followed by the sequence shown in Figure 5.5. It is visible that the sequence starts with a few write commands, like shown in Figure 5.4. The test then continues with one write command, followed by two read commands. The two read commands are necessary here due to a feature in ITkPixV1 described in Section C. Finally the data is received at the simulated BDAQ53 FPGA as the "FIFO_DATA" line indicates.

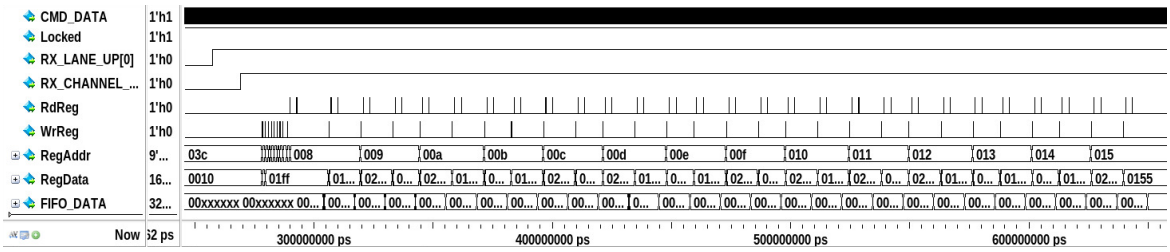


Figure 5.5: A waveform diagram from the , showing the signals, being triggered to conduct a register test.

5.2 Pixel Matrix

After implementing a reliable procedure to establish communication with RD53B and verifying the ability to write and read registers in RD53B with BDAQ53, the next step is to verify tests that utilize injection, trigger and configure the pixel matrix.

5.2.1 Digital Injection

Digital injection is a procedure in which a digital pulse is injected behind the comparator of the analog front end[2], to test the digital logic from pixel to readout. In order to test this, it is necessary to enable digital injection, as shown in the red region of Figure 5.6. Afterwards, it is sufficient to send an injection command and a trigger command with the correct timing. The trigger command must be correlated with the cal command, and the hit is kept within the pixel storage. The trigger commands can be seen in violet, while the injection command is marked in orange. The blue area indicates the receival of hit data in the simulated FPGA of the BDAQ53 board. In total, Figure 5.6 shows two manually triggered digital injections, with succesful data reception at the FPGA side.

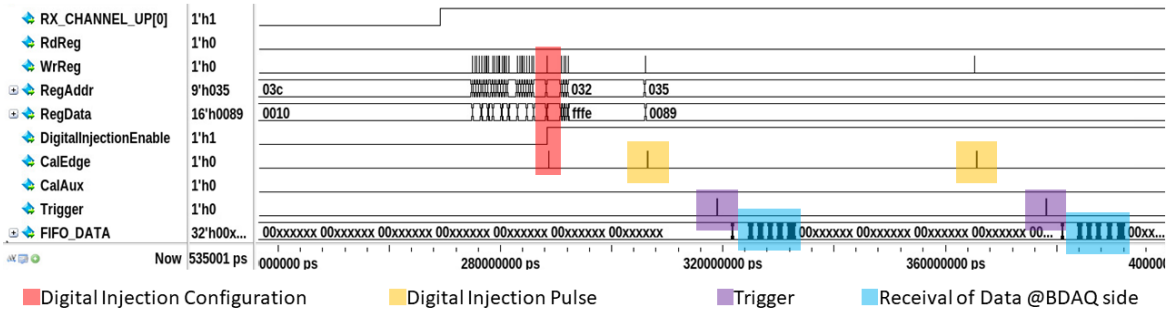


Figure 5.6: A waveform diagram from simulation, showing the signals, being triggered to conduct two digital injections.

5.2.2 Self-Trigger Test

Self-triggering is a RD53B feature, aimed to automatically detect hits on the hitor bus and send a trigger command with the correct timing to read out the data. Figure 5.7 shows the arming for digital injection in red, which consists of enabling the digital injection bit, along with a cal edge pulse to prime the calibration injection circuit. Immediately after that, the self-trigger bit is enabled, highlighted in mint color, followed by setting the trigger pattern to be sent (0x0000 –> 0xfffe), the trigger delay, and the trigger command multiplier (how often the trigger pattern 0xfffe is sent). Compared to Section 5.2.1 it is no longer necessary to send a trigger command via the command line. Here, the injection, marked in yellow, is automatically detected by the self-triggering block on the hitor bus, highlighted in orange. After a defined trigger delay, a trigger is sent automatically and the hit data is sent to BDAQ53 as the blue highlights in Figure 5.7 indicate.

[2] Star position in Figure 3.3(a)

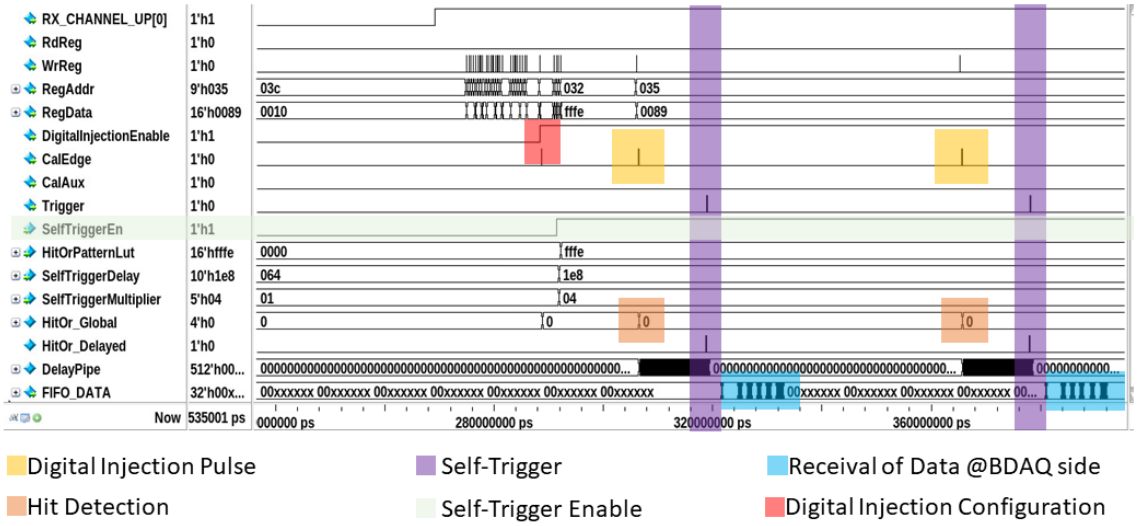


Figure 5.7: A waveform diagram from simulation, showing the signals, being triggered to conduct two self triggered injections.

5.2.3 Analog Single Injection

Analog single injection works according to the calibration injection circuit, at the rising edge of the Cal Edge signal. Figure 5.8 shows the RD53B configuration for analog injections in red, beginning with the definition of the vcal high and vcal med DACs, followed by the enabling of digital injection, with a couple of Cal Edge signals to prime the calibration injection circuit. This procedure is followed by a rising Cal Edge command, marked in orange, which leads to a hit being detected in one of the injected pixels. The trigger, highlighted in violet is send manually, while the data at the BDAQ53 board is received as labelled in blue.

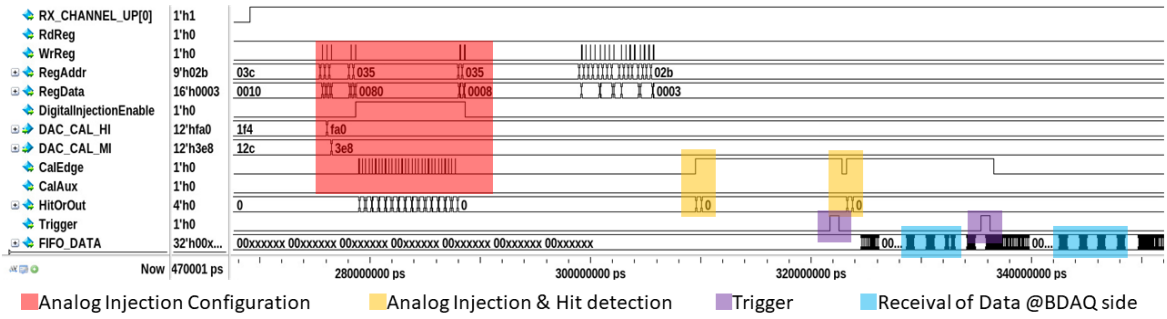


Figure 5.8: A waveform diagram from simulation, showing the signals, being triggered to conduct two analog single injections.

5.2.4 Matrix configuration

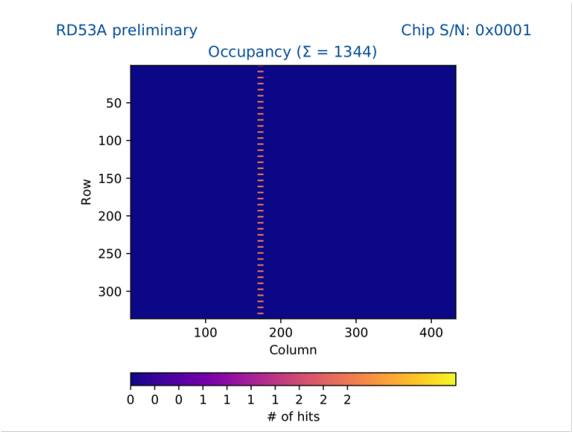
Each pixel in RD53B has 8 bit. 5 bit for TDAC tuning and 3 bit for enabling injection, powering the digital logic of each pixel and connecting the pixel to the hitor bus. Each of those bits need to be tuned and configured efficiently. Matrix writing is one of the most time-consuming steps in RD53B testing. Therefore, it is essential to have efficient means of configuring the pixel matrix. RD53B has two methods to configure the pixel matrix, the write mode is defined by the pix mode register. Each pixel matrix configuration method is based on simple write commands to the pixel portal register. This register is multiplexed to the corresponding pixel core via the region col and region row register, which address the correct pixel for configuration. The number of commands necessary to write the entire matrix varies greatly, as Table 5.1 shows.

Method	#commands to write full matrix
Single pixel at a time	77200 [44]
Broadcasting to first core column	1544[44]

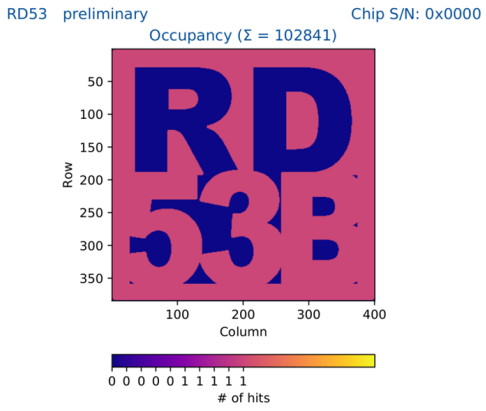
Table 5.1: Command length comparison for different write modes

The significantly reduced number of write commands in broadcasting mode is related to the fact that only the first core column is written, and this configuration is chip-internally copied to all other core columns. This write mode is especially well suited for mask shifting.

Figure 5.9(b) shows the BDAQ53s capability to write masks to ITkPixV1.1 in simulation, as well, as in hardware.



(a) A simulated ITkPixV1 digital scan, with default masking.



(b) A simulated ITkPixV1 digital scan, with the RD53B logo for masking.

Figure 5.9: Comparison between default injection pattern in RD53B and a configured pixel matrix.

5.2.5 Data Analysis

Figures 5.9 show fully analyzed scans, in the default BDAQ53 plotting style. This requires not only the ability to configure the readout chip in simulation, but also to interpret the received data and convert it to the standard BDAQ53 analyzed data format. This way the ITkPixV1 data format is confirmed to

work as intended, while verifying the new compatibility with BDAQ53, which required changes in hard- and software. From here it is concluded that the chip bottom blocks for chip command receival, trigger processing and hit data and data output introduced in Section 3.2 and described in [44], work as intended. In addition BDAQ53's compatability with all those blocks is confirmed.

CHAPTER 6

ITkPixV1.1 Characterization

ITkPixV1.1 characterization focuses on the performance measurements of the ITkPixV1.1 chip type. Therefore individual ITkPixV1.1 are tested in hardware and it is verified, that all components of this chip type perform as expected. The following Chapter will present an introduction to the setup used for characterization in Section 6.1. Section 6.2 presents a selection of measurements on the chip bottom, with Section 6.3 discussing a selection of measurements on the pixel matrix and analog front end 6.2. At the beginning of the RD53 Collaboration project the RD53 Collaboration design specifications are defined [70]. Table 6.1 lists the most relevant ones for this characterization chapter, with the following bullet list explaining the individual parameters:

- **Analog current per pixel** defines the current drawn per pixel in the analog power domain. The analog current consumption differs based on which ITk-layer, the corresponding ITkPixV1.1 will be located. The inner layers, which features higher vertex densities, allows for higher current consumption, while in the outer layers, less occupancy is expected and therefore its cooling system is dimensioned to handle less heat developed by ITkPix. The digital current defines the current drawn per pixel in the digital power domain.

- **In-time threshold** is defined in Section 4.1.3, which defines the minimum charge, detectable within one bunch crossing ID (Section 4.1.3).

- **Threshold dispersion** is the dispersion of all detection thresholds μ, measured in a threshold scan for all pixel. The dispersion can be reduced by tuning.

- **Noise occupancy** defines the number of received hits per sent triggers. In this case the maximum hit occupancy must not exceed 1 per 1 million trigger.

- **Deactivated pixels** defines the maximum number of pixels, that may be disabled during tuning.

- **Temperature range** defines, in which range RD53B needs to be able to fulfill all of the criteria in Table 6.1.

In the following, all of the performance parameters are investigated, starting with the introduction of the setup used for characterization.

Parameter	Specification
Analog current per pixel	3.0 µA, 3.5 µA, 4 µA, 5.0 µA, 5.5 µA
Digital current per pixel	<4 µA
In-time threshold	1 200 e^-
Threshold dispersion	60 e^-
Noise occupancy per pixel	$< 10^{-6}$
Deactivated pixels	< 2 %
Temperature range	−40 °C to 40 °C

Table 6.1: ITkPix specifications [70] at five different current consumptions.

6.1 Single-Chip Card Setup

The Single-Chip Card (SCC) setup is the most widely used BDAQ53 setup within the RD53 Collaboration. It consists of a BDAQ53 board as described in Section 4.1.1 and a RD53B Single-Chip Card as described in Table 4.1. Figure 6.1 shows the main connectors of the setup, as well as the cards mentioned above, in its most commonly used configuration. The most common configuration allows scans to be executed at a maximum bandwidth of 1 Gbit s^{-1}, over the 1 Gbit s^{-1} connection. In addition, the BDAQ53 board supports a 10 Gbit s^{-1} interface that allows RD53B chips to be read out at their maximum bandwidth of 5 Gbit s^{-1}. The primary data connection between the ITkPixV1 and BDAQ53 board is established using a display port cable that connects the receiver port 0-3 (RX0-3) of the BDAQ53 board to the CMD and the data port (DP1) of the Single-Chip Card. This configuration supports command- and aurora-based scans, where all data transmission is done via DP1. Other scans such as data-merging require an additional connection between the mDP port on the BDAQ53 side and DP3 on the SCC side. In addition, scan chain requires an additional connection between the GPIO DP on the BDAQ53 side and DP2 on the SCC side, as well as a few single wire connections (with a level shifter 3.3V–>VDDD) between the BDAQ53 PMOD bench and some of the pins on the SCC.

The Single-Chip Card setup is the one typically used to develop new scans, characterize chip performance and familiarize new users with the RD53B framework. One of the reasons for that is the easy access to a multitude of pin headers on the Single-Chip Card, shown on the right side of Figure 6.1. This makes measuring chip voltages and currents, as well as setting for example IREF trim bits very easy by either plugging in a multi meter, or placing a jumper at the corresponding position. For longer measurements, however, the analog monitoring board was developed. The analog monitoring board is shown in Figure 6.2.

The 2x15 pinheader row on the left of Figure 6.2 supplies the analog monitoring board with 3.3 V supply voltage, as well as an I^2C for control via BDAQ53. The rest of the pins are either used to measure currents or voltages coming from the chip or Single-Chip Card. Among the pin headers, there is also a connection to the voltage and current mux output of the chip. Further information on the RD53B mux can be found in Section 6.2.1. All these pins can be connected to the Lemo connector on the bottom right of Figure 6.2, to be measured by a single external multi meter. The active components on the analog monitoring board are responsible for configuring the mux to connect the correct input pin to the Lemo output, as well as pull configuration pins for e.g. IREF trimming, high or low. The unmounted pads on the right-hand site of Figure 6.2 are resistors, which can be wired in parallel, to e.g. the REXT shunt resistors. Please note that all measured voltages are relative to the Single-Chip

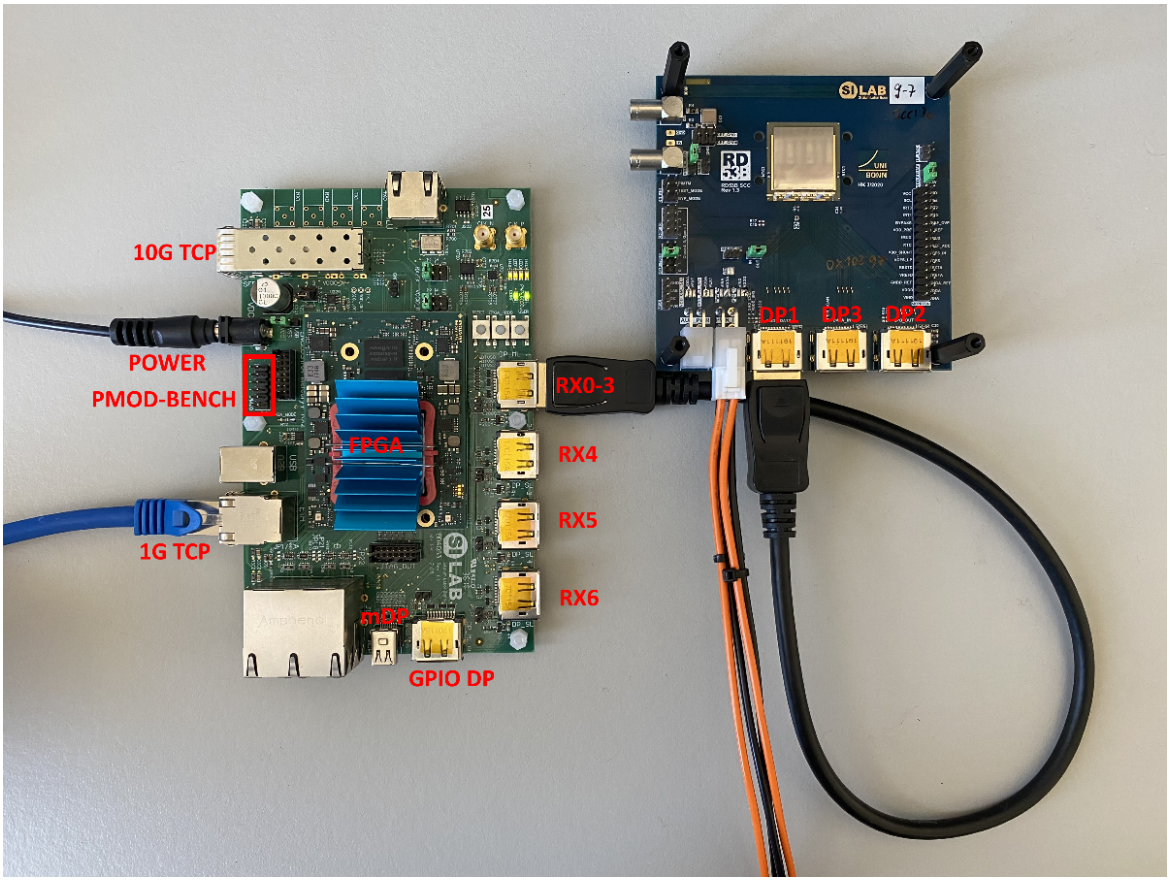


Figure 6.1: A BDAQ53 bench setup, with the BDAQ53 board on the left and an ITkPixV1 Single-Chip Card on the right.

Card and BDAQ53 board ground. The offsets between analog and digital ground on chip needs to be substracted. All in all the analog monitoring board, in combination with the Single-Chip Card and BDAQ53 board, features an efficient way to monitor RD53B voltages and currents with a single external multi meter, while varying the IREF trim and measuring analog front end performance.

6.2 Chip Bottom

The chip bottom is introduced in Section 3.2, summarizing its important blocks for ITkPixV1.1 operation. Most of the digital blocks are tested during verification in Section 5. However, many components, including analog receiver or sensor components can only be tested in hardware. Therefore two measurement campaigns are summarized in this Section; summarizing the IREF stability and temperature sensor performance of ITkPixV1.1 between −40 °C to 40 °C 6.2.1 and an unexpected feature discovered in the data-merging during characterization.

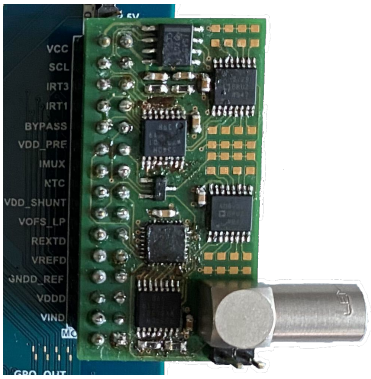


Figure 6.2: An image of the analog monitoring board while mounted on the Single-Chip Card

6.2.1 Temperature Measurements

A simple way to check how ITkPixV1.1's performance changes between −40 °C and 40 °C is by measuring all of ITkPixV1.1's reference currents, reference voltages and temperature sensors. For this purpose RD53B features a sensing and monitoring multiplexer, which allows the user to measure internal currents, voltages, temperatures or received total ionizing dose with an internal ADC or external multi meter. Figure 6.3 shows the schematic circuitry involved.

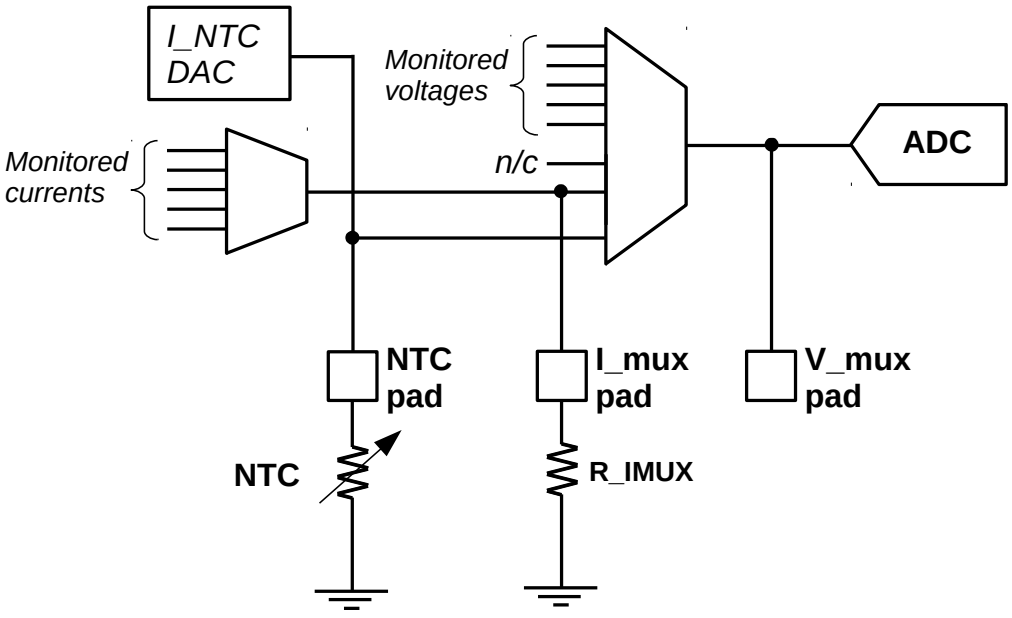


Figure 6.3: A schematic diagram of the RD53B monitoring circuit [44].

On the left of Figure 6.3 inputs into the current multiplexer are visible. The output of the multiplexer is connected to an external chip pad (I_mux pad), as well as an input of the voltage multiplexer. The

voltage multiplexer takes the input voltages and routes them to a common, selective output, which is connected to an external pad and the internal ADC. The measurable voltages and currents are documented in [44]. The ADC can only measure voltages, which, in the case of measuring currents through the current multiplexer, only works if the external resistor R_IMUX is mounted on the Single-Chip Card. RD53B features a 10 bit ADC.

In addition to internal voltages and currents, temperatures, and quantities relevant for the investigation of radiation damage can be measured using a multitude of sensors. One of them is shown in Figure 6.3. The NTC on the bottom left is a temperature-sensitive thermistor (NTC), which changes its resistance depending on temperature [71]. This resistive change can be measured by applying a known current via I_NTC DAC and measuring the voltage drop over the resistor with the internal ADC or an external multi meter.

In addition, there are two types of temperature sensors distributed in the chip bottom and top of the matrix of ITkPixV1.1 as shown in Figure 6.4.

Figure 6.4: Location of the five RD53B temperature sensors.

RD53B features two types of temperature sensors. The first type is a resistive sensor type, labeled as T & B in Figure 6.4, referring to the resistive temperature sensors on the top and bottom of the matrix. They measure the temperature based on a temperature-dependent resistor (RSENS) and a temperature-independent resistor (RREF) as Figure 6.5 shows. The temperature-dependent resistance is hereby implemented as a polysilcone resistance [44].

The resistive change between temperatures is small; therefore, the reference voltage of the ADC changes from the typical 0.9 V to VREF, which is a voltage dropping over a temperature insensitive resistor, with similar resistance as RSENS. This allows one to utilize the entire ADC range for precise temperature measurement, as shown on the right of Figure 6.5.

The second type of temperature sensors utilized in RD53B are diode-connected CMOS transistor based sensors, which change their base-emitter voltage based on temperature. Due to their larger footprint, they are solely located in the chip bottom, as shown in Figure 6.4. Diode A, D & C hereby

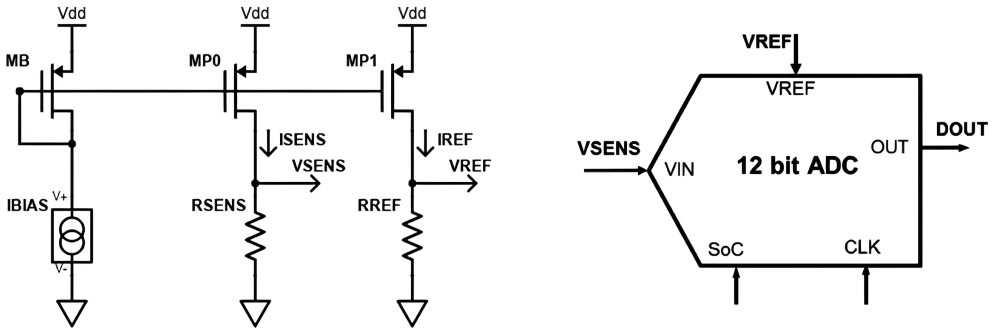


Figure 6.5: Resistive polysilicon temperature sensors schematics [44].

refer to their location at the A: analog shunt regulator, D: digital shunt regulator and C: center of the chip bottom. The temperature can be calculated based on at least two different currents, which are sent through the diode-connected CMOS transistor. The measured voltage difference is then proportional to the measured temperature according to Equation (6.1) [44].

$$\Delta V_D = V_D(R \cdot I_{bias}) - V_D(I_{bias}) = N_f \frac{k_B T}{q} \cdot ln(R) \tag{6.1}$$

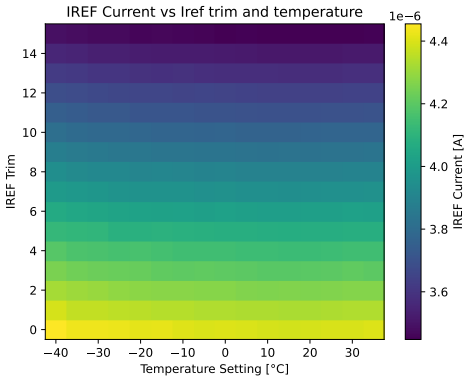
The factor N_f corresponds to the non-ideality factor of the diode-connected CMOS transistor, which is determined in this chapter. The simulated value is close to 1.24 [72]. K_b corresponds to the Boltzmann constant, T to the temperature, q to the fundamental electron charge and R is 15 in this design, due to the $15 \times I_{bias}$ multiplier. During wafer probing and chip characterization, the voltage differences for A, D & C are measured for 15 different currents, whose average voltage and ADC value are then used to calculate the temperature.

ITkPixV1 Temperature Characterization

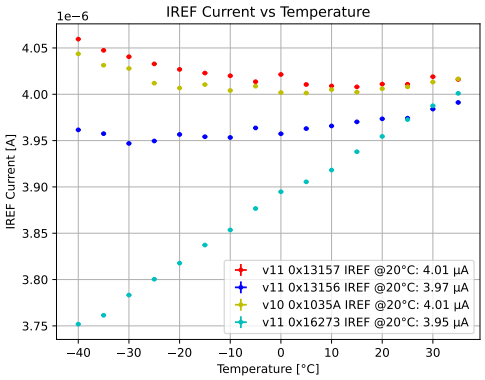
Table 6.1 defines the operating temperature range of RD53B and therefore ITkPixV1.1. It is expected that all chips, subject to the specification Table 6.1, can reliably detect hits between −40 °C and 40 °C. This assumes that all voltages and currents are constant over the defined temperature range. In addition, there are temperature sensors on ITkPixV1.1, which can be read out by the on-chip ADC, or an external multi meter, to give a reliable temperature reading of the on-chip temperature. In the following, the temperature sensor and ADC performance will be evaluated between −40 °C and 40 °C for four chips. The test is carried out using three ITkPixV1.1 and one ITkPixV1. For easy voltage and current measurement, as well as IREF trim control, the analog monitoring board, as shown in Figure 6.2 is used. The ambient temperature is varied by placing each ITkPix inside a climate chamber, while varying the temperature in 5 °C increments from −40 °C to 40 °C. At each temperature the chip is powered in direct powering mode [1], to minimize the heat developed on chip and all currents and voltages accessible on the internal mux as summarized in Table F.2 and Table F.3 are measured. In addition, the ADC is characterized by applying multiple known voltages to the ADC sequentially and reading back the measured values from the chip. The temperature sensors are read out according to

[1] VDDD & VDDA is directly supplied with 1.2 V, using sensing, without utilizing the LDO regulators

the procedure described in Section 6.2.1. To ensure a constant IREF current during all measurements over the full temperature range, all of the aforementioned parameters are measured for all 16 IREF trim bits. Figure 6.6(a) shows this measurement for ITkPixV1.1 0x13157. The x-axis shows the set ambient temperature as reported by the climate chamber, while the y-axis shows the 16 different IREF trim bit settings. The color scale indicates the measured IREF current in µA. The gradient along the y-axis is, as expected, much more dominant, since the IREF trim bit is expected to have a much larger influence on the IREF current than on the temperature.



(a) IREF current of ITkPixV1.1 module 0x13157, for different IREF trims and different temperatures



(b) IREF current of four measured chips, for different temperatures, with ideal IREF trim bit at 20 °C

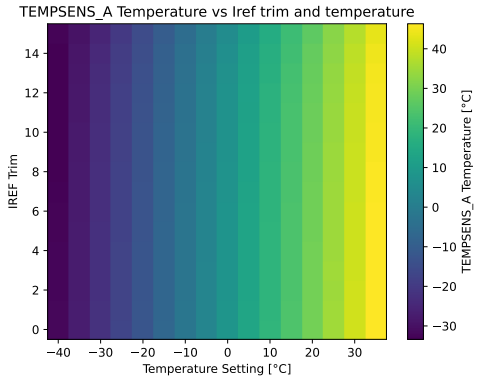
Figure 6.6: IREF plots between −40 °C to 40 °C

Figure 6.6(b) shows a cut of Figure 6.6(a) along the x-axis, picking the IREF trim value, that is closest to the nominal 4 µA at 20 °C, for all four measured chips. Three of the four measured chips exhibit little IREF variation over the measured temperature range, as expected, while one chip (0x16273) has an approximately linear IREF dependence with temperature, due to a broken core bandgap. In the following the temperature sensors of all four chips will be analyzed, while the results of ITkPixV1.1 0x16273 will be ignored, due to its suspicious IREF behavior.

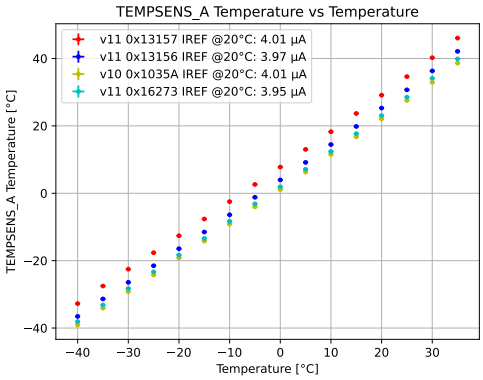
Diode Temperature Sensors

According to Equation (6.1), it is sufficient to measure the voltage difference at different bias currents of the diode-connected CMOS transistors to estimate their temperature. This voltage difference is measured with the external multi meter and with the RD53B internal ADC. Figure 6.7 shows the temperature measured using the external multi meter.

Figure 6.7(a) exhibits a strong gradient along the x-axis, which is expected for a temperature sensor. There is no observable gradient along the y-axis, which proves the diode sensor's independence of the supplied IREF current. Another proof for this is the nice behavior of the temperature sensor of ITkPixV1.1 0x16273, which showed suspicious IREF behavior in Figure 6.6(b). However, in Figure 6.7(b) the temperature sensor behavior is within the expected margin of error. From here it can be deduced that the diode temperature sensors are well suited to estimate the relative on-chip temperature between −40 °C and 40 °C using an external multi meter. Please note that all of the above calculations are done using the simulated non-ideality factor N_f of 1.24 [44]. The best temperature reference



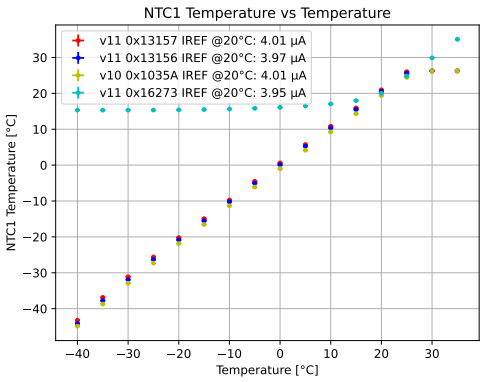
(a) Temperature sensor A temperature of ITkPixV1.1 module 0x13157, for different IREF trims and different temperatures



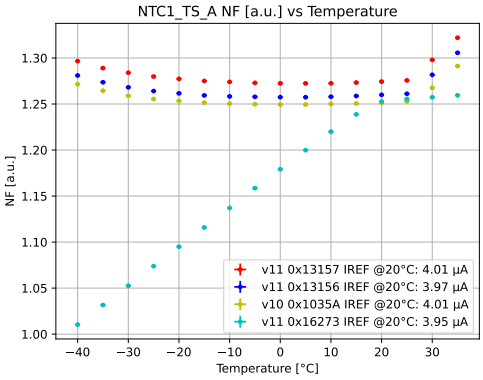
(b) Temperature sensor A temperature of four measured chips, for different temperatures, with ideal IREF trim bit at 20 °C

Figure 6.7: Temperature sensor A temperature plots between −40 °C and 40 °C

accessible on the ITkPixV1.1 Single-Chip Card is a NTC right and left next to the chip. The NTCs are also visible in Figure 3.1. These NTCs are measured in addition to the chip parameters. Figure 6.8(a) shows the temperature measured by NTC on the right of the chip on the Single-Chip Card. Please note that the NTC measurement in cyan is not successful at temperatures below 20 °C. For the following calibration its values will be excluded, as well as the values on the top left for temperatures larger than or equal to 30 °C. The linear behavior between measured and set temperature is expected, in addition, an offset can be observed, where the measured NTC temperature is, for lower temperatures, systematically lower than indicated by the climate chamber.



(a) Temperature measured by the NTC to the right of the chip



(b) Calculated N_F factor using NTC temperature data shown in Figure 6.8(a) and voltage data shown in Figure 6.7(b)

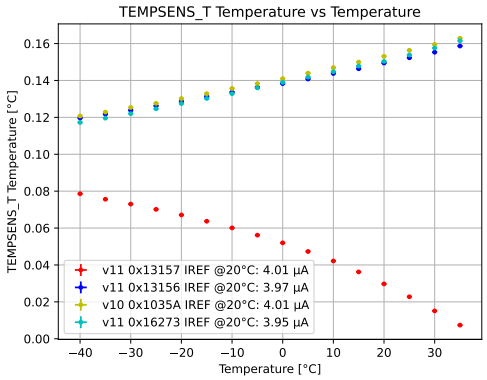
Figure 6.8: Non ideality factor N_f for Temperature sensor A in the range −40 °C to 40 °C

For the ITk production the goal is to calibrate each individual ITkPix and find its ideal N_f factor during wafer probing. Figure 6.8(b) shows the calculated N_f factors using the measured NTC

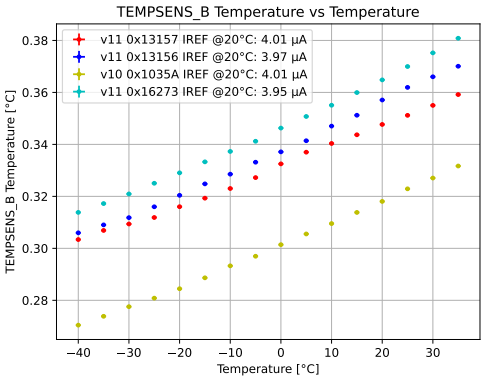
temperature and diode sensor voltage data. It is visible that the N_f factor is non-constant over the full temperature range, and fluctuates even more for a single chip over the full range than for all measured chips at 20 °C. The mean N_f over the full temperature range is **1.269 ± 0.021**, while the mean N_f between measured chips at 20 °C is **1.259 ± 0.009**. Please note, that the inter-chip spread is half of the N_f spread between the four measured chips. It is therefore questionable, whether a per-chip calibration yields more accurate temperature result, than using one N_f factor for all diode temperature sensors. In addition, the systematic error between chip and NTC is difficult to estimate, since the temperature in silicon cannot be measured. Even an infrared camera yielded no better measurement, due to infra-red reflection of the chips metal layers . Further analysis on the temperature sensors is conducted in Chapter 7.2.7, with Figure 7.15 showing little correlation between NTC temperature and measured delta voltage on diode sensor c during wafer probing.

Resistive Temperature Sensors

The resistive temperature sensors are designed to measure the relative temperature between the top of the chip and chip bottom. For his purpose those sensors consist of two resistors each, one with a resistance of roughly 10 kΩ at room temperature and the other non-temperature-dependent resistor with a resistance of 16 kΩ. They are both biased with 32 µA. Therefore a voltage drop of 0.32 V is expected at room temperature. Figure 6.9 shows the measured voltage drops over the two polysilicon temperature sensors measured with an external multi meter.



(a) Measured voltage drop over top polysilicon temperature sensor



(b) Measured voltage drop over bottom polysilicon temperature sensor

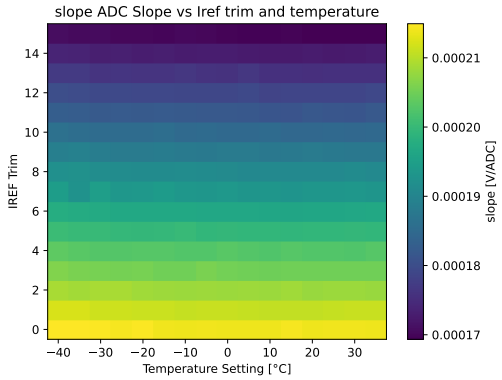
Figure 6.9: Measured voltage drops of polysilicon temperature sensors. Expected Value: 0.32 V

Figure 6.9(a) shows the voltage drop measured over the top polysilicon sensor with a bias of 32 µA. Three of the four chips have a consistent slope, but feature less than half the expected voltage drop of 0.32 V at room temperature. This is most likely related to an error in the polysilicon implantation of the temperature sensor. This lower slope is also observed during wafer probing in Section F.2.35. ITkPixV1.1 0x13157 has a known faulty top temperature sensor, proably due to insufficient doping in the sensor. In general, the top temperature sensors can still be used, with reduced accuracy. However, since the ADC reference is 0.512 V only a quarter of the ADC range can be used. Figure 6.9(b) shows the same measurement for the bottom polysilicon temperature sensor. All four chips feature

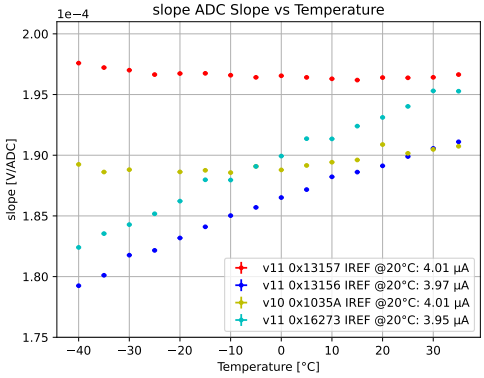
a similar slope, in the expected 0.32 V range, with different offsets. Here, a per-chip calibration at room temperature makes sense, to measure the offset for each chip individually. All in all the bottom polysilicon temperature sensor works as expected with the necessity to calibrate the offset on a per-chip base. Further measurements on the behavior of this sensor can be found in the wafer probing Section F.2.36.

ADC vs. Temperature

The ADC is a core element to measure on-chip voltages, currents and temperatures during ITk operation. On the module level it is tough to externally access chip voltages once the ITk is assembled. For reliable chip monitoring the functionality of the ADC is therefore critical. During each temperature step, the ADC slope and offset is measured for each individual IREF trim bit. Figure 6.10(a) shows the 2D-plot for chip 0x13157.



(a) Measured ADC slope for different IREF trim bits and different temperatures

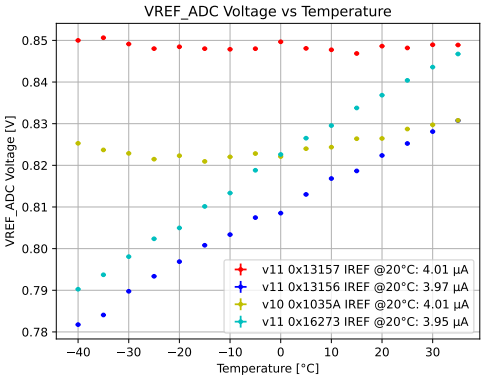


(b) Measured ADC slope for four chips with IREF closest to 4 µA at20 °C and different temperatures

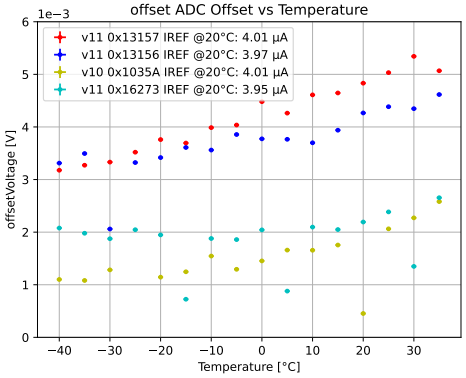
Figure 6.10: ADC slope analysis between −40 °C to 40 °C

It shows a strong dependence on IREF trim, which is expected, since IREF changes the ADC reference voltage, which changes the slope. However an additional temperature dependence is observed in Figure 6.10(b), especially for chip 0x16273, which already showed a strong temperature IREF dependence in Figure 6.6(b), and chip 0x13156, which behaved as expected in Figure 6.6(b). This could for example be related to a temperature dependence of the current mirrors supplying the ADC. All in all the measured chips can be clustered in two groups. One which features low temperature dependence on the ADC slope, and a second group, which exhibits a significantly increased temperature dependence on its ADC slope. Figure 6.11(a) shows this observation to be consistent with the ADC reference current changing in the same way as the slopes. This behavior is expected, since the ADC always measures 4095 steps between analog ground and ADC reference voltage. Therefore, if the ADC reference voltage changes, the step width and slope automatically changes.

In addition to a change in the ADC slope and ADC reference voltage, a change in the ADC offset is measured, as shown in Figure 6.11(b). The change over the full temperature range per chip corresponds to up to 10 LSB. This can be explained by a change in the analog ground potential for different temperatures, which could be triggered by a change in current consumption.



(a) Measured ADC reference voltage for different temperatures



(b) Measured ADC offset for four chips with IREF closest to 4 µA at 20 °C and different temperatures (expected: 0.845 V

Figure 6.11: ADC reference voltage and offset analysis between −40 °C and 40 °C

Conclusion Temperature Measurements

All in all, the diode temperature sensors work as expected and yield little N_f variation between chips at 20 °C. The bottom polysilicon sensor works as expected and requires no calibration for relative temperature measurement and per-chip calibration for absolute temperature measurement, if desired. The ADC behaves well in 50 % of tested chips over the full temperature range. However in two chips, one explained by IREF variation, one explainable by current mirror variation, the ADC reference voltage fluctuates by ≈6 %. Figure 6.12 shows the temperature measurement error introduced by the ADC if slope and offset at 20 °C are taken as basis for all ADC temperature measurements.

A large temperature deviation of >10 °C can be introduced by the ADC voltage measurement over the full temperature range, as ITkPixV1.1 0x13156 and 0x16273 show. In the other two cases the temperature deviation between ADC and multi meter measurement is ± 2.5 °C. From the measurements shown in this Section it is clear, that all measurements involving the ADC should be conducted at their corresponding temperature, due to the indistinguishability of chips with stable ADC reference voltage at room temperature.

6.2.2 Data-Merging Test

A second key component, which is investigated in the ITkPixV1.1 chip bottom, is the data-merging-block. Data merging is a feature foreseen to reduce cabling inside of ITk. For this purpose some chips forward their data to a neighboring RD53B chip. The neighboring chip then merges the data from the first chip with its own data. This feature is used especially in regions of ITk, where only a fraction of a chip's bandwidth is needed. Figure 6.13 shows the idea behind the reduction of data links. Both images resemble a module with four ITkPixV1.1. On the left the read out is shown without data merging, where each chip sends out its data on a dedicated 1x1.28 Gbit s^{-1} lane. The right Figure shows a module with data-merging, where chips 1-3 forward their data to chip 0, which only requires one cable through the detector.

This is one of the key features enabling the ATLAS ITk detector to be built with so many read out

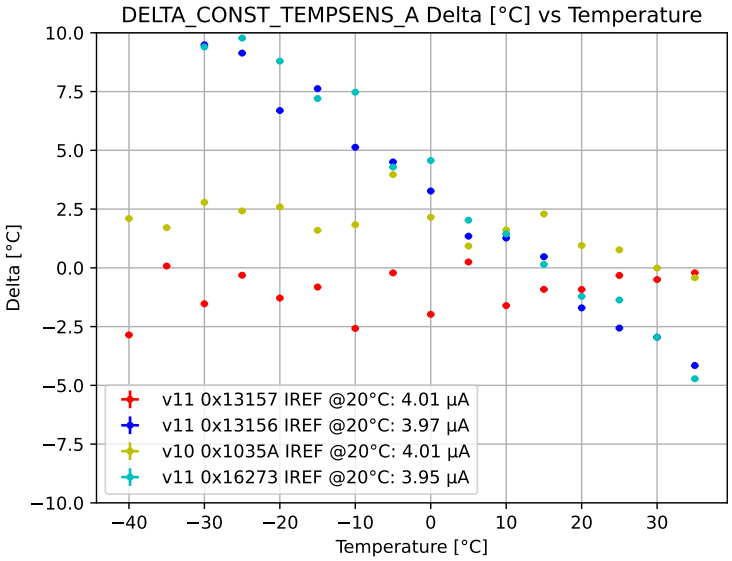


Figure 6.12: Temperature difference between measurements taken by ADC and external multi meter

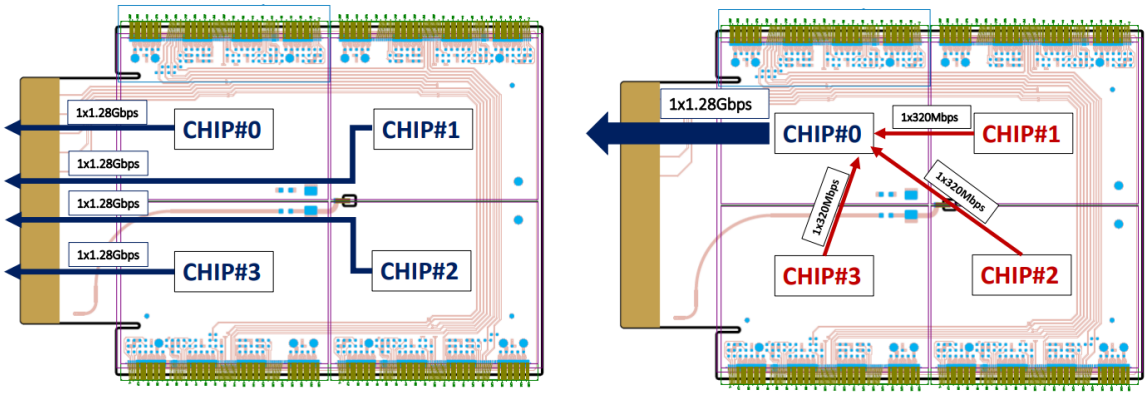


Figure 6.13: On the left a digital module with parallel read out lanes for each chip at full bandwidth. On the right the same module with merged data at a quarter of each module's bandwidth [73]

channels. Before and during wafer probing[2] this feature is tested. ITkPixV1.1 derives all its internal clocks from the supplied command data stream of 160 MHz. This means, all other modules are phase-locked with this input after initialization. One of these phase-locked modules is the data-merging module, which resamples the incoming data from all of the secondary chips. The incoming data is not phase-locked, due to e.g. different cable/trace lengths. This is expected and also accounted for inside the data-merging logic block, by resampling the incoming data with four clocks each shifted by 90°. The data-merging module should then pick the best sampling clock for every delay.

To test this, a dedicated data-merging module is implemented in BDAQ53. The mini Display Port is used to transmit simulated ITkPix data to the data-merging input of the primary chip, with adjustable

[2] Section F.1.7

payload, delay and headers. Figure 6.14 shows the number of successfully recovered merged data frames form the primary data stream as a function of phase shift between the command data and data merging data at the FPGA output for all four different aurora lanes. All four aurora lanes are routed differently internally, leading to a difference in signal travel time between them. This difference in signal travel time is measured as a phaseshift in Figure 6.14. The x-axis shows the variation of signal delay, which is introduced in 27 ps steps. The y-axis shows the number of successfully received data sent from BDAQ53 to ITkPixV1.1 back to the BDAQ53board. Each color represents one of four different aurora input lanes of the primary chip. In this measurement data is sent ten times. It is visible, that each lane features three to four dips in each measurement window. The data is transmitted at 320 MHz resulting in a repeating pattern every 3 125 ps. Therefore the first dip in Figure 6.14 is equivalent to the last dip in the same Figure. Each plot features two different dip widths, one 168 ps wide, for example the first and third dip in Figure 6.14. The second dip width is 307 ps and corresponds to e.g. the second dip in Figure 6.14. This is related to two different failure modes in the data-merging logic. The data-merging logic samples the incoming data stream with four clocks, each shifted by 90°. The logic then picks the correct clock to sample the data with. On the falling flanks to the dips, observed in Figure 6.14, the clock picked by the logic is ambiguous, while in the dips it is incorrect. This is related to a bug inside the chip, which is understood and expected to be fixed in ITkPixV2.

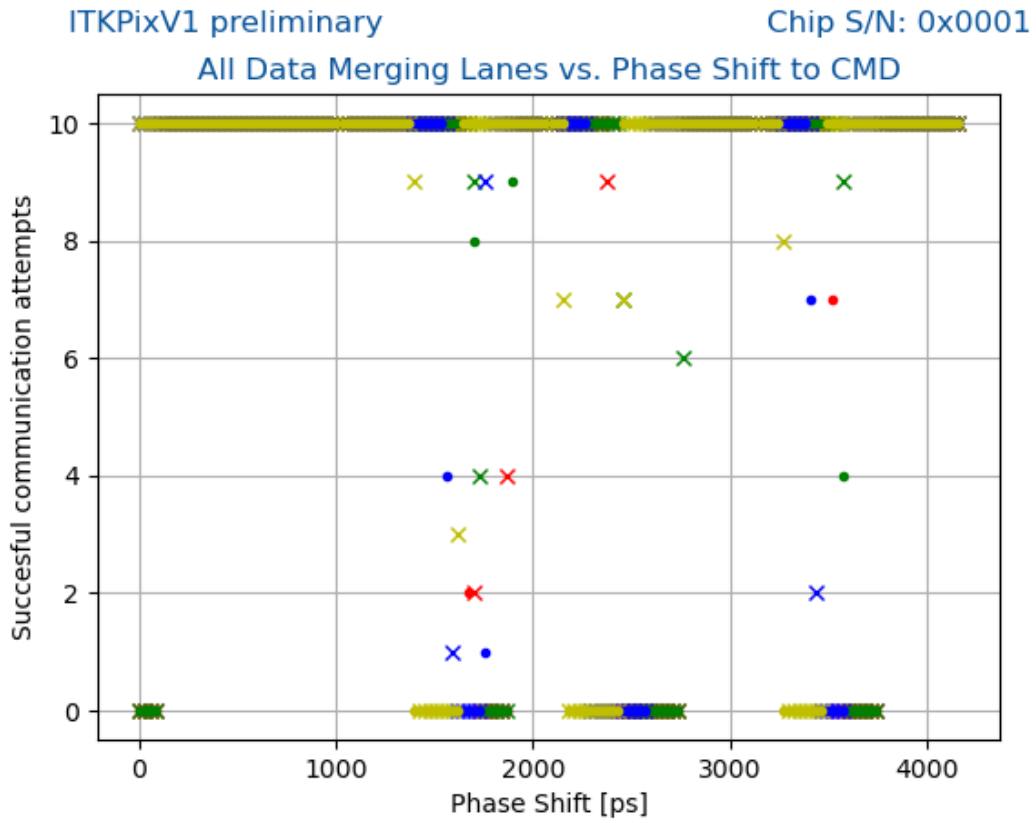


Figure 6.14: Data merging successfully recorded packages vs. phase delay

To use ITkPixV1 and ITkPixV1.1 to their full testing potential, a way to change the phase relation between primary and secondary ITkPixV1.1 needs to be found.

Therefore a data-merging testing setup, shown in Figure 6.15 is assembled. On the left, the computer is visible, which controls the BDAQ53 board, as well as a power supply and an oscilloscope for data taking. The oscilloscope can measure two signals, one marked with the turquoise star, which is the data coming from the secondary chip, the other marked with a yellow triangle is the data coming form the secondary chip, resampled by the primary chip. The oscilloscope is automatically triggered and transfers its raw data to the computer. The BDAQ53 board controls the two ITkPixV1.1 chips. The receiver of the primary ITkPixV1.1 is connected directly to the BDAQ53 board, while the secondary ITkPixV1.1 receives the command directly from BDAQ53, but sends its data to the primary chip. The aurora lane output is sent to the primary ITkPixV1.1s data-merging input. The data received from the primary can be observed on display port two, hosting RD53B's general purpose LVDS outputs. For best observability, the aurora lane output of the secondary ITkPixV1.1 is set to be a 320 MHz clock.

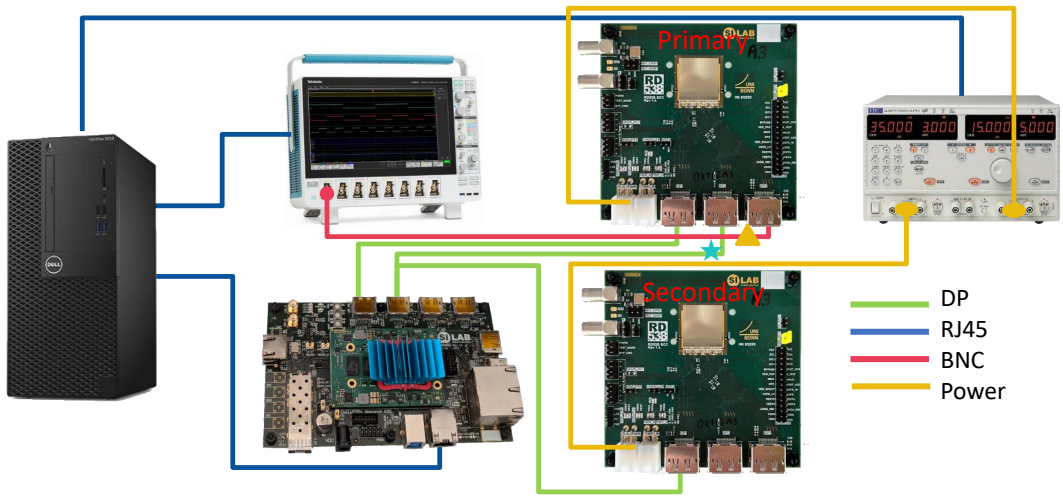
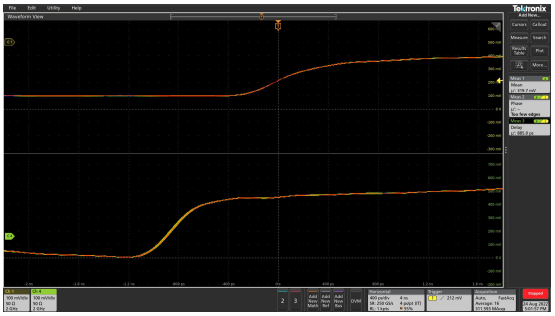


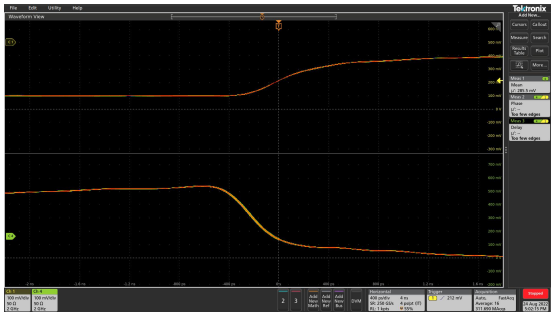
Figure 6.15: Data Merging Setup with two ITkPixV1.1 and an oscilloscope for data taking. The blue star (data-merging input) and Triangle (data-merging data as received by the primary) indicate the two measurement points

During the testing of the test setup described in Figure 6.15 another data-merging feature is discovered and summarized in Figure 6.16. The upper waveform in Figure 6.16 is the input command with a data rate of 160 MHz coming directly from the BDAQ53 board, while the bottom shows the resampled 320 MHz data merging clock of the primary ITkPixV1.1. This waveform is taken behind display port two, as indicated by the yellow triangle in Figure 6.15. The left and right image are measured at two different, random boot-up scenarios. A phase flip of the lower 320 MHz clock after initialization can be observed. It may be noted, that these phase flips can randomly occur in two states. This phase shift is related to a second clock divider inside the data-merging logic block, which generates its own 160 MHz clock. Therefore the dips measured in Figure 6.14 may occur with a phase

shift of 180°.



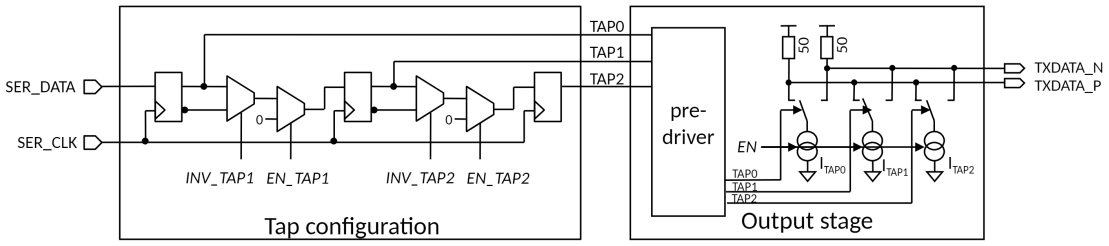
(a) Top: 160 MHz BDAQ53 command clock Bottom: Resampled 320 MHz data-merging clock



(b) Same measurement as in Figure 6.16(a), shifted by 180°)

Figure 6.16: Random phase flip occuring after initialization of ITkPixV1.1, in relation to input the input command.

Coming back to the idea of changing the phase relation between primary and secondary ITkPixV1.1. One of the ideas to influence the phase delay of the received data-merging stream is to change the pre-emphasis of the secondary ITkPixV1.1. Pre-emphasis is the oversteering of a fast signal, to compensate for the finite rise times of a real transistor. Figure 6.17 shows the command line driver of RD53B. The bottom right shows two constant current sources, labeled I_{TAP1} and I_{TAP2}. Their default current output is zero. One way to change the phase relation between the data received inside the primary chips data-merging block is to introduce a direct current offset to the data sent by the secondary ITkPixV1.1. This can be done by flipping the switch of I_{TAP2} by setting the registers on the left accordingly and then raising the currents on I_{TAP1} and I_{TAP2} in equal steps (in the following I_{TAP} curents).

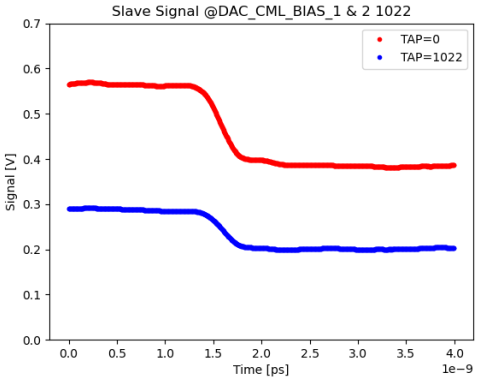


TAP configuration
- *INV_TAP[2:1]*
- *EN_TAP[2:1]*

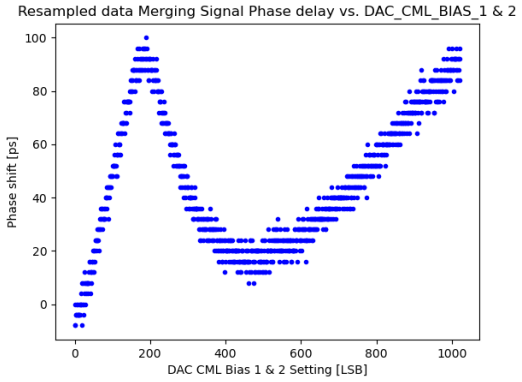
CML output configuration
- *EN*
- *TAP0_BIAS[9:0]*
- *TAP1_BIAS[9:0]*
- *TAP2_BIAS[9:0]*

Figure 6.17: The command line driver of RD53B [44]

Figure 6.18(a) shows the minimum I_{TAP} currents in red and maximum I_{TAP} currents in blue. The change in offset is clearly visible, as well as a compression of the signal amplitude . Figure 6.18(b) shows the changing I_{TAP} current values in units of the used DAC on the x-axis, while the y-axis shows the delay in picoseconds in relation to I_{TAP} current DACs zero. A linear increase from 0 ps to 100 ps



(a) Secondary ITkPixV1.1 output signal for minimum (red) and maximum (blue) I_{TAP} currents



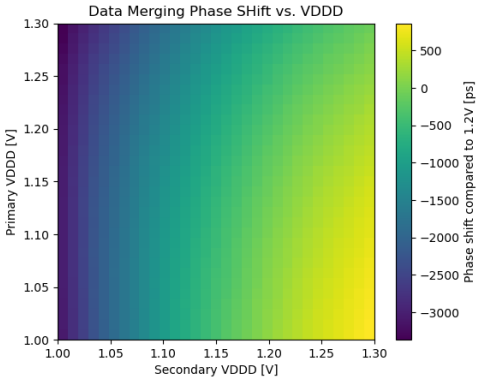
(b) Received clock delay by the secondary chip, as measured by the oscilloscope at the yellow triangle position indicated in Figure 6.15

Figure 6.18: Impact of I_{TAP} currents on signals measured at the primary input and primary output (star/triangle in Figure 6.15)

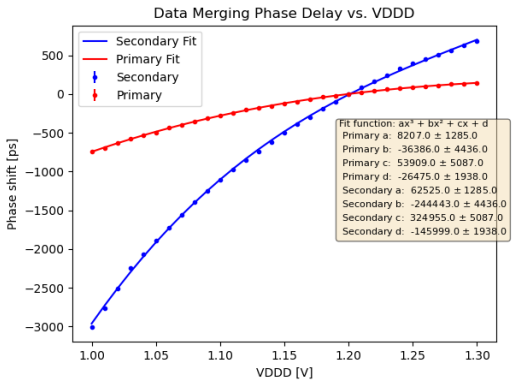
in delay is clearly visible, from I_{TAP} currents delay zero to 200, followed by a dip at I_{TAP} current DAC value 500, which then rises to a delay of 100 ps. As described before, there are two effects of the increase of the I_{TAP} current. First an offset of the signal, second a compression of high and low levels, in the region zero I_{TAP} current DACs to 200 I_{TAP} current DACs the offset effect seems to be dominant, while in the region above the signal compression effect seems to introduce a negative delay until I_{TAP} current DACs 500. All in all the I_{TAP} currents can be used to introduce a phase delay of up to 100 ps between primary and secondary chip, while influencing the signal shape. Since Figure 6.14 shows wider dips than 100 ps another way to introduce a controlable phase delay is investigated.

One tested solution is the change of VDDD, which is the digital supply voltage for all digital components in the chip. A lower VDDD influences the speed of all transistors in the chip, which naturally introduces a delay. This effect is measured in Figure 6.19.

Figure 6.19(a) shows a 2D plot, to investigate the variation of the phase shift between primary and secondary chip between 1.0 V and 1.3 V. The z-axis of the plot is normalized to the delay between primary and secondary at VDDD 1.2 V for both chips. A gradient from top left to bottom right is observed, which signals an influence of both chips on the data-merging phase delay. The horizontal gradient from l is more pronounced than the vertical one, which indicates a stronger dependence on the secondary chip VDDD. The influence of varying VDDD for one chip, and keeping VDDD of the second chip constant at 1.2 V can be observed in Figure 6.19(b). Also here the steeper gradient of the secondary chip is visible, confirming the observation of the steeper gradient in Figure 6.19(a). The data merging delay can be varied by more than a full phase of 3.125 ns by varying VDDD between 1.0 V and 1.3 V, as indicated by the blue dots. The blue line indicates the result of a third-order polynomial fit, whose parameter are shown in the plot. In contrast the data merging delay can only be varied by less than 1 ns by varying VDDD of the primary chip between 1.0 V and 1.3 V, as indicated by the red dots. The red line again corresponds to a third-order polynomial fit, whose parameters are shown in the plot. In general the variation of VDDD can introduce unknown failure modes, which is why the variation of this parameter should be kept as low as possible. In conclusion it is possible to



(a) A 2D plot, showing the phase delay between primary and secondary, measured at the yellow triangle position in Figure 6.15.



(b) A cut of Figure 6.19(a), in red at constant secondary VDDD, in blue constant primary VDDD, of 1.2 V

Figure 6.19: An investigation of the influence of VDDD on data-merging phase delay.

shift the phase delay between primary and secondary by varying VDDD. To circumvent the unexpected feature as explained in the beginning of this section. All in all the chip bottom and most of its logic blocks perform as expected. The most important components like command encoding, bias generation and shunt regulators work very well. The bugs documented in this Section 6.2 are expected to be fixed in the next chip iteration ITkPixV2.

6.3 Pixel Matrix

Next to the chip bottom also a few parameters in the pixel matrix are characterized. The pixel matrix is introduced in Section 3.1, summarizing its built up and important blocks. Most of the digital pixel matrix blocks are tested during verification in Section 5.2.4. However the analog front end can only be tested in hardware. Therefore two measurement campaigns are summarized in this Section comparing the analog front end performance of an ITkPixV1.1 module with 3D-Sensor [74] at −40 °C with the RD53 Collaboration design specifications [70] in Section 6.3.1. Additionally a measurement to investigate the time dependence of the detection threshold is discussed in Section 6.3.2.

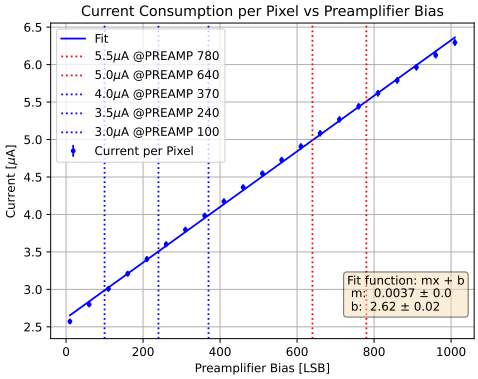
6.3.1 ITkPixV1 Analog Front-End Characterization

The analog front end converts the induced charge from the sensor to a digital signal, as discussed in Section 3.1.1. In this Section, the injected test charges are generated by the calibration injection circuit [44]. The calibration injection circuit charges the injection capacitance ("Injection" in Figure 3.3), to vcal high, then quickly flips to vcal med, injecting a well-known charge into the analog front end, according to Equation (6.2):

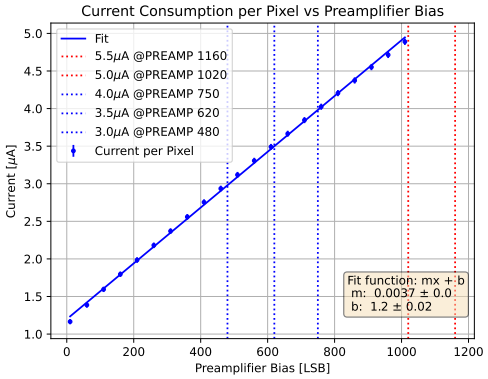
$$Q = C \cdot U \tag{6.2}$$

Where U is the voltage difference between vcal high and vcal med and Q is the injection capacitance, which is characterized in Section 7.2.5. The calibration injection circuit is used to measure the detection threshold of each individual pixel, by running a threshold scan as explained in Section 4.1.3.

Previous to the threshold scan, the chip is cooled to −40 °C ambient temperature in a climate chamber, to get close to the conditions in the detector. Figure 6.20 shows the analog current consumption per pixel for different preamplifier bias settings, introduced in Section 3.1.1.



(a) The analog front end current consumption of chip 0x13157, for different analog front end preamplifier bias settings and trimmed IREF.



(b) The analog front end current consumption of chip 0x13156, for different analog front end preamplifier bias settings and trimmed IREF.

Figure 6.20: The analog front end current consumption for different analog front end preamplifier bias settings. The vertical lines indicate current settings acceptable for the inner layer in red and acceptable for the outer layer in blue.

Figure 6.20(a) shows the current consumption for chip 0x13157, with a biased 3D-Sensor at −40 °C. The linear relation between preamplifier bias setting and current consumption is clearly observable. Information about the fit parameters can be found in the bottom right corner. The same information can be found in Figure 6.20(b), which shows the current consumption for chip 0x13156, with a biased 3D-Sensor at −40 °C. The slope of the two fits is as expected. However, the offset is significantly different between the two chips. The higher offset in 0x13157 seems to be a chip feature, which is solely observable in 0x13157, after testing three other chips. In addition, a misconfiguration can be excluded, since a higher current of 180 mA is observed right after power-up before configuration. According to simulation, chip 0x13156 behaves as expected, since the analog current consumption after power-up is around 100 mA and the preamplifier bias changes the current consumption per pixel between 0 µA and 4 µA, after the offset is substracted [75]. The ITk will consist of five layers of ITkPix modules, which allow for different current consumptions per pixel. The outer layers allow 3 µA to 4 µA per pixel, while the inner layers allow for 4 µA to 5.5 µA. The red vertical lines in Figure 6.20 indicate the inner layer power settings, while the blue vertical lines indicate the power settings of the outer layers. The preamplifier bias can be trimmed with a 10 bit register, which offers an operational range of 0-1000 LSB. As expected, chip 0x13156 never reaches 5.5 µA offering some headroom for other registers during operation and increasing irradiation damage[3]. As can be seen in the legends of Figure 6.20(a) the preamplifier setting for chip 0x13157 is 280 LSB lower than for 0x13156, due to the current consumption offset during powerup. In the following the in-time threshold, threshold-dispersion and noise-occupancy per pixel of the chips 0x13156 and 0x13157 will be tested at the five power settings indicated in Figure 6.20. In this procedure, both chips are

[3] visible by the red vertical 5.5 µA line being outside the range of 0-1023 in Figure 6.20(b)

cooled down to −40 °C, their IREF is trimmed to 4 µA and their current consumption is measured. This procedure is followed by multiple threshold tuning and noise scan procedures, tuning each chip from 3 000 e^- to 1 000 e^-, with a noise occupancy of $< 10^{-6}$. Based on the following results, it can be determined whether ITkPixV1.1 fulfills the specifications defined in 6.1 and whether changes to the chip or during wafer probing are necessary.

Table 6.2 summarizes the in-time-threshold, threshold dispersion and percentile of deactivated pixels of the two chips, whose current consumption was measured in Figure 6.20 at one of the five current settings introduced in the specification Table 6.1. The cell colors refer to whether a chip fulfills the specifications defined in Table 6.1, where green indicates a met specification, while red indicates a non met specification. For the three measured parameters met is defined as:

- **In-time-threshold** If the measured in-time-threshold is <1 200 e^-, the specification is met.
- **Threshold dispersion** If the measured threshold dispersion is <60 e^-, the specification is met.
- **Deactivated pixel** If the percentile of deactivated pixel is <2 %, the specification is met.

Current	Chip	Bias	In-Time-Threshold	Threshold-Dispersion	Deactivated Pixel
3.0 µA	0x13157	100	1 450 e^-	62 e^-	16.34 %
3.0 µA	0x13156	480	1 011 e^-	47 e^-	0.77 %
3.5 µA	0x13157	240	1 103 e^-	56 e^-	2.87 %
3.5 µA	0x13156	620	1 006 e^-	47 e^-	0.56 %
4.0 µA	0x13157	370	1 043 e^-	55 e^-	1.68 %
4.0 µA	0x13156	750	998 e^-	48 e^-	0.48 %
5.0 µA	0x13157	640	1 016 e^-	53 e^-	0.91 %
5.0 µA	0x13156	1020	994 e^-	51 e^-	0.40 %
5.5 µA	0x13157	780	1 011 e^-	53 e^-	0.75 %
5.5 µA	0x13156	1160	No Data	No Data	No Data

Table 6.2: In-time-threshold, threshold-dispersion and fraction of deactivated pixels at a noise level of $< 10^{-6}$, for two chips at different power settings. Green means it fulfills the specifications, red means, it does not fulfill the specifications.

It is noticeable, that chip 0x13157 only fulfills the specifications, when consuming 4.0 µA or more. However 0x13156 fulfills the requirements at all five power settings. The 4.0 µA row of chip 0x13156 additionally suggests an in-time-threshold below the 1 000 e^- tuning target. In this case, 0x13156 achieved a threshold tuning result of 995 e^-. The same applies to the 5.0 µA setting of 0x13156. Figure 6.20 suggests that the slower performance of 0x13157 can be mostly attributed to its analog current consumption offset, since the effective current available for the analog front end is the same per LSB for both 0x13156 and 0x13157, as wafer probing data shows. The last row of 0x13156 with the 5.5 µA setting cannot be reached, since the preamplifier bias DAC has an operating range of 0-1023 LSB. The increase in in-time threshold, threshold dispersion and deactivated pixels, for decreasing preamplifier bias currents is expected, since the preamplifier bias current is the main amplification bias. Lower amplification results in a slower, more noisy analog front end, therefore higher in-time threshold, with more noisy pixels and larger threshold dispersion is expected. All in all it can be concluded, that the analog front end fulfills the RD53 specification [70] for a preamplifier bias setting larger than

≈300, as measured in Reference [76] and interpolated from Table 6.2. An additional quality control measurement during wafer probing is recommended, which measures the initial current consumption of each chip without configuration, to reject faulty chips, such as 0x13157, early and prevent future problems on module level concerning chips with excessive current consumption.

6.3.2 Oscillating Threshold

During ITkPixV1.1 tuning and testing, a pattern in the ITkPixV1.1 noise scan is discovered. A noise scan is a scan, that enables the whole pixel matrix at once, sets the threshold voltages to a low setting, which sets a few hundred analog front ends into a noisy state, meaning that the electronic noise is detected by the analog front end and from time to time produces a noise hit. These noise hits are completely random in a spatial and time domain. So in essence a noise scan is expected to yield a random spatial hit distribution over the pixel matrix, with some pixels being noisier than others, as well as a flat time distribution, if sampled over longer times. In the default BDAQ53 case, a time window of $32 \cdot 25$ ns is triggered. The resulting bunch crossing ID distribution is shown in Figure 6.21.

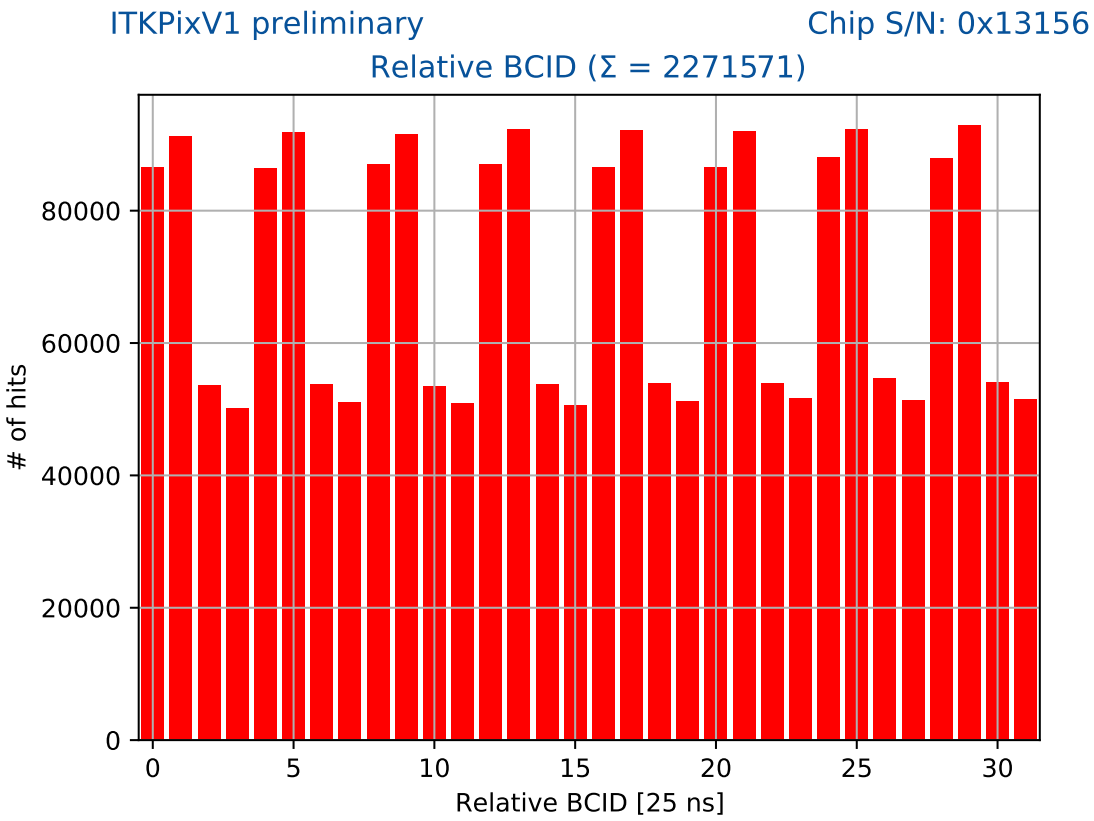


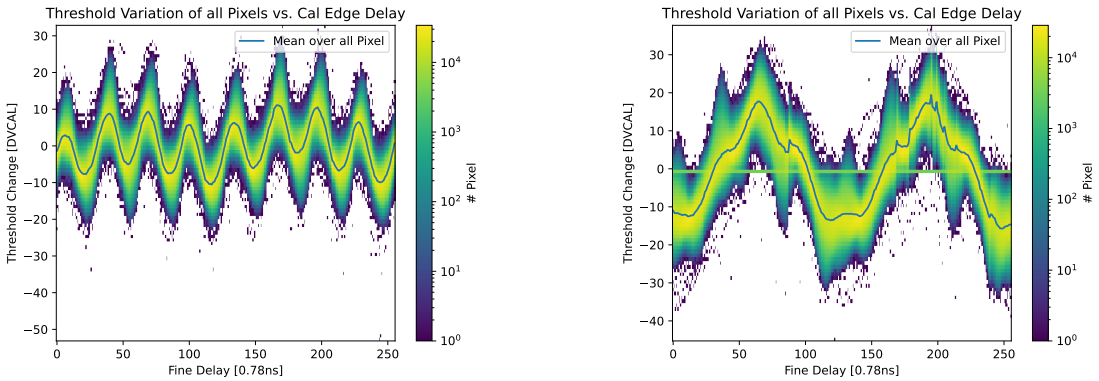
Figure 6.21: Suspicious, periodic noise distribution over multiple bunch crossing IDs. A flat histogram would be expected.

Figure 6.21 shows a periodic pattern in the number of detected hits per bunch crossing ID. The pattern exhibits a periodicity over four triggers. The first two triggers in the 4-trigger sequence detect

roughly twice as many hits, as the third and fourth trigger. The reason for that is investigated in the following. The initial observation suggests a variation of the detection threshold over time with a 10 MHz frequency. In RD53B there are many clock domains running at 40 MHz, but only individual counter bits in the pixel matrix running at 10 MHz. Therefore an early suspect of the origin of this 10 MHz coupling is the bunch crossing ID distribution network, which has multiple lanes running through the pixel matrix. One set of lanes distributes the current bunch crossing ID counter through the matrix, while another set of lanes distributes a trailing bunch crossing ID counter, which deletes detected hits, after the trailing bunch crossing ID counter equals the bunch crossing ID count, at which the hit was detected. To ensure that the bunch crossing ID counters have a fixed relation with the injection signal, the injection command in this test is structured as follows:

- **BCID reset:** Writing a bcid reset, to set the bcid counter to zero prior to each injection
- **Sync commands:** A variable number of sync commands is sent, to vary the timing between bunch crossing ID reset and injection command in 10 MHz steps.
- **Injection:** An analog injection command (cal command) is sent, with variable timing of 160 MHz.
- **Sync commands:** A fixed number of sync commands is sent to bridge the time between injection and trigger.
- **Trigger:** A trigger is sent, to request all detected hits, generated by the injection command.

The above list suggests, that the finest injection timing variation is possible with 160 MHz resolution. However there is another setting, which is globally configured with a register, which varies the injection commands with an additional 1 280 MHz, called "Fine Delay". Thanks to the combination of the three timing variation techniques, it is possible to measure the threshold variation for multiple µs with a resolution of 1 280 MHz.



(a) Overlayed threshold oscillation for all pixels of bare chip 0x16253 with double isolation

(b) Overlayed threshold oscillation for all pixels of chip 0x13156 with single isolation and biased sensor

Figure 6.22: Measured Threshold Oscillations for two different chips

Figures 6.22 on the x-axis shows the time difference between bunch crossing ID reset and cal command in Fine Delay steps of 0.78 ns. The y-axis shows the threshold variation of each individual

pixel normalized by its mean detection threshold measured over the full time window. The blue line is the averaged detection threshold variation over all pixels, the blue to yellow colors indicate how many pixels feature an oscillation with the corresponding amplitude. Figure 6.22(a) shows a clear 40 MHz component, with an underlying 10 MHz component, at an amplitude of -20 to +25 delta vcal. This ITkPixV1.1 is a bare chip, without a sensor and double isolated analog front ends. Figure 6.22(b) shows the same plot for a ITkPixV1.1 with single isolation and biased sensor. It exhibits a much stronger 10 MHz oscillation, at an amplitude of -25 to +30 delta vcal. The horizontal line in the plot is visible due to nonfunctional pixels, which do not exhibit any oscillation, due to e.g. failed S-curve measurements. In addition, there are glitches visible, especially in the second period of the curve, which is related to different runs. The splitting of data into runs is necessary to take data over multiple days. The left plot is acquired in one run. The next goal is to figure out, which other frequencies couple with ITkPixV1.1's detection threshold. Therefore many threshold scans are conducted for few pixels, varying the timing between bunch crossing ID reset and cal command from 0 to 512 bunch crossing ID counts (in units of 40 MHz). Figure 6.23 shows the measurement for the bare, double isolated ITkPixV1.1 0x16253. Figure 6.23 shows the measurement for the single isolated ITkPixV1.1 with sensor 0x13156.

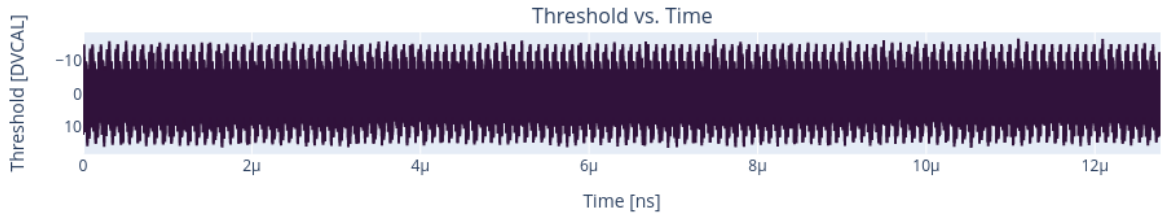


Figure 6.23: Single pixel threshold oscillation plot over full bunch crossing ID counter range for 0x16253

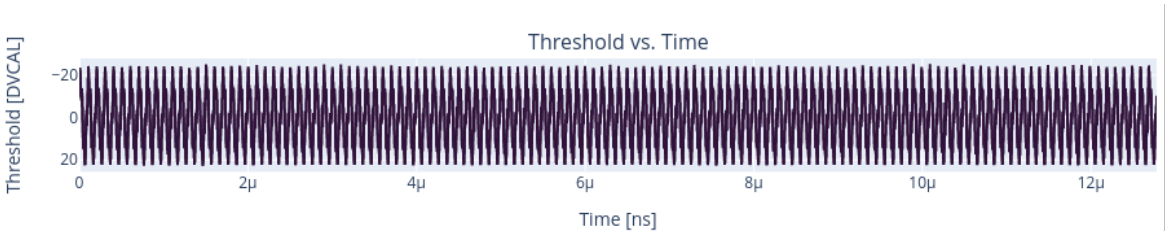


Figure 6.24: Single pixel threshold oscillation plot over full bunch crossing ID counter range for 0x13156

By eye, the frequencies, with which the detection threshold oscillates, is barely visible. Therefore a Fast Fourier Transformation is conducted on both data sets. The results are displayed in Figure 6.25 and Figure 6.26.

Both Figures show two dominant frequencies of 10 MHz and 40 MHz, plus negligible harmonics. Figure 6.25 shows a small 10 MHz component with a detection threshold variation of 4 delta vcal and a larger 40 MHz component with a detection threshold variation of 10 delta vcal. Figure 6.26 shows a large 10 MHz component with a detection threshold variation of 16 delta vcal and a larger 40 MHz component with a detection threshold variation of 6 delta vcal, which matches the observation in Figure 6.22. An explanation for the overall increased detection threshold oscillation in chip 0x13156 could be the single isolation, which allows the analog ground to oscillate more easily. At the same

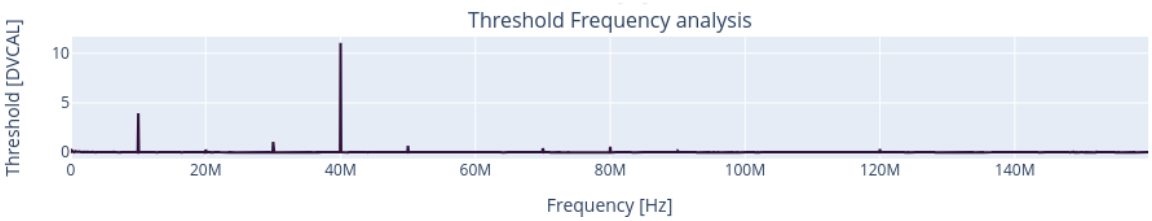


Figure 6.25: Fast Fourier Transformation of curve in Figure 6.23

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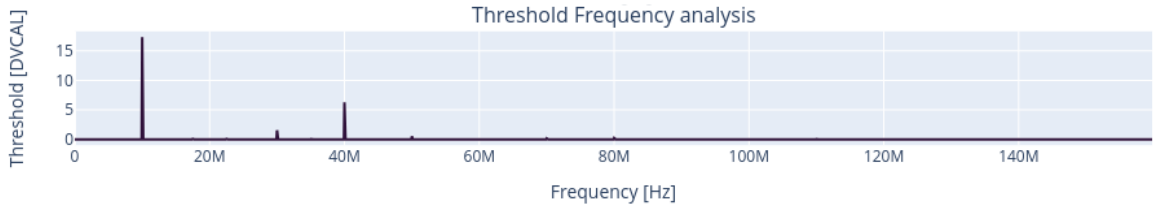

Figure 6.26: Fast Fourier Transformation of curve in Figure 6.24

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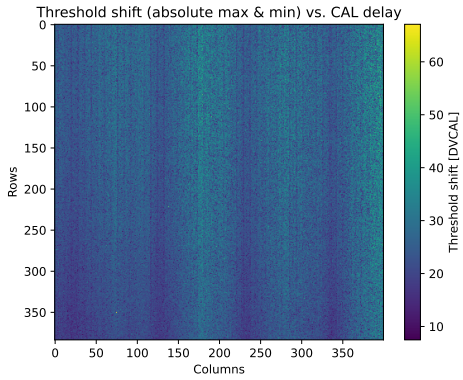
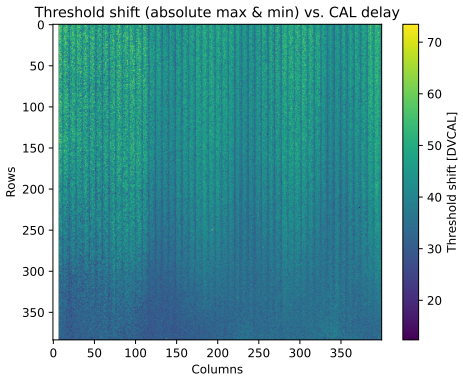
time, however, a suppression of the 40 MHz component is observed, which could be related to the change in capacitive load at the analog front end input, and therefore a reduction of the high frequency component. Please note that according to the charge calibration from Section 7.2.5, the threshold oscillations observed here are larger than the threshold dispersion observed in Section 6.3.1.
The next step of the investigation is the spatial analysis of this effect to figure out the variation of the effect on a per-pixel basis. For this purpose the maximum measured detection threshold is subtracted from the minimum measured detection threshold for each individual pixel and plotted in Figure 6.27 as a chip map. Figure 6.27(a) shows a maximum variation of 60 delta vcal for example in the top left corner of the chip, and a minimum detection threshold variation of 10 delta vcal at for example the bottom left of the plot. Along the vertical axis, a clear increase of the effect is visible, the further the pixel is away from the chip bottom. Along the horiontal axis two patterns are visible. One roughly every 100th column starting at column 140, with a minimum threshold shift and another with a minimum detection threshold oscillation every 8th column. Figure 6.27(b) shows the same patterns with different intensity, here the maximum detection threshold variation is measured in the top left at 70 delta vcal and the minimum detection threshold oscillation in the bottom right at <20 delta vcal. The pattern in every 8th column seems to be more pronounced, compared to Figure 6.27(a). The white bar on the left of the plot is related to the first 8 columns being disabled in the test.

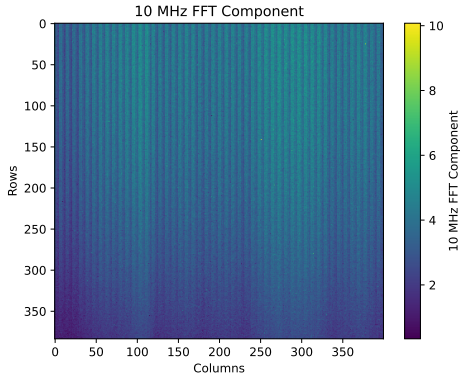
From Figure 6.26 it is known, that the 10 MHz component is more pronounced in chip 0x13156 with sensor and single isolation. Furthermore, it is known that in the same chip the pattern with a detection threshold oscillation minimum in every 8th column is more pronounced. Now the question is, whether the coupling of the 10 MHz component is therefore correlated with the pattern in every 8th column. This question is addressed in Figure 6.27(c) and Figure 6.27(d). Both plots show the 10 MHz component from the Fourier transformation for each pixel. It is evident, that the pattern concerning every 8th column is enhanced, while random pattern disappears. This random pattern, as well as parts of the horizontal pattern in every 100th column occur in Figure 6.27(e) and Figure 6.27(f) with the



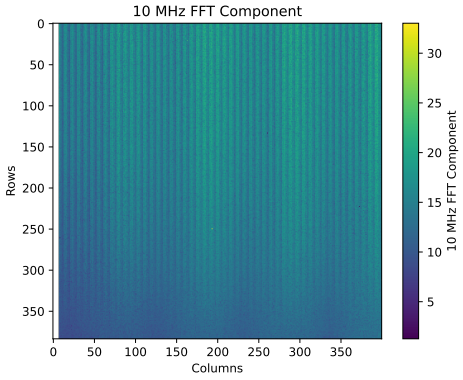
(a) Maximum detection threshold variation on a per pixel base for bare chip with double isolation 0x16253



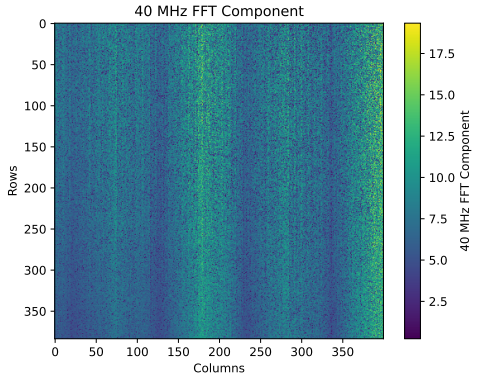
(b) Maximum detection threshold variation on a per pixel base for a chip with sensor and single isolation 0x13156



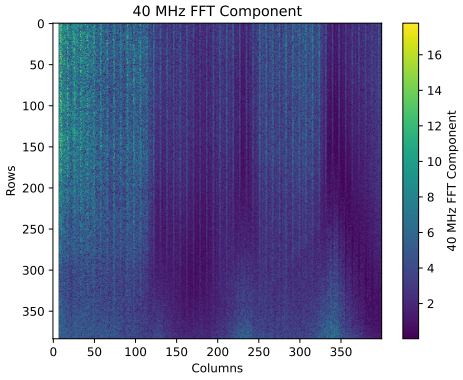
(c) 10 MHz amplitude from Fourier transformation per pixel for bare chip with double isolation 0x16253



(d) 10 MHz amplitude from Fourier transformation per pixel for bare chip with double isolation 0x13156



(e) 40 MHz amplitude from Fourier transformation per pixel for bare chip with double isolation 0x16253



(f) 40 MHz amplitude from Fourier transformation per pixel for bare chip with double isolation 0x13156

Figure 6.27: The detection threshold variation on a per-pixel basis

former exhibiting very small 40 MHz detection threshold oscillations on the right side of the chip. It is interesting to see that the 40 MHz component exhibits a completely new pattern in Figure 6.27(f), which might be related to the additional capacitance applied by the sensor on ITkPixV1.1. In general it is striking that the pixel pattern in ever 100th column correlates well with the wire bonds for the analog ground as Figure 6.28 shows.

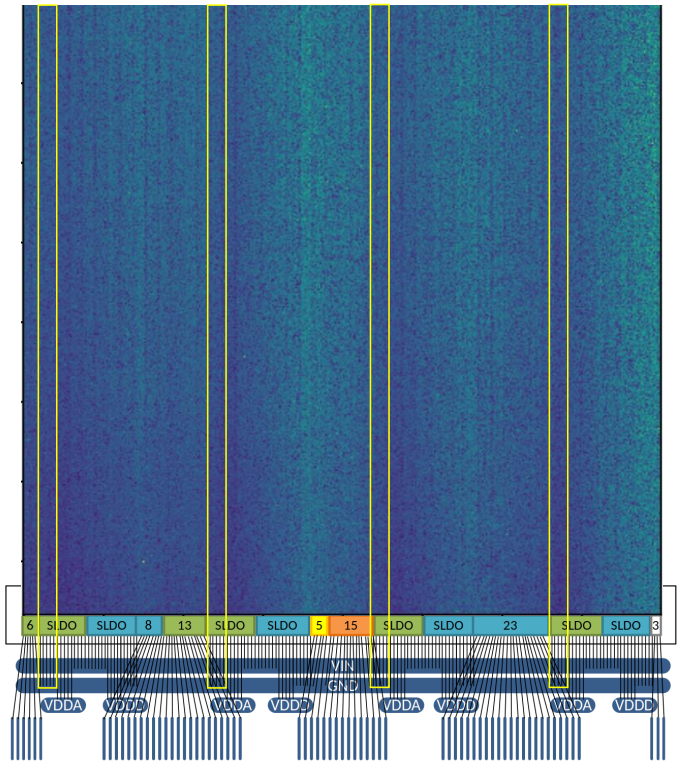
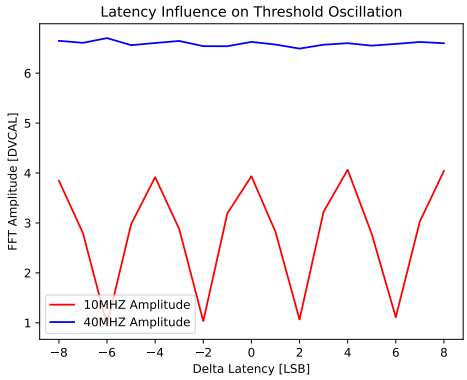
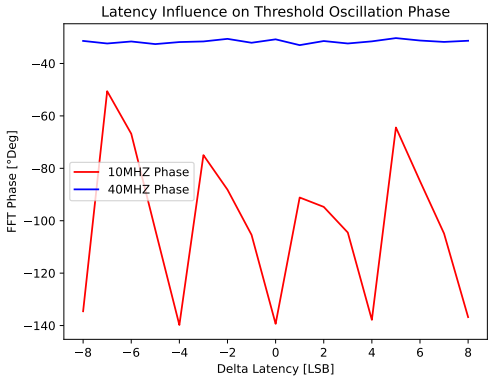


Figure 6.28: Overlay of Figure 6.27(a) with the pad frame of ITkPixV1.1

This could be an indication for the detection threshold oscillations being caused by the oscillation of the analog reference ground. To investigate the pattern in every 8th column, the same plots as shown in Figure 6.27 are generated as an average over all pixel cores for the maximum-minimum detection threshold shift, as well as the average 10 MHz and 40 MHz detection threshold shift per pixel in a pixel core. The plots can be inspected in Figure E.3. The dual stripe pattern in all of the shown plots in Figure E.3 is a good hint for the noise coupling to the biasing grid, which is shared among each pixel quad. In addition, projections of Figures 6.27 onto the column or row axis can be found in Figure E.4, as well as the phase-components of the 10 MHz and 40 MHz component, on a per-pixel (Figure E.1 and per-pixel core basis (Figure E.2). As expected the phase is shifting along the columns and, based on the grounding, along the rows. In the pixel cores the observed pattern matches well among both tested chips, for both frequency components. As mentioned earlier, there are two bunch crossing ID counters distributed over the matrix. To disentangle the effect of the two, it is possible, to vary the value of one of the two, while keeping the other value constant. Figure 6.29 shows the effect of the latency register, which defines the offset between bunch crossing ID counter and bunch crossing ID



(a) 10 MHz and 40 MHz amplitude variation for different latency settings



(b) 10 MHz and 40 MHz phase variation for different latency settings

Figure 6.29: Influence of the bunch crossing ID-Latency network on the Threshold oscillation.

latency counter. The default latency is 500, which is the value, that needs to be added to the x-axis of the plots in Figure 6.29 to acquire the true latency offset of the bunch crossing ID latency network. The y-axis in Figure 6.29(a) shows the amplitude of the corresponding frequency components in delta vcal. It is visible, that the 40 MHz component has a relative constant amplitude of 7 delta vcal, while the 10 MHz amplitude oscillates between 1 delta vcal and 4 delta vcal. The period is four bits, which suggests, that the highest influence on the 10 MHz detection threshold oscillation component is caused by the second least significant bit of the bunch crossing ID-latency network. When also considering Figure 6.29(b) little to no phase shift in the 40 MHz component is visible, while the phase of the 10 MHz component seems to depend on the latency setting. This dependence could hint at a second source of 10 MHz coupling, which couples to the detection threshold and interferes with the bunch crossing ID-latency network. From here it is clear, that the 10 MHz component can be suppressed by a clever setting of the latency offset.

After a possible origin for the coupling is found, the next question is where it couples. One possible coupling point in the analog front end could be behind the comparator and a digital buffer right behind the comparator. Figure 6.30 shows the potential coupling point.

The potential AC-coupling point marked in yellow, is particularly exposed behind the analog front end. This node is at the interface between the shielded analog front end and the non-shielded part in the digital logic, while the signal is not yet fully digitized. The signal behind the comparator may already be rectangular, but still not converted to a digital ToT value. Especially small rectangular signals may be affected by the high or low state of neighboring lanes, bringing them just in the detectable state for high neighboring lanes[4]. This hypothesis is supported by Figure 6.31, which shows a detection threshold dependence based on VDDA, which is expected. The VDDD dependence is surprising, since the speed of the digital logic behind the comparator seems to influence detection threshold, which so far is not considered relevant. It is further supported by the fact, that this feature is also observed in CROCV1[77], which uses a different analog front end than ITkPix. Therefore an analog front end independent coupling route is likely. Lastly, the oscillations are also observable in precision

[4] Please note, that all analog front end amplifiers and comparators are biased by VDDA, while the buffer behind the comparator is powered by VDDD.

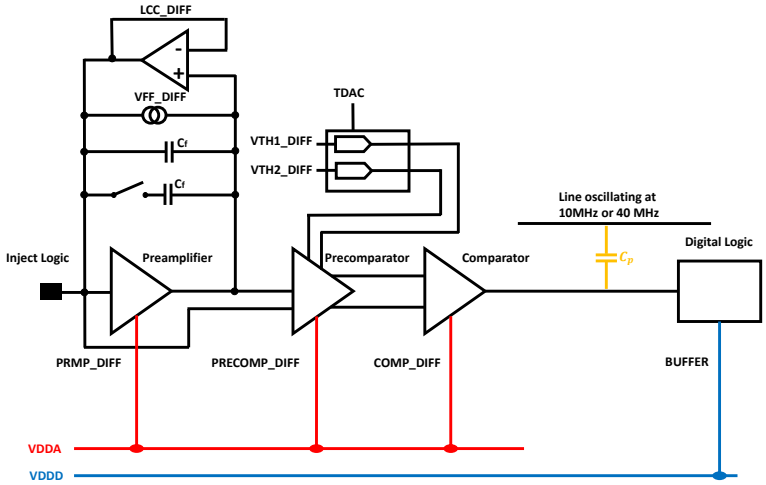


Figure 6.30: Schematic plot of the analog front end circuity, with potential parasitic coupling point for 10 MHz and 40 MHz coupling to analog front end signal marked by yellow capacitance and indicators for which biasing grid is used for which circuit.

Tot mode in ITkPixV1[78], which supports the hypothesis, that the coupling is not a local ToT artifact. In general, additional coupling paths are still possible.

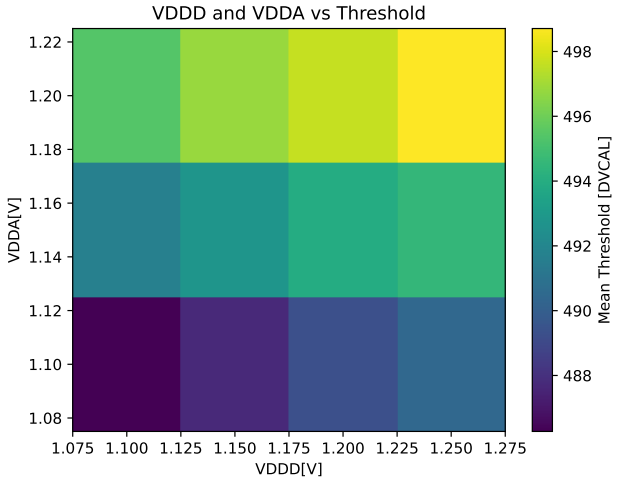


Figure 6.31: Threshold change based on bias voltages VDDD and VDDA

Due to time constraints, it is decided that the detection threshold oscillation feature will not be fixed in time for the ITkPixV2 submission. Therefore, this feature is expected to be present in the final detector. What does this mean for the final performance of ITkPixV2?

This feature influences two parameters in the specification Table 6.1. On the one hand, the minimum tunable threshold, which will be offset by the maximum detection threshold oscillation amplitude. In addition, the sigma of the calculated S-curve will be larger and proportional to the measured detection

threshold oscillation amplitude. Figure 6.32 shows these two effects, by showing an S-curve for one pixel at the minimum measured detection threshold over different injection timings with 160 MHz resolution in red, as well as an S-curve for one pixel at the maximum measured detection threshold over all injection timings with 160 MHz resolution in green. The blue S-curve shows the mean measured occupancy over all injection timings with 160 MHz resolution, including the corresponding S-curve fit. The increase in the S-curve sigma is clearly visible and translates to an increased S-curve noise. Simulations to quantify how far this influences the final ITk performance are still to be done.

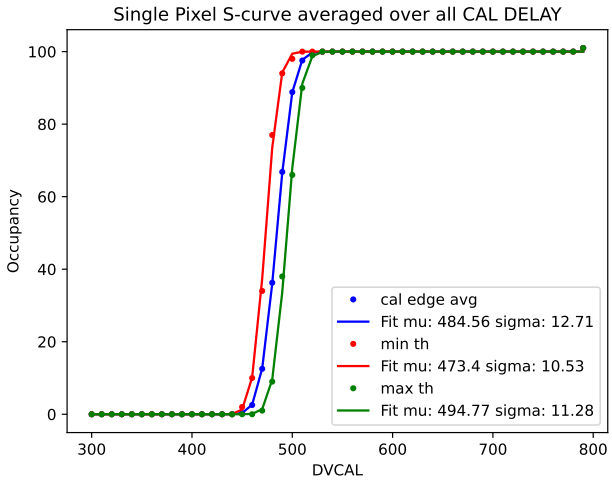


Figure 6.32: Threshold oscillation effect on a single S-curve

In total, this study shows a detection threshold oscillatory effect based on the state of the bunch crossing ID-latency networks during injection. The coupling frequencies are 10 MHz and 40 MHz. The effect is reduced based on the analog ground connection of the individual pixel and a clever latency choice. Moreover, the 10 MHz component is enhanced for RD53B with single isolation and sensor, while the 40 MHz component is suppressed for the same chips. In addition, the detection threshold μ and σ are expected to be larger by up to 100 e^- depending on the sampling time, as shown in Figure 6.32.

CHAPTER 7

ITkPixV1.1 Wafer probing

The performance of individual ITkPixV1.1 chips was shown in Section 6. This Chapter 7, will focus on testing large quantities of chips. To determine the production yield. The production yield defines the fraction of ITkPixV1.1, that work as expected. Since semiconductor manufacturing underlies statistical variation, it is therefore acceptable to have some nonworking chips. This Chapter focuses on the process of figuring out which ITkPixV1.1s do not work. For additional information feel free to check out Appendix F, giving a full overview of all tested parameters, with selection criteria and results. The following Section 7.1 introduces the wafer probing setup, followed by Section 7.2 discussing a selection of wafer probing results. Section 7.3 discusses the potential for future optimization.

7.1 Wafer-Probing Setup

The wafer probing setup is a permanent setup aimed at testing large quantities of chips on wafer level, immediately after arrival from the manufacturer. In this step, erroneous chips are caught by performing a series of standardized tests. Starting with the measurement of supply voltages and calibration of reference currents in addition to more complex scans testing the digital and analog functionality of the chip.

Figure 7.1 schematically shows the wafer probing setup. On the left, the DAQ PC with the BDAQ53 software is visible. This computer controls all the following components and stores the data acquired by the BDAQ53 board. The BDAQ53 board is connected to the DAQ PC via a 1 Gbit interface. The BDAQ53 board connects to the green probe card on the right through three display port connectors. The probe card is a design derived from the well-known Single-Chip Card, with few modifications to establish semi-permanent contact with a wafer and control of external chip pads through I2C, as well as a multiplexer to switch between multiple measurement pins, which are connected to the SMA connector of the probe card to a source meter. The source meter, as well as the two power supplies, are controlled via the USB-to-Serial interface by the DAQ PC.

The wafer probing setup is illustrated in Figure 7.1. The connection between the wafer and the probe card is established through 194 needles at an average inter-needle distance of 100 µm. Figure 7.6 shows two images of the mounted probe card and a zoom of the green frame in Figure 7.2(a), which shows a close-up of the probe needles, as well as the wafer-loaded chuck.

Figure 7.2(a) shows a photo of the probe station. At the bottom of Figure 7.2(a) the unloaded chuck is visible, which is responsible for supporting and moving a wafer. It uses vacuum to hold the wafer

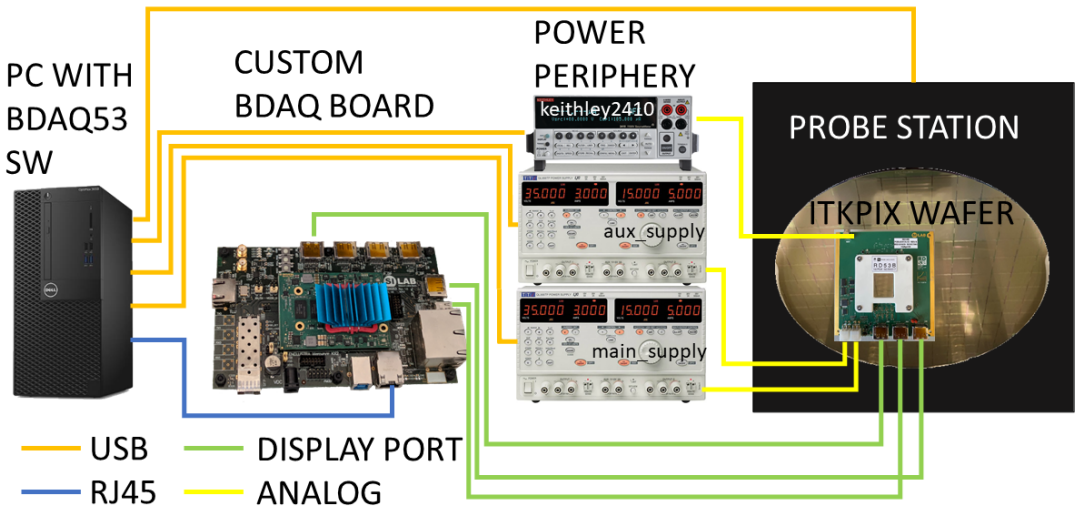


Figure 7.1: Schematics of all wafer probing components and their corresponding connections.

in place and a high-precision four-dimensional micrometer motor stage. The same image shows the probe card needle location in the center in a green frame. It is fixed to the probe station and calibrated every time a new probe card is loaded. It is of utmost importance that the probe card needles are perfectly parallel with the chuck to ensure good contact with the wafer on all 132 probed chips. The procedure for loading and unloading a wafer and probe card is documented in the probe manual [79] and Twiki[80]. On the top of the image a microscope is visible, which is used for the initial alignment of the wafer and needles. A view through the microscope is shown in Figure 7.2(b). The largest part of the images is occupied by an ITkPixV1.1. As a reminder, the difference between ITkPixV1 and ITkPixV1.1 is only an internal metal layer. An additional change of the top mask, to change the label, visible in Figure 7.2(b), was not conducted[1]. The bottom part of the image nicely shows the pixel matrix, with the chip bottom on the top[2]. The probe pads are tiny contact pads, which the probe needles on the probe card connect to. The black dots on the probe pads are dimples, caused by a previous needle contact. The pitch between the probe pads is 100 µm.

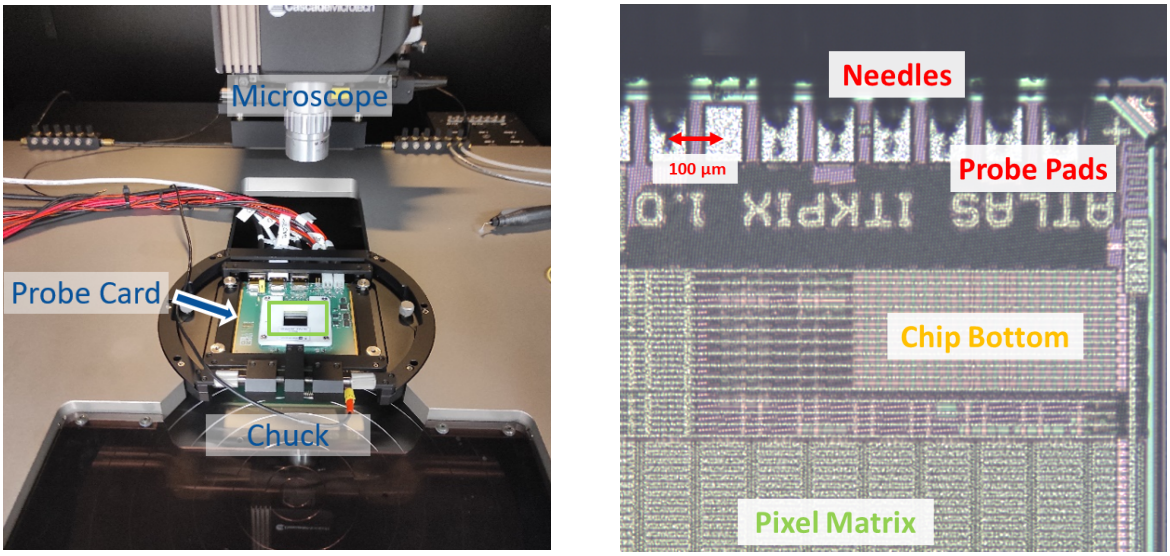
After the needles have established contact with the chip, the following routine is executed.

7.2 Wafer-Probing Routine

The ITkPixV1.1 wafer probing routine aims to test all major components of each individual ITkPixV1.1 chip, such as the powering, analog DAC and ADC components, as well as the digital readout of the matrix and the conversion of analog charges in the matrix. Figure 7.3 shows the tests performed per

[1] Hence, the ATLAS ITKPIXV 1.0 label

[2] The view corresponds to the bottom left corner in Figure 3.1



(a) Picture of the probe card installed in the probe station

(b) View through the probe station microscope

Figure 7.2: Images of the wafer probing setup as installed in the probe station

chip in their corresponding order. All tests are carried out in the shunt LDO mode with a constant voltage setting of 1.6 V for both, VINA and VIND.

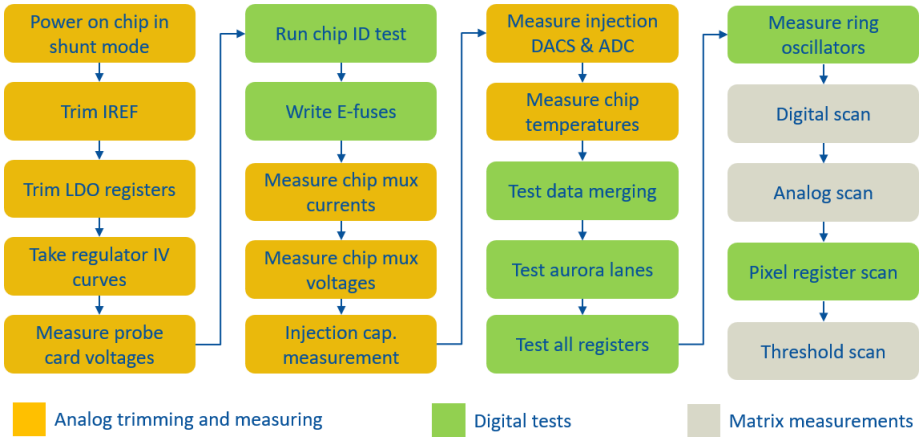


Figure 7.3: The order of tests of the wafer probing routine.

The tests are subdivided into three categories.

1. Analog and trimming measurements, ensuring that the correct voltages and currents are present at all measurable nodes.
2. Digital measurements, testing communication and setting blocks of ITkPixV1.1.
3. Matrix measurements, testing each analog front end in the matrix together with its digital readout logic.

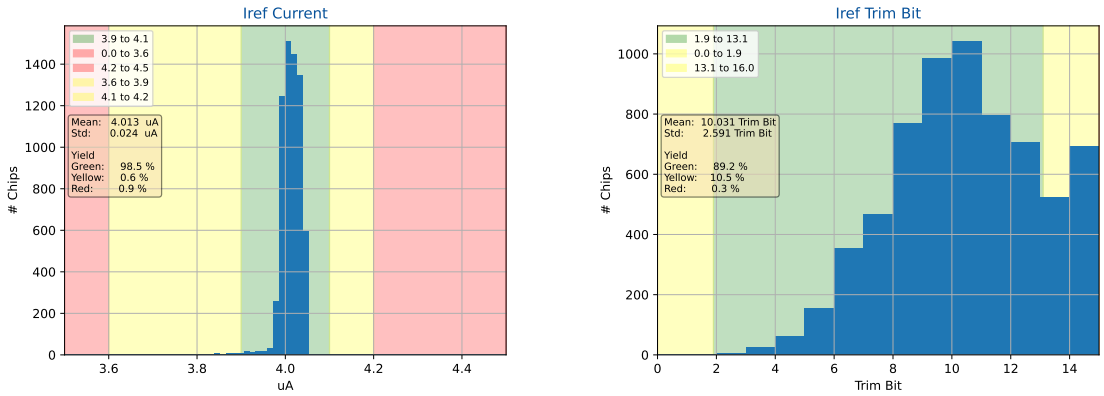
For each test, pass criteria have been extracted from simulation or by measurement. The pass criteria are indicated in the following Figures 7.4 by the following colors, all pass criteria are documented in Appendix F:

- **Green:** Green chips have been classified as chips, that can go into ITk.
- **Yellow:** Yellow classifies chips, that do work, but do not match a few classification parameters. Those chips will not go into ITk, but can be used for bench tests or DAQ development.
- **Red:** Red chips feature a serious problem, such as e.g. a short circuit and can neither be used for ITk nor for bench tests.

In the following the most relevant measurement results are discussed for 50 wafer and 6600 tested ITkPixV1.1.

7.2.1 Trim IREF

Section 3.2 introduces the IREF current as the fundamental RD53B reference current, which is used to derive many other biases and references in RD53B. The 4 bit IREF trim pads, during IREF trimming, are controlled by the probe card. Since the IREF current is not directly measurable on the chip pads, without configuration of the ITkPixV1.1, the offset voltage of the shunt regulator (VOFS) is measured. This voltage is connected by a current mirror to IREF. Over the external resistor R_OFS the current is transformed into a voltage. The expected VOFS voltage, at 4 µA IREF, is 498 mV. During trimming VOFS is measured starting with the highest to lowest IREF setting. Afterwards, the trim value, with a VOFS value closest to 498 mV is chosen as optimal IREF trim value.



(a) Histogram of IREF currents after trimming

(b) Histogram of IREF trim bits after trimming

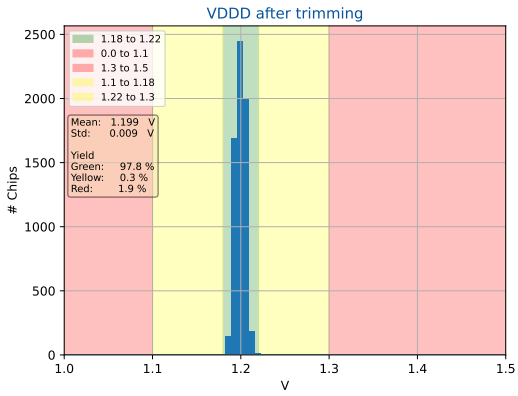
Figure 7.4: IREF histogram for 6600 ITkPixV1.1

Figure 7.4(a) shows the IREF current distribution after trimming. The current is well centered at 4 µA with a standard deviation of 0.24 µA. The chips are classified as green between 3.9 and 4.1 µA, with 98.5 % of chips fulfilling this criterion. Figure 7.4(b) shows the IREF trim bit distribution after trimming. The trim bits would ideally be centered around bin 8, with a standard deviation of 2-3. The chips are classified as green between 2 and 13, with 89.2 % of chips fulfilling this criterion. The IREF

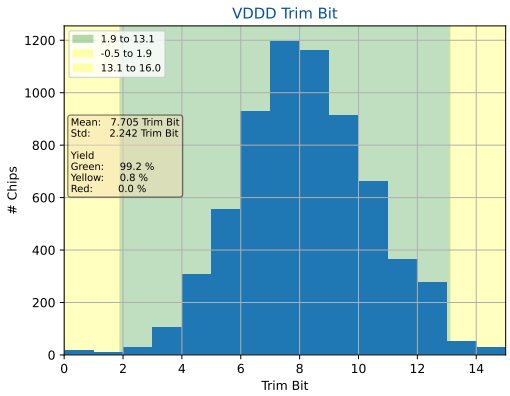
trim bit distribution is shifted to higher values due to a lower than expected core bandgap voltage, as shown in Figure F.4(a). The simulated and expected value is ≈490 mV, the mean core bandgap voltage for 6600 ITkPixV1.1 is 466 mV. The lower than expected voltage value can be corrected by lowering the R_IREF resistor shown in Figure 3.5. The current R_IREF value is 24.9 kΩ, the ideal calculated value is 24 572 Ω [81]. It was decided to keep the R_IREF value of 24.9 kΩ during wafer probing, due to the low availability of 24.6 kΩ resistors. In comparison to the RD53A wafer probing IREF trimming results [82], the IREF current distribution after trimming has similar features. However, the IREF trim bit distribution is more centered in the RD53A case, due to a better R_IREF match. The standard deviation in the current and trim bit case remain, as expected, unchanged. All in all the IREF trimming yields good results, with around 90 % green chips, despite the too large R_IREF value.

7.2.2 Trim LDO Regulators

LDO is short for low-dropout regulator, which regulates the voltages VDDD and VDDA entering the chip [65]. It is beneficial for microelectronics to be supplied with a higher external voltage, to compensate for losses on cables and printed circuit board and generate the needed VDDD and VDDA voltages on the chip, to be as stable as possible. This LDO regulator needs to be tuned. Figure 3.5 shows the internal chip trim registers as VrefA and VrefD trim bits. The trimmed voltages VDDD and VDDA can be measured on the probe card. All register settings for both VrefA and VrefD are measured consecutively, from highest to lowest value (15-0). Subsequently, the trim values, with VDDD and VDDA closest to 1.2 V, are chosen for all following tests.



(a) Histogram of VDDD voltage after trimming. The expected mean voltage is 1.2 V



(b) Histogram of VDDD trim bits after trimming. The expected mean trim bit is around 8.

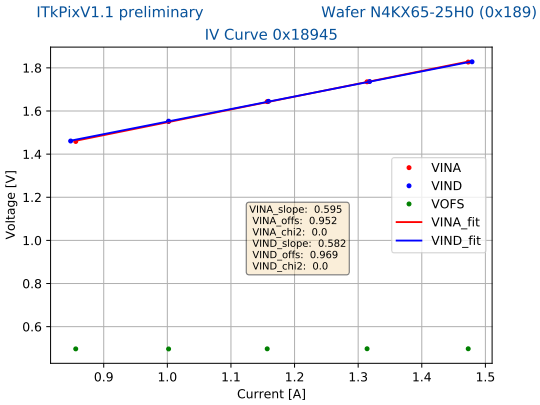
Figure 7.5: Test result plots of wafer probing test VDDD after trimming

Figure 7.5(a) shows the VDDD voltage distribution after trimming. The voltage is well centered at 1.2 V with a standard deviation of 9 mV. The chips are classified as green between 1.18 and 1.22 V, with 97.8 % of chips fulfilling this criterion. Figure 7.5(b) shows the VDDD trim bit distribution after trimming. The trim bits are well centered around bin 8, with a standard deviation of 2-3, which matches simulation and expectation. The chips are classified as green between 2 and 13, with 99.2 % of chips fulfilling this criterion. The results for VDDA trimming look similar, as shown in Figure F.11 and Figure F.9. Compared to the RD53A results [82], the standard deviation of the voltage

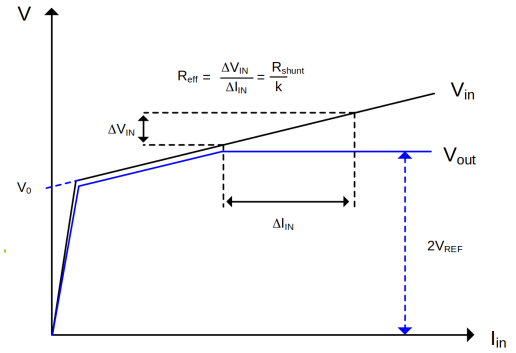
distributions decreased by ≈60 %, which resulted in the reduction of the green, acceptable VDDD and VDDA range from 1.1 V-1.3 in RD53A wafer probing to 1.18 V-1.22 V in ITkPixV1.1 wafer probing. The green yield however still increased from 92 % during RD53A wafer probing to 98 % in ITkPixV1.1 wafer probing.

7.2.3 Take regulator IV Curves

ITkPixV1.1 employs two shunt regulators, one for the analog and one for the digital powering domain. The shunt regulators are key for the serial powering plans of ATLAS ITk, which foresees to power multiple ITkPixV1.1 modules in series instead of in parallel as done in the current ATLAS inner detector. The shunt regulators ensure that the voltage drop over each chip remains constant, regardless of its current consumption (which changes, based on activity and configuration of ITkPixV1.1). Therefore, the shunt regulator delivers always a constant voltage at its output, while dumping access current to ground. This behavior looks like an ohmic resistance on the shunt regulator input. Figure 7.6(a) shows an exemplary current - voltage measurement (IV-Curve) of this behavior, taken during wafer probing.



(a) IV curve of the analog and digital shunt regulators of ITkPixV1.1 as taken during wafer probing



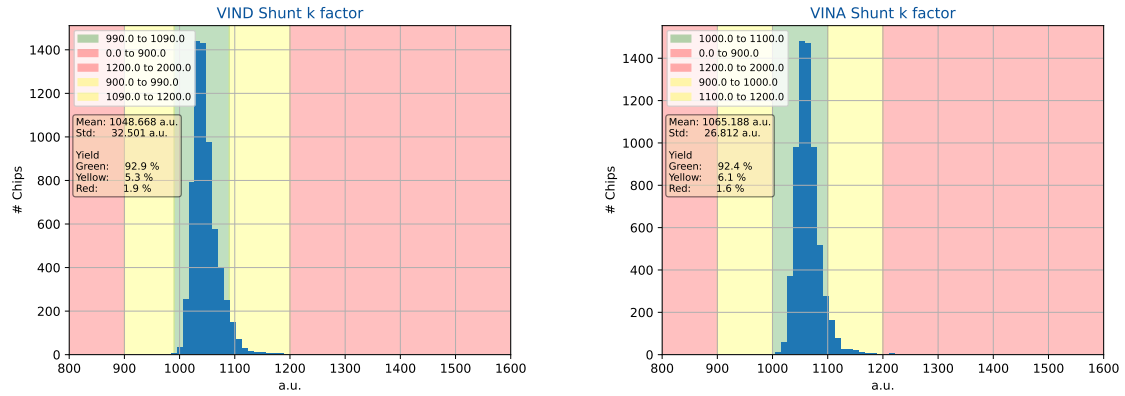
(b) Explanation of shunt regulator IV curve [44]

Figure 7.6: IV curves of ITkPixV1.1 shunt regulators

This measurement is conducted by applying a known voltage, while measuring the consumed current on the ITkPixV1.1 power supply. The red and blue dots indicate the measured input voltage and current at the shunt regulator inputs, while the lines indicate a linear fit of the measured dots. The fit parameters are shown in the plot. The green dots indicate the measured shunt regulator offset voltage, which is expected to be constant, as long as the shunt regulator start-up is successful. The slope and the offset give a fine indicator of the behavior of the shunt. Due to the dependence on the fit quality, however, it is chosen to evaluate the shunt regulator quality based on the k-factor. The k-factor is calculated as follows in Equation (7.1):

$$K = R_{shunt} \cdot \frac{I_{in}}{V_{in} - V_{ofs}} \tag{7.1}$$

R_{shunt} is a value of the external resistor that gives the user precise control over R_{eff} as shown in Figure 7.6(b). The design k-factor is 1000, therefore $R_{eff} = R_{shunt}/1000$ describes the effective resistance of the shunt regulator. Figure 7.6(b) shows the ohmic behavior of the shunt regulator in black, while the output voltage Vout remains constant after reaching, in this case, the desired 1.2 V. Figure 7.6(a) shows a measurement in the region, where $V_{in} > V_{out}$, but $V_{in} < 2$ V. The calculation of the k-factor during wafer probing occurs in the configured state of the chip, meaning the analog front end is enabled and all core columns are enabled. The measured IV curves are based on five measurement points between 1.5 V and 1.9 V, set on the Vin power supplies. The original shunt regulator measurement, as uploaded to the ITk production database, is based on a Vin measurement via a non current carrying needle, as it arrives on the chip. For each set voltage, the current is monitored by the power supply, as well as VOFS measured on the probe card. The ground shifts are subtracted accordingly. For the calculation of the k-factor only voltages measured via non-current-carrying needles, which are between 1.4 V and 1.8 V, are considered. The mean of those calculated k-factors is then assigned as ITkPixV1.1s k-factor. The digital and analog k-factor distribution is shown in Figure 7.7.



(a) Digital ITkPixV1.1 k-factor distribution for 6600 chips, using VIN_SENSE as Vin

(b) Analog ITkPixV1.1 k-factor distribution for 6600 chips, using VIN_SENSE as Vin, using VIN_SENSE as Vin

Figure 7.7: IV curves of ITkPixV1.1 digital and analog shunt regulators, using VIN_SENSE as Vin

Figures 7.7 show a distorted Gaussian distribution, with a tail towards higher k-factors. For a long time there has been a debate on where this tail comes from. In the end the mean value, which is around 5 % higher than the expected value of 1000, gave an additional hint to solving the mystery. To understand where the shift comes from, it is necessary to understand how the Vin voltage is measured. Figure 7.8 shows a simplified schematic view of the shunt regulator measurement setup. On the left the TTi Vin power supply and Keithley 2410 source meter connected to a multiplexer are visible. The green rectangle represents circuitry present on the probe card, with the blue rectangle representing part of an ITkPixV1.1 with some of its yellow probe pads. In addition to that the variable resistance between probe card and ITkPixV1.1 is indicated by green resistor boxes labeled R_needle. This resistance changes with every approach to the chip, based on e.g. force applied to the needles or surface structure of the probe pad. The red dots indicate voltage measurement points, which are measured during the wafer probing routine, as discussed here. The yellow point represents the voltage, which the shunt regulator sees, to adjust its resistance. This point is not yet measured but is expected

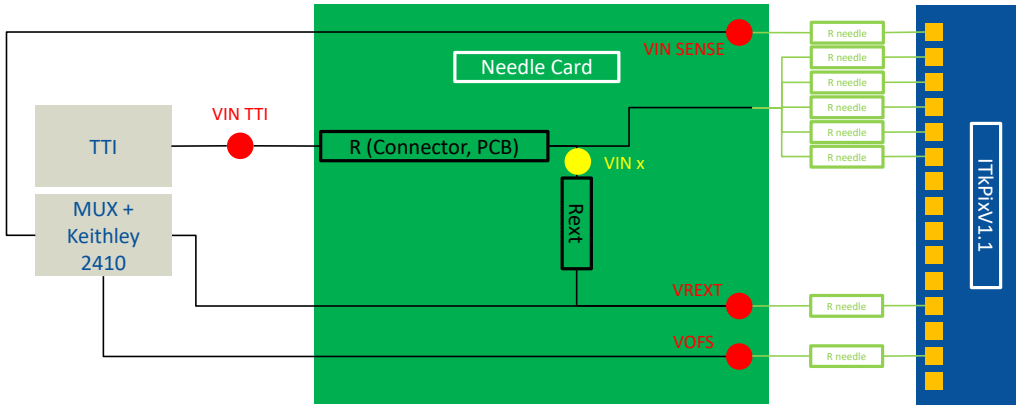
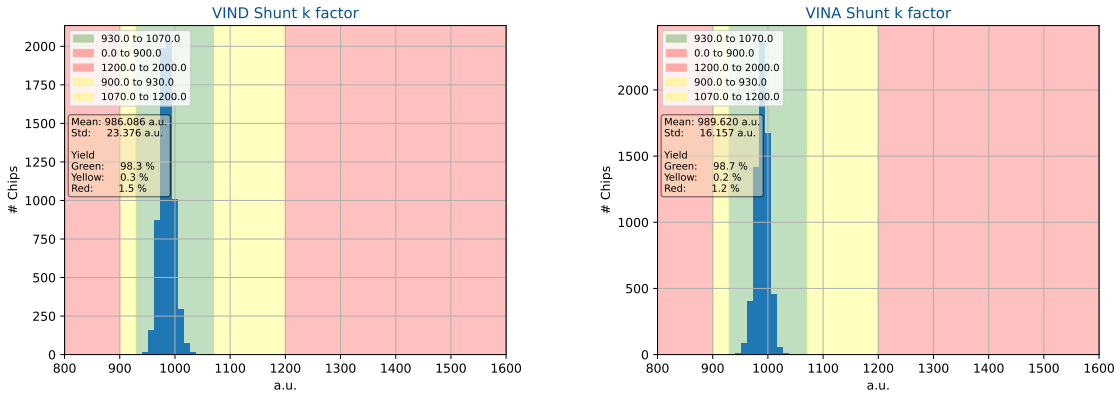


Figure 7.8: Simplified schematic view of the shunt regulator Vin measurement points.

to yield the most accurate Vin measurement to calculate the shunt regulator k-factor. To understand, why it matters where Vin is measured, it is important to be aware of the fact, that the Vin power lines carry a lot of current, which has influence on the voltage present at each of the red nodes based on their resistance to the power supply. In addition to that it is important to note, that the voltage, the shunt regulator sees can be different from the Vin voltage present on the chip. This is related to two different sets of needles, which supply Vin to the chip, via many current carrying probe card needles, where a significant voltage drop can occur and a second, single non-current-carrying needle, which supplies Vin to the shunt regulator.



(a) Digital ITkPixV1.1 k-factor distribution for 6600 chips (b) Analog ITkPixV1.1 k-factor distribution for 6600 chips

Figure 7.9: IV curves of ITkPixV1.1 digital and analog shunt regulators

In short, VIN_SENSE does not always correspond to the Vin the shunt regulator receives. It is even worse, that a VIN_SENSE measurement includes the variable resistance R_needle, which changes with every new contact to the chip and broadens the distributions shown in Figure 7.7. A better Vin reference, which has also been measured during ITk pre-production wafer probing, is VIN_TTI. This Vin still contains unknown resistances of the connector between TTI and probe card, as well as the unknown resistance of the probe card traces. However, theses resistances can be assumed to be constant, in contrast to the needle resistance. Equation (7.2) and Equation (7.3) summarize the error terms relevant for the k-factor calculation using either VIN_SENSE or VIN_TTI:

$$K = R_{shunt} \cdot \frac{I_{in}}{(Vin_{Sense} - (Iin \cdot R_{Needle})) - V_{ofs}} \tag{7.2}$$

$$K = R_{shunt} \cdot \frac{I_{in}}{(Vin_{TTI} + (Iin \cdot R_{PCB})) - V_{ofs}} \tag{7.3}$$

The main difference is the systematic character of R_{PCB} and statistic nature of R_{Needle}. Figure 7.9 shows histograms of the k-factors calculated according to Equation (7.3). These histograms exhibits significantly less spread, and especially no tail to higher k-factors. It is, however, expected, that Equation (7.3) systematically underestimates the k-factor, which is why the mean new k-factor appears lower than the previous one in Figures 7.7. All in all the new k-factor calculation method decreased the k-factor spread siginificantly, while allowing for a narrower green window around the simulated k-factor of 1000, thus increasing the yield by 5 %. A comparison to RD53A results does not make sense, due to a different parameter used to characterize the shunt regulator, as well as a start-up bug present in RD53A, preventing reliable shunt measurements. This bug was fixed in RD53B.

7.2.4 Injection Capacitance Measurement Circuit

The Injection Capacitance is a capacitance shown in Figure 3.3 labelled with "Injection" on the left side. It is responsible for injecting a well-known amount of charge into the analog front end of each pixel. According to Equation (6.2), introduced in Section 6.3.1.

Where Q represents the injected charge, C the injection capacitance, and U the voltage supplied to the Injection Capacitance. The accuracy of the injected charge Q depends on an accurate measurement of C and U. The voltage U can be easily measured with an external multi meter, while measurement of C requires an internal capacitance measurement circuit. The Capacitance Measurement Circuit is shown in Figure 7.10.

The design is based on a charge pump connected to two independent capacitance measurement branches:

1. A copy of 100 parallel injection capacitors in the chip bottom.

2. The same layout as in 1, without the injection capacitances. This is used to measure parasitic effects.

Therefore the capacitance measured on branch 1 is described by Equation (7.4):

$$C_{meas} = 100 \cdot (C_{pix} + \Delta C) + C_{par} \tag{7.4}$$

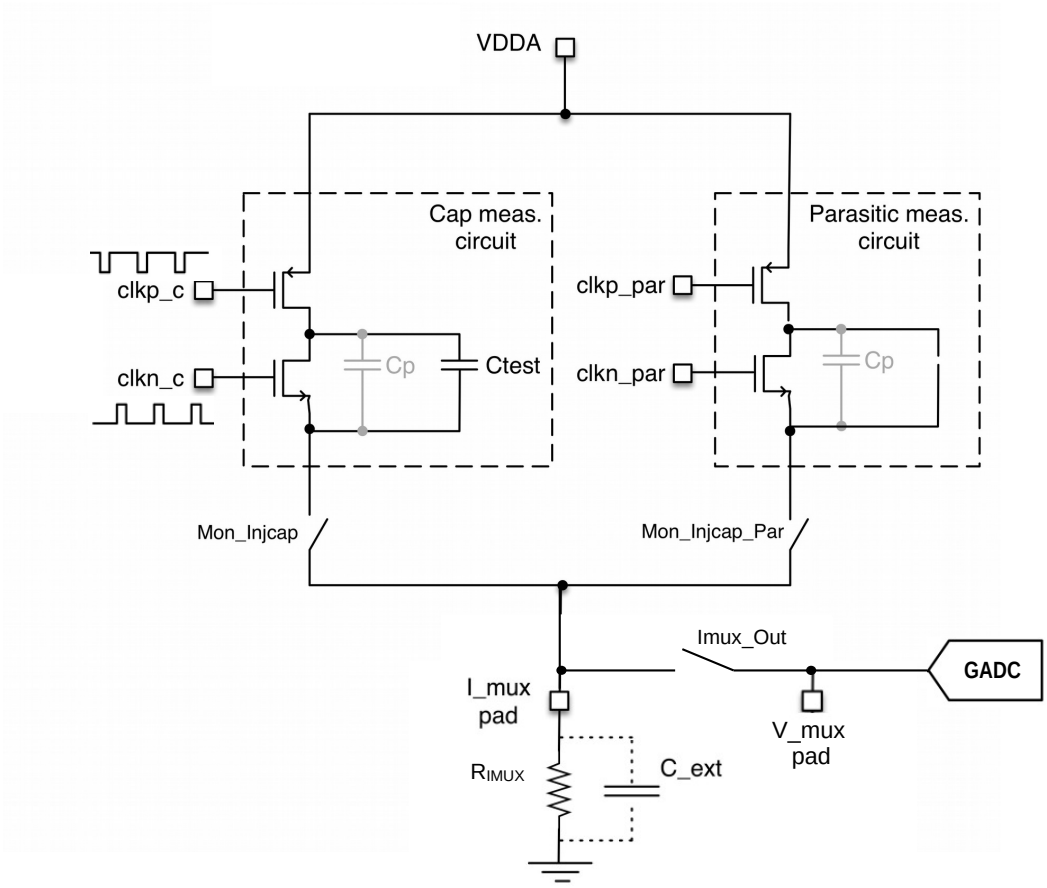


Figure 7.10: A schematic diagram of the RD53B injection capacitance measurement circuit [44].

Where C_{pix} is the capacitance seen by a single pixel, ΔC is the difference of the simulated capacitance between the connection of the injection capacitance measurement and the true injection capacitance array, and C_{par} is the parasitic capacitance measured in the second branch (right of Figure 7.10). The measured capacitances are proportional to the current I_{GADC} flowing from $VDDA$ through either of the measurement branches to the IMUX out, which is measured with an external multi meter. An additional dependence offers the frequency of the applied clocks F_{clk}, as shown in Equation (7.5):

$$C_{meas} = \frac{I_{GADC}}{F_{clk} \cdot VDDA} \tag{7.5}$$

The measured capacitance C_{meas} is therefore proportional to the measured current I_{GDAC}, as well as the analog supply voltage VDDA and F_{clk}.

7.2.5 ITkPixV1.1 charge calibration

In the experiment one of the most critical factors to determine a detector's performance is the detection threshold, which defines what amount of charge is detectable by the readout chip. The detectable

charge is measured in electrons (e^-). Section 3.1 describes, that a known charge can be injected into the analog front end if the injection capacitance is charged with a known injection voltage. The mean injection capacitance value for all measured chips during wafer probing as well as the mean slope of the injection DACs is discussed in the following Sections. The goal is to find a general conversion factor between the injection voltage (DVCAL) and e^-. The expected conversion factor from simulation between injection voltage DVCAL to e^- is $5\,e^-$ for the low-gain mode, where the injection DAC reference voltage is half the reference voltage of the high-gain mode, with an expected conversion factor from DVCAL to e^- of $10\,e^-$.

Injection Capacitance Measurement

The injection capacitance measurement circuit is described in Section 7.2.4. It measures a copy of 100 injection capacitances, as indicated on the left in Figure 3.3(a). The measurement circuit is based on a charge pump, measuring the current through either of the two measurement branches in Figure 7.10 at a given impedance frequency and VDDA. The impedance frequency is assumed to be constant at 10 MHz, it has a dependence on IREF, which is why IREF is monitored during the measurement. Furthermore, the ground of the injection capacitance measurement circuit differs from the ground of the multiplexer on the probe card, which is why an additional reference ground measurement is conducted. The currents through the non-parasitic and parasitic branches are measured 10 times each. The injection capacitance is then calculated using Equation (7.4) and Equation (7.5).

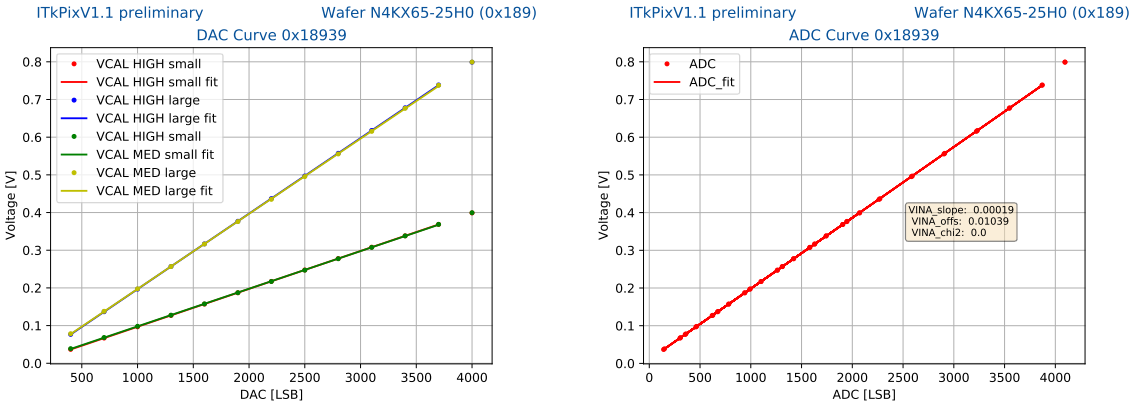
Injection DACs and ADC Measurement

The injection DACs vcal med and vcal high generate voltages for the injection capacitance according to Equation (6.2). During injection a charge proportional to the voltage difference between vcal high and vcal med is injected. Therefore, an accurate charge calibration requires precise knowledge of each chip's injection capacitance, vcal med and vcal high. Therefore, the voltage of vcal med and vcal high is measured using the voltage multiplexer described in Table F.3 and the external multi meter. This procedure is repeated for 12 DAC settings, followed by a slope and offset calculation for each DAC. At the same time, the DAC settings are measured with the internal ADC, the known voltages measured with the external multi meter are then used to get a calibration for the vcal med and vcal high DAC, as well as the ITkPixV1.1 internal ADC. Figure 7.11 shows example graphs for the slopes of DAC and ADC.

Figure 7.11(a) features four lines, two for the high-gain mode (blue and yellow), where the DAC reference voltage for vcal med and vcal high is twice the reference voltage for the low-gain mode indicated by the green and red lines. Figure 7.11(b) shows the ADC slope in red, with a higher density of measurement points in the lower half of the x-axis, which is due to the extra measurements in low-gain mode for the DACs. The highest measured value is not considered in the fit range, as DACs and ADC tend to saturate in these regions.

Charge Calibration

The charge-calibration factor is calculated using Equation (6.2) in units of e^-. Figure 7.12(a) shows the distribution of measured injection capacitances, with a distribution width of 2 %. The cut colors in the background are irrelevant since no chip is discarded due to poor injection capacitance. However all



(a) vcal med and vcal high curves for high and low gain mode

(b) ADC curve with fit

Figure 7.11: Example output of the DAC and ADCf calibration

injection capacitance values are stored in the ITk production database for future detector calibration. Figure 7.12(b) shows the vcal high DAC slope in low-gain mode, with a width of the distribution of 13 %. The color cuts in the background are irrelevant, for the same reason as mentioned before. The slope values are again stored in the ITk production database for future detector calibration. The rest of the vcal high, vcal med slopes and offsets in high- and low-gain mode can be found in Section F.2.

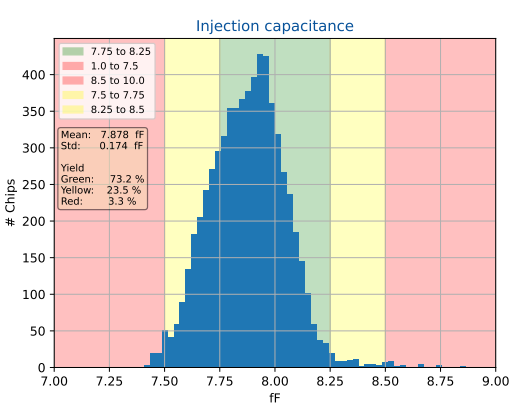
	vcal high	vcal med
low-gain mode	$4.93\,e^- \pm 0.25\,e^-$	$4.90\,e^- \pm 0.25\,e^-$
high-gain mode	$9.86\,e^- \pm 0.50\,e^-$	$9.80\,e^- \pm 0.50\,e^-$

Table 7.1: Mean charge calibration and error for 50 ITkPixV1.1 wafer

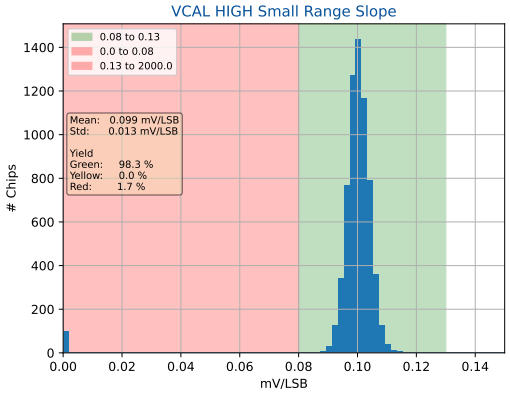
Table 7.1 summarizes the charge calibration values for vcal high, vcal med in high- and low-gain mode. The values are in good agreement with the $5\,e^-$ and $10\,e^-$ from simulation. The errors on the calibration values are, however, quite large. A variation of 5 % at a threshold of $2\,000\,e^-$ corresponds to $100\,e^-$. Therefore a per chip calibration during ITk production does make sense.

7.2.6 ADC and DAC Calibration

The calibration of reference voltages per chip is fundamental to achieve a more accurate DAC and ADC calibration. The data for the ADC calibration is taken during the routine explained in Section 7.2.5. From Section 6.2.1 an ADC reference voltage fluctuation of 6 % between −40 °C and 40 °C on a single chip is already known. Figure 7.13(a) shows the ADC slope for all probed chips. The expected ADC slope, at a (VREF_ADC) of 0.9 V, is expected to be $0.2\,\text{mV}\,\text{LSB}^{-1}$, according to simulation [44]. Figure 7.13(b), however, features a mean VREF_ADC of 0.791 V, which explains the lower mean ADC slope observed in Figure 7.13(a). The standard deviation of the Gaussian distribution in Figure 7.13(a) is 4 %, which is lower than the error introduced by temperature fluctuations. In the final detector the error on ADC measurements is therefore expected to be dominated by external factors such as temperature or radiation damage, as presented in References [83], [84] and [85]. Figure 7.13(b)

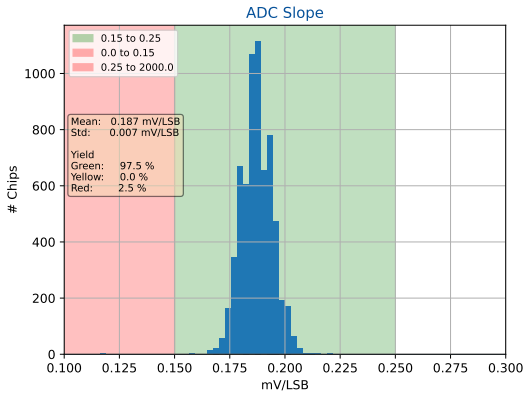


(a) Histogram of all measured injection capacitances

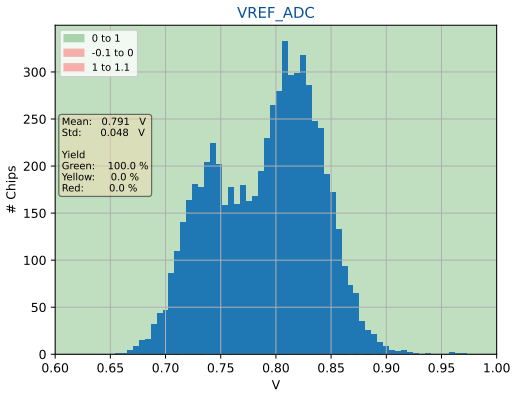


(b) Histogram of all measured vcal high slopes in low-gain mode

Figure 7.12: Exemplary distributions necessary for ITkPixV1.1 charge calibration



(a) Histogram of all measured ADC slopes



(b) Histogram of all measured VREF_ADC voltages

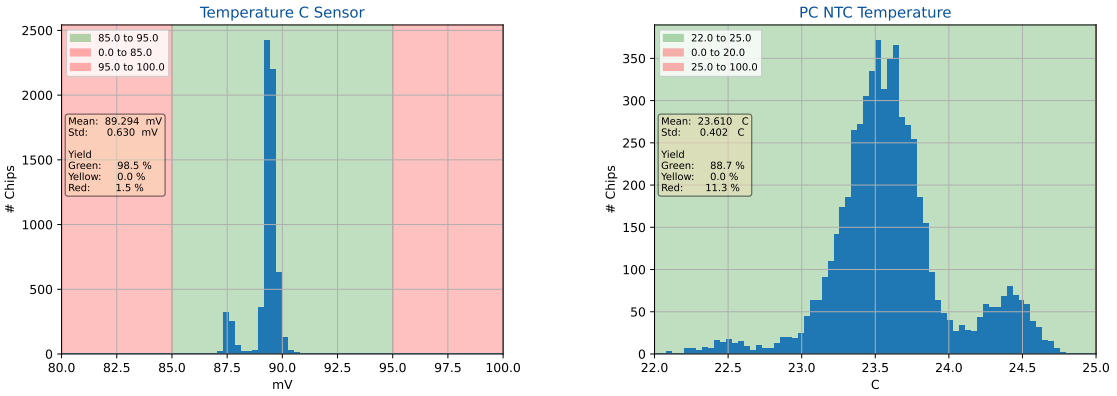
Figure 7.13: Histograms of ADC slope and VREF_ADC

shows a double-Gaussian distribution. The right distribution contains the first 32 probed wafers and the left distribution contains the last 18 probed wafers. The shift in VREF_ADC was introduced by a change in the IREF trimming routine, as documented in Reference [86]. With changing the IREF trimming routine, IREF is systematically trimmed lower, which automatically leads to a shift in VREF_ADC, that is dependent on IREF as shown in Figure 3.5.

7.2.7 Chip Temperature Sensor Calibration

The chip temperature sensors are part of the monitoring and sensing environment in the chip bottom, with the exception of a temperature sensor at the top of the matrix. All RD53B chips have five temperature sensors. Figure 6.4 shows the locations of the sensors. The measurement principle during wafer probing is described in Section 6.2.1. Figure 7.14(a) shows the voltage ΔV_D introduced in

Equation (6.1), for all measured chips. Two Gaussian distributions are visible, one centered around 87.5 mV, corresponding to 29.2 °C and one centered around 88.5 mV, corresponding to 32.7 °C, assuming a non-ideality factor N_f of 1.24. The standard deviation over the whole range corresponds to 2.1 °C. Figure 7.14(b) shows the measured temperatures by an NTC on the probe card. This Figure again shows two Gaussian distributions, one centered around 23.5 °C and one centered around 24.4 °C. The standard deviation is 0.4 °C. Comparing the mean and the standard deviation of the two plots suggests low correlation between the two values.



(a) Histogram of all measured ITkPixV1.1 central diode temperature sensors

(b) Histogram of all measured NTC temperatures on the probe card

Figure 7.14: Histograms of on-chip temperature and probe card temperature sensors

Figure 7.15 confirms the observation in Figure 7.14. There is no correlation between on-chip temperature sensor and probe card measured temperature. As a reminder, the standard deviation of the distribution shown in Figure 7.15 is 2.1 °C, with the center of the distribution at 35.4 °C.

All in all Figure 7.15 suggests the search for a different temperature calibration method than during wafer probing. Section 6.2.1 even suggests one calibration constant for all chips.

7.2.8 Threshold Measurement

The threshold scan is explained in Section 4.1.3. During wafer probing the threshold scan is the most complex and one of the most time-consuming scans conducted. It requires the establishment of communication bteween chip and DAQ, as described in Section 5 to work, as well as the digital matrix readout. Due to the lengthy scan time it would be a prime candidate to be removed from the wafer probing test sequence, if the information about e.g. the mean detection threshold of all pixels could be substituted. Section 3.1.1 introduces that the detection threshold can be controlled by the threshold voltage VTH1. Therefore the correlation between detection threshold and threshold voltage is investigated in the following Section.

Figure 7.16 shows the correlation between detection threshold, injected charge and threshold voltage. From Section 7.2.5 it is known, that the injection circuit varies from chip to chip. Therefore the injection charge is additionally shown in this Figure 7.16. A strong anticorrelation between detection threshold and injected charge is observed. This behavior is expected, since a higher injected charge at the same delta vcal setting will lead to an earlier detection at lower delta vcal of hits in the analog

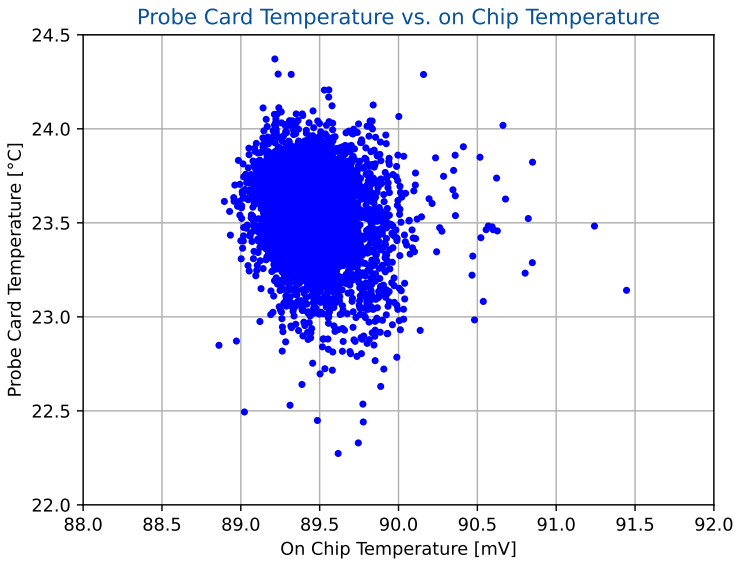


Figure 7.15: Correlation between on-chip temperature and reference temperature measured on the probe card.

front end. In addition, a threshold voltage correlation between chips with similar injected charge and similar detection threshold can be observed as indicated by the colors. All in all this analysis is a nice consistency study of the ITkPixV1.1 behavior. However, the detection threshold behavior is difficult to predict with just one additional threshold voltage measurement. Therefore it is advised to keep the threshold scan in the wafer probing routine.

7.2.9 Yield

The yield corresponds to the fraction of chips, which pass all functionality tests. If a chip is classified as green in the yield diagram, it is fit for detector deployment. The total yield distribution is visualized in Figure 7.17(a). This Figure shows three discrete peaks between zero and one. Zero representing chips with at least one red functionality test, 0.6 representing chips with at least one yellow functionality test and one representing chips with only green functionality tests. The green bin height corresponds to the final yield, which is 86.7 %, as indicated in Figure 7.17(a). The yellow bin height corresponds to 3.2 % of all tested ITkPixV1.1 and 10.1 % are classified as red chips after running all functionality tests. The wafer probing tests with the highest probability to be not classified green are:

1. The threshold scan with 8 % failure probability, which is the most complex scan conducted, testing communication, analog and digital pixel readout, as well as injection.

2. The digital scan, with 6 % failure probability, which is the first test, which relies on in pixel digital data readout, before the threshold scan.

3. The analog scan, with 5 % failure probability, which would usually have a higher failure probability than the digital scan, but due to the high-current bug, the analog scan during wafer probing is conducted in precision Tot mode.

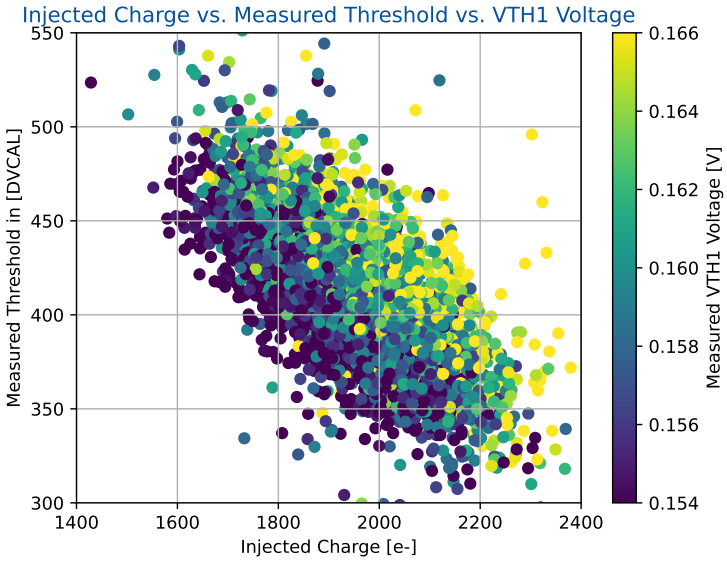
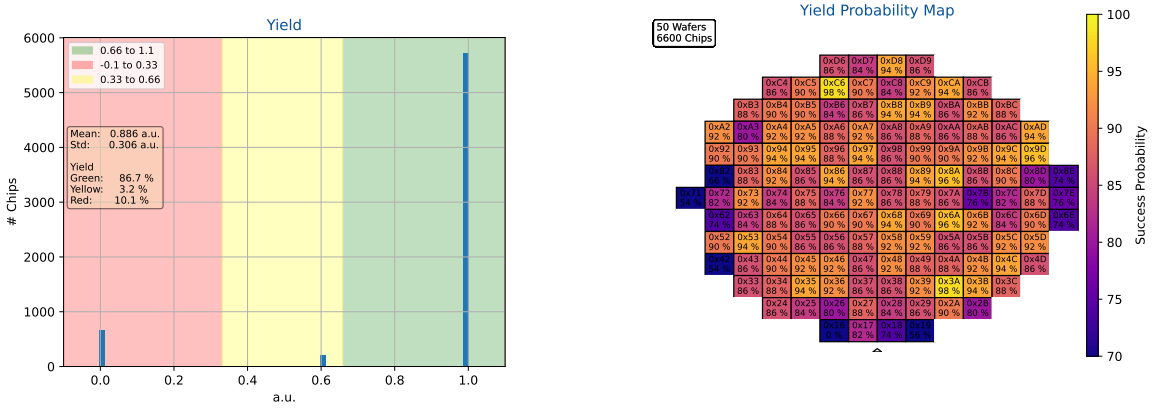


Figure 7.16: Correlation between detection threshold, injected charge and threshold voltage.

The failure probability for all wafer probing tests can be found in Appendix F.



(a) Yield Histogram for 50 wafers

(b) A wafer map with the average yield probability for a green chip averaged over 50 wafers

Figure 7.17: Test result plots of wafer probing test Yield

Figure 7.17(b) summarizes the probability for an ITkPixV1.1 to be green based on chip location on the wafer. The distribution over 6600 probed chips, on 50 wafers is homogeneous within the statistical errors, with lower green probability towards the edges and especially the bottom edge. This is related to lower process control concerning e.g. metal deposition or doping during production at the wafer edges. In addition to that, many of ITkPixV1.1's important communication circuits are located in the chip bottom and towards the chip edge. Logically chips, whose chip bottom is located closer to the edge of the wafer are more likely to fail. This expectation matches the observation in Figure 7.17(b).

All in all the ITk pre-production ITkPixV1.1 wafer probing result is better than expected. With an original yield expectation of 60 %, it is great to report that this goal is surpased by 16 %, with a final yield of 86 %. In comparison, the ITk pre-production RD53A wafer probing yield is 64.3 %. The increased yield can be attributed to improvements in the shunt regulator design [87], as well as improvements to the startup and command locking circuit [58]. Future steps concerning wafer probing of ITkPixV1.1 successor chips is discussed in the following Section 7.3.

7.3 Speed-up and Improvement Potential

Apart from the yield discussed in Section 7.2.9, the second important parameter in wafer probing is the test time per chip. The ITk pre-production wafer probing is designed to take 20 min per chip, which corresponds to 48 h per wafer. In the original ITk upgrade plan this time was acceptable, with the expectation of four test sites probing 3 wafers per week per site. With a change in the availability of sites and the delay of ITkPixV2 submission, quicker wafer probing is desirable. However, not any reduction in test time makes equal sense. In theory for example, 36 h per wafer increases the wafer output per site from 3 to 4, but implys a 24 h shift system at every site, since wafers would have to be changed at inconvenient times at night. Therefore it is an objective of this Section to discuss potential time savings, to reduce the probe time to something in the order of 24 h, increasing the wafer output per site to four a week, while maintaining reasonable working hours for the team. Table 7.2 summarizes the per-chip test times for all routines. A red highlight indicates a scan, that could be removed to save time. What other optimization measures can be taken will be discussed in the following.

The slowest scan is, as expected, the threshold scan, since it injects multiple different charges in every single pixel. From Section 7.2.8 it is known, that the data, as currently taken during wafer probing, does not yield sufficient information to substitute this test. However, one idea, that is currently investigated, is a substitution of the analog scan or digital scan with data acquired during threshold scan. Removal of the analog and digital scan is expected to save **2 min** per chip[88]. The second most time-consuming scan is the pixel register scan, explained in Section F.1.11, which has a high correlation with the digital scan result. This scan has proven to be replaceable by information acquired during a digital scan or threshold scan [89], saving **2 min 20 s** per chip. The IREF trimming routine involves the Keithley source meter and is therefore rather slow. The Keithley voltage and current measurement routines contain multiple wait commands for the voltages and currents to settle after chip, probe card and power supplies are configured correctly. With time optimization, the routines, which heavily use the Keithley source meter, such as "Trim Iref", "Trim LDO Registers", "Measure injection capacitance", "Measure injection DACs and ADC", "Measure Chip Mux Voltages", "Measure Chip Mux Currents", "Measure probe card voltages" and "Measure GND Offsets" are expected to reduce their measurement time by 30 %, saving another **2 min** per chip. The fourth most time consuming scan is the temperature calibration scan, which according to Section 7.2.7 is suboptimal to be carried out during wafer probing. Removing this scan will save another **1 min 40 s**. The measurements of injection capacitance, injection DAC and ADC can also be reduced, by lowering the sample points per chip. Furthermore, offline analysis for the threshold scan can be added, which would save another **30 s** per chip. All in all, the time reduction potential for ITkPixV2 wafer probing is still large. Assuming the time reductions from removing the analog scan, digital scan, pixel register scan, and temperature calibration and reducing the Keithley measurement time by 30 %, a test time per chip of 13 min would

Scan Name	Time [s]	Time [%]	Scan Name	Time [s]	Time [%]
threshold scan	157.95±24.83	12.32±1.94	measure chip MUX currents	31.84±3.14	2.48±0.24
pixel register scan	142.89±18.37	11.14±1.43	test data-merging	28.73±58.66	2.24±4.57
trim IREF	112.77±8.88	8.8±0.69	register test	27.02±2.44	2.11±0.19
measure temperatures	101.64±20.89	7.93±1.63	measure probe card voltages	21.38±1.13	1.67±0.09
trim LDO registers	87.98±4.63	6.86±0.36	aurora lane 0 test	19.7±17.17	1.54±1.34
measure injection capacitance	82.67±9.27	6.45±0.72	aurora lane 1 test	19.51±8.55	1.52±0.67
shunt regulator IV curve	79.74±12.84	6.22±1.0	aurora lane 2 test	19.35±1.48	1.51±0.12
analog scan	76.3±9.18	5.95±0.72	aurora lane 3 test	19.33±1.48	1.51±0.12
measure injection DACs and ADC	65.08±18.41	5.08±1.44	ring oscillator scan	18.37±1.37	1.43±0.11
power measurements	63.95±5.39	4.99±0.42	write E-fuses	9.56±1.19	0.75±0.09
measure chip MUX voltages	44.62±4.63	3.48±0.36	measure GND offsets	8.44±0.43	0.66±0.03
digital scan	41.79±4.64	3.26±0.36	chip ID test	1.62±1.19	0.13±0.09
total time per chip [s]	1278.39±128.46		total time per chip [min]	21 min18 s±2 min8 s	

Table 7.2: Summary of test times per chip in descending order

be achievable, which results in a test time per wafer of **28 h 36 s**. This test time would be acceptable to get a practical reduction of the wafer probing time.

Despite the goal of minimizing scan time per chip, there are a few ITkPix blocks, that should be covered additionally. All of the following measurements are simple voltage or current measurements, which do not add significantly to the current time budget. The list of tests to be added includes:

- **Initial test of Current consumption:** In Section 6.3.1, a ITkPixV1.1 with increased analog current consumption was labeled green. This can be prevented in the future by measuring the analog and digital current consumption right after power-up in LDO mode.
- **Test Overvoltage Protection:** In Section 7.2.3 a shunt regulator IV-curve is measured. The IV-curve exhibits a linear relation between voltage and current. Currently only the operating range of the shunt regulator IV-curve is measured. ITkPixV1.1 features an additional over voltage protection circuit, which dumps additional access current, in case Vin approaches 2 V.

All in all the current wafer probing setup has a solid routine, discussed in Section 7.1 which has been copied to multiple global test sites in Berkeley, Paris and Glasgow. In addition to that it has exceeded

the expectation concerning yield, as discussed in Section 7.2, with some room for improvements discussed in this Section 7.3. In general the wafer probing campaign has brought valuable insights for ITk production and could be executed as is upon the arrival of ITkPixV2.

CHAPTER 8

Conclusion and Outlook

The HL-LHC upgrade starting in 2026 will provide an opportunity for new high-energy physics experiments, but also present challenges for its tracking detectors. Particularly the pixel detectors close to the interaction point will be subjected to a significantly higher particle rate and radiation damage. To address this, new high resolution, radiation tolerant readout chips are being developed, and efforts are being made to establish ITk production processes to assemble the final ITk detector. ITk is the redesign of the current inner detector of the ATLAS experiment. ITk wil employ only silicon tracking detectors. Its inner five layers will consist of hybrid pixel detectors, that use readout chips, and sensors for tracking. In this thesis, the verification, characterization and mass testing of the ITkPixV1.1 readout chip for the ITk upgrade at the HL-LHC has been presented.

The ITkPixV1.1 is a full-scale prototype of the future readout chip for ITk. Its design and functionality have been described in detail. The signal generation process in the tracking detector and the design of the silicon hybrid pixel detector, which incorporates ITkPix, have also been outlined. A new BDAQ53 testing environment and accompanying software have been introduced in order to verify the performance of ITkPixV1.1. The BDAQ53 testing environment, in combination with the RD53B interface cards, provide a robust platform for verifying the performance of ITkPixV1.1.
During verification, ITkPixV1.1's digital logic in pixel matrix and chip bottom has been tested in simulation and continuous DAQ compatibility has been ensured using continuous integration in the BDAQ53 repository.

During ITkPixV1.1 characterization, individual chips have been tested and the general performance of analog and digital blocks has been verified. At first the specifications, have been introduced, stating, that ITkPixV1.1 should be capable of operating in a temperature range between −40 °C and 40 °C. This has been verified in a campaign, where all chip reference voltages and currents have been measured int he corresponding temperature range.From this it has been concluding that the main reference current "IREF" is sufficiently stable over the full temperature range.
Another specification concerns ITkPixV1.1's analog front end properties, which translates the charge generated by a traversing particle into a digital signal. This specification defines that the chip should be capable of detecting a charge of less than 1 200 e^- less than 25 ns after a particle's traversal, while detecting false positives, due to noise hits only once in 10^6 cases. The total detection threshold dispersion over the whole chip must not exceed 60 e^-, with less than 2 % disabled pixel, while

consuming between 3 µA and 5.5 µA per analog front end. It has been verified, that these specification is met at −40 °C.

In addition, a few ITkPixV1.1 bugs have been discovered. One of the bugs relates to data-merging, which is a feature, that enables a primary ITkPixV1.1 to receive data from a secondary ITkPixV1.1 and incorporate that data in its data output stream. During the verification of data-merging it has been discovered, that data with a certain phase relation between the data output of the secondary and data input of the primary chip is not correctly merged. This is related to an error in the resampling logic of the incoming signal, which will be fixed in ITkPixV2.
Another bug, that relates to a time dependent detection threshold, has been discovered. The detection threshold is modulated by up to 200 e^- with a 40 MHz and 10 MHz component, which are frequencies, that are commonly used in the pixel matrix. One possible coupling point has been identified at the transition between analog front end and digital pixel logic. However it is likely, that this is not the only coupling point, which led to the decision to not address this bug in the ITkPixV2 submission.

During wafer probing, the functionality of 6600 ITkPixV1.1 is tested. The setup has been introduced and the software for testing, analysis and database interfaces has been developed in the scope of this thesis. The total yield of 86 % has been achieved, which is a significant improvement over 60 % during RD53A wafer probing, despite stricter requirements. In the future, four probe sites will use the wafer probing setup and software developed during this thesis, to probe ITkPixV2 for ITk production. In the event, that one probe site will fail, the reduction of probe time has high priority, which has been discussed and a reduction from 48 h to 30 h per wafer is possible. In addition, two new tests are recommended to be added to the testing routine.

Future steps related to this work is the quantification of the oscillating detection threshold on ITk's tracking performance, the inclusion of ITkPixV2 drivers into the BDAQ53 framework and the verification on whether the addressed bugs are fixed in ITkPixV2. All in all the work in this thesis has significantly contributed to the development of the ITkPixV2 chip, and thus to the development of the new ITk of ATLAS at the HL-LHC.

APPENDIX A

High Current Bug in ITkPixV1

Within the first few days of arrival of ITkPixV1 it was clear, that the readout chip did not behave as expected. When initially turned on, a current consumption of a few hundred mA is expected. However the current consumption of the digital part turned out to be consistently higher by a factor of ten. What is causing this effect? Resistors, capacitors, register settings were checked, but in the end it turned out to be the novel 4 bit multibit latch inside the digital pixel logic, which is causing two connected issues.

1. High digital current consumption
2. Missing hits dependent on their ToT

Each pixel has multiple of these multibit latches, which are responsible for storing the digitized ToT values to store multiple consecutive hits. The design of these latches was custom and was logically incapable of storing more than two bits without generating a direct connection between VDDD and ground. Ergo large current. In addition to that, as soon, as a second bit was enabled, the other bits became undefined and had a high probability of turning one [90].

Above feature explains the high current consumption, but not yet the missing hits at certain ToT values. Let's consult Figure A.1 for this.

Figure A.1 from left to right shows an ITkPixV1 with a symbolic (not to scale) single pixel marked. This indicates an exemplary position for one of the faulty multibit latches. The reader may be reminded, that each pixel has multiple of those latches, which actually makes this a distributed issue in every single pixel. The center time-voltage graph shows the ToT signal in front of the counter, which writes to the multibit latch. On the right two multibit latches are visible, one with value 0b0111 (decimal 7), the other with 0b1111 (decimal 15). The graphic indicates the high probability of additional bits being switched on if more than one bit in the multibit latch is active. In this example a ToT value of 7 gets turned to ToT 15. This is particularly unfortunate, because ToT 15 is not a valid measured value, but the code for "no hit", which means this hit will be removed from the hit data output, leading with high probability to hitloss, if any ToT value is recorded, which is not (0, 1, 2, 4 or 8) [91].

As a consequence, ITkPixV1.1 was submitted with a change to one of the metal layers, effectively changing the 4 bit multibit latch to a 1 bit multibit latch, to prevent high current flow and rendering the regular ToT inoperational. In ITkPixV1.1 the ToT is always 7 allowing pure binary readout.

To enable charge measurement the precision ToT can be used in both ITkPixV1 and ITkPixV1.1. The precision ToT is located in the chip bottom and offers a sampling frequency of 640 MHz in stead

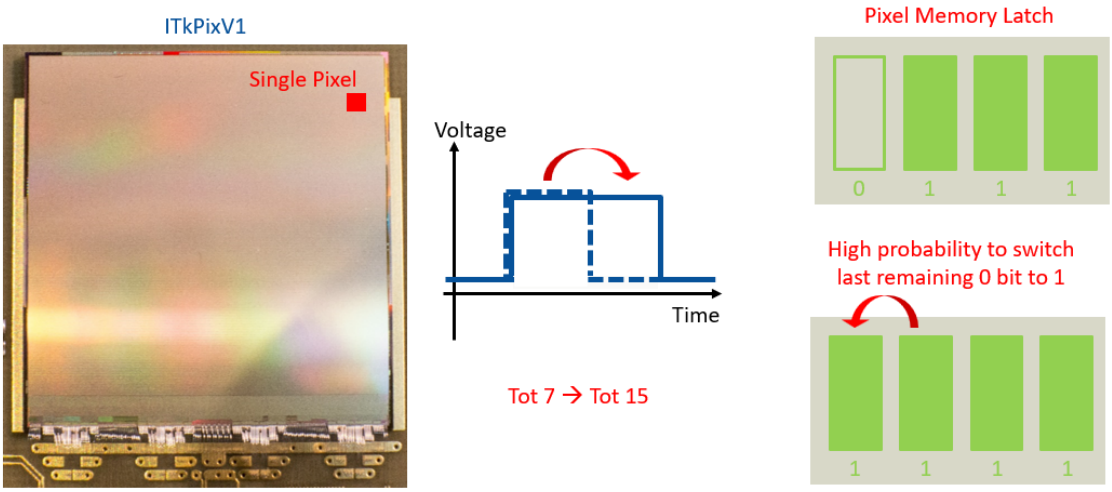


Figure A.1: Process of loosing hits in a single pixel, due to faulty multibit latch.

of the 40 MHz of the pixel ToT. This increased sampling frequency and especially the larger counter latches require additional space, which only allowed to place four precision ToTs per core column. Therefore a quarter of all pixels inside a core column is always connected to one precision ToT.

Figure A.2: A graphic summarizing the concept behind a precision ToT scan.

Figure A.2 shows on the left an image of ITkPixV1 overlayed with the precision ToT connection pattern per pixel core. On the bottom left the location and sum of all precision tot circuits is indicated by the red bar. The top right shows the 11 bit latch of the precision ToT (ptot), with the bottom right summarizing the advantages compared to the regular ToT multibit latch. The idea behind using the precision ToT is to activate always four pixels per core column (one per number in top left image), measure the precision Tot for the four pixels, then activate different four pixels and repeat, until the whole core column and therefore all pixels an a readout chip are tested. A resulting precision ToT distribution from an analog scan can be seen in Figure A.3.

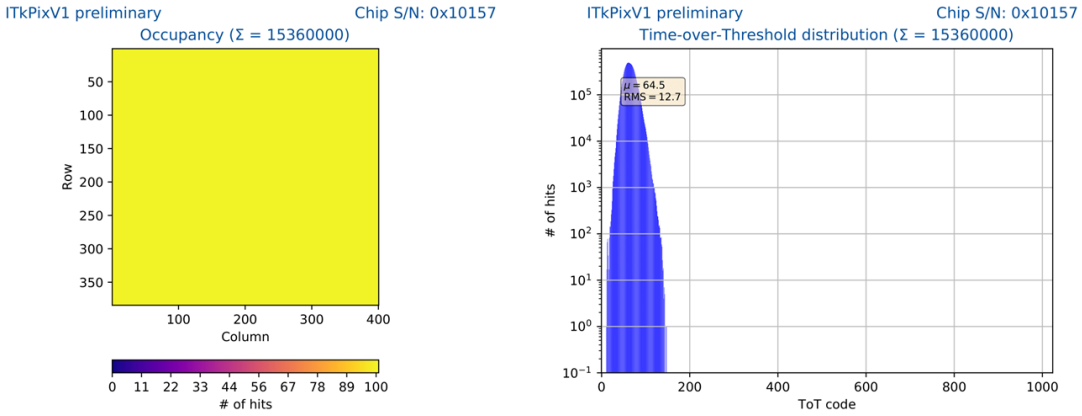


Figure A.3: A successful precision ToT analog scan.

On the left a 2D spacial view on an ITkPixV1 is visible. The homogeneous surface indicates, that all pixels have received the same - expected - amount of hits. On the right a precision ToT histogram is visible. The high granualrity on the x-axis indicates already the increased precision of this method. The logarithmic y-axis indicates the amount of hits with the corresponding precision ToT value as indicated on the x-axis.

This method only works with injection based scans, since this is the only time where the position information can be stored. During source scans or test beam, the amount of active pixels would have to be drastically reduced (four pixels per core column) or position information to be sacrificed.

APPENDIX B

Missing Hits in ITkPixV1 & ITkPixV1.1

During the development of a noise tuning or threshold baseline tuning [92] for ITkPixV1.1, a systematic study on the hit occupancy based in the length of consecutive trigger is conducted. Figure B.1 shows the amount of consecutively sent triggers on the x-axis and the amount of received hits, during digital injection for a single pixel in %. A saturation of occupancy at 100 % to triggers longer than three is observed. For less than four consecutive trigger, the occupancy is dropping towards one. The expected behavior would be that the shown occupancy is independent of the trigger length always at 100 %. The observed behavior is caused by a missing reset of the trigger table, if a trigger shorter than four is sent. In this case the trigger id stays in the trigger table and the next trigger, sent with the same trigger id is ignored. This bug can easily circumvented during testing, by sending longer trigger patterns, in addition to that, the bug is understood and expected to be fixed in ITkPixV2.

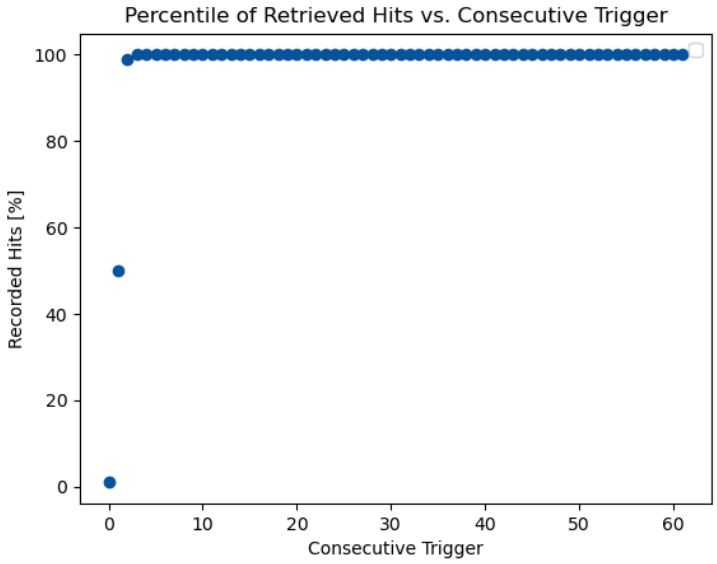


Figure B.1: Recorded Hits vs. Consecutive Trigger

APPENDIX C

Monitoring Data Frame Bug in ITkPixV1 & ITkPixV1.1

Monitoring Data, is data, which is injected periodically in the regular data stream to monitor chip parameters, such as analog front end currents, supply voltages, chip temperature, or total received chip dose. In general, every parameter, which can be retrieved using a register read command can also be transmitted using the monitoring data block. There are seven registers, which can be monitored in parallel. In addition to that there is a chip register, which controls the frequency of the injected monitoring frames. This feature is used to monitor chip health and performance over time, without the need to block command bandwidth. In the case of BDAQ53 this data is stored in a dedicated fifo which is then periodically transmitted to the computer. Already during the testing of RD53A the necessity to receive all this data continuously on the PC side was questioned and therefore a filter for monitoring frames was implemented in firmware. There are four types of 64 bit monitoring frames, one frame always contains two register information "M" refers to a monitoring register read, "A" refers to a manual register read:

1. MM: A frame containing two monitoring data frames
2. MA: The first half of the frame contains monitoring data, the second half contains the answers to a manual read request.
3. AM: The first half of the frame contains contains the answers to a manual read request, the second half contains monitoring data.
4. AA: A frame containing answers to two manual read requests

In ITkPixV1 and ITkPixV1.1 the "AA"-frame and "MM"-frame are unfortunately not distinguishable via their headers. Therefore an additional filtering mechanism was implemented in BDAQ53. This filtering mechanism consists of a software part, which configures all seven monitoring registers to be register 511, which is not a real register in RD53B. In BDAQ53 firmware a filter on address 511 is then applied, filtering out all frames, which contain only data for register 511. This simple filter is luckily possible due to the simple frame structure of monitoring data. This bug is expected to be fixed in ITkPixV2.

APPENDIX D

Scan Chain Investigation

A scan chain is a quick way to evaluate whether all flip-flops and combinatorical logic within a circuit work. It is a testing feature, as usually employed in industry, as part of design for testing [93]. Since ITk will consist of 33092[94] ITkPixV1.1, a fast and reliable way to determine the functionality of each ITkPixV1.1 digital logic is necessary. For the implementation of a scan chain the only additional feature necessary at the input of each flip flop is a multiplexer, which can switch between scan chain input and functional data input. In Figure D.1, the multiplexer is represented by the green trapezoid. The connections of the flip-flops in the case of an activated scan chain mode is shown in blue. The scan chain mode is activated by the global scan chain enable bit (SE). In this mode, data can be clocked in the scan chain by applying either a one- or zero-to the scan chain input and applying a clock pulse over the red "Pulse Clock" line to all flip-flops, ensuring the input of each flip-flop is propagated to its output. In this way, all flip-flops form a large shift register, where the D and Q points are defined by triggering clock pulses equivalent to the length of the scan chain. The procedure of clocking in the data is shown in Figure D.2 as shift cycle 1.

Figure D.2 shows the fourteen signals that must be controlled during scan chain operation for RD53B chips. CLK0 and CLK1 are the two clocks for each of the two scan chains implemented in the chip bottom of RD53B, the inputs of the scan chains are the signals called SC IN 0 and SC IN 1. The SE is the scan enable bit as shown in Figure D.1. The signals PMTM (Pixel Matrix Test Mode), TEST MODE, BYPASS MODE, CHIP ID 0, CHIP ID 1, CHIP ID 2, CHIP ID 3 are slow signals, which influence the combinatorical logic on RD53B, which must be defined during the multi clock capture cycle. The multi clock capture cycle is defined as the time when the SE signals gets pulled low and the flip-flops go back to their logic connections. If now one clock pulse is applied, the whole logic interacts and propagates their values back to the flip-flops. When shift cycle 2 is applied, SE is pulled high again and the data from the flip-flops is shifted out and can be monitored on the SC OUT 0 and SC OUT 1 and compared to an expected, simulated output. ITkPixV1.1 features 1255 test pattern, with a length of 284 032 bit and 284 033 bit.

D.1 Scan Chain

The working principle of a scan chain is explained in Section D. During ITkPixV1.1 scan chain testing, the shifting frequency, powering and correct connection of all pins is important. The development of a suitable scan chain implementation with BDAQ53 has started 2021, with the arrival of ITkPixV1.1.

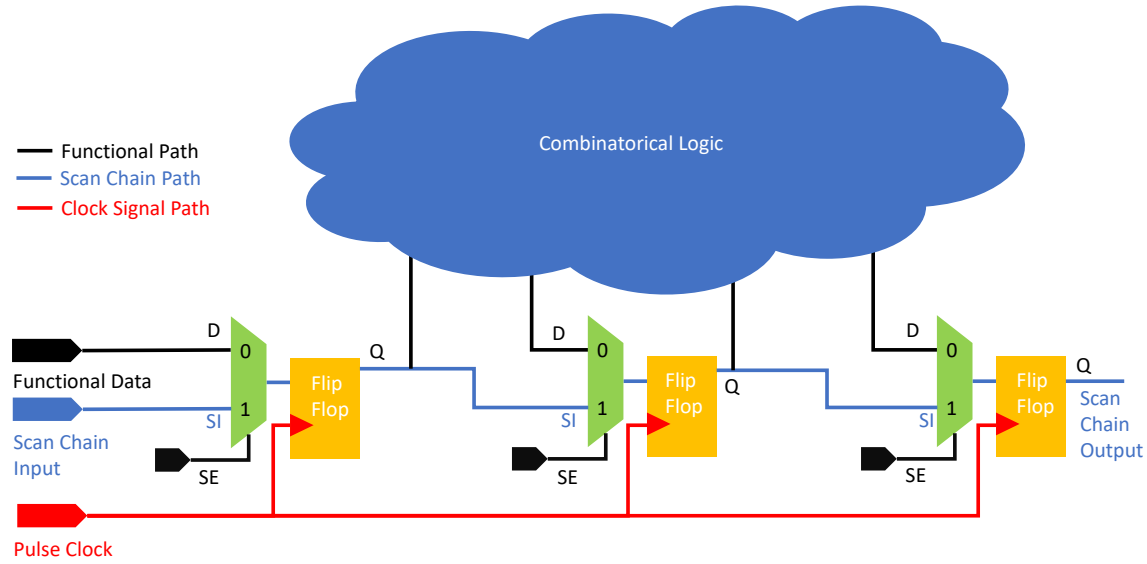


Figure D.1: A schematic diagram of a scan chain as used in RD53B.

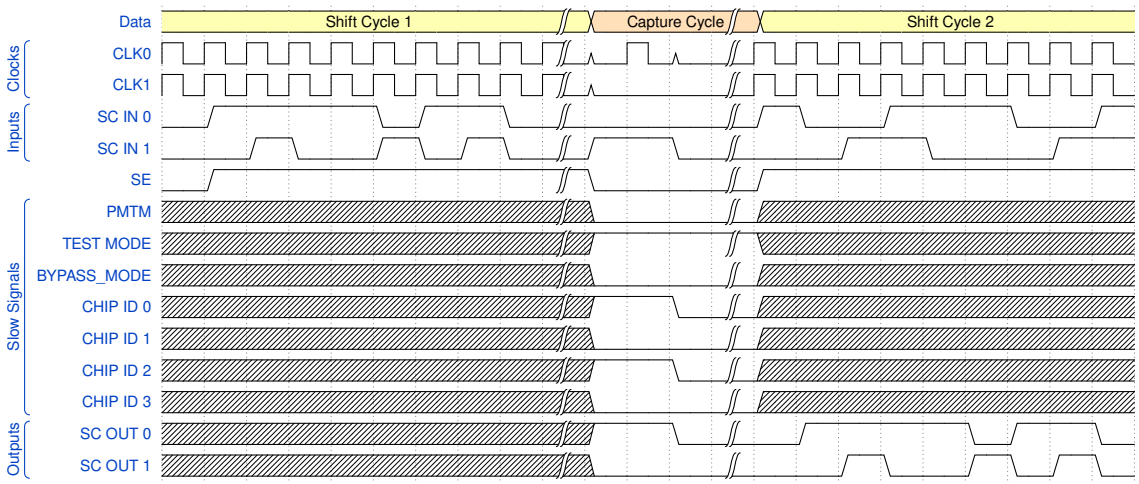


Figure D.2: A schematic wave diagram of shifting in data and applying a multiclock cycle in RD53B.

Until the submission of this document no working BDAQ53 implementation for the ITkPixV1.1 scan chain is reached. The following tests are conducted to debug the BDAQ53 scan chain. Figure D.3 shows an image of the scan chain setup.

The PMOD bench on the bdaq board is responsible for the slow signal control and runs at 3.3 V, which is sent through a level-shifter, which uses VDDD as a reference, to the slow control pins on the Single-Chip Card. The scan enable signal (SC enable) is hereby soldered directly to the trace on the Single-Chip Card, since it was originally planned to be controlled via a single ended line on the display port. The yellow scan chain input transmits the differential input clock and data signals form BDAQ53

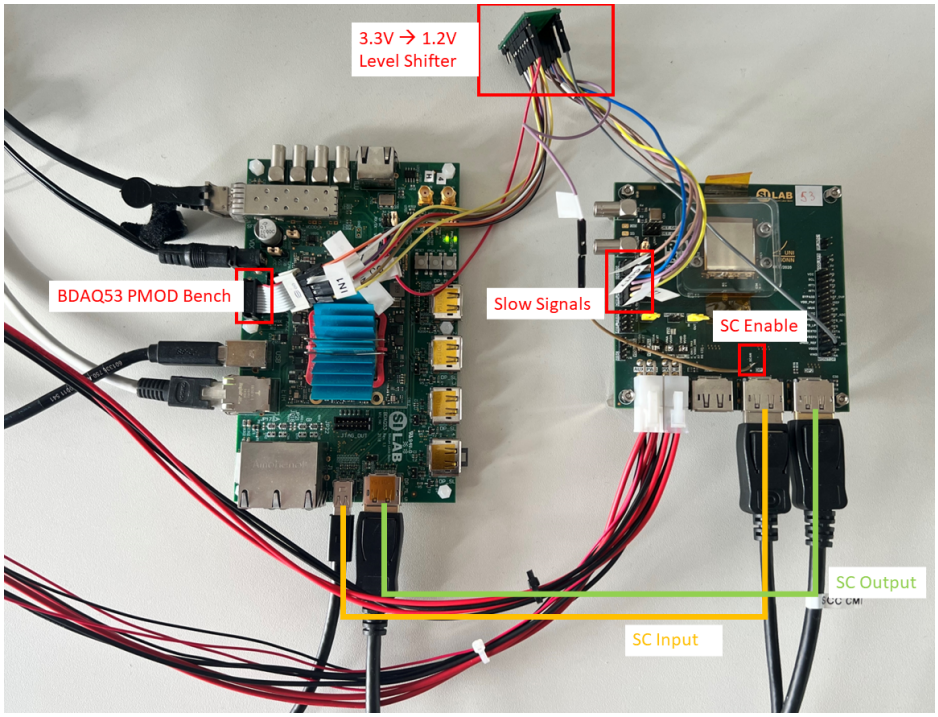


Figure D.3: A foto of the BDAQ53-ITkPix scan chain setup.

to ITkPixV1.1, while the green scan chain output transmits the output patterns back to BDAQ53.

D.1.1 Loading and Unloading

According to the RD53B manual [44], the optimal frequency to load the scan chain is 20 MHz. With a clock duty cycle of 0.48 % and a phase shift of 117° in relation to the rising edge of the input channels. Figure D.2 references two inputs, two outputs and two clocks, as well as multiple slow control pins. These three pair signals are driven in sync, with a fixed timing reference. This ensures, that chain 1 and chain 2 are loaded in parallel. At first the correct shifting into the ITkPixV1.1 scan chain is ensured. This is achieved by loading both chains in parallel, without applying a multi clock capture cycle. The chains are then unloaded to ensure that all defined bits have the desired bit setting. This is achieved, while paying attention to the different chain lengths and adjusting the shift in and shift out algorithm accordingly. It is ensured, that all input pattern are written correctly and can be read back correctly. Figure D.4 shows the two scan chain input signals, in red and green, with the scan chain clocks in yellow and cyan. The pattern written to the chip corresponds to $0b00110011$. The red and green data signals are shifted by one bit respectively, due to the different scan chain lengths. The shift frequency for both clocks is 10 MHz, which is half the optimal frequency, to mitigate power-spikes during shifting. Figure D.5 shows one data and one clock signals as measured deferentially using math mode. The peak to peak voltage is 1.9 V as set on the BDAQ53 board.

Originally the scan chain patterns are stored and loaded in a text file, which is large and inefficient to store in memory. For that reason the spf (text file) is cast into a h5 binary file, which is quick to load, efficient to store and features a preprocessed version of the scan chain vectors as used by the

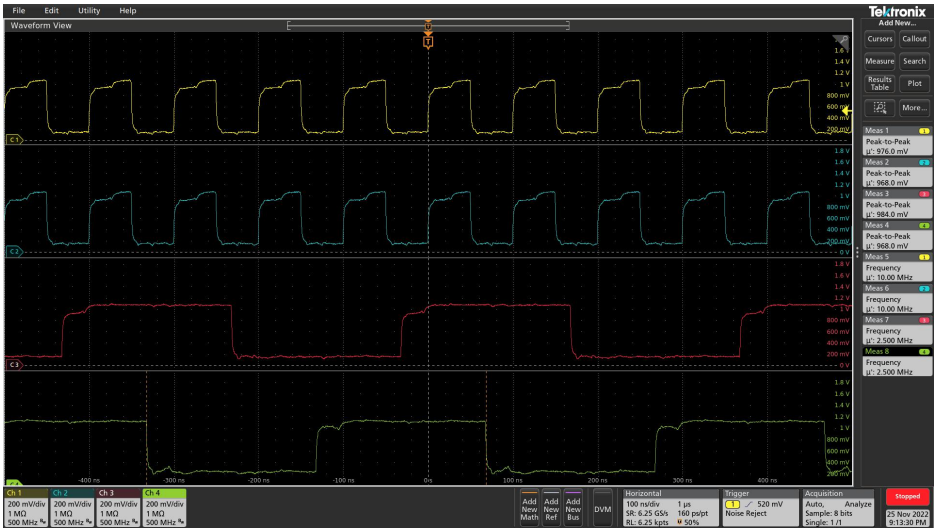


Figure D.4: Waveforms of the scan chain input as generated by the BDAQ53 board. Differential signal measured single ended. Yellow: Clock 1 Cyan: Clock 2, Red: Input 1, Green: Input 2

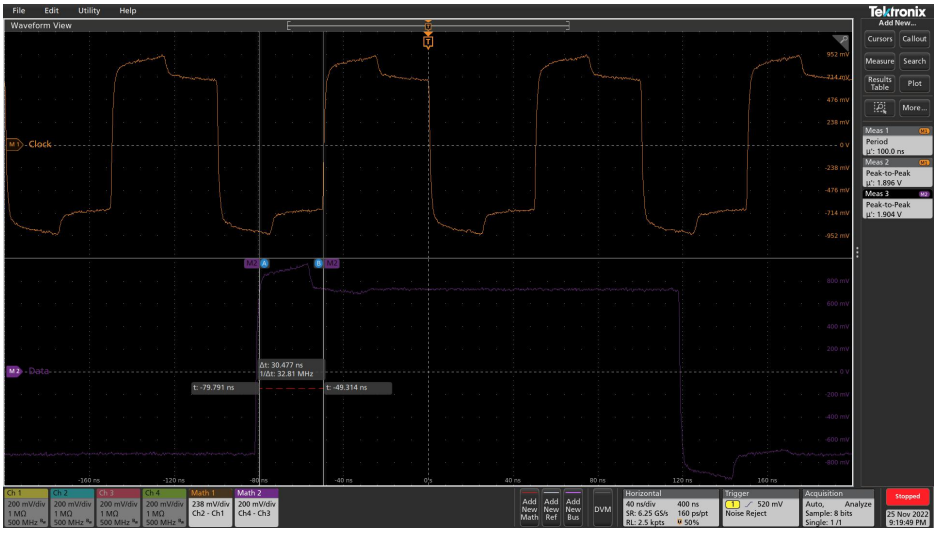


Figure D.5: Waveforms of the scan chain input as generated by the BDAQ53 board. Differential signal measured deferentially. Orange: Clock 1, Violet: Data 1

BDAQ53 scan chain. The shifting-in is tested for multiple frequencies, between 5 MHz and 20 MHz. All shifted read back vectors correspond to the same vectors, as shifted in, at all tested frequencies.

D.1.2 Multiclock Cycle

The multi clock capture cycle is the part of the scan chain, where the flip-flops are connected in their combinatorical logic state, as shown in Figure D.1, by disabling the SE bit. In this state, single, or double clock pulses are applied, while redefining the slow signals in Figure D.2. All flip-flops now interact as they were in operation and gain a new output state Q. This chain is then shifted out and

compared to a vector from simulation. Originally the control of the slow signals was exclusively planned to be used on the probe card, via its I^2C interface. This is proven to be too slow, which is why the PMOD bench on the BDAQ53 board is utilized to control the slow signals on the Single-Chip Card, as shown in Figure D.3. Please note that the BDAQ53 board is running at 3.3 V, while ITkPixV1.1 is running at 1.2 V supply voltage. Therefore a level-shifter is utilized to forward the signals between BDAQ53 board and Single-Chip Card. The multi clock capture cycle is tested for all existing pattern, it is ensured, that the timing of all slow signals is correct and all slow signals are connected to the correct pins. In this stage it is discovered, that after the application of the multi clock capture cycle some of the shifted out pattern do not correspond to the simulated vector as received by the ITkPixV1.1 scan chain designer.

D.1.3 Debugging

At this stage it is assumed, that loading and unloading cycles work as expected. During spring of 2022 1234 of 1255 test pattern are tested successfully. This is presented during one of the closed designer meetings. The test is run at 10 MHz in shunt LDO mode. It is assumed, that BDAQ53 has timing issues and has insufficient control over the flip-flop settings in ITkPixV1.1. On September 28th 2022 CMS reports a successful run of all test patterns in their chip CROCV1 [95]. Their setup incorporated the following changes compared to the previous ATLAS presentation from our side [96]:

1. Loading and Unlaoding at 8 MHz
2. Independent powering of PLL cml, VDDD and VDDA
3. Operating their chip in direct powering with sensing, without LDO or shunt LDO

All of the above changes are additional changes to the runs conducted previous to this presentation on ITkPixV1.1. In this thesis all of the above changes are incorporated into these measurements. With equal success as in spring 2022. The same 21 vectors, listed in Table D.1 fail, in direct powering mode, as in shunt LDO mode, as well as at 5 MHz, as well as at 10 MHz and 20 MHz. In LDO powering more than the 21 mentioned vectors fail.

33	1156	1157	1160	1162	1166	1167	1169	1171	1206	1207
1212	1213	1215	1223	1224	1226	1229	1231	1232	1234	

Table D.1: Failing scan chain vectors

The following other actions are tkaen to investigate the failures:

- During loading of all scan chain vectors a ≈10 µs VDDD drop of 400 mV is observed. To mitigate the influence of this effect, two large capacitors of 4 700 µF are soldered to the VDDD and VDDA supply rails, stabilizing both voltage rails on the Single-Chip Card.
- To exclude timing issues between shift clock and shift data a configurable delay with 1.5 ns was added and scanned vs all 1255 pattern. No delay yielded more than 1234 successful pattern.

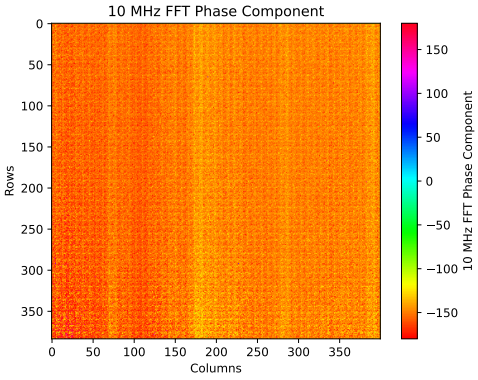
It is observed, that consistently the same patterns fail, but with slightly different failing bits each time. This is a hint to a random component in the system, which could e.g. be introduced by significant

voltage drops, which occur when certain multi clock capture cycle cycles are applied in combination with certain patterns. All in all the scan chain can be used to test ITkPixV1.1s functionality with reduced coverage, by ignoring the systematically failing patterns.

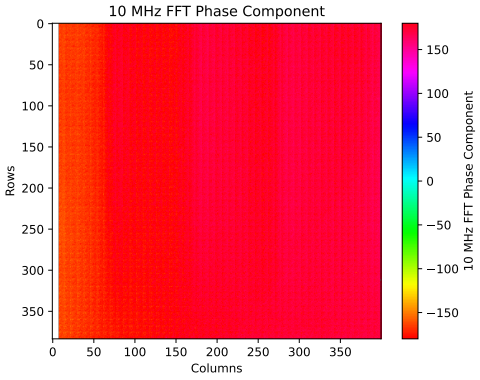
APPENDIX E

Additional Plots

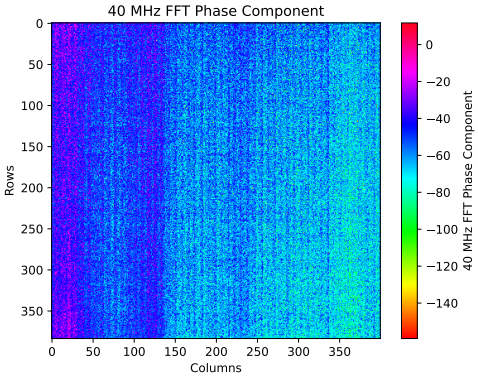
This chapter holds additional plots, discussed in Section 6.3.2.



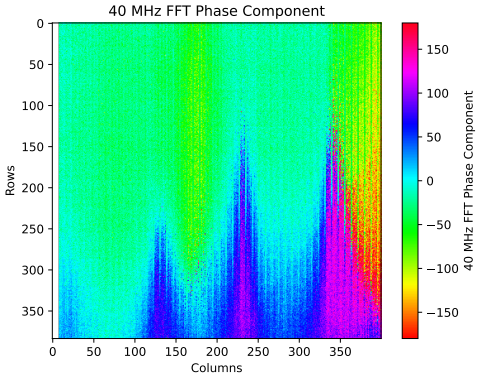
(a) FFT phase component for Figure 6.27(c)



(b) FFT phase component for Figure 6.27(d)

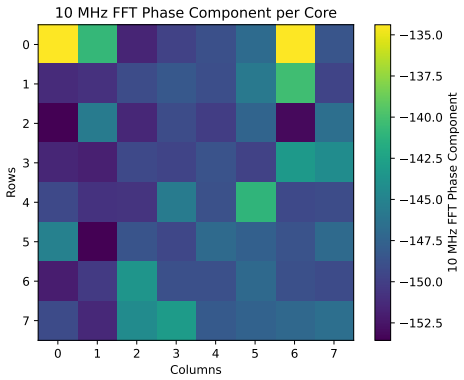


(c) FFT phase component for Figure 6.27(e)

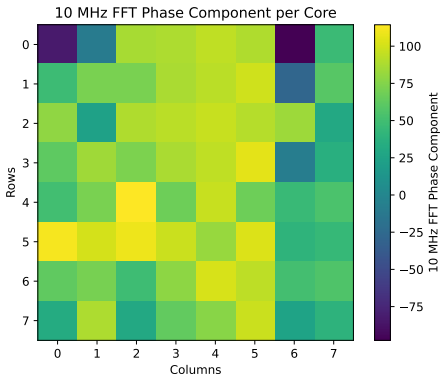


(d) FFT phase component for Figure 6.27(f)

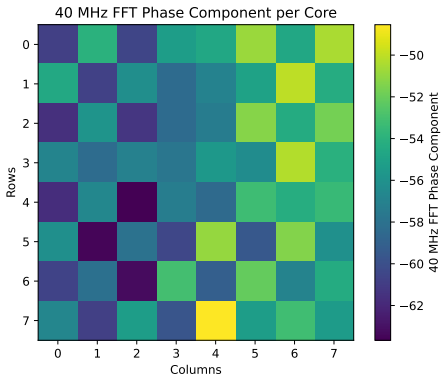
Figure E.1: detection threshold oscillations phase shift over the full pixel matrix



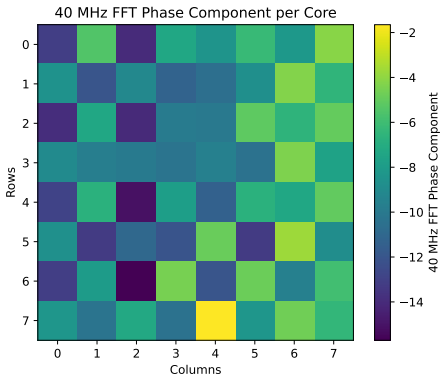
(a) FFT phase component averaged per core for Figure E.1(a)



(b) FFT phase component averaged per core for Figure E.1(b)

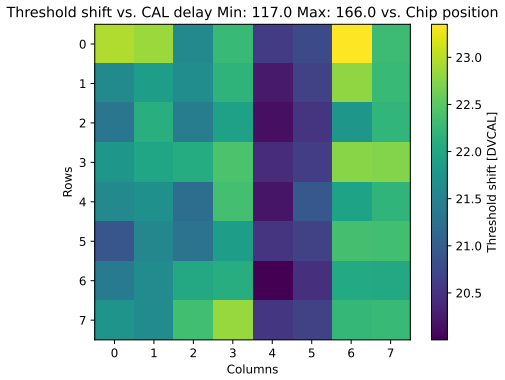


(c) FFT phase component averaged per core for Figure E.1(c)

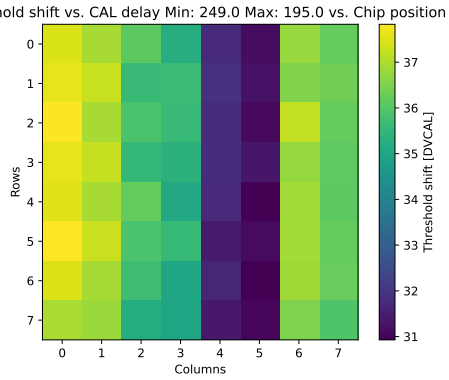


(d) FFT phase component averaged per core for Figure E.1(d)

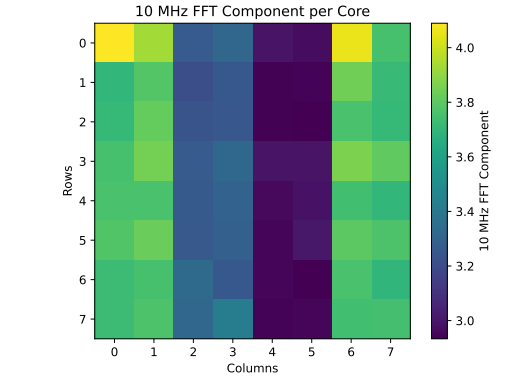
Figure E.2: detection threshold oscillations phase shift averaged over pixel core



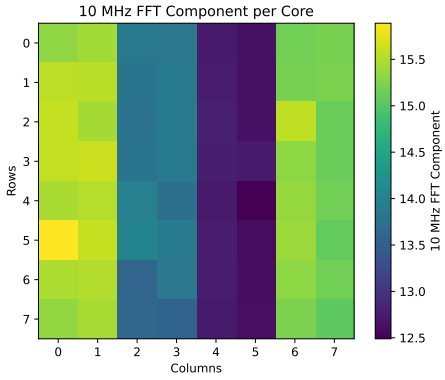
(a) Maximal detection threshold variation on a per core base for bare chip with double isolation 0x16253



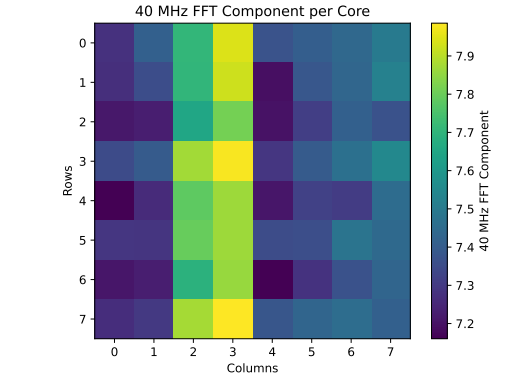
(b) Maximal detection threshold variation on a per core base for a chip with sensor andsingle isolation 0x13156



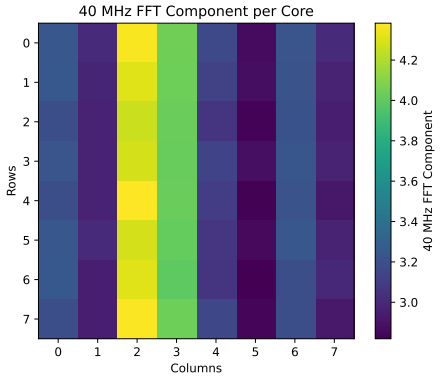
(c) 10 MHz amplitude from Fourier transformation per core for bare chip with double isolation 0x16253



(d) 10 MHz amplitude from Fourier transformation per core for single isolated chip with sensor 0x13156

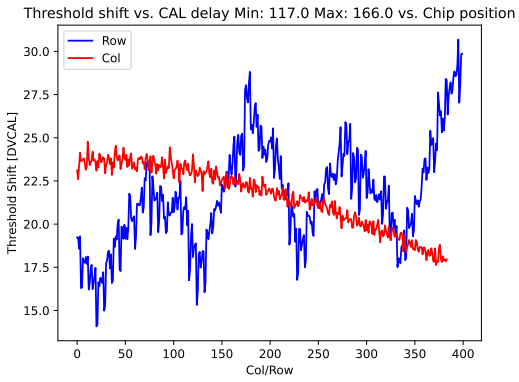


(e) 40 MHz amplitude from Fourier transformation per core for bare chip with double isolation 0x16253

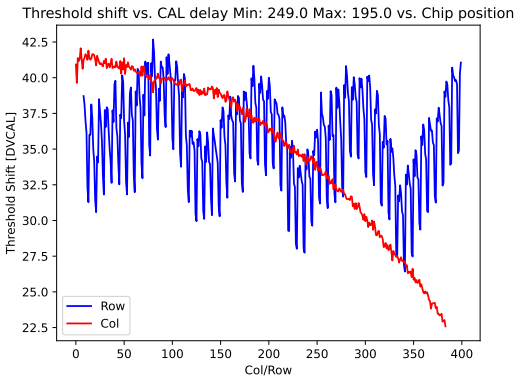


(f) 40 MHz amplitude from Fourier transformation per core for single isolated chip with sensor 0x13156

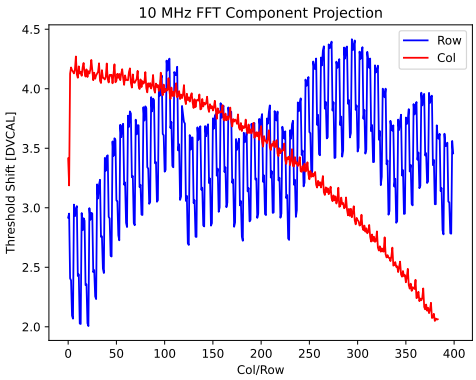
Figure E.3: detection threshold variation on a per core base



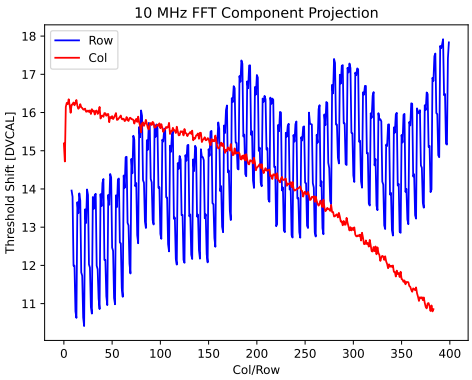
(a) Projection of Figure 6.27(a)



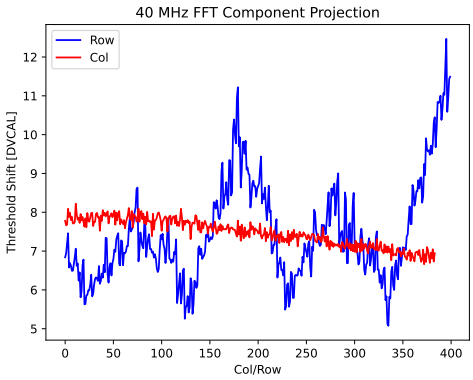
(b) Projection of Figure 6.27(b)



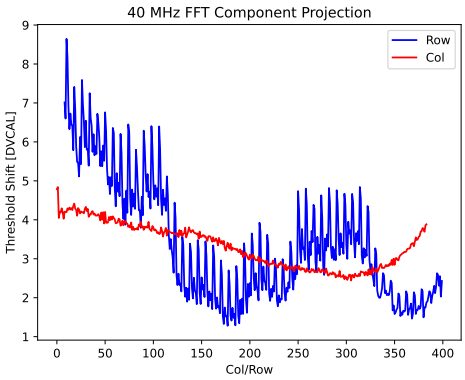
(c) Projection of Figure 6.27(c)



(d) Projection of Figure 6.27(d)



(e) Projection of Figure 6.27(e)



(f) Projection of Figure 6.27(f)

Figure E.4: Projections of Figure 6.27 on the column and row axis

APPENDIX F

Waferprobing Appendix

This is a Section to document the wafer probing tests and cuts, as conducted during the first two wafer batches during ITk pre-production. The wafer probing procedures are explained in Section 7.

F.1 Routine Appendix

This Section contains an explanation of all wafer probing routines, which are not discussed in Section 7.

F.1.1 Power on ITkPixV1.1

The initial step of each test is the powering of the corresponding ITkPixV1.1. Here, the initial power consumption is measured to detect short circuits in the analog (VDDA) or digital (VDDD) power domain. Since ATLAS ITk employs serial powering all wafer level tests are conducted in shunt LDO mode at 1.6 V.

F.1.2 Measure probe card voltages

The probe card features a multiplexer to measure the voltages shown in Table F.1. These are all measured, to find conspicuities in the chip behavior.

F.1.3 Chip ID test

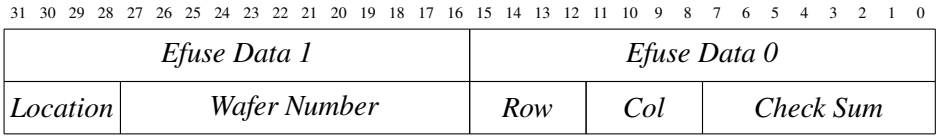
Each ITkPixV1.1 has four address bits, which can be externally set by wire-bonding specific pads to ground. This allows multiple ITkPixV1.1 on the same command bus to be addressed individually. The corresponding Chip ID is part of each command, which is sent according to the "Command and Trigger Encoding" Table in the RD53B manual [44]. To ensure, that each Chip ID bit is functioning, four register read commands are send. For each test, the probe card pulls a different chip ID bit to ground, making it addressable with the corresponding ID.

Setting	Selected Input	Setting	Selected Input
0	analog LDO input voltage	12	shunt regulator offset voltage
1	digital LDO input voltage	13	shunt regulator low power offset voltage
2	direct analog input voltage	14	voltage drop over analog R_{shunt}
3	direct digital input voltage	15	voltage drop over digital R_{shunt}
4	direct command line driver input voltage	16	VREFA (Figure 3.5)
5	direct PLL input voltage	17	VREFD (Figure 3.5)
6	direct pre regulator input voltage	18	Over voltage protection reference voltage
7	current multiplexer output	19	analog reference ground
8	voltage multiplexer output	20	digital reference ground
9	R_IREF (Figure 3.5)	21	BDAQ53 ground
10	NTC on probe card	22	E-fuse supply voltage
11	VREF_ADC (Figure 3.5)	23	analog reference ground

Table F.1: A summary of all pins accessible by the probe card multiplexer

F.1.4 Writing E-fuses

The E-fuses in ITkPixV1.1 are used to uniquely identify each chip after wafer probing by software. For this purpose, they are written with the corresponding ATLAS serial number. Each E-fuse has 32 bit. The encoding is as follows:



The location encoding corresponds to the following sites: 0 –> unprobed, 1 –> Bonn, 2 –> Glasgow, 3 –> Paris, and 4–> LBNL. The wafer number is taken from a central database, whereas the column and row correspond to the column and row location of the chip on the wafer. The check sum is calculated based on a standard Hamming codec, as described in the itkpix-efuse-codec repository [97]. After writing, all E-fuses are read and documented whether the write procedure was successful.

F.1.5 Measure Chip Mux Currents

Section 7.1 mentions the detection and monitoring functions of ITkPixV1.1. All currents accessible through this block are measured directly through the source meter as shown in Figure 7.1. The measured currents are summarized in Table F.2. The setting column refers to the address of the multiplexer input.

F.1.6 Measure Chip Mux Voltages

All monitored voltages, accessible via the monitoring mux, mentioned in Section 7.1 are measured using the source meter shown in Figure 7.1. The measured voltages are summarized in Table F.3. The

Setting	Selected Input	Setting	Selected Input	Setting	Selected Input
0	IREF main ref. current	11	Capmeasure parasitic	22	DIFF FE Preamp Top-Left
1	CDR VCO main bias	12	DIFF FE Preamp Main array	23	DIFF FE VTH1 Right
2	CDR VCO buffer bias	13	DIFF FE PreComp	24	DIFF FE Preamp Top
3	CDR CP current	14	DIFF FE Comparator	25	DIFF FE Preamp Top-Right
4	CDR FD current	15	DIFF FE VTH2	26	not used
5	CDR buffer bias	16	DIFF FE VTH1 Main array	27	not used
6	CML driver tap 2 bias	17	DIFF FE LCC	28	Ana. input current/21000
7	CML driver tap 1 bias	18	DIFF FE Feedback	29	Ana. shunt current/21600
8	CML driver main bias	19	DIFF FE Preamp Left	30	Dig. input current/21000
9	NTC_pad current	20	DIFF FE VTH1 Left	31	Dig. shunt current/21600
10	Capmeasure circuit	21	DIFF FE Preamp Right	32-63	not used

Table F.2: Current multiplexer (I_mux) assignments for ITkPixV1.1 chip [44]

setting column references the address of the multiplexer input.

Setting	Selected Input	Setting	Selected Input	Setting	Selected Input
0	Vref_ADC (GADC)	10	DIFF FE VTH1 Main array	31	Vref_CORE
1	I_mux pad voltage	11	DIFF FE VTH1 Left	32	Vref_PRE
2	NTC_pad voltage	12	DIFF FE VTH1 Right	33	VINA / 4
3	VCAL_DAC / 2	13	RADSENS Ana. SLDO	34	VDDA / 2
4	VDDA / 2 from capmeasure	14	TEMPSENS Ana. SLDO	35	VrefA
5	Poly TEMPSENS top	15	RADSENS Dig. SLDO	36	VOFS / 4
6	Poly TEMPSENS bottom	16	TEMPSENS Dig. SLDO	37	VIND / 4
7	VCAL_HI	17	RADSENS center	38	VDDD / 2
8	VCAL_MED	18	TEMPSENS center	39	VrefD
9	DIFF FE VTH2	19-30	Ana. GND	40-63	not used

Table F.3: Voltage multiplexer (V_mux) assignments for ITkPixV1.1 chip [44]

F.1.7 Measure Data Merging

The data-merging feature is, as described in Section 6.2.2 is responsible for receiving data from a neighboring RD53B. This extra data is then included in the receiving RD53Bs own aurora lane output data stream. Section 6.2.2 introduces a bug discovered in the data-merging logic. Therefore, the objective during wafer probing is to figure out if all input lanes for data-merging work. For this purpose, a new firmware module was added to BDAQ53, which enables the BDAQ53 board to send RD53B aurora like data over one of its display ports to the data-merging input of ITkPixV1.1. At the same time, the BDAQ53 board is connected to the data output of the same ITkPixV1.1, listening for data inserted into the data stream. During wafer probing ten register and hit data words are sent per data-merging input lane for two different clock relations between the data-merging clock and the command clock. The phase relation shifts by 180°.

F.1.8 Test Aurora Lanes

For fully operational modules, it is necessary for all ITkPixV1.1 on a module to be able to send data on the correct aurora lanes. For this purpose, the output aurora lanes of each ITkPixV1.1 are tested during wafer probing. For this purpose, ten registers are read over each lane.

F.1.9 Test all Registers

One common failure during chip production are registers, which are stuck in a constant high or low state. To detect such a failure, each register receives a write command with 0b0101 and 0b1010, according to its bit length. If identical register values are read as they were written, the register can be assumed to be fully functional. Critical communication registers are left out of the test.

F.1.10 Measure Ring Oscillators

In RD53B ring oscillators are used to measure the switching times of the used logic gates in the ring oscillator ring. For this purpose RD53B features 42 ring oscillators as summarized in Table F.4 and Table F.5. The two tables refer to an independent ring oscillator bench, with Table F.4 being an exact copy of the ring oscillator used in RD53A. Table F.5 uses the same and additional logic gates, with different oscillator lengths.

ROSC Nbr.	Type	Len.	ROSC Nbr.	Type	Len.
0	Strgth. 0 inv. clk. drvr.	55	4	Strgth. 0 4-input NAND	19
1	Strgth. 4 inv. clk. drvr.	51	5	Strgth. 4 4-input NAND	19
2	Strgth. 0 inverter	55	6	Strgth. 0 4-input NOR	19
3	Strgth. 4 inverter	51	7	Strgth. 4 4-input NOR	19

Table F.4: Ring Oscillator Bench A [44]

The frequencies measured in the ring oscillator, during wafer probing provide information about the switching speed of the logic gates utilized at room temperature and the ideal powering. If one of the frequencies is significantly out of specification, this is a hint to a production error and the ITkPixV1.1 is discarded during wafer probing.

F.1.11 Pixel Register Scan

As mentioned in Section 5.2.4, each pixel features eight bits that need to be tested, just as registers in the global register test. One common failure during chip production are stuck registers in a constant high or low state. To detect such a failure, each pixel register receives a write command with 0b01010101 and 0b10101010. If identical register values are read back as they are written, the register can be assumed to be fully functional. More information on pixel registers is found in Section 5.2.4.

F.2 Wafer Probing Test Results

Wafer probing test results are cuts, which are extracted from the routines mentioned in Section 7.2 and F.1. Figure F.1 summarizes the data structure and relation between wafer probing routines, wafer

ROSC Nbrs.	Type	Eff. Len.
0 & 1	Strgth. 0 inv. clk. driver	38.2
2 & 3	Strgth. 4 inv. clk. driver	44.5
4 & 5	Strgth. 0 inverter	38.1
6 & 7	Strgth. 4 inverter	44.3
8 & 9	Strgth. 0 4-input NAND	12.6
10 & 11	Strgth. 4 4-input NAND	16
12 & 13	Strgth. 0 4-input NOR	14.5
14 & 15	Strgth. 4 4-input NOR	14.5
16 & 17	Strgth. 0 scan D-flip-flop	6.1
18 & 19	Strgth. 1 D-flip-flop	6.2
20 & 21	Strgth. 1 Neg. edge D-flip-flop	5
22	Strgth. 0 LVT inverter	40.6
23	Strgth. 4 LVT inverter	56
24	Strgth. 0 LVT 4-input NAND	16.5
25	Strgth. 4 LVT 4-input NAND	22.8
26-33	Strgth. 4 inj-cap-loaded 4-input NAND	16.8

Table F.5: Ring Oscillator Bench B [44]

probing tests, functionality tests and characterization tests.

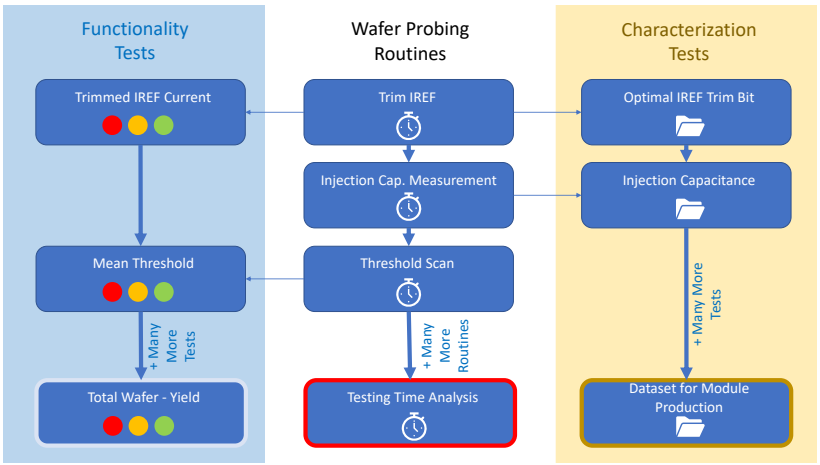


Figure F.1: Relation between wafer probing routine, functionality tests and characterization tests

At first the data is acquired by one of the wafer probing routines (white) described in Section 7.2. The acquired data will be analyzed by a wafer probing test (blue and yellow), which extracts a known value from the measurement, which can be compared to a value known form simulation or empirical measurements.

Based on whether the extracted known value is used for determining whether a chip will be used in the detector, or whether the extracted known value will exclusively be used for trimming and calibration of a chip, the wafer probing tests can be classified into functionality tests or characterization tests, as indicated by the blue and yellow columns in Figure F.1. Each wafer probing routine can have multiple wafer probing tests from both the functionality- and characterization- domain. The

functionality tests are wafer probing tests, which have hard cut-values on whether a ITkPixV1.1 is working or not. Those wafer probing tests classify each chip in three traffic light like categories, as indicated by the three colored circles at the bottom of each functionality test in Figure F.1. The colors represent:

- **Green**: ITkPixV1.1 are chips that pass a test and are candidates for ITk production
- **Yellow**: ITkPixV1.1 are chips that are outside the ideal specification for ITk production, but still meet the requirements for bench testing
- **Red**: ITkPixV1.1 are chips that are outside the ideal specification for ITk production and do not qualify for bench testing

This traffic light like scheme is used to calculate a chips final yield-color. If all functionality tests are classified as green, the corresponding chip is classified as green in the yield-map. If one functionality test has a different color, the final chip yield has the same color. The yield analysis can be found in Section 7.2.9. The yellow column in Figure F.1 indicates characterization tests, where the cut-value does not matter. Regardless of the calculated value in the corresponding test, the chip is not rejected, but the value is saved for future calibration of the chip at, for example, module level, as indicated by the white folder icon in each of the corresponding tests. The characterization tests and functionality tests can be differentiated in the following Sections by the "Char." parameter in the corresponding Table. In Appendix F, all wafer probing tests are individually evaluated on a single page for 50 wafers

	characterization test	functionality test
Char.	Yes	No

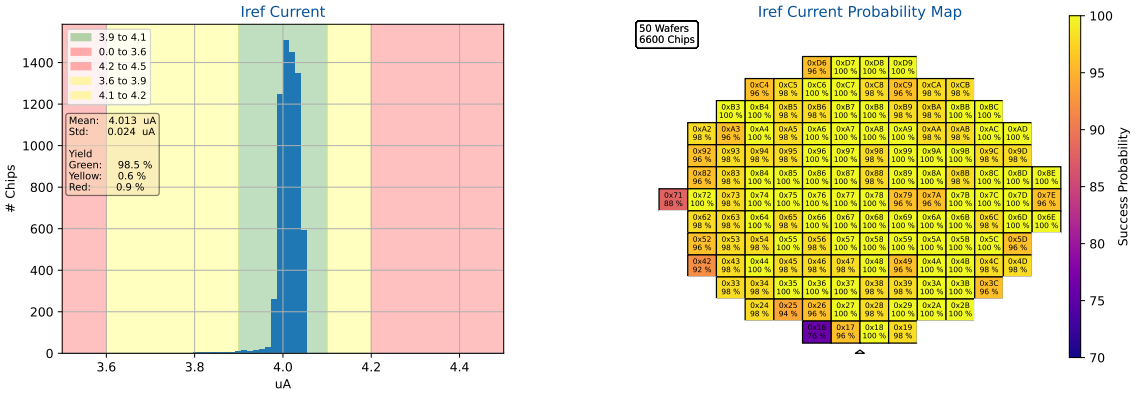
Table F.6: wafer probing test indicator for characterization test or functionality test

and 6600 chips, which were run with a well comparable wafer probing routine. Each wafer probing test-page features four analysis components:

1. The histogram plot, histograming all calculated values of a wafer probing test and showing the boundaries of cut-value in green, yellow, and red colors. (Example Figure F.2(a)
2. The wafer map-plot, showing the mean success probability of each chip based on its wafer-location. Patterns in this plot can be a hint to a systematic error. (Example Figure F.2(b)
3. The wafer probing test summary table. It summarizes the cut-values, mean and standard deviation of the histogram in the plotted region, as well as the indicator for a characterization test or functionality test, as well as the yield of this particular wafer probing test. (Example Table F.7)
4. The summary text, explaining in more detail, what was measured and discussing features of the measurement.

F.2.1 Iref Current

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.1.



(a) Histogram of Iref Current

(b) Averaged Wafer map of Iref Current

Figure F.2: Test result plots of wafer probing test Iref Current

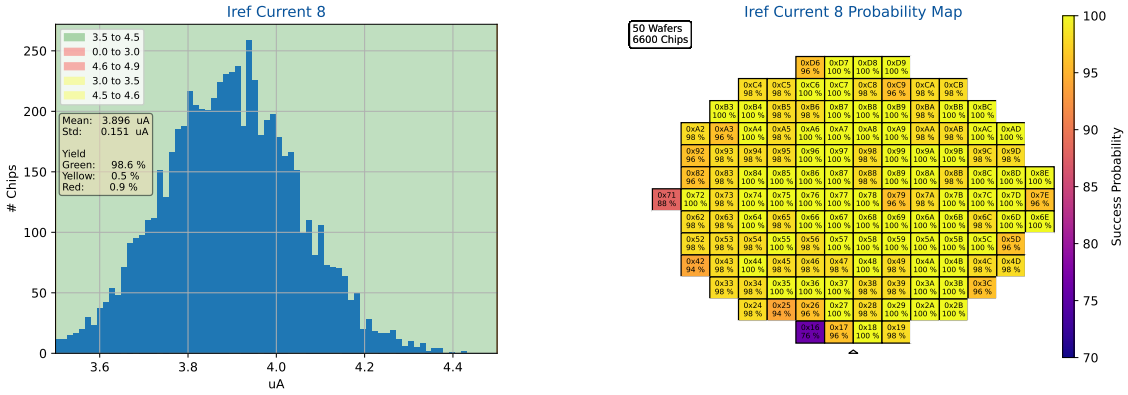
Cuts [uA]						Distribution [uA]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	4.013	**Green**	99
High	3.6	3.9	4.1	4.2	4.5	**Std.**	0.024	**Yellow**	1
Low	0.0	3.6	3.9	4.1	4.2	**Char.**	No	**Red**	1

Table F.7: Summary of wafer probing test Iref Current

This wafer probing test is the 16th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s IREF current tuning capabilites. This is achieved by measuring the IREF current, which is closest to 4 µA. The IREF current can be changed by varying the IREF trim bits. The measured values are histogrammed in Figure F.2(a). Its x-axis shows the measured IREF current, using the procedure described in Section 7.2.1. The expected histogram mean is 4.0 µA. The measured mean value is 4.013 µA, which is, considering the measured standard deviation of 0.024 µA, in good agreement with the expected value. This wafer probing test differentiates between green, yellow, and red ITkPixV1.1. Green chips are qualified as such between 3.9 µA and 4.1 µA with a yield of 99 %. Chips are classified as not green if their IREF cannot be tuned to the desired value. Since the functionality tested in this wafer probing test is a key element of ITkPixV1.1, during operation in ITk, it can be classified as a functionality test. The probability map in Figure F.2(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits an even distribution of high functionality probability. However it is notable, that chips on the left side of the wafer, more particular on the bottom left, have a lower probability to be green. This can be attributed to the analog IREF and current mirroring block being located in the bottom left of ITkPixV1.1. Since the edges of a wafer are more likely to process inaccuracies, it makes sense, that chips on the left side have a slightly lower yield, then their center or right counter parts.

F.2.2 Iref Current 8

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.1.



(a) Histogram of Iref Current 8

(b) Averaged Wafer map of Iref Current 8

Figure F.3: Test result plots of wafer probing test Iref Current 8

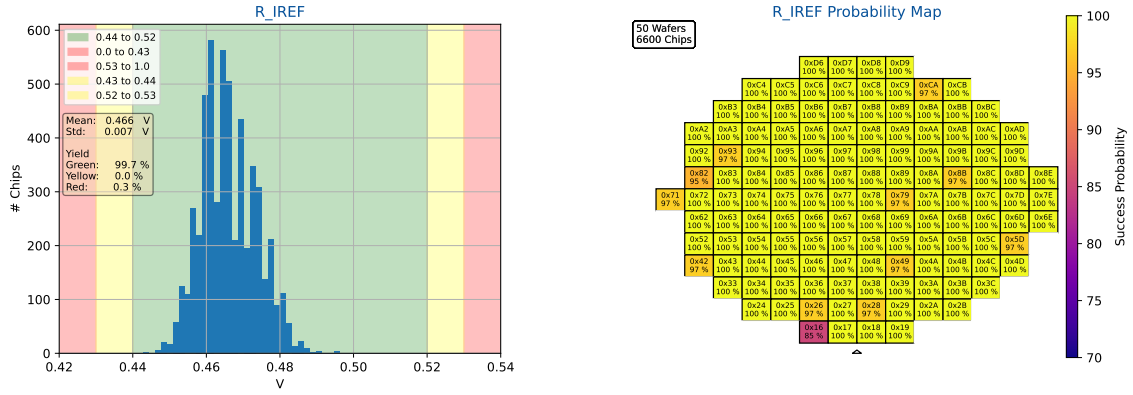
Cuts [uA]						Distribution [uA]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	3.896	**Green**	99
High	3.0	3.5	4.5	4.6	4.9	**Std.**	0.151	**Yellow**	0
Low	0.0	3.0	3.5	4.5	4.6	**Char.**	Yes	**Red**	1

Table F.8: Summary of wafer probing test Iref Current 8

This wafer probing test aims to characterize ITkPixV1.1s untrimmed IREF current. The measured values are histogrammed in Figure F.3(a). Its x-axis shows its untrimmed IREF current in µA, using the procedure described in Section 7.2.1. The expected histogram mean is <4 µA. The measured mean value is 3.896 µA. This wafer probing test differentiates between green, yellow, and red ITkPixV1.1. Green chips are qualified as such between 3.5 µA and 4.5 µA with a yield of 99 %. Due to its calculation of the untrimmed IREF current, this wafer probing test can be classified as a characterization test. The probability map in Figure F.3(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same gradient features as discussed in Section F.2.1.

F.2.3 R IREF

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.1.



(a) Histogram of R IREF

(b) Averaged Wafer map of R IREF

Figure F.4: Test result plots of wafer probing test R IREF

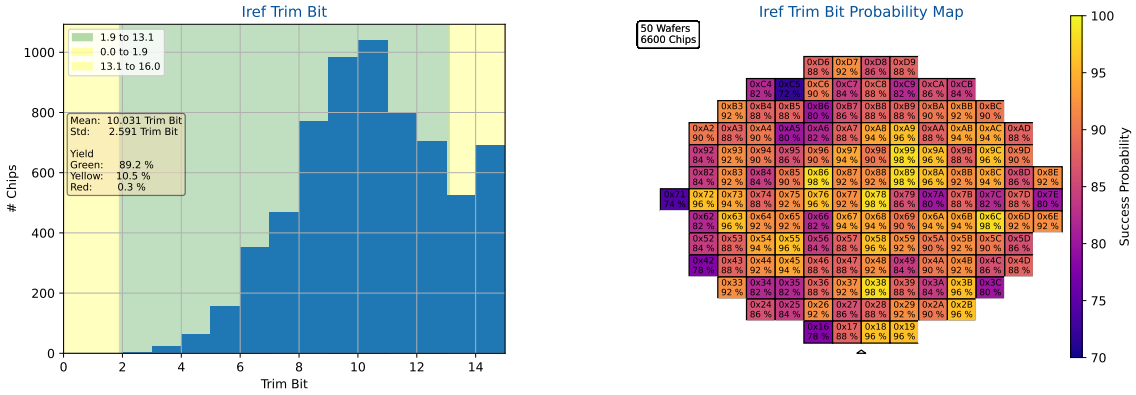
Cuts [V]						Distribution [V]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.466	**Green**	100
High	0.43	0.44	0.52	0.53	1.0	**Std.**	0.007	**Yellow**	0
Low	0.0	0.43	0.44	0.52	0.53	**Char.**	Yes	**Red**	0

Table F.9: Summary of wafer probing test R IREF

This wafer probing test aims to characterize ITkPixV1.1s untrimmed core bandgap current. The measured values are histogrammed in Figure F.4(a). Its x-axis shows the voltage drop of the core bandgap current of ideally 20 µA over a 22.6 kΩ resistor in V, using the procedure described in Section 7.2.1. The expected histogram mean is 0.452 V. The measured mean value is 0.466 V. This wafer probing test differentiates between green, yellow, and red ITkPixV1.1. Green chips are qualified as such between 0.44 V and 0.52 V with a yield of 100 %. Due to its calculation of the untrimmed core bandgap voltage , this wafer probing test can be classified as a characterization test. The probability map in Figure F.4(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits a few failing chip locations, despite its yield of 100 %, this is related to the stop of testing, after one of the previous wafer probing tests has failed. All in all this test succeded in all cases, where it was conducted.

F.2.4 Iref Trim Bit

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.1.



(a) Histogram of Iref Trim Bit

(b) Averaged Wafer map of Iref Trim Bit

Figure F.5: Test result plots of wafer probing test Iref Trim Bit

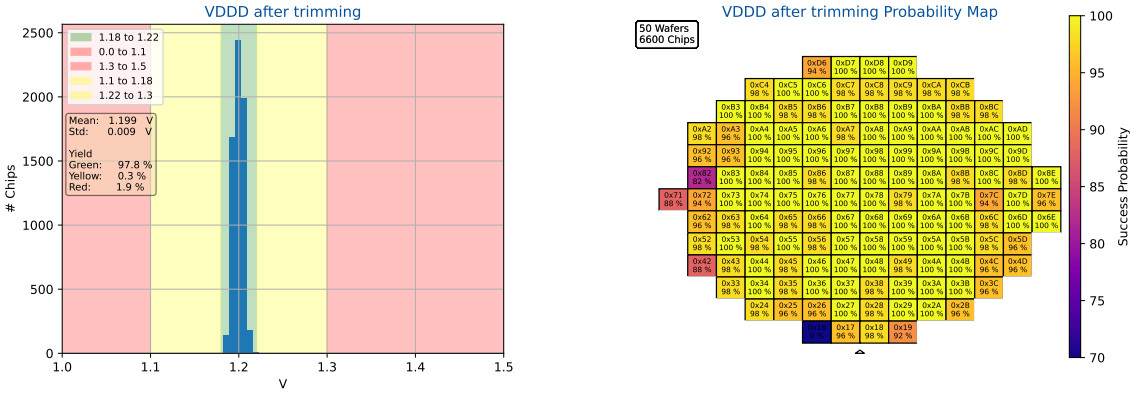
Cuts [Trim Bit]						Distribution [Trim Bit]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	10.031	**Green**	89
High		1.9	13.1	16.0		**Std.**	2.591	**Yellow**	10
Low		0.0	1.9	13.1		**Char.**	Yes	**Red**	0

Table F.10: Summary of wafer probing test Iref Trim Bit

This wafer probing test aims to characterize ITkPixV1.1s IREF trimbit distribution after IREF trimming. The measured values are histogrammed in Figure F.5(a). Its x-axis shows the trim bit, which yields an IREF current closest to 4 µA, using the procedure described in Section 7.2.1. The expected histogram mean is 7-8 LSB. The measured mean value is 10.031 LSB. This is not within specification and sparked a heavy discussion within RD53 Collaboration on whether to change the R_IREF resistor on the probe card and module flex to a larger value, to move the distribution to the left. In conclusion the R_IREF resistor value was chosen to be kept constant, due to the lack of commercially available fitting resistors and the large deviation between VREF_ADC and VOFS IREF trimming routines.This wafer probing test differentiates between green and yellow ITkPixV1.1. Green chips are qualified as such between 1.9 LSB and 13.1 LSB with a yield of 89 %. Due to its calculation of the ideal IREF trimbit, this wafer probing test can be classified as a characterization test. The probability map in Figure F.5(b) shows the mean probability of all tested ITkPixV1.1 to be green. It features, as expected a quite low yield, due to the offset of the IREF trim bit distribution and the harsh cut criterion of two trimbit on the left and right. Like all other characterization test this wafer probing test is not applied to the final yield cut.

F.2.5 VDDD after trimming

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.2.



(a) Histogram of VDDD after trimming

(b) Averaged Wafer map of VDDD after trimming

Figure F.6: Test result plots of wafer probing test VDDD after trimming

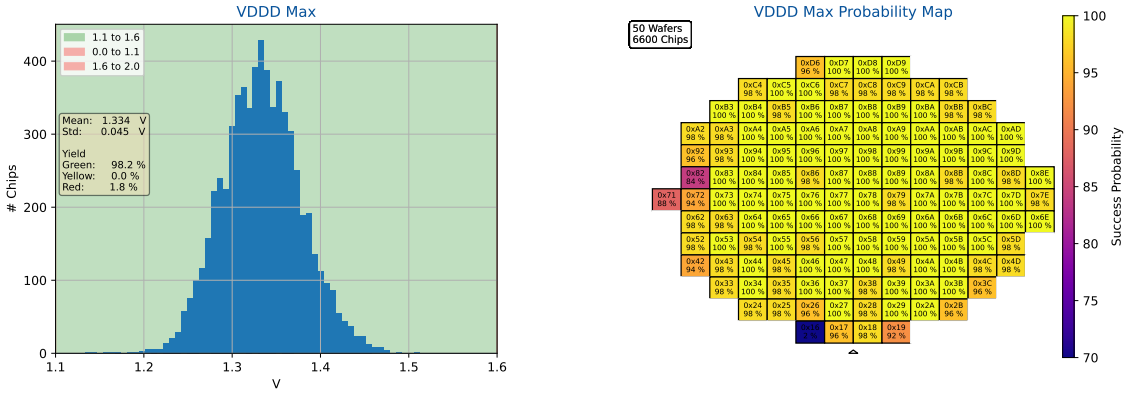
Cuts [V]						Distribution [V]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	1.199	**Green**	98
High	1.1	1.18	1.22	1.3	1.5	**Std.**	0.009	**Yellow**	0
Low	0.0	1.1	1.18	1.22	1.3	**Char.**	No	**Red**	2

Table F.11: Summary of wafer probing test VDDD after trimming

This wafer probing test is the 14th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s VDDD voltage spread after trimming. This is achieved by measuring the VDDD voltage, which is closest to 1.2 V.The VDDD voltage can be adjusted by varying the VDDD trim bits. The measured values are histogrammed in Figure F.6(a). Its x-axis shows the measured VDDD voltage after trimming, using the procedure described in Section 7.2.2. The expected histogram mean is 1.2 V. The measured mean value is 1.199 V, which is, considering the measured standard deviation of 0.009 V, in good agreement with the expected value. This wafer probing test differentiates between green, yellow, and red ITkPixV1.1. Green chips are qualified as such between 1.18 V and 1.22 V with a yield of 98 %. Chips are classified as not green if their VDDD cannot be tuned to the desired value. Since the functionality tested in this wafer probing test is a key element of ITkPixV1.1, during operation in ITk, it can be classified as a functionality test. The probability map in Figure F.6(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits an even distribution of high functionality probability. However it is notable, that chips on the left and bottom left side of the wafer, have a lower probability to be green. This can be attributed to the VDDD regulators being located in the bottom left of ITkPixV1.1. Since the edges of a wafer are more likely to be exposed to process variation, it makes sense, that chips on the left side have a slightly lower yield, then their center or right counter parts.

F.2.6 VDDD Max

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.2.



(a) Histogram of VDDD Max

(b) Averaged Wafer map of VDDD Max

Figure F.7: Test result plots of wafer probing test VDDD Max

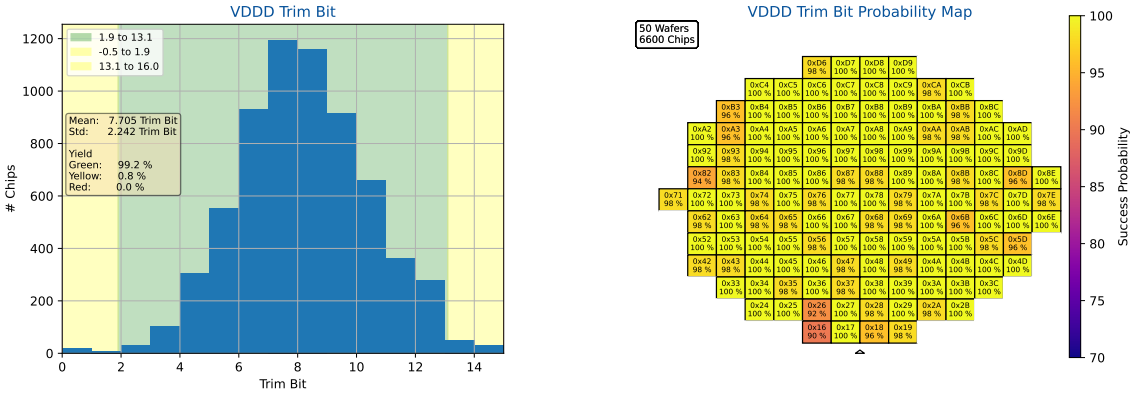
Cuts [V]						Distribution [V]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	1.334	**Green**	98
High	1.1		1.6		2.0	**Std.**	0.045	**Yellow**	0
Low	0.0		1.1		1.6	**Char.**	No	**Red**	2

Table F.12: Summary of wafer probing test VDDD Max

This wafer probing test is the 11th most likely not to be green among all 21 functionality tests. This wafer probing test aims to characterize ITkPixV1.1s maximal VDDD voltage at the highest trim bit. This is a quick test to check if a chips LDO regulators are capable of producing the desired 1.2 V. The measured values are histogrammed in Figure F.7(a). Its x-axis shows the maximal VDDD voltage at the highest trim bit setting, using the procedure described in Section 7.2.2. The expected histogram mean is >1.2 V. The measured mean value is 1.334 V. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 1.1 V and 1.6 V with a yield of 98 %. Due to its calculation of , this wafer probing test can be classified as a characterization test. The probability map in Figure F.7(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.5. Currently this test filters no additional chips, which are not filtered by Section F.2.5 or Section F.2.7. For the future it could be considered to define the lower green boundary to >1.2 V, which in this campaign has proven to be a weaker filter than the compination of the afore mentioned wafer probing test cut-values.

F.2.7 VDDD Trim Bit

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.2.



(a) Histogram of VDDD Trim Bit

(b) Averaged Wafer map of VDDD Trim Bit

Figure F.8: Test result plots of wafer probing test VDDD Trim Bit

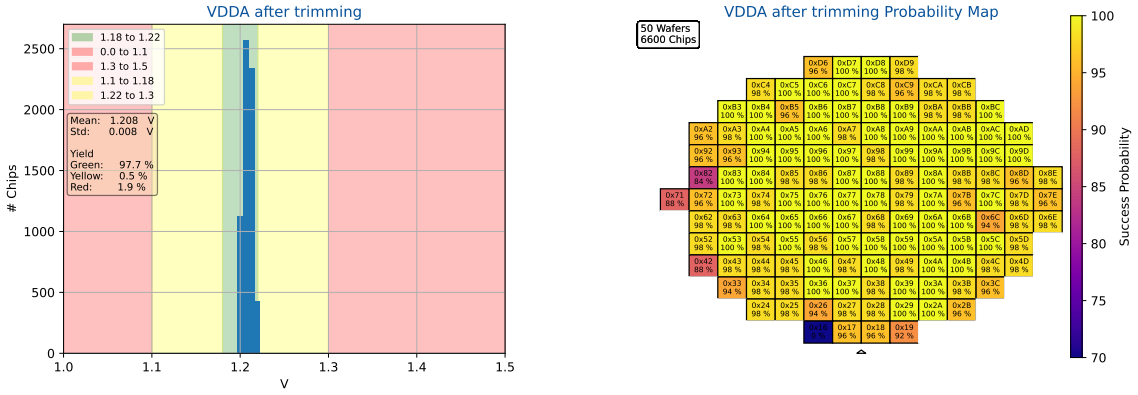
Cuts [Trim Bit]						Distribution [Trim Bit]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	7.705	**Green**	99
High		1.9	13.1	16.0		**Std.**	2.242	**Yellow**	1
Low		-0.5	1.9	13.1		**Char.**	No	**Red**	0

Table F.13: Summary of wafer probing test VDDD Trim Bit

This wafer probing test is the 19th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s VDDD tuning range. It displays the trimbits, which were chosen for the wafer probing test in Section F.2.5, bein closest to 1.2 V. The measured values are histogrammed in Figure F.8(a). Its x-axis shows the chosen VDDD trimbit, which sets VDDD closest to 1.2 V, using the procedure described in Section 7.2.2. The expected histogram mean is 7-8 LSB. The measured mean value is 7.705 LSB. This wafer probing test differentiates between green and yellow ITkPixV1.1. Green chips are qualified as such between 1.9 LSB and 13.1 LSB with a yield of 99 %. Chips are classified as not green if their VDDD trimbit is in the range of 0-1 or 13-14, featuring insufficient range for retuning during operation. Due to its calculation of the ideal VDDD trimbit, this wafer probing test can be classified as a characterization test, as well as a functionality test, due to the tested functionality being a key element of ITkPixV1.1, during operation in ITk. The probability map in Figure F.8(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits an even distribution of high functionality probability. The effect of less yield on the left is reduced, since chips, which do not work have a probabilty for the trimbits to be set in the middle of the range. These chips however do not feature a VDDD in the acceptable range and are therefore rejected by a different test.

F.2.8 VDDA after trimming

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.2.



(a) Histogram of VDDA after trimming

(b) Averaged Wafer map of VDDA after trimming

Figure F.9: Test result plots of wafer probing test VDDA after trimming

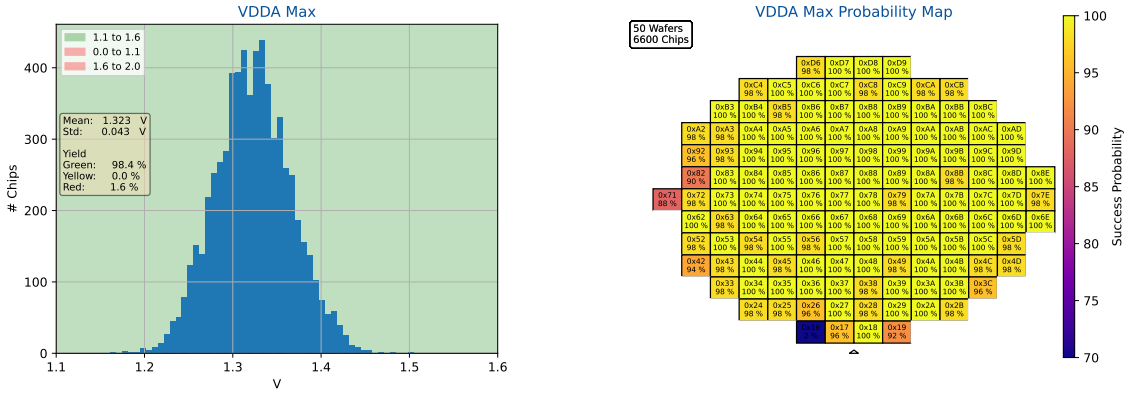
Cuts [V]						Distribution [V]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	1.208	**Green**	98
High	1.1	1.18	1.22	1.3	1.5	**Std.**	0.008	**Yellow**	0
Low	0.0	1.1	1.18	1.22	1.3	**Char.**	No	**Red**	2

Table F.14: Summary of wafer probing test VDDA after trimming

This wafer probing test is the 15th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s VDDA voltage spread after trimming. This is achieved by measuring the VDDA voltage, which is closest to 1.2 V. The VDDA voltage can be adjusted by varying the VDDA trim bits. The measured values are histogrammed in Figure F.9(a). Its x-axis shows the measured VDDA voltage after trimming, using the procedure described in Section 7.2.2. The expected histogram mean is 1.2 V. The measured mean value is 1.208 V. This wafer probing test differentiates between green, yellow, and red ITkPixV1.1. Green chips are qualified as such between 1.18 V and 1.22 V with a yield of 98 %. Chips are classified as not green if their VDDA cannot be tuned to the desired value. Since the functionality tested in this wafer probing test is a key element of ITkPixV1.1, during operation in ITk, it can be classified as a functionality test. The probability map in Figure F.9(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits an even distribution of high functionality probability. However it is notable, that chips on the left and bottom left side of the wafer, have a lower probability to be green. This can be attributed to the VDDA regulators being located in the bottom left of ITkPixV1.1. Since the edges of a wafer are more likely to be exposed to process variation, it makes sense, that chips on the left side have a slightly lower yield, then their center or right counter parts.

F.2.9 VDDA Max

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.2.



(a) Histogram of VDDA Max

(b) Averaged Wafer map of VDDA Max

Figure F.10: Test result plots of wafer probing test VDDA Max

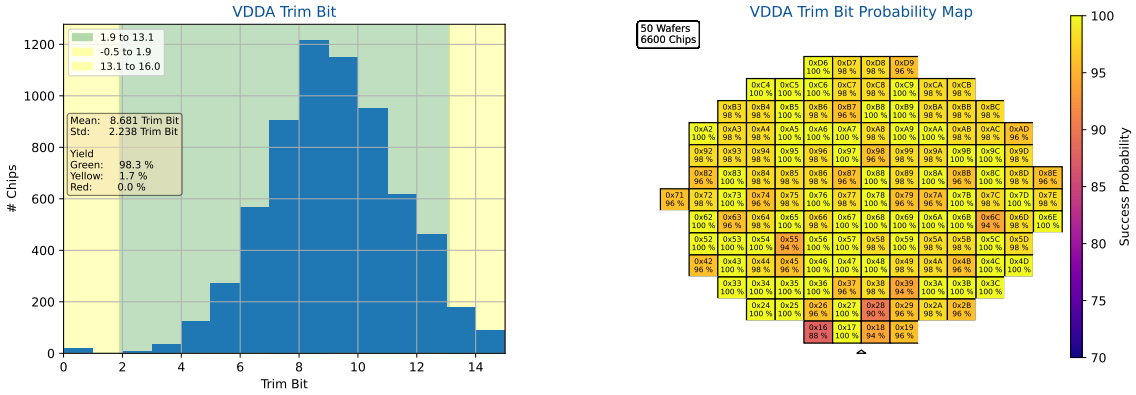
Cuts [V]						Distribution [V]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	1.323	**Green**	98
High	1.1		1.6		2.0	**Std.**	0.043	**Yellow**	0
Low	0.0		1.1		1.6	**Char.**	No	**Red**	2

Table F.15: Summary of wafer probing test VDDA Max

This wafer probing test is the 6th most likely not to be green among all 21 functionality tests. This wafer probing test aims to characterize ITkPixV1.1s maximal VDDA voltage at the highest trim bit. This is a quick test to check if a chips LDO regulators are capable of producing the desired 1.2 V. The measured values are histogrammed in Figure F.10(a). Its x-axis shows the maximal VDDA voltage at the highest trim bit setting, using the procedure described in Section 7.2.2. The expected histogram mean is >1.2 V. The measured mean value is 1.323 V. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 1.1 V and 1.6 V with a yield of 98 %. Due to its calculation of , this wafer probing test can be classified as a characterization test. The probability map in Figure F.10(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.8. Currently this test filters no additional chips, which are not filtered by Section F.2.8 or Section F.2.10. For the future it could be considered to define the lower green boundary to >1.2 V, which in this campaign has proven to be a weaker filter than the combination of the afore mentioned wafer probing test cut-values.

F.2.10 VDDA Trim Bit

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.2.



(a) Histogram of VDDA Trim Bit

(b) Averaged Wafer map of VDDA Trim Bit

Figure F.11: Test result plots of wafer probing test VDDA Trim Bit

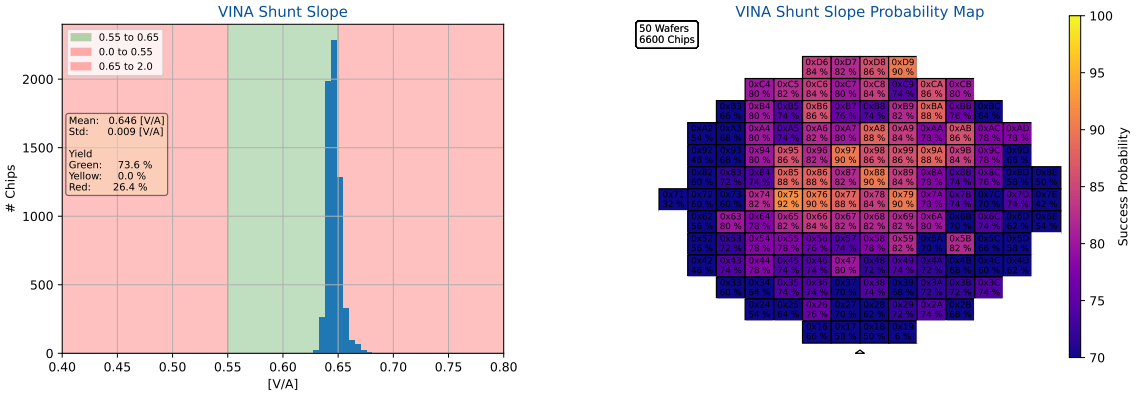
Cuts [Trim Bit]						Distribution [Trim Bit]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	8.681	**Green**	98
High		1.9	13.1	16.0		**Std.**	2.238	**Yellow**	2
Low		-0.5	1.9	13.1		**Char.**	No	**Red**	0

Table F.16: Summary of wafer probing test VDDA Trim Bit

This wafer probing test is the 9th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s VDDA tuning range. It displays the trimbits, which were chosen for the wafer probing test in Section F.2.8, bein closest to 1.2 V. The measured values are histogrammed in Figure F.11(a). Its x-axis shows the chosen VDDA trimbit, which sets VDDA closest to 1.2 V, using the procedure described in Section 7.2.2. The expected histogram mean is 7-8 LSB. The measured mean value is 8.681 LSB. Here the mean is slightly higher than expected, which could be related to the higher chosen VDDA voltages, shown in Figure F.9(a).This wafer probing test differentiates between green and yellow ITkPixV1.1. Green chips are qualified as such between 1.9 LSB and 13.1 LSB with a yield of 98 %. Chips are classified as not green if their VDDA trimbit is in the range of 0-1 or 13-14, featuring insufficient range for retuning during operation. Due to its calculation of the ideal VDDA trimbit, this wafer probing test can be classified as a characterization test, as well as a functionality test, due to the tested functionality being a key element of ITkPixV1.1, during operation in ITk. The probability map in Figure F.11(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits an even distribution of high functionality probability. The effect of less yield on the left is reduced, since chips, which do not work have a probabilty for the trimbits to be set in the middle of the range. These chips however do not feature a VDDA in the acceptable range and are therefore rejected by a different test.

F.2.11 VINA Shunt Slope

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.3.



(a) Histogram of VINA Shunt Slope

(b) Averaged Wafer map of VINA Shunt Slope

Figure F.12: Test result plots of wafer probing test VINA Shunt Slope

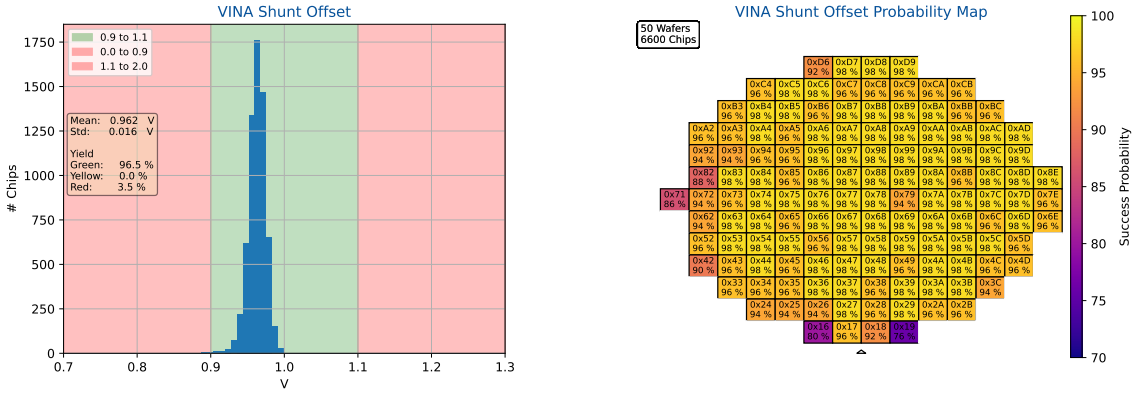
Cuts [V/A]						Distribution [V/A]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.646	**Green**	74
High	0.55		0.65		2.0	**Std.**	0.009	**Yellow**	0
Low	0.0		0.55		0.65	**Char.**	Yes	**Red**	26

Table F.17: Summary of wafer probing test VINA Shunt Slope

This wafer probing test aims to characterize ITkPixV1.1s analog shunt regulator slope. The measured values are histogrammed in Figure F.12(a). Its x-axis shows the analog shunt regulator slope in $\mathrm{V\,A^{-1}}$, using the procedure described in Section 7.2.3. The expected histogram mean is $0.59\,\mathrm{V\,A^{-1}}$. The measured mean value is $0.646\,\mathrm{V\,A^{-1}}$. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between $0.55\,\mathrm{V\,A^{-1}}$ and $0.65\,\mathrm{V\,A^{-1}}$ with a yield of 74 %. Due to its calculation of the analog shunt regulator slope, this wafer probing test can be classified as a characterization test. The probability map in Figure F.12(b) shows the mean probability of all tested ITkPixV1.1 to be green. This wafer probing test is a legacy functionality test, which was originally used to cut on the shunt regulator properties. This test is based on the same data as Section F.2.17.

F.2.12 VINA Shunt Offset

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.3.



(a) Histogram of VINA Shunt Offset

(b) Averaged Wafer map of VINA Shunt Offset

Figure F.13: Test result plots of wafer probing test VINA Shunt Offset

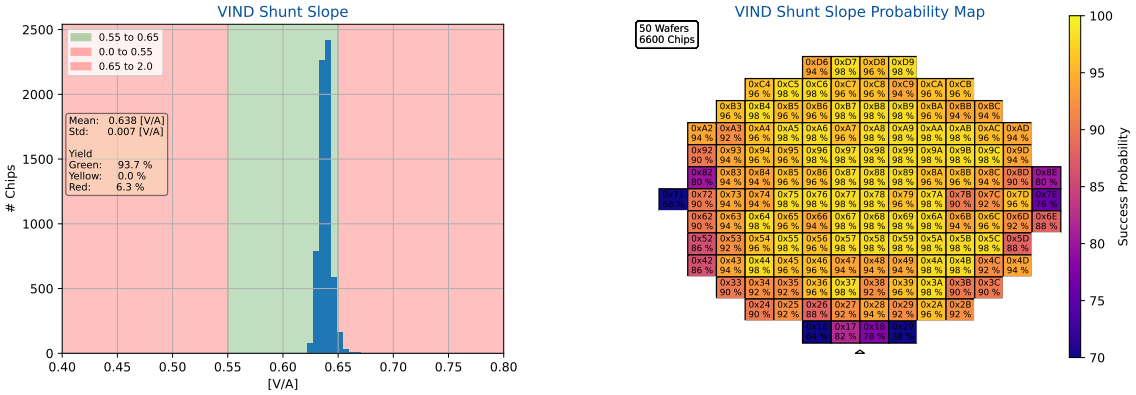
Cuts [V]						Distribution [V]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.962	**Green**	97
High	0.9		1.1		2.0	**Std.**	0.016	**Yellow**	0
Low	0.0		0.9		1.1	**Char.**	Yes	**Red**	3

Table F.18: Summary of wafer probing test VINA Shunt Offset

This wafer probing test aims to characterize ITkPixV1.1s analog shunt regulator offset voltage. The measured values are histogrammed in Figure F.13(a). Its x-axis shows the analog shunt regulator offset in V, using the procedure described in Section 7.2.3. The expected histogram mean is 0.996 V. The measured mean value is 0.962 V. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.9 V and 1.1 V with a yield of 97 %. Due to its calculation of the analog shunt regulator offset voltage, this wafer probing test can be classified as a characterization test. The probability map in Figure F.13(b) shows the mean probability of all tested ITkPixV1.1 to be green. This wafer probing test is a legacy functionality test, which was originally used to cut on the shunt regulator properties. This test is based on the same data as Section F.2.17.

F.2.13 VIND Shunt Slope

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.3.



(a) Histogram of VIND Shunt Slope

(b) Averaged Wafer map of VIND Shunt Slope

Figure F.14: Test result plots of wafer probing test VIND Shunt Slope

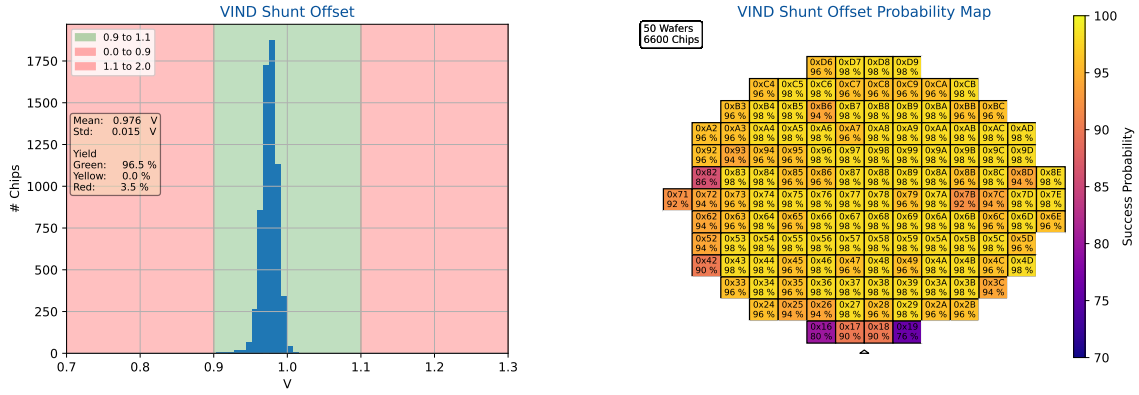
Cuts [V/A]						Distribution [V/A]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.638	**Green**	94
High	0.55		0.65		2.0	**Std.**	0.007	**Yellow**	0
Low	0.0		0.55		0.65	**Char.**	Yes	**Red**	6

Table F.19: Summary of wafer probing test VIND Shunt Slope

This wafer probing test aims to characterize ITkPixV1.1s digital shunt regulator slope. The measured values are histogrammed in Figure F.14(a). Its x-axis shows the digital shunt regulator slope in $\mathrm{V\,A^{-1}}$, using the procedure described in Section 7.2.3. The expected histogram mean is $0.59\,\mathrm{V\,A^{-1}}$. The measured mean value is $0.638\,\mathrm{V\,A^{-1}}$. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between $0.55\,\mathrm{V\,A^{-1}}$ and $0.65\,\mathrm{V\,A^{-1}}$ with a yield of 94 %. Due to its calculation of the digital shunt regulator slope, this wafer probing test can be classified as a characterization test. The probability map in Figure F.14(b) shows the mean probability of all tested ITkPixV1.1 to be green. This wafer probing test is a legacy functionality test, which was originally used to cut on the shunt regulator properties. This test is based on the same data as Section F.2.15.

F.2.14 VIND Shunt Offset

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.3.



(a) Histogram of VIND Shunt Offset

(b) Averaged Wafer map of VIND Shunt Offset

Figure F.15: Test result plots of wafer probing test VIND Shunt Offset

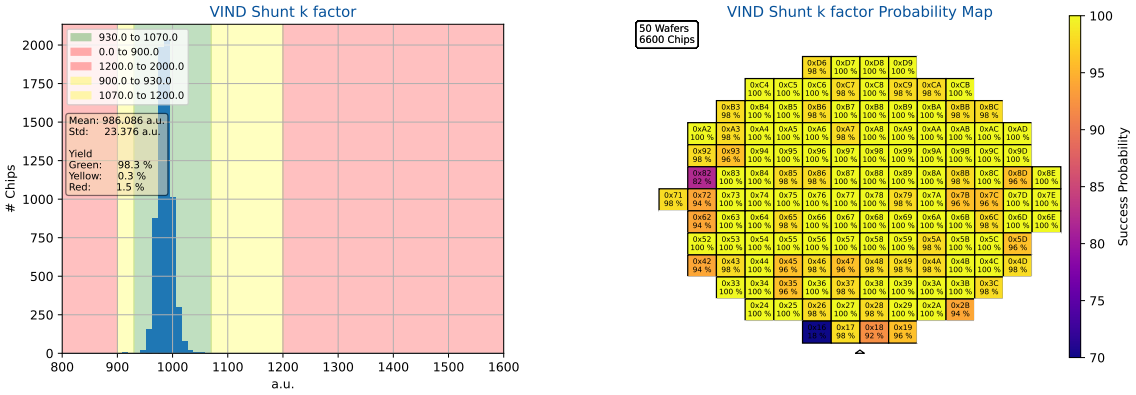
Cuts [V]						Distribution [V]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.976	**Green**	96
High	0.9		1.1		2.0	**Std.**	0.015	**Yellow**	0
Low	0.0		0.9		1.1	**Char.**	Yes	**Red**	4

Table F.20: Summary of wafer probing test VIND Shunt Offset

This wafer probing test aims to characterize ITkPixV1.1s digital shunt regulator offset voltage. The measured values are histogrammed in Figure F.15(a). Its x-axis shows the digital shunt regulator offset in V, using the procedure described in Section 7.2.3. The expected histogram mean is 0.996 V. The measured mean value is 0.976 V. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.9 V and 1.1 V with a yield of 96 %. Due to its calculation of the digital shunt regulator offset voltage, this wafer probing test can be classified as a characterization test. The probability map in Figure F.15(b) shows the mean probability of all tested ITkPixV1.1 to be green. This wafer probing test is a legacy functionality test, which was originally used to cut on the shunt regulator properties. This test is based on the same data as Section F.2.15.

F.2.15 VIND Shunt k factor

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.3.



(a) Histogram of VIND Shunt k factor

(b) Averaged Wafer map of VIND Shunt k factor

Figure F.16: Test result plots of wafer probing test VIND Shunt k factor

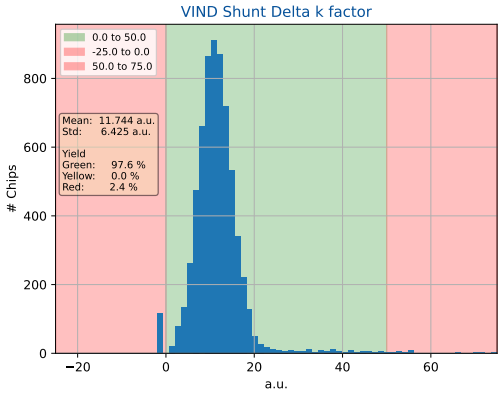
Cuts [a.u.]						Distribution [a.u.]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	986.086	**Green**	98
High	900.0	930.0	1070.0	1200.0	2000.0	**Std.**	23.376	**Yellow**	0
Low	0.0	900.0	930.0	1070.0	1200.0	**Char.**	No	**Red**	1

Table F.21: Summary of wafer probing test VIND Shunt k factor

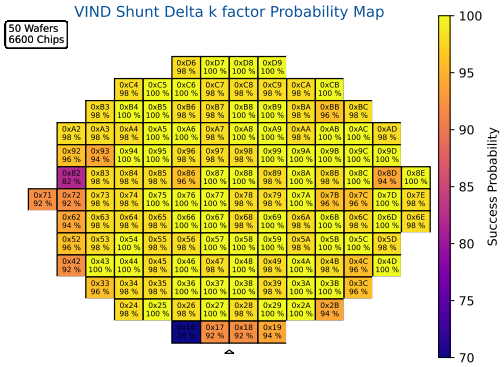
This wafer probing test is the 10th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s digital shunt regulator. The measured values are histogrammed in Figure F.16(a). Its x-axis shows the mean digital k-factor for input voltages between 1.5 V and 1.8 V, using the procedure described in Section 7.2.3. The expected histogram mean is 1000.0. The measured mean value is 986.086, which is, considering the measured standard deviation of 23.376, in good agreement with the expected value. The deviation between expected value and measured value is further discussed in Section 7.2.3.This wafer probing test differentiates between green, yellow, and red ITkPixV1.1. Green chips are qualified as such between 930.0 and 1070.0 with a yield of 98 %. Chips are classified as not green if their digital k-factor deviates more than 10 % from the measured mean. Due to its calculation of the digital k-factor, this wafer probing test can be classified as a characterization test, as well as a functionality test, due to the tested functionality being a key element of ITkPixV1.1, during operation in ITk. The probability map in Figure F.16(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same gradient features as discussed in Section F.2.1, since the shunt regulators are set off to the bottom left..

F.2.16 VIND Shunt Delta k factor

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.3.



(a) Histogram of VIND Shunt Delta k factor



(b) Averaged Wafer map of VIND Shunt Delta k factor

Figure F.17: Test result plots of wafer probing test VIND Shunt Delta k factor

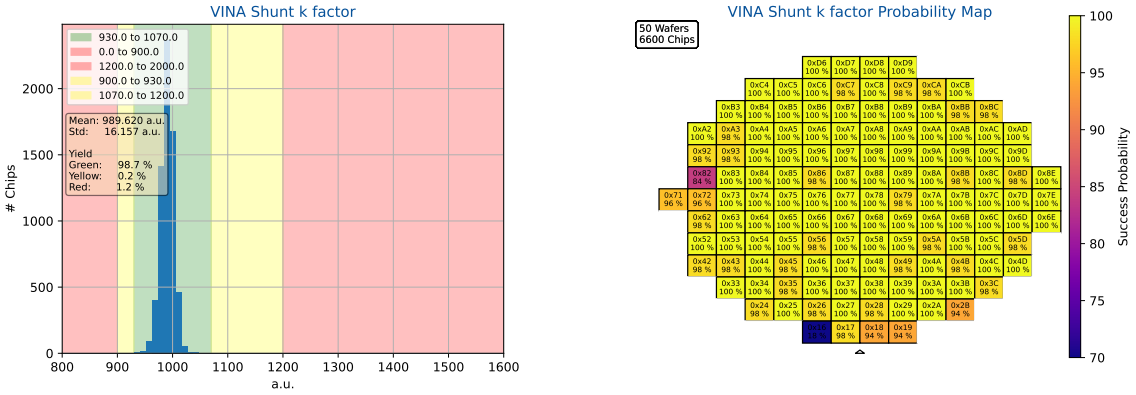
Cuts [a.u.]						Distribution [a.u.]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	11.744	**Green**	98
High	0.0		50.0		75.0	**Std.**	6.425	**Yellow**	0
Low	-25.0		0.0		50.0	**Char.**	No	**Red**	2

Table F.22: Summary of wafer probing test VIND Shunt Delta k factor

This wafer probing test is the 12th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s digital k-factor spread over different voltages. The measured values are histogrammed in Figure F.17(a). Its x-axis shows the maximal digital k-factor substracted by the minimal digital k-factor for input voltages between 1.5 V and 1.8 V, using the procedure described in Section 7.2.3. The expected histogram mean is as low as possible. The measured mean value is 11.744. RD53A already exhibited a voltage dependent k-factor, which is now quantified in wafer probing.This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.0 and 50.0 with a yield of 98 %. Chips are classified as not green if their digital delta k-factor deviates more than 10 % from the measured mean of Section F.2.15. Since the functionality tested in this wafer probing test is a key element of ITkPixV1.1, during operation in ITk, it can be classified as a functionality test. The probability map in Figure F.17(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, since the shunt regulators are set off to the bottom left. The average yield however is higher, since the dominant cut criterion for the shunt regulator block is defined in Section F.2.15.

F.2.17 VINA Shunt k factor

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.3.



(a) Histogram of VINA Shunt k factor

(b) Averaged Wafer map of VINA Shunt k factor

Figure F.18: Test result plots of wafer probing test VINA Shunt k factor

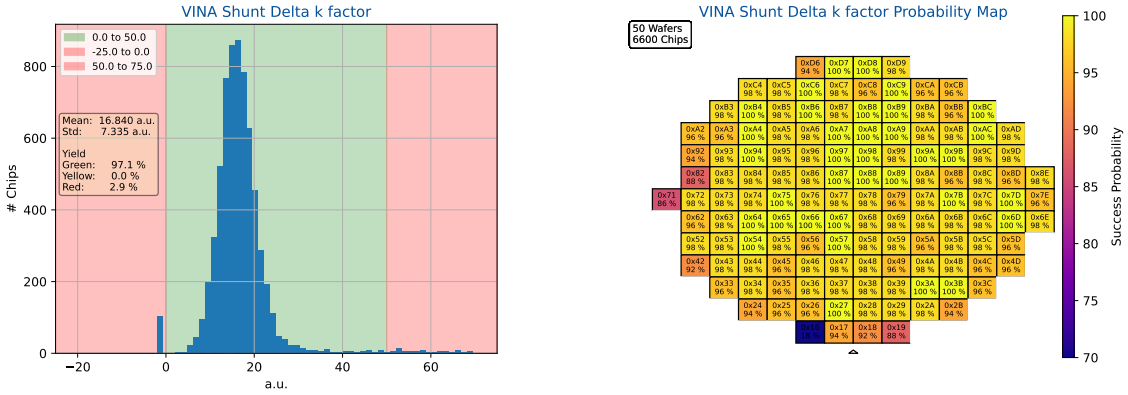
Cuts [a.u.]						Distribution [a.u.]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	989.62	**Green**	99
High	900.0	930.0	1070.0	1200.0	2000.0	**Std.**	16.157	**Yellow**	0
Low	0.0	900.0	930.0	1070.0	1200.0	**Char.**	No	**Red**	1

Table F.23: Summary of wafer probing test VINA Shunt k factor

This wafer probing test is the 20th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s analog shunt regulator. The measured values are histogrammed in Figure F.18(a). Its x-axis shows the mean analog k-factor for input voltages between 1.5 V and 1.8 V, using the procedure described in Section 7.2.3. The expected histogram mean is 1000.0. The measured mean value is 989.62, which is, considering the measured standard deviation of 16.157, in good agreement with the expected value. The deviation between expected value and measured value is further discussed in Section 7.2.3.This wafer probing test differentiates between green, yellow, and red ITkPixV1.1. Green chips are qualified as such between 930.0 and 1070.0 with a yield of 99 %. Chips are classified as not green if their analog k-factor deviates more than 10 % from the measured mean. Due to its calculation of the analog k-factor, this wafer probing test can be classified as a characterization test, as well as a functionality test, due to the tested functionality being a key element of ITkPixV1.1, during operation in ITk. The probability map in Figure F.18(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same gradient features as discussed in Section F.2.1, since the shunt regulators are set off to the bottom left..

F.2.18 VINA Shunt Delta k factor

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.3.



(a) Histogram of VINA Shunt Delta k factor

(b) Averaged Wafer map of VINA Shunt Delta k factor

Figure F.19: Test result plots of wafer probing test VINA Shunt Delta k factor

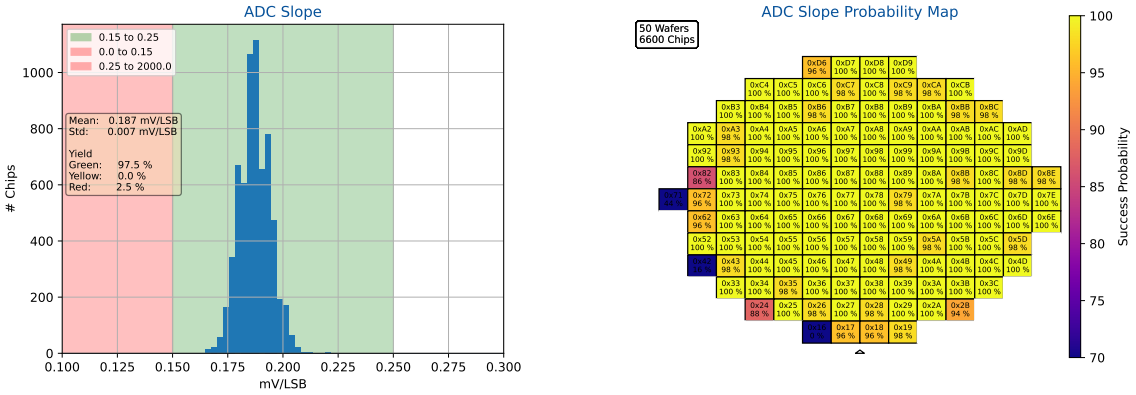
Cuts [a.u.]						Distribution [a.u.]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	16.84	**Green**	97
High	0.0		50.0		75.0	**Std.**	7.335	**Yellow**	0
Low	-25.0		0.0		50.0	**Char.**	No	**Red**	3

Table F.24: Summary of wafer probing test VINA Shunt Delta k factor

This wafer probing test is the 4th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s analog k-factor spread over different voltages. The measured values are histogrammed in Figure F.19(a). Its x-axis shows the maximal analog k-factor substracted by the minimal analog k-factor for input voltages between 1.5 V and 1.8 V, using the procedure described in Section 7.2.3. The expected histogram mean is as low as possible. The measured mean value is 16.84. RD53A already exhibited a voltage dependent k-factor, which is now quantified in wafer probing.This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.0 and 50.0 with a yield of 97 %. Chips are classified as not green if their analog delta k-factor deviates more than 10 % from the measured mean of Section F.2.17. Since the functionality tested in this wafer probing test is a key element of ITkPixV1.1, during operation in ITk, it can be classified as a functionality test. The probability map in Figure F.19(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, since the shunt regulators are set off to the bottom left. The average yield however is higher, since the dominant cut criterion for the shunt regulator block is defined in Section F.2.17.

F.2.19 ADC Slope

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.5.



(a) Histogram of ADC Slope

(b) Averaged Wafer map of ADC Slope

Figure F.20: Test result plots of wafer probing test ADC Slope

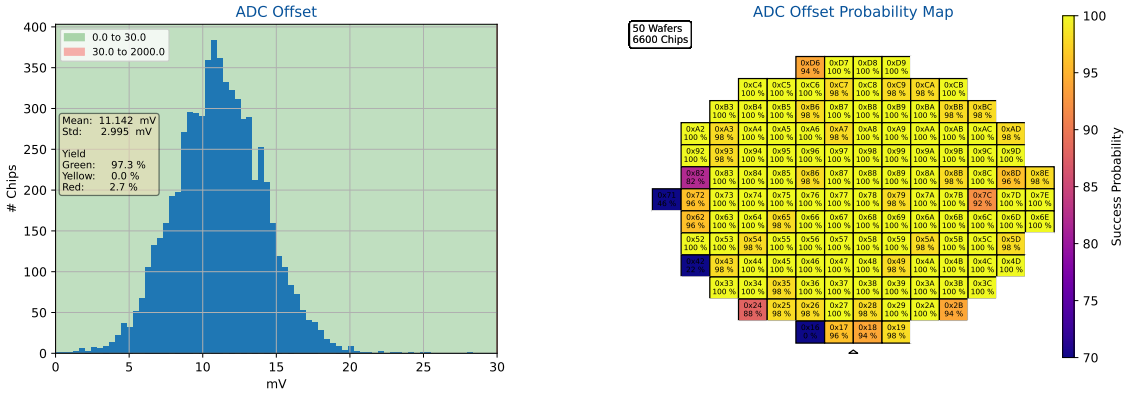
Cuts [mV/LSB]						Distribution [mV/LSB]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.187	**Green**	97
High	0.15		0.25		2000.0	**Std.**	0.007	**Yellow**	0
Low	0.0		0.15		0.25	**Char.**	Yes	**Red**	3

Table F.25: Summary of wafer probing test ADC Slope

This wafer probing test aims to characterize ITkPixV1.1s ADC slope. The slope is propotional to the resolution of the ADC, which describes how much the output digital value changes based on the input voltage. The measured values are histogrammed in Figure F.20(a). Its x-axis shows the measured ADC slope in mV bit^{-1}, using the procedure described in Section 7.2.5. The expected histogram mean is 0.2 mV bit^{-1}. The measured mean value is 0.187 mV bit^{-1}. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.15 mV bit^{-1} and 0.25 mV bit^{-1} with a yield of 97 %. Due to its calculation of the ADC slope, this wafer probing test can be classified as a characterization test. The probability map in Figure F.20(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, plus statistical fluctuation. For further discussion, please consult Section 7.2.6.

F.2.20 ADC Offset

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.5.



(a) Histogram of ADC Offset

(b) Averaged Wafer map of ADC Offset

Figure F.21: Test result plots of wafer probing test ADC Offset

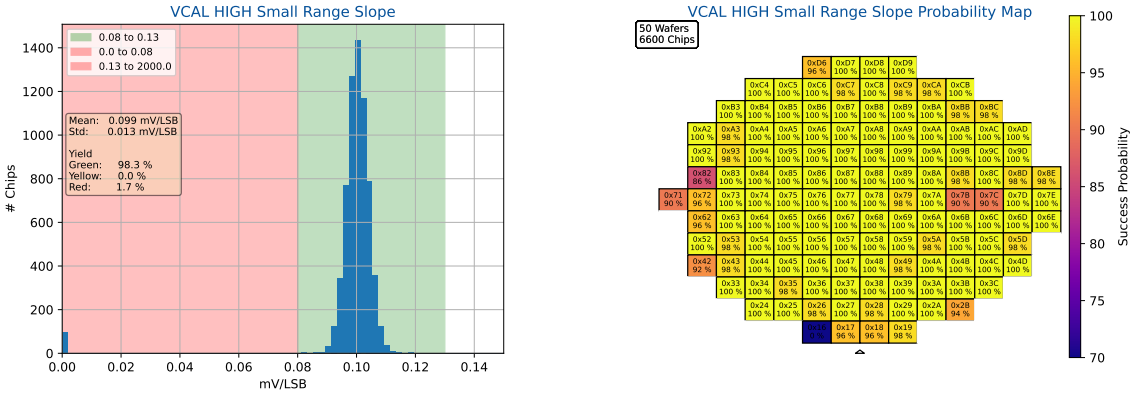
Cuts [mV]						Distribution [mV]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	11.142	**Green**	97
High	2000.0		30.0			**Std.**	2.995	**Yellow**	0
Low	30.0		0.0			**Char.**	Yes	**Red**	3

Table F.26: Summary of wafer probing test ADC Offset

This wafer probing test aims to characterize ITkPixV1.1s ADC offset. The offset is a constant voltage, which describes the maximal input voltage, at which the ADC still outputs zero. The measured values are histogrammed in Figure F.21(a). Its x-axis shows the measured ADC offset in mV, using the procedure described in Section 7.2.5. The expected histogram mean is 0.0 mV. The measured mean value is 11.142 mV. The expected histogram mean is hereby based on an ideal ADC.This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.0 mV and 30.0 mV with a yield of 97 %. Due to its calculation of the ADC offset, this wafer probing test can be classified as a characterization test. The probability map in Figure F.21(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits an almost fully homogeneous success probability for all chips, since the value for failing chips (0 mV) is within the green range. Chips with lower success probability fail already in earlier tests.

F.2.21 VCAL HIGH Small Range Slope

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.5.



(a) Histogram of VCAL HIGH Small Range Slope

(b) Averaged Wafer map of VCAL HIGH Small Range Slope

Figure F.22: Test result plots of wafer probing test VCAL HIGH Small Range Slope

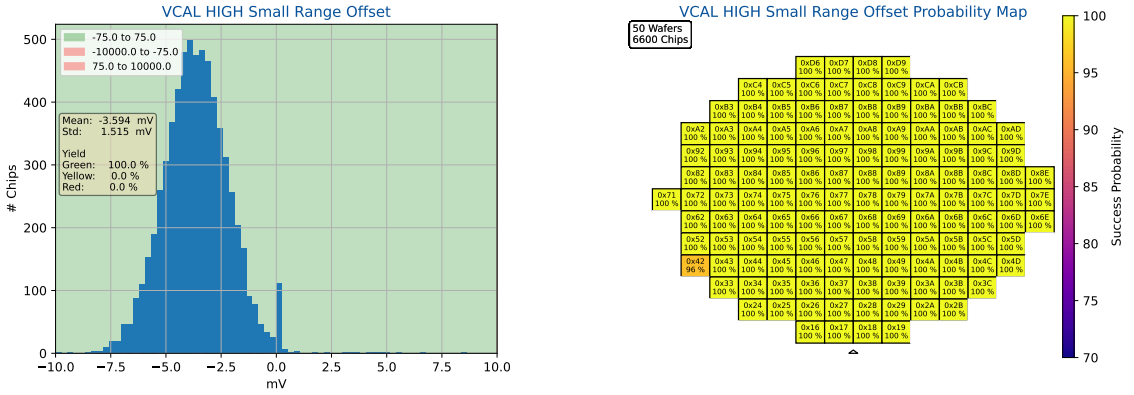
Cuts [mV/LSB]						Distribution [mV/LSB]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.099	**Green**	98
High	0.08		0.13		2000.0	**Std.**	0.013	**Yellow**	0
Low	0.0		0.08		0.13	**Char.**	Yes	**Red**	2

Table F.27: Summary of wafer probing test VCAL HIGH Small Range Slope

This wafer probing test aims to characterize ITkPixV1.1s small injection range vcal high DAC slope. The DAC slope describes how much the output voltage changes based on the input digital value. The measured values are histogrammed in Figure F.22(a). Its x-axis shows the measured small injection range vcal high DAC slope in mV bit^{-1}, using the procedure described in Section 7.2.5. The expected histogram mean is 0.1 mV bit^{-1}. The measured mean value is 0.099 mV bit^{-1}, which is, considering the measured standard deviation of 0.013 mV bit^{-1}, in good agreement with the expected value. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.08 mV bit^{-1} and 0.13 mV bit^{-1} with a yield of 98 %. Due to its calculation of the small injection range vcal high DAC slope, this wafer probing test can be classified as a characterization test. The probability map in Figure F.22(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, plus statistical fluctuation.

F.2.22 VCAL HIGH Small Range Offset

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.5.



(a) Histogram of VCAL HIGH Small Range Offset

(b) Averaged Wafer map of VCAL HIGH Small Range Offset

Figure F.23: Test result plots of wafer probing test VCAL HIGH Small Range Offset

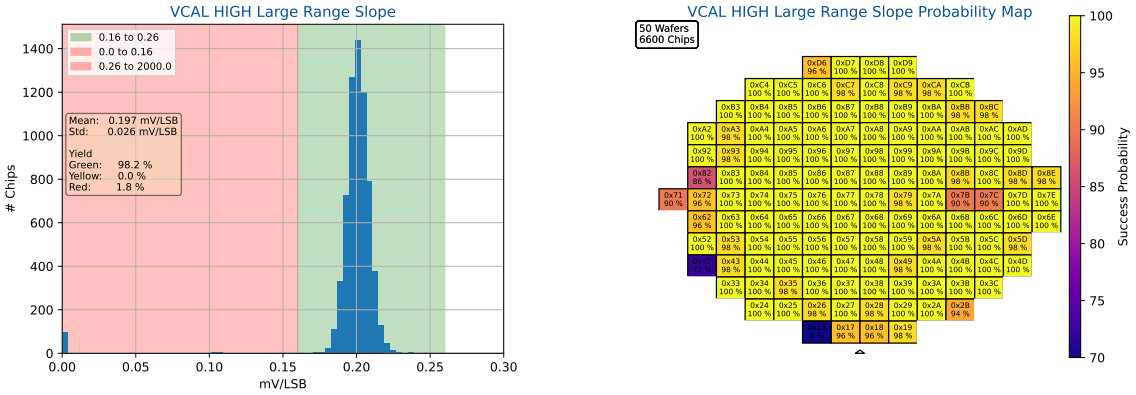
Cuts [mV]						Distribution [mV]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	-3.594	**Green**	100
High	-75.0		75.0		10000.0	**Std.**	1.515	**Yellow**	0
Low	-1.0		-75.0		75.0	**Char.**	Yes	**Red**	0

Table F.28: Summary of wafer probing test VCAL HIGH Small Range Offset

This wafer probing test aims to characterize ITkPixV1.1s small injection range vcal high DAC offset. The offset is a constant value, which describes the output voltage of the DAC at a digital input value of 0. The measured values are histogrammed in Figure F.23(a). Its x-axis shows the measured small injection range vcal high DAC offset in mV, using the procedure described in Section 7.2.5. The expected histogram mean is 0.0 mV. The measured mean value is −3.594 mV. The expected histogram mean is hereby based on an ideal DAC.This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between −75.0 mV and 75.0 mV with a yield of 100 %. Due to its calculation of the small injection range vcal high DAC offset, this wafer probing test can be classified as a characterization test. The probability map in Figure F.23(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits an almost fully homogeneous probability for all chips, since the value for failing chips (0 mV) is within the green range.

F.2.23 VCAL HIGH Large Range Slope

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.5.



(a) Histogram of VCAL HIGH Large Range Slope

(b) Averaged Wafer map of VCAL HIGH Large Range Slope

Figure F.24: Test result plots of wafer probing test VCAL HIGH Large Range Slope

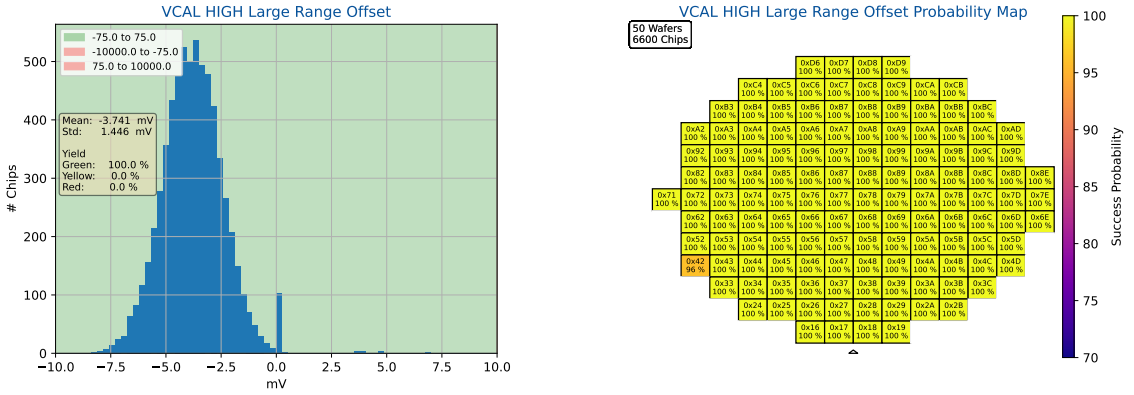
Cuts [mV/LSB]						Distribution [mV/LSB]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.197	**Green**	98
High	0.16		0.26		2000.0	**Std.**	0.026	**Yellow**	0
Low	0.0		0.16		0.26	**Char.**	Yes	**Red**	2

Table F.29: Summary of wafer probing test VCAL HIGH Large Range Slope

This wafer probing test aims to characterize ITkPixV1.1s large injection range vcal high DAC slope. The DAC slope describes how much the output voltage changes based on the input digital value. The measured values are histogrammed in Figure F.24(a). Its x-axis shows the measured large injection range vcal high DAC slope in mV bit^{-1}, using the procedure described in Section 7.2.5. The expected histogram mean is 0.2 mV bit^{-1}. The measured mean value is 0.197 mV bit^{-1}, which is, considering the measured standard deviation of 0.026 mV bit^{-1}, in good agreement with the expected value. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.16 mV bit^{-1} and 0.26 mV bit^{-1} with a yield of 98 %. Due to its calculation of the large injection range vcal high DAC slope, this wafer probing test can be classified as a characterization test. The probability map in Figure F.24(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, plus statistical fluctuation.

F.2.24 VCAL HIGH Large Range Offset

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.5.



(a) Histogram of VCAL HIGH Large Range Offset

(b) Averaged Wafer map of VCAL HIGH Large Range Offset

Figure F.25: Test result plots of wafer probing test VCAL HIGH Large Range Offset

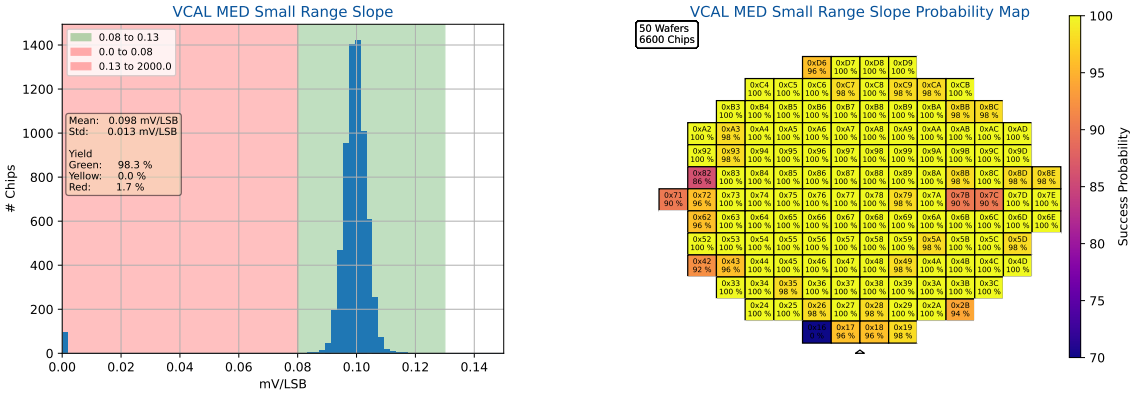
Cuts [mV]						Distribution [mV]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	-3.741	**Green**	100
High	-75.0		75.0		10000.0	**Std.**	1.446	**Yellow**	0
Low	-1.0		-75.0		75.0	**Char.**	Yes	**Red**	0

Table F.30: Summary of wafer probing test VCAL HIGH Large Range Offset

This wafer probing test aims to characterize ITkPixV1.1s large injection range vcal high DAC offset. The offset is a constant value, which describes the output voltage of the DAC at a digital input value of 0. The measured values are histogrammed in Figure F.25(a). Its x-axis shows the measured large injection range vcal high DAC offset in mV, using the procedure described in Section 7.2.5. The expected histogram mean is 0.0 mV. The measured mean value is −3.741 mV. The expected histogram mean is hereby based on an ideal DAC.This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between −75.0 mV and 75.0 mV with a yield of 100 %. Due to its calculation of the large injection range vcal high DAC offset, this wafer probing test can be classified as a characterization test. The probability map in Figure F.25(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits an almost fully homogeneous probability for all chips, since the value for failing chips (0 mV) is within the green range.

F.2.25 VCAL MED Small Range Slope

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.5.



(a) Histogram of VCAL MED Small Range Slope

(b) Averaged Wafer map of VCAL MED Small Range Slope

Figure F.26: Test result plots of wafer probing test VCAL MED Small Range Slope

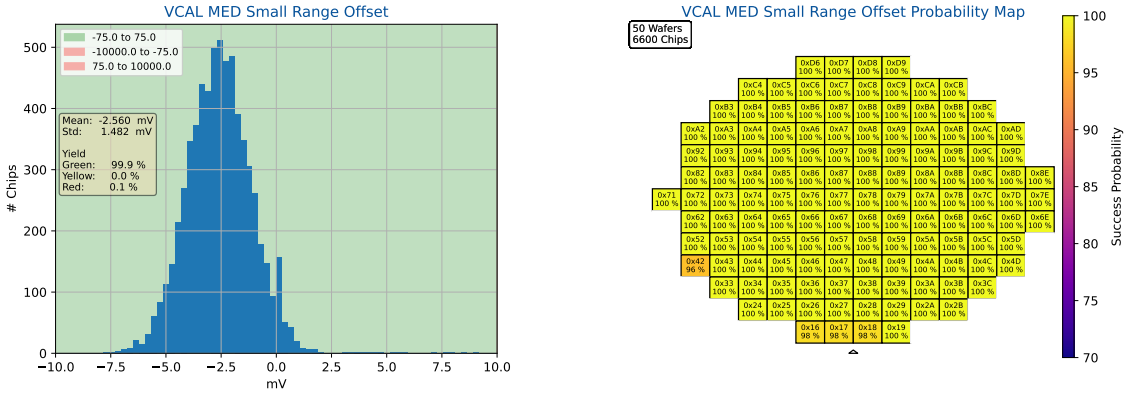
Cuts [mV/LSB]						Distribution [mV/LSB]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.098	**Green**	98
High	0.08		0.13		2000.0	**Std.**	0.013	**Yellow**	0
Low	0.0		0.08		0.13	**Char.**	Yes	**Red**	2

Table F.31: Summary of wafer probing test VCAL MED Small Range Slope

This wafer probing test aims to characterize ITkPixV1.1s small injection range vcal med DAC slope. The DAC slope describes how much the output voltage changes based on the input digital value. The measured values are histogrammed in Figure F.26(a). Its x-axis shows the measured small injection range vcal med DAC slope in mV bit^{-1}, using the procedure described in Section 7.2.5. The expected histogram mean is 0.1 mV bit^{-1}. The measured mean value is 0.098 mV bit^{-1}, which is, considering the measured standard deviation of 0.013 mV bit^{-1}, in good agreement with the expected value. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.08 mV bit^{-1} and 0.13 mV bit^{-1} with a yield of 98 %. Due to its calculation of small injection range vcal med DAC slope, this wafer probing test can be classified as a characterization test. The probability map in Figure F.26(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, plus statistical fluctuation.

F.2.26 VCAL MED Small Range Offset

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.5.



(a) Histogram of VCAL MED Small Range Offset

(b) Averaged Wafer map of VCAL MED Small Range Offset

Figure F.27: Test result plots of wafer probing test VCAL MED Small Range Offset

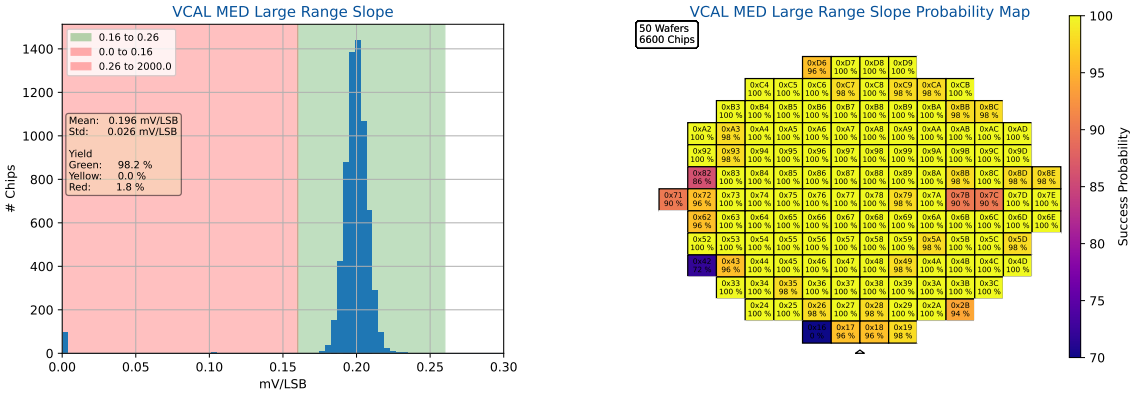
Cuts [mV]						Distribution [mV]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	-2.56	**Green**	100
High	-75.0		75.0		10000.0	**Std.**	1.482	**Yellow**	0
Low	-1.0		-75.0		75.0	**Char.**	Yes	**Red**	0

Table F.32: Summary of wafer probing test VCAL MED Small Range Offset

This wafer probing test aims to characterize ITkPixV1.1s small injection range vcal med DAC offset. The offset is a constant value, which describes the output voltage of the DAC at a digital input value of 0. The measured values are histogrammed in Figure F.27(a). Its x-axis shows the measured small injection range vcal med DAC offset in mV, using the procedure described in Section 7.2.5. The expected histogram mean is 0.0 mV. The measured mean value is −2.56 mV. The expected histogram mean is hereby based on an ideal DAC.This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between −75.0 mV and 75.0 mV with a yield of 100 %. Due to its calculation of the small injection range vcal med DAC offset, this wafer probing test can be classified as a characterization test. The probability map in Figure F.27(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits an almost fully homogeneous probability for all chips, since the value for failing chips (0 mV) is within the green range.

F.2.27 VCAL MED Large Range Slope

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.5.



(a) Histogram of VCAL MED Large Range Slope

(b) Averaged Wafer map of VCAL MED Large Range Slope

Figure F.28: Test result plots of wafer probing test VCAL MED Large Range Slope

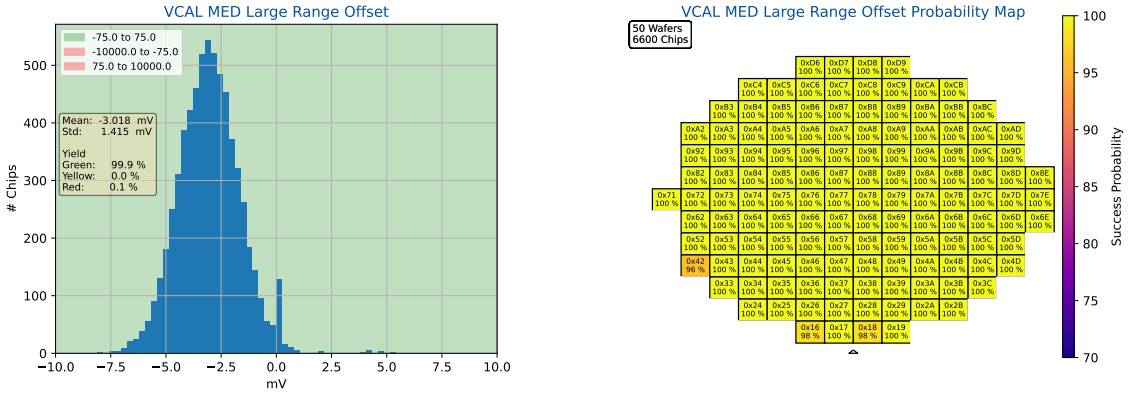
Cuts [mV/LSB]						Distribution [mV/LSB]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.196	**Green**	98
High	0.16		0.26		2000.0	**Std.**	0.026	**Yellow**	0
Low	0.0		0.16		0.26	**Char.**	Yes	**Red**	2

Table F.33: Summary of wafer probing test VCAL MED Large Range Slope

This wafer probing test aims to characterize ITkPixV1.1s large injection range vcal med DAC slope. The DAC slope describes how much the output voltage changes based on the input digital value. The measured values are histogrammed in Figure F.28(a). Its x-axis shows the measured large injection range vcal med DAC slope in mV bit^{-1}, using the procedure described in Section 7.2.5. The expected histogram mean is 0.2 mV bit^{-1}. The measured mean value is 0.196 mV bit^{-1}, which is, considering the measured standard deviation of 0.026 mV bit^{-1}, in good agreement with the expected value. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.16 mV bit^{-1} and 0.26 mV bit^{-1} with a yield of 98 %. Due to its calculation of the large injection range vcal med DAC slope, this wafer probing test can be classified as a characterization test. The probability map in Figure F.28(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, plus statistical fluctuation.

F.2.28 VCAL MED Large Range Offset

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.5.



(a) Histogram of VCAL MED Large Range Offset

(b) Averaged Wafer map of VCAL MED Large Range Offset

Figure F.29: Test result plots of wafer probing test VCAL MED Large Range Offset

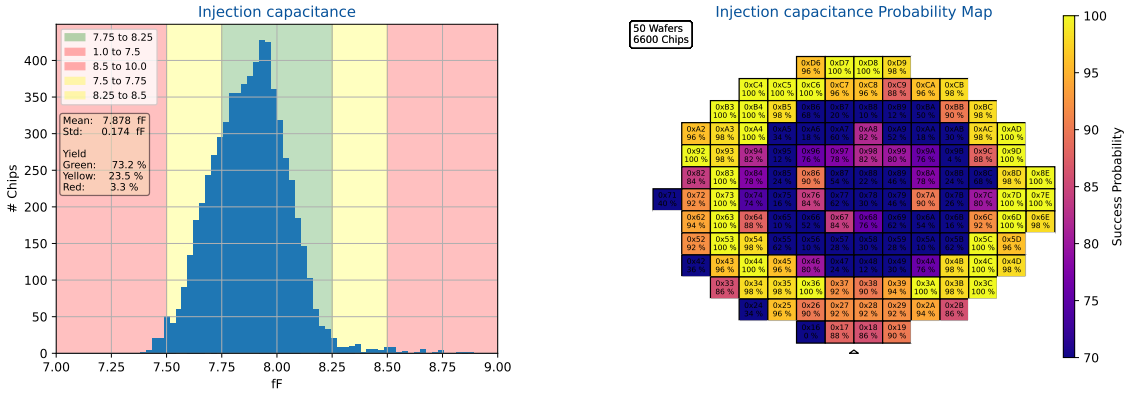
Cuts [mV]						Distribution [mV]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	-3.018	**Green**	100
High	-75.0		75.0		10000.0	**Std.**	1.415	**Yellow**	0
Low	-1.0		-75.0		75.0	**Char.**	Yes	**Red**	0

Table F.34: Summary of wafer probing test VCAL MED Large Range Offset

This wafer probing test aims to characterize ITkPixV1.1s large injection range vcal med DAC offset. The offset is a constant value, which describes the output voltage of the DAC at a digital input value of 0. The measured values are histogrammed in Figure F.29(a). Its x-axis shows the measured large injection range vcal med DAC offset in mV, using the procedure described in Section 7.2.5. The expected histogram mean is 0.0 mV. The measured mean value is −3.018 mV. The expected histogram mean is hereby based on an ideal DAC.This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between −75.0 mV and 75.0 mV with a yield of 100 %. Due to its calculation of the large injection range vcal med DAC offset, this wafer probing test can be classified as a characterization test. The probability map in Figure F.29(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits an almost fully homogeneous probability for all chips, since the value for failing chips (0 mV) is within the green range.

F.2.29 Injection capacitance

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.5.



(a) Histogram of Injection capacitance

(b) Averaged Wafer map of Injection capacitance

Figure F.30: Test result plots of wafer probing test Injection capacitance

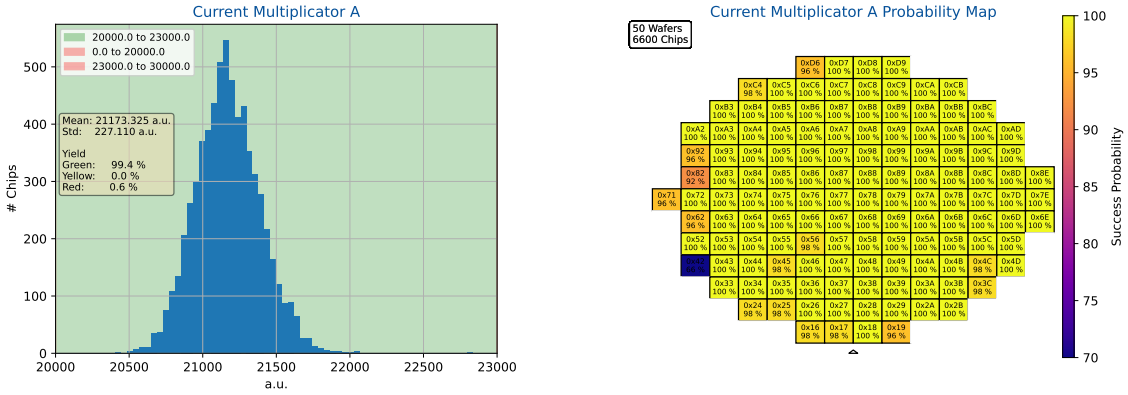
Cuts [fF]						Distribution [fF]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	7.878	**Green**	73
High	7.5	7.75	8.25	8.5	10.0	**Std.**	0.174	**Yellow**	23
Low	1.0	7.5	7.75	8.25	8.5	**Char.**	Yes	**Red**	3

Table F.35: Summary of wafer probing test Injection capacitance

This wafer probing test aims to characterize ITkPixV1.1s injection capacitance. The measured values are histogrammed in Figure F.30(a). Its x-axis shows the measured injection capacitance, using the procedure described in Section 7.2.5. The expected histogram mean is 8.02 fF. The measured mean value is 7.878 fF, which is, considering the measured standard deviation of 0.174 fF, in good agreement with the expected value. TSMC guarantees those capacitors to be accurate within ± 10 %. We observe a mean, which is 3 % lower than the expected value, with a 2 % standard deviaiton.This wafer probing test differentiates between green, yellow, and red ITkPixV1.1. Green chips are qualified as such between 7.75 fF and 8.25 fF with a yield of 73 %. Due to its calculation of The injection capacitance, this wafer probing test can be classified as a characterization test. The probability map in Figure F.30(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits a new pattern, thanks to the picked green lower boundary. The reagular positions have the usual lower success probabilities, due to before failing tests, however an additional blue, centered area is visible on the wafer. This is an expected pattern due to the excentric polishing procedure during manufacturing. During polishing more metal is removed in the center of the wafer, which reduces the measured injection capacitance in this region.

F.2.30 Current Multiplicator A

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.3.



(a) Histogram of Current Multiplicator A

(b) Averaged Wafer map of Current Multiplicator A

Figure F.31: Test result plots of wafer probing test Current Multiplicator A

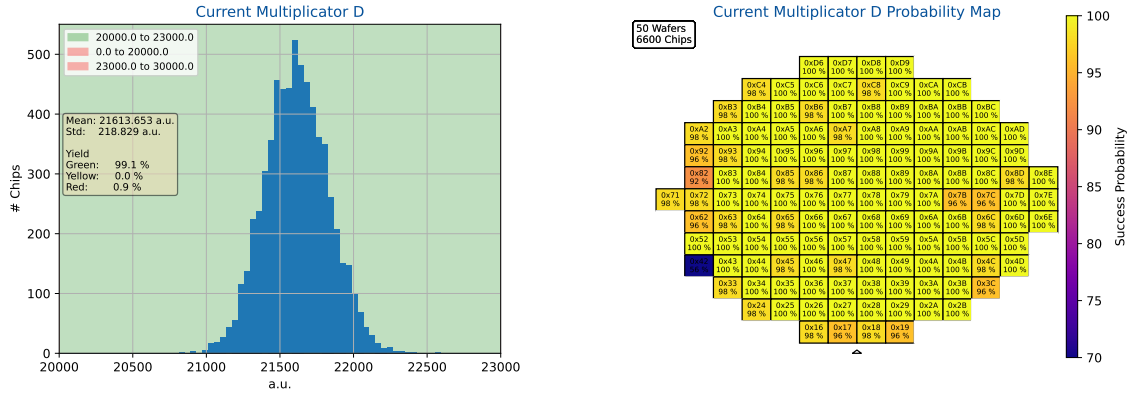
Cuts [a.u.]						Distribution [a.u.]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	21173.325	**Green**	99
High	20000.0		23000.0		30000.0	**Std.**	227.11	**Yellow**	0
Low	0.0		20000.0		23000.0	**Char.**	Yes	**Red**	1

Table F.36: Summary of wafer probing test Current Multiplicator A

This wafer probing test aims to characterize ITkPixV1.1s digital current mirror factor, between the measured current at “Dig. Shunt current” described in Table F.2 and the true digital input current, by dividing the measured digital input current measured at the power supply and the measured current at the IMUX. The measured values are histogrammed in Figure F.31(a). Its x-axis shows the calculated digital current mirror factor in arbitrary units (dimensionless), using the procedure described in Section 7.2.3. The expected histogram mean is 21000.0. The measured mean value is 21173.325, which is, considering the measured standard deviation of 227.11, in good agreement with the expected value. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 20000.0 and 23000.0 with a yield of 99 %. Due to its calculation of , this wafer probing test can be classified as a characterization test. The probability map in Figure F.31(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, since the shunt regulators are set off to the bottom left. The average yield however is higher, since the dominant cut criterion for the shunt regulator block is defined in Section F.2.15.

F.2.31 Current Multiplicator D

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.3.



(a) Histogram of Current Multiplicator D

(b) Averaged Wafer map of Current Multiplicator D

Figure F.32: Test result plots of wafer probing test Current Multiplicator D

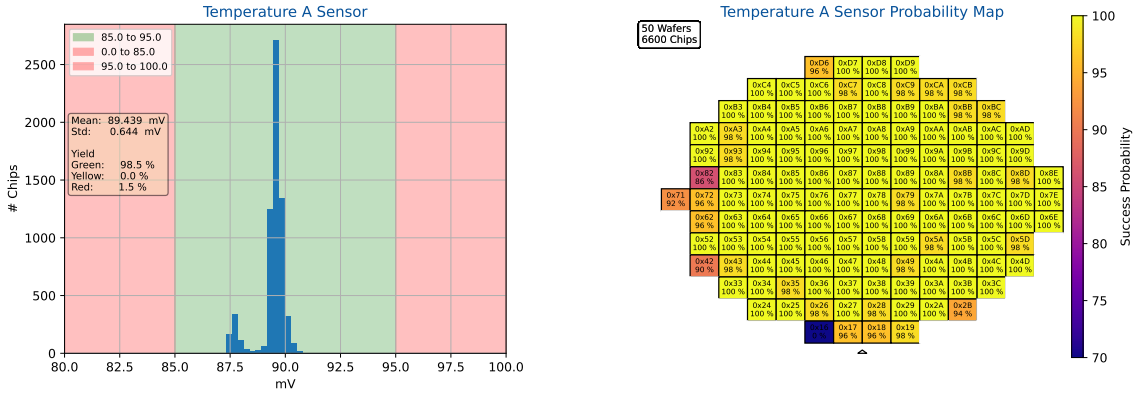
Cuts [a.u.]						Distribution [a.u.]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	21613.653	**Green**	99
High	20000.0		23000.0		30000.0	**Std.**	218.829	**Yellow**	0
Low	0.0		20000.0		23000.0	**Char.**	Yes	**Red**	1

Table F.37: Summary of wafer probing test Current Multiplicator D

This wafer probing test aims to characterize ITkPixV1.1s analog current mirror factor, between the measured current at “Ana. Shunt current” described in Table F.2 and the true analog input current, by dividing the measured analog input current measured at the power supply and the measured current at the IMUX. The measured values are histogrammed in Figure F.32(a). Its x-axis shows the calculated analog current mirror factor in arbitrary units (dimensionless), using the procedure described in Section 7.2.3. The expected histogram mean is 21000.0. The measured mean value is 21613.653. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 20000.0 and 23000.0 with a yield of 99 %. Due to its calculation of , this wafer probing test can be classified as a characterization test. The probability map in Figure F.32(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, since the shunt regulators are set off to the bottom left. The average yield however is higher, since the dominant cut criterion for the shunt regulator block is defined in Section F.2.15.

F.2.32 Temperature A Sensor

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.7.



(a) Histogram of Temperature A Sensor

(b) Averaged Wafer map of Temperature A Sensor

Figure F.33: Test result plots of wafer probing test Temperature A Sensor

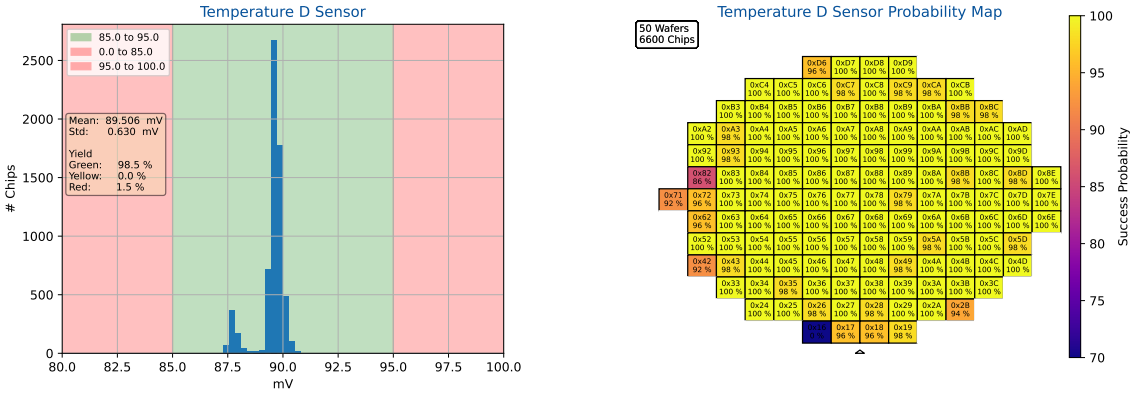
Cuts [mV]						Distribution [mV]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	89.439	**Green**	99
High	85.0		95.0		100.0	**Std.**	0.644	**Yellow**	0
Low	0.0		85.0		95.0	**Char.**	Yes	**Red**	1

Table F.38: Summary of wafer probing test Temperature A Sensor

This wafer probing test aims to characterize ITkPixV1.1s analog shunt regulator diode temperature sensor. The measured values are histogrammed in Figure F.33(a). Its x-axis shows the measured delta voltage in mV, using the procedure described in Section 7.2.7. The expected histogram mean is 85.873 mV. The measured mean value is 89.439 mV. The expected histogram mean is calculated using Equation 6.1, with a non linearity factor of 1.24 as acquired from simulation and mean room temperature of 23.61 °C. The offset between expected delta voltage and measured delta voltage suggests, that the NTC on the probe card is an insufficient temperature reference. The standard deviation of the measured delta voltages suggests a temperature variation of 2.18 °C, including the small peak (0.7 °C without the small peak) on the left of Figure F.35(a).This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 85.0 mV and 95.0 mV with a yield of 99 %. Due to its calculation of the delta voltage for the ITkPixV1.1 temperature sensor calibration, this wafer probing test can be classified as a characterization test. The probability map in Figure F.33(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, plus statistical fluctuation.

F.2.33 Temperature D Sensor

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.7.



(a) Histogram of Temperature D Sensor

(b) Averaged Wafer map of Temperature D Sensor

Figure F.34: Test result plots of wafer probing test Temperature D Sensor

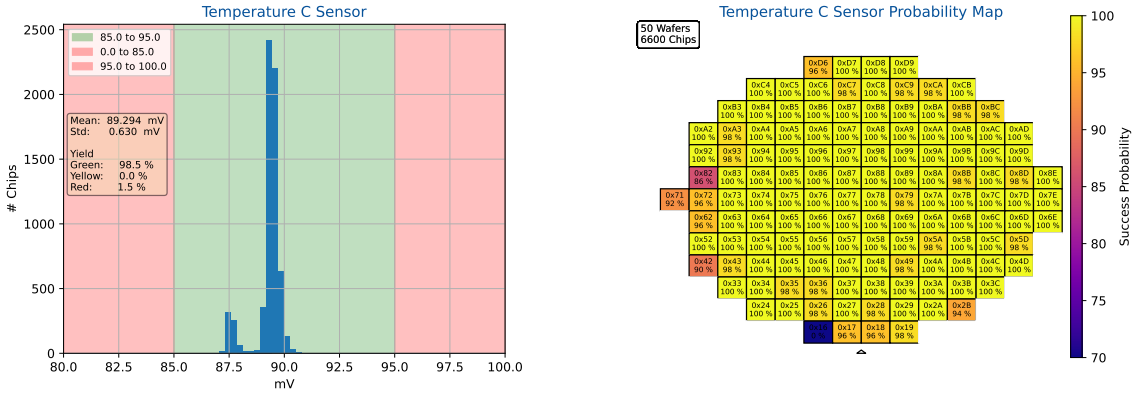
Cuts [mV]						Distribution [mV]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	89.506	**Green**	99
High	85.0		95.0		100.0	**Std.**	0.63	**Yellow**	0
Low	0.0		85.0		95.0	**Char.**	Yes	**Red**	1

Table F.39: Summary of wafer probing test Temperature D Sensor

This wafer probing test aims to characterize ITkPixV1.1s digital shunt regulator diode temperature sensor. The measured values are histogrammed in Figure F.34(a). Its x-axis shows the measured delta voltage in mV, using the procedure described in Section 7.2.7. The expected histogram mean is 85.873 mV. The measured mean value is 89.506 mV. The expected histogram mean is calculated using Equation 6.1, with a non linearity factor of 1.24 as acquired from simulation and mean room temperature of 23.61 °C. The offset between expected delta voltage and measured delta voltage suggests, that the NTC on the probe card is an insufficient temperature reference. The standard deviation of the measured delta voltages suggests a temperature variation of 2.18 °C, including the small peak (0.7 °C without the small peak) on the left of Figure F.35(a).This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 85.0 mV and 95.0 mV with a yield of 99 %. Due to its calculation of the delta voltage for the ITkPixV1.1 temperature sensor calibration, this wafer probing test can be classified as a characterization test. The probability map in Figure F.34(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, plus statistical fluctuation. An indepth discussion of an equivalent measurement can be found in Section F.2.34.

F.2.34 Temperature C Sensor

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.7.



(a) Histogram of Temperature C Sensor

(b) Averaged Wafer map of Temperature C Sensor

Figure F.35: Test result plots of wafer probing test Temperature C Sensor

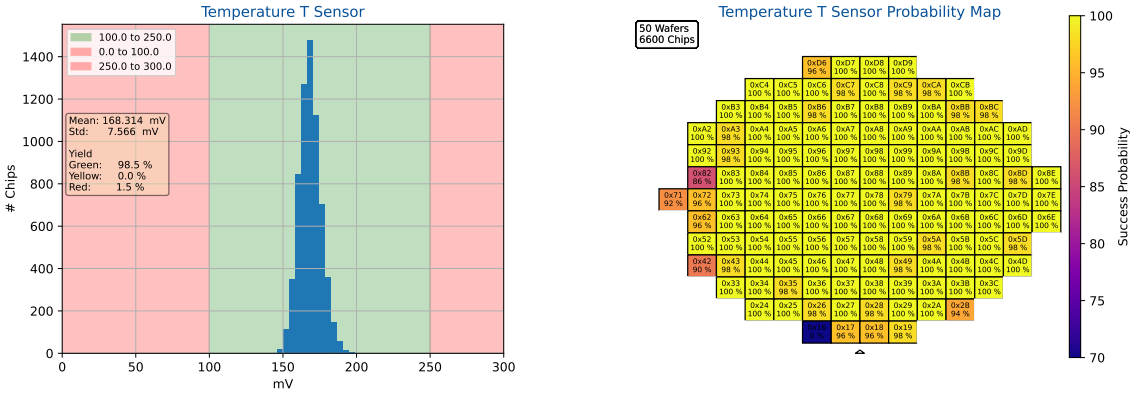
Cuts [mV]						Distribution [mV]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	89.294	**Green**	99
High	85.0		95.0		100.0	**Std.**	0.63	**Yellow**	0
Low	0.0		85.0		95.0	**Char.**	Yes	**Red**	1

Table F.40: Summary of wafer probing test Temperature C Sensor

This wafer probing test aims to characterize ITkPixV1.1s central diode temperature sensor. The measured values are histogrammed in Figure F.35(a). Its x-axis shows the measured delta voltage in mV, using the procedure described in Section 7.2.7. The expected histogram mean is 85.873 mV. The measured mean value is 89.294 mV. The expected histogram mean is calculated using Equation 6.1, with a non linearity factor of 1.24 as acquired from simulation and mean room temperature of 23.61 °C. The offset between expected delta voltage and measured delta voltage suggests, that the NTC on the probe card is an insufficient temperature reference. The standard deviation of the measured delta voltages suggests a temperature variation of 2.18 °C, including the small peak (0.7 °C without the small peak) on the left of Figure F.35(a).This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 85.0 mV and 95.0 mV with a yield of 99 %. Due to its calculation of the delta voltage for the ITkPixV1.1 temperature sensor calibration, this wafer probing test can be classified as a characterization test. The probability map in Figure F.35(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, plus statistical fluctuation.

F.2.35 Temperature T Sensor

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.7.



(a) Histogram of Temperature T Sensor

(b) Averaged Wafer map of Temperature T Sensor

Figure F.36: Test result plots of wafer probing test Temperature T Sensor

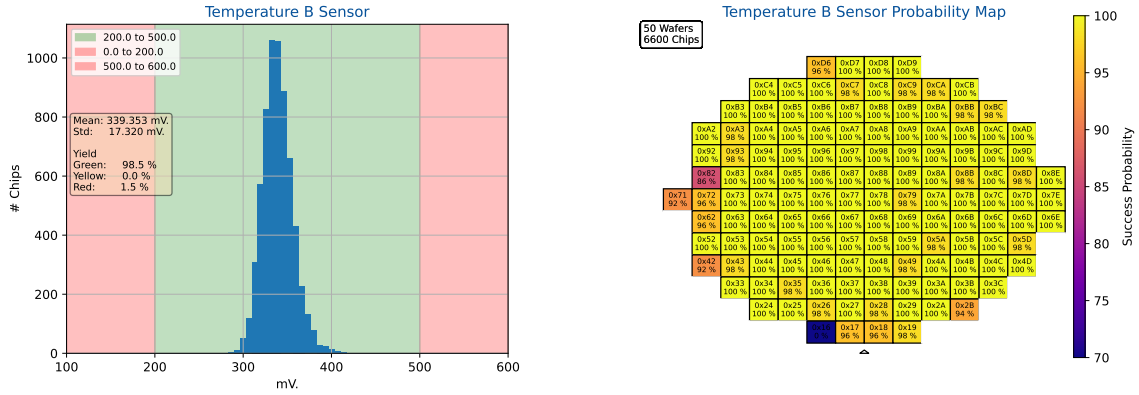
Cuts [mV]						Distribution [mV]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	168.314	**Green**	99
High	100.0		250.0		300.0	**Std.**	7.566	**Yellow**	0
Low	0.0		100.0		250.0	**Char.**	Yes	**Red**	1

Table F.41: Summary of wafer probing test Temperature T Sensor

This wafer probing test aims to characterize ITkPixV1.1s poly silicone temperature sensor at the top of the matrix. The measured values are histogrammed in Figure F.36(a). Its x-axis shows the measured voltage drop over the polysilicone resistor, using the procedure described in Section 7.2.7. The expected histogram mean is 0.32 mV. The measured mean value is 168.314 mV. The deviation between expected and measured value is related to an issue in the doping of the top polysislicone temperature sensor.This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 100.0 mV and 250.0 mV with a yield of 99 %. Due to its calculation of the voltage of the top poly silicone temperautre sensor, this wafer probing test can be classified as a characterization test. The probability map in Figure F.36(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, plus statistical fluctuation.

F.2.36 Temperature B Sensor

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.7.



(a) Histogram of Temperature B Sensor

(b) Averaged Wafer map of Temperature B Sensor

Figure F.37: Test result plots of wafer probing test Temperature B Sensor

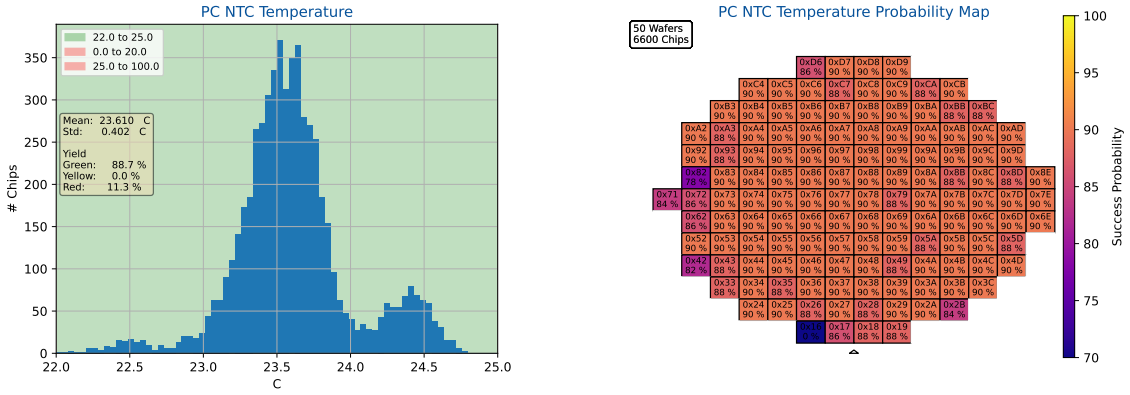
Cuts [mV.]						Distribution [mV.]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	339.353	**Green**	99
High	200.0		500.0		600.0	**Std.**	17.32	**Yellow**	0
Low	0.0		200.0		500.0	**Char.**	Yes	**Red**	1

Table F.42: Summary of wafer probing test Temperature B Sensor

This wafer probing test aims to characterize ITkPixV1.1s poly silicone temperature sensor at the bottom of the matrix. The measured values are histogrammed in Figure F.37(a). Its x-axis shows the measured voltage drop over the polysilicone resistor, using the procedure described in Section 7.2.7. The expected histogram mean is 0.32 mV. The measured mean value is 339.353 mV. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 200.0 mV and 500.0 mV with a yield of 99 %. Due to its calculation of the voltage of the bottom poly silicone temperature sensor at room temperature, this wafer probing test can be classified as a characterization test. The probability map in Figure F.37(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, plus statistical fluctuation.

F.2.37 PC NTC Temperature

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 7.2.7.



(a) Histogram of PC NTC Temperature

(b) Averaged Wafer map of PC NTC Temperature

Figure F.38: Test result plots of wafer probing test PC NTC Temperature

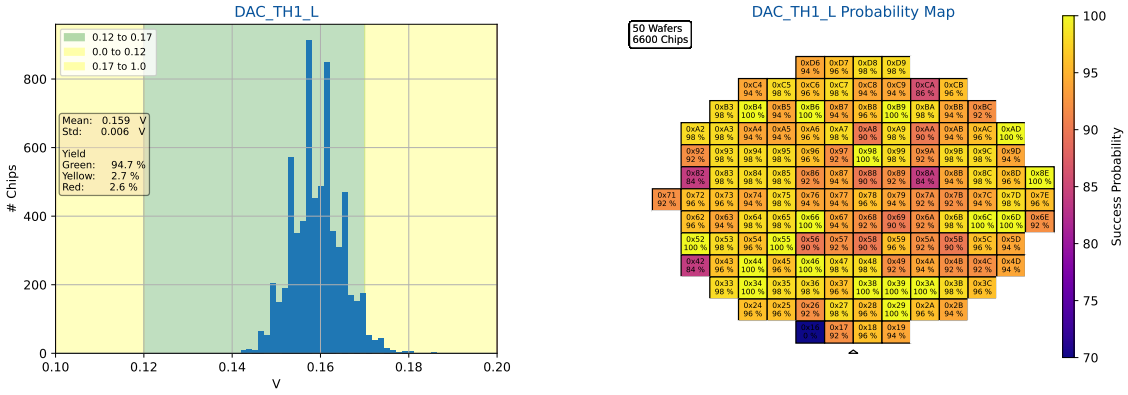
Cuts [extcelsius]						Distribution [extcelsius]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	23.61	**Green**	89
High	20.0		25.0		100.0	**Std.**	0.402	**Yellow**	0
Low	0.0		22.0		25.0	**Char.**	Yes	**Red**	11

Table F.43: Summary of wafer probing test PC NTC Temperature

This wafer probing test aims to characterize ITkPixV1.1s environmental temperature, measured on the probe card. The measured values are histogrammed in Figure F.38(a). Its x-axis shows the measured temperature in °C, using the procedure described in Section 7.2.7. The expected histogram mean is . The measured mean value is 23.61 °C. It is known, that the air-condition in the clean room was set do different temperatures from time to time, due to a neighboring experiment. Other than that, an observed standard deviation for 6600 measurement points distributed, over a year is well within expectation.This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 22.0 °C and 25.0 °C with a yield of 89 %. Due to its calculation of the enviromental temperature as a reference for ITkPixV1.1s temperature sensor calibration, this wafer probing test can be classified as a characterization test. The probability map in Figure F.38(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits no relevant information about any ITkPixV1.1 properties, since the measurement is solely based on an external probe card NTC. Please note, that chips, which failed eralier tests exhibit a lower success probability, since following tests are no longer conducted.

F.2.38 DAC TH1 L

The data for this wafer probing test was acquired using the wafer probing routine as described in Section F.1.6.



(a) Histogram of DAC TH1 L

(b) Averaged Wafer map of DAC TH1 L

Figure F.39: Test result plots of wafer probing test DAC TH1 L

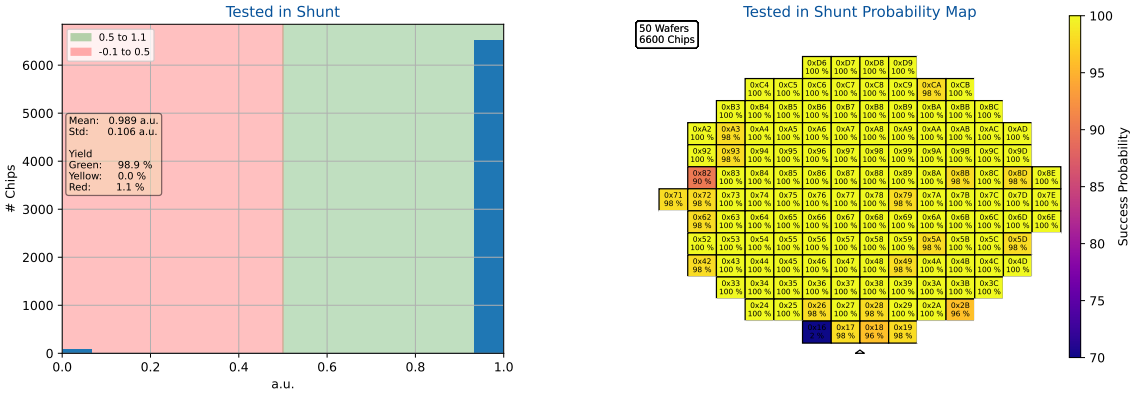
Cuts [V]						Distribution [V]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.159	**Green**	95
High		0.12	0.17	1.0		**Std.**	0.006	**Yellow**	3
Low		0.0	0.12	0.17		**Char.**	Yes	**Red**	3

Table F.44: Summary of wafer probing test DAC TH1 L

This wafer probing test aims to characterize ITkPixV1.1s threshold voltage (DAC TH1) at a DAC setting of 220, after VDDD, VDDA and IREF trimming. The measured values are histogrammed in Figure F.39(a). Its x-axis shows the measured DAC TH 1 in V, using the procedure described in Section F.1.6. The expected histogram mean is 0.16 V. The measured mean value is 0.159 V, which is, considering the measured standard deviation of 0.006 V, in good agreement with the expected value. This wafer probing test differentiates between green and yellow ITkPixV1.1. Green chips are qualified as such between 0.12 V and 0.17 V with a yield of 95 %. Due to its calculation of the DAC TH1 voltage, this wafer probing test can be classified as a characterization test. The probability map in Figure F.39(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits similar features as discussed in Section F.2.1, but no additional gradient, which excludes a systematic production error.

F.2.39 Tested in Shunt

The data for this wafer probing test was acquired using the wafer probing routine as described in Section F.1.1.



(a) Histogram of Tested in Shunt

(b) Averaged Wafer map of Tested in Shunt

Figure F.40: Test result plots of wafer probing test Tested in Shunt

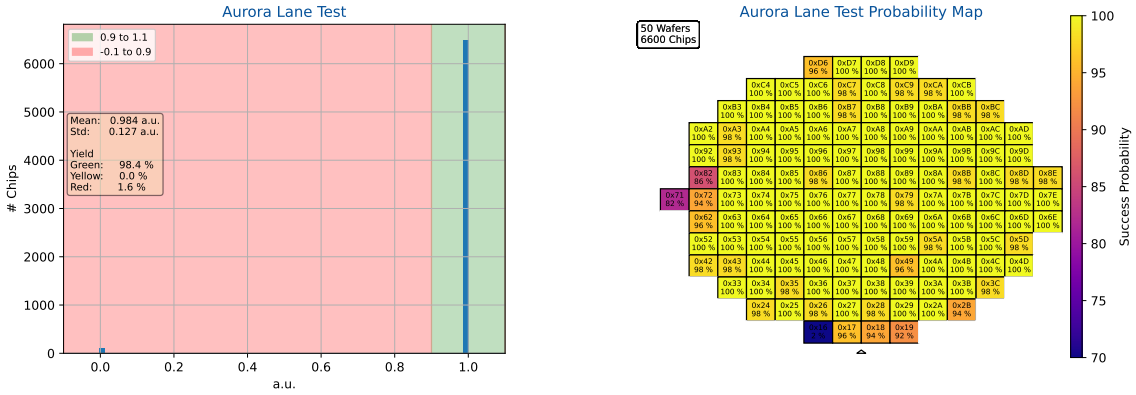
Cuts [a.u.]						Distribution [a.u.]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.989	**Green**	99
High	0.5		1.1			**Std.**	0.106	**Yellow**	0
Low	-0.1		0.5			**Char.**	No	**Red**	1

Table F.45: Summary of wafer probing test Tested in Shunt

This wafer probing test is the 17th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s capability to run all wafer probing tests in shunt LDO mode. The measured values are histogrammed in Figure F.40(a). Its x-axis shows whether aurora lane communication can be established in shunt LDO mode at 1.6 V, using the procedure described in Section F.1.1. The expected histogram mean is 1.0. The measured mean value is 0.989, which is, considering the measured standard deviation of 0.106, in good agreement with the expected value. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.5 and 1.1 with a yield of 99 %. Chips are classified as not green if they cannot establish aurora lane communication in shunt LDO mode. Since the functionality tested in this wafer probing test is a key element of ITkPixV1.1, during operation in ITk, it can be classified as a functionality test. The probability map in Figure F.40(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits a uniformly high success probability with the regular chips in the left with a slightly higher failure probability.

F.2.40 Aurora Lane Test

The data for this wafer probing test was acquired using the wafer probing routine as described in Section F.1.8.



(a) Histogram of Aurora Lane Test

(b) Averaged Wafer map of Aurora Lane Test

Figure F.41: Test result plots of wafer probing test Aurora Lane Test

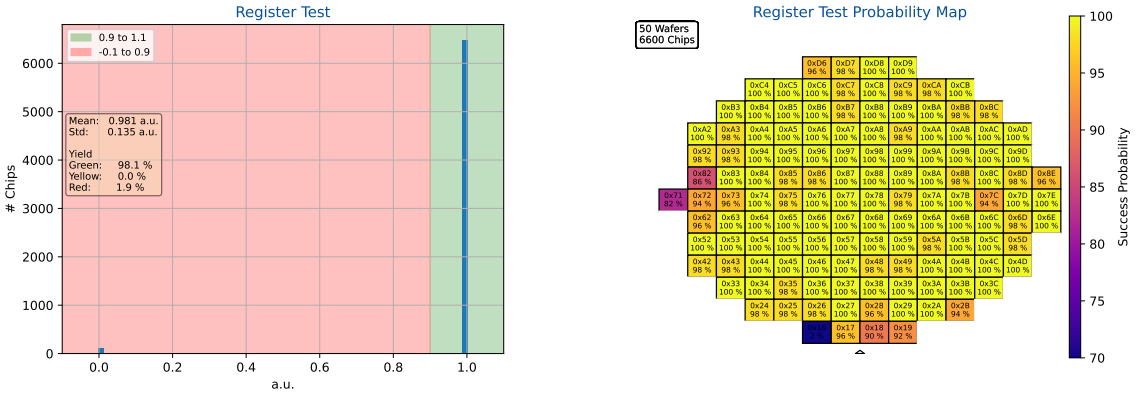
Cuts [a.u.]						Distribution [a.u.]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.984	**Green**	98
High	0.9		1.1			**Std.**	0.127	**Yellow**	0
Low	-0.1		0.9			**Char.**	No	**Red**	2

Table F.46: Summary of wafer probing test Aurora Lane Test

This wafer probing test is the 8th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s aurora output lanes. The measured values are histogrammed in Figure F.41(a). Its x-axis shows whether all four aurora lanes are working, using the procedure described in Section F.1.8. The expected histogram mean is 1.0. The measured mean value is 0.984, which is, considering the measured standard deviation of 0.127, in good agreement with the expected value. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.9 and 1.1 with a yield of 98 %. Chips are classified as not green if one ore more aurora lane is not working. Since the functionality tested in this wafer probing test is a key element of ITkPixV1.1, during operation in ITk, it can be classified as a functionality test. The probability map in Figure F.41(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.42, since both wafer probing tests require aurora lane communciation to work. Plus a few extra failing chips, since in this wafer probing test chips, which have already one failing aurora lane are classfied as red.

F.2.41 Register Test

The data for this wafer probing test was acquired using the wafer probing routine as described in Section F.1.9.



(a) Histogram of Register Test

(b) Averaged Wafer map of Register Test

Figure F.42: Test result plots of wafer probing test Register Test

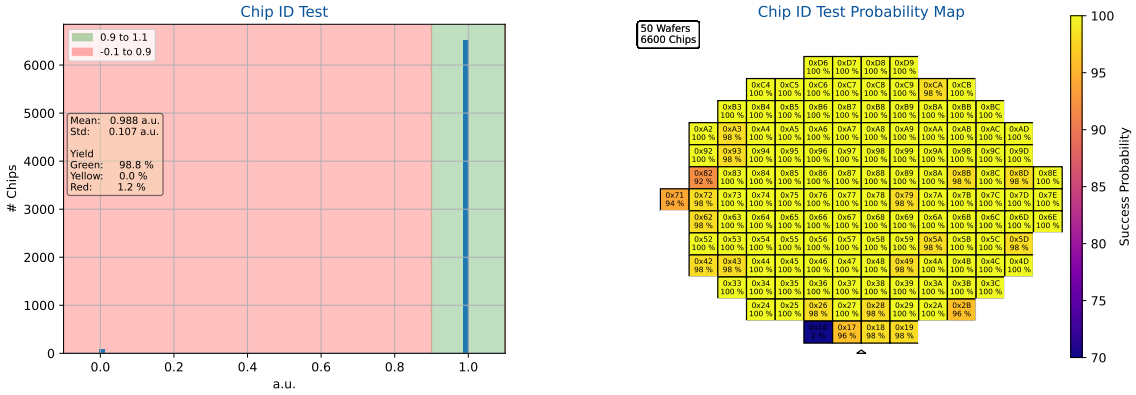
Cuts [a.u.]						Distribution [a.u.]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.981	**Green**	98
High	0.9		1.1			**Std.**	0.135	**Yellow**	0
Low	-0.1		0.9			**Char.**	No	**Red**	2

Table F.47: Summary of wafer probing test Register Test

This wafer probing test is the 13th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s read- and write-ability of all global registers. The measured values are histogrammed in Figure F.42(a). Its x-axis shows whether all bits in all testable global registers work in their on and off state, using the procedure described in Section F.1.9. The expected histogram mean is 1.0. The measured mean value is 0.981, which is, considering the measured standard deviation of 0.135, in good agreement with the expected value. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.9 and 1.1 with a yield of 98 %. Chips are classified as not green if one or more register bit is broken. Since the functionality tested in this wafer probing test is a key element of ITkPixV1.1, during operation in ITk, it can be classified as a functionality test. The probability map in Figure F.42(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.42, since both wafer probing tests require aurora lane communciation to work. A few extra ITkPixV1.1 fail here, since more registers are tested.

F.2.42 Chip ID Test

The data for this wafer probing test was acquired using the wafer probing routine as described in Section F.1.3.



(a) Histogram of Chip ID Test

(b) Averaged Wafer map of Chip ID Test

Figure F.43: Test result plots of wafer probing test Chip ID Test

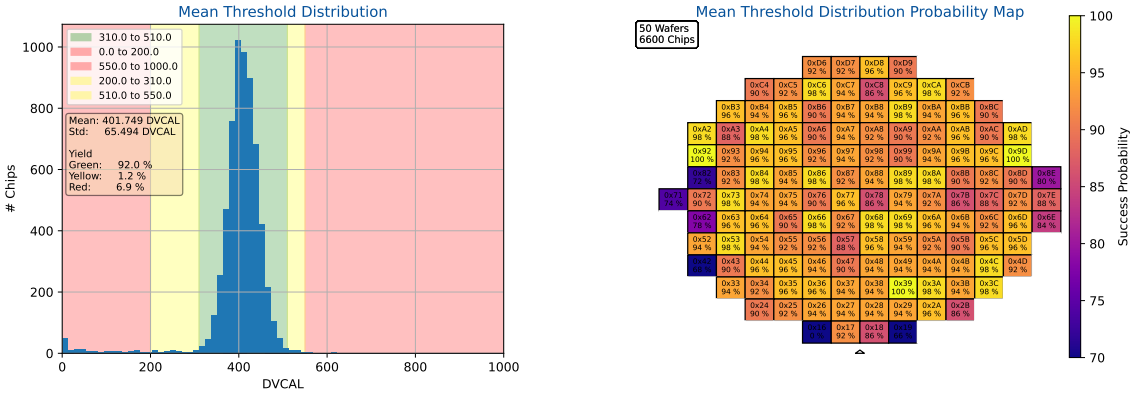
Cuts [a.u.]						Distribution [a.u.]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.988	**Green**	99
High	0.9		1.1			**Std.**	0.107	**Yellow**	0
Low	-0.1		0.9			**Char.**	No	**Red**	1

Table F.48: Summary of wafer probing test Chip ID Test

This wafer probing test is the 18th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s adress bits. Each command, sent as described in the "Command and Trigger Encoding" Table [44], contains a 4 bit address. This address can be defined by pulling four wire-bonding pads high or low. This wafer probing test ensures, that none of the four pads is constantly stuck high or low. The measured values are histogrammed in Figure F.43(a). Its x-axis shows whether all four chip id bits work or not, using the procedure described in Section F.1.3. The expected histogram mean is 1.0. The measured mean value is 0.988, which is, considering the measured standard deviation of 0.107, in good agreement with the expected value. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.9 and 1.1 with a yield of 99 %. Chips are classified as not green if one or more of the four address bits is broken. Since the functionality tested in this wafer probing test is a key element of ITkPixV1.1, during operation in ITk, it can be classified as a functionality test. The probability map in Figure F.43(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same gradient features as discussed in Section F.2.1. This test is highly correlated with the test in Section F.2.1, since all ITkPixV1.1, which have an untunable IREF current are incapable of establishing aurora lane communication.

F.2.43 Mean Threshold Distribution

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 4.1.3.



(a) Histogram of Mean Threshold Distribution

(b) Averaged Wafer map of Mean Threshold Distribution

Figure F.44: Test result plots of wafer probing test Mean Threshold Distribution

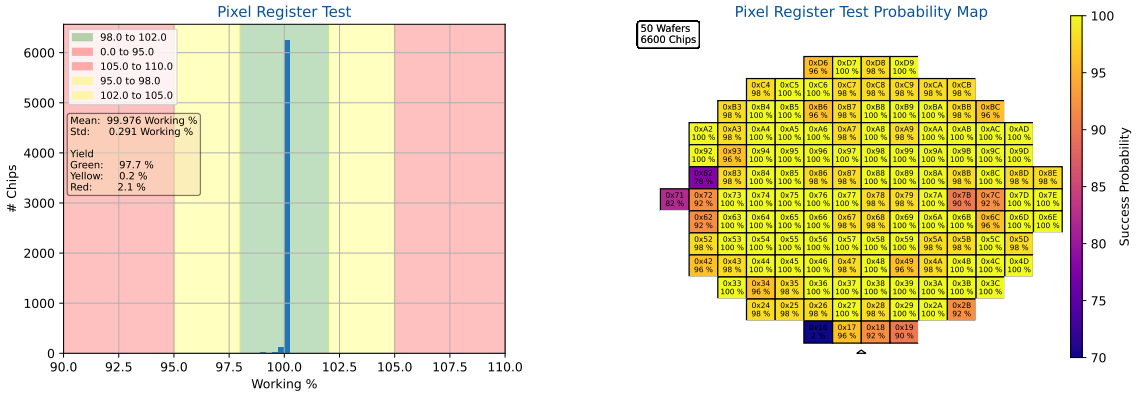
Cuts [DVCAL]						Distribution [DVCAL]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	401.749	**Green**	92
High	200.0	310.0	510.0	550.0	1000.0	**Std.**	65.494	**Yellow**	1
Low	0.0	200.0	310.0	510.0	550.0	**Char.**	No	**Red**	7

Table F.49: Summary of wafer probing test Mean Threshold Distribution

This wafer probing test is the 1st most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s detection threshold. The measured values are histogrammed in Figure F.44(a). Its x-axis shows the mean measured detection threshold for all pixel, using the procedure described in Section 4.1.3. The expected histogram mean is 410.0 delta vcal. The measured mean value is 401.749 delta vcal, which is, considering the measured standard deviation of 65.494 delta vcal, in good agreement with the expected value. This wafer probing test differentiates between green, yellow, and red ITkPixV1.1. Green chips are qualified as such between 310.0 delta vcal and 510.0 delta vcal with a yield of 92 %. Chips are classified as not green if the mean detection threshold is too far away from the expected threshold, which would put the tunability of the tested ITkPixV1.1 in question. Due to its calculation of the mean detection threshold, this wafer probing test can be classified as a characterization test, as well as a functionality test, due to the tested functionality being a key element of ITkPixV1.1, during operation in ITk. The probability map in Figure F.44(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same gradient features as discussed in Section F.2.45. This test is highly correlated with the test in Section F.2.45, since all ITkPixV1.1, which have non working pixels, will also not be capable of producing an S-curve within the green cut-values.

F.2.44 Pixel Register Test

The data for this wafer probing test was acquired using the wafer probing routine as described in Section F.1.11.



(a) Histogram of Pixel Register Test

(b) Averaged Wafer map of Pixel Register Test

Figure F.45: Test result plots of wafer probing test Pixel Register Test

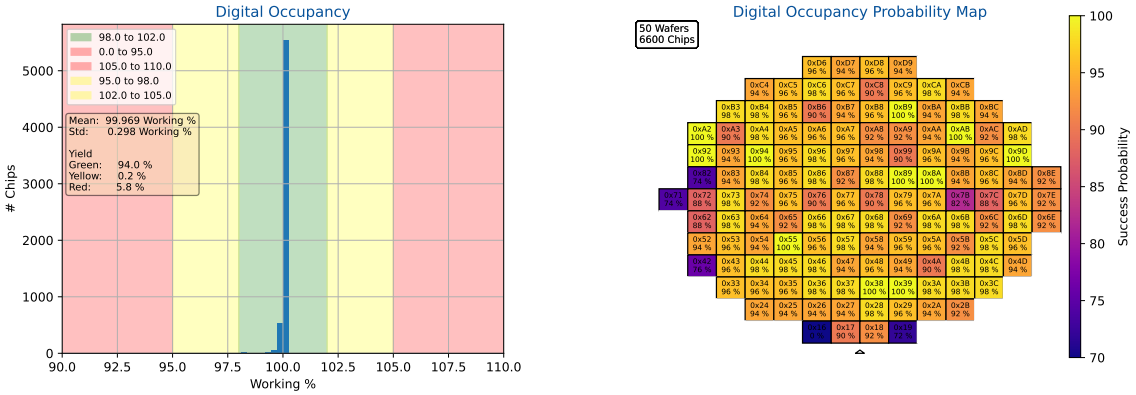
Cuts [Working %]						Distribution [Working %]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	99.976	**Green**	98
High	95.0	98.0	102.0	105.0	110.0	**Std.**	0.291	**Yellow**	0
Low	0.0	95.0	98.0	102.0	105.0	**Char.**	No	**Red**	2

Table F.50: Summary of wafer probing test Pixel Register Test

This wafer probing test is the 7th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s pixel configuration bits. The measured values are histogrammed in Figure F.45(a). Its x-axis shows the percentile of pixels with fully working pixel configuration bits, using the procedure described in Section F.1.11. The expected histogram mean is 100.0. The measured mean value is 99.976, which is, considering the measured standard deviation of 0.291, in good agreement with the expected value. This wafer probing test differentiates between green, yellow, and red ITkPixV1.1. Green chips are qualified as such between 98.0 and 102.0 with a yield of 98 %. Chips are classified as not green if they feature more than 2 % or 3072 non working pixel, which is equivalent to one non working core column. Since the functionality tested in this wafer probing test is a key element of ITkPixV1.1, during operation in ITk, it can be classified as a functionality test. The probability map in Figure F.45(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same bias as observed in the first aurora lane communication wafer probing tests, plus an unbiased randomly distributed cut for all ITkPixV1.1, which have more than 2 % non working pixels. It may be noted, that this test never failed, without the analog, digital or threshold scan failing, which require the pixel matrix registers to work. This suggests that this scan could be left out in future ITk production wafer probing testing.

F.2.45 Digital Occupancy

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 4.1.3.



(a) Histogram of Digital Occupancy

(b) Averaged Wafer map of Digital Occupancy

Figure F.46: Test result plots of wafer probing test Digital Occupancy

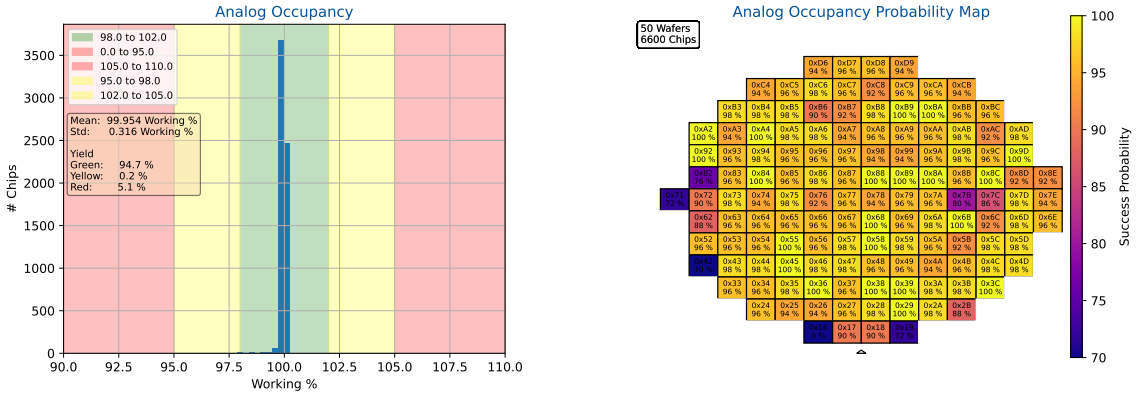
Cuts [Working %]						Distribution [Working %]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	99.969	**Green**	94
High	95.0	98.0	102.0	105.0	110.0	**Std.**	0.298	**Yellow**	0
Low	0.0	95.0	98.0	102.0	105.0	**Char.**	No	**Red**	6

Table F.51: Summary of wafer probing test Digital Occupancy

This wafer probing test is the 2nd most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s digital pixel matrix readout. The measured values are histogrammed in Figure F.46(a). Its x-axis shows the percentile of working pixels, using the procedure described in Section 4.1.3. The expected histogram mean is 100.0 % working pixel. The measured mean value is 99.969 % working pixel, which is, considering the measured standard deviation of 0.298 % working pixel, in good agreement with the expected value. This wafer probing test differentiates between green, yellow, and red ITkPixV1.1. Green chips are qualified as such between 98.0 % working pixel and 102.0 % working pixel with a yield of 94 %. Chips are classified as not green if they feature more than 2 % or 3072 non working pixel, which is equivalent to one non working core column. Since the functionality tested in this wafer probing test is a key element of ITkPixV1.1, during operation in ITk, it can be classified as a functionality test. The probability map in Figure F.46(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same bias as observed in the very first aurora lane communication wafer probing tests, plus an unbiased randomly distributed cut for all ITkPixV1.1, which have more than 2 % non working pixels.

F.2.46 Analog Occupancy

The data for this wafer probing test was acquired using the wafer probing routine as described in Section 4.1.3.



(a) Histogram of Analog Occupancy

(b) Averaged Wafer map of Analog Occupancy

Figure F.47: Test result plots of wafer probing test Analog Occupancy

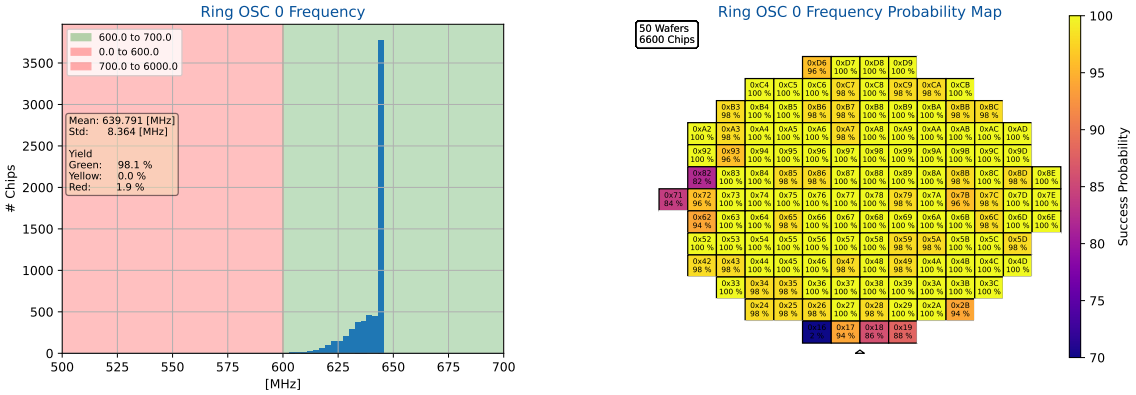
Cuts [Working %]						Distribution [Working %]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	99.954	**Green**	95
High	95.0	98.0	102.0	105.0	110.0	**Std.**	0.316	**Yellow**	0
Low	0.0	95.0	98.0	102.0	105.0	**Char.**	No	**Red**	5

Table F.52: Summary of wafer probing test Analog Occupancy

This wafer probing test is the 3rd most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s analog front ends in the pixel matrix. The measured values are histogrammed in Figure F.47(a). Its x-axis shows the percentile of working analog front ends, using the procedure described in Section 4.1.3. The expected histogram mean is 100.0 % working pixel. The measured mean value is 99.954 % working pixel, which is, considering the measured standard deviation of 0.316 % working pixel, in good agreement with the expected value. This wafer probing test differentiates between green, yellow, and red ITkPixV1.1. Green chips are qualified as such between 98.0 % working pixel and 102.0 % working pixel with a yield of 95 %. Chips are classified as not green if they feature more than 2 % or 3072 non working pixel, which is equivalent to one non working core column. Since the functionality tested in this wafer probing test is a key element of ITkPixV1.1, during operation in ITk, it can be classified as a functionality test. The probability map in Figure F.47(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as observed in the aurora lane communication test, as described in Section F.2.41. On first sight it is counterintuitive, that this test is more likely to succeed, than the Digital Occupancy wafer probing test addressed in Section F.2.45. However, this test, is conducted in precision Tot mode, which circumvents the digital readout of each individual pixel. .

F.2.47 Ring OSC 0 Frequency

The data for this wafer probing test was acquired using the wafer probing routine as described in Section F.1.10.



(a) Histogram of Ring OSC 0 Frequency

(b) Averaged Wafer map of Ring OSC 0 Frequency

Figure F.48: Test result plots of wafer probing test Ring OSC 0 Frequency

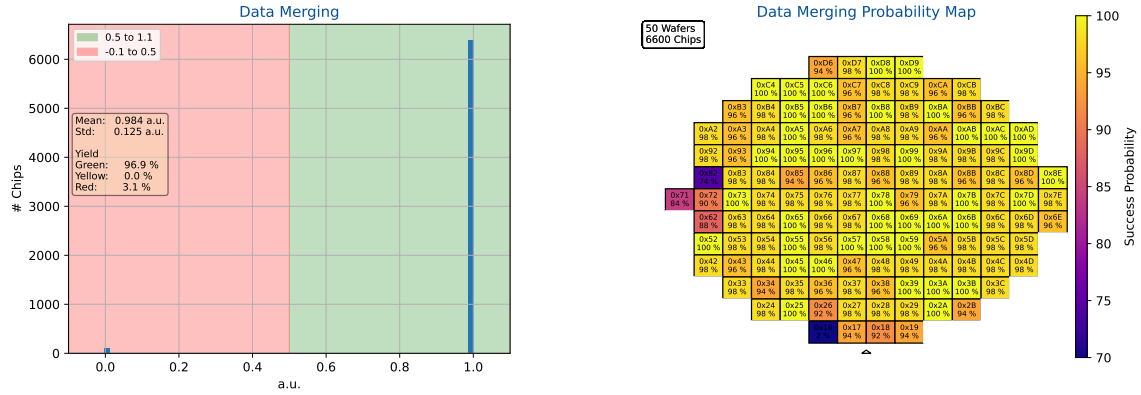
Cuts [MHz]						Distribution [MHz]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	639.791	**Green**	98
High	600.0		700.0		6000.0	**Std.**	8.364	**Yellow**	0
Low	0.0		600.0		700.0	**Char.**	Yes	**Red**	2

Table F.53: Summary of wafer probing test Ring OSC 0 Frequency

This wafer probing test aims to characterize ITkPixV1.1s ring oscillator 0. ITkPixV1.1 features many ring oscillator this wafer probing test aims to be an example for all such measurements. The measured values are histogrammed in Figure F.48(a). Its x-axis shows the measured ring oscillator frequency in MHz, using the procedure described in Section F.1.10. The expected histogram mean is 644.882 MHz. The measured mean value is 639.791 MHz, which is, considering the measured standard deviation of 8.364 MHz, in good agreement with the expected value. Is what one would usually think, however the super high peak at the maximum frequency is striking. Usually a sharp gaussian distribution would be expected. The distorted distribution is related to a too long sampling time for the ring oscillator measurement, where the frequency counter saturates before the measurement ends. This problem has been addressed in the code, by reducing the global pulse length, which defines the sampling time. Unfortunately this will only take effect after ITk pre-production.This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 600.0 MHz and 700.0 MHz with a yield of 98 %. Due to its calculation of the the ring oscillator frequency, this wafer probing test can be classified as a characterization test. The probability map in Figure F.48(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as observed in the aurora lane communication test, since this test requires not much more than aurora lane communication to work.

F.2.48 Data Merging

The data for this wafer probing test was acquired using the wafer probing routine as described in Section F.1.7.



(a) Histogram of Data Merging

(b) Averaged Wafer map of Data Merging

Figure F.49: Test result plots of wafer probing test Data Merging

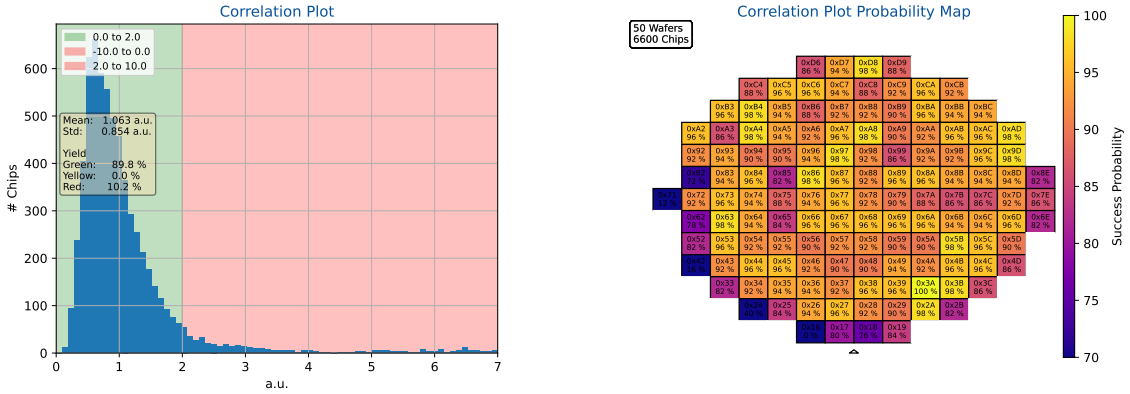
Cuts [a.u.]						Distribution [a.u.]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	0.984	**Green**	97
High	0.5		1.1			**Std.**	0.125	**Yellow**	0
Low	-0.1		0.5			**Char.**	No	**Red**	3

Table F.54: Summary of wafer probing test Data Merging

This wafer probing test is the 5th most likely not to be green among all 21 functionality tests. It aims to test ITkPixV1.1s data merging input lanes functionality. The measured values are histogrammed in Figure F.49(a). Its x-axis shows whether all four data-merging input lanes work, using the procedure described in Section F.1.7. The expected histogram mean is 1.0. The measured mean value is 0.984, which is, considering the measured standard deviation of 0.125, in good agreement with the expected value. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.5 and 1.1 with a yield of 97 %. Chips are classified as not green if one or more of the four data-merging input lanes are non functional. Since the functionality tested in this wafer probing test is a key element of ITkPixV1.1, during operation in ITk, it can be classified as a functionality test. The probability map in Figure F.49(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the same features as discussed in Section F.2.1, plus statistical fluctuation.

F.2.49 Correlation Plot

The data for this wafer probing test was acquired using all wafer probing tests as described in this Section, which exhibit a Gaussian-like distribution.



(a) Histogram of Correlation Plot

(b) Averaged Wafer map of Correlation Plot

Figure F.50: Test result plots of wafer probing test Correlation Plot

Cuts [a.u.]						Distribution [a.u.]		Yield [%]	
	Red	Yellow	Green	Yellow	Red	**Mean**	1.063	**Green**	90
High	0.0		2.0		10.0	**Std.**	0.854	**Yellow**	0
Low	-10.0		0.0		2.0	**Char.**	Yes	**Red**	10

Table F.55: Summary of wafer probing test Correlation Plot

This wafer probing test is an analysis of the mean distance of a measurement result of chips from a Gaussian distributed mean, normalized by its standard deviation (D_{chip}). It aims to visualize whether chips are rejected in many wafer probing tests or whether they perform badly in one particular wafer probing test. The measured values are histogrammed in Figure F.50(a). Its x-axis shows D_{chip} in arbitrary units. The D_{chip} is calculated as shown in Equation (F.1).

$$D_{chip} = \frac{1}{n}\sum_{k=1}^{n}\frac{(\mu_k - x_k)}{\sigma_k} \tag{F.1}$$

Its y-axis shows the number of chips with the particular x value. The expected histogram mean is 1. The measured mean value is 1.063. With a standard deviation of 0.854 this is in good agreement with the measurement. This wafer probing test differentiates between green and red ITkPixV1.1. Green chips are qualified as such between 0.0 and 2.0 with a yield of 90 %. Due to its calculation of D_{chip}, this wafer probing test can be classified as characterization test. The probability map in Figure F.50(b) shows the mean probability of all tested ITkPixV1.1 to be green. It exhibits the known patterns, with ITkPixV1.1 in the center exhibiting a higher success probability than at the edges.

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Glossary

ADC An analog to digital converter (ADC) is a circuit, which compares an in coming voltage to a reference voltage and indicates its value relative to the incoming voltage in bits. Hence the name analog voltage to digital value converter. Please note that the incoming voltage must be lower than the reference voltage. 23, 46–49, 51–54, 72, 81–83, 87, 88, 135, 136, 178, 179, 190

ALICE A Large Ion Collider Experiment is one of the four main detectors at the LHC. It is specialized in studying heavy-ion (Pb-Pb nuclei) collisions. 2, 3, 177

analog front end This is an analog circuit inside each pixel of the readout chip (e.g. RD53A, ITkPixV1.1, which integrates the charge received from sensor or injection capacitance to output a digital signal to the data encoder. The analog front end significantly influences the capability of readout chip to detect low charges in time with low energy consumption. 18, 19, 21, 29, 30, 38, 43, 45, 59–62, 64, 65, 68, 69, 73, 77, 79, 81, 84, 91, 92, 99, 162, 179, 185–188, 190–194

analog monitoring board The analog monitoring board is an extension board for the Single-Chip Card, enabling easy manipulation and measurement of the monitoring pins on the Single-Chip Card. For more information, see Section 6.1. 44–46, 48, 178

analog scan An analog scan is a scan, which injects a charge into the analog front end of a pixel, sends a trigger and checks whether the hit was detected, testing the whole signal chain from charge, over analog front end to readout logic. 30, 85, 87, 88, 94

ATLAS A Toroidal LHC Apparatus - One of two general purpose particle detectors at the LHC. General purpose hereby refers to its ability to reconstruct a large solid angle detecting many particles momenta and energies. v, 1–8, 14, 15, 18, 53, 76, 91, 92, 105, 111, 112, 177, 187, 190

aurora lane An aurora lane references to one of four data transmission lanes of the RD53B chip. Aurora is a Xilinx implementation of a 66/68bit encoded point to point link layer protocol, in the case of RD53B running at either 640 MHz or 1 280 MHz [64]. 55, 56, 88, 113, 114, 155–158, 160–163, 186

BDAQ53 Bonn DAQ is the Read-Out-System developed in Bonn to test chips developed by the RD53 Collaboration. 25–29, 31, 32, 35–41, 44, 45, 54–57, 62, 71, 91, 92, 99, 101–105, 112, 113, 177, 178, 180, 187

bunch crossing ID A bunch crossing ID (BCID) is a unique sequential number assigned to each bunch crossing inside of HL-LHC, to keep book about the events recorded in each bunch collision. 2, 31, 43, 62–64, 67, 68, 70, 179, 188

Cal Aux Cal Aux is one the two signals responsible for the rapid switching between vcal high and vcal med. For further information checkout the RD53 Manual [44]. 186

cal command The cal command is used to perform analog or digital injection. For further information checkout the RD53 Manual [44]. 38, 63, 64

Cal Edge CalEdge is one the two signals responsible for the rapid switching between vcal high and vcal med. For further information checkout the RD53 Manual [44]. 39, 186

calibration injection circuit The calibration injection circuit is responsible for injecting charge into the analog front end using vcal high, vcal med, Cal Edge and Cal Aux. Further information on the calibration injection circuit can be found in the RD53 Manual [44]. 38, 39, 59

CERN European Organization for Nuclear Research (French: Conseil européen pour la recherche nucléaire). 4, 9, 18, 192

characterization test A characterization test is a wafer probing test, which tests a chip for a property, featuring a wide acceptable range. Here it is sufficient to know the test value and unnecessary to discard a chip if the value is know for calibration. 115, 116, 118–120, 122, 123, 125–131, 133, 135–154, 159, 163, 165, 180, 183

chip bottom The chip bottom, is the part of RD53B chips, among others, responsible for packing all data received from the matrix and sent it out via the aurora lane to the DAQ. Further information can be found in Section 3.2. 17, 22, 23, 35, 41, 43, 45, 47, 48, 51, 53, 59, 65, 72, 79, 83, 86, 91, 101, 177, 187, 190, 191

CI Continuous integration or CI is a software development practice, which continuously tests new code, which is added to a repository, to prevent e.g. breaking changes. 25, 27, 31, 32, 177

CMS Compact Muon Solenoid - One of two general purpose particle detectors at the LHC. General purpose hereby refers to its ability to reconstruct a large solid angle detecting many particles momenta and energies. 1–4, 18, 105, 177, 186, 187, 190

command encoder The command encoder is responsible for receiving commands form the DAQ and decoding them to control the chip accordingly. In a simplified forms, the encoder can be visualized as a switch board, with one input line, receiving the commands and depending on the received command enabling individual switches on the board. More information can be found in the RD53 manual [44]. 35

core bandgap A core bandgap derives voltages from an intrinsic silicone property, which is stable over large temperature and radiation ranges. 23, 49, 75, 119, 189

core column A core column is a column of pixel cores, which is 8 pixels wide and n pixels long. One core column shares for example the same readout architecture. See also Section 3.1. 40, 77, 94, 95, 160–162, 188

CROC CMS readout chip, is the general term for all silicon chips developed by the RD53 Collaboration with respect to CMS upgrade. All chips developed under this name are manufactured in 65 nm CMOS technology with 432 x 336 pixels and 2 cm x 2 cm in size. 190, 193

CROCV1 CMS readout chip Version 1, is the first full-scale prototype chip for CMS upgrade. This chip was submitted after ITkPixV1.1, incorporating fixes and additional features relevant to ITkPIxV2. 18, 68, 105, 192

CSCs Cathode Strip Chambers. 5

cut-value A cut-value, or cut values, are the values, which define whether a ITkPixV1.1 is classified as green, yellow or red. Those values are summarized in the corresponding Table for each wafer probing test. 116, 122, 125, 159, 188

DAC A DAC is a digital to analog converter, which transforms an input value, into an analog voltage. 23, 39, 61, 72, 81, 82, 87, 88, 137–144, 154, 179, 187, 190, 193, 194

DAQ Data Acquisition Systems are the system behind readout chips collecting data and forwarding it to a PC for further processing. BDAQ53 can be considered as test DAQ in this thesis. 23–25, 27, 28, 37, 71, 74, 84, 91, 186–188, 192, 193

Dark Matter Dark matter is so far a postulated kind of matter thought to account for the majority of gravitationally interacting matter in the universe. Dark matter is considered "dark" because it does not interact electromagnetically, meaning it does not absorb, reflect, or emit e.g. light [98]. 3

data-merging Data-merging, merges the data from two chips into one data stream. Hereby a primary chip receives the data output from a secondary chip at its data-merging input, resamples the data and merges the data from the secondary readout chip into its own data output stream [44]. 18, 23, 28, 44, 45, 53–59, 88, 92, 113, 164, 178

delta vcal Delta Vcal is proportional to the injected charge into the analog front end. It is the delta DAC setting between vcal high and vcal med. As a rule of thumb a charge of 5 e corresponds to one Delta Vcal. 30, 31, 64, 65, 68, 84, 159

detection threshold The detection threshold of an analog front end is determined by the threshold voltage and measured using a threshold scan. The resulting mean of the S-curve, acuired by the threshold scan corresponds to the detection threshold of the given pixel. 14, 30, 31, 43, 59, 63–70, 80, 84–86, 91, 92, 107–109, 159, 179, 180, 188, 192

differential analog front end The differential analog front end is the analog front end incorporated into the ATLAS ITkPix readout chip. Section 3.1 has more details on its functionality. 20, 177

digital pixel logic Digital pixel logic is the digital configuration and processing logic inside each pixel, forwarding hit information to the chip bottom. 19, 187, 191

digital scan A digital scan tests part of the digital pixel logic, behind the analog front end, by injecting a digital pulse, as it would be produced by the comparator output of the analog front end into the digital logic and monitor the response of each pixel, whether the digital pixel logic has processed the digital injection signal correctly. 29, 30, 85, 87, 88

double isolat ITkPixV1.1 wafers come in two flavours, one with double isolation, where an additional deep n-well is implanted below each analog island of each pixel quad. This deep n-well shields the analog front end from noise coupled to the bulk. 63, 64, 109

E-fuse An E-fuse or electronic fuse, which can be used to enable one time writing of information to a bit. Hereby one register consists of multiple fuses, which are blown in case of a one being written to them. This process is not reversible and holds its information even after power cycling the chip. 88, 112

fifo A fifo is a type of storage, which send out the data first, which it received first. The counter part to a fifo would be a lifo, which would sent out the data, which it received last first. 99

FPGA A Field Programmable Gate Array is a collection of programmable logic blocks, which are defined via firmware. It is basically a hardware-programmable chip. 25, 26, 37, 38, 55

functionality test A functionality test is a wafer probing test, which tests a chip for a broken feature, influencing the final yield calculation. If the test value is outside a defined cut-value, the corresponding test is flagged as red and the chip will be discarded. 85, 115–117, 121–134, 155–162, 164, 180, 183

high-current bug ITkPixV1 featured a high current bug due to the use of a tot latch, which was not envisioned to be inside the submission of afore mentioned design. A Explains in more detail why this latch led to a high current. 18, 19, 23, 85

hitor bus The RD53B hitor bus connects the comparator output of a quarter of all pixels per core column on four lines to the precision Tot circuitry. Thereafter all core columns hit ors are joined on four lines and routed to a pad for external monitoring. The hitor bus pattern is displayed on the left of Figure A.2. 38, 40

HL-LHC High Luminosity Large Hadron Collider - An upgrade program which aims to increase the collision density of the LHC. v, 1–4, 6, 10, 18, 91, 92, 177, 185, 189

hybrid pixel detector This is a sandwich of two chips, where one side is used for charge collection and one side is used for charge integration and data transmission to the detector DAQ. The two chips are interconnected by bump bonding. This process allows different technologies to be used for the production of sensor (charge collection) and readout chip (charge processing), while offering more space for logic on readout chip, allowing very fast readout rates. 2, 6, 91, 190, 192

I2C I2C is a serial communication bus, to control a multitude of active components on e.g. a printed circuit board. 33, 71, 191

in-time threshold The in time threshold is a measured detection threshold considering only hits, which arrive within <25 ns. This defines the true charges, which can be detected within one bunch crossing ID. 31

injection capacitance The injection capacitance is an auxiliarry source of charge for testing and tuning the analog front end. See also Section 3.1. 21, 23, 81, 88, 145

IREF Iref is the internal reference current, generated by a core bandgap, and trimmed via four external trim pins [44]. 23, 24, 44, 45, 48–50, 52, 53, 60, 61, 74, 75, 81, 83, 87, 88, 91, 117, 118, 120, 154, 158, 177–179

isolated hit removal Isolated Hit removal is logic feature, designed to remove noise hits from the ITkPixV1.1 Data-stream. This feature is based on the assumption that true particle hits inside the detector form clusters. A particle traversing a sensor, usually induces charge in more than one pixel. Every isolated hit is therefore assumed to be electronic noise and removed. 18

ITk The inner tracker or ATLAS ITk is an upgrade of the ATLAS detector required by the HL-LHC program. ITk is the redesign of the ATLAS inner detector, that replaces the old TRT, STRIP, and PIXEL detectors with an all new PIXEL detector in the first 5 layers and STRIP detector in the following four layers. 6–8, 10, 14, 17, 18, 22, 23, 43, 52, 53, 60, 70, 74, 76, 87, 91, 92, 101, 111, 117, 121, 123, 124, 126, 131–134, 155–162, 164, 177, 183, 189, 190

ITk pre-production ITk pre-production is the phase of the ATLAS HL-LHC upgrade, before ITk production, where production processes are defined and qualified. 8, 79, 87, 111, 163

ITk production ITk production is the phase of the ATLAS HL-LHC upgrade, where actual components for the upgrade are produced for final ITk detector assembly. 8, 50, 77, 82, 89, 91, 92, 116, 160, 189

ITkPix Inner Tracker Pixel chip, is the general term for all in silicon chips developed by the RD53 collaboration concerning the ATLAS inner tracker upgrade replacing the old PIXEL detector chips in ATLAS. All chips developed under this name are manufactured in 65 nm CMOS technology with 400 x 384 pixels and 2 cm x 2 cm in size. 8, 15, 18, 19, 22, 43, 44, 48, 50, 54, 60, 68, 88, 91, 103, 177, 180, 183, 187, 189, 191, 193

ITkPixV1 Inner Tracker Pixel chip Version 1, the first full-scale prototype chip for the ATLAS ITk upgrade. This chip had an unintended feature, increasing the digital current consumption unbearably and implementing uncontrollable hit-loss. v, vi, 17, 18, 25, 27–30, 35, 37, 40, 44, 45, 48, 56, 69, 72, 93–95, 97, 99, 177, 178, 188, 189, 192

ITkPixV1.1 Inner Tracker Pixel chip version 1.1, is the fixed version for the bug observed in ITkPixV1, fixing high currents and hit loss, by sacrificing its charge resolution. In addition to that, it is indistinguishable from ITkPixV1. v, vi, 17–19, 21–23, 25–30, 32, 33, 40, 43, 45–51, 53–59, 61, 62, 64, 67, 71–78, 80–88, 91–93, 97, 99, 101–103, 105, 106, 111–114, 116–165, 178, 179, 183, 185, 187–189, 192, 193

ITkPixV2 Inner Tracker Pixel chip Version 2, is the final version of the ITkPix chip, which will be used in ITk production to build the final detector. 18, 55, 59, 69, 87, 89, 92, 97, 99

k-factor The scale factor-k of the shunt regulator. Figure 7.6(b) offers further information. 76, 77, 131–134

LDO Low dropout or LDO regulators are circuits, which can down regulate voltages with high efficiency. 23, 24, 48, 75, 88, 105, 112, 122, 125, 193

LEP Large Electron–Positron Collider - A positron electron collider with a center of mass energy of 209 GeV. This collider is the predecessor of LHC. 2

LHC Large Hadron Collider - A proton collider with a center of mass energy of 14 TeV located at CERN. v, 1–4, 6, 177, 185, 190

LHCb Large Hadron Collider beauty is one of the four main detectors at the LHC. It is optimized to study the slight differences between matter and antimatter by studying a type of particle called the "beauty quark", or "b quark". 2, 3, 177

linear analog front end The linear front end is the analog front end incorporated into the CMS readout chip CROC. 18

LSB LSB or least significant bit is a unit corresponding to one DAC or ADC bit. 52, 60, 61, 120, 123, 126

LVDS Low-voltage differential signaling or LVDS are differential transmission lines, which allow for low voltage and high speed transmission, apart from the usually standardized 3.3V GPIO outputs. 56

mask shifting Mask shifting is a process applied during scans involving a large amount of pixels. To ensure, that the chip bottom has sufficient time to process all data and make sure, that all pixel receive the same charge, only a portion of all pixels are enabled at the same time. This mask of enabled pixel is then shifted over the matrix, until all pixel are tested. 40

matrix core A matrix core or pixel core is a design entity of RD53B, consisting of 8x8 pixel. Each matrix core shares the same analog and digital layout, which is then stepped over large parts of the readout chip, constituting the pixel matrix. 19, 191

MDTs Monitored Drift Tubes. 5

MGT Multi-Gigabit Transceiver accepts parallel data and allows high-bandwidth data to be transmitted over serial lines. 26, 27

MIP A MIP is a minimum-ionizing particle, referring to the minimum charge, which it is ionizing while traversing matter. This minimum-ionizing property is mainly dependent on the mass of the particles and its kinetic energy. 15, 177

module Modules are the building blocks of ATLAS ITk. A module consists of multiple readout chips and a single (large) sensor. The interconnection of the chips is achieved as in hybrid pixel detectors. Module is the technical term for hybrid pixel detectors in ATLAS. 7, 49, 50, 52–54, 59, 60, 76, 114, 116, 120, 178, 194

multi clock capture cycle A multi clock capture cycle happens after shifting in a full scan chain pattern, then defining some external pins and applying one or multiple multi clock capture cycles, with disabled scan enable bit, which allows all defined flip flops to interact as they would in regular operation. Afterward the full scan chain is shifted out and compared to a simulated test vector. 101, 103–106

noise intensity The noise intensity of an analog front end is determined by the electronic noise inside and measured using a threshold scan. The resulting sigma of the S-curve, acuired by the threshold scan corresponds to the noise intensity of the given pixel. 31, 192

noise scan A noise scan is a scan, which only sends triggers to a chip, to evaluate, if there was a noise hit, generated by e.g. electronic noise [92]. 62

NTC An NTC or Negative Temperature Coefficient Thermistor is a resistor, which changes its resistance based on the environmental temperature. 47, 50, 51, 84, 148–150, 153

PEP8 PEP8 is a style standard for python, defining e.g. the amount of empty lines, after a new class, or the amount of empty spaces between mathematical operators and many more. 32

pixel A pixel is the smallest repeating entity on a readout chip, many pixels make up the pixel matrix. A pixel consists of the analog front end, as well as digital pixel logic. 7, 8, 19, 22, 29–31, 40, 43, 59, 61–65, 67, 70, 80, 91, 97, 114, 159, 160, 162, 179, 187, 188, 190–193

pixel core A pixel core, or matrix core, is the smallest unit of equally synthesized traces on a chip. It consists of 8x8 pixels. These cores are then copied over the whole chip, making up the pixel matrix. See also Section 3.1. 67, 108, 180, 190, 191

pixel matrix The pixel matrix of a readout chip is its largest and only active part. It consists of many pixels, which are responsible to digitize all charge received by e.g. a sensor. 17–19, 22, 23, 29, 40, 43, 59, 62, 63, 72, 91, 92, 161, 162, 177, 178, 190, 191

pixel quad A pixel quad is the compositor of a pixel core, consisting of 4x4 pixel. One pixel quad shares the same VDDA powering bus along its column. 19, 67, 188, 193

PLL A phase locked loop (PLL) generates an output clock or data stream with a fixed phase relation, based on an input signal. A simple PLL consists of a variable frequency oscillator chip, a phase detector and a feedback loop. 35, 36, 105, 112, 178

pre-emphasis Pre-emphasis is the oversteering of a fast signal, to compensate for the finite rise times of real transistors and compensate for potential distortions introduced on the way to the receiver. 57

precision Tot The precision Tot measures, just like ToT, the amount of charge injected in a single pixel. In comparison to regular ToT the time resolution is increased from 25 ns to 1.5 ns. Due to the larger circuit size, the ptot is located in the chip bottom. More detail can be found in the RD53B manual [44]. 23, 30, 68, 85, 94, 162, 188

probe card The Probe-card is a printed circuit board designed to be mounted with hundreds of tungsten needles to contact an ITkPix chip on a probe station. Its design is derived from the Single-Chip Card with all pins being exchanged with multiplexers or I2C to gpio converters. More detailed description can be found in Table 4.1. 32, 33, 71–75, 77–79, 81, 84, 85, 87, 88, 105, 111, 112, 120, 148–150, 153, 179, 183, 192

probe station The probe station is a high precision machine responsible for moving a wafer with the accuracy of a few µm to the probe card, ensuring precise alignment of all probe needles to all tested chips on a wafer. Figure 7.2(a) shows a view of parts of the probe station. 71–73, 179

RD53 Collaboration CERN Research and development group 53 will design and produce the next generation of readout chips for ATLAS and CMS pixel detector upgrades at the HL-LHC. Collaboarating institutes can be found in Europe, America, and Asia. 18, 28, 43, 44, 59, 120, 183, 185, 186

RD53A RD53A is the first large-scale prototype chip for ATLAS and CMS upgrades, to test features such as large-scale readout and multiple charge-integrating amplifier designs for particle detection. This chip is the predecessor to ITkPixV1. 18, 32, 35, 75, 76, 79, 87, 92, 99, 114, 132, 134, 185, 193

RD53B RD53B is the chip framework, on which ITkPixV1, ITkPixV1.1 and CROCV1 are based. All RD53B chips share similar digital logic, command encoding and data output format. v, 18, 22, 23, 25, 27, 32, 33, 35–40, 43–49, 53, 56, 57, 63, 70, 74, 79, 80, 83, 91, 99, 101–103, 113, 114, 177–180, 185, 186, 188, 190, 193, 194

readout chip This is the data processing part of a hybrid pixel detector that receives the charge from a sensor and converts it into a digital data stream to be processed by a DAQ. 2, 7, 8, 14, 15, 17–19, 22, 33, 35, 40, 80, 91, 93, 94, 185–188, 190–193

repository A repository is like a directory in a versioning system, such as gitlab or github, to store code and keep track of its change history. 32, 186

ring oscillator A ring oscillator is an electronic oscillator circuit with non-sinusoidal signals. It is based on the propagation time of an odd number of digital amplifiers connected together to form a ring. The simplest case is a ring circuit of three inverters. 88, 114, 163

RPCs Resistive Plate Chambers. 5

S-curve An S-curve is the measurement result of a threshold scan. An exemplary plot for a single pixel S-curve can be found in Figure 4.7. The Mean of the S-curve defines the detection threshold and the sigma of the S-curve defines the noise intensity. An S-curve is defined by Equation 4.1. 31, 64, 69, 70, 159, 178, 179, 187, 191–193

scan chain Scan chain is an industry standard testing methodology to quickly evaluate whether all flip-flops inside a chip are working as expected. 18, 23, 28, 44, 101–106, 180

sensor This is the charge collection part of a hybrid pixel detector, responsible for collecting the induced charge by a traversing, charged particle. It guides the charge, induced in a pixel, through electric fields and bump bonds to the analog front end of one pixel in the readout chip. 7, 13–15, 19, 21, 33, 59, 63–67, 70, 91, 109, 177, 185, 188, 189, 191–193

serial powering Serial powering refers to a powering circuit, where all consumers in an electric circuit are connected in series. When building a detector this has the advantage of reducing the amount of cable, necessary to power every e.g. readout chips in parallel. 76, 111

shunt LDO The shunt LDO mode employs the shunt regulator and LDO regulator in ITkPixV1.1, to generate VDDD and VDDA. 73, 105, 111, 155

shunt regulator A shunt regulator is a voltage regulator, which ensures a constant load on the input, while supplying a constant voltage at its output and shunting the excess current to ground. 23, 48, 59, 74, 76–79, 87, 88, 112, 127–134, 146–149, 179, 189, 193, 194

single isolat ITkPixV1.1 wafers come in two flavours, one with single isolation, where an additional deep n-well below each analog island of each pixel quad is missing. This deep n-well would usually shield the analog front end from noise coupled to the bulk, but could influence radiation hardness of ITkPixV1.1. 63–65, 70, 109

Single-Chip Card The Single Chip Card (SCC) is a printed circuit board designed to be mounted with one RD53B style chip for bench testing. It features only passive components and connectors for operating a readout chip, as well as biasing connectors for operating a sensor if mounted. More detailed description can be found in Table 4.1. 32, 33, 44–47, 50, 71, 102, 105, 178, 183, 185, 191, 194

supersymmetry Supersymmetry is a hypothetical particle symmetry, that transforms bosons (particles with integer spin) and fermions (particles with half-integer spin) into each other. In this context, particles that transform into each other under a supersymmetry transformation are called superpartners. 3

sync command The sync command is used to align the frames inside the command DAQ to RD53B command stream. It is the only non DC balanced command (meaning it has an unequal amount of ones and zeros in every 8 bit). 36, 63, 178

TDAC TDAC is short for local threshold voltage DAC, which is an offset voltage, which can be applied to the global threshold voltage on a per pixel basis. This way production inhomogeneities over the matrix can be trimmed out. 21, 30, 40

threshold scan A threshold scan generates a S-curve, to determine the threshold of one or multiple pixels. A detailed description can be found in Section 4.1.3. 30, 31, 43, 59, 60, 64, 84, 85, 87, 88, 178, 187, 191, 192

threshold voltage The threshold voltage is a way of trimming the charge detection threshold of an analog front end. See also Section 3.1. 21, 22, 30, 62, 84–86, 154, 179, 187, 193

ToT Time over threshold (ToT) is a measure for the amount of charge injected in a single analog front end pixel. See also Section 3.1. 21, 23, 30, 68, 69, 93–95, 179, 191

trigger A trigger signal is a command to the chip asking it to send the data of one or more hit data multibit latches to the DAQ. 22, 62, 97, 185, 191

TSMC TSMC or Taiwan Semiconductor Manufacturing Company, is the manufacturer of RD53A, ITkPix and CROC. 145

vcal high Vcal High is the upper voltage of the two injection voltages vcal high and vcal med. Both voltages can be operated in a small and high range mode, where only half, of the regular reference voltage is applied to the DAC. Due to rapid switching between the two voltages, charge is injected into the analog front end proportional to $vcalhigh - vcalmed$. For further information checkout the RD53 Manual [44]. 39, 59, 81–83, 137–140, 186, 187, 194

vcal med Vcal Med is the lower voltage of the two injection voltages vcal high and vcal med. Both voltages can be operated in a small and high range mode, where only half, the regular reference voltage is applied to the DAC. Due to rapid switching between the two voltages, charge is injected into the analog front end proportional to $vcalhigh - vcalmed$. For further information checkout the RD53 Manual [44]. 39, 59, 81, 82, 141–144, 186, 187, 194

VDDA VDDA is the analog supply voltage, responsible for supplying all transistors and analog components e.g. analog front end of RD53B chips with exactly 1.2 V. 24, 48, 68, 69, 75, 76, 80, 81, 105, 111, 124–126, 154, 179, 191, 193

VDDD VDDD is the digital supply voltage, responsible for supplying all transistors and digital components of RD53B chips with exactly 1.2 V. 24, 48, 58, 59, 68, 69, 75, 76, 102, 105, 111, 121–123, 154, 178, 179, 193

VOFS The shunt offset voltage (VOFS) defines the offset of the shunt regulator function. The homogeneity of this voltage is very important within a module to optimize power efficiency within a module. 23, 74, 77, 120

wafer probing Wafer probing is the process of testing micro chips on a wafer level, by establishing semi-permanent connection to its pads via highly accurate tungsten needles. 25, 33, 48, 50–52, 54, 61, 62, 71–73, 75–77, 79, 81, 83–85, 87–89, 92, 111–114, 132, 134, 179, 194

wafer probing routine Wafer probing routines are the measurement routines, which are run on each chip during wafer probing. All routines are described in Section 7.2. 111, 114–164, 180, 194

wafer probing test Wafer probing tests are measurement values, either directly measured, or derived from wafer probing routines. These tests, produce the values, which determine, whether a tested chip is green, yellow or red. 75, 85, 86, 114–165, 179–181, 183, 184, 186–188, 194

wire-bonding Wire-bonding is the process of establishing a permanent electrical connection between a printed circuit board and a chip. This procedure employs fine wires, which are friction welded to a pad on the chip and on the other side to a pad on the printed circuit board e.g. Single-Chip Card. 33, 111, 158

yield Yield is the total number of chips in percent, which passed all wafer probing tests. 71, 85, 87, 92, 116–165