Characterization and Operation of Final DEPFET Pixel Detector Modules for the Belle II Experiment

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Contents

Introduction

Once upon a time there was a happy little High Energy Physics (HEP) experiment called Belle. The experiment took data from 1999 to 2010 [1]. It was located at the Interaction Point (IP) of the KEKB accelerator in Tsukuba, Japan. KEKB provided asymmetric-energy collisions of electrons (e^-) and positrons (e^+) with a Center-of-Mass (CM) energy of $E_{CM} = 10.58\,\text{GeV}$. This is the mass of the $\Upsilon(4S)$ resonance, which almost always decays into $B\overline{B}$ meson pairs. B mesons are short-lived particles which decay with an average lifetime $\tau = 1.5$ to $1.6\,\text{ps}$[2]. The difference in energy of the primary particles translates to a boost given to the B-mesons in the laboratory frame. This increases their momenta resulting in flight paths of $O(100)\mu\text{m}$ before decay, from which the lifetimes can be calculated. By making exact lifetime measurements a violation of the Charge-Parity (CP) symmetry was experimentally observed. Subsequently, the Nobel price for physics was awarded to Cabbibo, Kobayashi, and Maskawa in 2008 for their theoretical predictions of the mechanism of CP violation [3].

After finishing data taking with Belle, the accelerator was upgraded to provide an increased instantaneous luminosity [4, 5]. At the same time, the Belle detector was upgraded to become the Belle II experiment [6, 7]. The new detector was designed to cope with the new environment providing the same or better accuracy of the measured particle lifetimes and other parameters. The goal is to collect a data set 50 times larger than that of Belle. This will make possible new and improved measurements of parameters of the Standard Model of particle physics (SM), such as Cabibbo–Kobayashi–Maskawa (CKM) matrix elements and quark masses, as well as studies of rare decays and searches for new phenomena in precision measurements.

Important modifications are the changed beam energies, the increased collision rate, increased beam currents and changed geometry. The CM energy remains unchanged, but the collisions are less asymmetric. Therefore, the flight paths of decaying particles are shorter and a better spacial resolution is required. Higher collision rates and increased beam backgrounds require a finely segmented tracking detector to keep the occupancy at acceptable levels.

The Belle II VerteX Detector (VXD) was designed to meet these specifications. For the two layers closest to the IP a thin silicon pixel detector was developed. It is based on DEpleted P-channel Field Effect Transistors (DEPFETs). This technology is used for the first time in a HEP experiment. It makes thin, self-supported modules possible, and thus reduces the amount of material present within the detector's tracking acceptance.

This thesis presents results from the characterization and operation of final PiXel Detector (PXD) modules. The focus is put on understanding the currents flowing through the silicon bulk of the detector as well as through the Field Effect Transistors (FETs) on top of the sensors. Furthermore, the behavior of the modules during long-term operation in the Belle II detector environment is studied during the first stage of common operation.

In Chapter 1 the Belle II experiment is described. The Super-KEKB accelerator, the Belle II detector, its subsystems and physics goals are briefly discussed.

Chapter 2 presents a brief introduction to the working principles of silicon trackers.
Chapter 3 gives an overview of the Belle II PXD. The design parameters, components and working principle of the detector are explained here.
DEPFET bulk current-voltage characteristics and lessons learned from them are presented in Chapter 4
A detailed analysis of the PXD sensor FET dark currents is presented in Chapter 5.
The accelerator is commissioned in three phases:

- Phase 1: no beam collisions and no Belle II detector in the Interaction Region (IR)
- Phase 2: Belle II is rolled in, the VXD volume is instrumented with dedicated beam monitoring detectors including a number of PXD and Silicon Vertex Detector (SVD) modules. First beam collisions are recorded.
- Phase 3: the full detector, including VXD is taking collision data together

The setup and performance of the PXD during Phase 2 is described in Chapter 6.
Finally, a conclusion and outlook to the future of the PXD is given in 7.

CHAPTER 1

The Belle II Experiment

The Belle II experiment is a large multipurpose detector recording asymmetric-energy electron-positron collisions.

The electron is the particle constituting the atomic shell and together with atomic nuclei makes up all matter, therefore governing chemistry, biology and life as we know it. According to the Standard Model of particle physics (SM) [8] it is a fundamental particle, i.e. it is not composed of other, smaller particles. It carries a negative electric charge of one. The positron is the antiparticle of the electron. It has the exact same properties but a positive electric charge of one. Electron and positron are both stable particles as they are the lightest charged particles of the SM. In matter environments though, as here on earth, positrons usually annihilate very quickly with electrons.

The Super-KEKB accelerator is made up of a linear accelerator and a ring section with two beam pipes for the electron and and positron beams. The High Energy Ring (HER) stores the electron beam. Each electron has an energy of 7 GeV. The Low Energy Beam (LER) stores the positron beam with 4 GeV per particle. The beams consist of 2500 bunches of up to 9×10^{10} particles each. They are brought to collision in the Interaction Point (IP) in an almost head-on fashion. The Center-of-Mass (CM) energy of two colliding particles corresponds exactly to the mass of the $\Upsilon(4S)$ resonance of $m_{\Upsilon(4S)} = 10.58\,\mathrm{GeV}/c^2$[2]. The $\Upsilon(4S)$ is a meson, consisting of a bottom (b) and an antibottom ($\overline{b}$) quark.

Quarks are another type of fundamental particles of the SM. There are six different quarks (q) and their respective antiparticles ($\overline{q}$): up (u), down (d), strange (s), charm (c), bottom (b), and top (t). They differ in spin and mass, t being the heaviest and u the lightest. They cannot exist as free particles and are always bound in hadrons by the strong force, typically $q\overline{q}$ (meson) or 3-quark (baryon) states.

If the electron and positron annihilate in the collision their entire energy is available to form the $\Upsilon(4S)$ in the CM frame, i.e. a frame of reference comoving with the center of mass. Due to the asymmetry in electron and positron energies the CM and therefore the produced $\Upsilon(4S)$ has a boost of $\beta\gamma = 0.28$ in the laboratory frame, i.e. it moves with a velocity $v \sim 0.27c$ relative to the detector, c being the speed of light. The $\Upsilon(4S)$ immediately decays in $> 96\,\%$ of the cases into $B\overline{B}$ meson pairs. A picture of a typical $\Upsilon(4S)$ decay to $B\overline{B}$ is shown in Fig. 1.1. B mesons are composed of a $\overline{b}$ quark and either an u, d, s or c quark. $\overline{B}$ mesons are their respective antiparticles. Because of the copious production of B mesons Super-KEKB is called a B factory, following in the footsteps of other B factories like CESR, PEP-II and KEKB. Even though most collisions do not produce the sought after B mesons but other particles, constituting background events, the $B\overline{B}$ events are of special interest. Studying their decays

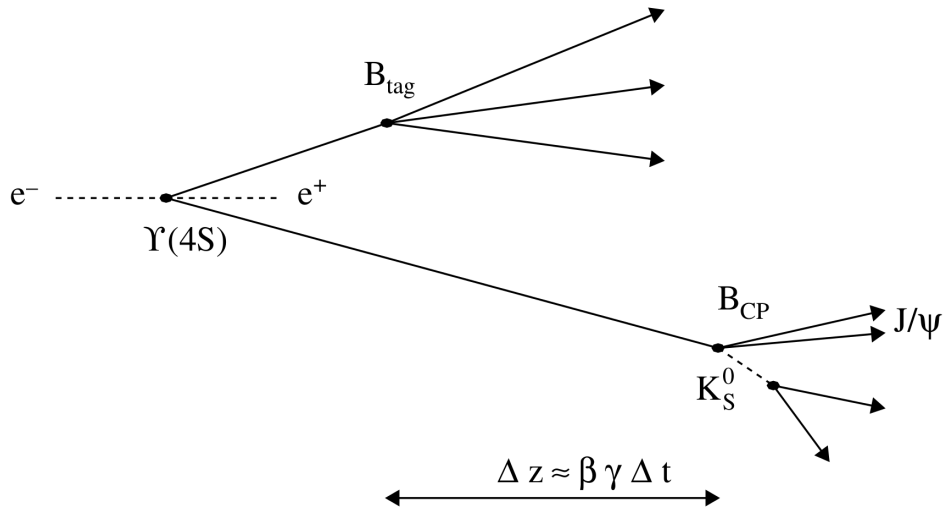


Figure 1.1: Schematic of a $\Upsilon(4S) \rightarrow B\overline{B}$ decay created in an electron-positron collision in the laboratory frame [1]. The electron comes from the left with higher energy than the positron from the right. They annihilate forming an $\Upsilon(4S)$ which decays into two B mesons. The boost due to the energy asymmetry results in both mesons moving to the right. The vertices labeled B represent their decay vertices into other particles. The distance along the beam axis Δz between these vertices can be used to calculate their lifetime difference. The formula assume $c = 1$.

allows measuring time dependent charge conjugation parity (CP) symmetry violation, i.e. differences or asymmetries in the physical laws of matter and antimatter straying from the assumption of a CP symmetry. Also, new physics beyond the energy scale of the collision can be probed, since they enter in quantum loop corrections of the decay processes.

B mesons themselves have a lifetime of $\sim 1.5\,\mathrm{ps}$ and at Belle II decay within $O(100)\mu\mathrm{m}$ of their production vertex, still within the beam pipe. Measuring the decay of $\overline{B}$ mesons therefore means observing their respective longer-lived decay products. Since the events of interest occur only in a small fraction of collisions a large set of samples has to be collected for precise measurements of their probabilities. Luminosity measures the interaction rate $\dot{N}$ per reaction cross section σ

$$L = \frac{\dot{N}}{\sigma} \quad . \tag{1.1}$$

SuperKEKB reached a luminosity of $4.71 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ [9] in June 2022, setting the current world record, and is planned to ramp up further in two steps up to $2.4 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ [10].

High luminosities are challenging for detectors. They have to deal with high particle rates and event frequencies. The Belle II detector aims to enable reconstructing individual $B\overline{B}$ events as completely as possible. This entails tracking the paths of secondary decay particles, identifying their type, momentum and energy and reconstructing the decay vertices of the B mesons. Belle II consists of several subdetectors layered around the IP with approximate rotational symmetry taking over these different tasks. Detailed descriptions can be found in [6, 7]. Figures 1.2 and 1.3 show the layout of the Belle II detector.

The innermost detector is dedicated to the tracking of charged particles. It comprises the VerteX Detector (VXD), consisting of two layers of silicon pixel detector (PiXel Detector (PXD)) and four layers of double-sided strip detector (Silicon Vertex Detector (SVD)). These detectors measure the

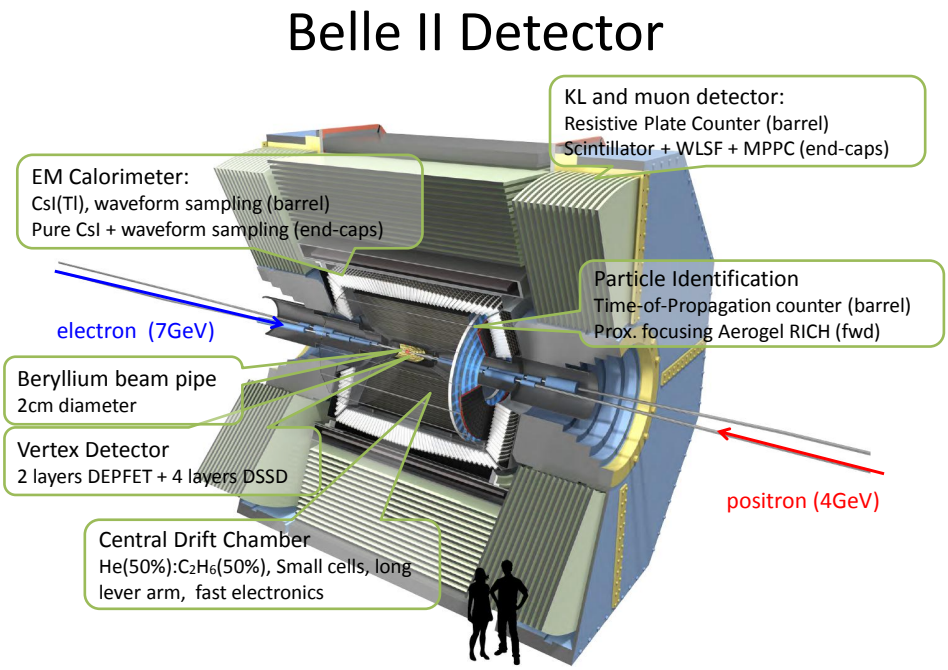


Figure 1.2: 3D illustration of the Belle II detector. © Belle II / KEK [11].

intersection points of charged particles leaving the interaction region. Surrounding the VXD is the Central Drift Chamber (CDC), which consists of a gas filled volume with wires for tracking traversing charged particles.

Outside the trackers are the Time Of Propagation detector (TOP) and the Aerogel Ring Imaging Cherenkov counter (ARICH) detectors for Particle IDentification (PID). They use Cherenkov radiation for identifying the type of charged particles.

Surrounding the tracker and PID is the Electromagnetic CaLorimeter (ECL). It consists of an array of thallium-doped cesium iodide CsI(Tl) crystals arranged in a barrel layer around the inner detectors and two end caps at its ends. Its task is detecting photons (γ) and identifying electrons.

The outermost subdetector encompassing the entire rest of the detector is the K_L^0-Muon detector (KLM). It detects and differentiates the only charged particles leaving the ECL, which are K_L^0 mesons and muons.

A superconducting solenoid is located outside the ECL providing an axial magnetic field of 1.5 T inside all inner subdetectors. The field facilitates measuring particle charges and momenta by means of their track curvatures.

For studies involving the lifetime of B mesons the length of their flight paths has to be determined accurately. This requires resolving the decay vertices with high precision. The vertex resolution is dominated by the sensor distance from the IP and the spacial resolution of the innermost tracking detector layers as well as the amount of material leading to Coulomb scattering of the traversing particles. For this reason the PXD was designed to be located on top of the beam pipe and have ultra-thin silicon sensors. The details of this detector will be presented in Chapter 3.

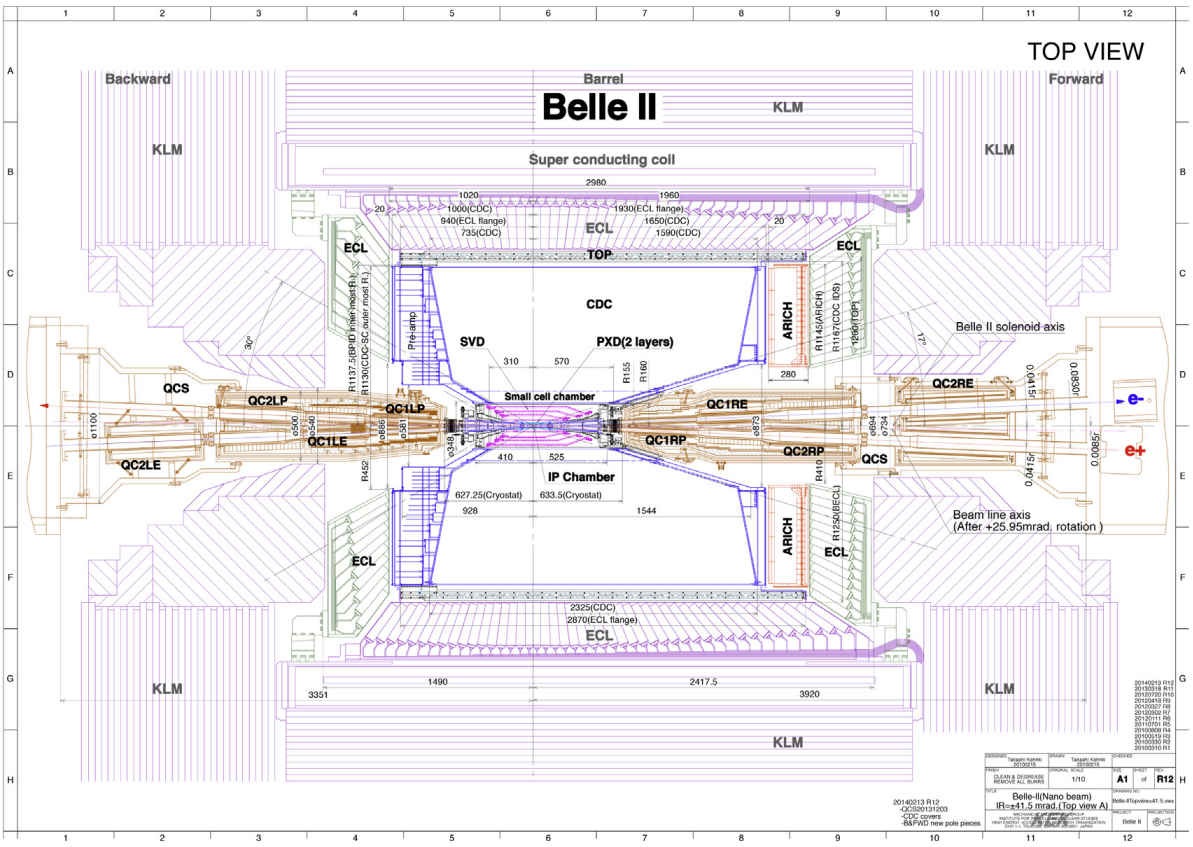


Figure 1.3: Belle II top view [7].

CHAPTER 2

Silicon tracking detectors

Silicon tracking detectors are used in High Energy Physics (HEP) experiments to provide trajectories of charged particles. High track densities, fast repetition rates and large integrated absorbed doses of radiation near the IP of collision experiments make these environments especially challenging. Silicon detectors can be finely segmented, read out fast with low dead times and manufactured to be radiation-tolerant, making them suitable for these conditions.

The sensor volume is made from silicon. Particles passing through the material can lose part or all of their energy and transfer it to the silicon or secondary particles. Energy deposited in silicon by ionization, i.e. interactions with the electron shell, can then be detected.

The main interaction mechanisms for charge generation in silicon are briefly laid out in the first part of this chapter. The second part describes the working principle of charge detection in silicon.

2.1 Ionizing energy loss of charged particles

Charged particles scatter with electrons of the atomic shell. They typically undergo several interactions when traversing a medium. The number of interactions and the amount of energy transferred in each of them are different every time and follow probability distributions. The expected average energy loss per length of traversed matter is given by the Bethe-Bloch equation [12]:

$$-\frac{dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\left(\frac{2m_e c^2\beta^2\gamma^2 T_{\max}}{I^2}\right) - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right] \tag{2.1}$$

The parameters of the Bethe-Bloch equation are defined in Table 2.1

Most of the individual energy transfers are small, but occasionally large transfers occur leading to a tail in the probability distribution. Therefore, the energy loss distribution is asymmetric. It can be approximated by a Landau function. Especially for thin absorbers also the Landau distribution does not satisfactorily describe the energy loss and instead *straggling* functions have to be obtained from simulations. Figure 2.1 shows an example for straggling functions of 500 MeV pions in silicon of different thicknesses.

Variable	Description
$-\frac{dE}{dx}$	Stopping power (energy loss per unit distance)
K	A constant depending on the units
z	Charge of the incident particle
Z	Atomic number of the target material
A	Atomic mass of the target material
β	Velocity of the incident particle relative to the speed of light
γ	Lorentz factor of the incident particle
$T_{\max}$	Maximum kinetic energy transferable from the incident particle to an electron
I	Mean excitation energy of the target material
δ	Density correction term
m_e	Electron mass
c	Speed of light in vacuum

Table 2.1: Description of the parameters of the Bethe-Bloch equation Eq. (2.1)

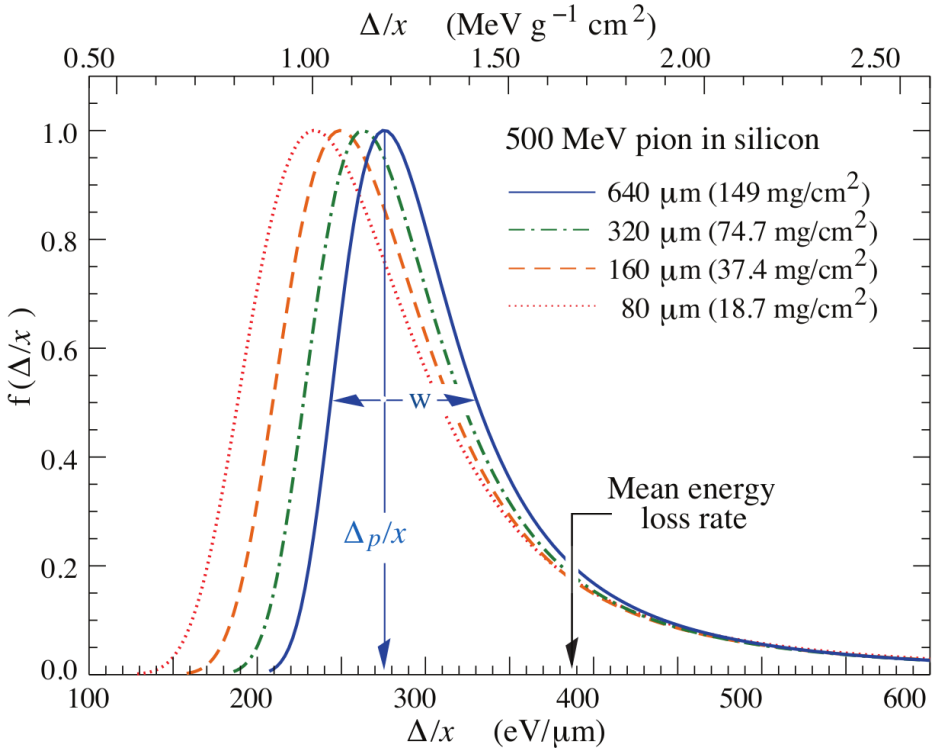


Figure 2.1: Straggling functions in silicon for 500 MeV pions, normalized to unity at the most probable value Δ_p/x. The width w is the full width at half maximum. Taken from [12].

2.2 Photon interactions with matter

Photon interactions depend on the photon energy and absorber material. Figure 2.2 shows the mass attenuation of photons in silicon. For photons below 100 keV the photoeffect is dominant. The photon transfers its entire energy to one electron, which in turn dissipates its energy in its local surroundings by e.g. ionization. Photons in this range are often used for calibration of sensors since the deposited energy is equal to the initial energy of the photon and therefore exactly known. Radioactive sources like ^{55}Fe and ^{109}Cd with well-known emission energies in the corresponding range are available for laboratory measurements. The interaction likelihood drops exponentially with energy. Thin silicon sensors can only efficiently detect photons in the low energy range.

For photons of higher energies Compton scattering starts dominating the cross section. In scattering interactions only part of the photon energy is transferred to an electron.

Beyond the electron-positron production threshold of ~ 1 MeV pair creation is possible and becomes the dominant process for energies higher than ~ 10 MeV. It can only occur in the vicinity of a nucleus taking part of the momentum.

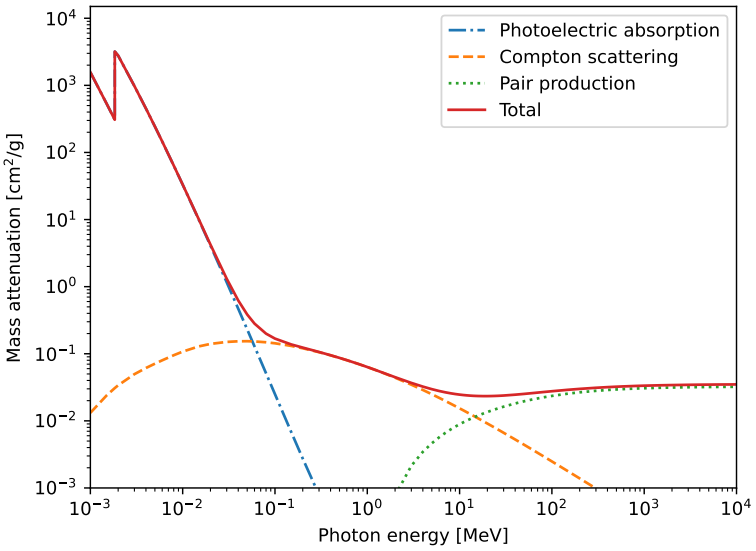


Figure 2.2: Photon mass attenuation in silicon. [13]

2.3 Silicon sensors

Silicon is an indirect semiconductor [14]. In the band model the electron states in the material form continuous energy bands, see Fig. 2.3. At low temperatures silicon becomes an insulator. The valence band is completely filled and the conduction band is empty. Consequently, all reachable states are occupied and electrons cannot travel across the lattice, i.e. no current is conducted. When energy is added to the system, electrons can be elevated into the conduction band. They are then called quasi-free electrons as they are not bound to an atomic nucleus anymore and can move freely through the material, i.e. constitute an electric current. Each electron leaving the valence band leaves behind an unoccupied state, called a hole. These can be treated as quasi-particles with positive charge of one and constitute an electric current with opposite sign.

The band gap of silicon is 1.12 eV. The energy extrema of the conduction and the valence bands have different momenta. This makes silicon an indirect semiconductor. The average energy required for lifting one electron across the band gap is 3.65 eV at 300 K [15]. Roughly two thirds of the energy is kinetic and eventually converted into lattice vibrations (phonons).

The energy deposited in the sensor material by traversing particles generates free electron-hole pairs. If an electric field is applied across the sensor the electrons and the holes drift in opposite directions and can be collected. By depleting the silicon of free charge carriers as described in the following section, the dark currents in the silicon are small while the signals from traversing particles can be detected.

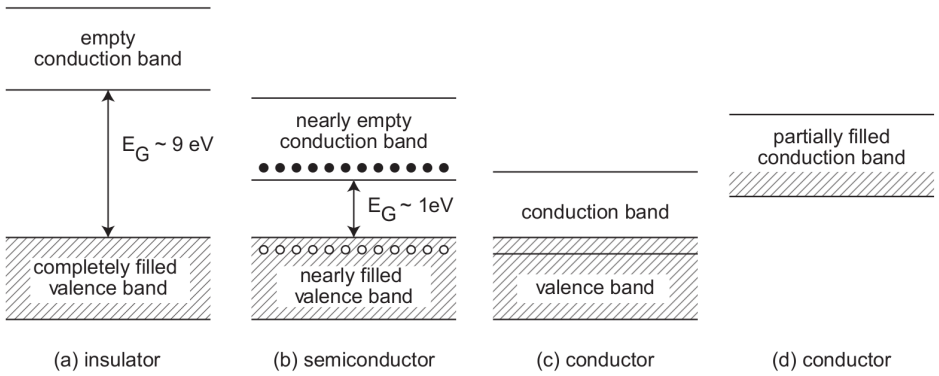


Figure 2.3: Schematic energy-band structure of insulators (a), semiconductors (b) and conductors (c,d). E_G is the width of the energy band gap. Figure from [15]

2.4 Silicon doping and diodes

In a silicon crystal, each Si atom has four valence electrons and is bound to four neighbor atoms. Pure silicon is called intrinsic. The material can be intentionally doped with atoms with different numbers of valence electrons. These impurities introduce free electrons or holes increasing the conductivity of the silicon. Depending on the type of dopant and the resulting majority charge carrier the resulting silicon is called n-type (negative electrons) or p-type (positive holes). It is important to note that either type of doped silicon is electrically neutral.

A diode is formed by combining n-type and p-type silicon. The interface of the n- and p-type region is called pn-junction. Figure 2.4 shows a schematic of a pn-junction and its space charge, electric field and potential in one dimension. At the junction the free majority carriers diffuse into the neighboring regions and recombine with the opposite type. This creates a space charge region causing an electric field counteracting the diffusion of further charge carriers until an equilibrium is reached. Since the space charge region is depleted of free charge carriers it is also called depletion region. The resulting potential difference is called built-in voltage V_{bi}.

The ideal current-voltage characteristic for a diode is shown in Fig. 2.5. It behaves according to the Shockley equation [17]:

$$I = I_{\text{SAT}} \left(e^{eV/kT} - 1 \right) \quad . \tag{2.2}$$

I_{SAT} is the saturation current, V the diode voltage, e the elementary charge, k the Boltzmann constant and T the temperature in Kelvin. If a positive voltage is applied to the p-type and a negative to the n-type it counteracts the built-in voltage at the junction. After surpassing the threshold voltage an exponentially increasing current flows. This is called forward bias/direction. If biased in the opposite direction, the

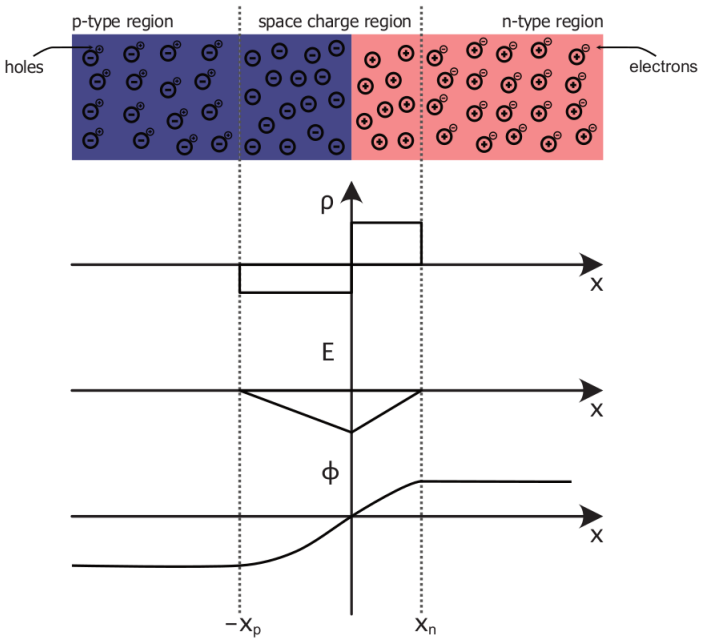


Figure 2.4: Schematic of a pn-junction and its space charge ρ, electric field E, and potential Φ in one dimension, from [16].

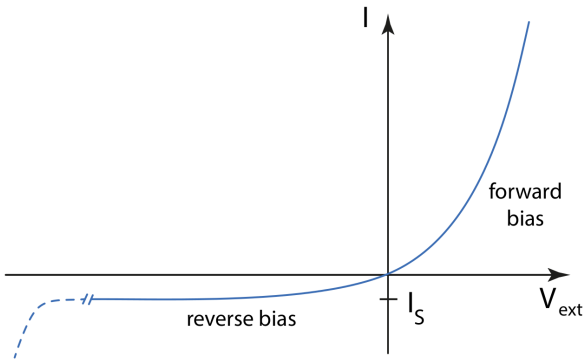


Figure 2.5: Ideal pn-diode characteristic according to Eq. (2.2) from [15].

external voltage increases the electric field at the pn-junction extending the depletion region. This regime is called reverse bias. Because of the depleted pn-junction no charges can drift across. Only small currents can flow caused by charge generation within the depletion zone, e.g. thermal generation.

2.5 Biasing and read-out

For biasing and direct read-out of the signal, metal contacts are applied on the surface of the silicon bulk. Often these are aluminum structures. To create an ohmic contact, the silicon material in contact with the metal needs to be highly doped. Lowly doped silicon forms Shottky diodes at metal junctions.

Read-out can also be facilitated by capacitive coupling. In this case the read-out nodes are not ohmically connected but electrically insulated from the sensor.

The direct and capacitive read-out of sensor currents depends on the weighting field, i.e. the sensor geometry, and the amount and speed of charges according to the Shokley-Ramo theorem [18, 19]. The current seen by the read-out electronics is induced by the moving charges in the sensor during their collection.

Another way of biasing implants is Punch-Through (PT) biasing. When the depletion zones of neighboring pn-junctions merge into each other conduction occurs from thermionic emission of charge carriers from the biasing implant. Figure 2.6 shows PT biasing in a strip sensor. This is used in guard ring structures around diode implants to shape smooth potential drop-offs and prevent high spikes in electric fields which cause avalanche breakdown. This technique can also save space for biasing structured implants or collection implants that are read out capacitively and therefore do not have resistive connections to their read-out electrodes.

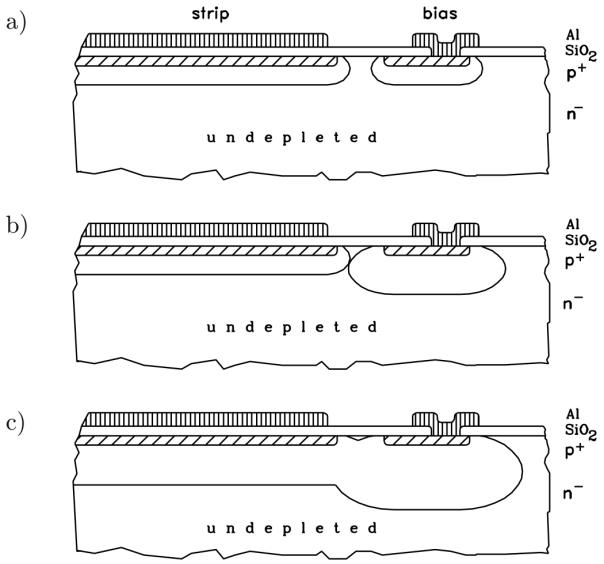


Figure 2.6: Cross section of a PT biasing structure from [20].

2.6 Structured silicon sensors

To gain spatial information from silicon sensors, diodes of large surface areas can be segmented by micro-structuring their implantations. A widely used approach is structuring the anode or cathode of a planar pn-diode and attaching each segment to an individual read-out channel. Silicon strip sensors are a common example for these types of sensors. For high particle flows segmentation into even finer structures becomes necessary to retain unique two-dimensional resolution. Sensors divided into small quadratic or low aspect ratio rectangle fields are called pixel sensors. As opposed to strip sensors the read-out connections for pixel detectors cannot be made at the side but have to reach every pixel on the sensor surface individually. Hybrid pixel detectors, as currently employed in many HEP experiments, such as the multi-purpose detector experiment ATLAS at the LHC at CERN (ATLAS) [21], electrically connect read-out circuits by stacking them vertically onto the sensor. This provides the fastest possible read-out of the signal. LHC experiments routinely reach 25 ns timing resolution. Monolithic pixel detectors integrate the read-out circuits for each pixel and the sensor into a single silicon die [22]. Another option is sharing read-out channels among pixels. Charge Coupled Devices (CCDs) do this by transporting charges between pixels. This approach generally comes at the cost of a lower speed, since pixels have to be read sequentially. But it reduces the power consumption since fewer electronics are needed. This can be a decisive factor since power supply and cooling capacities are usually limited in the spatially restricted environments of particle detectors.

CHAPTER 3

The Belle II Pixel Detector

The PXD is based on all-silicon modules with integrated DEpleted P-channel Field Effect Transistor (DEPFET) sensors [23]. Figure 3.1 shows the layout of the PXD. 40 modules are arranged in two barrel layers around the IP covering the full angle of 2π around the beam pipe and between 17 to 150° polar angle.

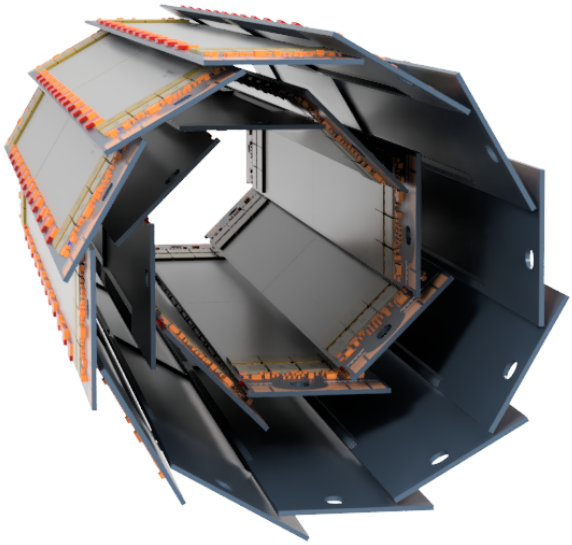


Figure 3.1: Computer Aided Design (CAD) drawing of the PXD. From [16], provided from technical drawings by David Kittlinger.

3.1 The PXD module

3.1.1 Layout

The PXD module is formed of a 75 µm thin silicon sensor layer with front- and back-side processing bonded to a stabilizing silicon handle layer of 450 µm or 375 µm thickness providing rigidity. The dimensions of the module are $(15.4 \times 68.0(85.0))$ mm^2 for inner (outer) modules. A picture of a PXD module is shown in Fig. 3.2.

The module is divided into three functional areas. The largest part is the active sensor area containing the DEPFET pixel matrix. It is $(12.5 \times 44.8(61.4))$mm^2. A balcony along the sensor holds the six switcher Application Specific Integrated Circuits (ASICs) [24] in charge of steering the matrix read-out and clearing voltages. The End Of Stave (EOS) region contains four pairs of Drain Current Digitizer (DCD) [24] and Data Handling Processor (DHP) ASICs [25, 26]. The DCDs sample and digitize the output signals of the matrix. The DHPs process the digital signal data, coordinate DCD and switcher operation and handle the communication to the backend read-out system (Data Handling Hub (DHH))

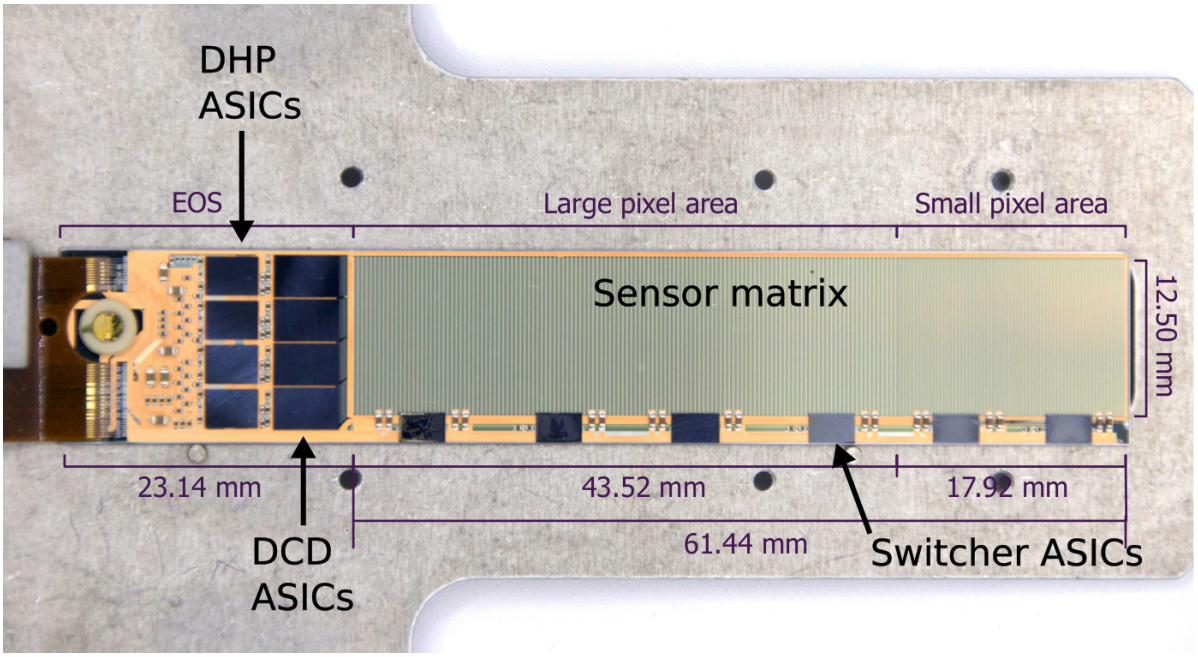


Figure 3.2: Top view of an Outer Backward (OB) module in the Bonn laboratory [16].

module	pixel size [µm^2]	
	rows 0-511	rows 512-767
IF/IB	50×60	50×55
OF/OB	50×85	50×70

Table 3.1: Pixel sizes of different modules and sensor regions.

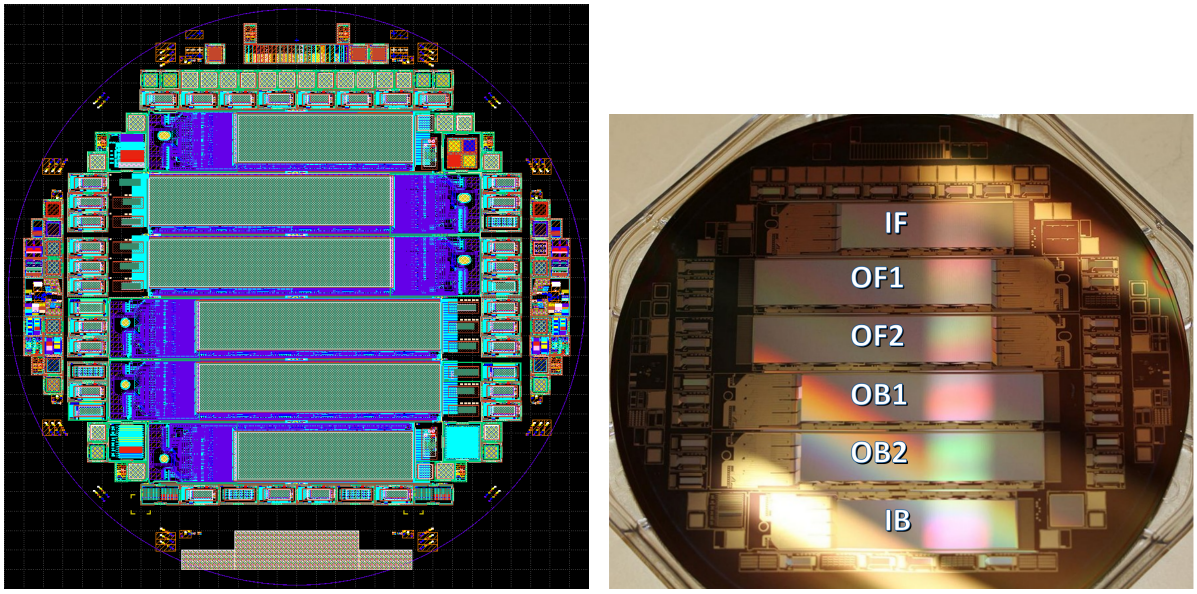
[27, 28].

The different lengths of inner and outer layer modules are due to the larger length of the acceptance region along the beam direction at a larger radius. Four different module designs are necessary. Their nomenclature describes their position: Inner Backward (IB), Inner Forward (IF), OB, Outer Forward (OF). To keep the functional designs as similar as possible, the number of pixels is the same on all modules, i.e. 768×250. Only the lengths of the pixels varies along the sensor and depending on the module type. Close to the IP, the pixels are shorter as the particle incidence angle is closer to perpendicular. All pixel sizes are given in Table 3.1.

3.1.2 Production

The modules are produced at the semiconductor laboratory of the Max-Planck Society (HLL). The base for manufacturing silicon structures like this are thin round slabs of silicon, called wafers. Their size limits the number and size of devices, which can be built by processing them. Due to the relatively large dimensions of the PXD modules, they make use of almost the entire available 6-inch diameter wafer area. Each wafer yields two inner and four outer layer modules. The layout is shown in Fig. 3.3(a).

Individual modules are referred to according to their wafer number, type, and position on the wafer as



(a) PXD9 wafer layout [29].

(b) Photograph of a PXD9 wafer with sensor locations marked.

Figure 3.3: The HLL PXD9 DEPFET wafers.

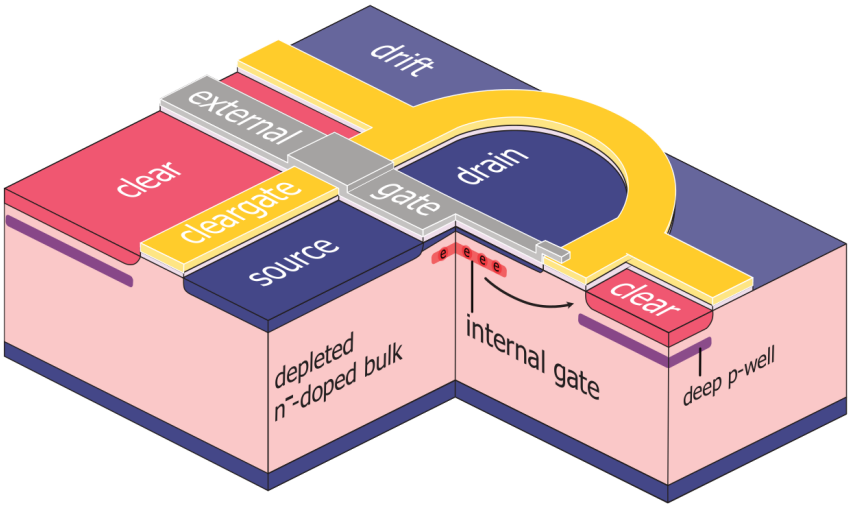


Figure 3.4: Schematic drawing of a PXD DEPFET pixel from [16].

Wxx_yy(z). xx specifies the wafer number and yy(z) specify the module type and position on the wafer, with yy(y) one of IF/IB/OBz/OFz and z either 1 or 2, see Fig. 3.3(b).

3.1.3 DEPFET sensor

The DEPFET sensor is based on a fully depleted n-type silicon bulk and segmented into a pixel matrix. Figure 3.4 shows a schematic drawing of a DEPFET pixel. Generated electrons drift to the internal gate

region of a pixel where they are stored while holes drift to the back side. The stored charge is read out by a Field Effect Transistor (FET) on top of the pixel. The internal gate is located less than one µm below the FET channel [30]. The charge in the internal gate influences the holes in the channel and therefore increases the source-drain current when the FET is switched on. Assuming the FET is operated in saturation, a current gain per charge of

$$g_q = \frac{\partial I_\mathrm{D}}{\partial Q_\mathrm{sig}} = \frac{500\,\mathrm{pA}}{e^-} \tag{3.1}$$

is expected, where I_D is the source-drain current of the FET and Q_sig the signal charge in the internal gate. This is referred to as internal amplification g_q. It is closely related to the transconductance of the FET

$$g_m = \frac{\partial I_\mathrm{D}}{\partial V_\mathrm{G,eff}} = \frac{W}{L}\mu_p C_\mathrm{ox} V_\mathrm{D} \quad , \tag{3.2}$$

where W is the gate width, L the gate length, μ_p the hole mobility, C_ox the gate-oxide capacitance and V_D the drain voltage. A charge present in the internal gate will induce a fraction f (close to one) of mirror charge in the channel. Therefore, its effect is equivalent to a change of the external gate voltage by the amount of $\Delta V_\mathrm{G} = \mathrm{f}\, Q_\mathrm{sig}/C_\mathrm{G}$ with $C_\mathrm{G} = WLC_\mathrm{ox}$. It follows that

$$g_q = \frac{\partial I_\mathrm{D}}{\partial Q_\mathrm{sig}} = \frac{\partial I_\mathrm{D}}{\partial V_\mathrm{G,eff}} \cdot \frac{\partial V_\mathrm{G,}}{\partial Q_\mathrm{sig}} = \frac{\partial I_\mathrm{D}}{\partial V_\mathrm{G,eff}} \cdot \frac{f}{C_\mathrm{G}} = g_m \cdot \frac{f}{C_\mathrm{G}} \quad . \tag{3.3}$$

The internal gate is the maximum of the electric potential. The static potential maximum is achieved by applying a positive voltage of typically 10 V to the n-bulk, a negative depletion voltage of typically ~ -30 V to the p-doped back side, and keeping the front side, i.e. the FET source, at ~ 0 V. This configuration also largely depletes the sensor volume from free charge carriers. Additionally, there is a deep n-implant defining the internal gate. This causes the internal gate voltage to be the most positive potential. Lateral drift is ensured by a drift p-implant in the pixel periphery which is held at a low negative potential of typically ~ -5 V.

For clearing the accumulated charges from the internal gate there is an n-implant, called clear, next to the p-FET. It is held at a positive potential. During charge collection the clear potential is lower than the internal gate. A potential barrier is formed between them by the clear-gate conductor on top, which is held at ~ 0 V. For clearing, a high positive voltage, typically 19 V, is applied to the clear contact. The barrier between internal gate and clear is lowered by bringing the clear-gate to a more positive voltage as well. In this situation the electrons can travel from the internal gate to clear and are removed from the sensor volume. This process dynamically depletes the sensor from electrons. The bulk voltage is applied at the module edges and therefore is only relevant at the sensor edges. Free holes are removed through the front- and back-side p-implants.

The external gate and the clear gate conductors are implemented as poly-silicon traces. The clear gate is made up of long poly-silicon lines running along the pixel rows. It is connected to a constant voltage supply by large resistors in the periphery. Switching of its voltage for clearing is implemented through capacitive coupling to clear.

Gate conductors, clear and drift lines are implemented by aluminum lines running along the pixel rows. Source implants are supplied by aluminum lines going vertically and horizontally along the matrix. The drain implants are connected to aluminum drain lines along the pixel columns.

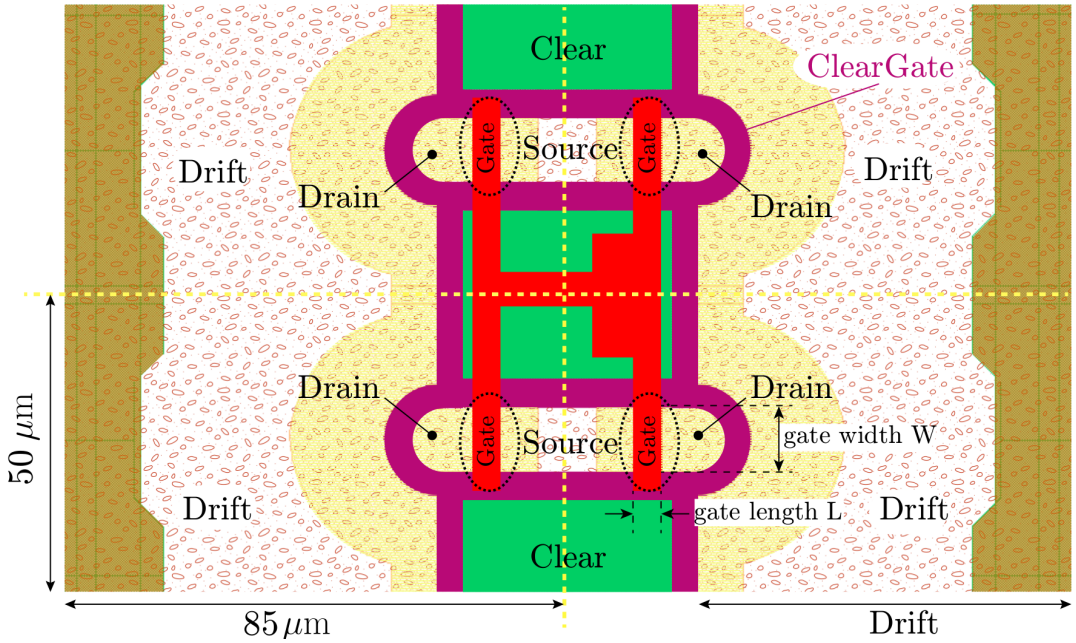


Figure 3.5: Layout of the PXD9 DEPFET pixel double row. Two pixels share a common Source implant and a common Clear implant. Color code: purple: polysilicon 1 (ClearGate), red: polysilicon 2 (external Gate), green: n+ implant (Clear implant), light yellow: n implant (also internal Gate), red pattern: p implant (drift), orange: additional drift implants [31].

As shown in Fig. 3.5 the pixels are structured in a double-row layout. Two pixels share a common source region. Four pixels share a common clear region. In the picture the rows run from top to bottom and the columns from left to right. The design of the central double-pixel row structure is identical for all pixels sizes. Only the size of the drift region varies.

3.1.4 Sensor operation

During signal integration the FETs are switched off and no power is dissipated in the pixels. A positive gate voltage of typically 5 V is applied. Integration time of the sensor is exactly twice the bunch revolution time of SuperKEKB, ca. 20 µs. The read-out is implemented in rolling shutter fashion. Groups of pixels are switched on consecutively. Gates and clear contacts of four rows of pixels are connected to a common gate and a common clear line, respectively. Each gate and clear line are steered by a dedicated output channel of a switcher ASIC. The read-out speed of the DEPFET is limited by settling times of the drain current after switching of the gate and clear voltages. Therefore, simultaneous read-out of four rows reduces the overall shutter time fourfold. Since no drain currents are present in the off state, consecutive pixel groups can share drain lines. Every fourth pixel of a column is connected to the same drain line.

Due to the fourfold row scheme the 250×768 pixel matrix is controlled by 192 gate and clear lines. The current settling, read-out and successive clearing of a pixel takes about 100 ns [32]. The currents are read out via 1000 common drain lines.

Each switcher controls 32 gate (clear) lines, i.e. a sixth of the sensor rows. Each DCD+DHP pair reads out and processes 250 drain lines, i.e. a quarter of the sensor columns.

The timing of the four DHPs is controlled by a common 76 MHz clock signal from the DHH, called GCK. Frame synchronization is implemented by a synchronization signal from the DHH on the trigger line, called TRG. The DHPs generate a 300 MHz clock and the control signals for the DCDs and switchers.

3.2 Module services

The PXD module is connected to a Kapton[1] flex at the EOS edge, further referred to as Kapton in this work. It is soldered to the module providing good contacts for the ground connection and two high current lines of the DCD power supply, AVDD and AmpLow. Two layers of lines are connected by stacked wire bonds between Kapton and module. In total 23 voltages, six differential control signals and four differential data outputs are accommodated on the Kapton module connection. It is 43 to 47 cm in length, depending on the module type. A 100-pin Samtec connector is located at its far end to provide the link to a custom patch panel with cables to Power Supply (PS) and DHH. Since PS and DHH are located on top of the Belle II detector the necessary length of the cables to the patch panel is 16 m.

The PS is custom-made [33], creating 23 voltages in four independent power domains according to the specifications of the PXD module. 16 of the channels feature remote sensing capabilities to compensate the voltage drops over the long cables. One PS unit per module is needed.

The DHH is the read-out and control system [27, 28]. It is a Field Programmable Gate Array (FPGA) system based on the Advanced Telecommunications Computing Architecture (ATCA) standard. In the full scale system, five modules are attached to a DHH unit. Internally, the DHH comprises several FPGA boards for different tasks.

- Data Handling Engine (DHE), one for each module
- Data Handling Concentrator (DHC), one per DHH unit
- Data Handling Insulator (DHI), one per DHH unit

The DHI sends the control signals to five modules. It attaches to each of them via a Camera Link Cable (CLC). The DHEs each receive the data of one module. The DHC combines data of all DHEs to full events and sends them off to the ONline SElector Node (ONSEN) and the local PXD Data Acquisition (DAQ).

For development and testing in the laboratory environment only a single FPGA board is needed. A DHE with dedicated carrier board and firmware to combine control, configuration and data receiving functionalities is used for these purposes.

3.3 Laboratory setups

For testing prototypes and modules in the laboratory a simplified system is used. The standard PXD PS and a single-board FPGA-based read-out system together with custom interconnection Printed Circuit Boards (PCBs) form the basis of it. Cooling, if necessary, is supplied by regular water cooling with aluminum or brass cooling blocks. Two different laboratory setups are used in the work described in this thesis differing in the used FPGA system.

[1] Kapton is a registered trademark of the DuPont corporation. It is an electrically isolating polyimide film used for creating flexible printed circuits

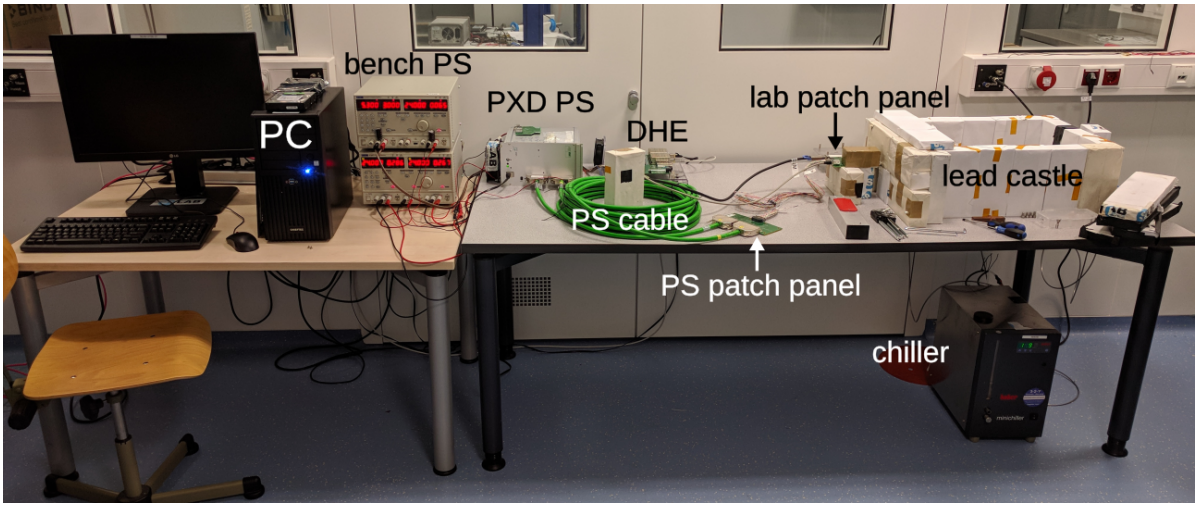


Figure 3.6: The standard PXD laboratory test setup in Bonn, full view.

3.3.1 Standard PXD setup

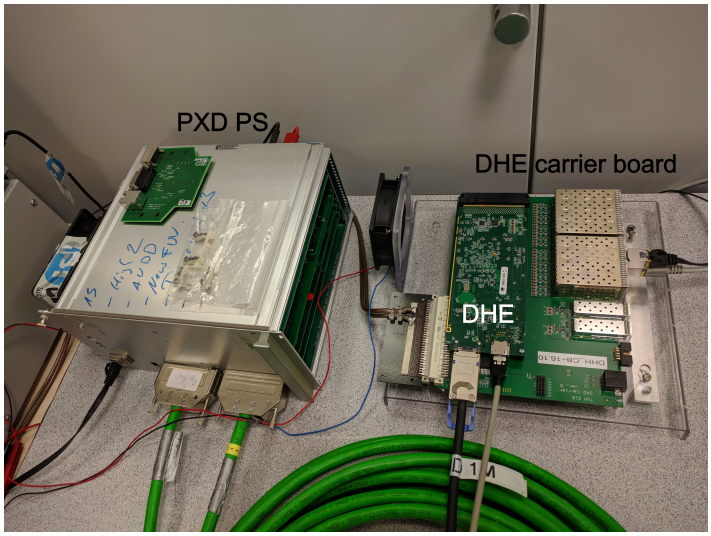
The standard setup which was used during PXD development and mass testing during the production of the detector is based on the DHE FPGA board. An overview of the Bonn setup is given Fig. 3.6. It features a lead housing for the module to facilitate measurements with radioactive sources. Two bench PS power the PXD PS, the DHE and multiple fans for cooling of the electronics. The DHE connects to power and network through a dedicated carrier board, see Fig. 3.7(a). The module Kapton cable attaches to the *lab patch panel* from where the control and data lines are routed on an Infiniband cable and a network cable to the DHE. The power lines are connected via a 51 line Glenair[2] cable to a patch panel PCB (the *PS patch panel*), which connects to the two large green PS cables interfacing the PXD PS, see Fig. 3.7(b).

In this setup, the DHE is running a dedicated firmware taking over control signal distribution, module configuration, and data collection. The data are sent out via a User Datagram Protocol (UDP) link to the PC.

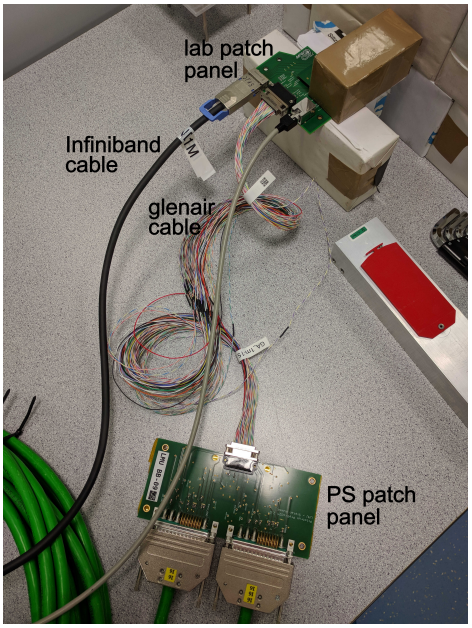
3.3.2 BDAQ-PXD

For other laboratory studies a new read-out system was developed by Patrick Ahlburg [16], the *BDAQ-PXD* system. It is based on the BDAQ53 base board, which is also used for ATLAS pixel read-out in the Bonn group. It provides easy and direct control of the firmware and system state. To operate a PXD module, the standard PXD PS is used together with the BDAQ-PXD board and a dedicated new patch panel, providing connections to the Glenair cable for power and display and network cables for control, configuration, and read-out, see Fig. 3.8.

[2] A cable connecting two Micro-D type connectors produced by the company Glenair (https://www.glenair.com/). For simplicity, the cable is referred to as *Glenair cable* in this work.



(a) Closeup of the PXD PS and the DHE on its carrier board.



(b) Closeup of the PS patch panel, the 51-line Glenair cable connecting it to the *lab patch panel*.

Figure 3.7: Closeups of standard laboratory setup components.

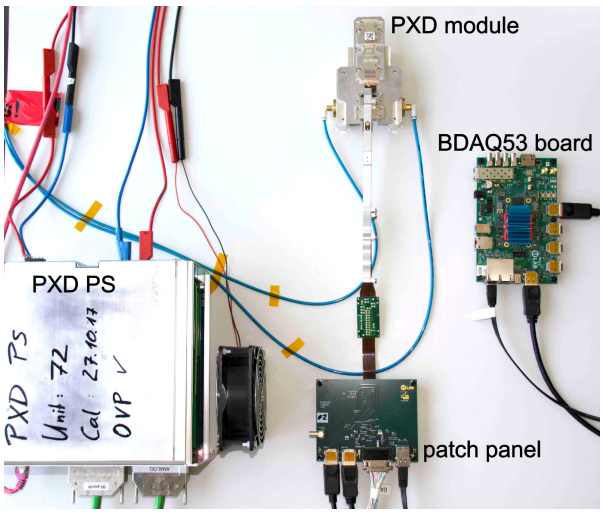


Figure 3.8: The BDAQ-PXD laboratory setup (from [16]).

CHAPTER 4

DEPFET current-voltage characteristic and backside contact

The DEPFET silicon bulk currents are expected to be of $\mathcal{O}(100\,\mu\text{A})$ according to its design. During operation in the Belle II experiment the PXD silicon bulk currents were observed to increase continuously as a function of the total received ionizing radiation dose, exceeding 10 mA.

This chapter presents studies to understand the interplay of the DEPFET biasing voltages and the origin of these currents. They are carried out in the laboratory with a previously irradiated module.

As the resolution of the PXD Power Supply current monitoring is limited to 1 mA external devices are employed to enable fine-grained measurements. Furthermore, the impact of externally applied voltages to the module backside, i.e. the handle wafer, is investigated.

4.1 Measurement setup

The base setup consists of the BDAQ-PXD laboratory setup (Section 3.3.2) and the irradiated W05_OB1 PXD module. Key components are the PXD PS 72 for powering, and the BDAQ-PXD control/readout system for configuration of the module. The BDAQ patch panel connects to the module Kapton flex. The connection to the PS is realized via the standard PXD PS cables, an adapter PCB and a modified Glenair power cable. Control and data communication to the BDAQ board are implemented with Display Port cables.

The module itself is screwed to an aluminum jig at the end-of-stave with the standard screw and torque of 15 mN m, see Fig. 4.2.

The modified Glenair power cable one to add multimeters or Source Measure Units (SMUs) with banana cables to the voltage supply lines, see Figs. 4.1 and 4.3. The currents are measured with Keithley 2400, 2500 and 2600-series SMUs and 2000-series multimeters. The readout is implemented by standard SCSI commands via LAN and serial interfaces. To facilitate the combined measurement of PXD-PS-internally-monitored currents and the external measurements the device readout is implemented into StreamApp EPICS IOCs.

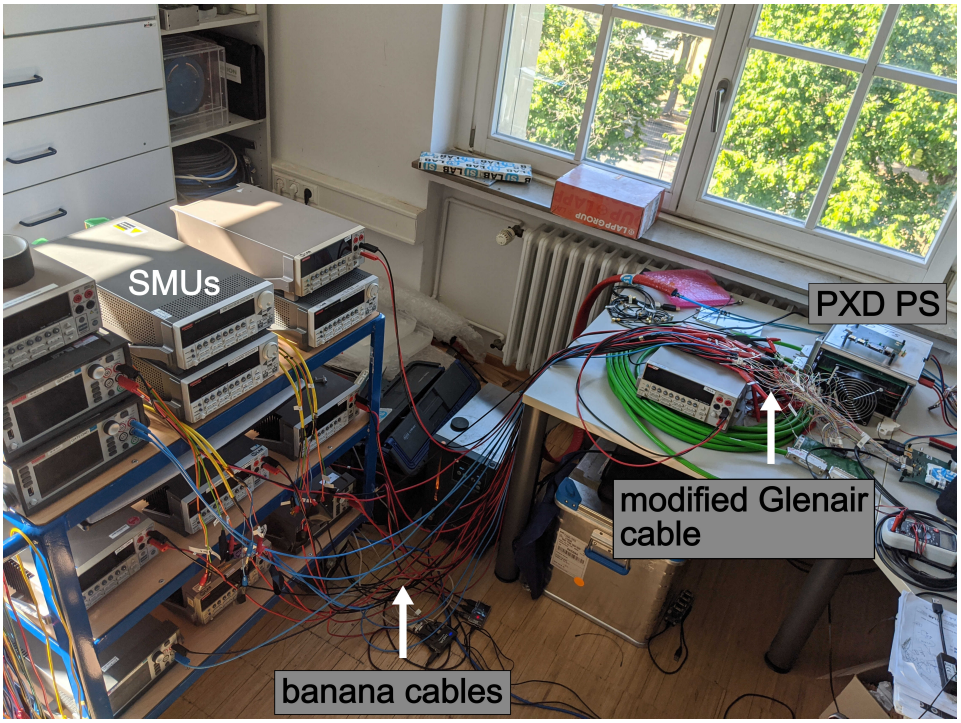


Figure 4.1: Overview of the module current measurement setup. On the left side is the array of Keithely SMUs and multimeters, on the right side are the patch panel, PXD PS, cables and PS adapter board.

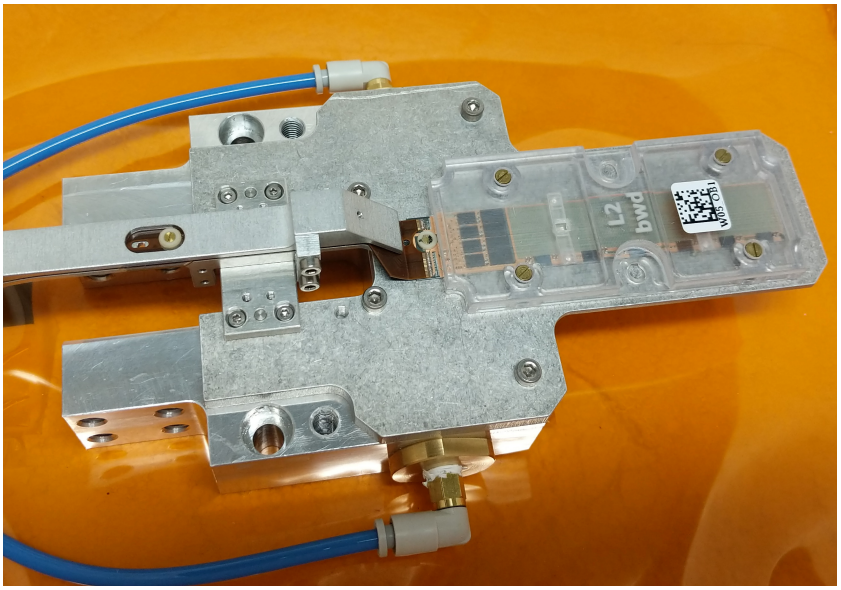


Figure 4.2: Module W05_OB1 on aluminum jig with attached cooling block and protective plastic cover.

Figure 4.3: Glenair power cable with banana plug modification.

4.1.1 W05_OB1 module

The W05_OB1 module was irradiated to $\sim 100\,\mathrm{kGy}$ in January 2019. Before and after the irradiation, it was extensively tested in the laboratory and at beam tests. Apart from a problematic DCD/DHP pair, it behaves well and can be seen as a nominally operational module. Details on its irradiation and beam test characterizations are found in [34, 35]. The measurements presented in this chapter were conducted in June 2020. Therefore, effects of the previous irradiation, especially the increased backside currents, are present in the module.

4.2 DEPFET IV curves

The current-voltage characteristic or I-V curve is defined as a graph of the current and corresponding voltage through a device. It provides information about basic parameters like resistance for linear devices, differential resistance for diodes or transconductance for transistors. For multi-terminal devices like the DEPFET the current of one terminal generally depends on several voltages. Therefore, multiple graphs and families of curves have to be considered. The results of the I-V curve measurements are presented in the following.

4.2.1 HV I-V curves

The High-Voltage (HV) channel biases the p+ sensor backside via PT (cf. Section 2.5). It is referenced to source and negative in comparison. When the PT is established the sensor bulk depletion grows from the backside depending on the voltage difference between n-bulk and p+ backside. The front side of the sensor is largely p-doped with the source, drain and drift implantations, where source is the most positive (0 V). The HV current is a pure hole current. Below the front side PT threshold it is caused by bulk- and surface-generation currents between the bulk n-contact and the HV p+ front-side implantation.

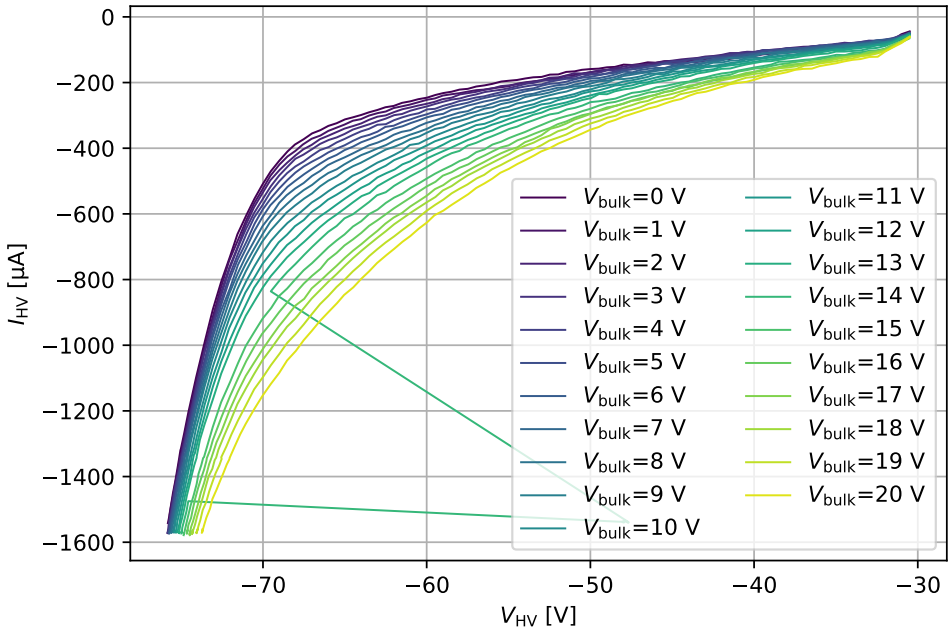


Figure 4.4: HV I-V curve for varied bulk voltages.

Once the PT to the front side is established, the current increases exponentially as a direct hole-current between source and back side can overcome the potential barrier.

Figure 4.4 shows the HV IV curve of module W05_OB1 for different fixed values of the bulk voltage V_{bulk}. From the right, the curves start close to −30 V as the lowest absolute V_{HV}. This is where the PT to the back side is expected to be established, which can be accompanied by a relative jump in current, since all back-side surface defects become depleted. For the lowest bulk voltage, $V_{\text{bulk}} = 0$ V, the lowest HV current, I_{HV}, flows. The current increases from $\sim -100\,\mu$A to $\sim -350\,\mu$A at about −67 V. At this point a characteristic kink occurs and I_{HV} starts increasing steeply. This indicates that the PT to the front side is reached and a current flows between HV and source. The increase is theoretically exponential with V_{HV}.

For more positive V_{bulk}, I_{HV} is generally higher (more negative). I_{HV} increases more quickly with increased $V_{\text{bulk}} - V_{\text{HV}}$ difference and the difference to the $V_{\text{bulk}} = 0$ V I-V curve becomes largest around the expected front-side PT of −67 V. This increased current is likely due to the preceding irradiation of the module. Increased I_{HV} values were observed in irradiation campaigns and during operation in the Belle II experiment, as described above. Dedicated studies are in progress and will be published by Georgios Giakoustidis, PhD student at the Bonn Belle II group, later this year. The current hypothesis is an avalanche due to high fields at the edges of the back-side diode implant. With irradiation the fields increase because of accumulating positive charge in the oxide layer between bulk and handle wafer. The location of the presumed avalanche is marked in Fig. 4.6.

4.2.2 Bulk I-V curves

Figure 4.5 shows the bulk current I_{bulk} as a function of V_{HV} for different fixed V_{bulk} values. The current I_{bulk} becomes more positive as V_{HV} gets more negative. This coincides with the increasing (more negative) HV current, I_{HV}, as a large portion of the current flows between HV and bulk, especially at the

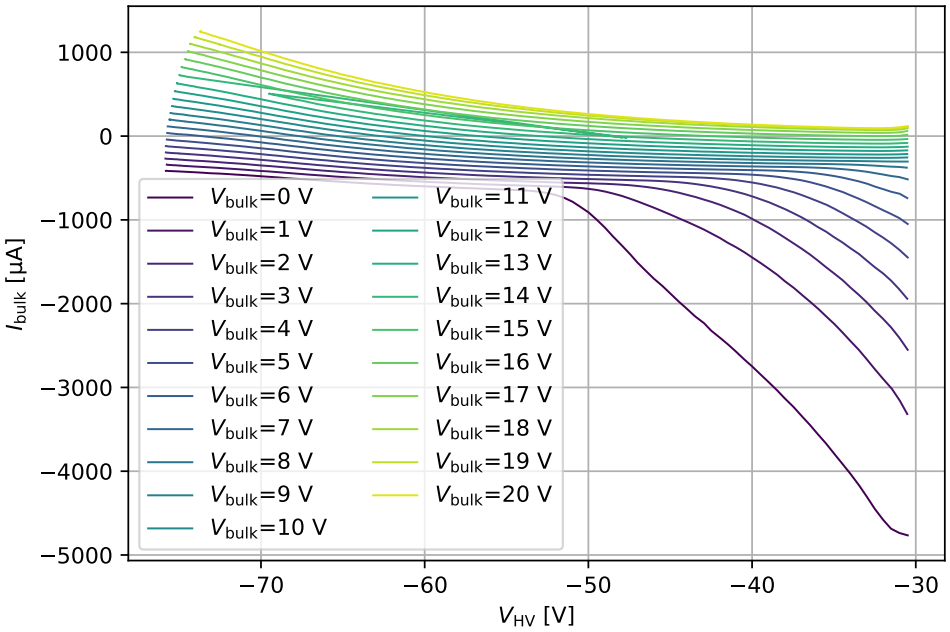


Figure 4.5: Bulk current vs. HV for varied bulk voltages.

edges of the back-side implant.

For V_{bulk} values lower than ~ 8 V a substantial negative bulk current flows, i.e. current flows into bulk from a more positive implant. This is a current between bulk and clear at the edge of the sensor which gets inhibited once the silicon bulk is sufficiently depleted by U_{HV}.

For large negative V_{HV} values I_{bulk} increases more slowly compared to I_{HV} as a large fraction of the HV current flows into source.

4.2.3 Handle-wafer contact

Since the potential of the handle wafer influences the electric field in the hypothesized avalanche generation region around the back-side implant, it is instructive to vary it. Therefore, the aluminum jig is biased to a defined voltage relative to the PS analog ground (AGND) by an SMU. The PXD PS provides four different power domains, defining four grounds. AGND constitutes the ground of the source voltage V_{source}, while steer GND constitutes the ground is referenced to V_{source} and constitutes the ground of the steer domain providing several DEPFET voltages, such as HV and bulk. Figure 4.6 shows a schematic image of the DEPFET sensor, DCD, PS and aluminum jig biasing. The voltages are given for standard PXD operation voltages, $V_{\text{HV}} = -60$ V, $V_{\text{bulk}} = 10$ V. As illustrated, the HV PT is expected to be symmetric, dropping 30 V from implant to back side and again 30 V from back side to source implant on the front side.

Figure 4.7 shows the current I_{HV} as a function of V_{HV} for different applied V_{jig} values. In the floating case (no current) a voltage of 18.9 V is measured. This is assumed to correspond roughly to $V_{\text{back side}}$.

$$V_{\text{jig}} = V_{\text{drop,AGND}} + V_{\text{source}} + V_{\text{drop,steer-¿source}} + V_{\text{bulk}} + V_{\text{drop,bulk-¿cutting-edge}} \tag{4.1}$$

Here, V_{source} and V_{bulk} are known to be 6 V and 10 V, respectively. The voltage drop on the AGND line

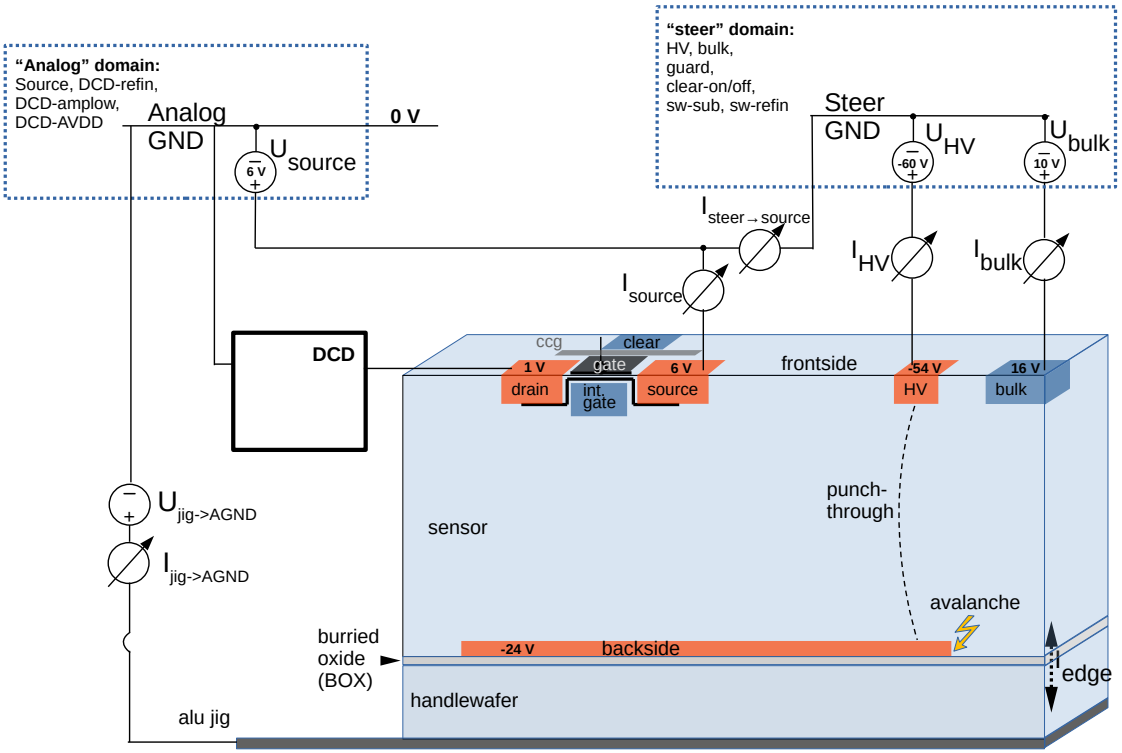


Figure 4.6: Schematic of the PS, aluminum jig, and implant voltages and current measurements. The location of the avalanche is shown at the edge of the back side implant.

is quite large due to the high current of ~ 1.8 A flowing on this line and has to account for most of the difference between the measured 18.9 V and the roughly 16 V of $V_{\text{bulk}} + V_{\text{source}}$. The 0 V reference is given close to the module, therefore AGND on the PS is actually negative relative to it. There is also a voltage difference between source and steer-GND, but it is not very large.

As can be read off from the measurement results, for V_{jig} values between 10 to 20 V, the I-V curve does not change much. But for more negative values I_{HV} decreases (becomes less negative). At the approximate front-side PT of -67 V, a current difference of 200 µA is observed for $V_{\text{jig}} = -20$ V. This corresponds to a change from $V_{\text{bulk}} = 10$ V to 3 V compared to the previous measurements without a voltage attached to the jig.

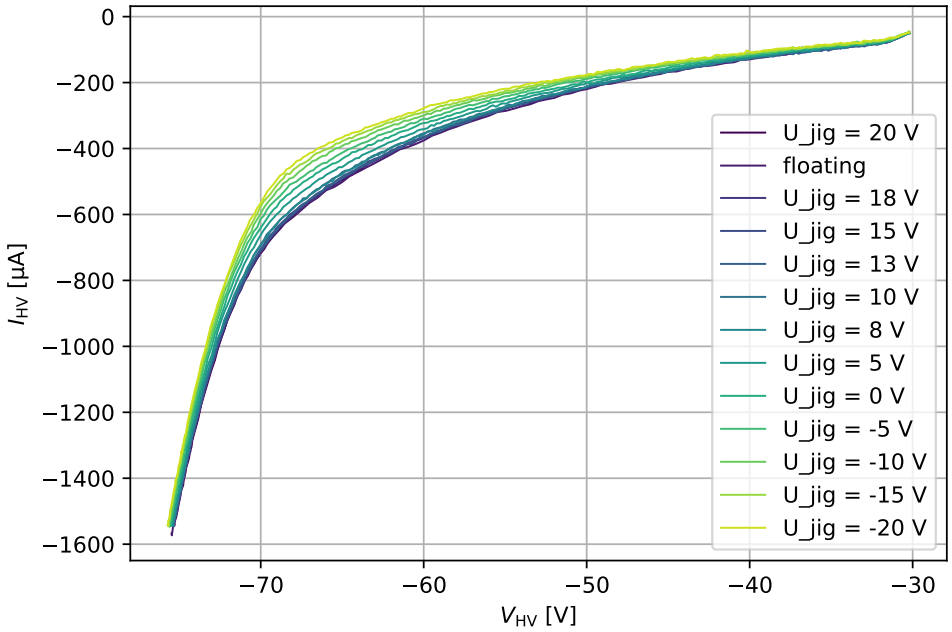


Figure 4.7: HV I-V curve for varied support-jig voltage, $V_{\text{bulk}} = 10\,\text{V}$.

4.3 Conclusion

The results provide evidence that the handle wafer potential changes the size of the current between HV and bulk in this irradiated module. This observation fits the hypotheses of increased electric fields around the back-side implant after irradiation. The effect appears to be alleviated when changing the handle wafer voltage.

Another observation is that a bare connection between module back side and untreated aluminum surface provides an electrical connection. But the effect on the module currents appears small. In the experiment or other setups a handle wafer to ground connection could accidentally be established if the isolation to the cooling block fails. According to this measurement no large impact, at least on DC-level, would be expected.

CHAPTER 5

PXD9 Pedestal Currents

For operation of the PXD, the variation of the DEPFET currents constitutes the signal. The nominal working point of the pixels is $\sim 1\,\mu A$. Most of the current is subtracted before digitization by adjustable current sinks in the DCDs. Their input range therefore only needs to encompass the *pedestal spread* and signal. The selected amplification together with the 8-bit Analog to Digital Converter (ADC) results in an input range of 20 to 25 μA.

The pedestal spread is of significant size compared to this range. It arises from process variations and property variations of the underlying substrate. In this chapter, different contributions to the pedestal spread are investigated. They can be attributed to process level and wafer scale property fluctuations on one side and variations between channels and chips of the DCD and switcher ASICs on the other side.

All presented results originate from measurements conducted with fully equipped modules in nominal operation. They reflect the situation as expected in operation in the Belle II experiment. As a caveat, contributions of ASICs and sensor cannot be fully separated without measuring the components independently. All components are quality-checked before assembly[1], but the measurements are coarse and under static conditions and can therefore not be compared with these fine-grained evaluations.

In the following, the term *pedestals* refers to the signal-free DEPFET currents as measured by the DCD, i.e. after subtraction of global offset currents at the input.

5.1 X-ray Inspection Damage

The modules undergo X-ray inspection during production to check the connection of components after assembly. After flip-chip connection of the ASICs to the module, X-ray inspection is carried out to visually confirm placement and quality of the bump connections. Radiation damage from these inspections can be seen in many modules at the edges of the sensor.

Figure 5.1 shows the raw pedestals of module W46_OB1. Visible radiation damage from X-ray inspection of the ASICs is present at the left and bottom edges.

For a quantitative evaluation of the radiation induced pedestal shift, a correction is calculated and shown in Fig. 5.2. The edge of the damaged area is determined by finding the step in the pedestal distribution for each row (column) by differentiation. The correction for the damaged region is then

[1] The sensors are tested at HLL. They are checked for shorts and collective (parallel) IV-curves. No pixel-wise IV-curves of the whole sensor exist. DCDs and switchers are tested at KIT [24][36, p. 111].

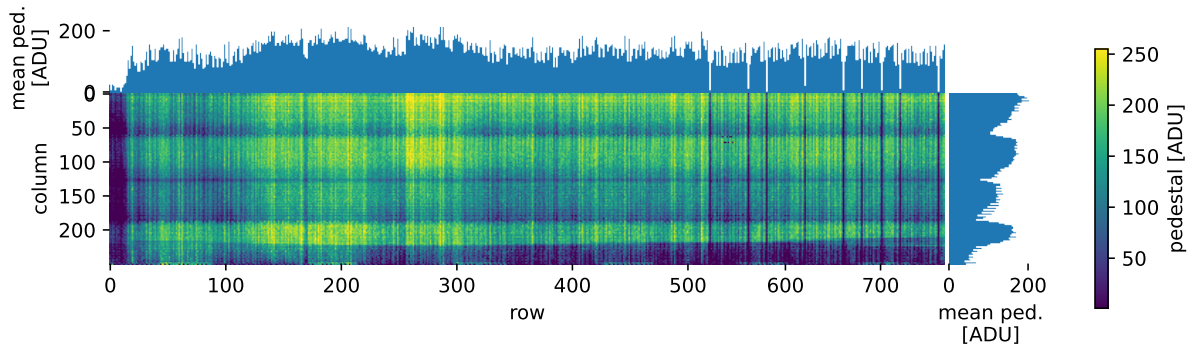


Figure 5.1: Pedestals of module W46_OB1 in Analog Digital Units (ADUs). The central plot shows a map of pixel pedestals according to their position on the sensor. Relative scales of rows and columns corresponds to actual sensor size. The top (right) plot shows the mean pedestals per row (column). The DCDs are located near row 0 (left) and the switchers near column 250 (bottom) in this representation.

evaluated for each row (column) by calculating the mean pedestal difference per row (column) of the areas with and without damage. For the damage from switcher inspection only pixels of the DCD at the corresponding module edge are taken into account in the calculation. Figure 5.3 shows histograms of the pedestal distribution highlighting pedestals of the damaged region and the size of the shift. Pedestals originally outside the DCD's input range could not be corrected as their values are not known from the measurement.

The average shift is of size 50 to 100 ADU. The shift appears to be larger, around ~ 100 ADU, near the DCDs. This could be explained by longer exposure or different energy spectrum used for inspection of these ASICs compared to the switchers. Assuming a DCD gain of $A_{\mathrm{DCD}} = 10\,\mathrm{ADU}\,\mu\mathrm{A}^{-1}$, $g_{\mathrm{m}} = \frac{\mathrm{d}I}{\mathrm{d}V} = -70\,\mu\mathrm{A}\,\mathrm{V}^{-1}$ and voltage shift per ionizing dose $\frac{\Delta V}{D} = 230\,\mathrm{Gy}\,\mathrm{mV}^{-1}$ [37, p.181][2], we get:

$$\Delta I \approx \Delta I_{\mathrm{ADU}} / A_{\mathrm{DCD}} = 5 \text{ to } 10\,\mu\mathrm{A}$$
$$\Delta V \approx \Delta I / g_{\mathrm{m}} = 70 \text{ to } 140\,\mathrm{mV}$$
$$D \approx \frac{D}{\Delta V} \cdot \Delta V \approx 0.3 \text{ to } 0.6\,\mathrm{Gy}$$

[2] This value was determined by irradiation with operating matrix. Here, the irradiation takes place while the matrix is off. This effectively changes the voltage across the gate-oxide which has a significant influence on the radiation induced oxide charge and therefore the threshold shift. On the other hand, during integration time a comparatively positive voltage $V_{\text{gate-off}}$ is applied, switching off the FET and reducing the electric field across the oxide. In test structure measurements, to be published, a similar threshold shift per dose was observed also for a switched-off device. Details: H5_30 with matrix W46_J00 (PXD9-7, L5_Z85).

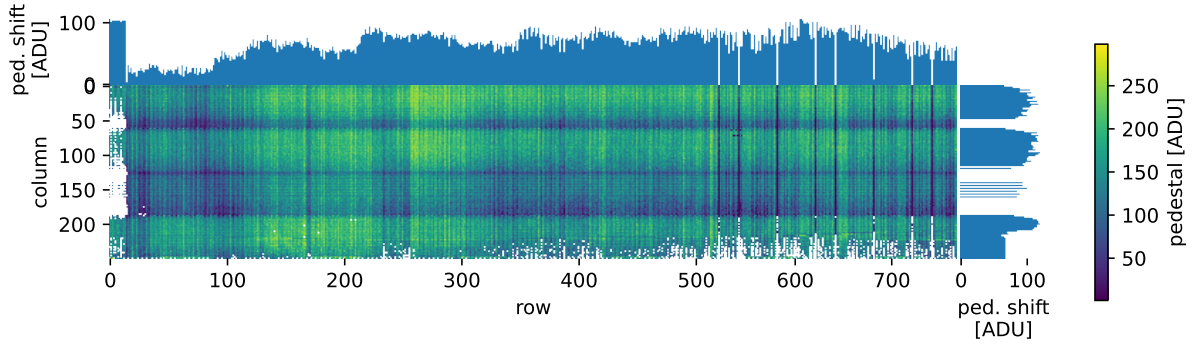


Figure 5.2: Pedestals of module W46_OB1 in ADUs with corrected damaged areas. The central plot shows a map of pixel pedestals according to their position on the sensor. Relative scales of rows and columns corresponds to actual sensor size. The top (right) plot shows the mean radiation-induced pedestal shift of the affected areas per row (column). White pixels are outside the DCD range (¡ 2 or ¿ 254). The DCDs are located near row 0 (left) and switchers near columns 250 (bottom) in this representation.

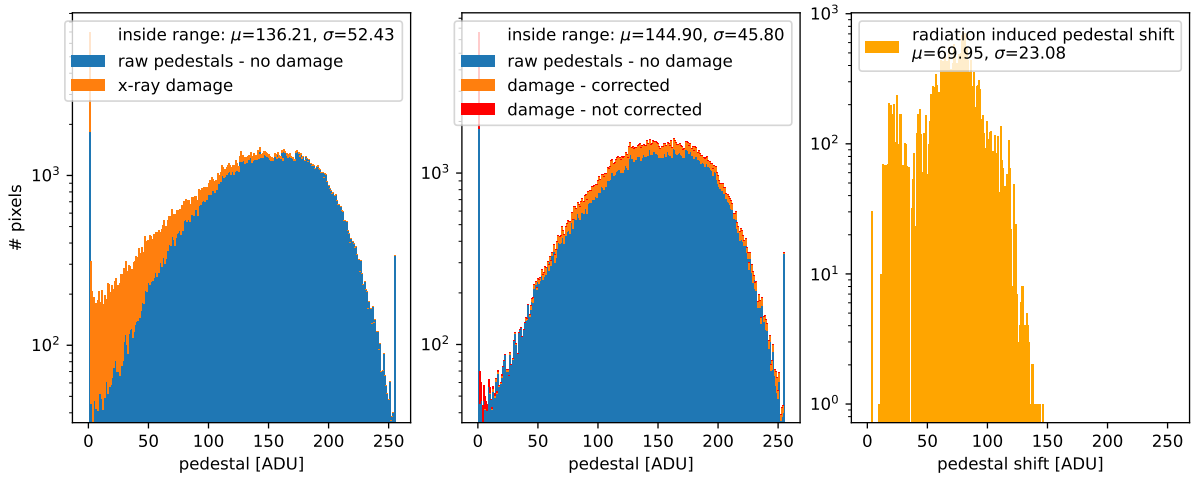


Figure 5.3: Histograms of pedestals of W46_OB1 before (left) and after (middle) correction of X-ray-inspection radiation damage. Right: Histogram of pedestal shift in damaged area. The parameters μ and σ denote the mean and standard deviations of the distributions, respectively. For the pedestal histograms only values within the DCD input range (1 ¡ value ¡ 255) are taken into account in their calculation.

5.2 Row Pedestal Deviations

Most modules exhibit significant row-to-row variations. These are visible as vertical stripes in the pedestal map, e.g. in Fig. 5.1. Upon inspection, significant outliers are visible in the last third of the rows of W46_OB1 where every 20th row shows significantly lower values compared to their neighboring rows. Having a look at the raw pedestals of all W46 sensors in Fig. 5.4, it is apparent that all modules show patterns of deviating rows of pedestals. The severity and frequency of the outliers appears to vary between sensors and also change in the same sensor with pixel size.

5.2.1 Recurring Pattern Length

To find the length of repeating outlier patterns the mean row pedestals of the different sensor areas are divided into sub-samples of n rows and their mutual correlation is measured. The Pearson correlation coefficients $R_{i,j}$ are calculated for all pairs of sub-samples of length n. Afterwards they are averaged and divided by their standard deviation σ_R to obtain a single Figure Of Merit (FOM):

$$r_{\mathrm{n}} = \frac{\sum_{i<j} R_{i,j}}{\sigma_R} \tag{5.1}$$

Subsequently, the results are normalized for each area for easier comparison:

$$\hat{r}_{\mathrm{n}} = r_{\mathrm{n}} / \max_{\text{px. area}} (r_{\mathrm{n}}, n \in [2..70]) \tag{5.2}$$

The results for all modules of wafer 46 are shown in Fig. 5.5 and Fig. 5.6. The two plots show the same results once as bar plot once as a 2D histogram.

Clear peaks in correlation are found and can be verified by plotting the row sub-samples next to each other as in Fig. 5.7. Periodically occurring relative variations of mean pedestals stand out as horizontally continuous features in these plots. For most sensors the periodicity is evident in this visualization. The checkered pattern for the 60 µm pixel areas of the IF/IB module arises from a double-row effect overlaid with the ten-row period of the pattern, details are given in Section 5.3.

The obtained periodicity of the recurring row patterns is listed in Table 5.1. It is evident that the length of the pattern corresponds to the Least Common Multiple (LCM) of the pixel pitch and 200 µm.

The same plots have been produced and analyzed for wafers 9, 37, 56, 57 and 67. They can be found in Appendix A.1.1. Table 5.2 summarizes the obtained periodicities. Wafers 9, 37 and 46 all exhibit the same pattern lengths, while wafers 56, 57 and 67 have different pattern lengths pointing at a difference in the production process. The repetition lengths in µm are given in Table 5.3 and shown to be a common multiples of the pixel pitches and 160 µm. Wafers with numbers ≥ 50 belong to PXD9-20 and following

pixel pitch [μm]	pattern length [rows]	pattern length [µm]
55	40	2200
60	10	600
70	20	1400
85	40	3400

Table 5.1: W46 length of periodically occurring patterns in mean row pedestals.

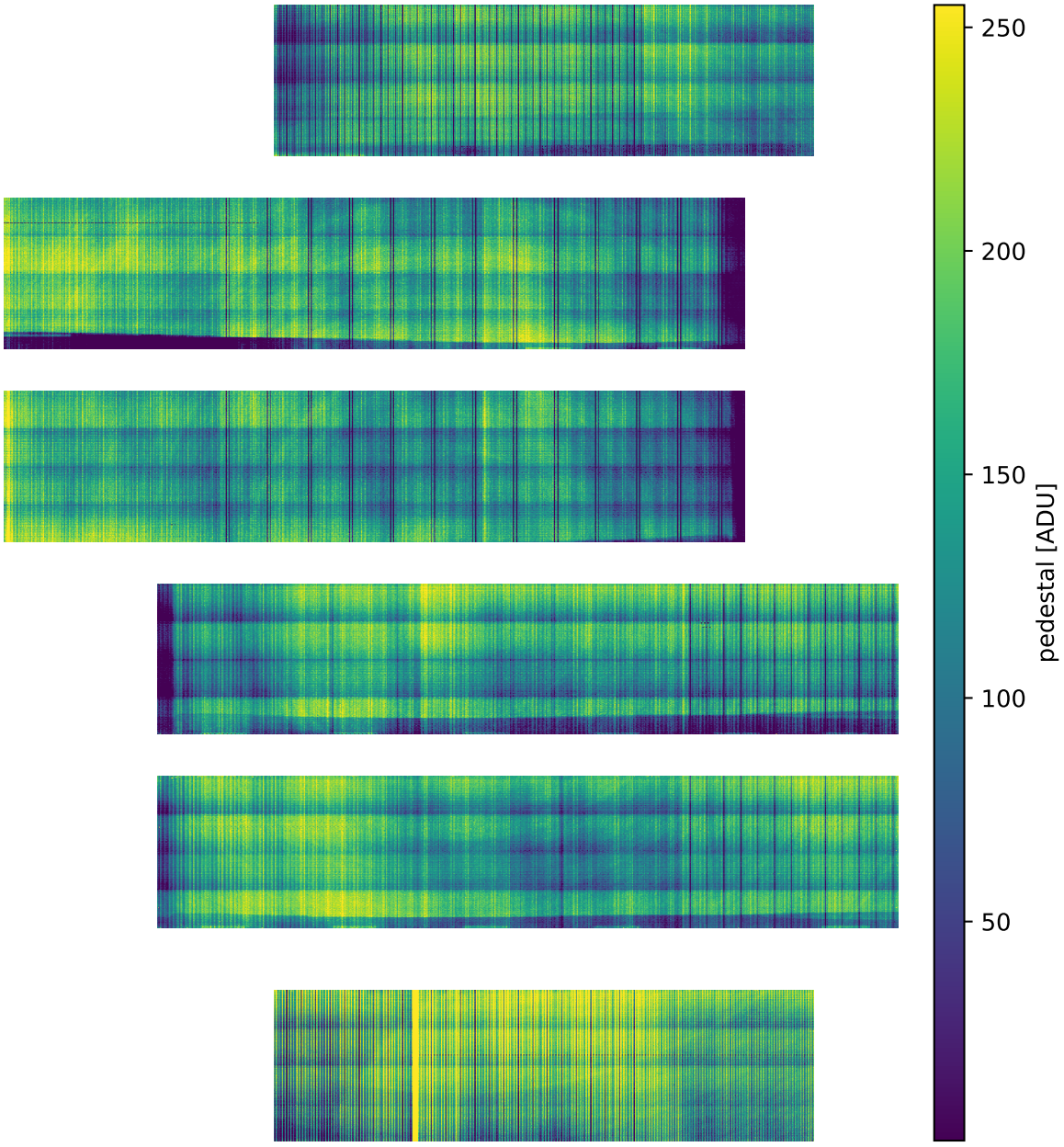


Figure 5.4: Raw pedestal maps of modules from wafer 46. The relative position and size of the pixels in this figure corresponds to their position and size on the wafer. The color code denotes the pedestal value in ADU.

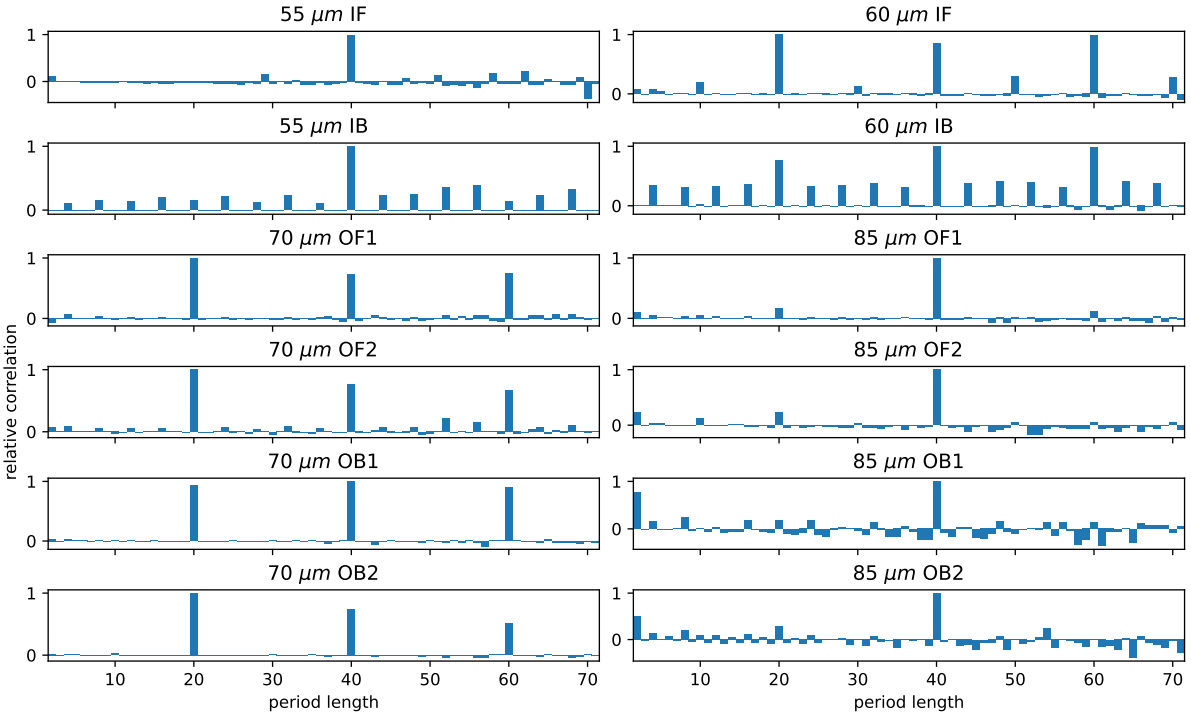


Figure 5.5: W46 relative correlation $\hat{r}$ of mean row pedestal sub-samples. For each sensor, both pixel size regions are shown individually.

wafer	periodicity [rows]			
pixel pitch [µm]	55	60	70	85
W09	40	10	20	40
W37	40	10	20	40
W46	40	10	20	40
W56	32(64)	16	32	64
W57	32(64)	16	32	64
W67	64	16	–	–

Table 5.2: Length of periodically occurring patterns in all examined wafers.

production batches.

5.2.2 Row Deviation Strength and Correlation

Calculating the mean value of every n-th row, a measure for the variation of rows in the pattern can be obtained. Figure 5.8 displays this quantity. The histograms in this figure exhibit an obvious correlation between same-type modules, i.e. OF1/2 and OB1/2. Especially the outlier row 'nine' in the OB 70 µm region and the double-outlier in rows 22 and 25 in the OF 85 µm regions stand out. Also, the IF and IB module sub-rows appear to be correlated, well visible in the 60 µm region with the outlier in row eight. Figure 5.9 shows correlation plots of these same-type sensor regions and quotes the R-values, confirming

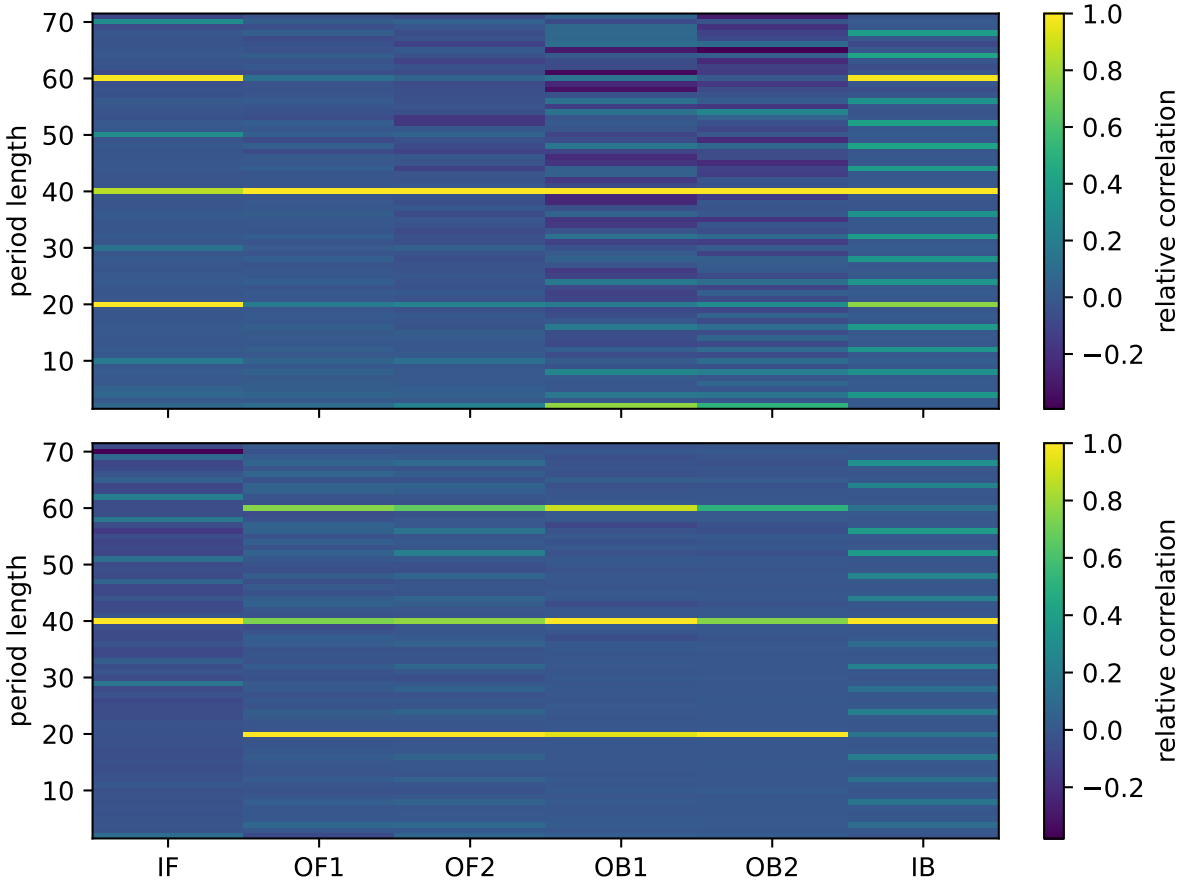


Figure 5.6: W46 relative correlation $\hat{r}$ of mean row pedestal sub-samples.

pixel pitch [μm]	pattern length [rows]	pattern length [µm]
55	32	1760
60	16	960
70	32	2240
85	64	5440

Table 5.3: Wafers 56, 57 and 67 length of periodically occurring patterns in mean row pedestals.

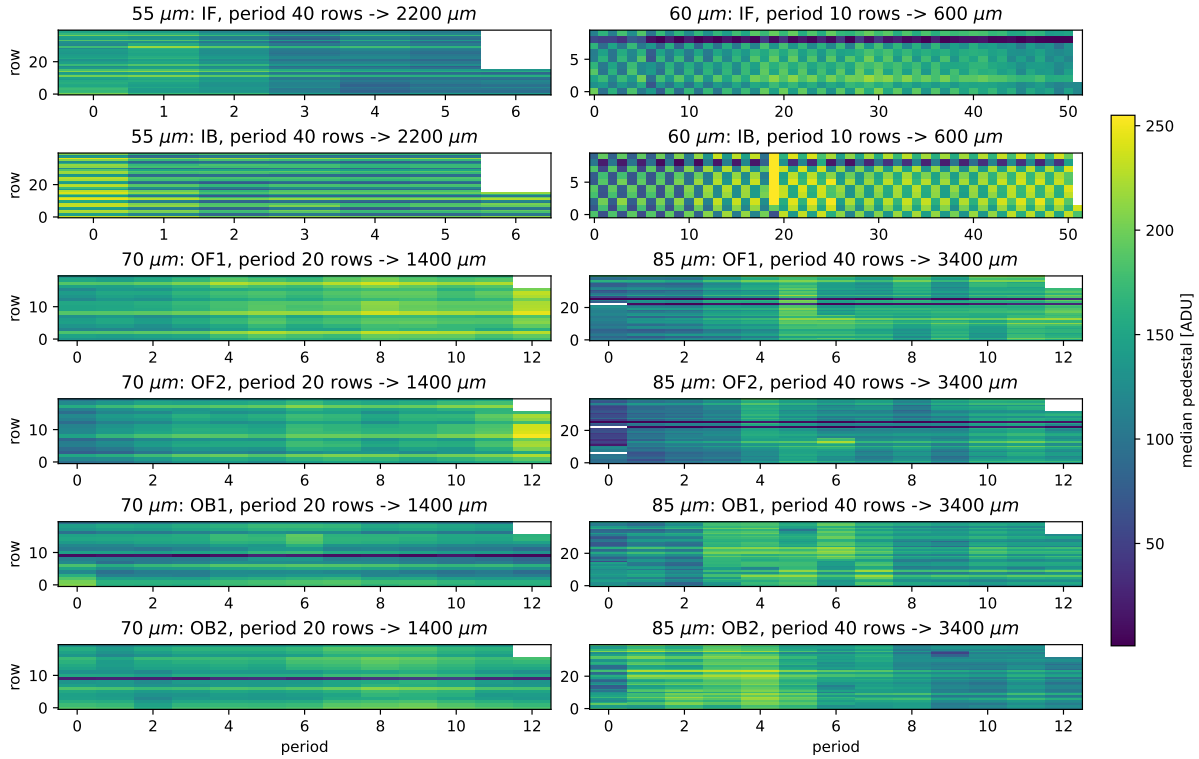


Figure 5.7: W46 row sub-samples of n rows. n is given in the title of the respective sub-plot.

significant numerical correlations for these pairs. The 70 µm and 85 µm pixel areas of OF/OB-type sensors have the same design, but they are shifted by 85 µm horizontally on the wafer. This could explain the non-correlation between these areas. IF/IB modules on the other hand are exactly identical and on identical x-positions on the wafer.

The plots illustrating the same analysis for wafers 9, 37, 56, 57, and 67, are available in Appendix A.1.2. Table 5.4 summarizes the strength of the outliers in each measured sensor in ADU.

wafer	deviation [ADU]											
pitch [μm]	55		60		70				85			
sensor	IF	IB	IF	IB	OF1	OF2	OB1	OB2	OF1	OF2	OB1	OB2
W09	11	25	23	58	26	26	80	60	68	67	19	14
W37	48	–	13	–	31	–	30	–	49	–	30	–
W46	59	73	133	100	39	36	133	124	134	117	38	43
W56	27	15	60	40	18	19	53	39	65	59	30	26
W57	–	41	–	48	34	50	43	–	50	56	50	–
W67	30	19	56	28	–	–	–	–	–	–	–	–

Table 5.4: Outlier row strength in ADU.

After extracting the average periodic row deviations, the raw pedestals can be corrected by that amount. The result is shown for wafer 46 in Fig. 5.10. Inhomogeneities along the columns are visibly reduced. As

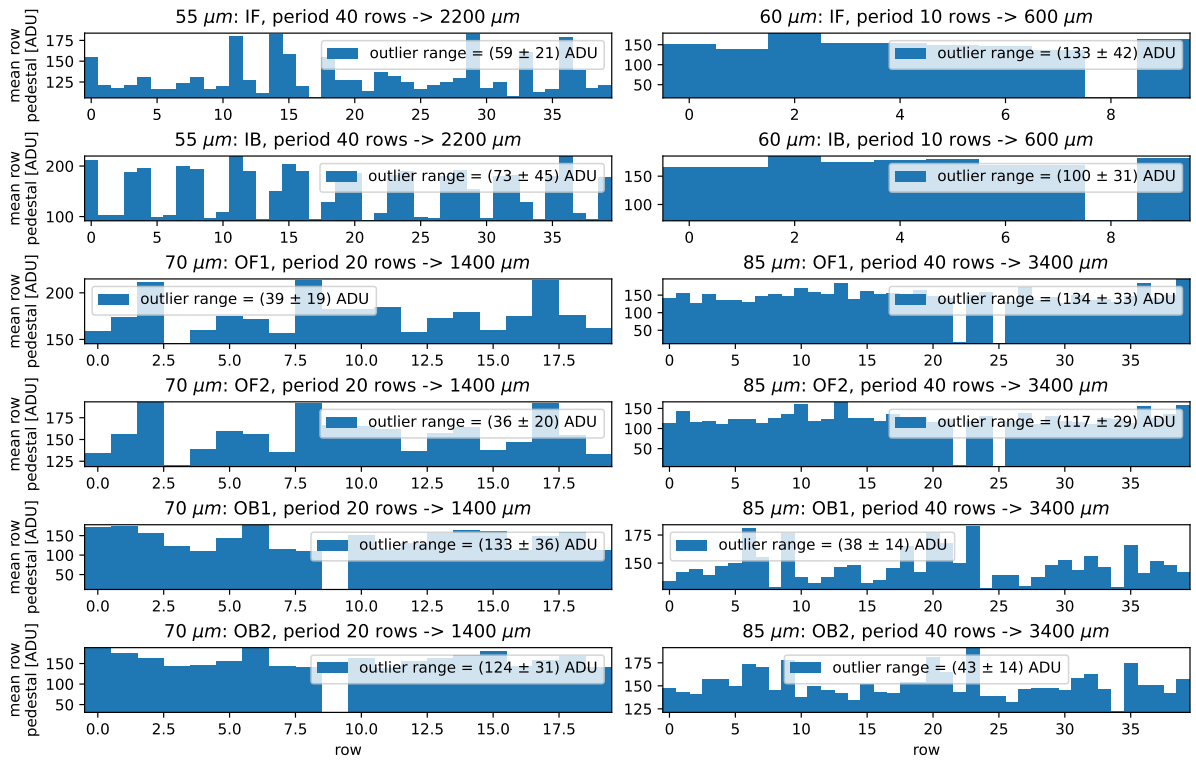


Figure 5.8: W46 mean sub-sample row pedestals in recurring pattern. The legend quotes the maximum deviation from the mean and the standard deviation in ADU

a more detailed example, Fig. 5.11 shows the difference before and after periodic row pattern correction for module W46_OB1 and the mean row pedestal values which become visibly smoother. All pixels with raw pedestal values outside the DCD input range, i.e. ≤ 1 ADU or ≥ 255 ADU are removed in these visualizations since their initial offset cannot be known from a simple pedestal measurement.

Nevertheless, significant row-to-row inhomogneities are still visible after the periodic row pattern correction. These are investigated in Section 5.3.

5.2.3 Conclusion

The pattern direction, periodicity and length point to a connection to the Direct Wafer Lithography (DWL) in the production. DWL is used at HLL for writing photo resist masks for etching the poly-silicon and metal layers. The masks for poly-Si and aluminum structures are written with a laser system working along the wafer in row direction (vertically) in stripes of a specific width It was confirmed by HLL that for older productions, $W < 50$, a Heidelberg Instruments DWL-200 machine with a scan width of 200 µm was used, while for newer productions, $W \geq 50$, a Heidelberg Instruments DWL-2000 machine with a scan width of 160 µm was used. This matches exactly the observations.

The vertical stripes are stitched together in horizontal direction by moving the writing head along after each stripe. The laser spot intensity varies within the lines and the line-to-line position can slightly vary leading to variations of length or width of layout features. Since the DEPFET gates run in row direction, particularly their length dimension could be influenced by these variations. Similar observations have

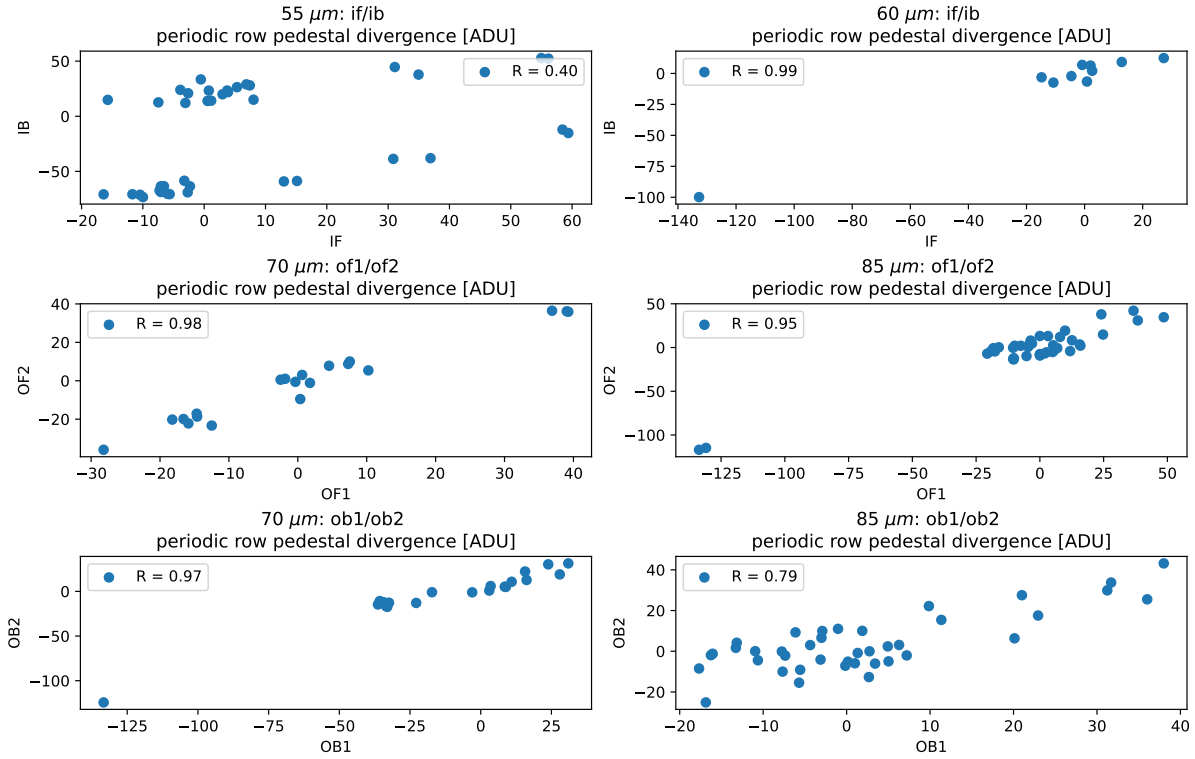


Figure 5.9: W46 correlation of same-layout areas.

been made in the characterization of different test structures of the DEPFET sensors for the Advanced Telescope for High-ENergie Astrophysics (ATHENA) with a DWL with of 200 µm and a pixel width of 100 µm, resulting in an even-odd column pattern [38, p. 69]. The FET drain current in saturation, $I_{\mathrm{D,sat.}}$, depends on the width, W, and length, L, of the gate:

$$I_{\mathrm{D,sat.}} \propto \frac{W}{L} \quad . \tag{5.3}$$

Therefore, variations in gate length L cause drain current $I_{\mathrm{D,sat.}}$ variations of

$$\Delta I_{\mathrm{D,sat.}} = \left(\frac{L}{\Delta L} - 1\right)^{-1} \cdot I_{\mathrm{D,sat.}} \overset{L \gg \Delta L}{\approx} \frac{\Delta L}{L} \cdot I_{\mathrm{D,sat.}} \quad . \tag{5.4}$$

Especially notable are the distances between the extreme outlier rows 22 and 25 in the W(< 50)_OF1/2 85 µm pixel area in e.g. Fig. 5.8 and the extreme outlier rows 17 and 54 in the W(≥ 50)_OF1/2 85 µm regions, e.g. in Fig. A.23. These outliers appear in the same rows on different wafers. Since these outliers are much larger than the deviations of most other rows from the mean it is likely that a significant discontinuity in the process aligns with a particularly vulnerable structure in these cases. The common contributor to the periodic pattern was shown to be 200 µm for the W(< 50) cases. Going from row 22 to row 25, the distance between the gates is very close to 200 µm because of the double-cell design: Two rows of pixels span 2 · 85 µm = 170 µm and the gate-to-gate distance between two neighboring pixels of a double-cell (even to odd numbered row) is ∼ 30 µm. The gate-to-gate distance of rows 17 and 54 in the

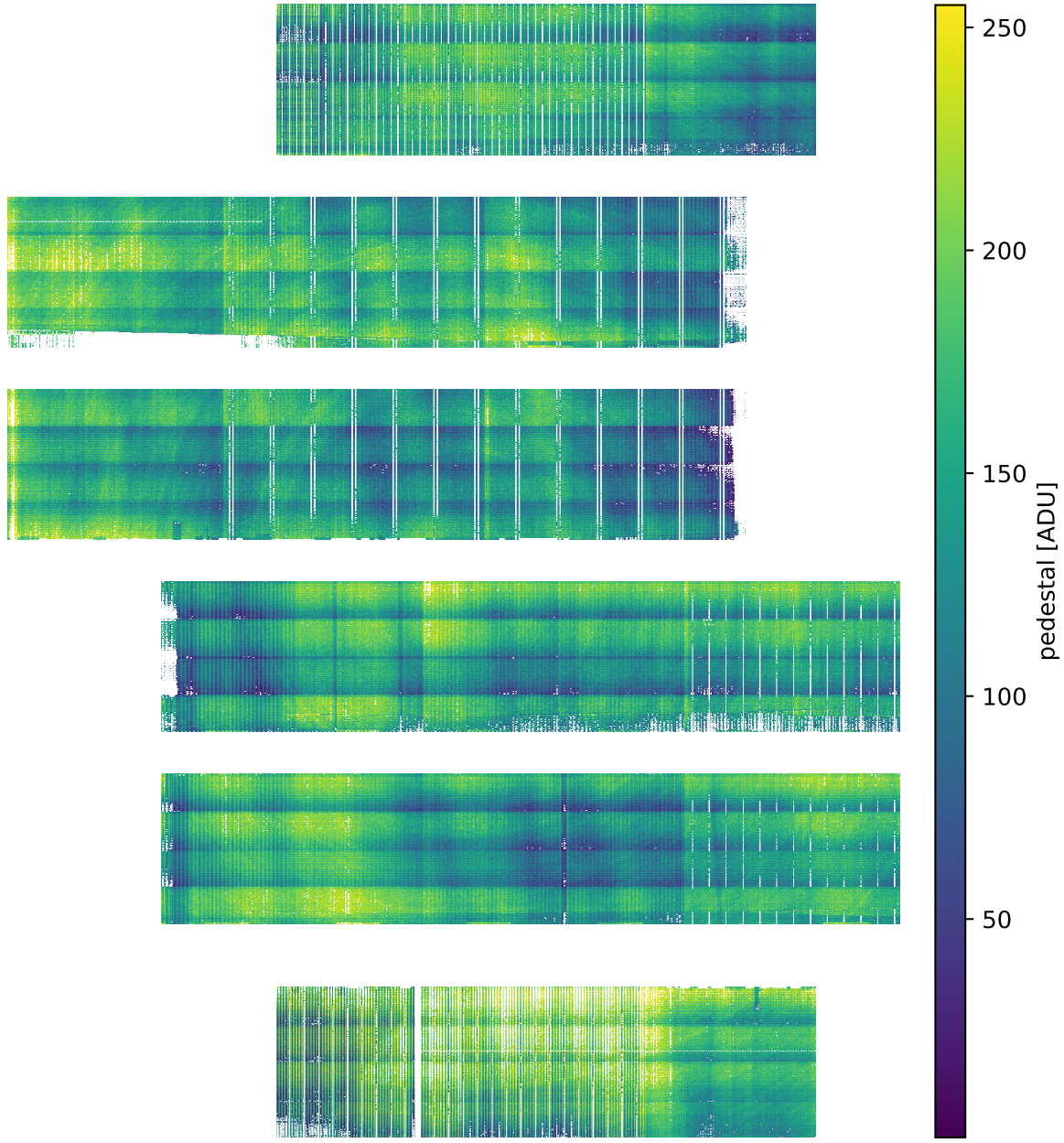


Figure 5.10: W46 pedestals corrected for X-ray inspection damage near the ASICs and for the periodic row patterns described above. The color scale indicates the corrected pedestal values in ADU. White pixels have raw pedestals outside the dynamic range and are therefore not corrected.

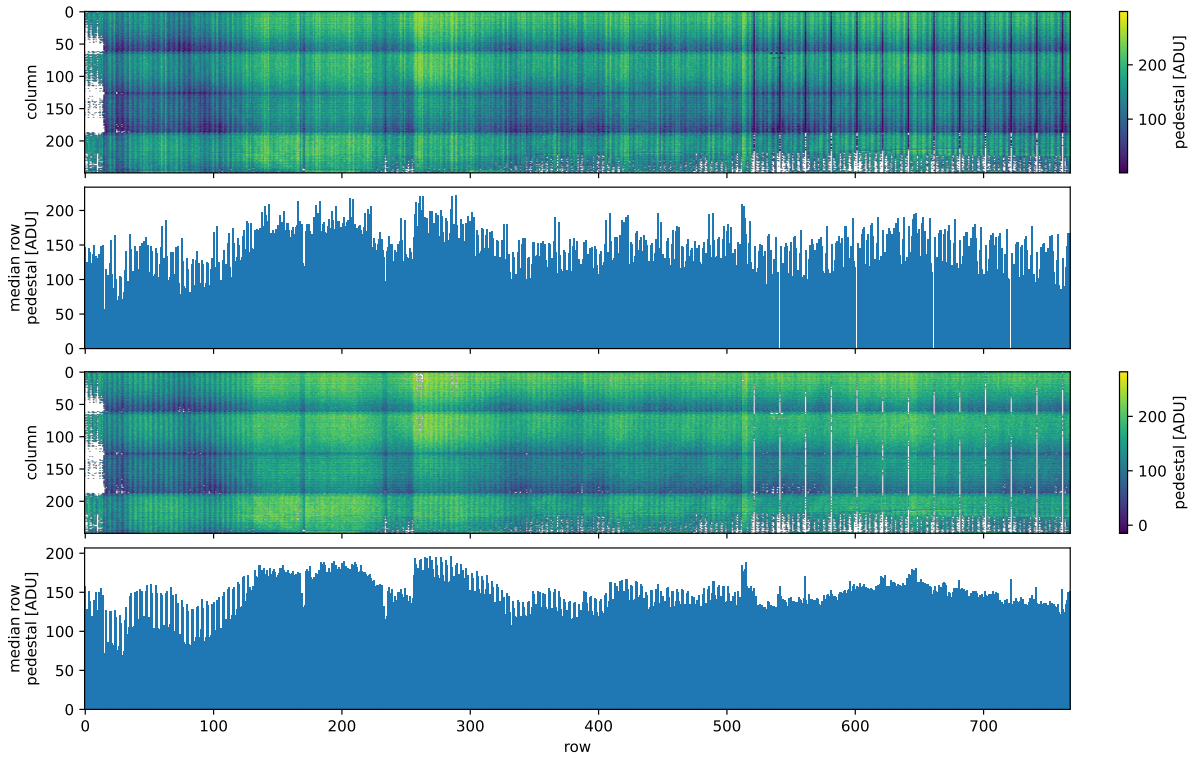


Figure 5.11: W46_OB1 pedestals corrected for X-ray inspection damage near the ASICs in the top two graphs and with additional periodic row correction in the bottom two graphs. The first and third graphs show the pedestal map. The color scale indicates the corrected pedestal values in ADU. White pixels have raw pedestals outside the dynamic range and are therefore not corrected. The second and fourth graphs show the mean row pedestal values to highlight the smoothing.

W($\geq$ 50) case is composed of 18 double rows plus one row. $36 \cdot 85\,\mu\text{m} = 3\,060\,\mu\text{m}$ is the length of the 18 double rows, and $2 \cdot 85\,\mu\text{m} - 30\,\mu\text{m} = 140\,\mu\text{m}$ is the gate-to-gate distance from uneven to even row numbers. This totals 3 200 µm, an exact multiple of the obtained second pattern "base frequency" of the "beat frequency" of 160 µm.

This is strong evidence for the gate being the affected structure. It can be assumed that the stitching changes the effective length of the gate and thereby modulates the drain currents as shown in Eq. (5.4). According to Table 5.4, the outliers have a deviation from the mean of roughly 60 to 120 ADU corresponding to $\Delta I_{\text{D,sat.}}$ of 6 to 12 µA. This translates to a gate-length variation

$$\frac{\Delta L}{L} = \frac{\Delta I_{\text{D,sat.}}}{I_{\text{D,sat.}} + \Delta I_{\text{D,sat.}}} \tag{5.5}$$

of 6 to 11 % with nominal PXD9 gate length of $L = 5\,\mu\text{m}$.

Modules		pitch [µm]	period n	R
W09_IF	W09_IB	55	40	0.77
W09_IF	W09_IB	60	10	0.95
W09_OF1	W09_OF2	70	20	0.96
W09_OF1	W09_OF2	85	40	0.96
W09_OB1	W09_OB2	70	20	0.99
W09_OB1	W09_OB2	85	40	0.93
W46_IF	W46_IB	55	40	0.40
W46_IF	W46_IB	60	10	0.99
W46_OF1	W46_OF2	70	20	0.98
W46_OF1	W46_OF2	85	40	0.95
W46_OB1	W46_OB2	70	20	0.97
W46_OB1	W46_OB2	85	40	0.79
W56_IF	W56_IB	55	32	0.78
W56_IF	W56_IB	60	16	0.75
W56_OF1	W56_OF2	70	32	0.98
W56_OF1	W56_OF2	85	64	0.95
W56_OB1	W56_OB2	70	32	0.92
W56_OB1	W56_OB2	85	64	0.97
W57_OF1	W57_OF2	70	32	0.97
W57_OF1	W57_OF2	85	64	0.88
W67_IF	W67_IB	55	32	0.80
W67_IF	W67_IB	60	16	0.91

Table 5.5: Correlation of periodic row deviations from mean between sensor pairs with same layout.

5.3 Double-row variations

Throughout all investigations of module properties ”double-row” patterns have been observed, as documented e.g. in [39, p. 86]. The expression ”double-row pattern” describes regular patterns of two consecutive pixel rows in this context. Figure 5.12 demonstrates an example for module W46_OB1.

The unit cell of the sensor layout is four pixel rows long. That means, every four rows the design repeats itself. Therefore, a periodic pattern with a length of four rows could arise from asymmetries between pixels in the layout.

First, the shape and severity of the four-row patterns is determined across entire sensors. To characterize the pattern, the sensor is divided into four-row blocks, called quad rows in the following (short for quadruple rows). Each quad row consists of four sub-rows:

$$\text{quad-row}_i = [\text{sub-row}_{i,j}] = [\text{row}_{4i}, \text{row}_{4i+1}, \text{row}_{4i+2}, \text{row}_{4i+3}] \quad \text{with} i \in [0..192], j \in [0..3] \tag{5.6}$$

The mean pedestal value of each block is subtracted from its sub-row pedestal values to extract their relative deviations:

$$\Delta I_{\text{sub-row}_{i,j}} = I_{\text{sub-row}_{i,j}} - \bar{I}_{\text{quad-row}_i} = I_{\text{sub-row}_{i,j}} - \frac{\sum_j^4 I_{\text{row}_{4i+j}}}{4} \quad . \tag{5.7}$$

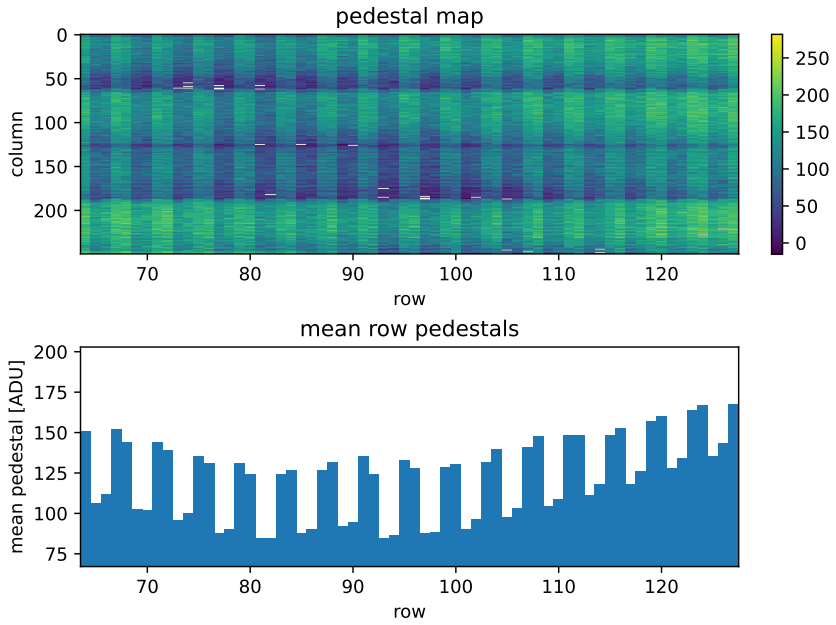


Figure 5.12: Pedestal map and row projection of section of W46_OB1 sensor after correction for x-ray damage and periodic row patterns. The representation is strongly skewed to highlight the *double-row* effect.

To work out recurring patterns several quad rows can be combined and the mean of their respective sub-rows taken. Figure 5.13 shows the row pattern of W46_OB1 after inspection damage and periodic row pattern corrections. Eight four-row unit-cell blocks are combined and shown below the corresponding region of the sensor. In the row region 0-127 (quad rows 0-31), a pattern emerges. The first sub-row shows an increased pedestal value, the second and third a decreased and the fourth row an increased value again. First and fourth, second and third row have similar values, respectively. This forms the described *double-row* pattern.

Interestingly, in rows 128-255 (quad-rows 32-63) the pattern appears to vanish. In rows 256-511 (quad-rows 64-127) the pattern emerges again with more or less constant magnitude, but inverted. Now the first and fourth sub-row's pedestals deviate negatively and second and third sub-row's values positively. The last third of the sensor, the 70 µm pixels in rows 512 and up, do not exhibit a pattern.

Since the analyzed pedestals here were already corrected for periodic row patters, see previous section, it has to be checked if those corrections contain sub-patterns with a length of four rows which interfere with the double-row pattern. To get an overview of the influence of the first correction and the behavior of other modules, Fig. 5.14 shows the sub-row deviation of all modules of wafer 46 and their respective periodic row correction patterns. Similarities can be made out between different modules. They all exhibit the double-row pattern. Near the EOS the deviations appear to be largest, always with the same *polarity*. Along the large pixels the magnitude of the pattern decreases. It mostly vanishes in quad-rows 32-63 for all layer-two modules and re-emerges with inverted polarity and increasing magnitude for quad-rows 64-127. The correction patterns do not show significant double-row patterns except in the short pixel region of the IB module and slight double-row patterns in the short pixel regions of the OF modules.

Since the double-row pattern is established uniformly in all modules and all areas a FOM can be

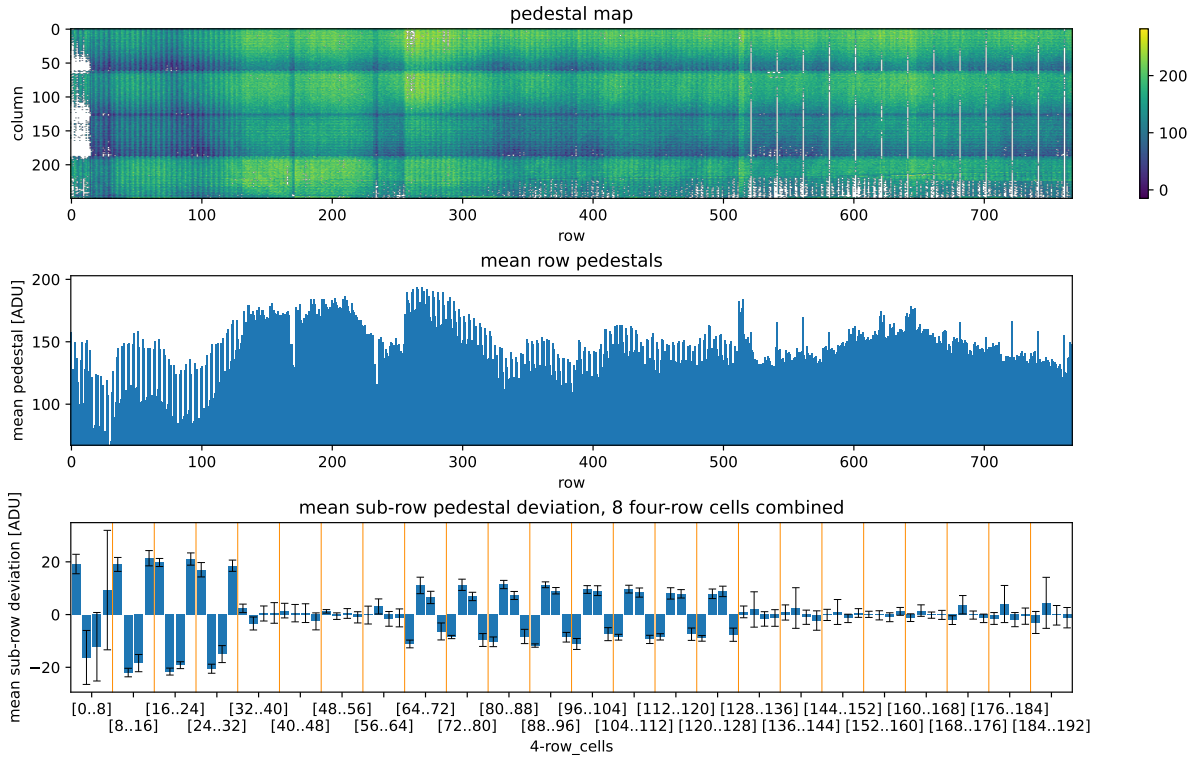


Figure 5.13: Pedestal map, row projection and folded four-row-blocks of W46_OB1 sensor after correction for x-ray damage and periodic row patterns. The top plot shows a map of the pedestals as a function of the pixel location on the sensor. The plot shows the mean row value of the pedestals and the bottom plot shows the mean value of eight consecutive folded four-rows. The black error bars correspond to the standard deviation.

introduced. The magnitude of the double-row pattern is:

$$\eta_{\text{double-row}}(\text{quad-row}_i) = \frac{\text{sub-row}_{i,0} + \text{sub-row}_{i,3}}{2} - \frac{\text{sub-row}_{i,1} + \text{sub-row}_{i,2}}{2} \tag{5.8}$$

Plotting this quantity in the same fashion as before, the evolution of the effect is easier to follow in this type of plot, as shown in Fig. 5.15. The trend of decreasing magnitude is clearly visible for all modules. The size of the effect appears to be very similar between same-type modules, i.e. OF1/2 show a −20 to 20 ADU magnitude, OB1/2 −20 to 30 ADU. IF and IB show the largest effects with 50 ADU and 100 ADU, respectively. They both do not show an inversion of polarity and IB also exhibits a large effect in the small sensor area as the only module, which is a component part of the correction in the right column. An important difference for W46_IB is that it is pre-irradiated. The shown measurement is a laboratory measurement after the module was used in Phase 2. Subsequently, it is also operated at adjusted $V_{\text{gate-on}}$ of −4 V. It was observed in laboratory X-ray irradiation experiments on PXD9 sensors that double-row patterns of increasing magnitude emerge. Therefore, W46_IB is a special case, adding evidence to the observation that radiation damage increases the magnitude of the double-row effect.

The same evaluation of the double-row magnitude was done for modules of wafers 9, 37, 56, 57 and 67 and can be found in Appendix A.2. The observations are very similar for wafers 9 and 46. Wafer 37 does not show large double-row variations. Wafers 56, 57 and 67 show the same gradient along the

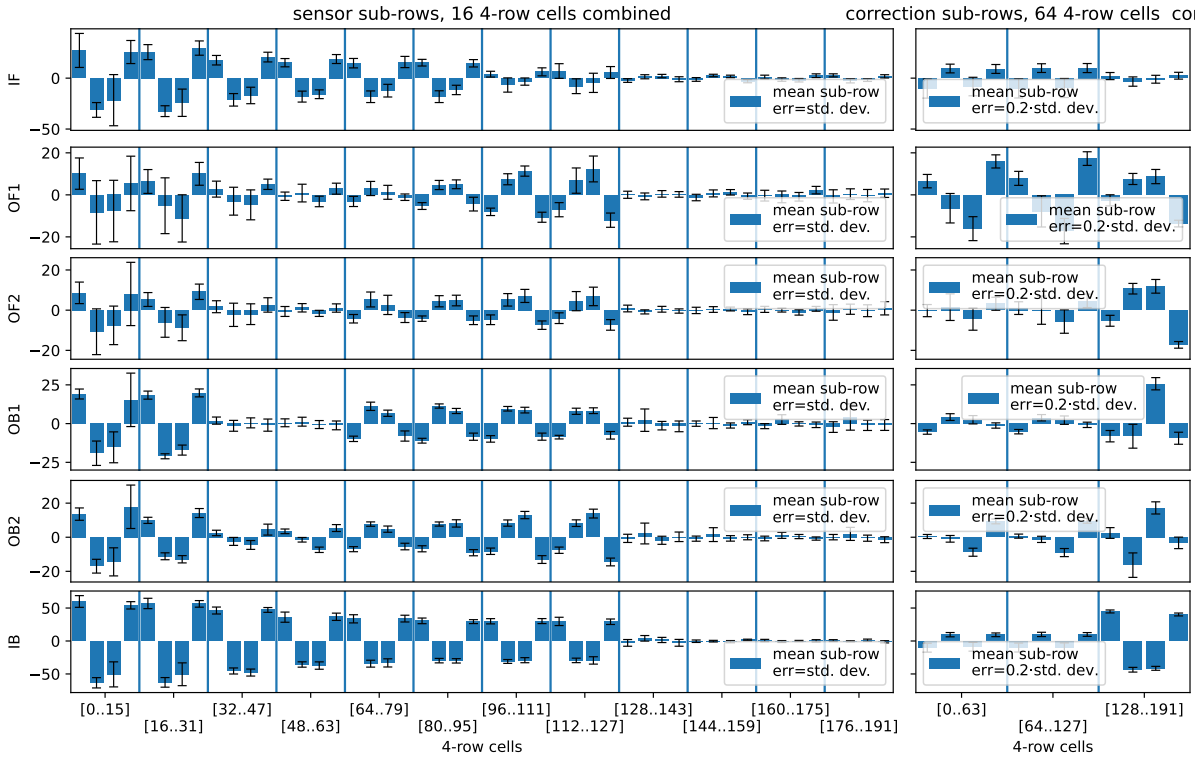


Figure 5.14: W46 mean sub-row deviations of consecutive quad-rows for all sensors. The left column shows results of the calculation for each sensor with 16 quad-rows combined after periodic-row correction was applied. The right column shows the same analysis for the applied correction pattern. The black error bars represent the standard deviation of the combined values. In the right correction pattern column the error bars denote only a fifth of the standard deviation to keep vertical plot limits small. Row 0 signifies the first row of the sensor's large pixel area, adjacent to the DCDs. Row 767 is the last row of the short pixel area at the far end of the module.

modules, but also large contributions of double-row patterns in the periodic row correction patterns. This might be a consequence of the different pattern periods compared to the lower numbered wafers.

In conclusion, the reason for this pattern is not understood, but it can be related to an existing asymmetry in the sensor design. The pixel layout is a double-pixel layout. Two pixels share a common source. But, as mentioned above, the unit-cell is four rows long. The reason for this are biasing lines for source, gate and drift. The source voltage is distributed in a grid, lines run parallel to the drain lines across the entire sensor. However, to prevent gradients in these long lines, perpendicular to these, i.e. parallel to the rows, additional source lines connect them to wide biasing lines at the sensor periphery. These lines parallel to the rows are placed at the edge of each unit cell, i.e. every four rows between two double-pixel rows. In the center of the unit cell, between the two double-pixel rows, run the gate line and the drift line. This means the drift implants are only connected between the double-pixel rows in the center of the unit cell. This could potentially introduce a difference in the drift potentials between every second double-row if there are currents flowing or couplings from the lines running on the surface. The size of the effect is shown to be in the range of

$$\eta_{\text{double-row}} = 20 \text{ to } 60 \,\text{ADU} = 2 \text{ to } 6 \,\mu\text{A} \tag{5.9}$$

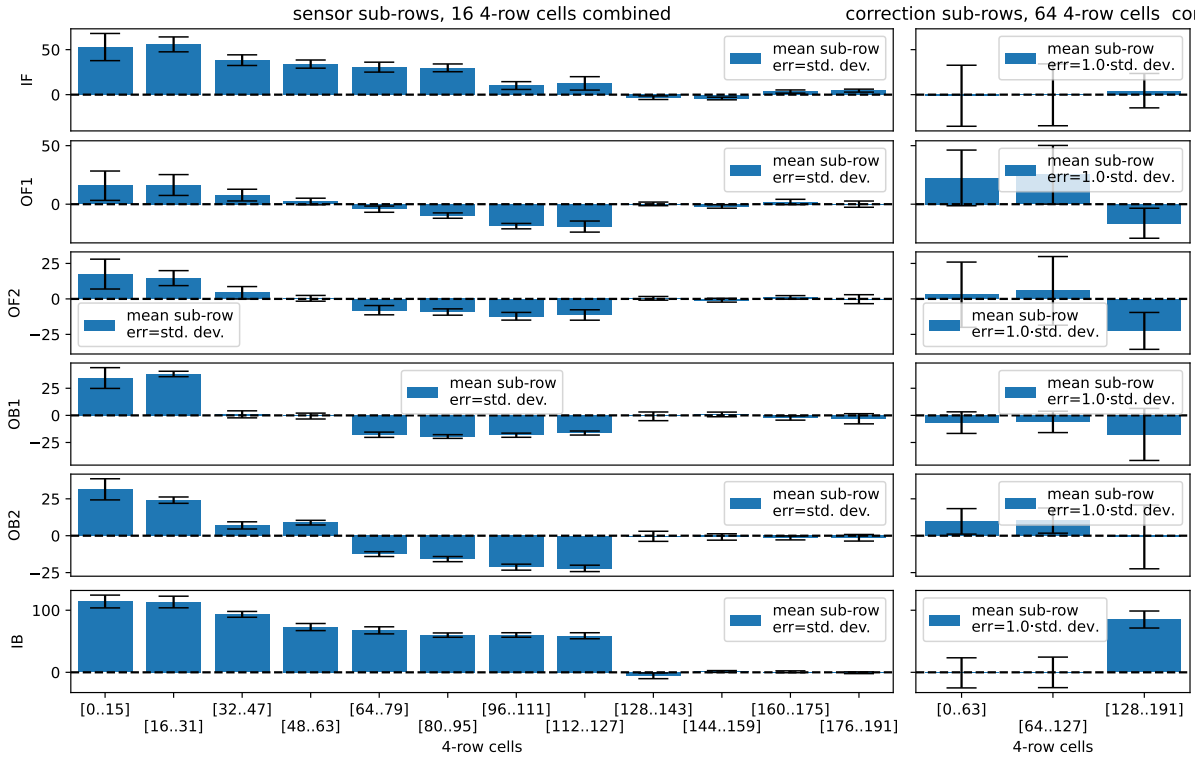


Figure 5.15: W46 double-row effect magnitude $\eta_{\text{double-row}}$ of consecutive quad-rows for all sensors. The left column shows results of the calculation for each sensor with 16 quad-rows combined after periodic-row correction was applied. The right column shows the same analysis for the applied correction pattern. The black error bars represent the standard deviation of the combined values. Row 0 signifies the first row of the sensor's large pixel area, adjacent to the DCDs. Row 767 is the last row of the short pixel area at the far end of the module.

for the examined modules.

5.4 DCD pedestal contributions

The maps of all modules' pedestals show clear contributions from the DCDs. Their effect manifests itself as a sawtooth pattern along the rows (column projection), as evident already in Fig. 5.1.

To evaluate the DCDs' effects it is instructive to look at their layout or module footprint, respectively, and their connection to the sensor drain lines. Figure 5.16 illustrates the location of the channels on the ASICs and their connection to the sensor drain lines . The channels of a single DCD are arranged in an almost quadratic 16×16 grid. Looking at their footprint as seen on the module, the DCD channels are numbered from bottom to top in columns and the columns increase from right to left. The DCDs themselves are counted from left to right. When assigning module channel numbers, the leftmost DCD therefore has channels 0-255, etc. The drain lines are connected in a simple fashion to the DCD channels from bottom to top and left to right. Because of their counter-directional numbering and connection some attention is needed to correctly correlate DCD channel properties to their geometry. Therefore, where applicable, geometrical channel property overviews are ordered according to their module footprint as shown in Fig. 5.16.

Figure 5.17 shows pedestal values of W46_OB1, their projection along sensor columns and mean pedestal values of the DCD channels arranged according to their module footprint. The aforementioned sawtooth pattern is apparent in the mean pedestals per sensor column. It describes a large scale pedestal variation of ~ 80 ADU along the sensor rows. The center plot of the figure shows the mean pedestals per drain line or DCD channel. The geometric representation reveals a prominent gradient across the DCD columns with a similar shape for each ASIC. This points to an effect originating in the DCD itself. Also the distance to switchers, on the right for W46_OB1, could be speculated to cause asymmetries in the sensor performance due to voltage drops or pulse deformation along the rows. Comparing to other modules in Fig. 5.18 shows the same shape of the effect independent of the switcher position (right side for OB/IF and left side for OF/IB). It can be concluded that the gradient is caused by properties of the DCDs. The variations could originate from offset or gain fluctuations of the amplifiers, ADCs or current sources. Since the DCDs define the drain voltages V_{D}, differences translate to different source-drain voltages V_{SD}. These in turn induce channel length modulations causing changes in the drain currents [40]:

$$I_{\mathrm{D,sat.}} = \mu C_{\mathrm{ox}} \frac{W}{2L} \left(V_{\mathrm{GS}} - V_{\mathrm{Th}}\right)^2 \cdot \left[1 + \lambda V_{\mathrm{SD}}\right] \quad , \tag{5.10}$$

with μ the charge carrier mobility, C_{ox} the oxide capacitance, W and L the gate width and length, respectively, V_{Th} the threshold voltage, and λ the channel-length modulation parameter.

Looking at the DCD channel pedestals in the left column of Fig. 5.18 common shapes can be seen. Generally, there appears to be a maximum plateau on the left side of the DCD and a falling slope on the right side. The width, shape and location of the maximum can vary. Additionally, the first column on the left of each DCD is significantly lower than the left-side plateau and presents a discontinuity in the otherwise smooth trend of the mean column pedestal values. Plots of mean DCD channel pedestals in module footprint representation and mean DCD column pedestals for modules of the remaining investigated wafers are found in Appendix A.3. A single exception can be found in module W37_OB1, shown in Fig. A.36. Here DCDs 3 and 4 display a slope in the opposite direction. This could potentially be due to the cooling situation as these data were taken inside the Belle II detector during Phase 2.

Table 5.6 and Fig. 5.19 summarize the DCD column pedestal variation for all examined sensors. The quoted magnitude corresponds to the difference between maximum and minimum mean DCD column pedestal values. On average, the first DCD exhibits the strongest gradient, followed by the middle two

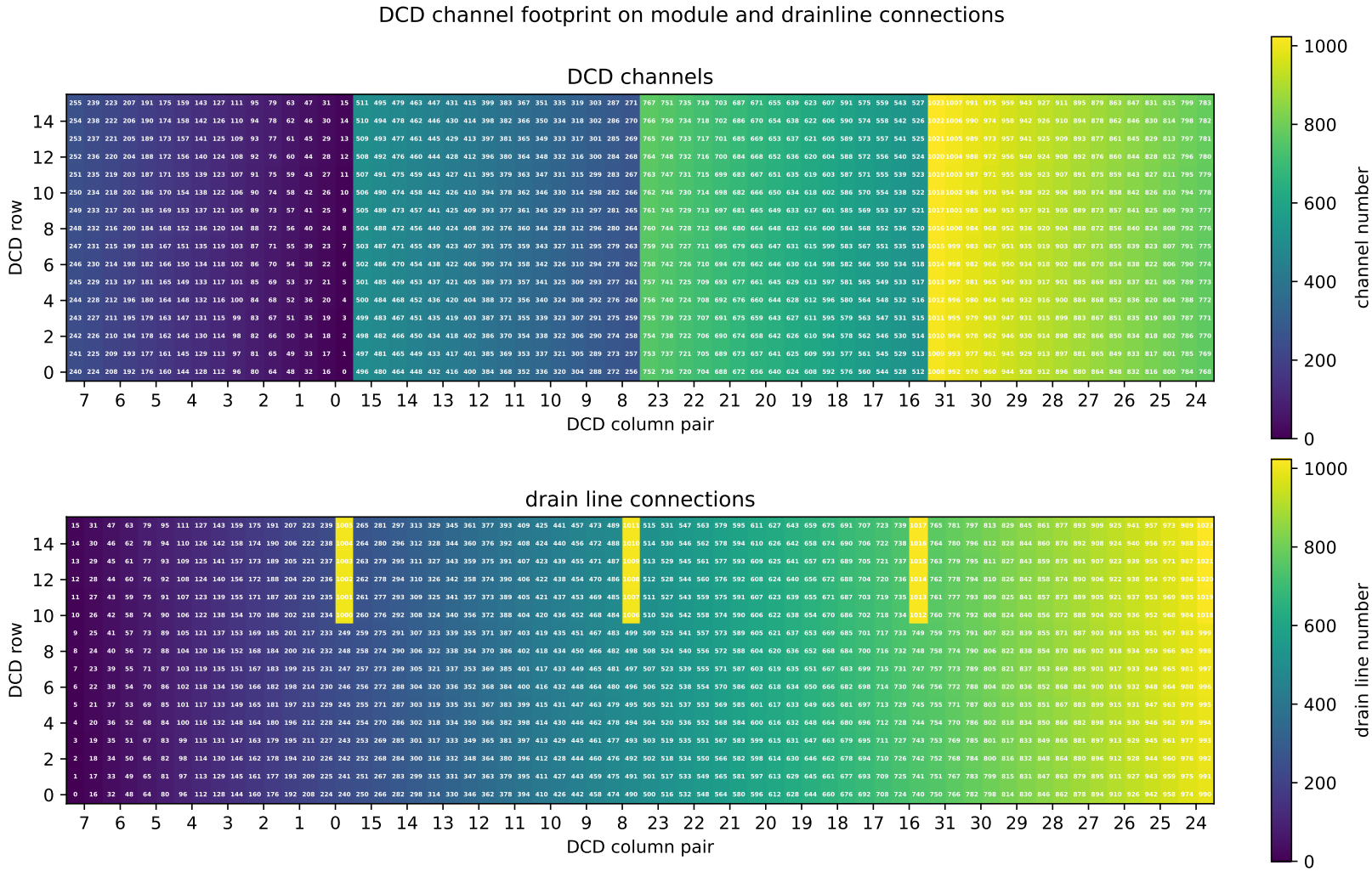


Figure 5.16: Schematic footprints of DCDs on the PXD9 module as seen from the top (looking at the ASICs) and the EOS towards the bottom. Drain lines are numbered 0-1000 from left to right. DCD channel numbers are shown on the top. Connected drain line numbers are shown on the bottom. The 24 non-existent drain lines 1000-1024 are assigned to the not-connected DCD channels 10-15, 266-271, 522-527, and 778-783.

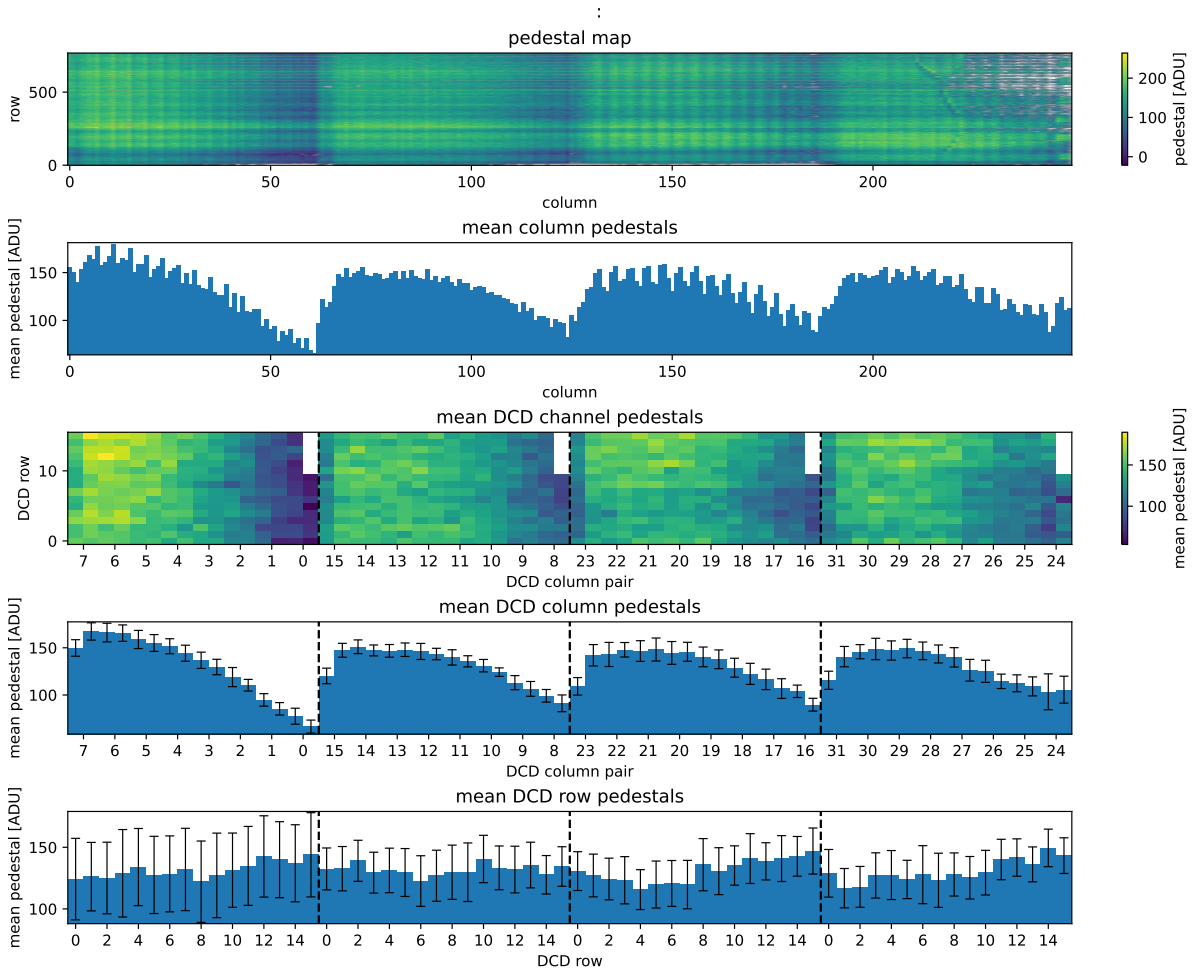


Figure 5.17: Mean column and DCD channel/drain line pedestal values of W46_OB1 after x-ray inspection damage, periodic row pattern and double-row effect corrections. The mean values of each DCD region were adjusted to 128 ADU. The first plot shows a map of pedestals as a function of their position on the sensor as viewed from the top with DCDs on the bottom and switchers to the right. The color code denotes the pedestal values in ADU. The second plot shows the mean pedestal values along the sensor columns. The third plot shows the mean pedestal values of each drain line/DCD channel arranged according to the module location of the channel. Below, in plot four, the mean pedestal value of each DCD column is given. The black error bars represent the standard deviation. The bottom plot shows the mean DCD row pedestals and their standard deviation.

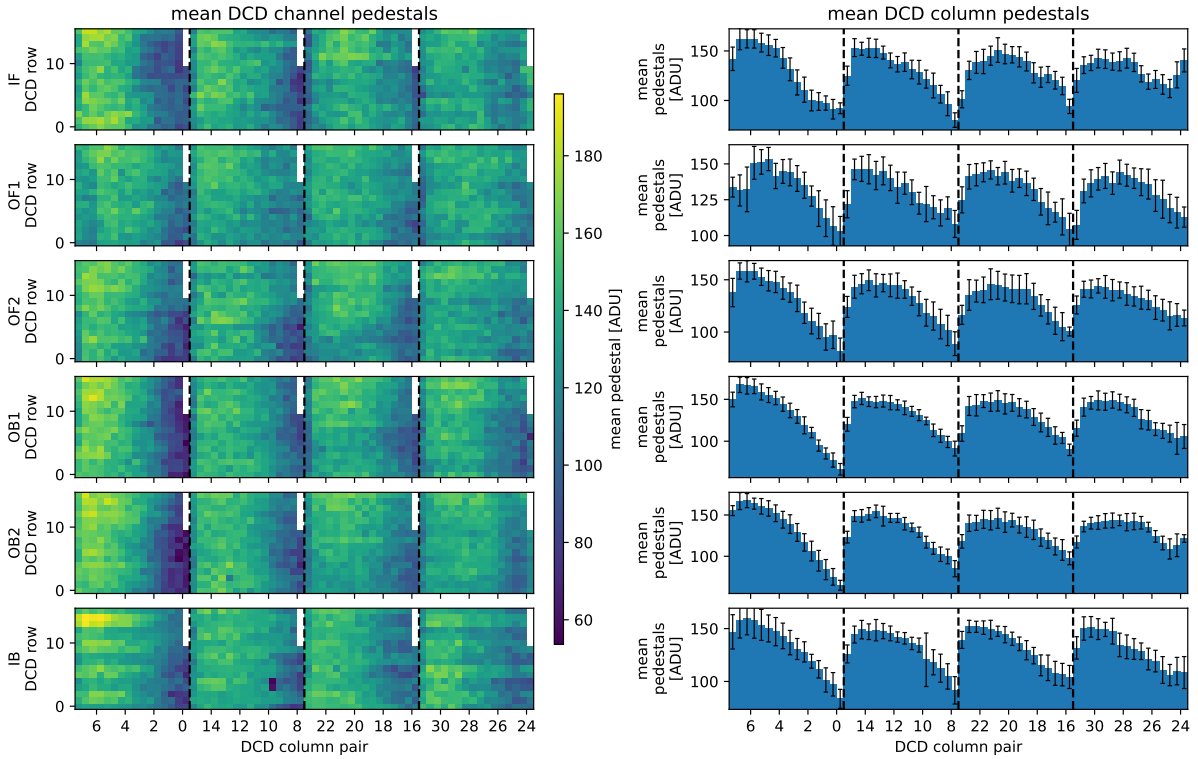


Figure 5.18: Mean pedestals of DCD channels of wafer 46 and mean DCD column pedestals. The left column shows the mean DCD channel pedestals arranged according to their location on the module for each module. The right column shows the mean DCD column pedestals. The black error bars correspond to the standard deviation.

DCDs 2 and 3. DCD 4 has the lowest variation.

Correcting for these clearly DCD-dependent large gradients smoothens the pedestal distributions across the columns significantly. Still there appear to be periodic contributions as visible in Fig. 5.20. Due to not-connected channels 10-16, the rightmost column of each DCD is corrected to match the mean value of DCD channel-rows 0-9, respectively.

wafer/sensor	DCD column pedestal variation [ADU]			
	DCD 1	DCD 2	DCD 3	DCD 4
W09 IF	25 ± 6	8 ± 5	29 ± 9	45 ± 8
OF1	70 ± 10	49 ± 9	26 ± 11	30 ± 11
OF2	53 ± 12	64 ± 11	30 ± 10	29 ± 16
OB1	95 ± 11	47 ± 11	41 ± 9	51 ± 11
OB2	92 ± 9	41 ± 9	41 ± 9	34 ± 9
IB	48 ± 11	31 ± 15	35 ± 16	21 ± 14
W37 IF	79 ± 12	66 ± 16	49 ± 14	22 ± 11
OF1	37 ± 12	26 ± 14	42 ± 17	51 ± 15
OB1	69 ± 9	40 ± 15	76 ± 13	41 ± 12
W46 IF	71 ± 15	73 ± 12	57 ± 14	31 ± 14
OF1	51 ± 13	38 ± 13	42 ± 13	37 ± 13
OF2	77 ± 15	61 ± 15	45 ± 15	31 ± 10
OB1	101 ± 11	60 ± 11	58 ± 14	46 ± 21
OB2	103 ± 10	69 ± 12	49 ± 14	35 ± 14
IB	76 ± 18	57 ± 16	48 ± 12	46 ± 14
W56 IF	86 ± 11	39 ± 10	40 ± 8	40 ± 15
OF1	51 ± 12	52 ± 11	50 ± 11	35 ± 14
OF2	61 ± 11	64 ± 11	51 ± 13	33 ± 12
OB1	90 ± 12	45 ± 11	42 ± 16	38 ± 16
OB2	107 ± 10	49 ± 16	38 ± 16	25 ± 22
IB	111 ± 14	71 ± 14	48 ± 13	47 ± 16
W57 OF1	97 ± 11	59 ± 12	53 ± 12	45 ± 9
OF2	120 ± 12	100 ± 15	86 ± 14	57 ± 13
OB1	106 ± 13	48 ± 14	32 ± 14	39 ± 27
IB	76 ± 15	53 ± 15	62 ± 15	28 ± 20
W67 IF	63 ± 15	45 ± 18	39 ± 15	36 ± 17
IB	47 ± 14	42 ± 12	30 ± 13	30 ± 12

Table 5.6: DCD column pedestal variation for examined modules determined by difference of maximum and minimum values.

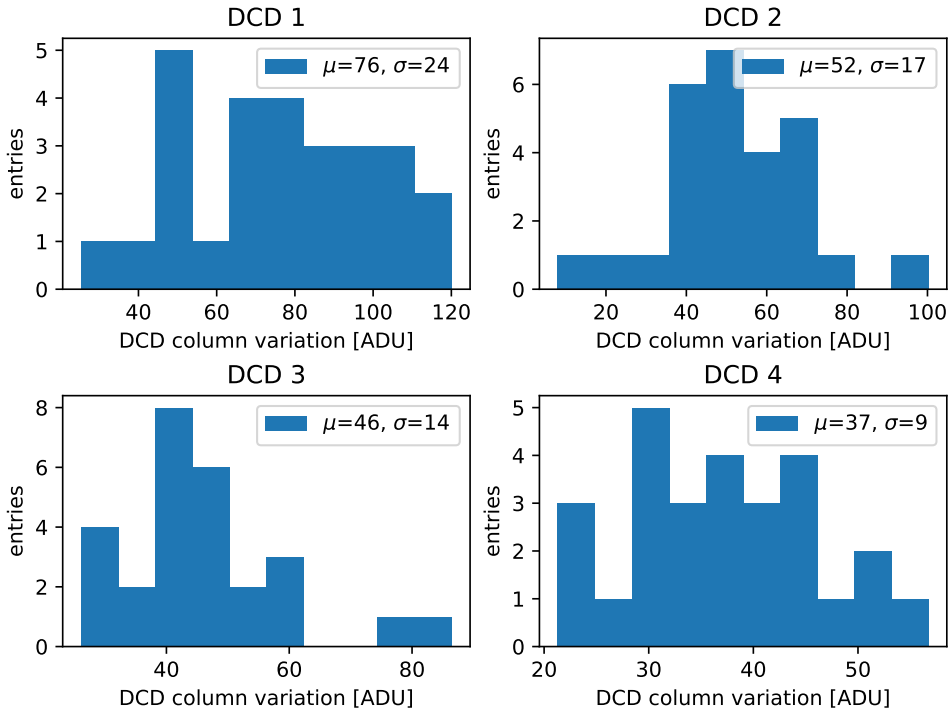


Figure 5.19: Histograms of column pedestal variation for all examined modules.

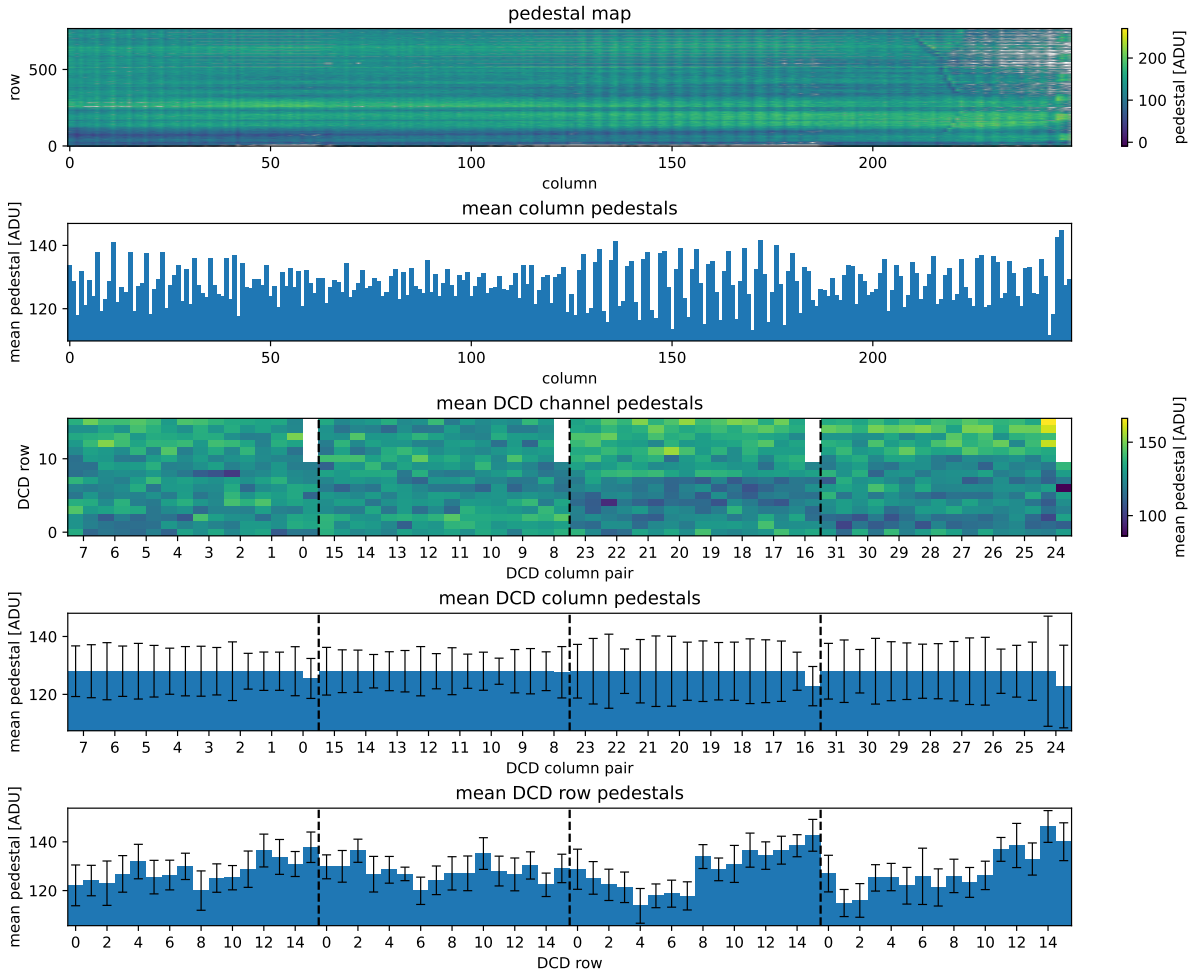


Figure 5.20: Mean column and DCD channel/drain line pedestal values of W46_OB1 after X-ray inspection damage, periodic row pattern, double-row effect and DCD channel column corrections. The mean values of each DCD region were adjusted to 128 ADU. The first plot shows a map of pedestals as a function of their position on the sensor as viewed from the top with DCDs on the bottom and switchers to the right. The color code denotes the pedestal values in ADU. The second plot shows the mean pedestal values along the sensor columns. The third plot shows the mean pedestal values of each drain line/DCD channel arranged according to the module location of the channel. In the fourth plot, the mean pedestal value of each DCD column is given. The black error bars represent the standard deviation. The bottom plot shows the mean DCD row pedestals and their standard deviation.

5.5 Sensor column and drain line asymmetry

As seen in Fig. 5.20, regular patterns are present in the pedestals averaged along the sensor pixel columns, even after DCD mean column pedestal correction. The pattern evidently also changes depending on the DCD region, which points to a contribution from the remaining DCD row inhomogeneities as seen in the lowest panel of Fig. 5.20.

Checking module W46_OB1 for repeating patterns in the mean pixel-column pedestals, as described already in Section 5.2 for the pixel-rows, the resulting auto-correlation pattern is shown in Fig. 5.21. There are spikes present for correlations with even numbered repetition periods. Figure 5.22 demonstrates the mean sensor pixel-column pedestals subdivided into stacks of n and the mean values of the corresponding sub-columns. The influence of the DCDs is clearly visible here, especially the third DCD appears to introduce a pattern with larger deviations between the columns. From the figure a periodicity of four appears to result in the most prominent mean sub-column pedestal value deviations. But looking at the OB1 modules from all examined wafers divided into stacks for four sub-rows in Fig. 5.23, it seems that an even-odd column pattern is visible. Calculating the difference of the mean pedestals of all even/odd pixel columns $\bar{I}_{\text{col, even}} - \bar{I}_{\text{col, odd}}$ for all examined sensors a pattern emerges, presented in Fig. 5.24. All modules exhibit an even-odd pixel-column pedestal asymmetry, wafer 46 one that is smaller than those of other wafers. Since all pixels are 50 µm wide, a double-column pattern would correspond to a physical structure of 100 µm. IF, OB and IB modules all have increased pedestals in odd columns, while the pedestals of OF modules have increased even columns. As a reminder, columns are all counted starting at the left edge of DCD 1 in these considerations. Since on the wafer, IF, OB and IB modules have the DCDs on the left side, their columns are counted in the same directions. All sensors are exact multiples of 100 µm apart in y-direction, therefore a 2-column wide pattern could be expected to continue across sensors. The OF modules have the DCDs on the right side of the wafer, therefore switching even and odd numbered columns with respect to the other modules in this representation, explaining their switched even/odd ratio.

As each sensor column is read out by four DCD channels, but only 250 drain lines are connected to each DCD, the column-to-channel pattern shifts in each DCD on the module as shown in Fig. 5.25 (compare also Fig. 5.16).

In addition to the mean column pedestals also the DCD channel level substructures can be studied. For this purpose the mean pedestals of each drain line, i.e. all 192 pixels connected to the same DCD channel, are studied. Figure 5.26 shows the auto-correlation of drain lines for different periods n of module W46_OB1. Clear correlations can be seen at multiples of eight drain lines , corresponding to two columns. Figure 5.27 shows the stacks of sub-lines for different periods n and the mean sub-line pedestals. A drain line substructure is apparent. Because of the shift between drain-line and DCD channel periodicities between DCDs (see Fig. 5.25) this pattern of eight is unlikely to arise from regular DCD properties. Instead, it must be intrinsic to the sensor. Figure 5.28 shows the mean drain-line auto-correlation for all examined sensors and for all the same period of eight becomes apparent. Figure 5.29 shows the mean sub-drain-line patterns for eightfold pattern repetition in all examined wafers and sensors as well as the correlation between sensors on the same wafer in the rightmost column and same-type sensors across wafers in the bottom row. The pattern is generally strongly correlated between the same sensors on different wafers pointing to reproducible properties of the layout/production process. The two OB modules, OB1 and OB2, on the same wafer always show strongly correlated patterns. The same is true for the OF1 and OF2 pairs on each wafer. Also, correlations between the patterns of IF, IB, and OB on the same wafer are detectable, particularly strong for wafers 56 and 57. This coincides with

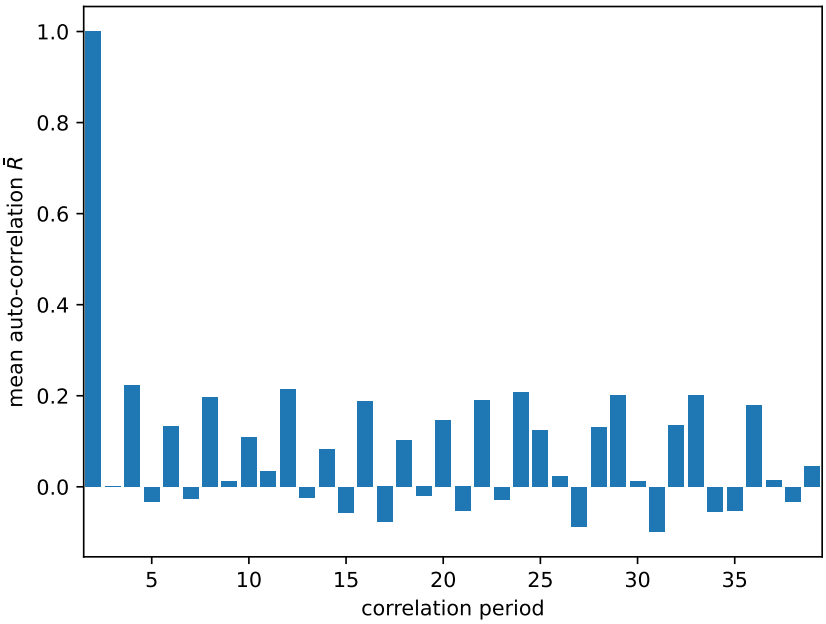


Figure 5.21: W46_OB1 auto-correlation of sensor pixel-column pedestals.

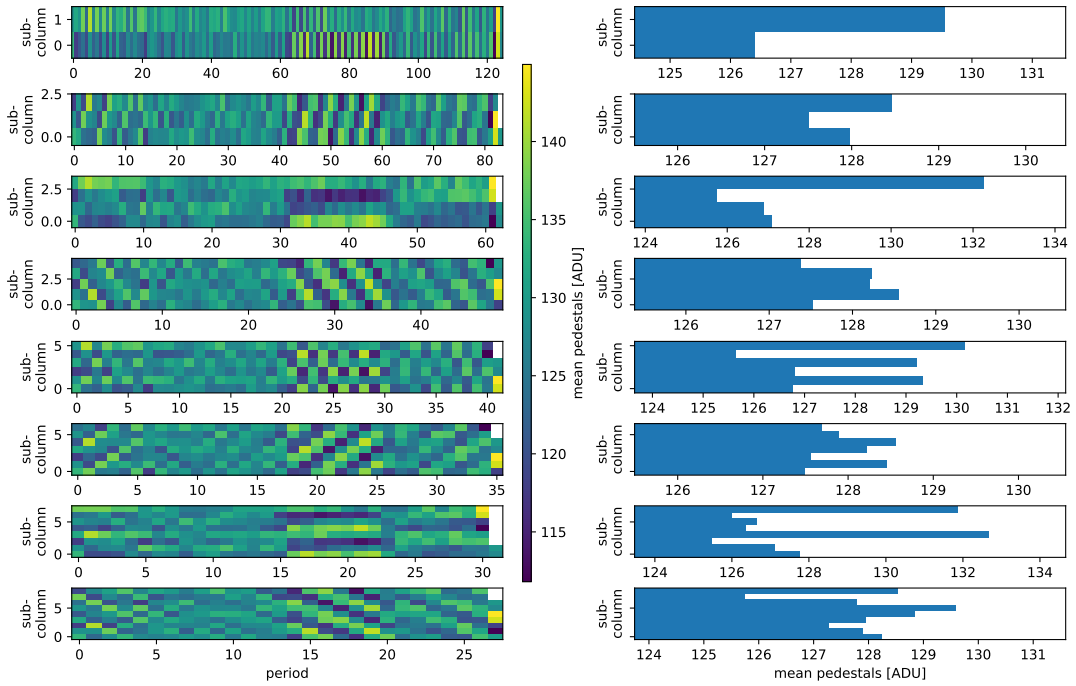


Figure 5.22: W46_OB1 mean pixel-column pedestals divided into stacks of different lengths. The left column shows the mean pixel-column pedestals and the right the mean value of the sub-columns.

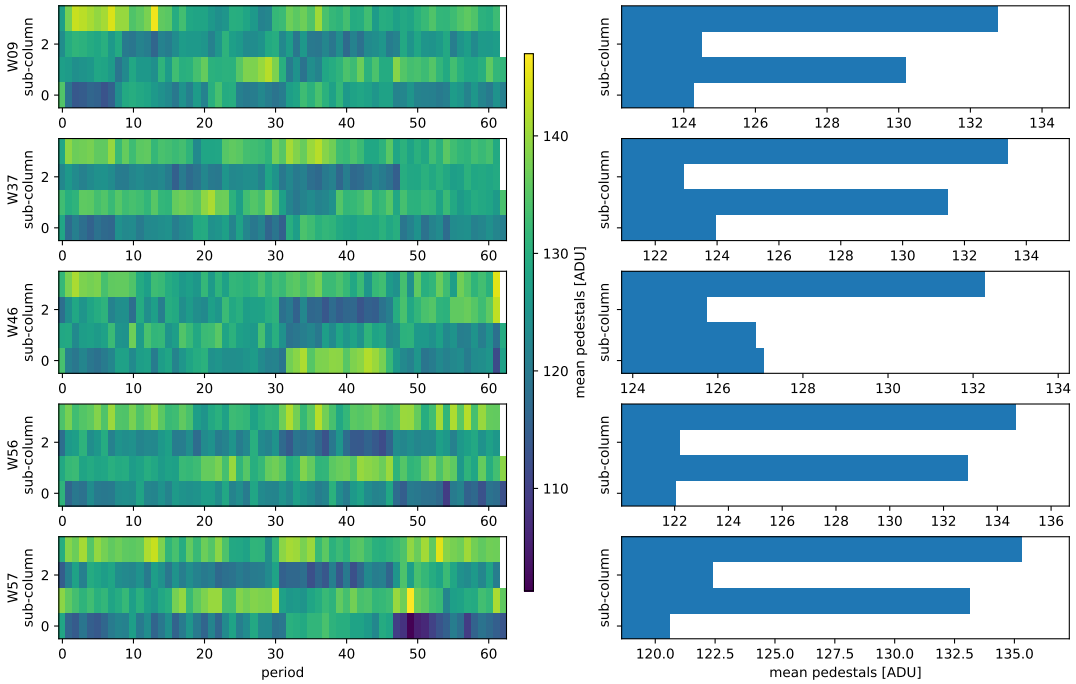


Figure 5.23: Mean pixel-column pedestals divided into stacks of different lengths for all modules of wafer 46. The left column shows the mean pixel-column pedestals and the right the mean value of the sub-columns.

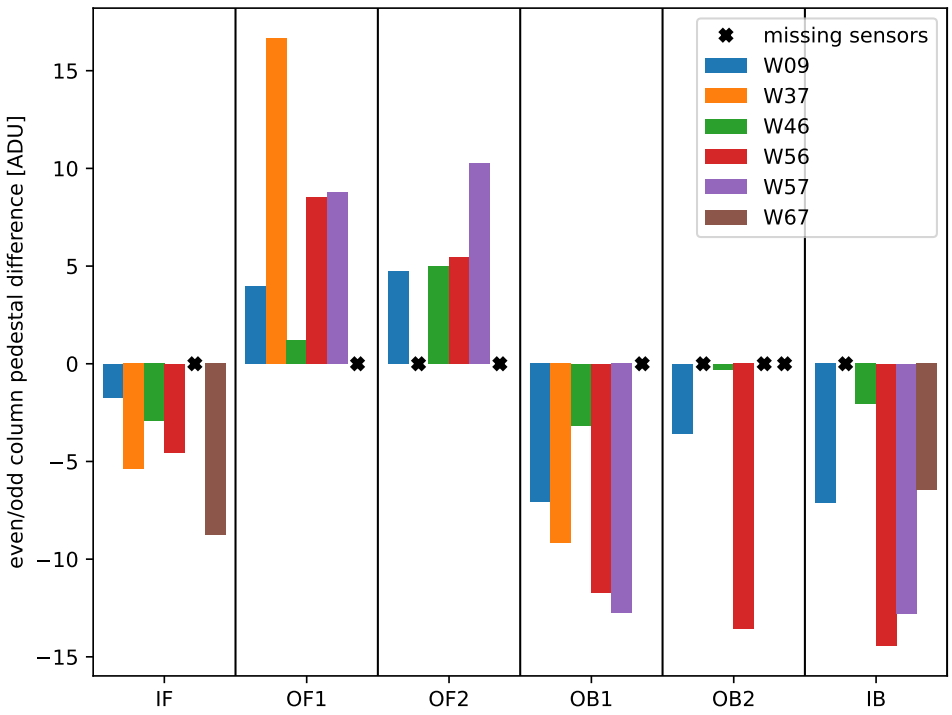


Figure 5.24: Even-odd pixel-column pedestal asymmetry for all examined modules.

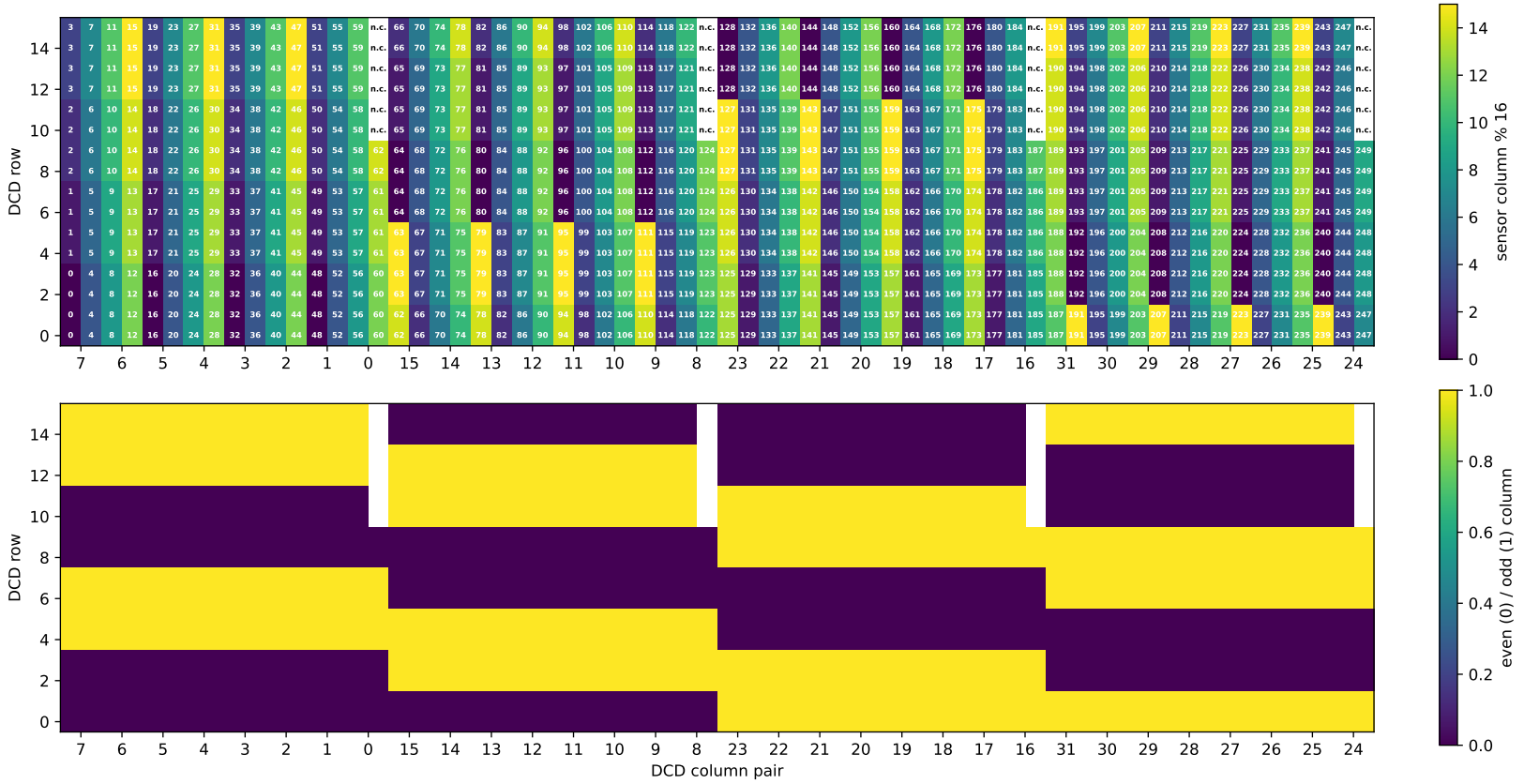


Figure 5.25: Column-to-DCD channel connection on the schematic module DCD floor plan. The top plot shows the sensor pixel-column number for each DCD channel and marks 16 successive sensor pixel-columns with a repeating color pattern. The bottom plot marks the locations of even (dark) and odd (light) pixel-columns on the DCD footprint.

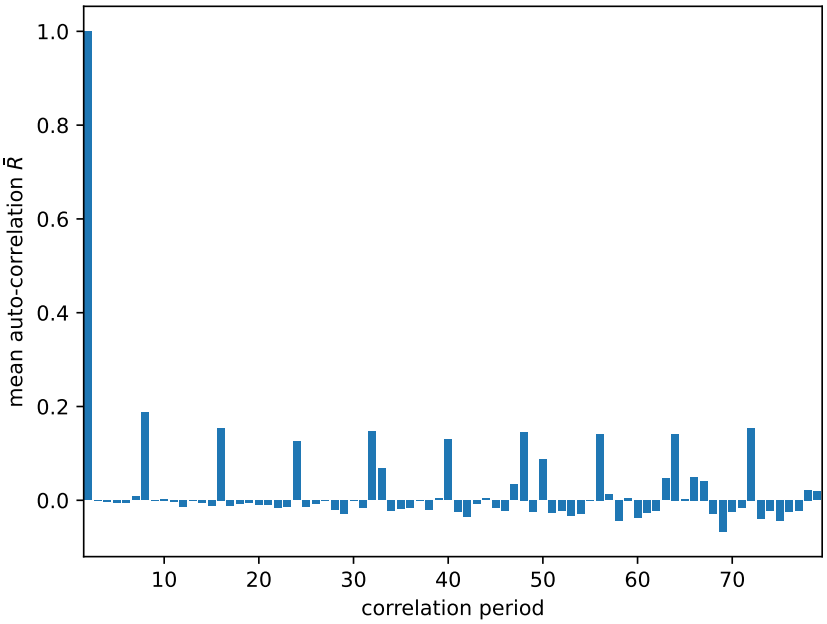


Figure 5.26: Auto-correlation of W46_OB1 drain-line mean pedestals for different correlation lengths.

their correlated even/odd pixel-column pedestal differences as shown above. The same is true for their anti-correlation with the OF modules.

Figure 5.30 and Fig. 5.31 show the effect of correcting for the determined periodic drain line patterns in W46_OB1 and W57_OB1, respectively. In accordance with the even-odd pixel-column pedestal difference shown in Fig. 5.24, the corrective effect on the column pedestal variation is not large for W46_OB1. For W57_OB1 the effect is larger. The main observed effect is a smoothing of the DCD mean row pedestal distribution.

The size of the drain-line pattern correction is given as the average deviation per drain line:

$$\Delta_{\text{drain line}} = \frac{\sum_i^8 \Delta_{\text{sub-line, i}}}{8} \quad . \tag{5.11}$$

Its distribution is shown in Fig. 5.32

In conclusion, a significant even-odd pixel-column asymmetry and related consistent eight-drain-line periodic patterns are present in all sensors with varying strength between wafers. The effects appear to be smaller in wafers 9 and 46 and larger in wafers 37, 56, 57 and 67. A difference in production for wafers < 50 and wafers ≥ 50 might cause this change in magnitude. The measurements of wafer 37 were performed inside the Belle II experiment and therefore under different environmental conditions. The more pronounced effect in this wafer could point to a temperature dependence.

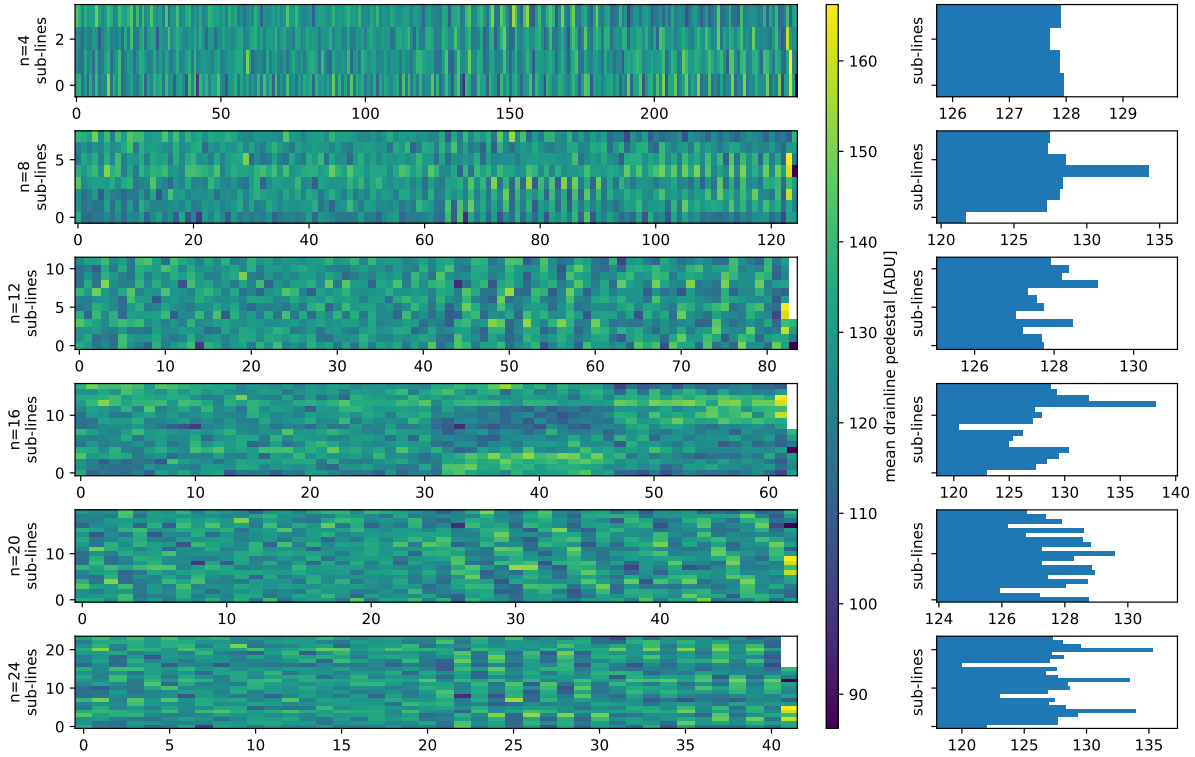


Figure 5.27: W46_OB1 mean drain-line pedestals divided into stacks of different length. The left column shows the mean drain-lin pedestals and the right the mean value of the sub-lines.

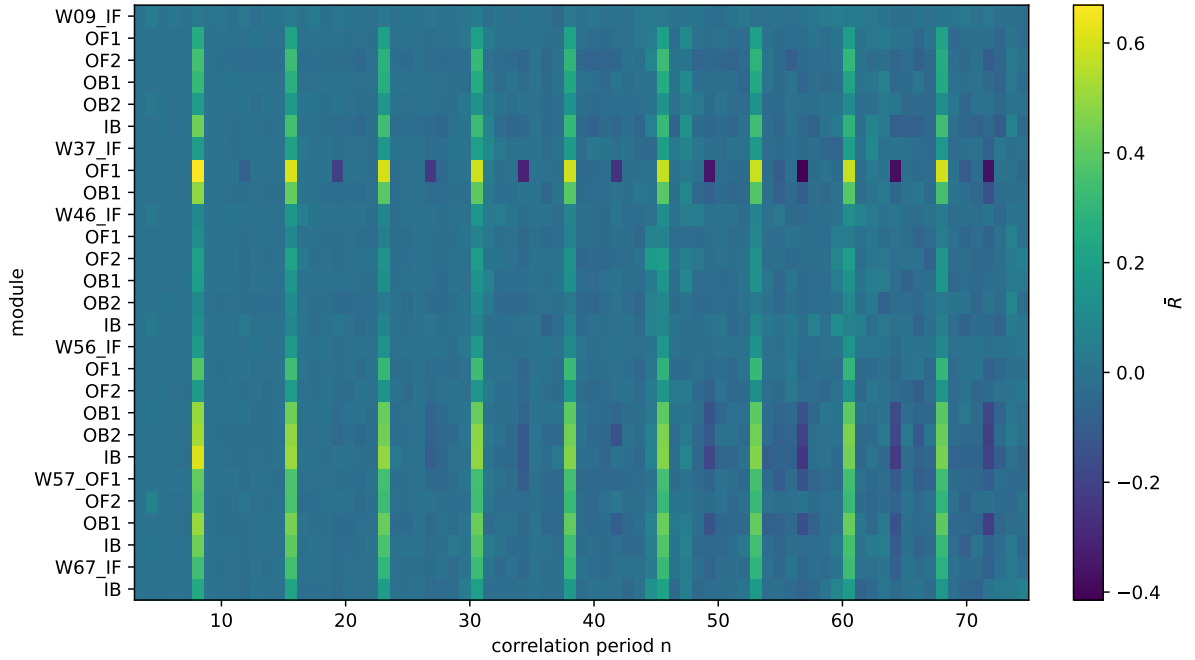


Figure 5.28: Drain-line auto-correlation for all examined modules.

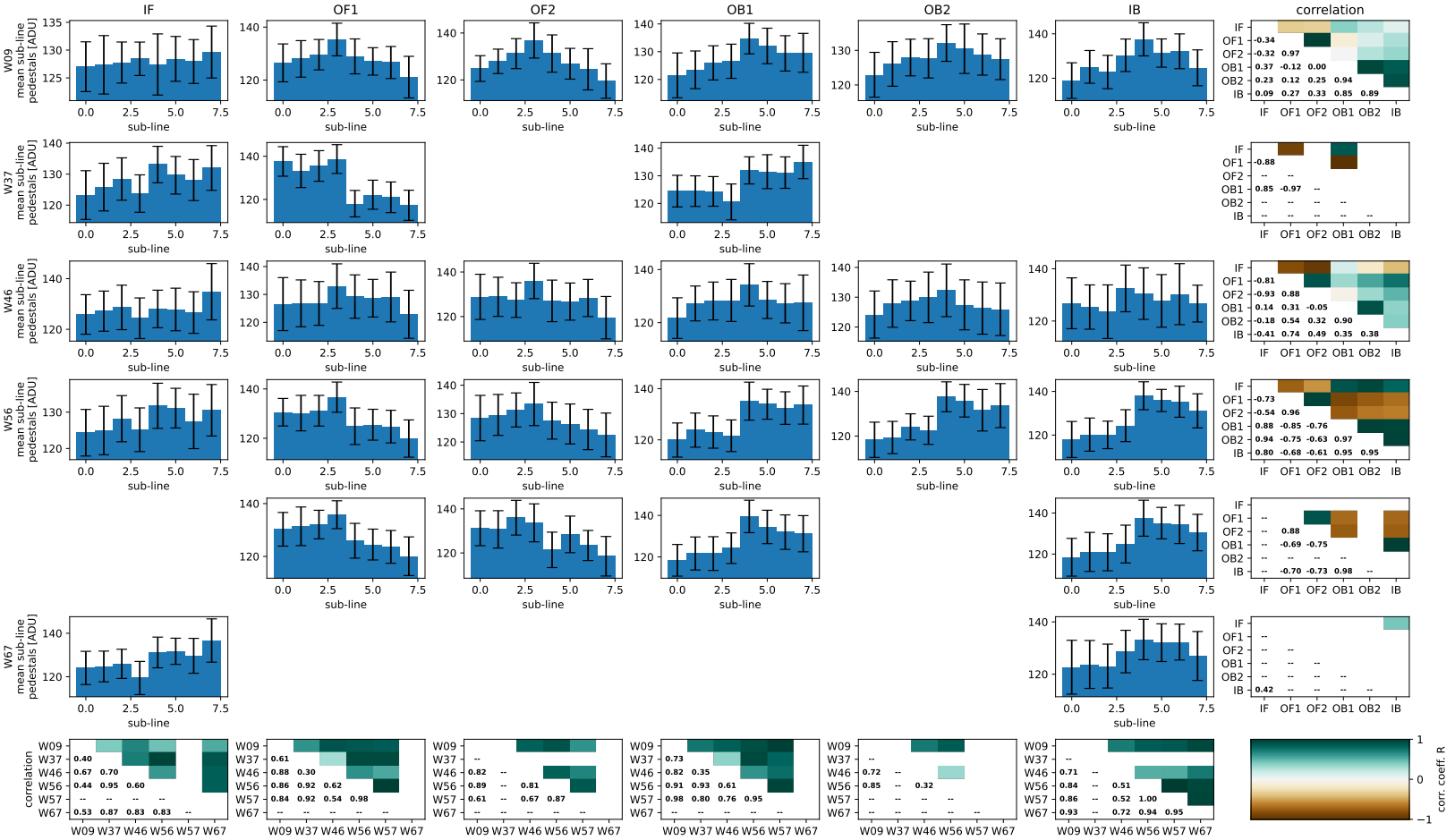


Figure 5.29: Mean of repeating drain line pattern of length eight for all examined modules. The last column shows the correlation between different modules of the same wafer. The last row shows the correlation of the same module types between different wafers.

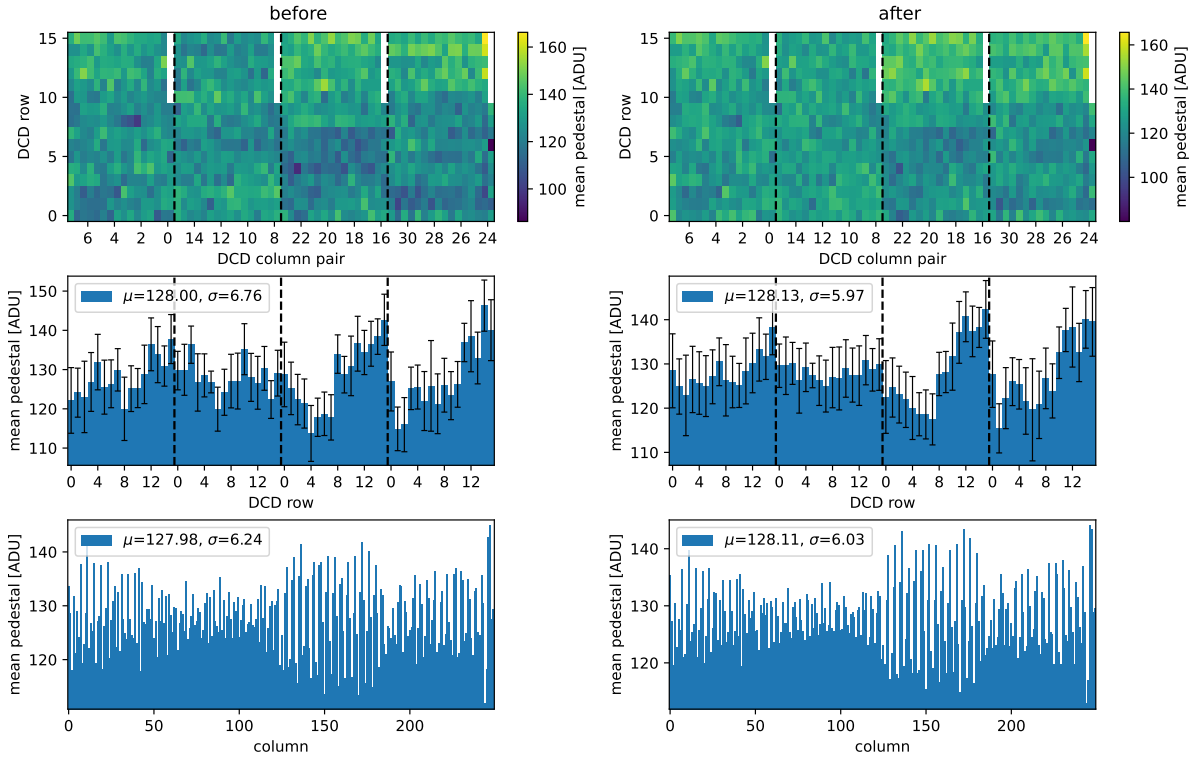


Figure 5.30: W46_OB1 mean DCD channel pedestals, mean DCD row pedestals and mean sensor column pedestals before and after the correction of the drain line octet variation. X-ray damage, sensor row pattern and DCD column variation corrections have been applied before.

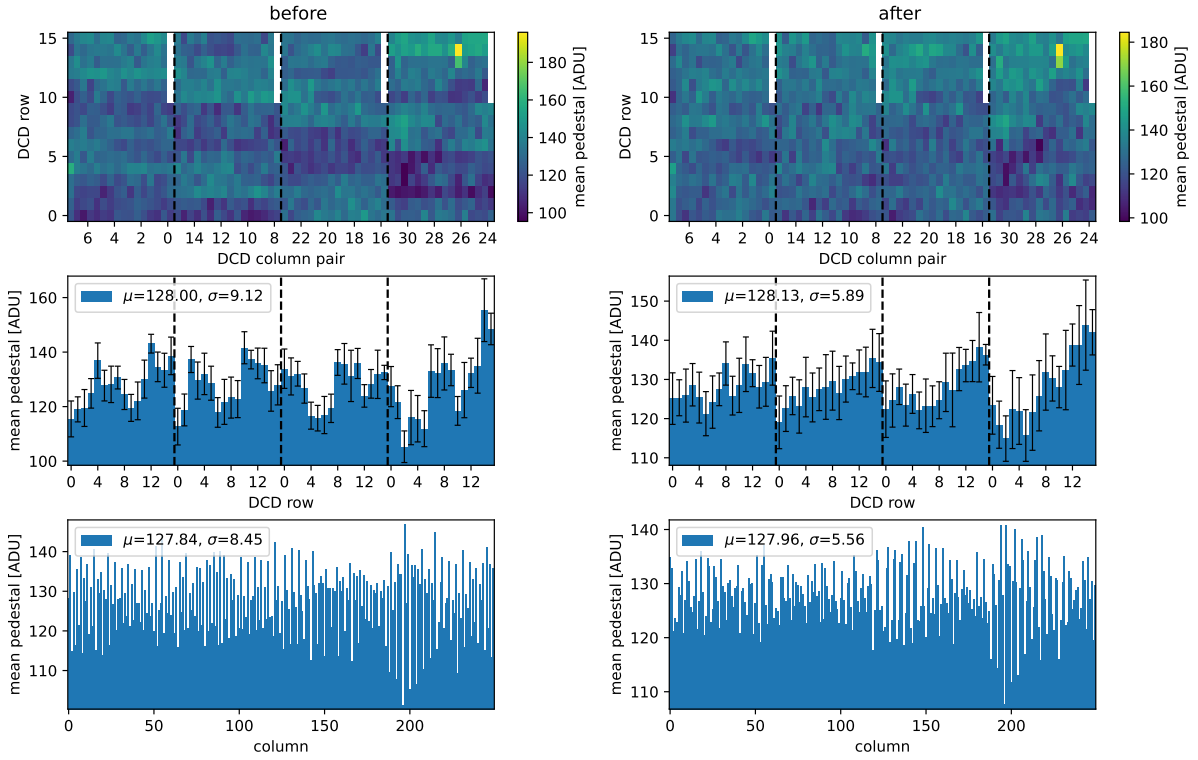


Figure 5.31: W57_OB1 mean DCD channel pedestals, mean DCD row pedestals and mean sensor column pedestals before and after the correction of the drain line octet pattern. X-ray damage, sensor row pattern and DCD column variation corrections have been applied before.

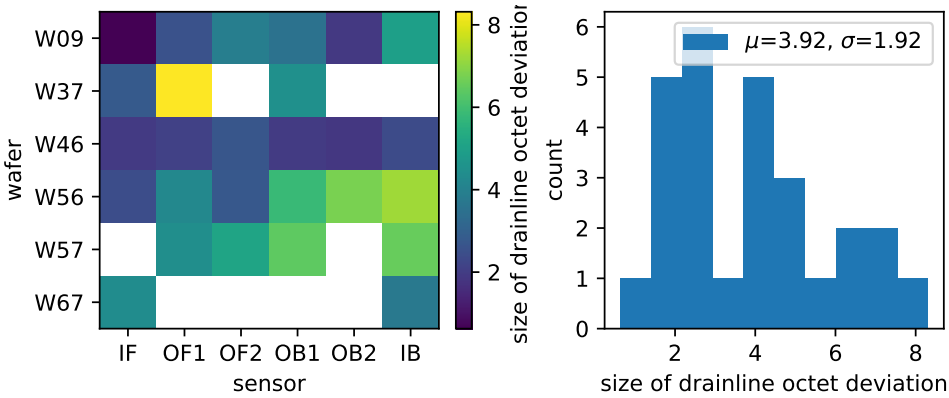


Figure 5.32: Size of drain-line octet variation for all examined modules as a 2D color coded map (left) and histogrammed (right).

5.6 DCD row pedestal variations

Finally, there are variations across the DCD rows. Figure 5.33 shows the mean DCD channel and row pedestals as well as the mean sensor pixel-column pedestals for W46_OB1 before and after correction for the DCD row variations. Figure 5.34 summarizes the mean sensor pixel-column and DCD channel pedestals in histograms before and after the DCD row correction. The standard distribution of the mean column pedestals decreases from 6.0 ADU to 3.4 ADU. A smoothing of the variation across the columns is clearly visible. For the mean DCD channel pedestals it decreases from 8.8 ADU to 6.5 ADU, their distribution looks homogeneous.

The first DCD of W46_OB1 shows a small slope in the mean row pedestals with increasing rows. The distribution of the second is almost flat to start with. DCDs three and four exhibit stronger fluctuations and a strong increase towards the higher numbered rows.

To get an overview of the size of the fluctuations, Figs. 5.35 and 5.36 show histograms of the span of the variation per DCD, i.e. the difference of maximum and minimum deviation, separately for each DCD number and summarized for all DCDs. No significant difference is found between the four DCDs on a module. Figures 5.37 and 5.38 histogram the deviations per row for all DCDs. On average a significant slope is visible. From Fig. 5.35 an average size of the row variation of 16 ADU can be derived. Table 5.7 summarizes the size of the DCD row pedestal variation for all examined modules.

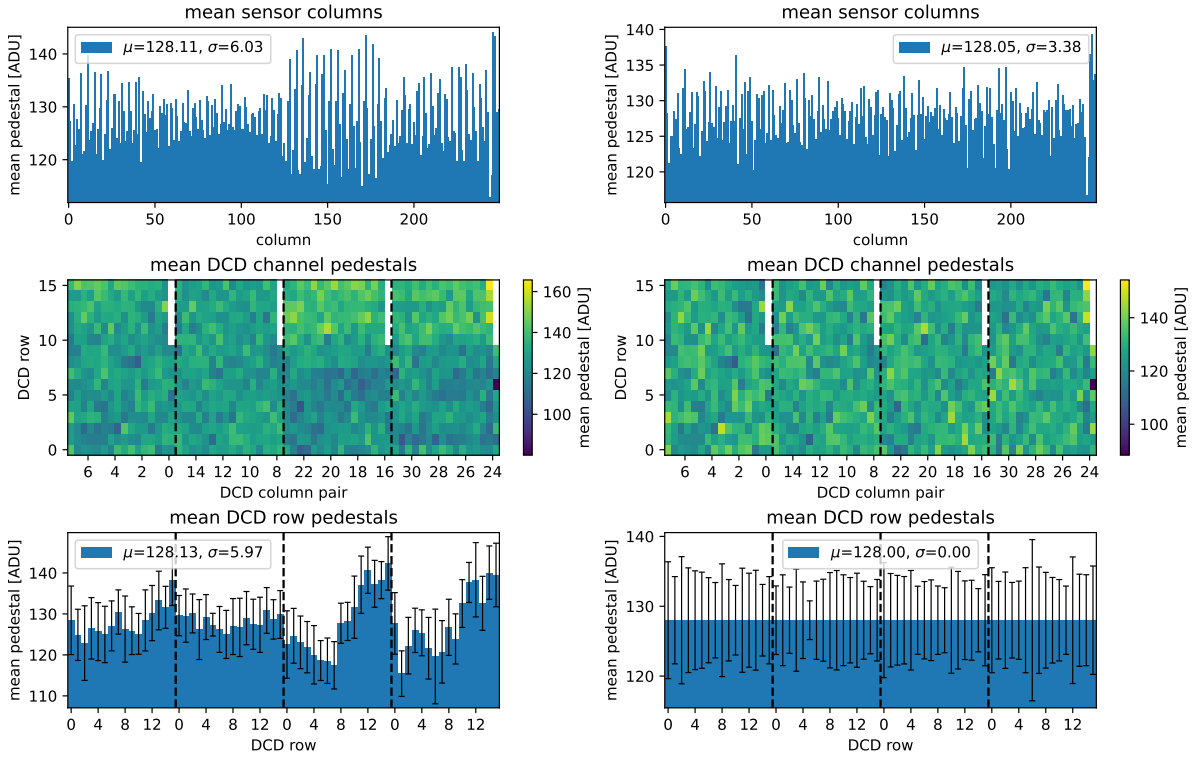


Figure 5.33: W46_OB1 row deviation and correction. The left column shows mean sensor pixel-column pedestals, DCD-channel and DCD-row pedestals before correction. The right column shows the same quantities after correction.

wafer/sensor	DCD row pedestal variation [ADU]			
	DCD 1	DCD 2	DCD 3	DCD 4
W09 IF	4 ± 7	5 ± 5	8 ± 5	9 ± 5
OF1	15 ± 7	17 ± 8	14 ± 7	16 ± 8
OF2	23 ± 9	10 ± 7	17 ± 6	25 ± 8
OB1	18 ± 8	15 ± 10	10 ± 9	7 ± 7
OB2	9 ± 8	14 ± 6	15 ± 7	6 ± 8
IB	14 ± 7	18 ± 8	26 ± 7	16 ± 8
W37 IF	8 ± 9	19 ± 12	13 ± 8	7 ± 7
OF1	13 ± 11	17 ± 12	14 ± 8	12 ± 7
OB1	11 ± 7	9 ± 10	15 ± 10	12 ± 7
W46 IF	22 ± 9	15 ± 14	18 ± 10	24 ± 12
OF1	30 ± 10	23 ± 10	17 ± 9	17 ± 11
OF2	33 ± 9	15 ± 12	24 ± 11	17 ± 10
OB1	15 ± 11	6 ± 8	25 ± 9	25 ± 9
OB2	24 ± 10	13 ± 8	31 ± 7	23 ± 11
IB	34 ± 12	16 ± 11	11 ± 9	21 ± 8
W56 IF	14 ± 8	9 ± 8	7 ± 8	17 ± 9
OF1	13 ± 9	9 ± 10	11 ± 7	14 ± 10
OF2	13 ± 8	17 ± 8	19 ± 8	17 ± 7
OB1	15 ± 10	12 ± 10	13 ± 10	17 ± 8
OB2	17 ± 10	18 ± 8	12 ± 10	28 ± 7
IB	21 ± 9	16 ± 8	19 ± 8	15 ± 8
W57 OF1	13 ± 10	11 ± 8	8 ± 5	14 ± 8
OF2	25 ± 11	14 ± 11	15 ± 11	9 ± 9
OB1	14 ± 9	16 ± 10	16 ± 10	29 ± 13
IB	17 ± 12	18 ± 11	22 ± 10	27 ± 8
W67 IF	8 ± 9	11 ± 11	18 ± 9	17 ± 7
IB	21 ± 10	26 ± 10	21 ± 10	12 ± 7

Table 5.7: DCD row pedestal variations for all examined modules.

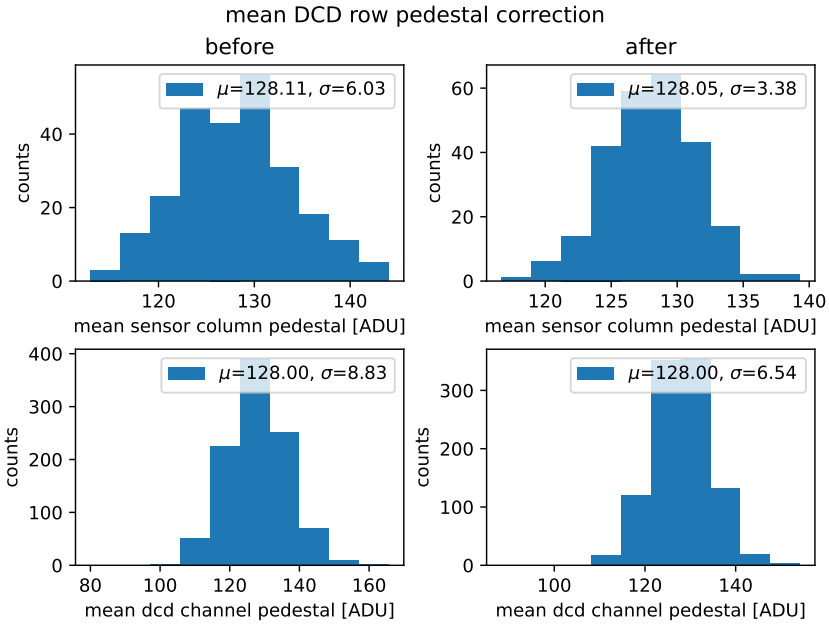


Figure 5.34: W46_OB1 mean sensor pixel-column (top) and DCD channel (bottom) pedestals before (left) after row (right) correction.

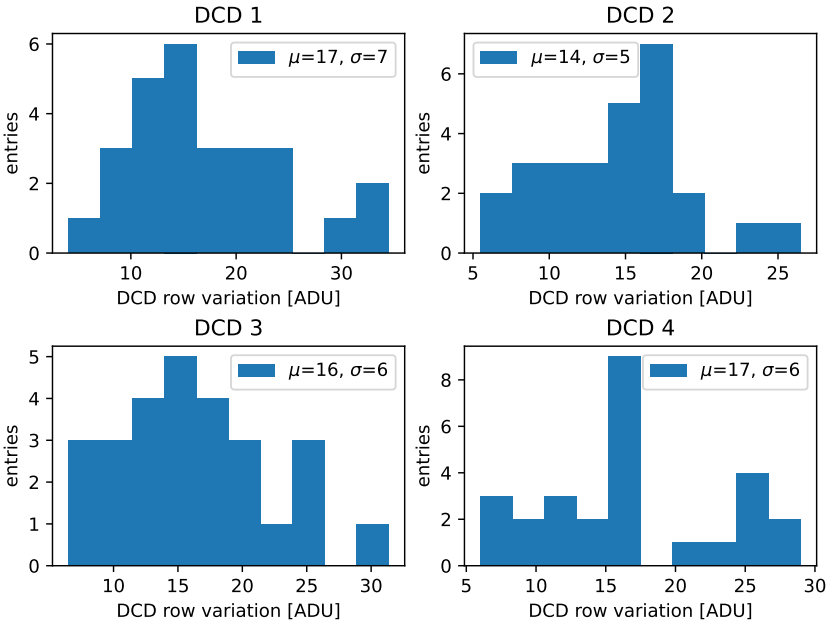


Figure 5.35: W46_OB1 mean DCD row pedestal variation per DCD.

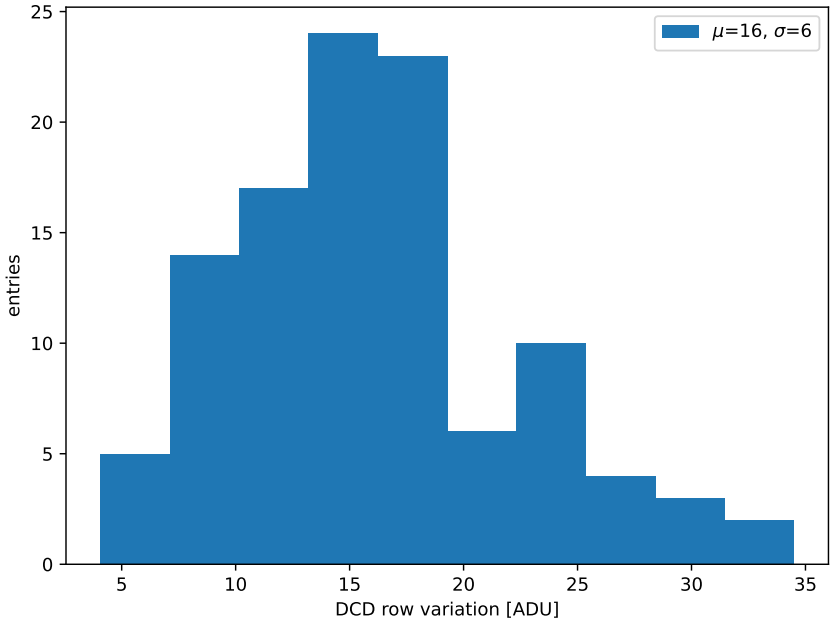


Figure 5.36: W46_OB1 mean DCD row pedestal variation summary.

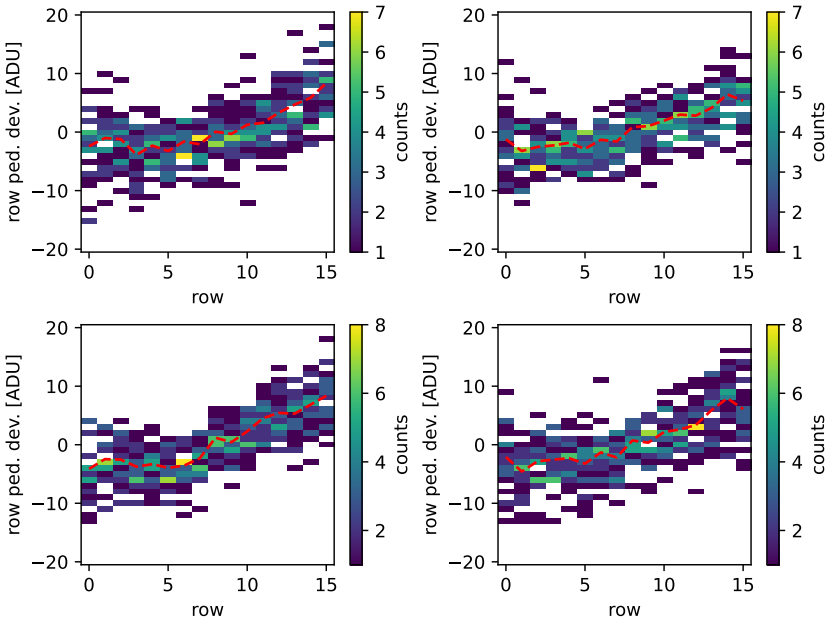


Figure 5.37: Histograms of DCD row pedestal deviations of all examined modules, separated by DCD.

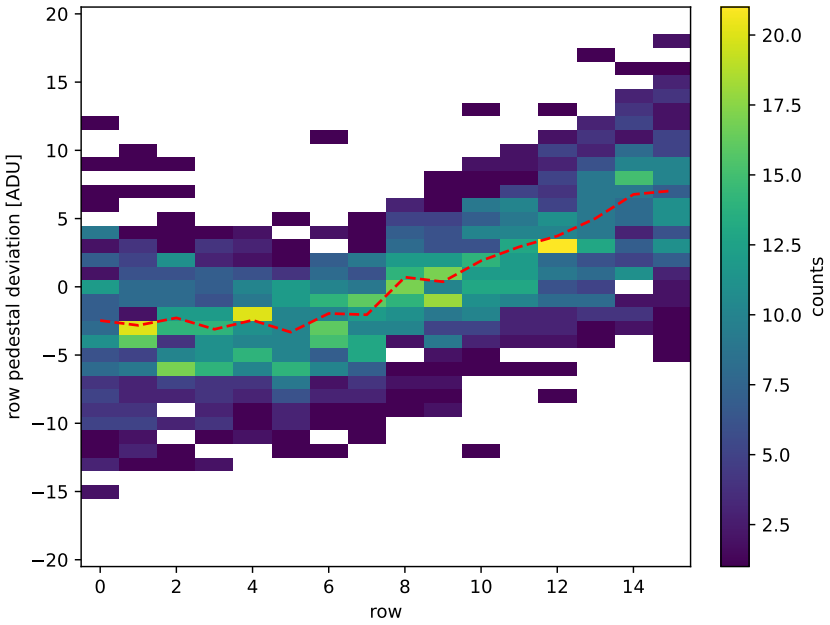


Figure 5.38: Histogram of DCD row pedestal deviations for all examined modules, summing all DCDs.

5.7 Diagonal Stripes

After application of corrections for the pedestal variations described above some wafer level variations become apparent. There appear to be diagonal stripes at certain angles. Their angles and contribution can be found when rotating the wafer and calculating the average projected pedestal. These stripes are especially prominent in wafers 9 and 46. Figure 5.39 shows the projected pedestals of wafer 46 as a function of rotation angle. As FOM the weighted standard deviation of the pedestals is calculated and peaks at around 11°. Figure 5.40 shows a map of the pedestals of the rotated wafer 46 and their mean projection. The stripes of pedestal variations appear to be spaced ~ 6 mm from peak to peak and cause variations of ~ 10 to 30 ADU, i.e. ~ 1 to 3 µA. Figure 5.41 and Fig. 5.42 show the same plots for wafer 9. Here even more prominent stripes of up to 6 ADU, i.e. 6 µA, are found at a similar spacing.

Wafers 56 and 57 also feature distinct stripes at a similar angle. For the other wafers 37 and 67 no distinct stripes are seen.

The pattern can be seen to be continuous across all modules of the same wafer and of consistent magnitude. Due to the angle it cannot be caused by DWL. Other possibilities are implant doping variations, variations of the oxide layer thickness or dark current differences due to surface defects. Since the oxide is very well controlled, bulk variations in this pattern are unlikely and no doping process with this angle is known, surface defects appear to be most likely. They could be introduced in cutting or polishing operations. Since no polishing is done at HLL, these variations are probably already introduced by the manufacturer of the wafers. Surface defect variations cause variations in thermal generation of charge carriers and therefore the dark current.

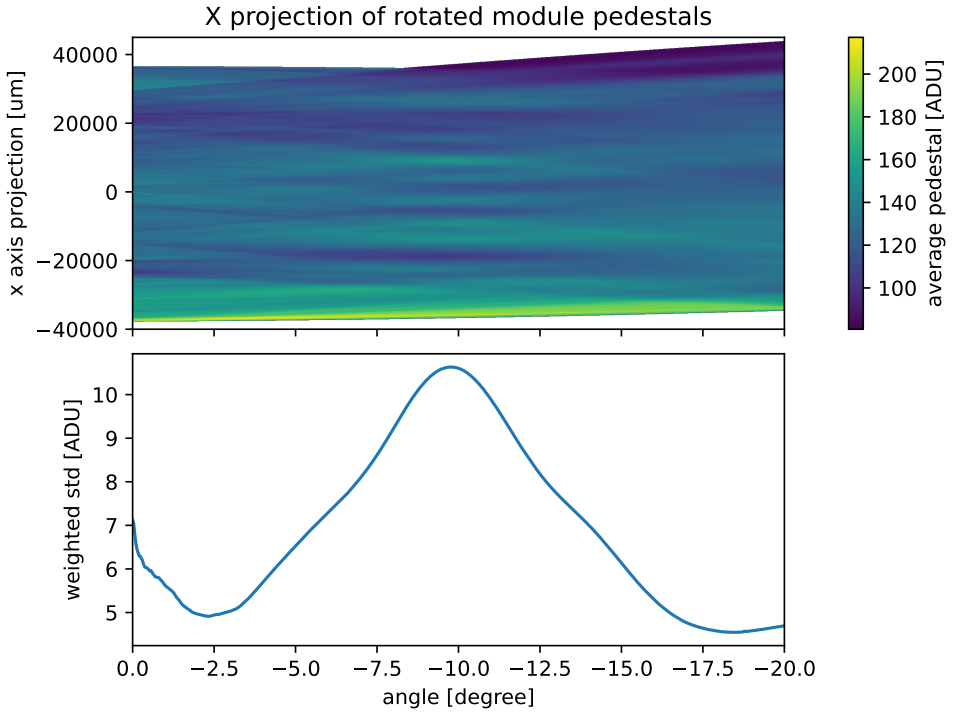


Figure 5.39: Top: Average pedestals of rotated wafer 46 projected onto the x-axis. Bottom: weighted standard deviation to determine the angle of the diagonal stripes.

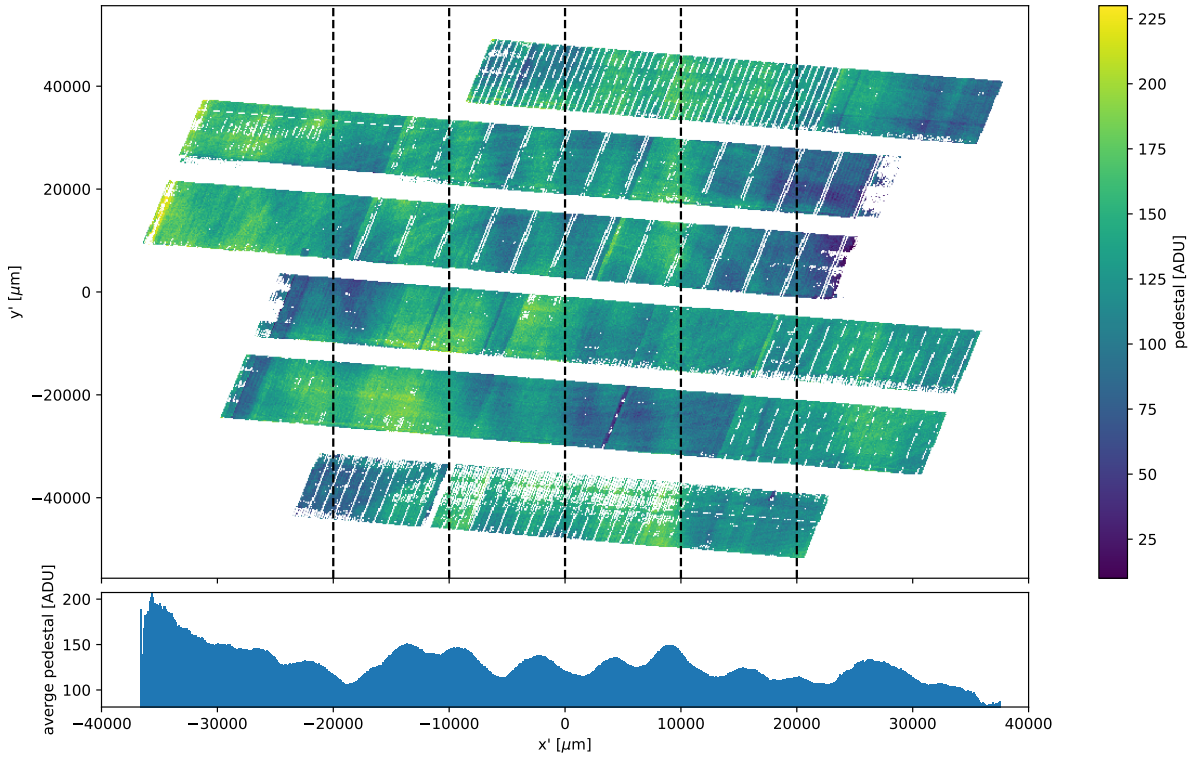


Figure 5.40: Pedestals of wafer 46 sensors rotated by $-10.5°$ and their average projection onto the x-axis.

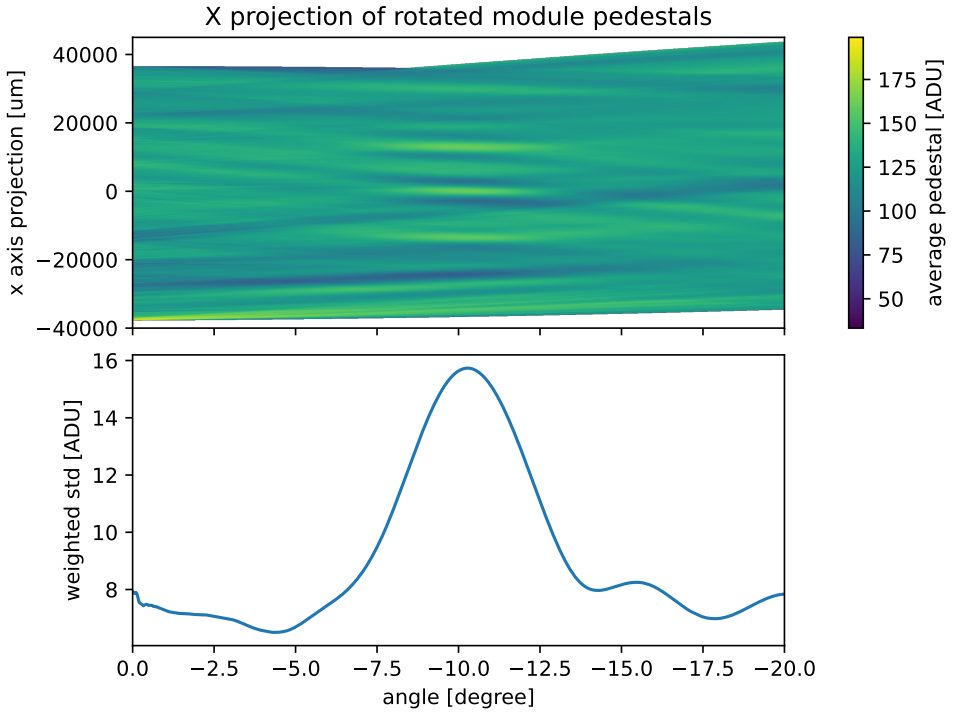


Figure 5.41: Top: Average pedestals of rotated wafer 9 projected onto the x-axis. Bottom: weighted standard deviation to determine the angle of the diagonal stripes.

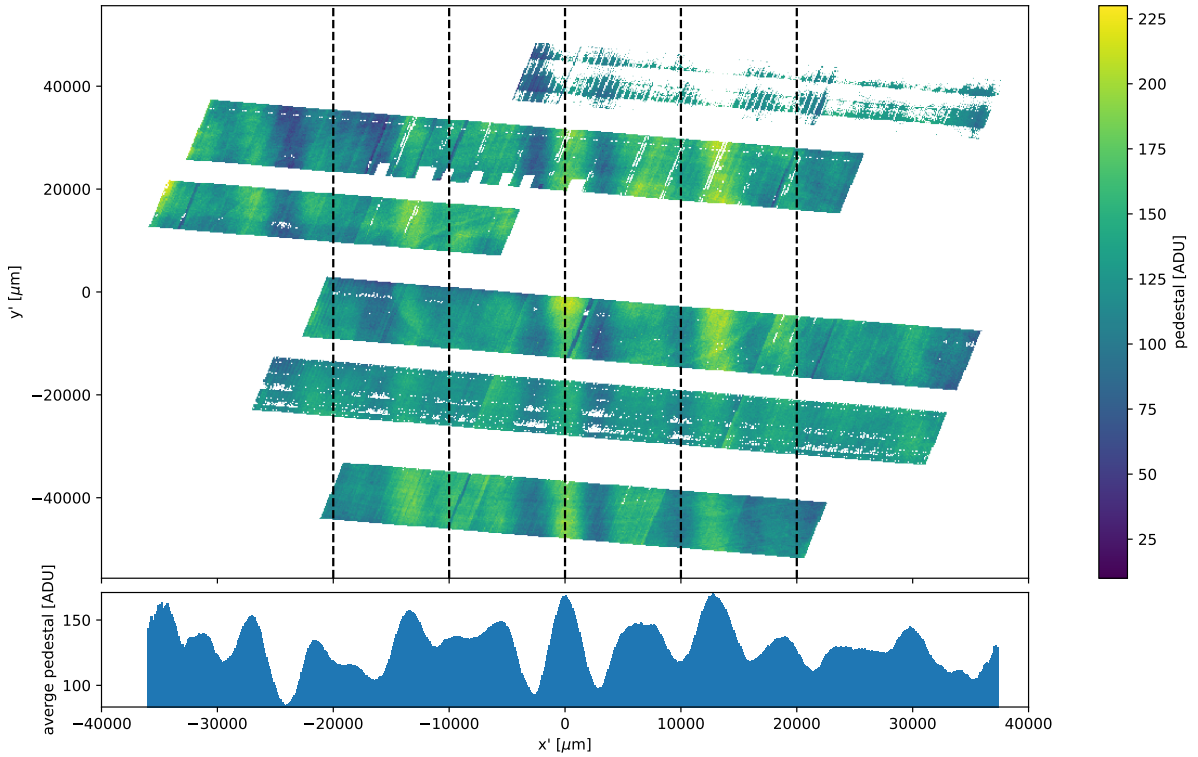


Figure 5.42: Pedestals of wafer 9 sensors by $-10.5°$ and their average projection onto the x-axis.

5.8 Rings

Figures 5.43 to 5.48 show maps of the pedestals of all examined wafers after all corrections. As can be seen in the wafer representation, all pedestals exhibit rings concentric to the wafer. These fluctuations cannot originate from any wafer processing. Instead, they must stem from the production of the silicon ingot itself. Since the ingot is grown from the center outward, these rings are most likely bulk doping variations.

Figures 5.49 and 5.50 show the mean pedestals of W37_OF1 and W46_OF1 as a function of radius from the wafer center. Regular peaks and valleys are visible as a consequence of the ring pattern. They are spaced at roughly 1 mm on average and have a height of up to 20 ADU, corresponding to $\sim 2\,\mu\text{A}$ difference in drain current I_D.

If this change is assumed to be due to bulk variation the required size can be estimated:

$$\begin{aligned} I_\text{D} &= g_\text{m} \cdot V_\text{FET} \\ \Delta V_\text{FET} &\approx 0.003 \cdot \Delta V_\text{depl.} \\ \Delta V_\text{depl.} &= \frac{d^2 \Delta N_\text{d} q}{2\epsilon_\text{Si}} \end{aligned}$$

The factor 0.003 between change in depletion voltage $V_\text{depl.}$ and change in FET voltage $V_\text{FET channel}$ is due to the capacitive voltage divider between the gate and the back side with gate oxide capacitance C_Ox and bulk capacitance C_Si. The parameter ϵ_Si is the permittivity of silicon, d the thickness of the bulk of 75 µm, N_d the doping concentration and q the unit charge.

Solving for ΔN_d we get

$$\Delta N_\text{d} = \frac{I_\text{D} \cdot 2\epsilon_\text{Si}}{0.003 \cdot g_\text{m} d^2} \quad . \tag{5.12}$$

Plugging in the observed I_D variation of $2\,\mu\text{A}$ this results in an estimated $\Delta N_\text{d} = 2 \times 10^{12}\,\text{cm}^{-3}$ corresponding to about 20 % of the nominal bulk doping concentration of $N_\text{D} = 1 \times 10^{13}\,\text{cm}^{-3}$.

These ring structures are also commonly observed in sensor hit maps when a non-optimal high voltage V_HV is chosen. Due to the differences in doping concentration the bulk depletes at different voltages. Too low and too high depletion voltages lead to loss of charges [35, p.63]

Ring shaped variations were also observed in clear-threshold measurements of the DEPFET sensors of the Mercury Imaging X-ray Spectrometer (MIXS) [41] as well as drain current measurements of ATHENA DEPFET sensors [42]. The respective authors attribute them to bulk doping variations or charge carrier mobility variations due to crystal quality variations in the growing process.

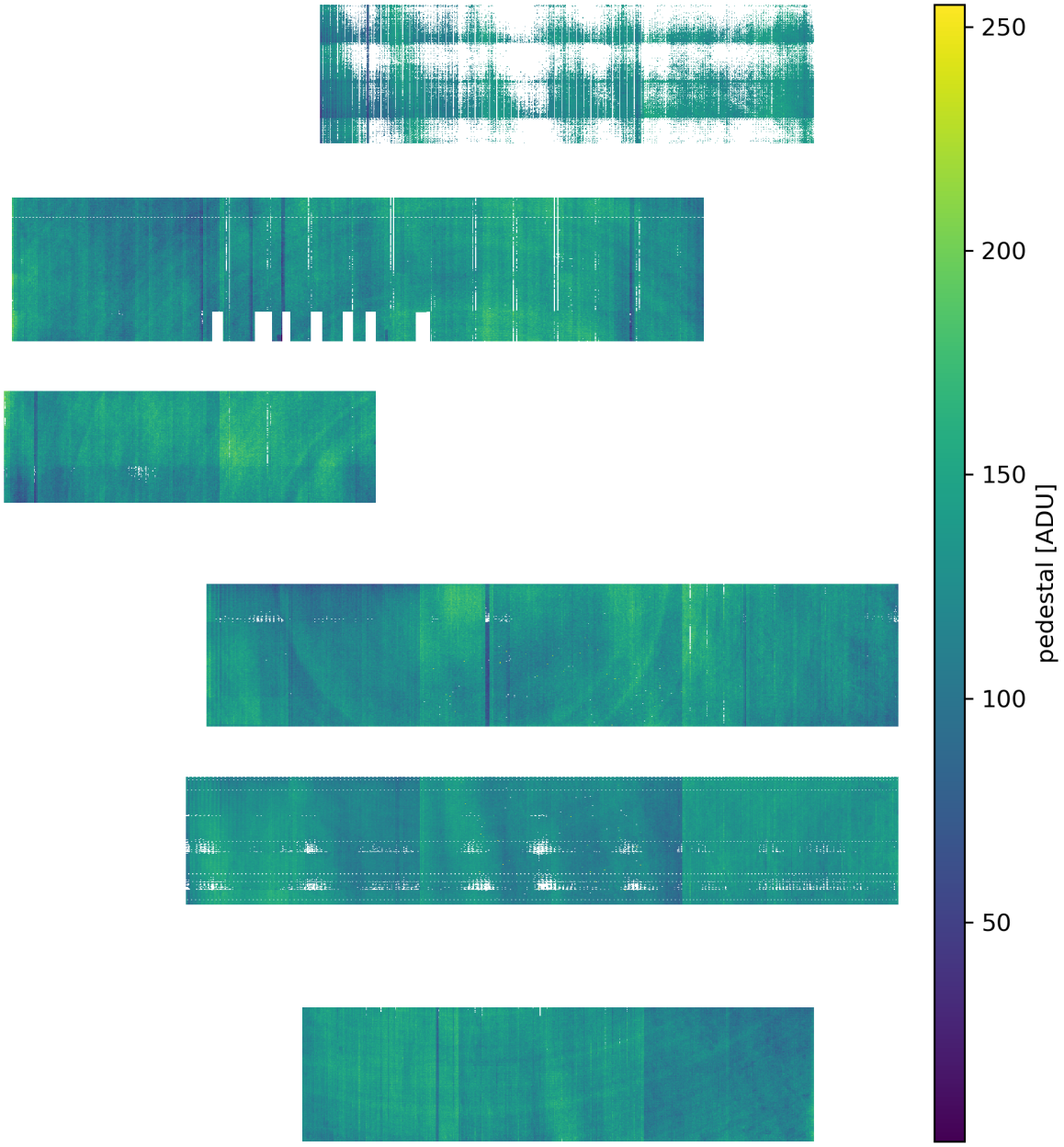


Figure 5.43: Pedestals of wafer 9 after all corrections.

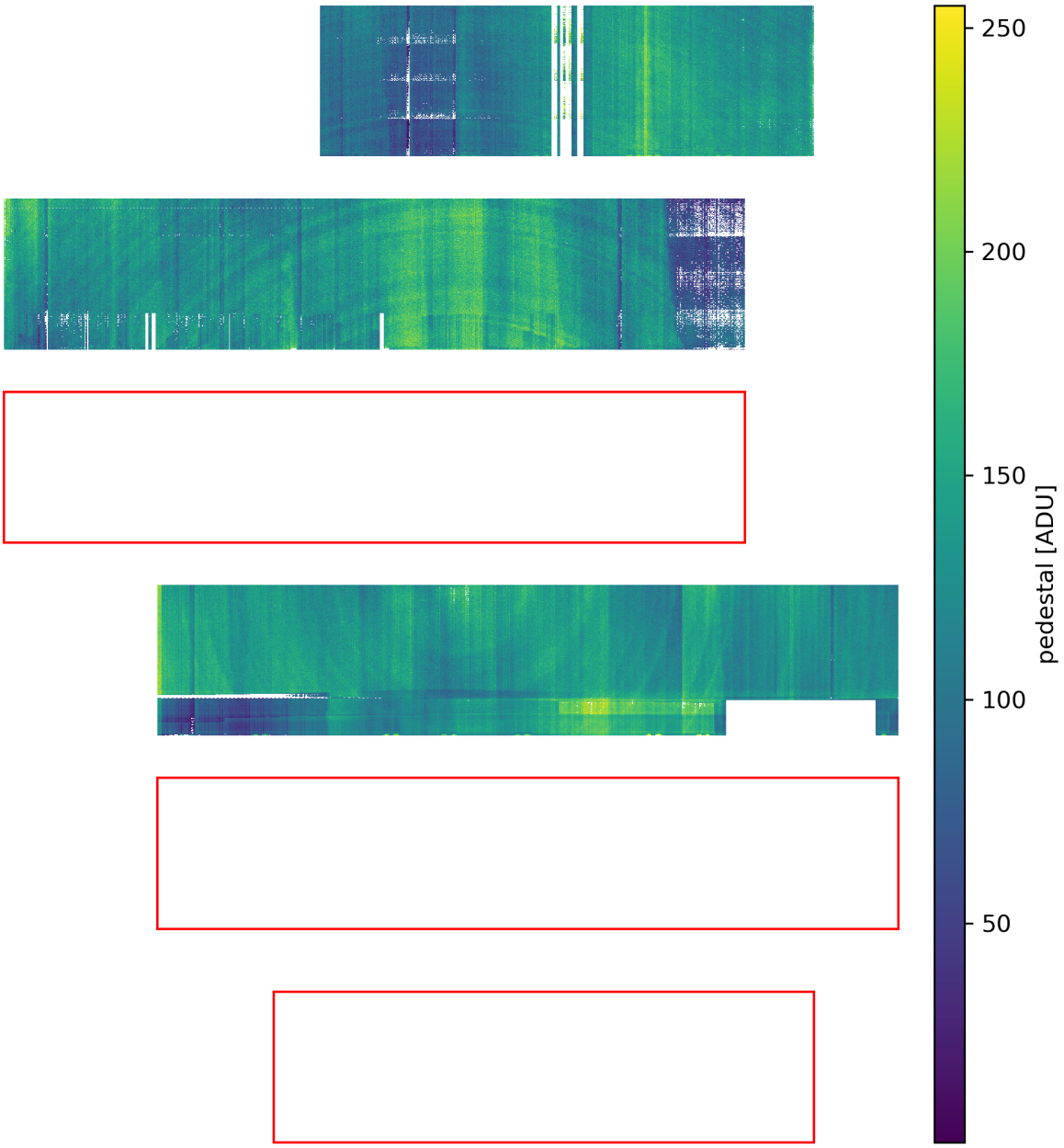


Figure 5.44: Pedestals of wafer 37 after all corrections. The relative position and size of the pixels in this figure corresponds to their position and size on the wafer. The color code denotes the pedestal value in ADU. The red boxes mark the outlines of sensors without measured pedestals.

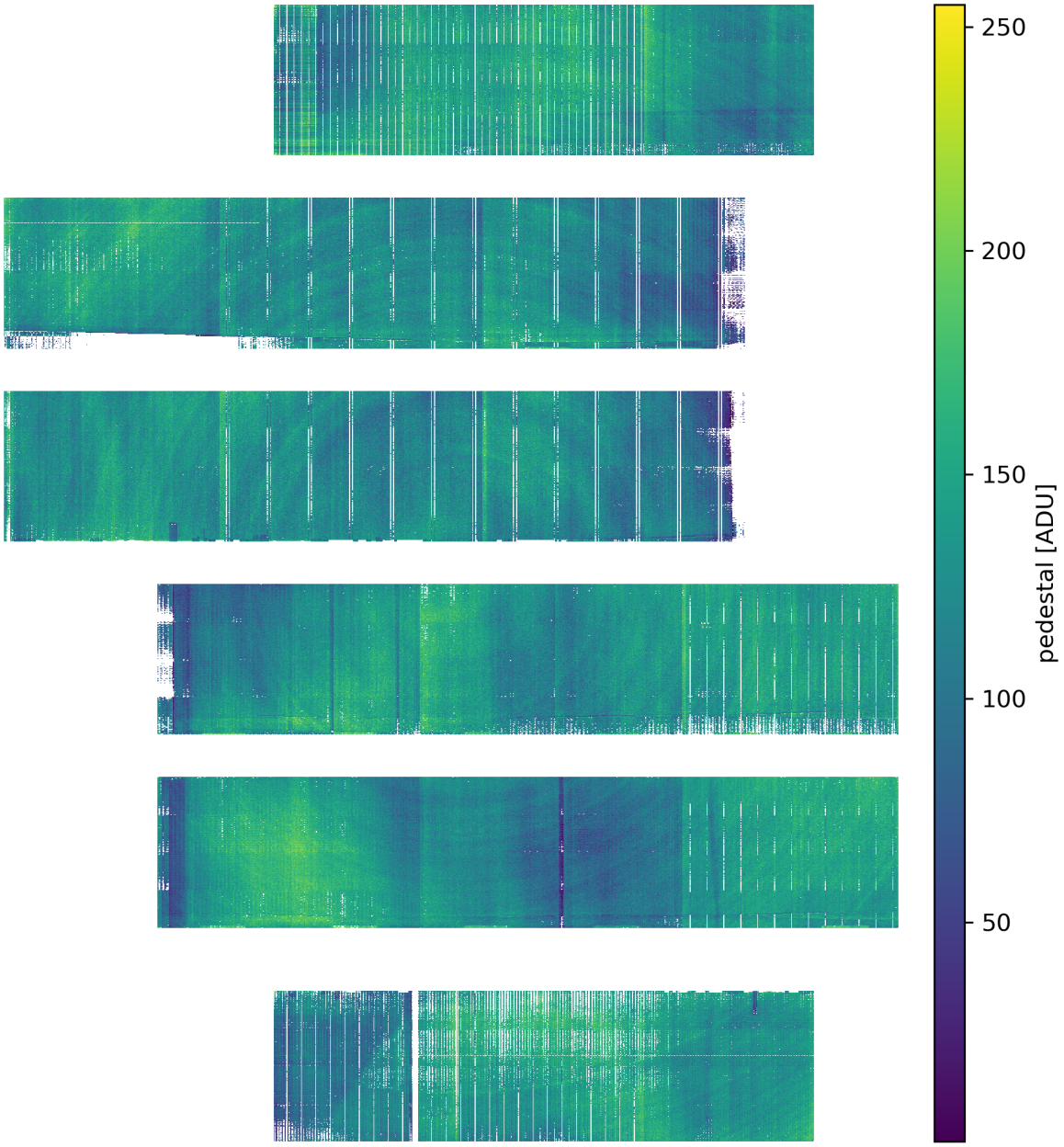


Figure 5.45: Pedestals of wafer 46 after all corrections.

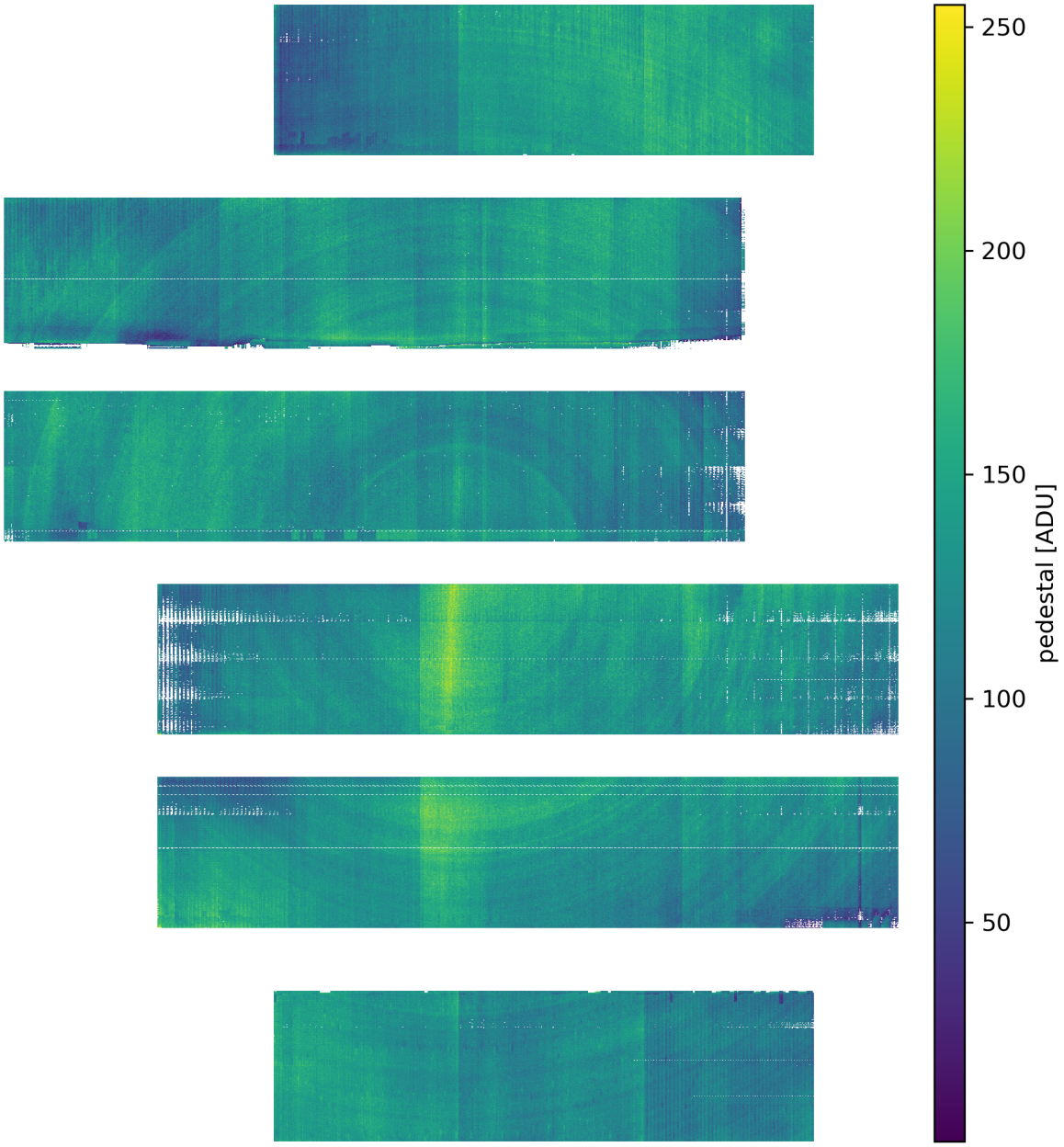


Figure 5.46: Pedestals of wafer 56 after all corrections.

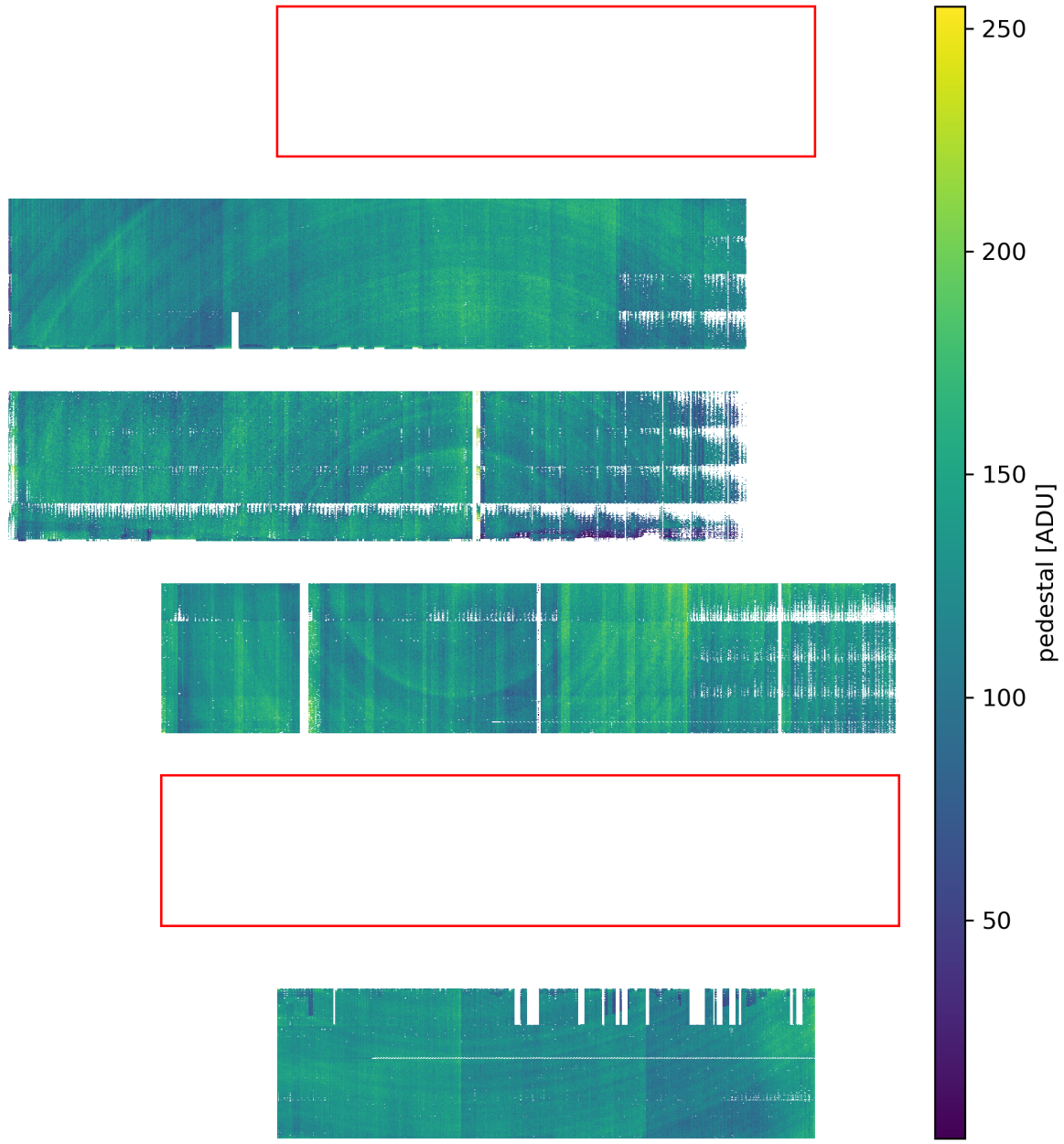


Figure 5.47: Pedestals of wafer 57 after all corrections. The red boxes mark the outlines of sensors without measured pedestals.

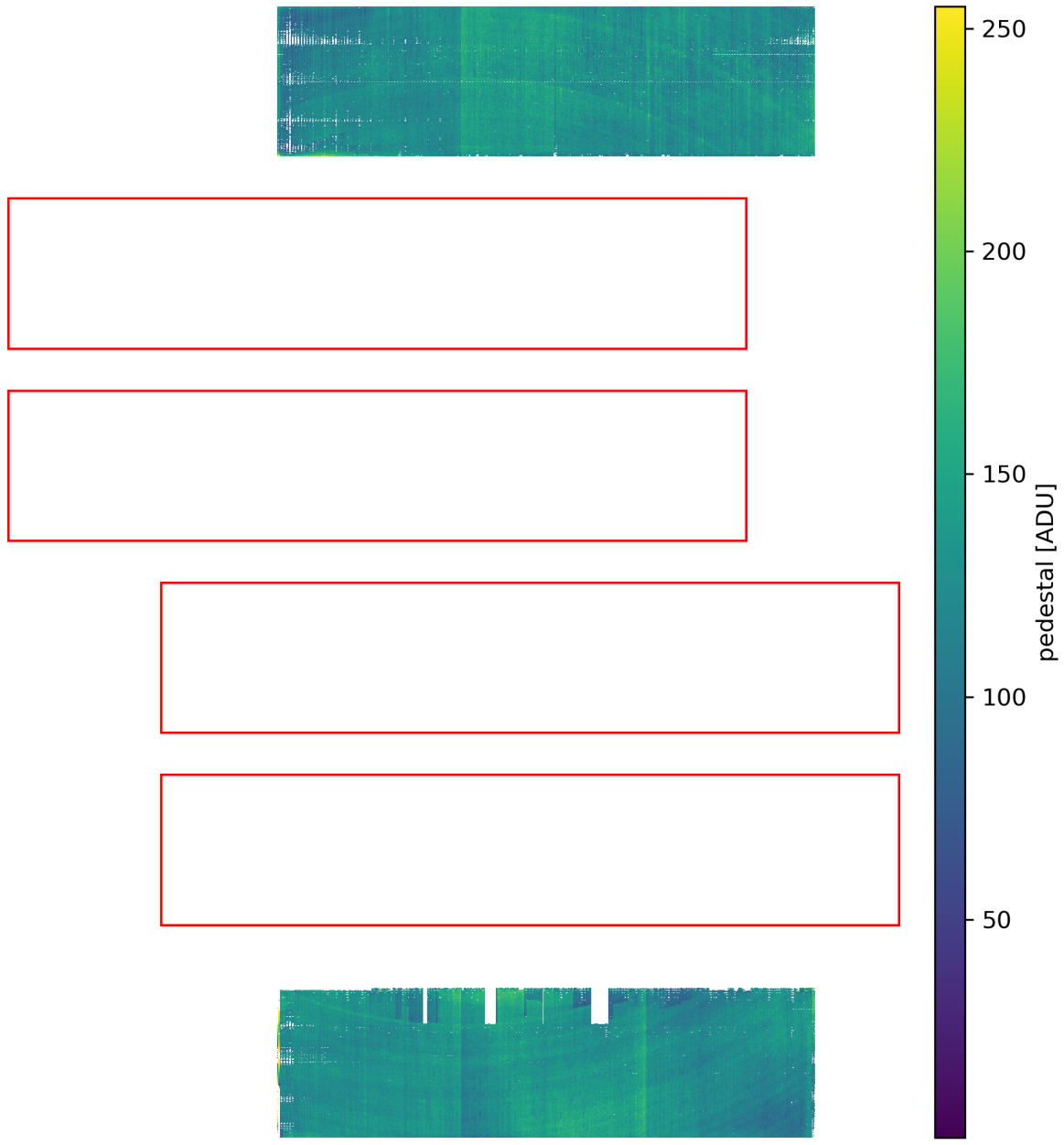


Figure 5.48: Pedestals of wafer 67 after all corrections. The red boxes mark the outlines of sensors without measured pedestals.

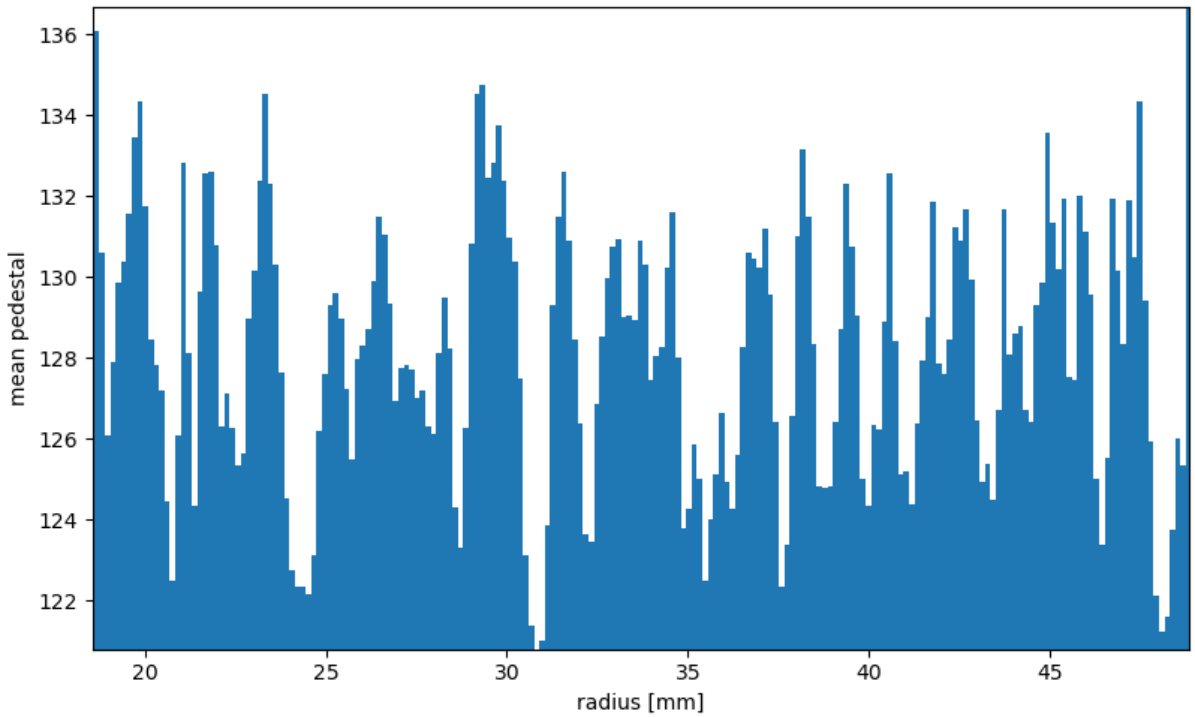


Figure 5.49: Average pedestal values at distance 'radius' from the wafer center for module W37_OF1 after corrections. The binning is 150 µm.

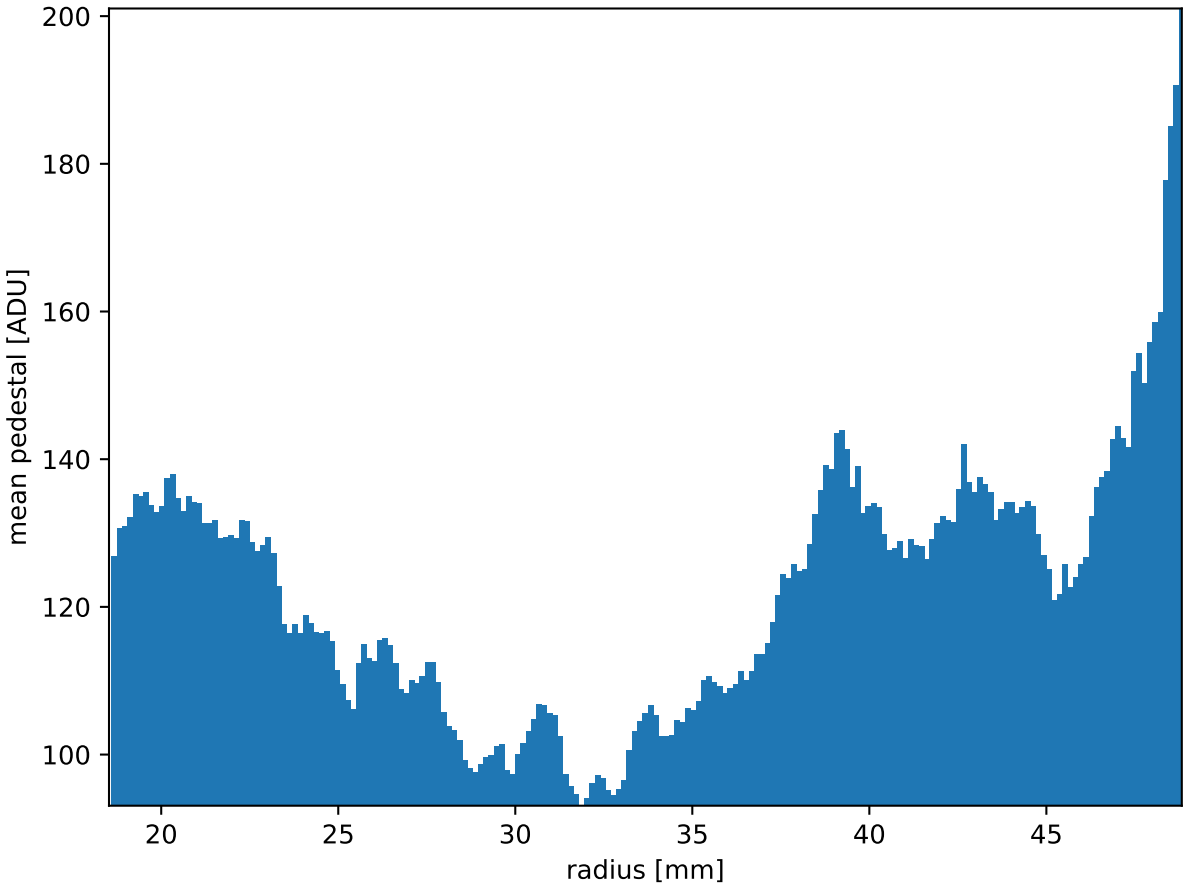


Figure 5.50: Average pedestal values at distance 'radius' from the wafer center for module W46_OF1 after corrections. The binning is 150 µm.

5.9 Other Variations

As seen in the corrected pedestal maps, there are still other contributions to the pedestal spread. Individual groups of four rows (read-out rows) can be observed to deviate from the surrounding rows. This can be due to switcher channel variations or problems with the shared gate line for these rows.

Additionally, gradients are visible in many modules, especially close to the DCDs. Here the pedestals appear to decrease in the first sixth to third of the sensor rows the closer they are to the ASICs. Similarly, decreased g_{m} and g_{m} values were measured in the same region [35, 39, 43]. The reason is not quite clear. Speculations include variation of the sampling point across the sensor or changes in the capacitive load of the drain line.

Other gradients across the sensors can also be observed as well as separations between the three different gate/ccg regions.

5.10 Conclusion

The main contributions of the pedestal spread of unirradiated modules have been examined on a number of sensors from different wafers and production runs. The magnitude of the variations has been quantified and is summarized in Table 5.8.

The resulting pedestal spread at nominal operation biases often exceeds the limited dynamic range of the DCD. The DCD implements two main correction mechanisms, namely Analog Common Mode Correction (ACMC) and a two-bit offset correction. These correct pedestal offsets and effectively widen the dynamic range by theoretically up to a factor 4. More details about these corrections can be found in [31].

The DCD itself contributes significantly to the pedestal spread, especially with the observed gradient across its columns.

The next largest contributions are X-ray inspection damage, which can be optimized by shielding or even irradiation. These inhomogeneities will vanish over time in the experiment since the rate of the FET threshold shift decreases with increasing total ionizing dose.

Periodic row outliers shift a number of lines outside the dynamic region of the uncorrected pedestals. This can be corrected by DCD offset correction and could possibly be further optimized in production by adjusting DWL parameters.

phenomenon	size µA
X-ray inspection damage	5-10
periodic row outliers	3-13
double row effect	2-6
DCD column gradient	4-10
even-odd column / periodic drain line pattern	1-2
DCD row variation	1-2
Diagonal stripes	1-3
Rings	2

Table 5.8: Pedestal variation contributions and the size of their effect.

The double-row effect might increase in severity during irradiation and so could become the leading contribution to the fluctuations over time.

In summary, with the current settings the PXD modules can be operated well. Additional space for measurement of the signal charge could be freed with optimization of the ASIC and sensor properties. For the case of the PXD the exact charge determination only plays a minor role, as for tracking a binary hit/no-hit information is sufficient.

CHAPTER 6

PXD performance in Phase 2

The commissioning of the Super-KEKB accelerator and the Belle II experiment was spread out over three phases. This strategy was chosen to evaluate beam backgrounds and allow for accelerator tuning before inserting the final VXD.

During *phase 1* in 2016 the Super-KEKB accelerator was operated without final focussing around the Interaction Region (IR) and without the Belle II detector in place. Instead, an array of dedicated radiation detectors was situated around the IR measuring background radiation created by the accelerator beams [44].

In *phase 2* [45] (2018) the accelerator was in its final configuration with focussing magnets and beam pipe. The Belle II detector was rolled in without the final VXD. The VXD volume was instrumented with only a slice of the actual VXD and a number of dedicated other detectors. First beam collisions of Super-KEKB were recorded in this phase.

Finally, *phase 3* commenced in fall 2018 with the fully equipped Belle II detector around the IP.

This chapter describes the *phase 2* PXD setup and its performance.

6.1 Phase 2 PXD Setup

Figure 6.1 shows the layout of the detectors in the VXD volume during Phase 2. Two PXD and four SVD ladders form a slice of the VXD. Additionally, three dedicated detector systems are installed to record background radiation.

The FE-I4 ATLAS Near Gamma Sensors (FANGS) [16] detector is next to PXD the closest system to the interaction point. Three staves at azimuthal angles $\phi = 90^\circ, 180^\circ, 270^\circ$ are installed in place of the layer-two PXD ladders.

Two staves of sCintillation Light And Waveform Sensors (CLAWS) [46] and Pixelated Ladder using Ultra-light Material Embedding (PLUME) [47] detectors are placed at $\phi = 135^\circ$ and $\phi = 225^\circ$.

6.1.1 Phase 2 PXD System

The *phase 2* PXD setup consists of four modules with final design and final ASICs. They are arranged as one inner and one outer ladder, but contrary to the final design, they are not glued together. Instead, they are screwed to the Support and Cooling Blocks (SCBs) on each side.

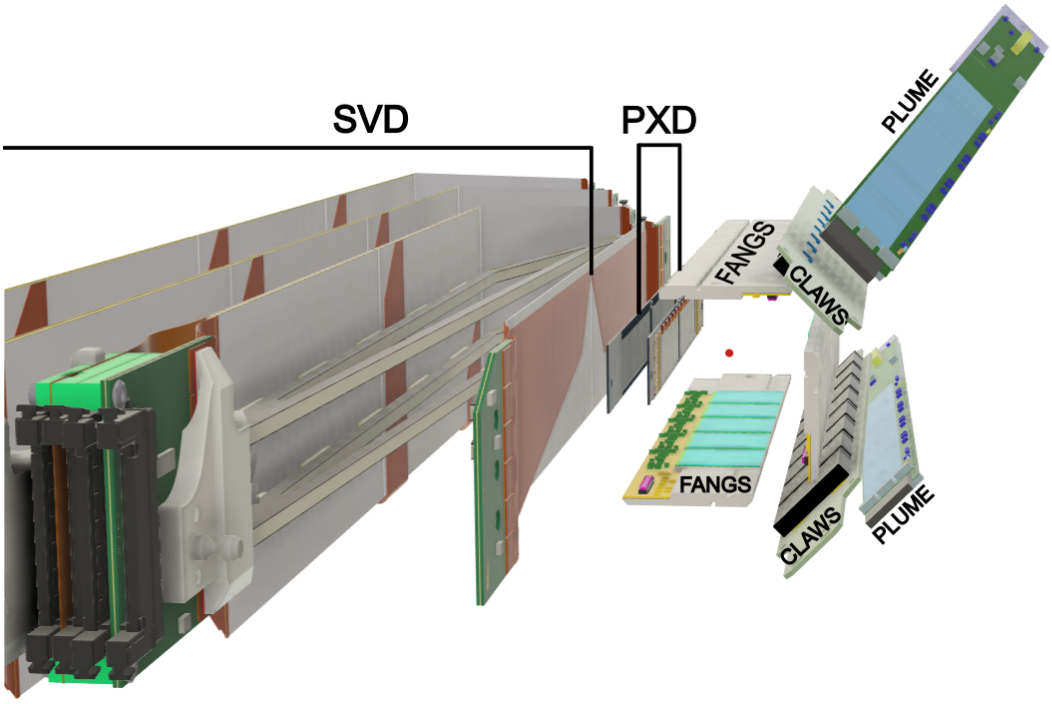


Figure 6.1: Layout of the detectors in the *phase 2* VXD volume.

The services, i.e. cooling, PS, backend readout and cables are close to the final design. A prototype of the DHI was used connecting the InfiniBand (IBa) DHE outputs and CLC cables to the dock boxes, as shown in Fig. 6.2.

6.1.2 Power Supply Issues

This section presents the issues encountered with the PXD PS system during Phase 2 operation and their solutions.

Slow Control Communication

It was found that the slow control communication of the PS was not stable when multiple units are running in parallel. Communication was based on the CHROMOSOME run-time environment [48]. It is not known where the problem exactly originated, possibly network multicasting used by the protocol was to blame. The communication layer was simplified by implementing a solution purely based on Transmission Control Protocol (TCP). The changes were made and applied by Michael Ritzert (University of Heidelberg) in spring 2018.

DGND sense line short

The PS provide 23 supply lines, of which 16 are *sensed*. This means the voltage at load is monitored on the module via dedicated additional wires called *sense wires*. Since depending on the current sizeable voltage drops occur over the long cable connections between PS and module, sensing is necessary to

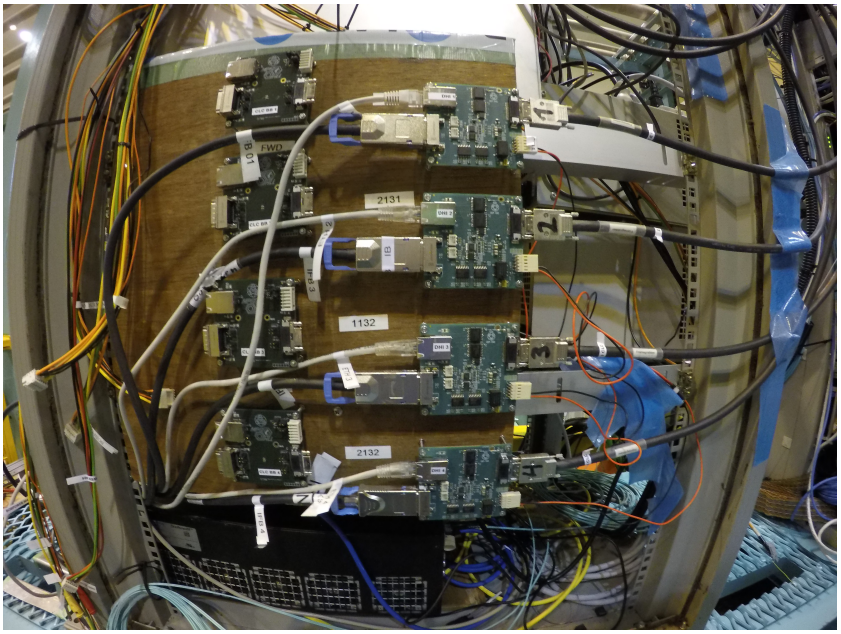


Figure 6.2: Phase 2 DHI prototype boards. To the left RJ45 and Infiniband cables are connected to the DHE boards of the DHH, to the right external power supplies are attached and CLCs are routed towards the dock boxes.

reach the desired voltages at load. The PS compensates the voltage drop by increasing the output voltages on the supply lines beyond the set voltage until the sensed voltage at load agrees with the set voltage.

Since the DHH system needs to communicate with the DHPs for control (clock, trigger, Joint Test Action Group (JTAG)) and data read-out, a common voltage reference is needed. Therefore, the DGND sense line is routed to the optical transmitter receiving the DHP data and to the DHI. The data links were found not to be stable under these conditions and a connection of the DHI ground to the Belle II ground improved this. The connection improvised connection on the PCB is shown in Fig. 6.3. Figure 6.4 shows a schematic of the affected lines in the system. The hypothesis is that the VSS sense line, i.e. the DGND sense, does not provide a sufficiently stable reference for clock generation of the DHI. Therefore, the added connection as a workaround provides a stable reference, but disturbs the DGND sensing of the PS. As a consequence, the effective digital voltage is lower than the set voltage on the modules.

6.1.3 Data Acquisition System

The DAQ configuration is shown in Fig. 6.5. It constitutes a subset of the final DAQ. The read-out and control of the PXD is split into ForWarD side (FWD) and BackWarD side (BWD). On each side, a DHC receives clock and triggers from the Front end Timing SWitch (FTSW) [49]. Each DHC controls two DHEs, each of which handles the control of one module and receives its data. The data for each trigger are sent to the DHC after collection and then combined into events. The events are sent from DHC to ONSEN and to the local DAQ. ONSEN receives Region Of Interests (ROIs) from DATa CONcentrator (DATCON) [50] and High Level Trigger (HLT) and event triggers from HLT. ROI information can be used for data reduction by using extrapolated online tracking data for defining geometric read-out windows.

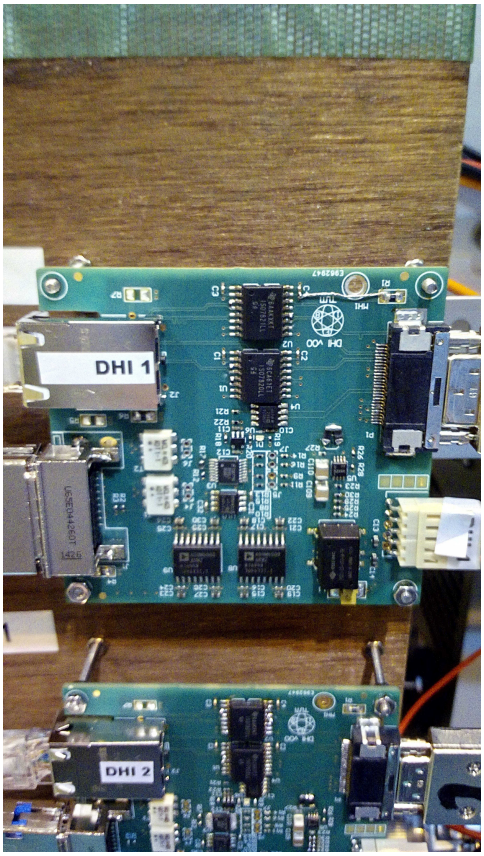


Figure 6.3: Phase 2 DHI with short to Belle II ground. The short is introduced in the top right corner of the board via a thick soldered cable connecting the shield of the CLC (Belle II GND) to the DHP sense GND on the DHI.

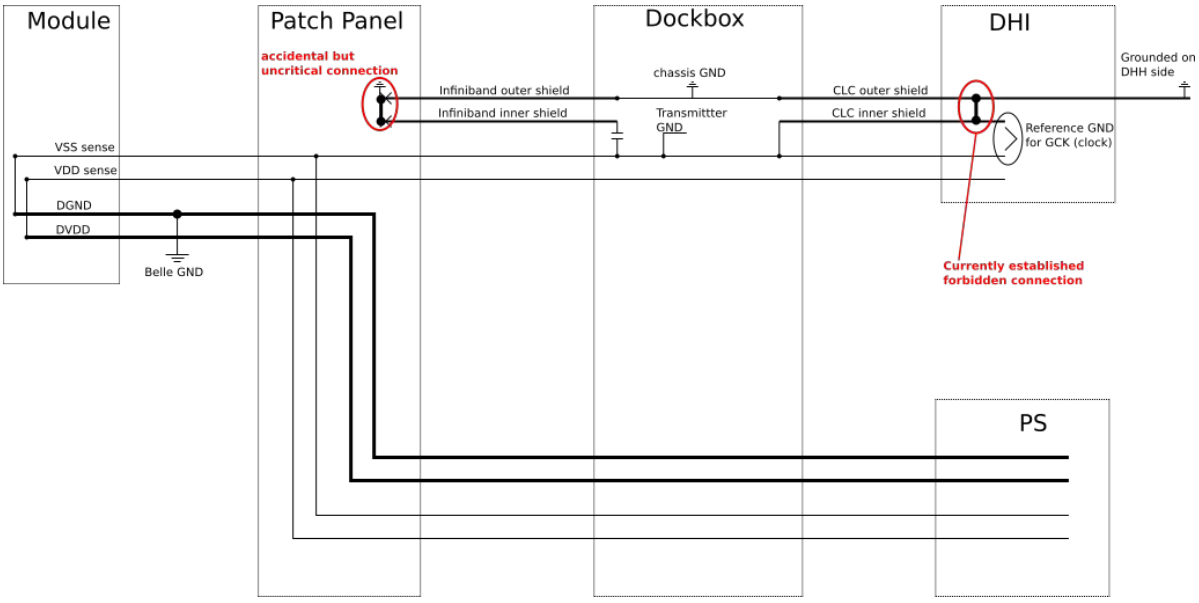


Figure 6.4: Phase 2 grounding and sensing schematic.

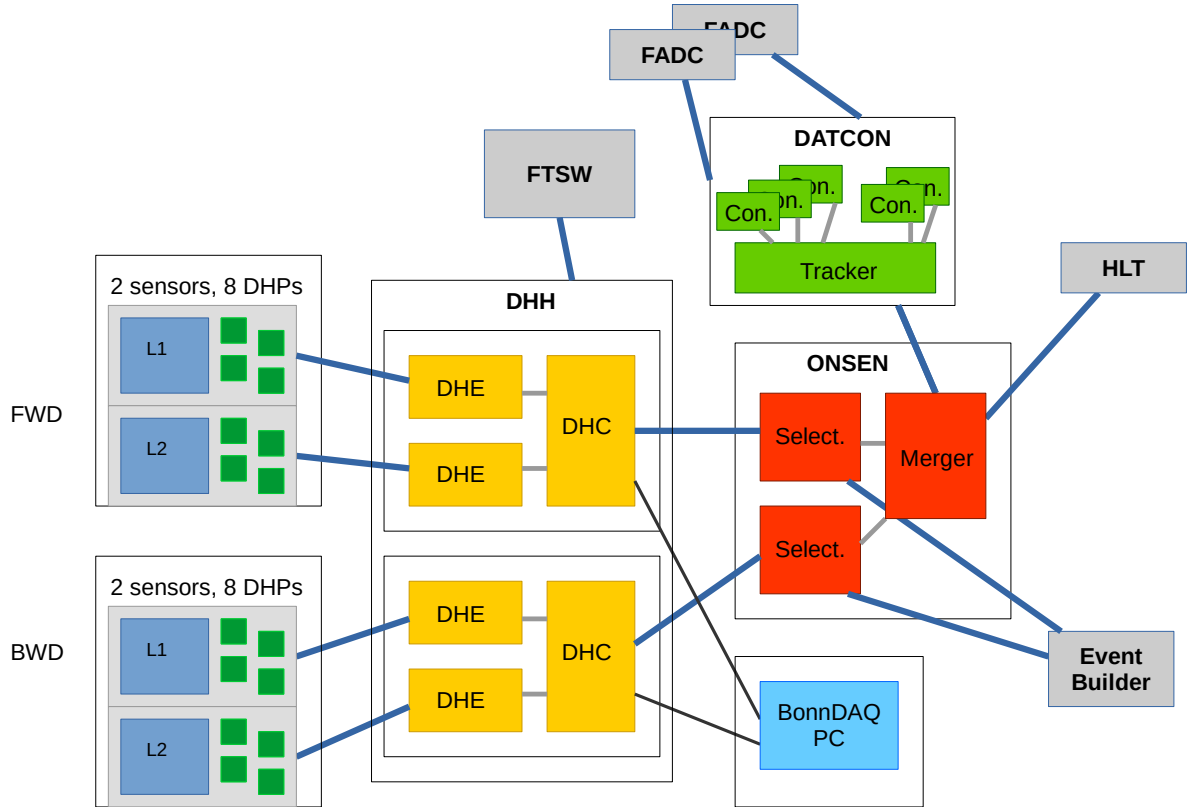


Figure 6.5: The phase-2 PXD DAQ. The DAQ system and its components are explained in the main text (see Section 6.1.3).

local DAQ is a regular PC/server receiving read-out data from the DHH on network interfaces via UDP for monitoring and offline analysis. It is used during regular runs and for pedestal updates and for module calibration in between runs. All data presented in this chapter are obtained from the local DAQ.

During Phase 2 the DHH did not have overlapping trigger capabilities. This means each read-out and event building have to be finished before another trigger is issued. Details about the implications of this will be described in Section 6.2.3.

6.1.4 Modules

Four modules were installed in the Phase 2 PXD, one of each type.

- W46_IB
- W37_IF
- W37_OB1
- W37_OF1

They feature the final module layout and are equipped with the final ASICs, i.e. DHPT 1.2B, DCD 4.2 and switcherB2. .

6.2 Operation and Performance

This section presents the operation and performance of the Phase 2 PXD system.

6.2.1 Module Configuration

Configuration Changes

The configuration of the PXD is described by entries in the configuration database, the *configDB*. Each full set of configurations is referred to by a running *commit ID*. During Phase 2 active development of PXD configuration and optimization was ongoing and a number of changes with significant implications for the operation were applied over time. Table 6.1 lists the significant configuration changes during the Phase 2 run. It omits commits with minor maintenance changes such as regular $V_{\text{gate-on}}$ compensation.

run	configDB commit ID	configuration change
	32	
1866	81	Use pedestal compression
1869	82	Increase BWD module gains ($I_{\text{source}} \approx 50$ mA)
1936	83	Increase IB gain ($\Delta_{\text{gate-on}} = -350$ mV)
2320	90	Change IB biasing: HV -50 V→ -60 V, clear-off 2 V → 4 V, drift -5 V→ -3 V
2404	91	DHP latency set to 51 (gates), trigger window set to 200 gates (trg_len=1593)
2708	99	ACMC off → on
3337	102	DHE timeout 9216 → 2000 GCK
6156	129	DHP pedestal offset bug workaround

Table 6.1: Major configuration changes of the PXD modules.

Voltage Configuration

The voltage settings during Phase 2 correspond largely to the nominal voltages. All voltages and currents of the four modules towards the end of Phase 2 are given in Table 6.2. dcd-dvdd, dhp-core, and dhp-io can be seen to be set to slightly higher than nominal voltages for IF, OF, and OB modules. This is due to the digital GND sensing issue described above. The IB module was running with a lowered voltage in comparison, which was chosen because it enabled a stable data link connection.

DHP configuration

The important DHP parameters and their settings during Phase 2 are given in Table 6.3. Especially noteworthy are the latency and threshold settings. The latency will be discussed in detail below.

DCD configuration

The main DCD settings for all modules are given in Table 6.4. They largely correspond to the optimum values found in the laboratory measurements of demonstrator systems. In the preparation of Phase 2 the optimization on module level was not yet developed.

PS channel	IF		IB		OF		OB	
	voltage [mV]	current [mA]	voltage [mV]	current [mA]	voltage [mV]	current [mA]	voltage [mV]	current [mA]
sw-sub	-7000	-9	-7000	-9	-7000	-10	-7000	-9
sw-dvdd	1800	15	1700	19	1900	15	1800	14
sw-refin	-5200	0	-5300	0	-5100	0	-5200	0
dcd-amplow	275	-674	275	-702	275	-698	275	-694
dcd-avdd	1800	2490	1800	2596	1800	2550	1800	2613
dcd-dvdd	1900	737	1700	782	1900	706	2000	764
dcd-refin	725	248	725	228	725	232	725	287
dhp-core	1400	632	1150	653	1500	639	1400	583
dhp-io	1900	263	1700	279	1900	244	2000	259
bulk	10000	0	10000	0	10000	0	10000	0
clear-on	19000	27	19000	27	19000	25	19000	24
clear-off	5000	-21	2000	-21	5000	-19	5000	-18
gate-on1	-2960	-6	-3290	-6	-2740	-5	-2890	-5
gate-on2	-2960	-5	-3290	-6	-2840	-5	-2790	-5
gate-on3	-2960	-5	-3290	-6	-2940	-5	-2890	-5
gate-off	3540	22	3460	25	3760	23	3810	22
source	6000	50	6000	67	6000	52	6000	48
ccg1	0	0	0	0	0	0	0	0
ccg2	0	0	0	0	0	0	0	0
ccg3	0	0	0	0	0	0	0	0
hv	-70000	4	-50000	-17	-64000	1	-66000	0
drift	-5000	0	-5000	0	-5000	0	-6000	0
polycover	0	0	0	0	0	0	0	0
guard	-5000	0	-5000	0	-5000	0	-5000	0

Table 6.2: Set voltages and currents of all four modules on 2018-07-01 09:58 JST at the start of run 4956

6.2.2 Trigger Timing Measurement during Cosmic Run

Before turning on the accelerator, the Belle II subdetectors took data measuring cosmic muons originating from highly energetic cosmic particles interacting with the atmosphere. They traverse the experimental hall and the detector in relatively straight paths due to their energy and mass. Since they are charged they leave ionization signals in the detectors and their tracks are used for testing the common DAQ chain, trigger and track reconstruction. The results are used for alignment by measuring the position of the sensors with respect to each other and in the Belle II coordinate system.

For the PXD this mode of data taking can be used to determine the optimal trigger window. Due to the rolling shutter read-out of the matrix (Section 3.1.4) the effective 20 µs time frame contained in each read-out is shifted by ≈ 100 ns per read-out row. Therefore, the timing of the read-out has to be chosen so that the event of interest is contained in the signal-integration window of all rows. A schematic visualization of the read-out timing is given in Fig. 6.6.

The trigger signal is generated in the outer detectors and is issued to the PXD to prompt a read-out. The read-out of the other detectors, the processing of the trigger decision and the propagation of the

register	setting
latency	51
last_row	191
last_row_dump	191
frame_sync_proc_dly	65
row2_sync_dcd_clk_dly	2
pedestal_subtraction	1
pedestal_offset	0
active_ped_mem	1
cm_correction_en	1
cm_use_dcd_chan_mask	1
cm_use_overflow_bit	0
cm_offset	0
threshold	7
offset_frame_sync_dly	0
offset_des_dly	7
offset_en_out	0
dcd_row2_sync_dly	0
pll_cml_dly_sel	0
idac_cml_tx_bias	130
idac_cml_tx_biasd	255
iref_trimming	8

Table 6.3: Main DHP settings in Phase 2.

trigger signal to the DHH all take time. The resulting total delay between the event and trigger signal is called latency. It has to be taken into account when reading out data from the PXD so that the correct signal-integration window is assigned to each event.

PXD Setup for Cosmics Run

The decisive parameter in the DHP is a register called latency, which determines which data are sent out. Data are continuously written into the DHP data memory, as they arrive from the digitization in the DCD. The latency register decides the difference between the write pointer, pointing to the memory region of the currently active read-out row, and the read pointer. The difference is specified in number of read-out rows.

On DHH side two trigger parameters can be set: *trg_dly* inserts an additional delay before the DHH sends arriving triggers to the module. This functionality is generally not used, and the parameter is set to zero. The parameter *trg_len* specifies the trigger length in units of the Global ClocK signal (GCK). The DHP trigger mechanism is level sensitive, therefore the DHH has to issue the trigger command for the duration of the active trigger. Each command cycle on the TRiGger line (TRG) defines the trigger for one read-out row, i.e. effectively eight GCK. Due to specifics in the DHE firmware during Phase 2, *trg_len* has to be set according to the following formula:

$$\text{trg\_len}_{\text{GCK}} = n_{\text{read-out rows}} \times 8 - 7 \quad , \tag{6.1}$$

register	setting
dacipaddout	0
dacifbpbias	[[70, 75, 70, 70], [70, 75, 70, 70], [70, 75, 70, 70], [70, 75, 70, 70]]
dacipsource	70
dacipsource_middle	67
dacipsource2	70
dacipdac	[[11, 11, 13, 15], [22, 17, 21, 25], [14, 14, 12, 14], [16, 12, 12, 14]]
dacvnsubin	[[20, 21, 21, 23], [30, 29, 31, 31], [22, 22, 23, 22], [25, 22, 19, 19]]
dacvnsubout	[[35, 35, 35, 15], [35, 35, 35, 35], [30, 20, 0, 0], [30, 30, 30, 30]]
dacipaddin	0
encmccap	0
amplowshort	1
encap0	1
encap1	1
encap2	1
pulldownvdc	0
en30	0
en60	0
en90	1
pulldowncmc	1
lvds_current	1
lvds_threshold	1

Table 6.4: Main DCD settings in Phase 2.

where $n_{\#\text{ of read-outrows}}$ is the number of read-out rows on the sensor. That means, to read out 192 read-out rows, it is set to 1529.[1]

To make sure the triggering particles are contained in the read-out without knowing the actual latency beforehand, the PXD trigger was set to two full frames, i.e. 384 read-out rows, and the latency was set high to 100 read-out rows, i.e. about 10 µs. Additionally, to be able to determine the start of the read-out frame from the data, one pixel in each read-out row was assigned to send a hit in read-out. This is achieved by setting the pedestal value to zero. Consequently, if the actual pedestal value of the pixel is larger than the threshold, the DHP hit finder will treat it as a hit and send out the data. The list of parameters used during cosmics runs is:

- commitid = 42
- trg_dly = 0
- trg_len = 3065
- frame_timeout = 4608
- latency = 100
- pedestal_offset = ?

[1] The formula changed for the final system used in phase 3.

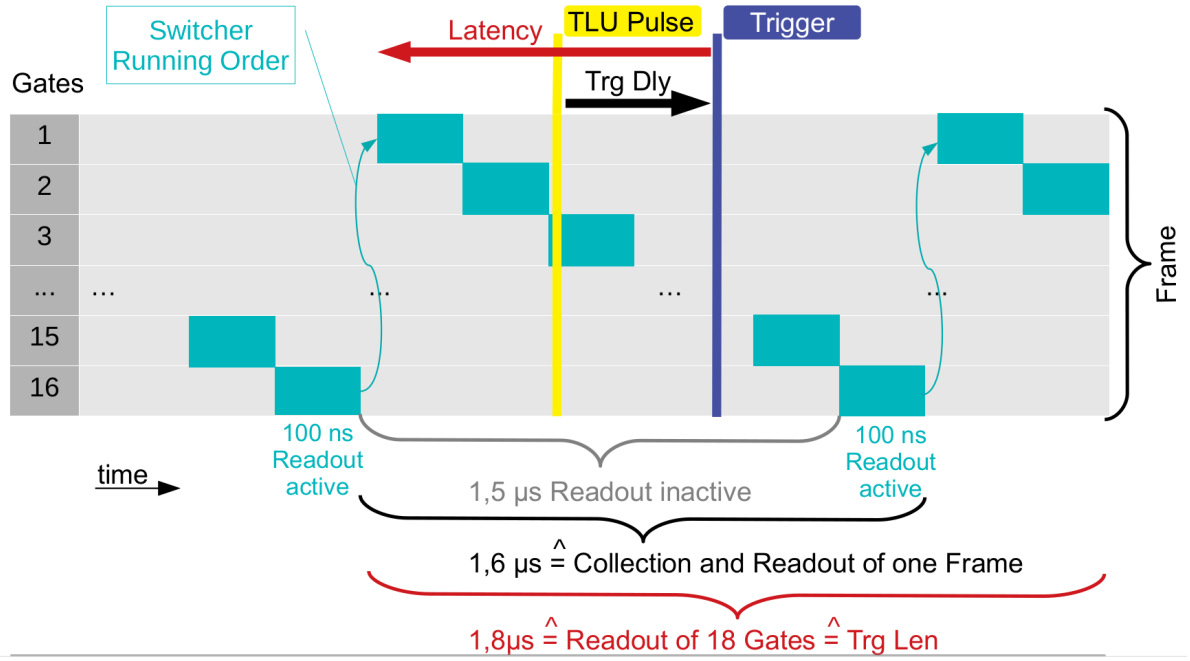


Figure 6.6: Schematic of the PXD sensor readout timing [51].

Results of the Cosmics Run

From the local PXD data we assume that all pixel hits with charges greater than a certain threshold originate from cosmic muons. The read-out position of the hit relative to the start of the read-out frame is then histogrammed for all observed hits. Since the start of frame should be randomly distributed with respect to the trigger and the location of the hit along the sensor should be randomly distributed, the distance of the hit with respect to the first read-out row should be randomly distributed within a window of 192 read-out rows.

The results are shown in Fig. 6.7. According to these results the DHP latency was adjusted to 51 read-out rows and the DHE trigger width to 1594 GCK, i.e. 200 read-out rows, for the remainder of Phase 2, as can also be seen from Table 6.1. These settings allow for some trigger jitter on top of the expected trigger window size of a single frame, i.e. 192 read-out rows.

6.2.3 Trigger Mismatch

The final PXD runs with the possibility to record overlapping triggers. Since the read-out of the entire sensor takes $\sim$ 20 µs the data for individual events overlap if the trigger frequency surpasses $\sim$ 50 kHz. The design average trigger rate of Belle II is 30 kHz, but the minimum separation of events can be lower than 20 µs.

During Phase 2 the DHH firmware did not implement capabilities for overlapping triggers. Instead, data for each event are collected after a trigger arrives until a timeout is reached. The timeout clock starts after the last hit data are received from the modules.

If the next trigger arrives before the event was successfully closed by a DHE, the data of the consecutive event are added to the current frame. This condition leads to a trigger mismatch as the frames of

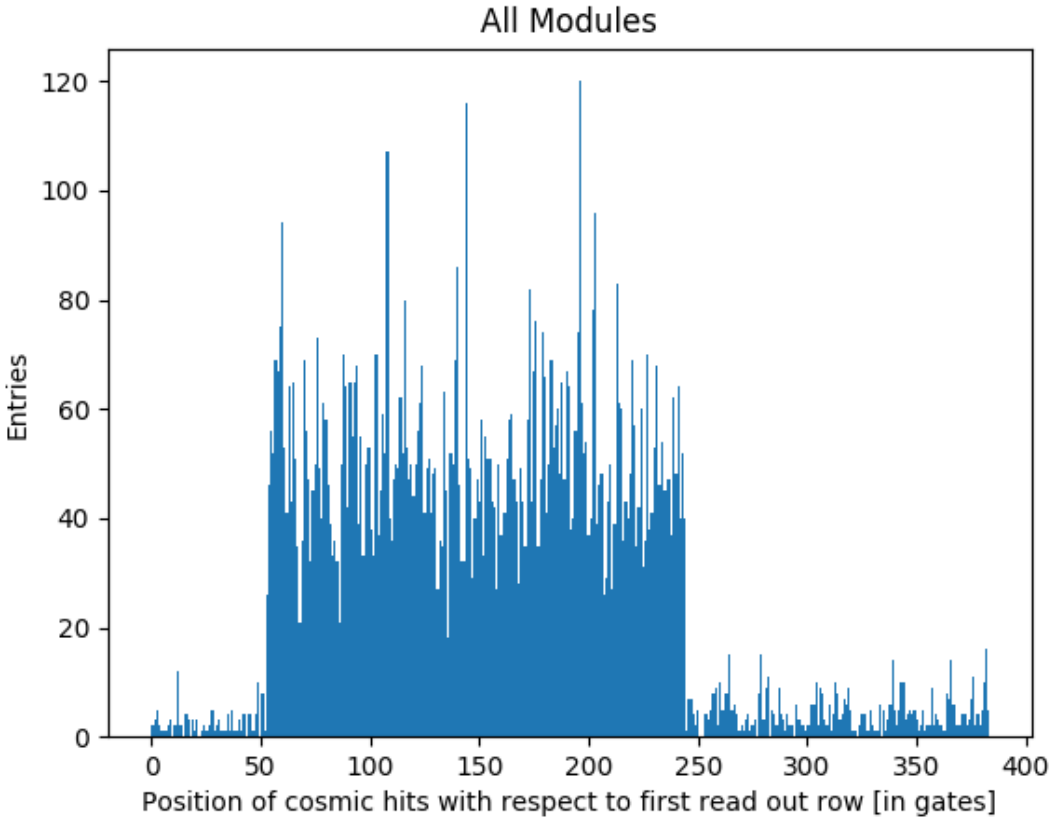


Figure 6.7: Results of cosmics run from 18.03.2018. Position of observed hits with respect to the first read-out row of the frame. The data for all four modules are summed up.

individual DHEs and the DHC are not synchronized anymore. The processing time of an event depends on the time of last arrival of the data as well as the amount of data.

To avoid trigger mismatches in the PXD DAQ a minimum time between triggers, the "trigger holdoff" was set in the FTSW to higher than 200 µs during Phase 2 (the FTSW parameter is call 'max time').

Nevertheless, events with high occupancy could still cause trigger mismatches. Therefore, the timeout length of the DHE (*frame_timeout*) needed to be optimized. The size of *frame_timeout* specifies the DHE internal timeout in units of GCK. Figure 6.8 shows high occupancy events for two different timeout settings. As can be seen the minimum trigger interval is 200 µs as specified by the FTSW setting. The maximum safe amount of hits per module at the shortest trigger interval which does not cause trigger mismatches is marked by vertical lines in the plot. As expected, decreasing the timeout increases the safe threshold for the module occupancy.

After this analysis the parameter *frame_timeout* was set to 2000 GCK for the remainder of Phase 2, as shown in Table 6.1.

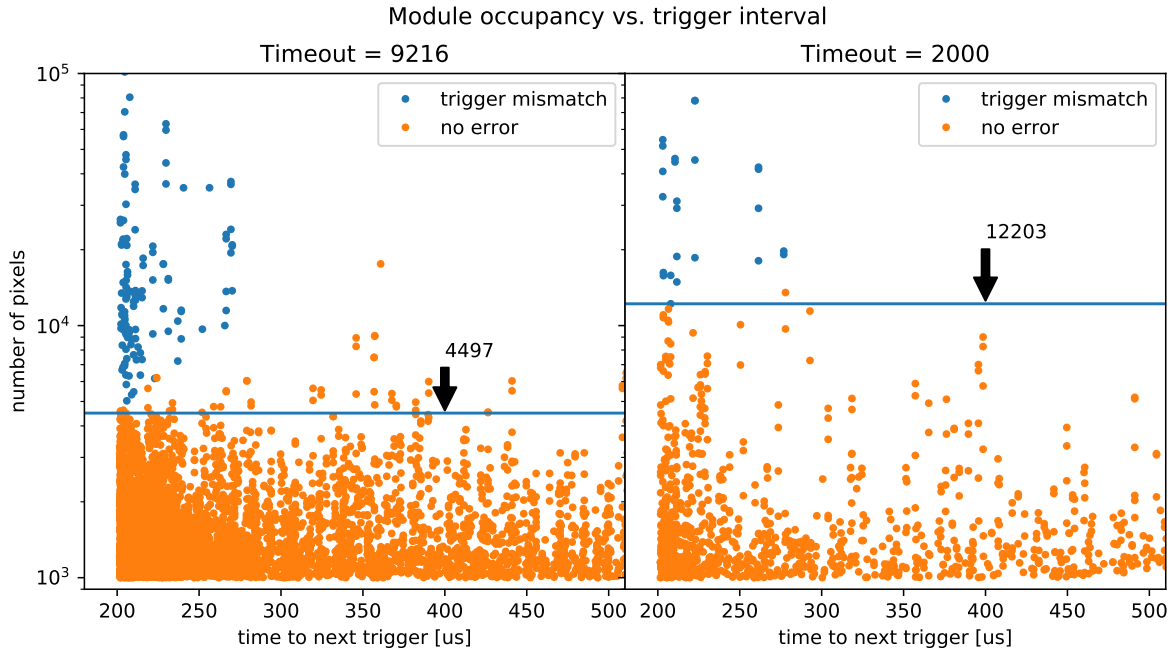


Figure 6.8: Module occupancy vs. trigger interval for events with more than 3000 hits in one module. The orange entries towards the bottom of the plot denote events with successfully built DHH frames. The blue entries denote events with trigger mismatches. Data for two different timeout settings are shown, with a higher setting in the left plot and a lower setting on the right.

6.2.4 Radiation Damage

During the operation of the accelerator all parts of the detector are subject to different levels of radiation. The most accurate estimate of the received dose during Phase 2 was obtained by estimating the dose from the PXD data themselves and extrapolating these results according to the recorded beam conditions over time [34]. This results in an estimated integrated dose of $\approx 2\,\mathrm{kGy}$ for the inner-layer and $\approx 1\,\mathrm{kGy}$ for the outer-layer PXD sensors.

FET Threshold Shift

Most notably ionizing radiation shifts the thresholds of FETs. For the DEPFETs of the sensors the threshold voltages of the main FET and the clear FET become more negative with dose. Laboratory measurements to quantify the threshold drift of PXD modules under X-ray irradiation were executed during the course of this thesis and can be found in [52].

To keep the source currents and signal size of the DEPFETs constant, the voltage $V_{\text{gate-on}}$ was adjusted over the course of the Phase 2 run. The threshold shift of the clear gate was not compensated during the time. Figure 6.9 shows the compensating $V_{\text{gate-on}}$ adjustments over time.

Fig. 6.10 shows the evolution of the source current I_S over time. The gradual decrease with radiation and resets due to $V_{\text{gate-on}}$ adjustments can be seen. During the run there was an adjustment of the gate voltages of the backward modules to adapt their source currents and modify the signal sizes. This change was possible due to improved pedestal optimization, i.e. ACMC and offset correction.

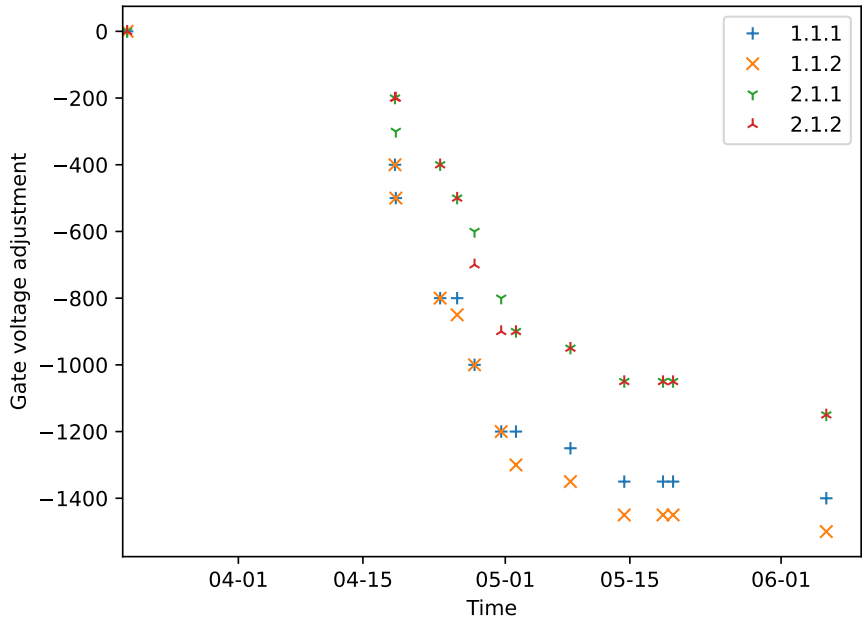


Figure 6.9: Radiation related adjustments of $V_{\text{gate-on}}$ over the course of Phase 2. The four PXD modules are denoted by different colors and symbols.

Pedestal Shift

Even though $V_{\text{gate-on}}$ is compensated, relative pixel shifts can be observed. The received total dose varies across the sensor. Figures 6.11 to 6.14 show the raw pedestals of all modules at the beginning and the end of Phase 2, as well as their difference. All maps use the standard mapping, with row 0 being closest to the DCDs. Since gate adjustments and DCD offset adjustments (vnsubin) took place, the absolute difference does not reflect radiation damage. But the relative pedestal difference within a module shows interesting features. Firstly, the radiation damage at the edge of the module can be seen to be compensated, as expected. This happens, because the rate of pedestal shift slows down with increasing total dose.

All modules display some rows or read-out rows with outlier behavior. The difference between individual DCDs within a module are due to the shifted offsets.

The inner modules seem to have gradients along the length (columns) of the sensors. The total dose appears to be lower at the far ends of the sensors. The IB also shows a round structure between rows 100-200. This could be caused by synchrotron radiation, which is cut off beyond a certain angle.

The OF module shows some unexpected slightly rounded structures along the rows which coincide with structures seen in the pedestals already at the beginning of Phase 2. Therefore, these structures are most likely pre-existing radiation damage or due to other processing variations.

The pedestal shift in all modules exhibits a double-row effect. The pedestal values of alternating double rows appear to shift differently in a pattern, as discussed in Chapter 5.

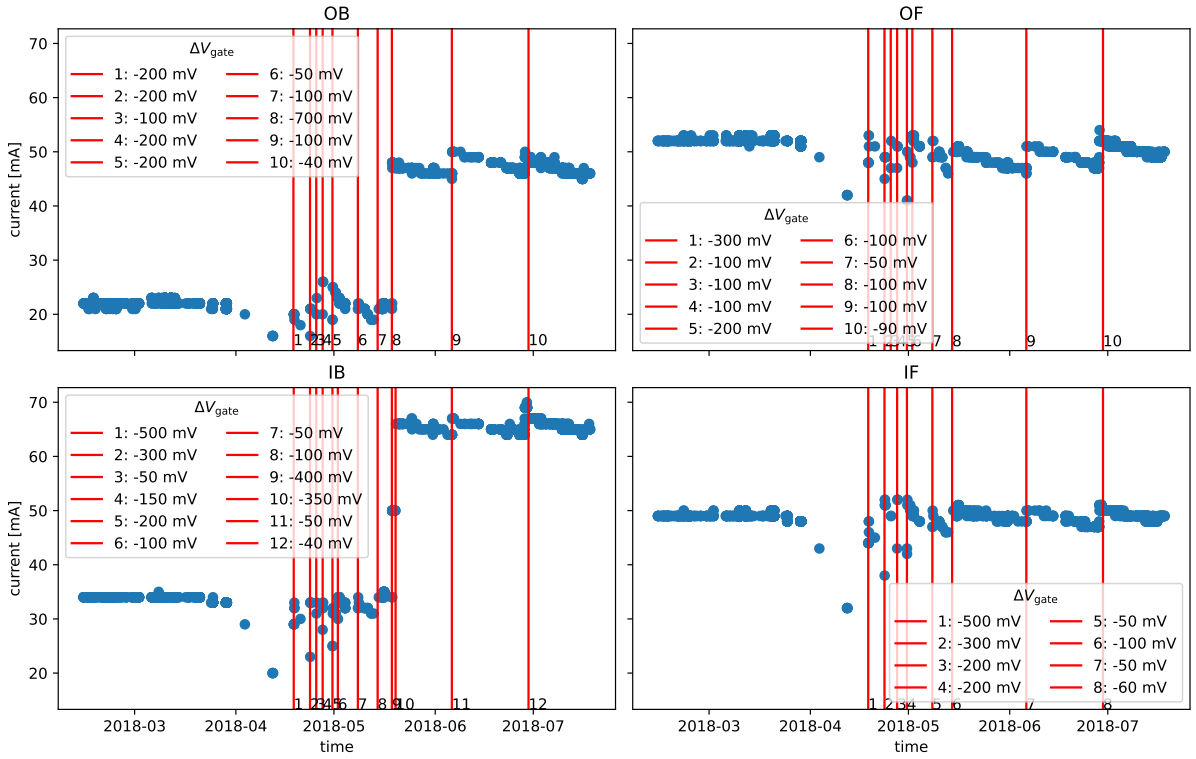


Figure 6.10: Source current of Phase 2 modules over time. Changes of the gate voltages are marked with their respective voltage shifts.

ASIC Currents

The module ASICs are subject to irradiation as well and consequently receive damage. As a consequence, their current consumption is expected to change over time. Figure 6.15 shows the dcd-dvdd current, i.e. the digital supply current of the DCDs for all modules. The start of a continued increase is visible for the two inner modules, which are exposed more directly to the beam radiation as they face towards the beam. The DCDs of the outer modules are shielded by the SCB.

Other ASIC currents did not change notably during Phase 2. But the beginning change of the DCDs supply currents shows that all currents will have to be monitored, and supply limits will have to be adjusted over time. From X-ray irradiation campaigns it is known that the currents stay within tolerable limits and during Phase 3 more experience was collected under final operation conditions.

6.2.5 Conclusion

The PXD operation during Phase 2 demonstrated reliable operation in the final experimental environment for the first time. Several shortcomings in the service hardware could be detected and modified in time for the final detector. Furthermore, the development of optimization and operation procedures and software was to a large extent jump-started and improved during this time. More information about this can be found in [34, 53]. During Phase 2 the PXD supplied valuable live radiation monitoring data as feedback to the accelerator as well. Details of the radiation background studies are found in [45].

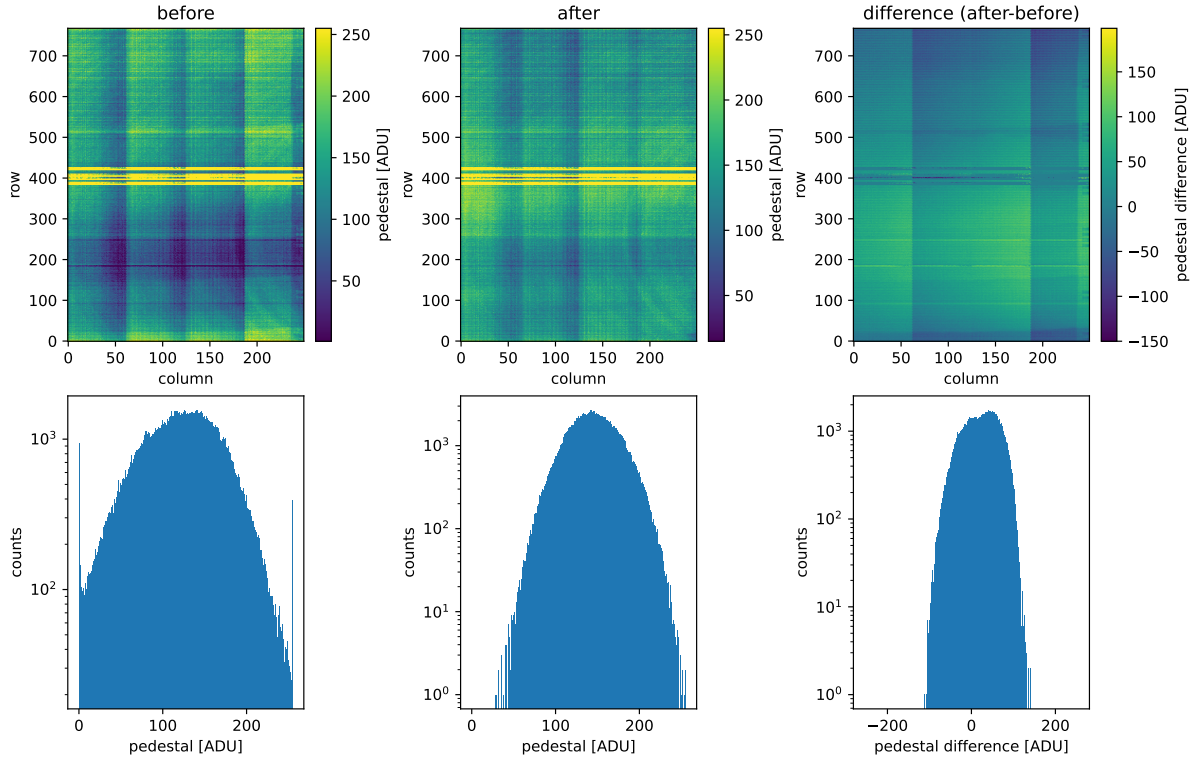


Figure 6.11: Before and after pedestal comparison of IF module W37_IF.

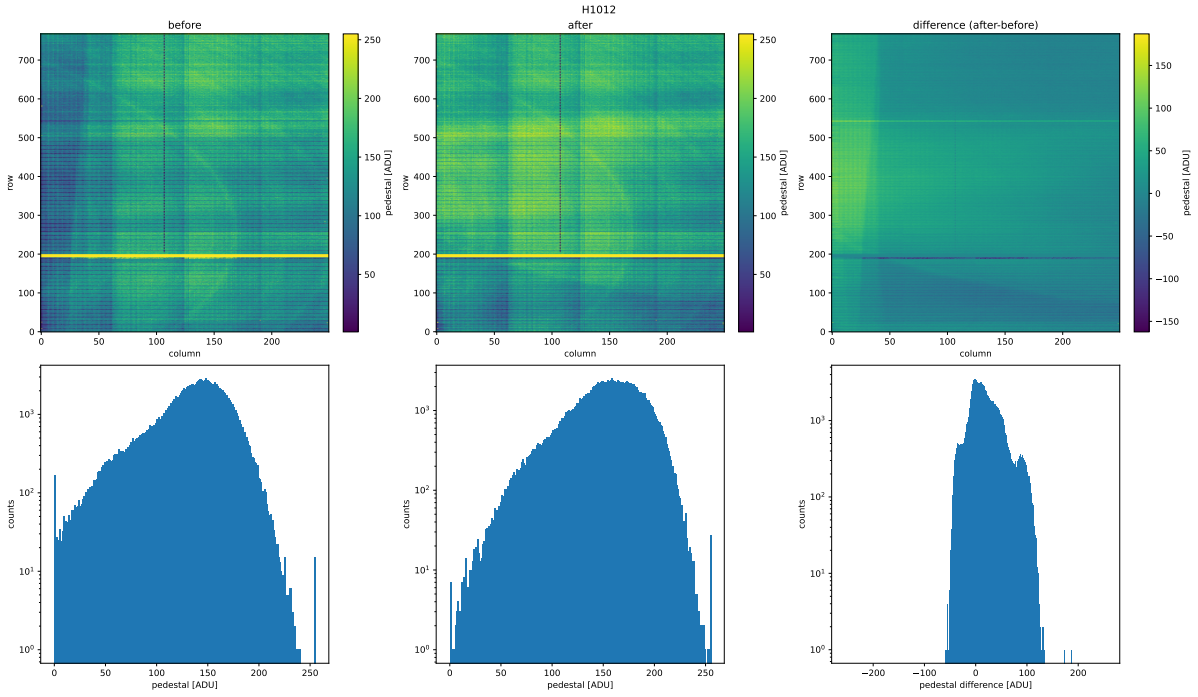


Figure 6.12: Before and after pedestal comparison of IB module W46_IB.

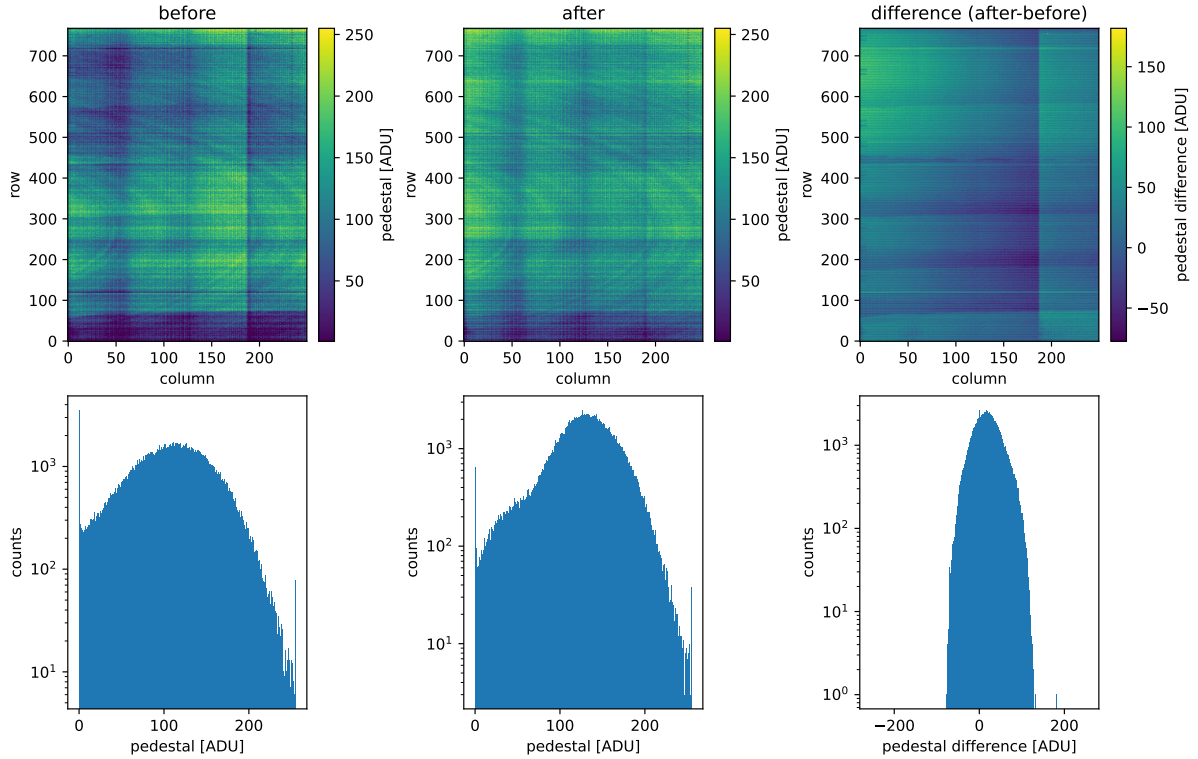


Figure 6.13: Before and after pedestal comparison of OF module W37_OF1.

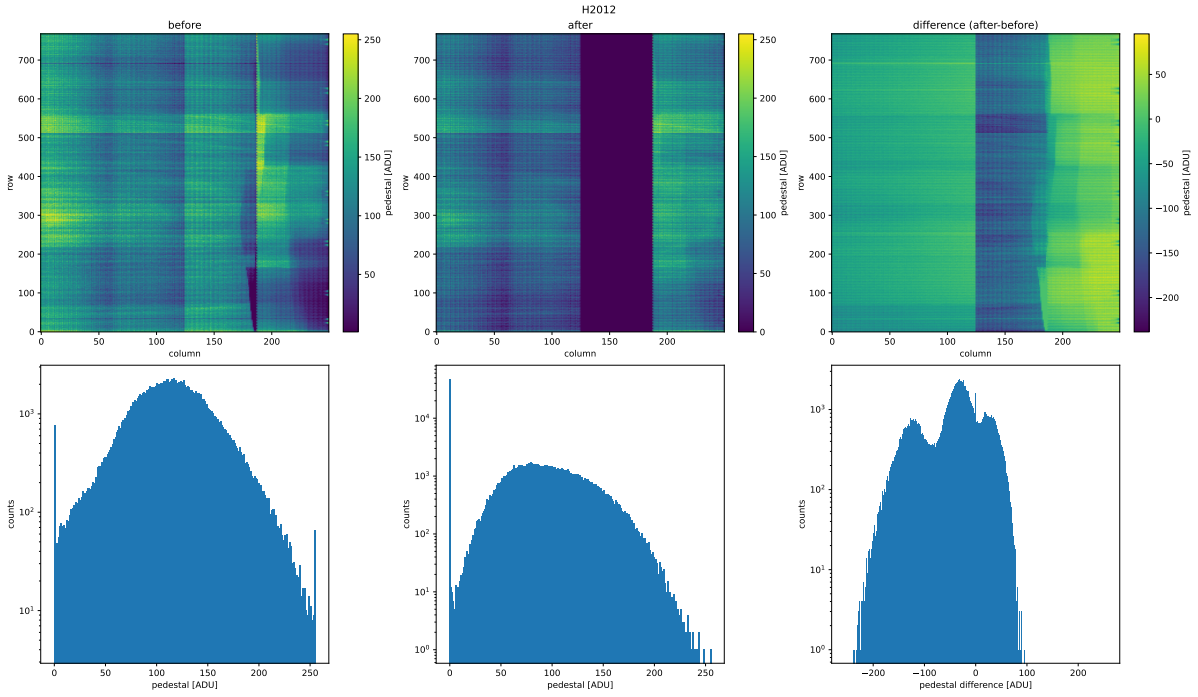


Figure 6.14: Before and after pedestal comparison of OB module W37_OB.

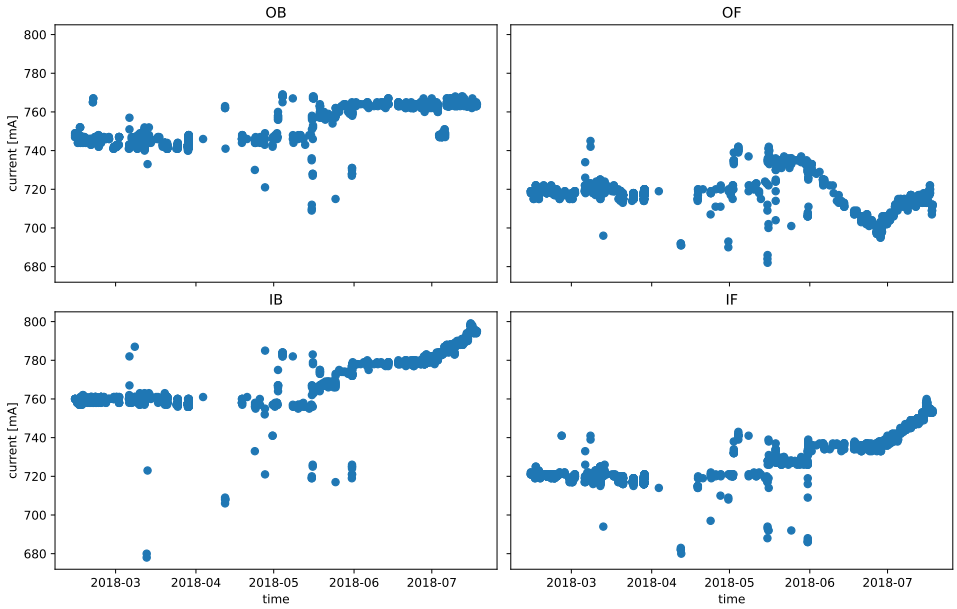


Figure 6.15: dcd-dvdd current of Phase 2 modules over time.

CHAPTER 7

Conclusion

The Belle II PiXel Detector (PXD) detector has the lowest material budget of all High Energy Physics (HEP) pixel detectors. This is made possible through the use of DEpleted P-channel Field Effect Transistor (DEPFET) and a unique self-supporting module concept.

This work investigates the bulk and drain current characteristics of the final modules. The handle-wafer potential was shown to influence the backside currents in an irradiated module. This points to an unforeseen avalanche mechanism near the edges of the back-side implantation that is triggered by charge trapped in the bonding oxide between the wafers.

The drain current distributions have been thoroughly analyzed and contributions from wafer property inhomogeneities, production features and, Application Specific Integrated Circuit (ASIC) channel variations were identified and quantified. Irradiation from X-ray inspection and gate-width variations introduced by Direct Wafer Lithography (DWL) are shown to cause the most significant modifications of currents across the sensors. Drain Current Digitizer (DCD) channel variations contribute gradients on a similar level. Bulk property variations generally contribute smaller fluctuations seen as rings or stripes.

These insights might prove useful for subsequent future DEPFET sensors for other project.

During Phase 2 several problems were discovered which could not have been found beforehand in single-module laboratory operation. They could be overcome and a reliable operation of the reduced system with four modules inside the Belle II detector was demonstrated. This paved the way for the insertion and long-term operation of the final detector.

The first version of the PXD was operated from 2019 to 2022. It featured a reduced configuration with only the inner layer being fully populated with ladders and two additional outer-layer ladders. In 2023, it was replaced by a newly produced fully populated version, called PXD2.

Open questions about the details of the back-side current increases remain and are currently being investigated. Also, the double-row effect observed in the drain current studies warrants further study, as its effect increases with total ionizing dose and becomes more and more challenging to handle by the available optimization procedures.

Overall, the system is expected to be capable of providing high-quality tracking data throughout its lifetime.

APPENDIX A

Pedestal of Wafers 9, 37, 56, 57 and 67

A.1 Raw Pedestals

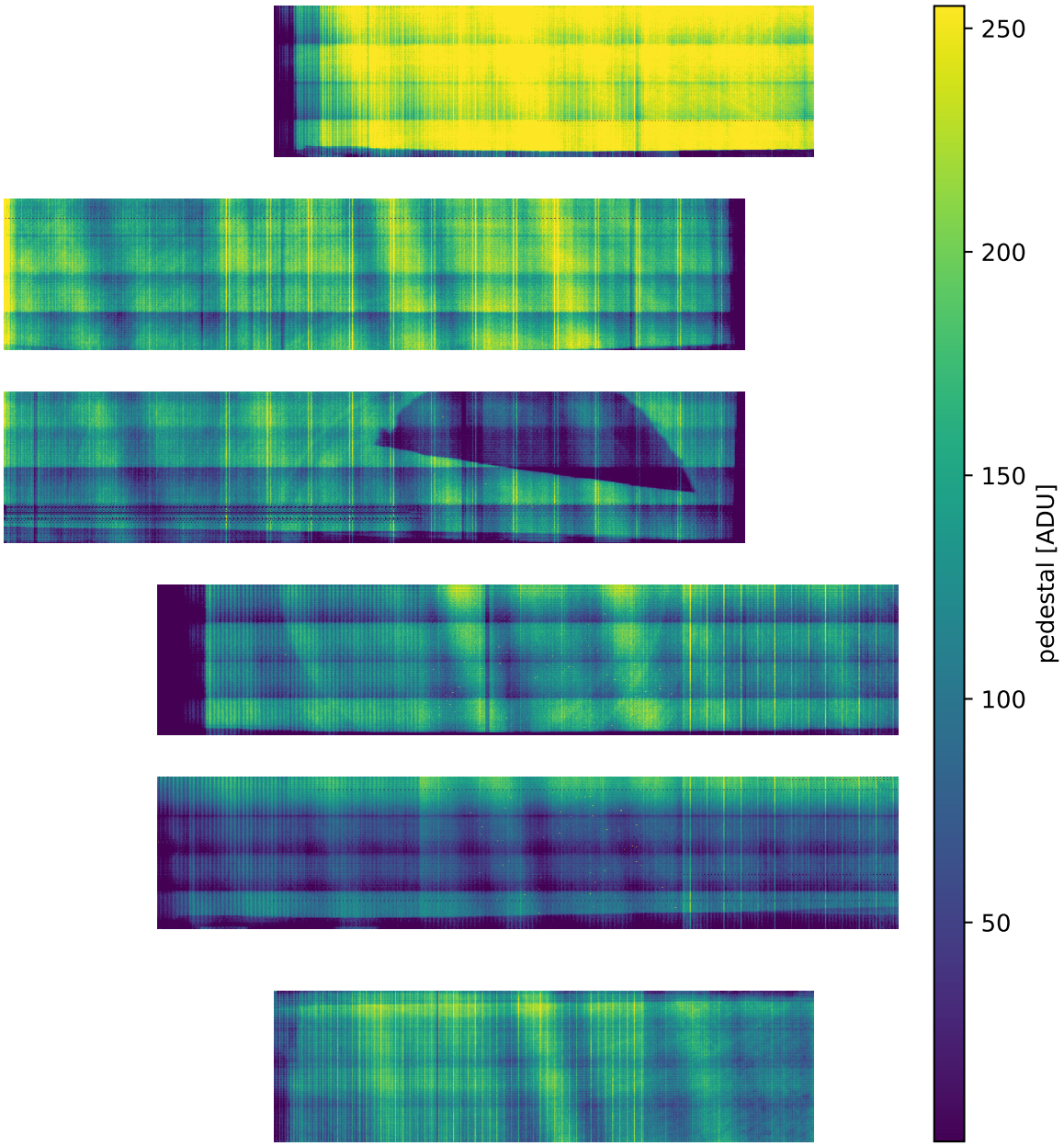


Figure A.1: Raw pedestal maps of modules from wafer 9. The relative position and size of the pixels in this figure corresponds to their position and size on the wafer. The color code denotes the pedestal value in Analog Digital Unit (ADU).

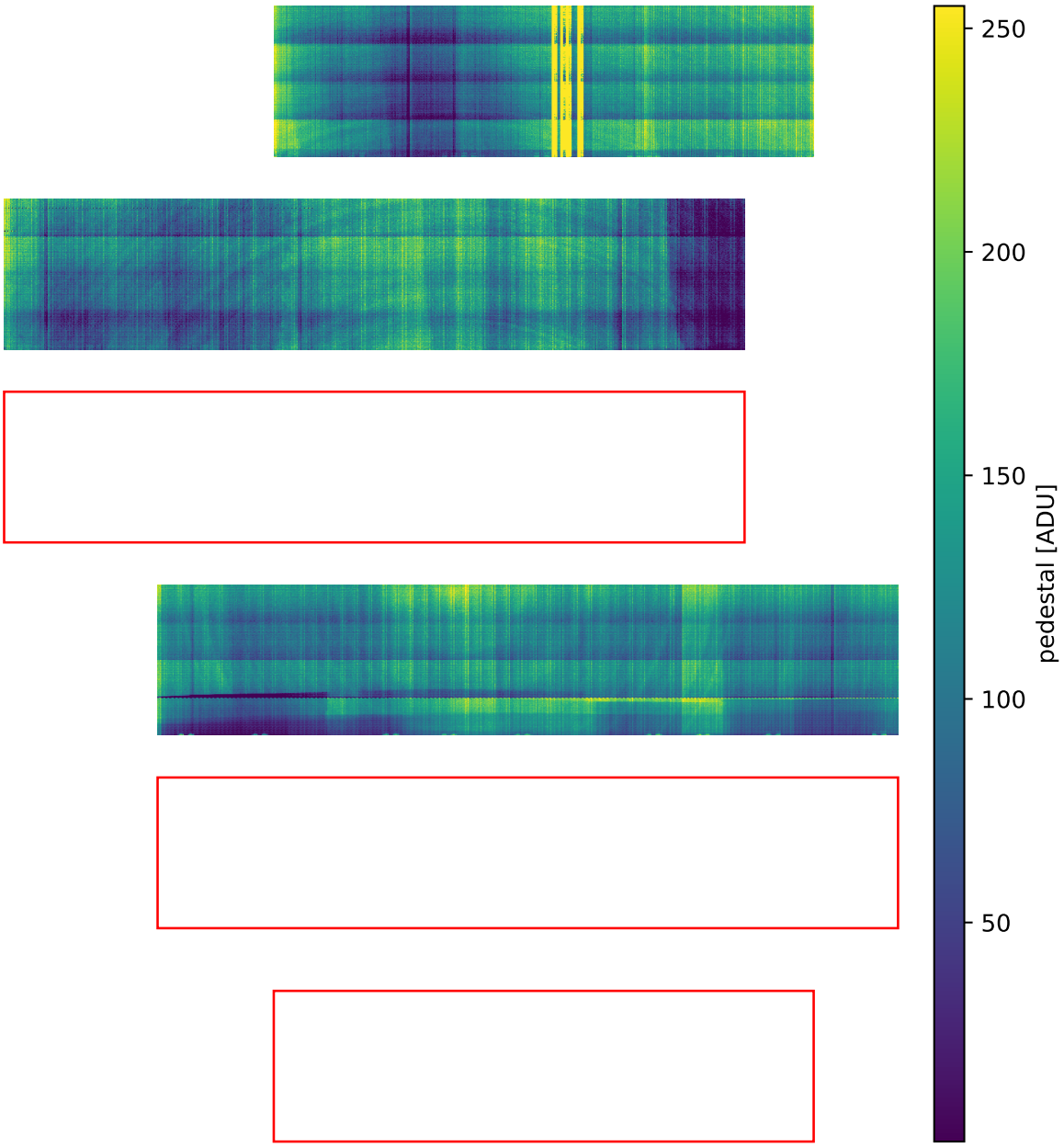


Figure A.2: Raw pedestal maps of modules from wafer 37. The relative position and size of the pixels in this figure corresponds to their position and size on the wafer. The color code denotes the pedestal value in ADU. The red boxes mark the outlines of sensors without measured pedestals.

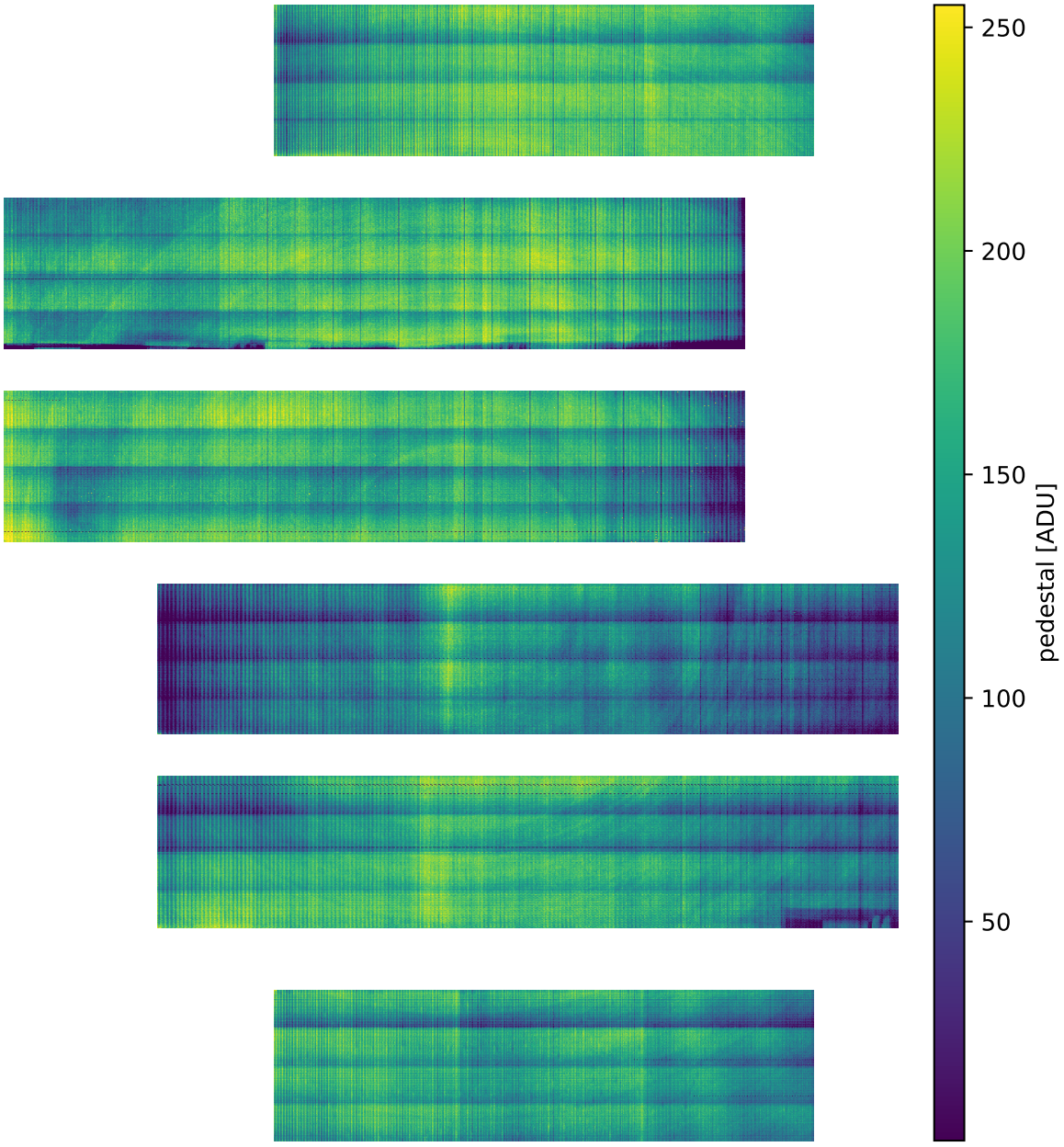


Figure A.3: Raw pedestal maps of modules from wafer 56. The relative position and size of the pixels in this figure corresponds to their position and size on the wafer. The color code denotes the pedestal value in ADU.

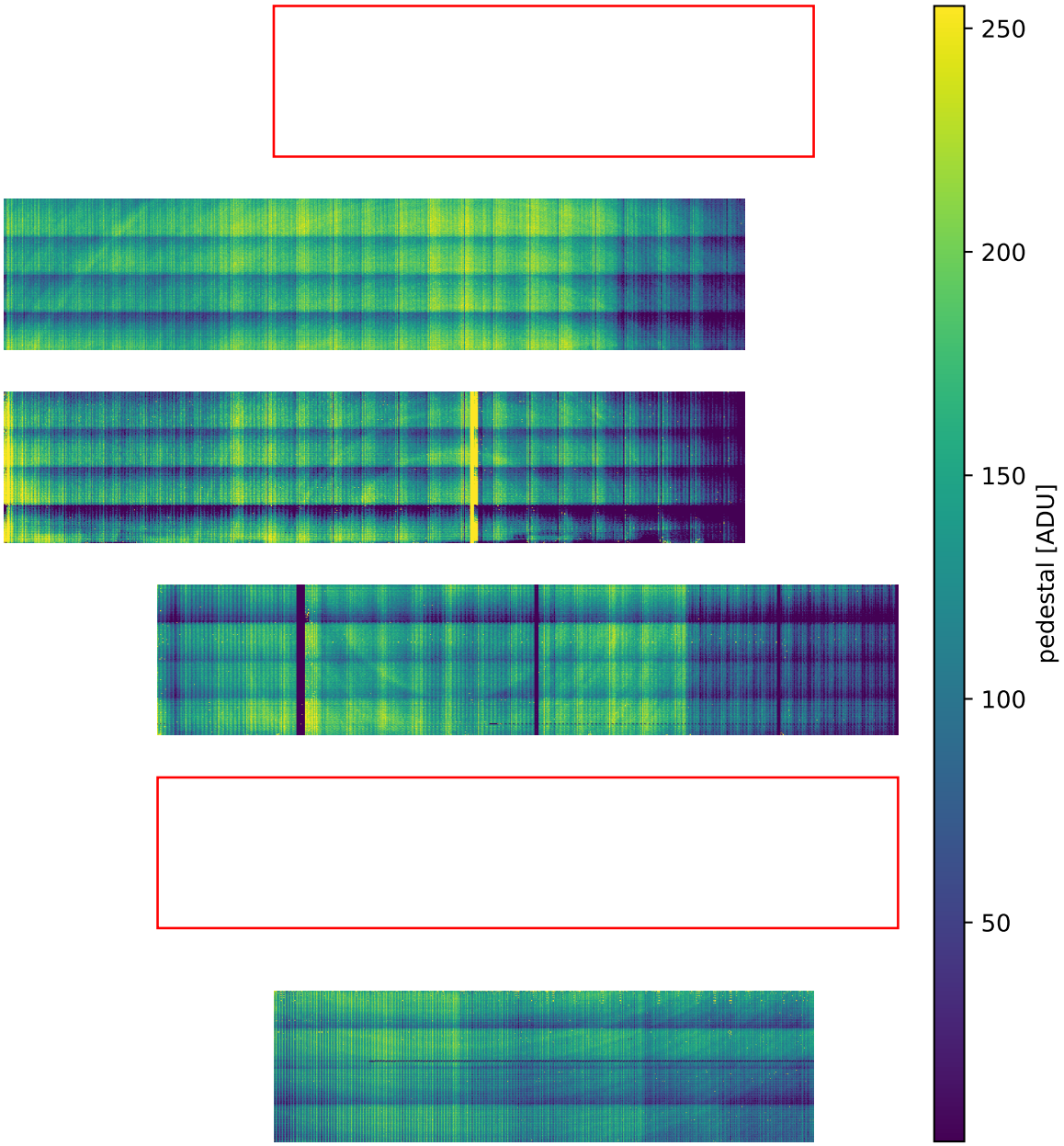


Figure A.4: Raw pedestal maps of modules from wafer 57. The relative position and size of the pixels in this figure corresponds to their position and size on the wafer. The color code denotes the pedestal value in ADU. The red boxes mark the outlines of sensors without measured pedestals.

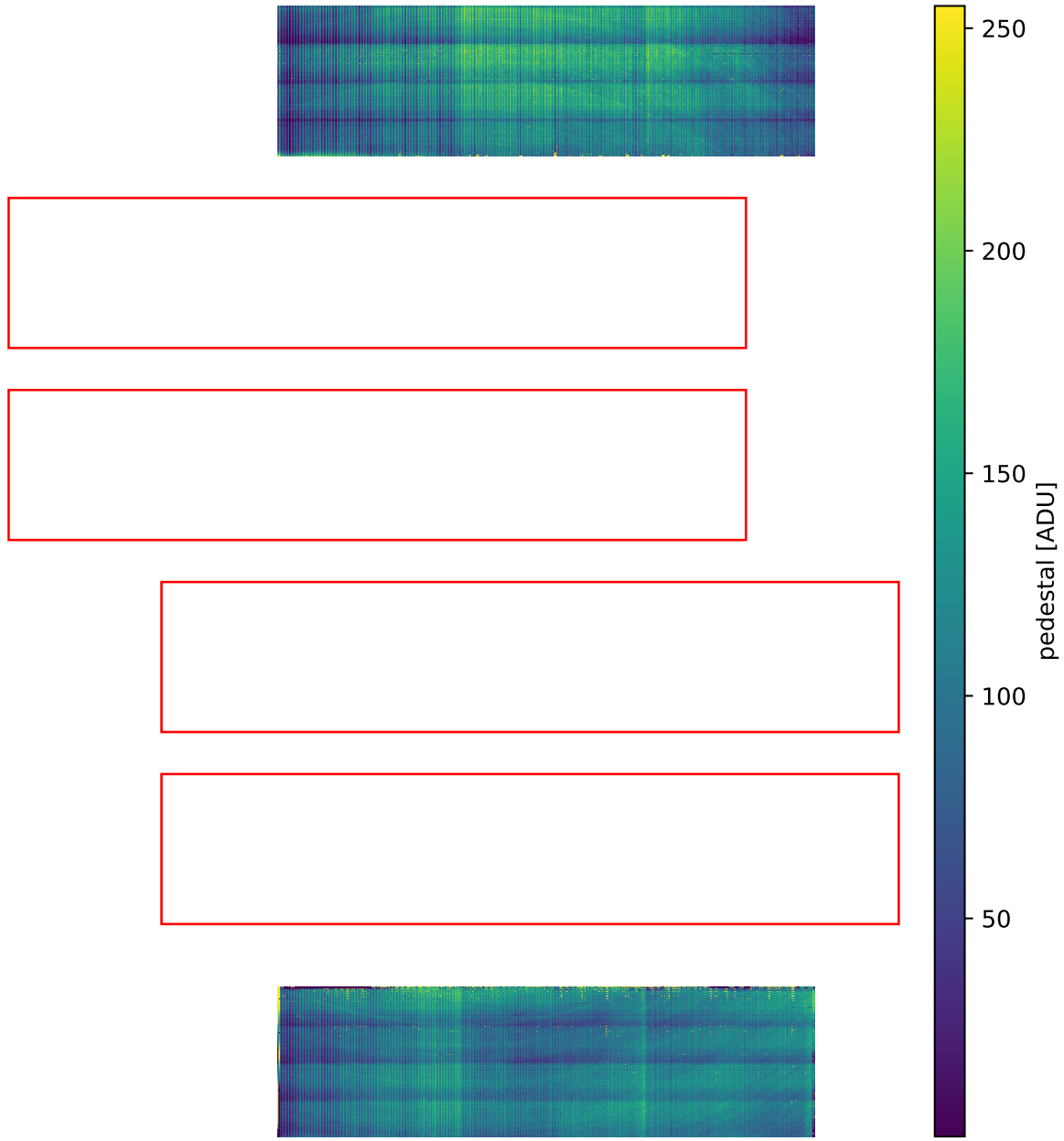


Figure A.5: Raw pedestal maps of modules from wafer 67. The relative position and size of the pixels in this figure corresponds to their position and size on the wafer. The color code denotes the pedestal value in ADU. The red boxes mark the outlines of sensors without measured pedestals.

A.1.1 Recurring Row Pattern Length

W09

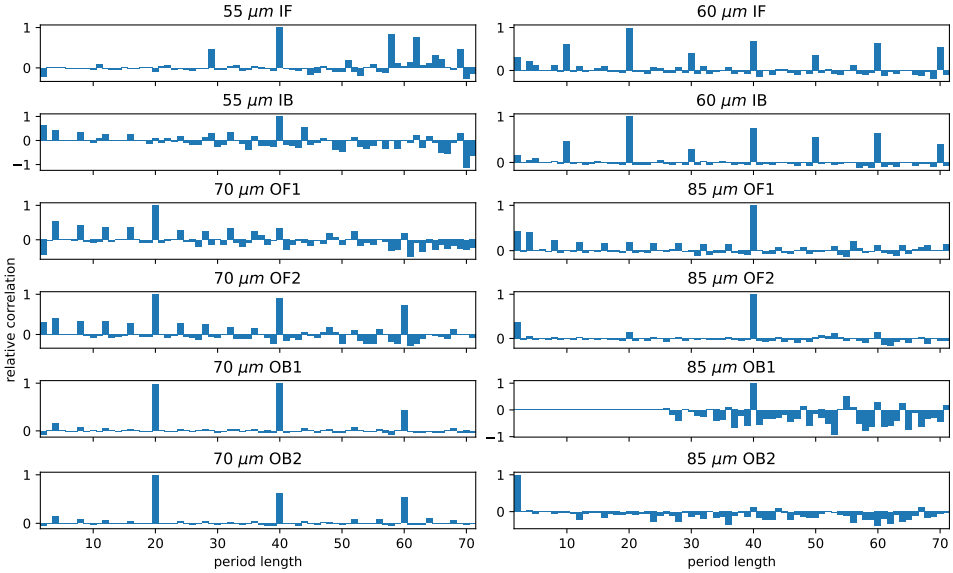


Figure A.6: W09 relative correlation $\hat{r}$ of mean row pedestal sub-samples. For each sensor, both pixel size regions are shown individually.

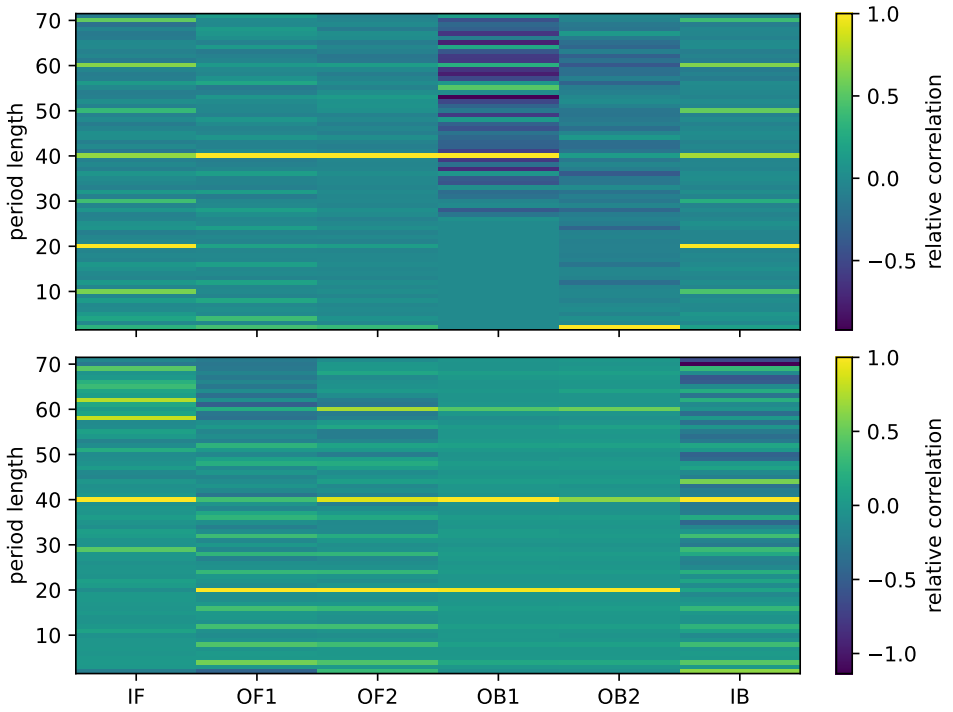


Figure A.7: W09 relative correlation $\hat{r}$ of mean row pedestal sub-samples.

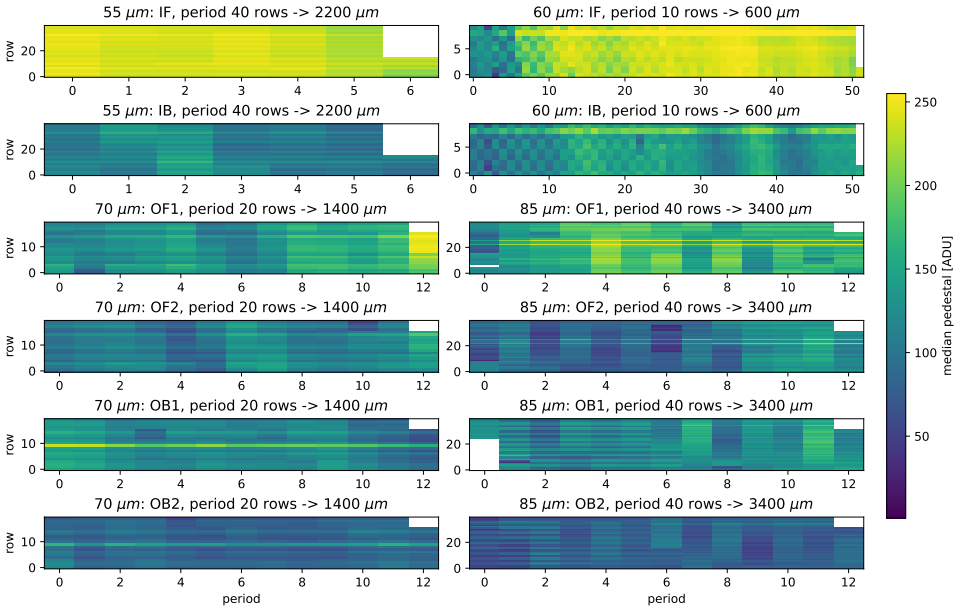


Figure A.8: W09 row sub-samples of n rows. n is given in the title of the respective sub-plot.

W37

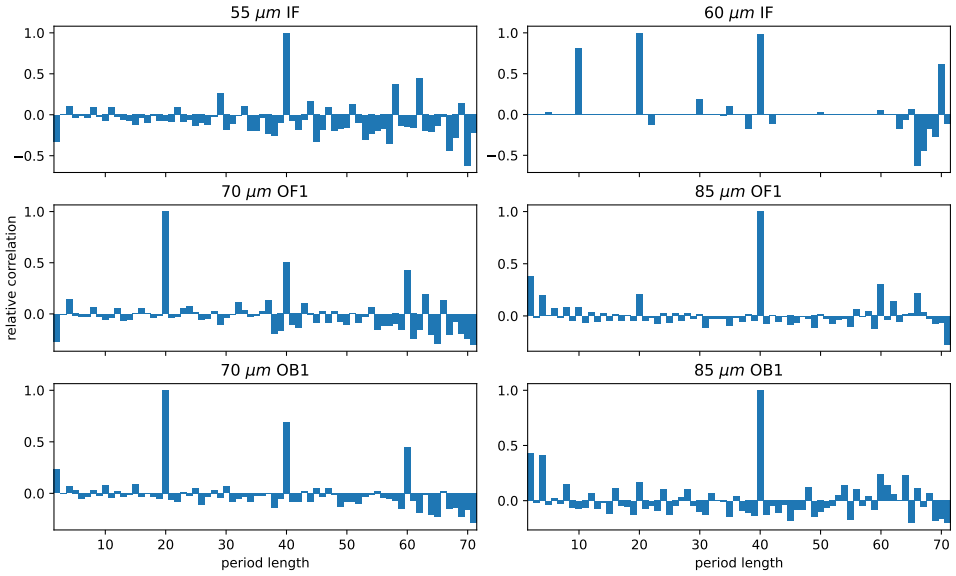


Figure A.9: W37 relative correlation $\hat{r}$ of mean row pedestal sub-samples. For each sensor, both pixel size regions are shown individually.

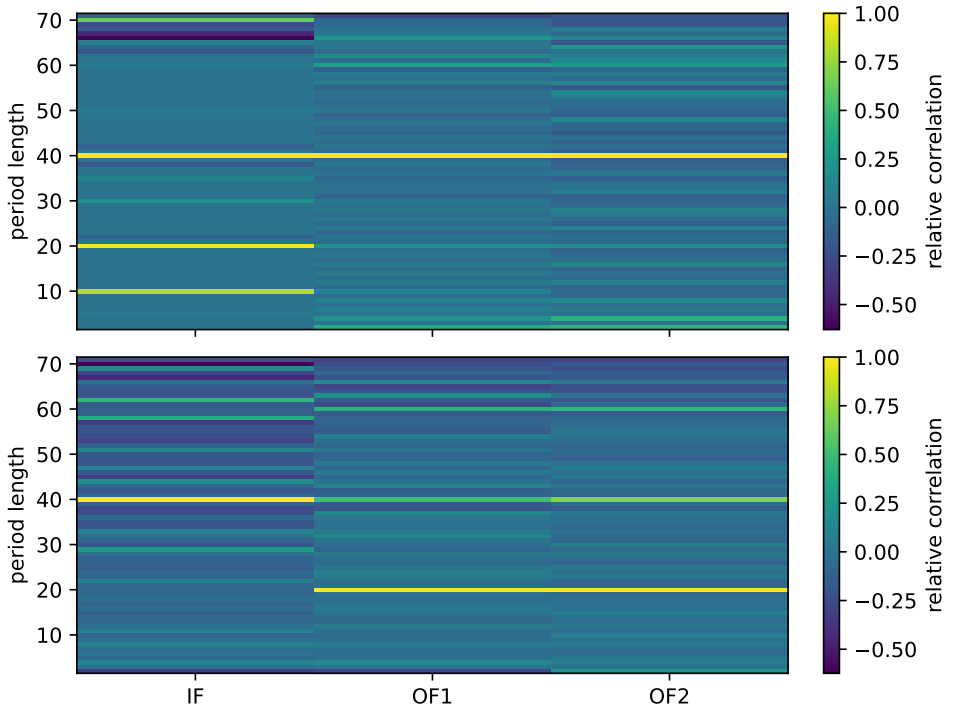


Figure A.10: W37 relative correlation $\hat{r}$ of mean row pedestal sub-samples.

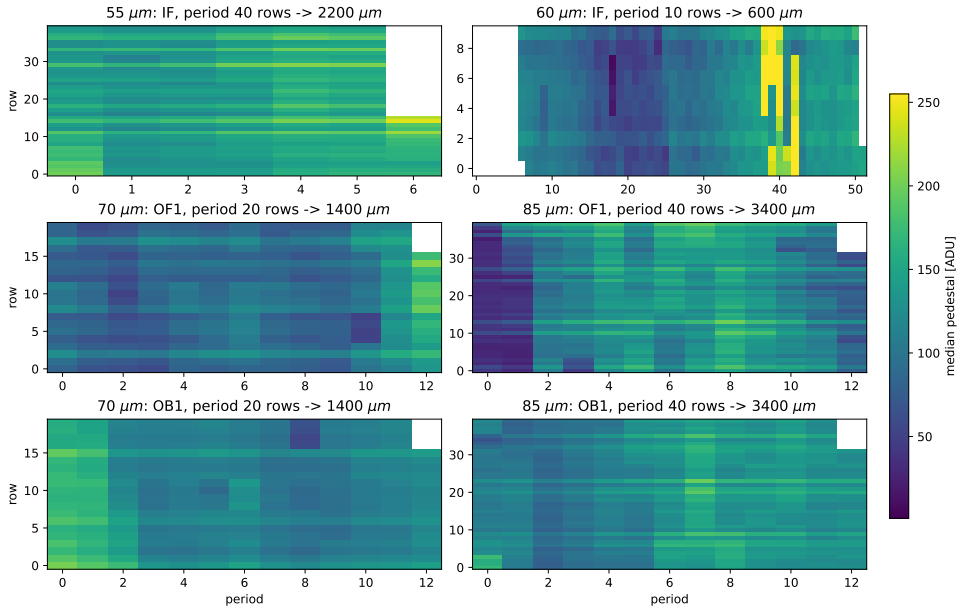


Figure A.11: W37 row sub-samples of n rows. n is given in the title of the respective sub-plot.

W56

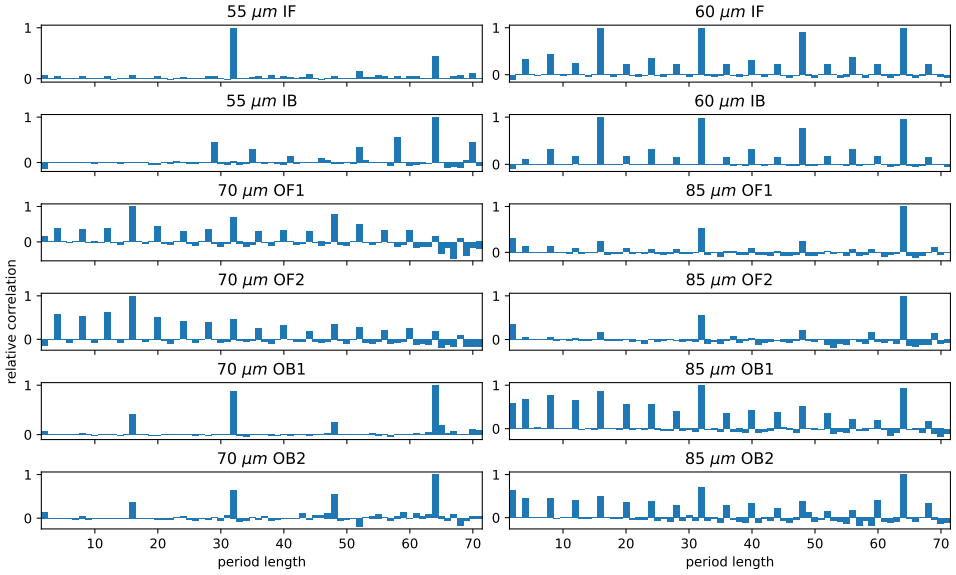


Figure A.12: W56 relative correlation $\hat{r}$ of mean row pedestal sub-samples. For each sensor, both pixel size regions are shown individually.

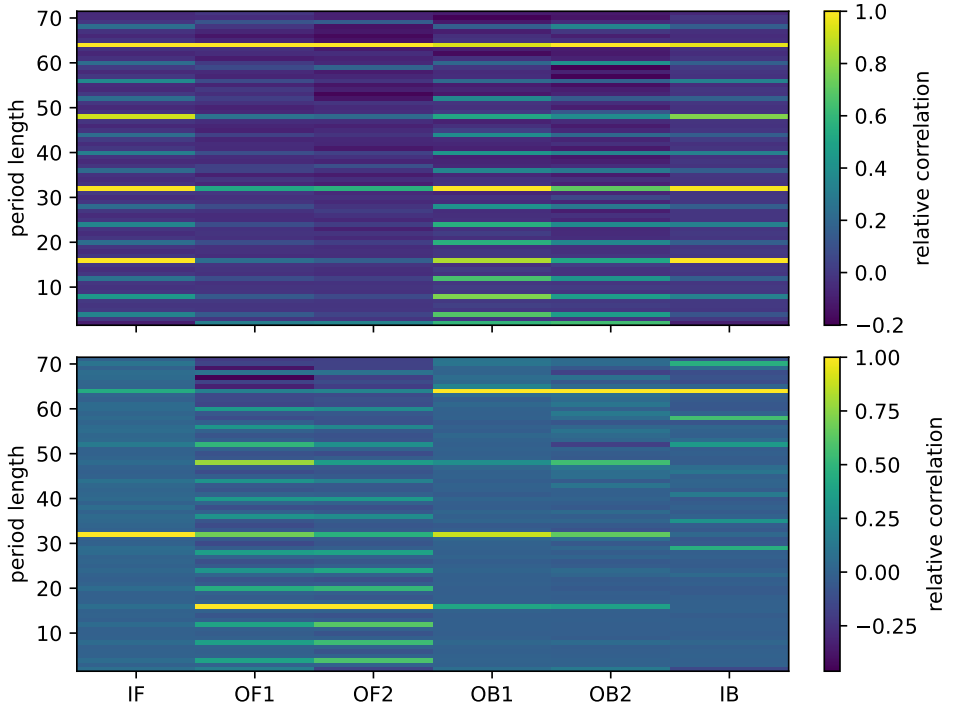


Figure A.13: W56 relative correlation $\hat{r}$ of mean row pedestal sub-samples.

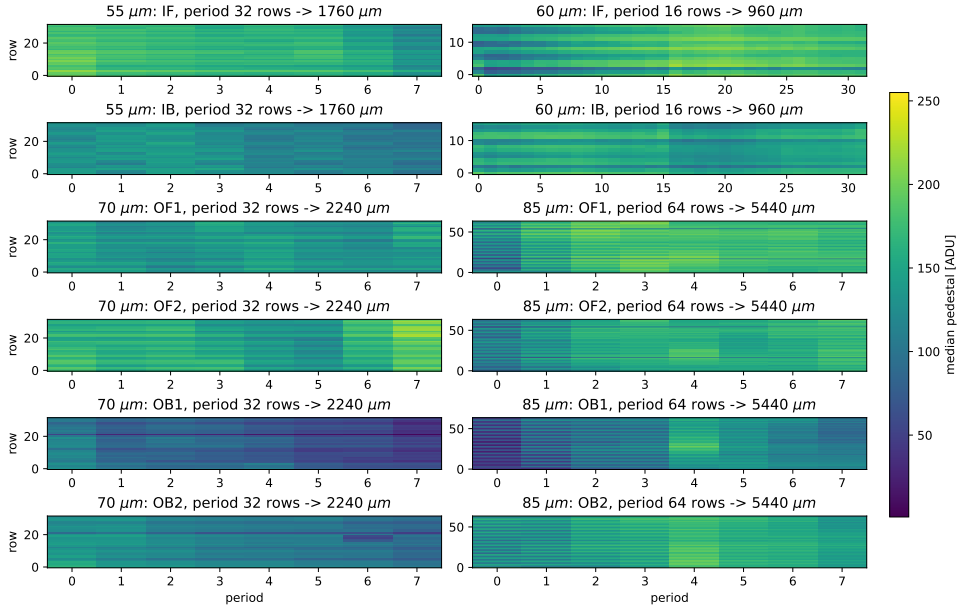


Figure A.14: W56 row sub-samples of n rows. n is given in the title of the respective sub-plot.

W57

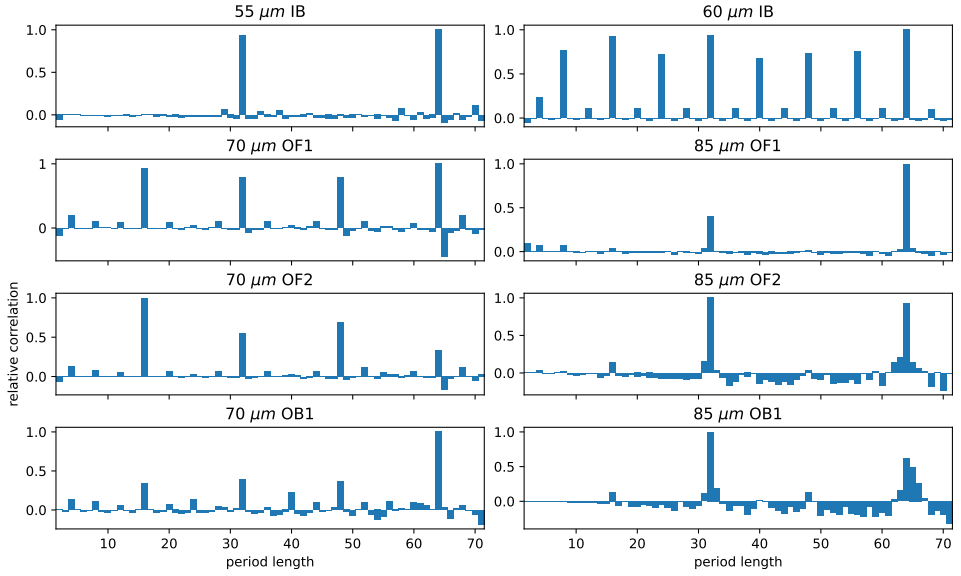


Figure A.15: W57 relative correlation $\hat{r}$ of mean row pedestal sub-samples. For each sensor, both pixel size regions are shown individually.

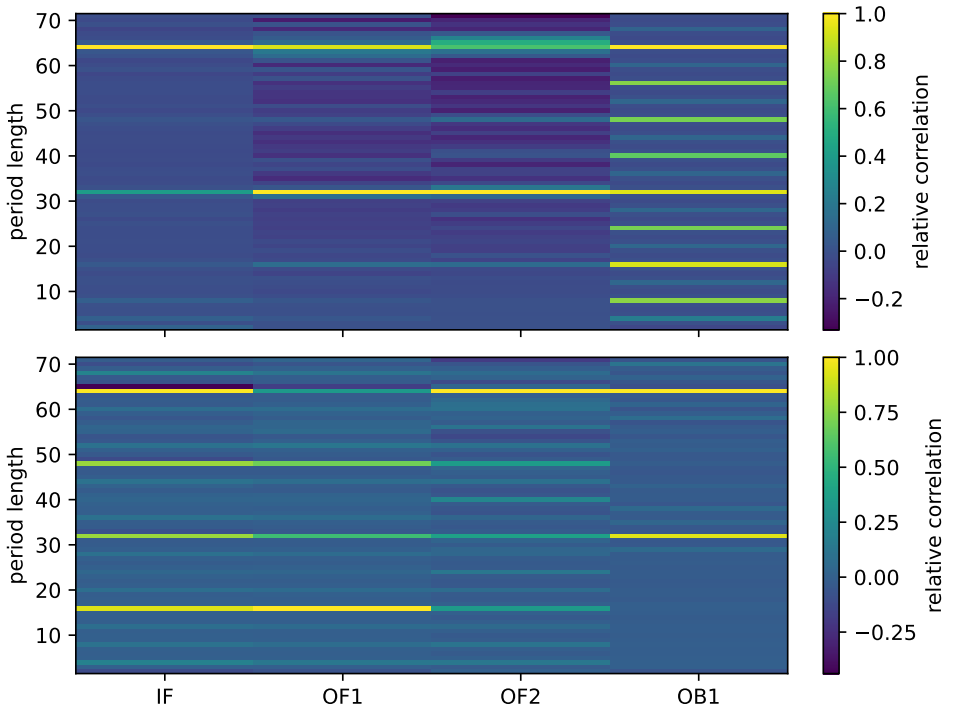


Figure A.16: W57 relative correlation $\hat{r}$ of mean row pedestal sub-samples.

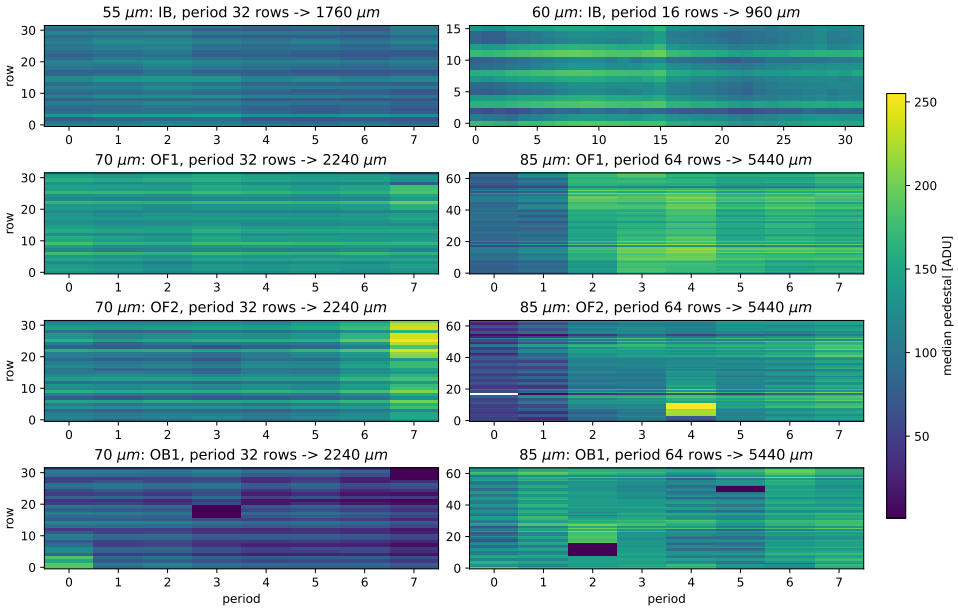


Figure A.17: W57 row sub-samples of n rows. n is given in the title of the respective sub-plot.

W67

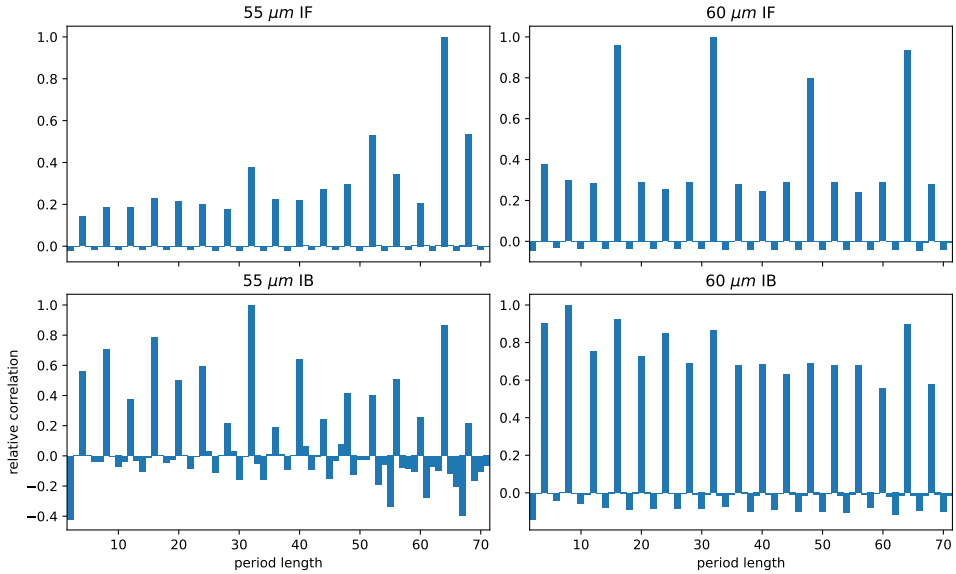


Figure A.18: W67 relative correlation $\hat{r}$ of mean row pedestal sub-samples. For each sensor, both pixel size regions are shown individually.

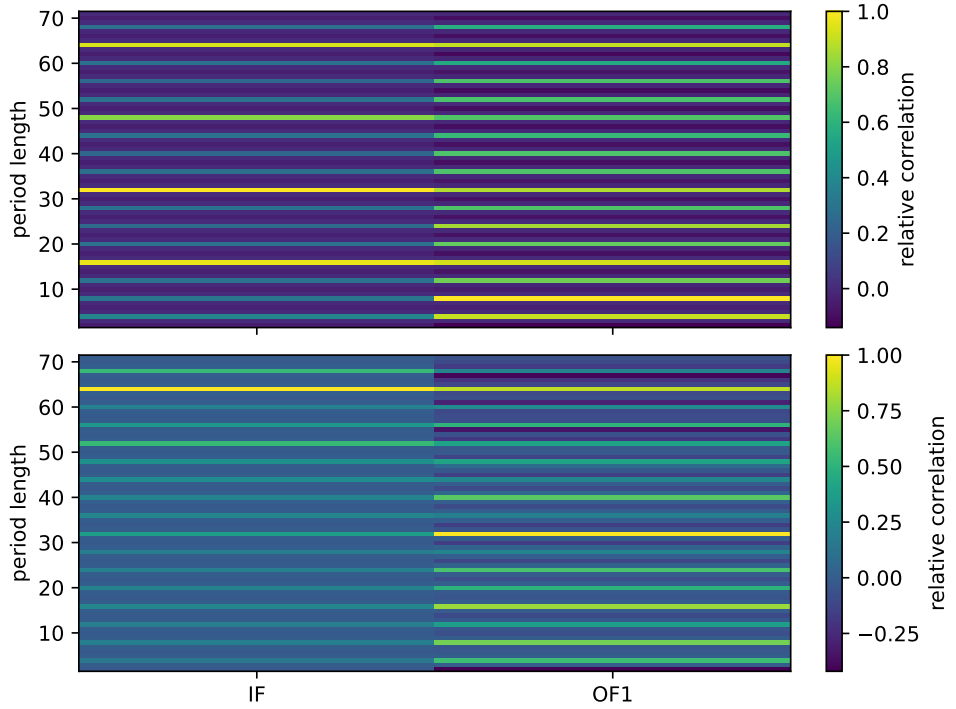


Figure A.19: W67 relative correlation $\hat{r}$ of mean row pedestal sub-samples.

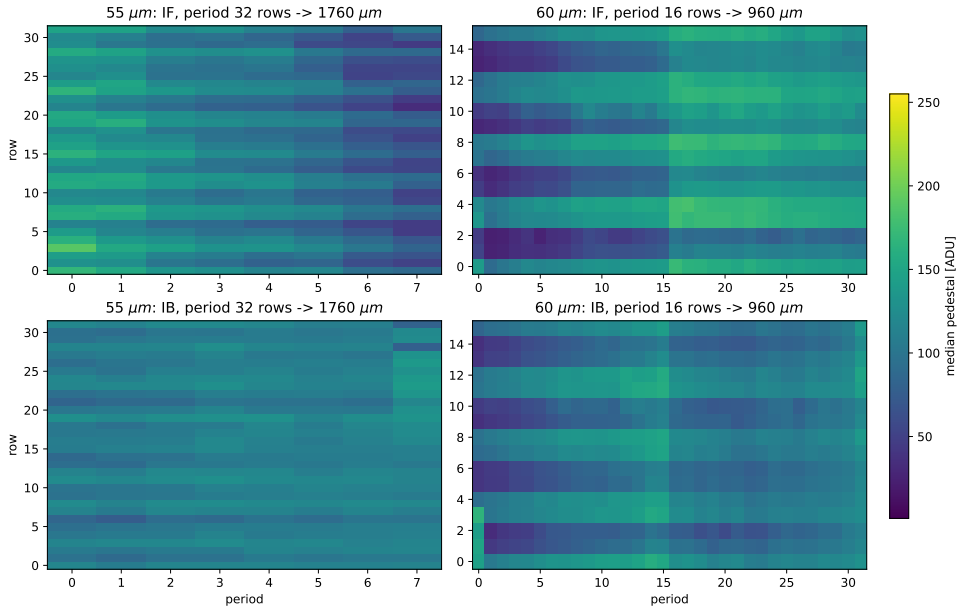


Figure A.20: W67 row sub-samples of n rows. n is given in the title of the respective sub-plot.

A.1.2 Recurring Pattern Shape

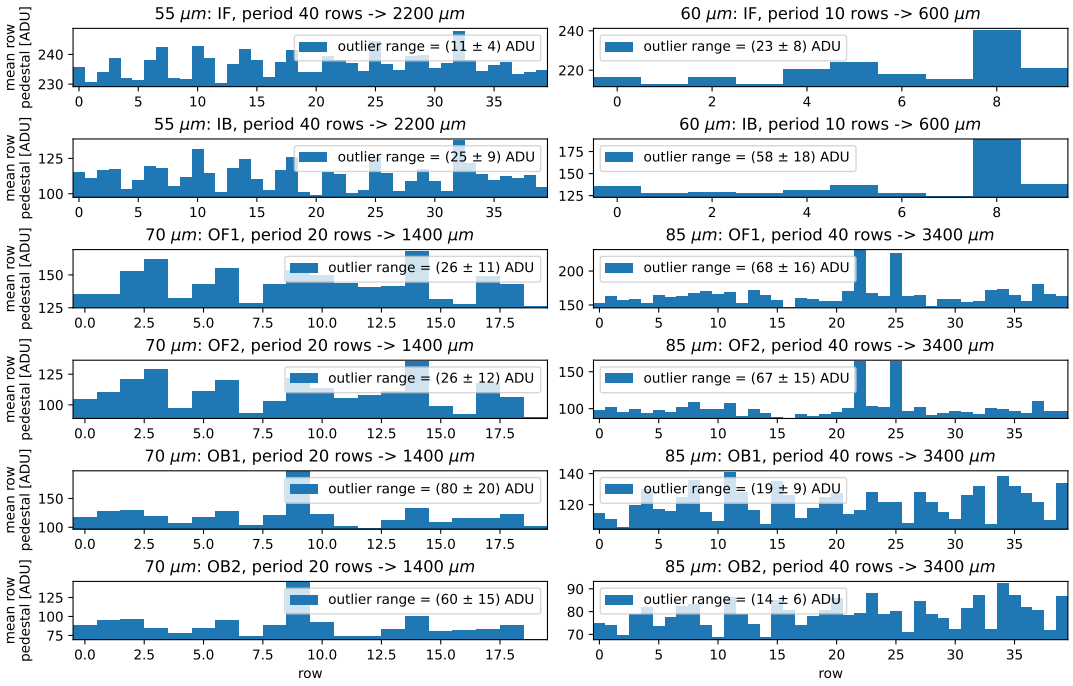


Figure A.21: W09 mean sub-sample row pedestals in recurring pattern. The legend quotes the maximum deviation from the mean and the standard deviation in ADU

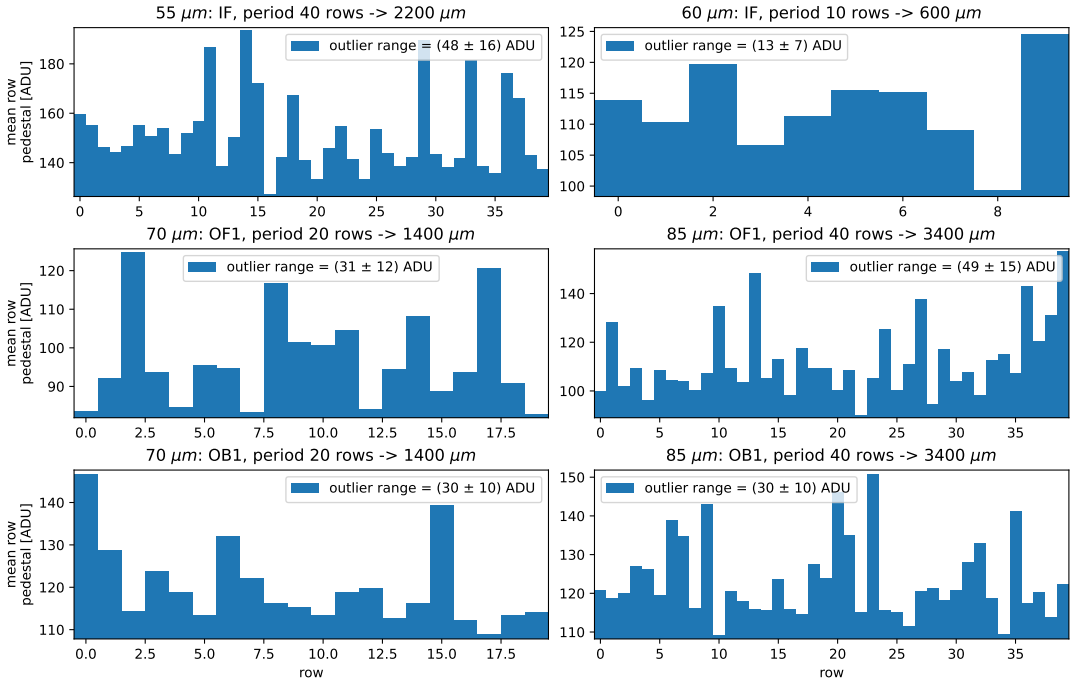


Figure A.22: W37 mean sub-sample row pedestals in recurring pattern. The legend quotes the maximum deviation from the mean and the standard deviation in ADU

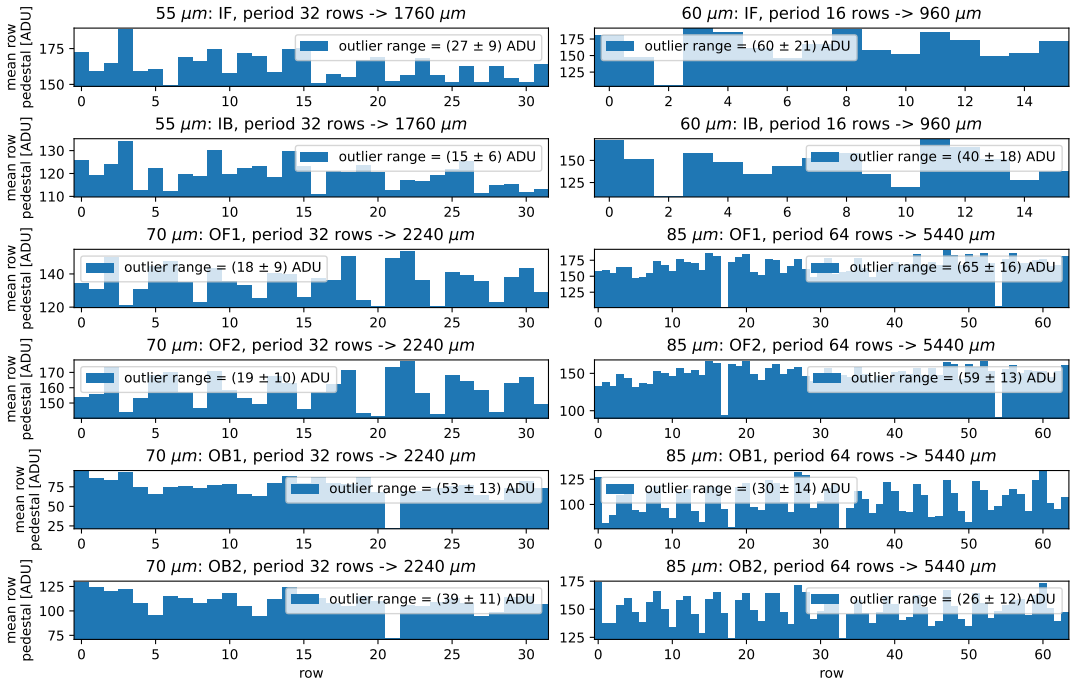


Figure A.23: W56 mean sub-sample row pedestals in recurring pattern. The legend quotes the maximum deviation from the mean and the standard deviation in ADU

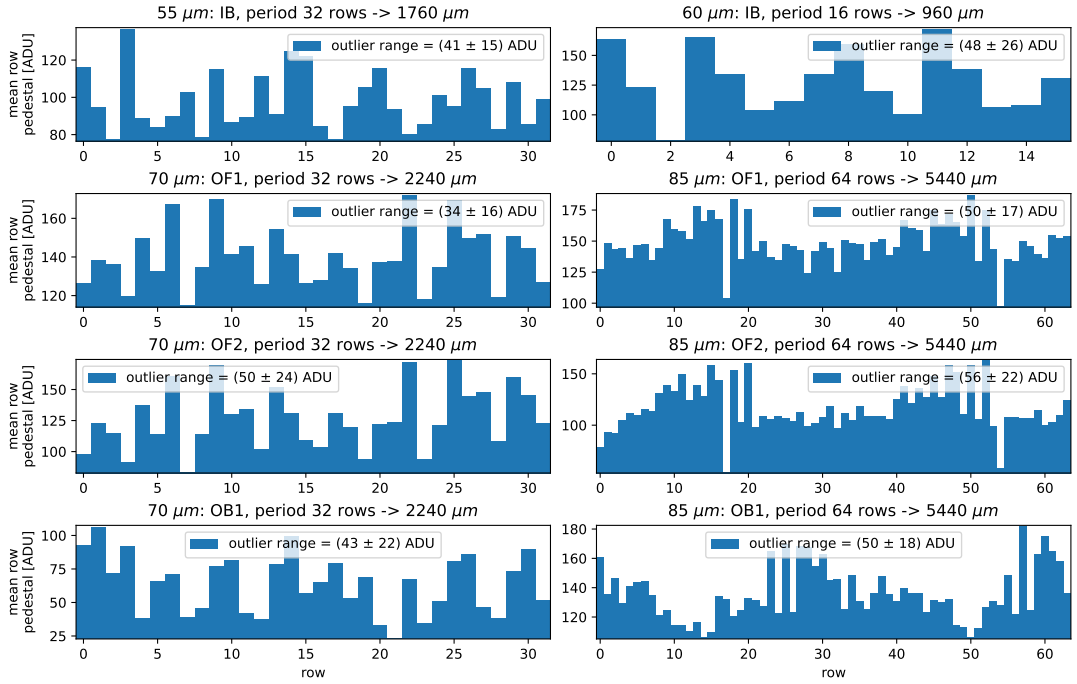


Figure A.24: W57 mean sub-sample row pedestals in recurring pattern. The legend quotes the maximum deviation from the mean and the standard deviation in ADU

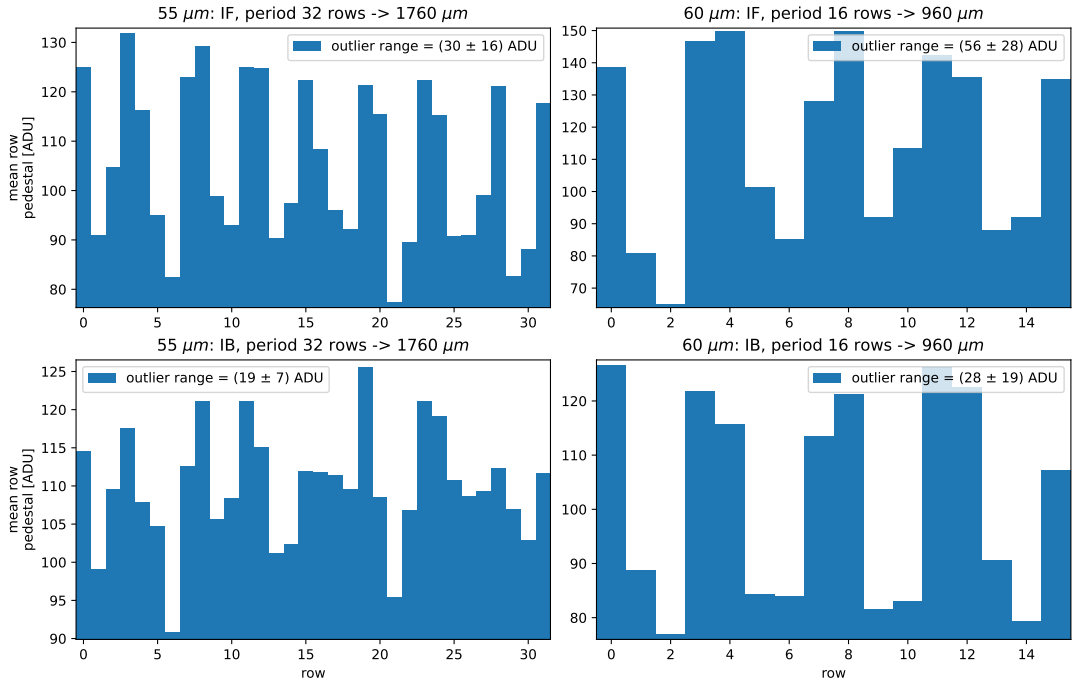


Figure A.25: W67 mean sub-sample row pedestals in recurring pattern. The legend quotes the maximum deviation from the mean and the standard deviation in ADU

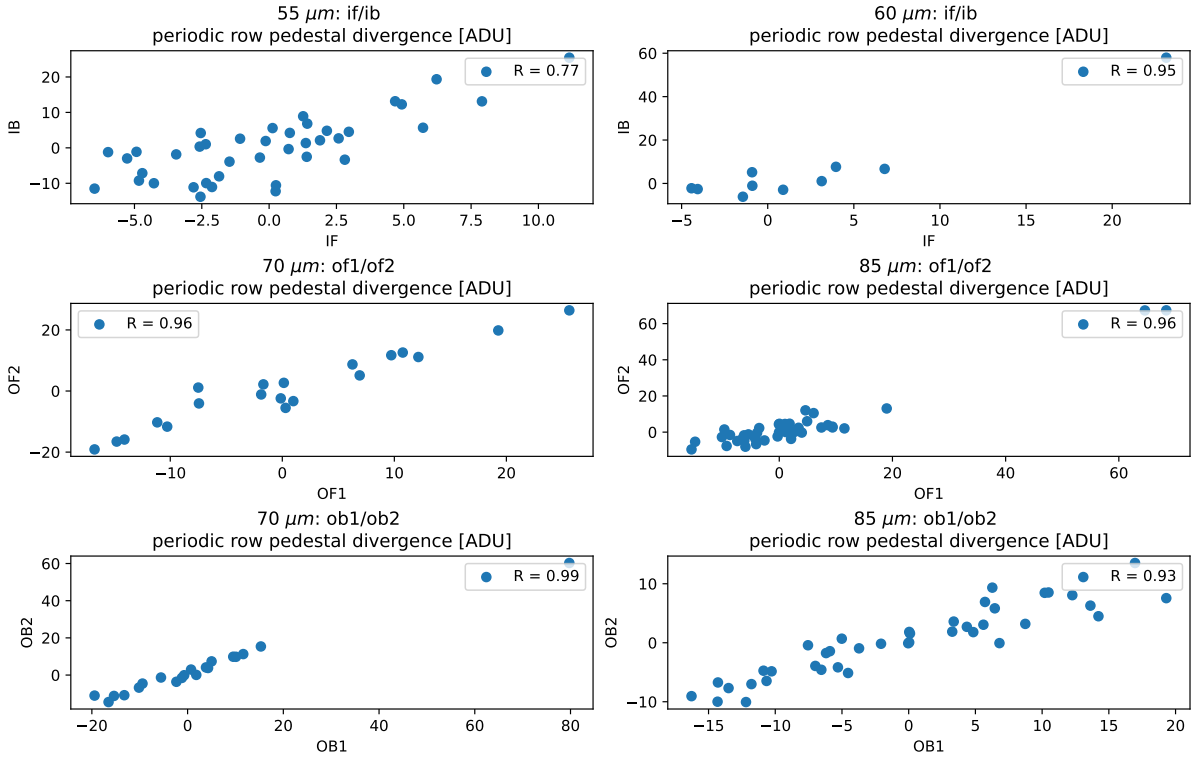


Figure A.26: W09 correlation of same-layout areas.

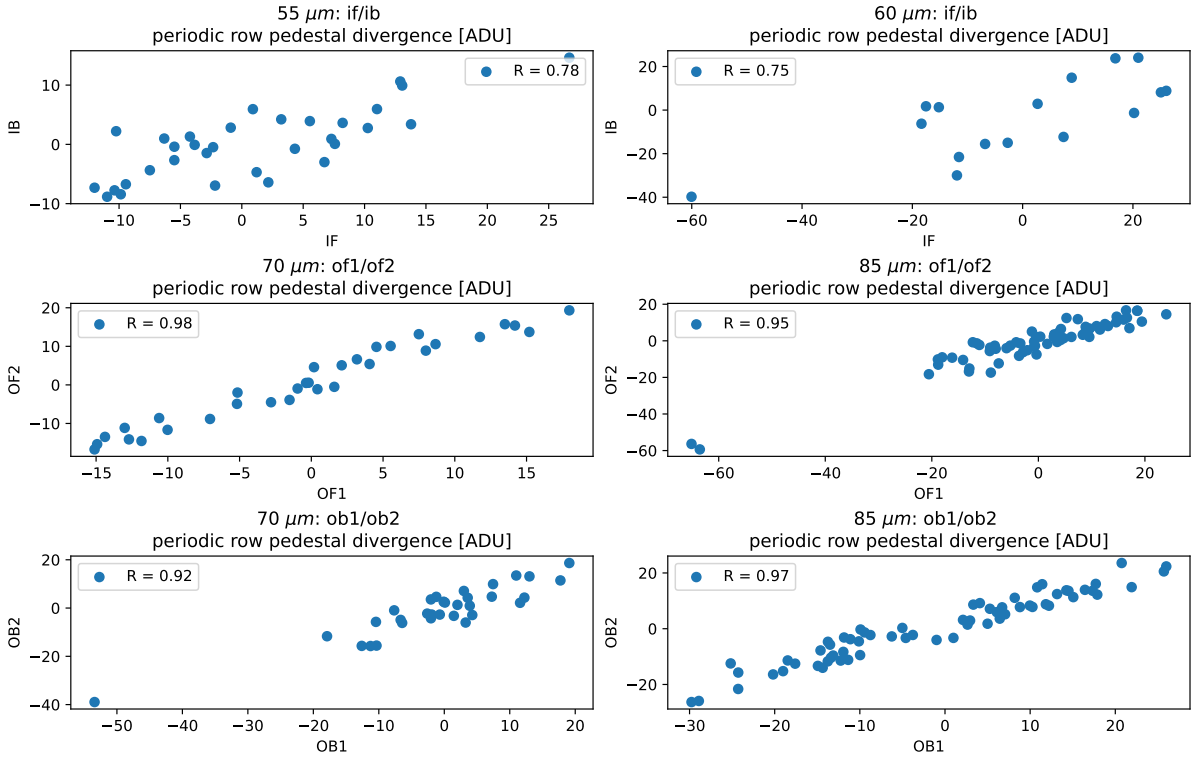


Figure A.27: W56 correlation of same-layout areas.

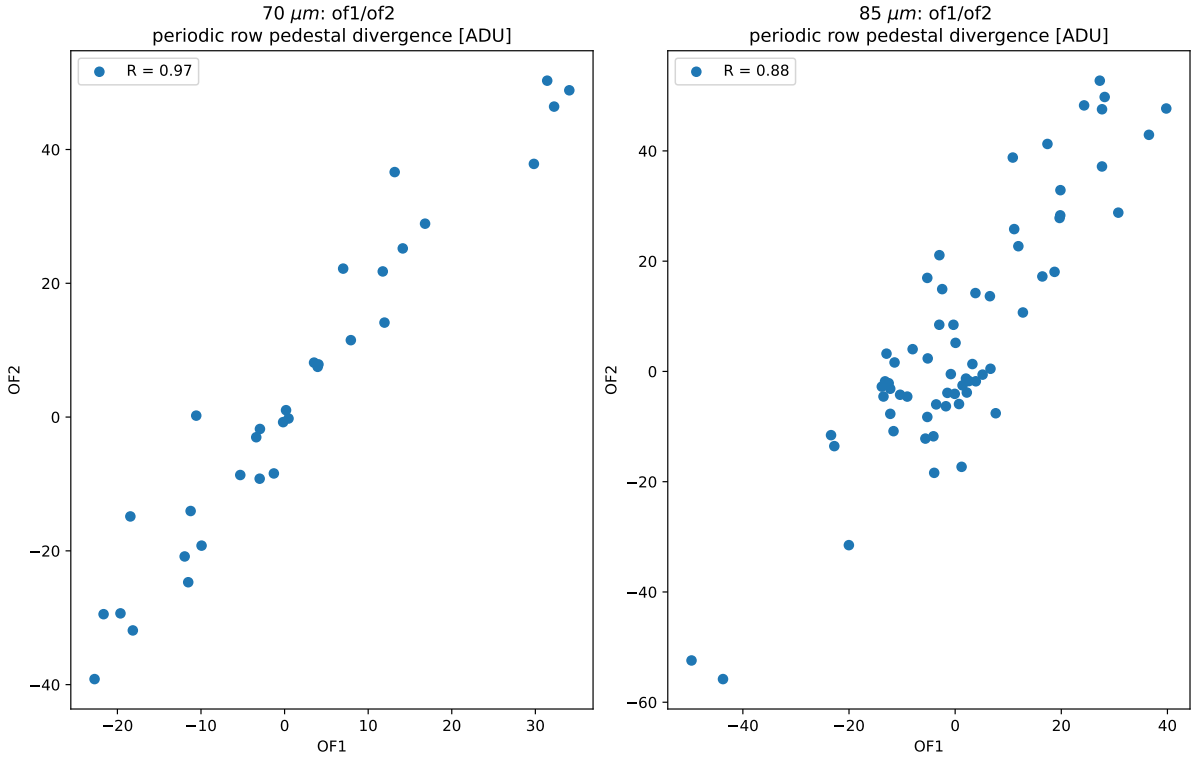


Figure A.28: W57 correlation of same-layout areas.

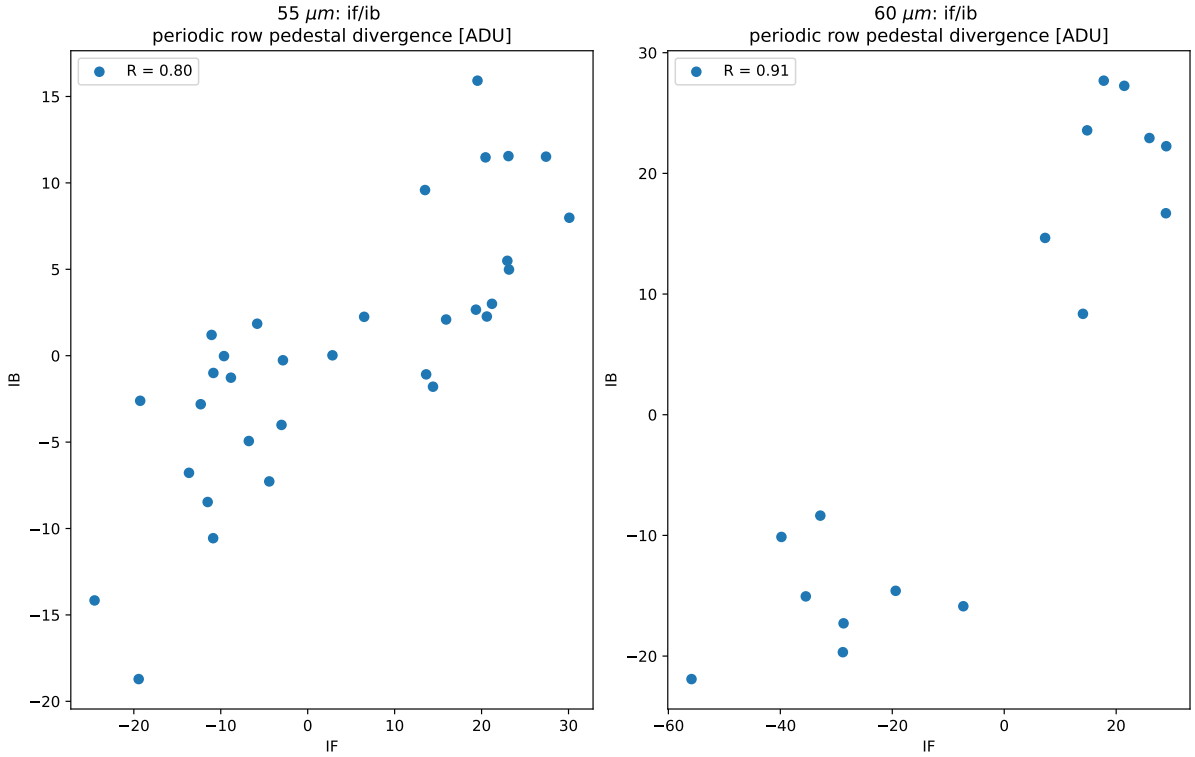


Figure A.29: W67 correlation of same-layout areas.

A.2 Double-Row Pattern

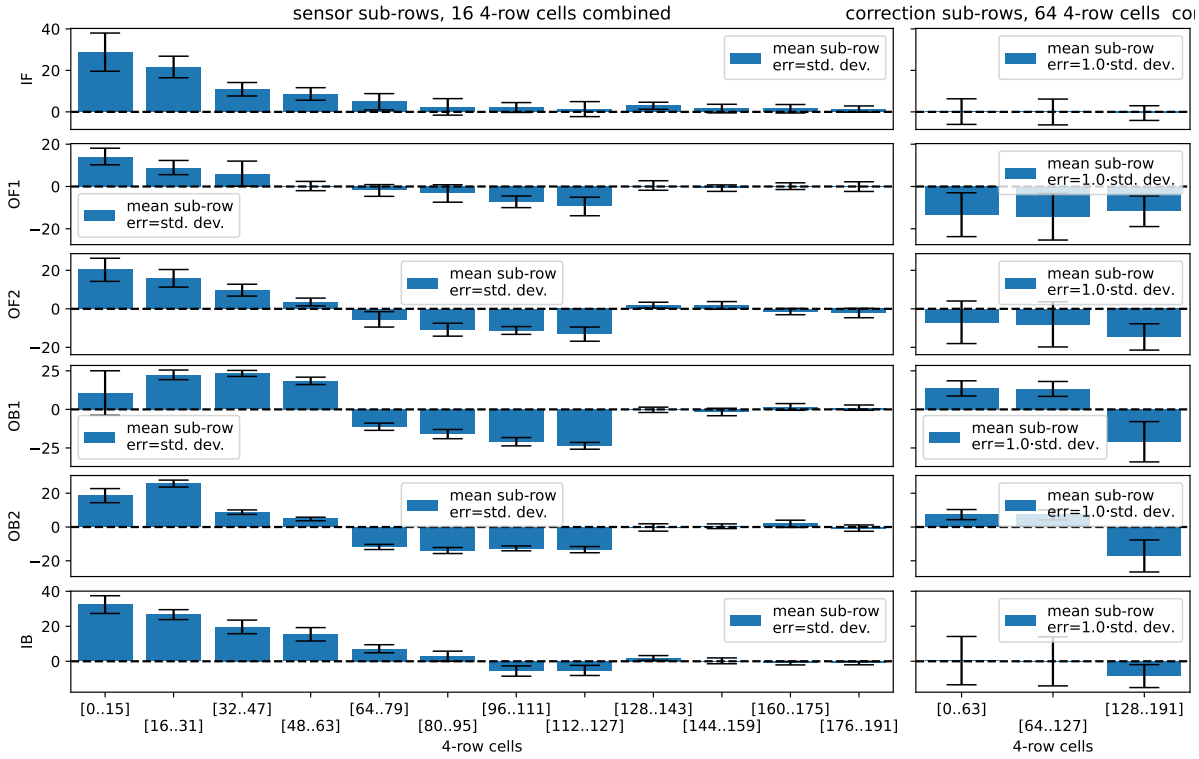


Figure A.30: W09 double-row effect magnitude $\eta_{\text{double-row}}$ of consecutive quad-rows for all sensors. The left column shows results of the calculation for each sensor with 16 quad-rows combined after periodic-row correction was applied. The right column shows the same analysis for the applied correction pattern. The black error bars represent the standard deviation of the combined values. Row 0 signifies the first row of the sensor's large pixel area, adjacent to the DCDs. Row 767 is the last row of the short pixel area at the far end of the module.

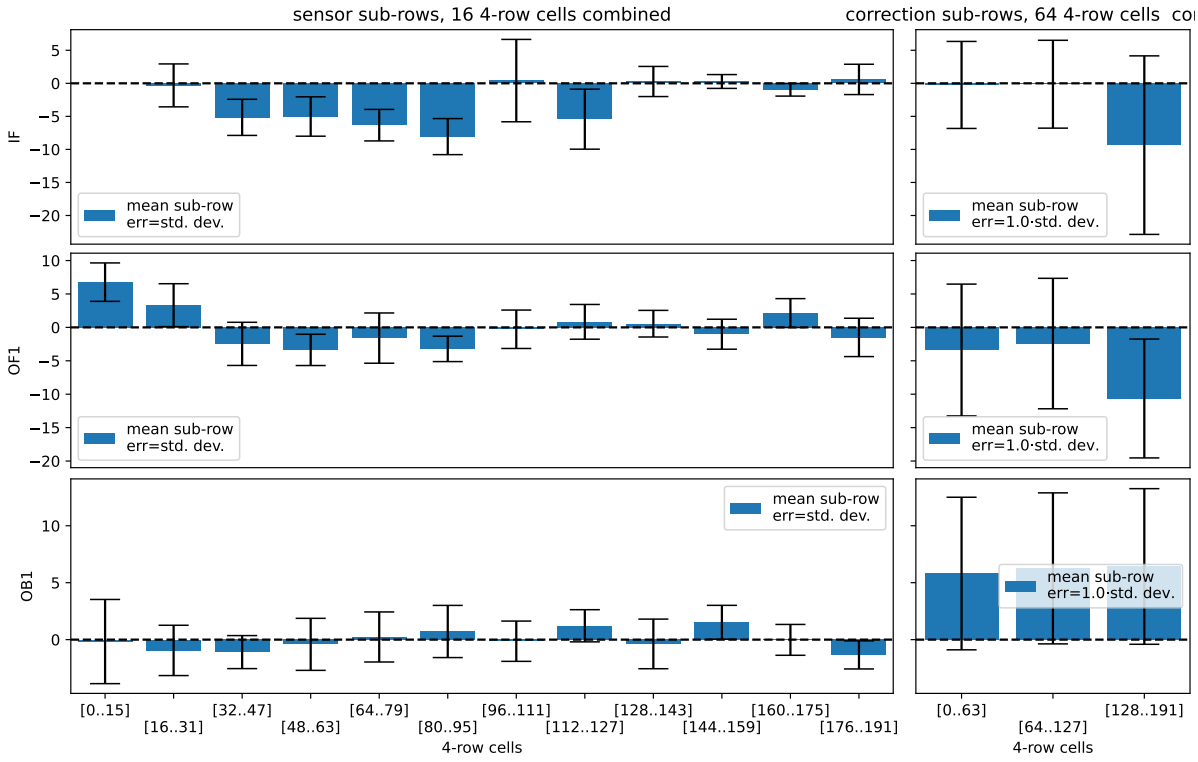


Figure A.31: W37 double-row effect magnitude $\eta_{\text{double-row}}$ of consecutive quad-rows for all sensors. The left column shows results of the calculation for each sensor with 16 quad-rows combined after periodic-row correction was applied. The right column shows the same analysis for the applied correction pattern. The black error bars represent the standard deviation of the combined values. Row 0 signifies the first row of the sensor's large pixel area, adjacent to the DCDs. Row 767 is the last row of the short pixel area at the far end of the module.

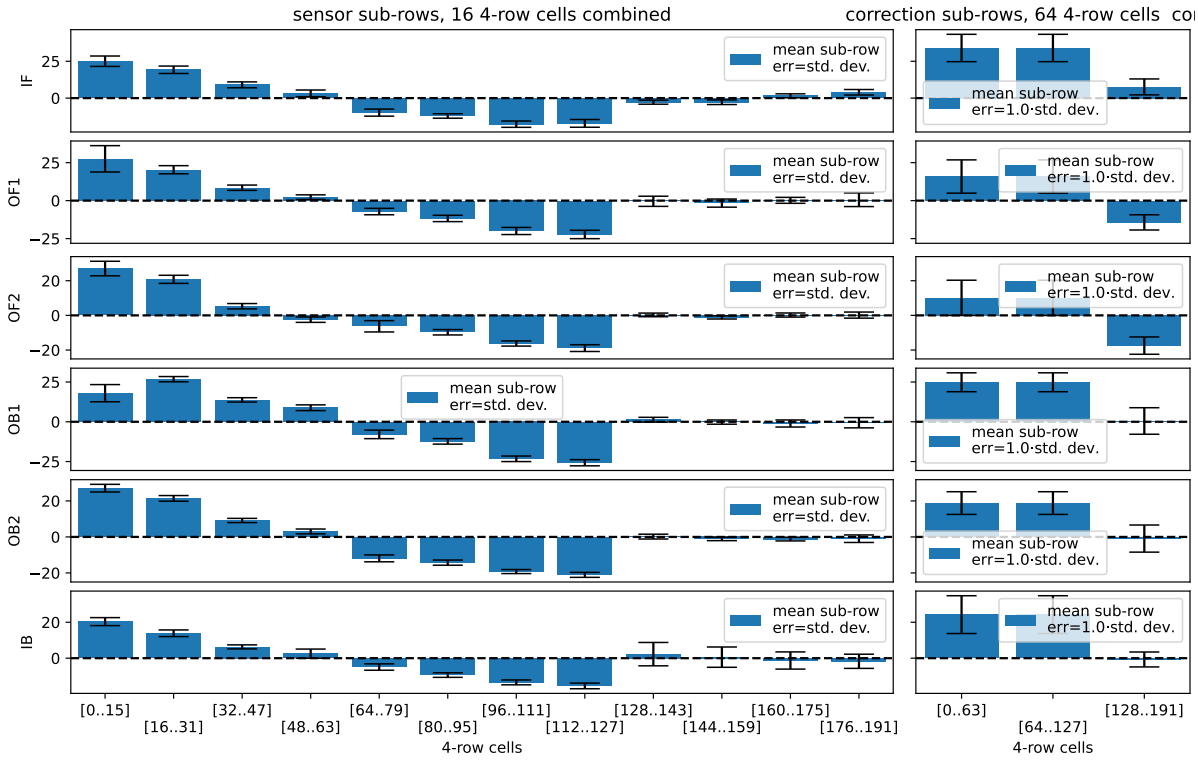


Figure A.32: W56 double-row effect magnitude $\eta_{\text{double-row}}$ of consecutive quad-rows for all sensors. The left column shows results of the calculation for each sensor with 16 quad-rows combined after periodic-row correction was applied. The right column shows the same analysis for the applied correction pattern. The black error bars represent the standard deviation of the combined values. Row 0 signifies the first row of the sensor's large pixel area, adjacent to the DCDs. Row 767 is the last row of the short pixel area at the far end of the module.

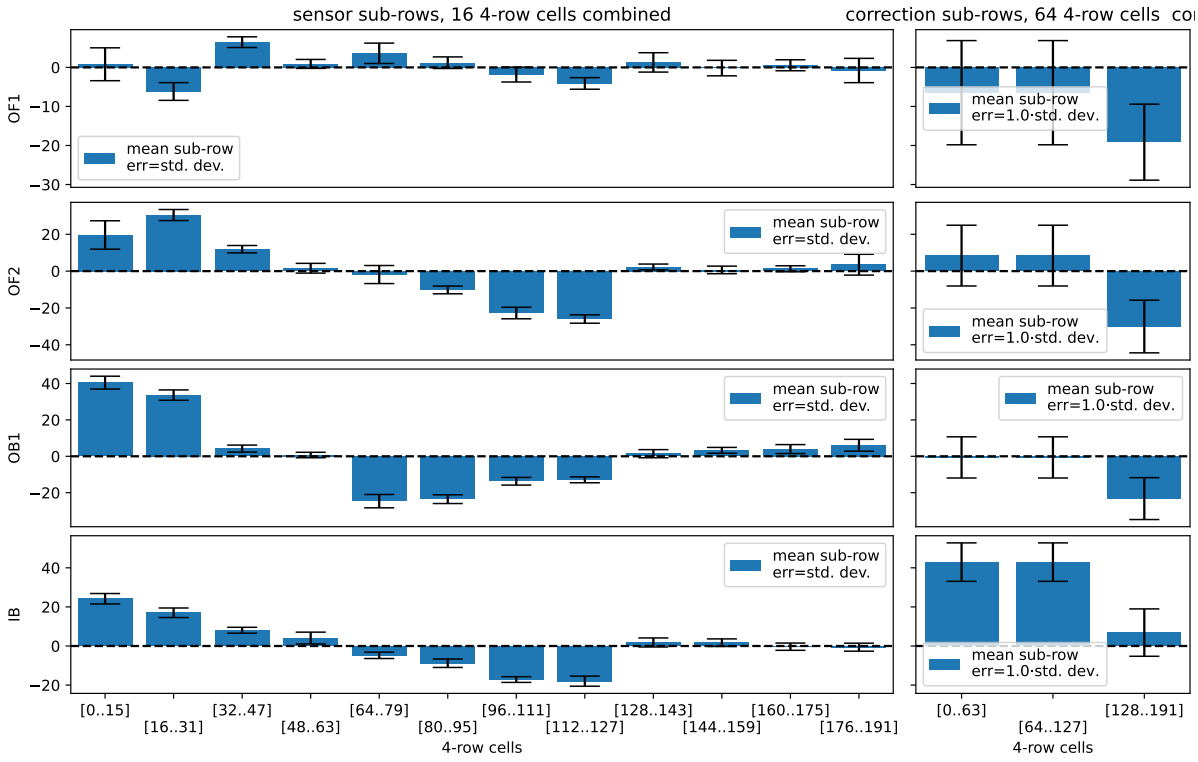


Figure A.33: W57 double-row effect magnitude $\eta_{\text{double-row}}$ of consecutive quad-rows for all sensors. The left column shows results of the calculation for each sensor with 16 quad-rows combined after periodic-row correction was applied. The right column shows the same analysis for the applied correction pattern. The black error bars represent the standard deviation of the combined values. Row 0 signifies the first row of the sensor's large pixel area, adjacent to the DCDs. Row 767 is the last row of the short pixel area at the far end of the module.

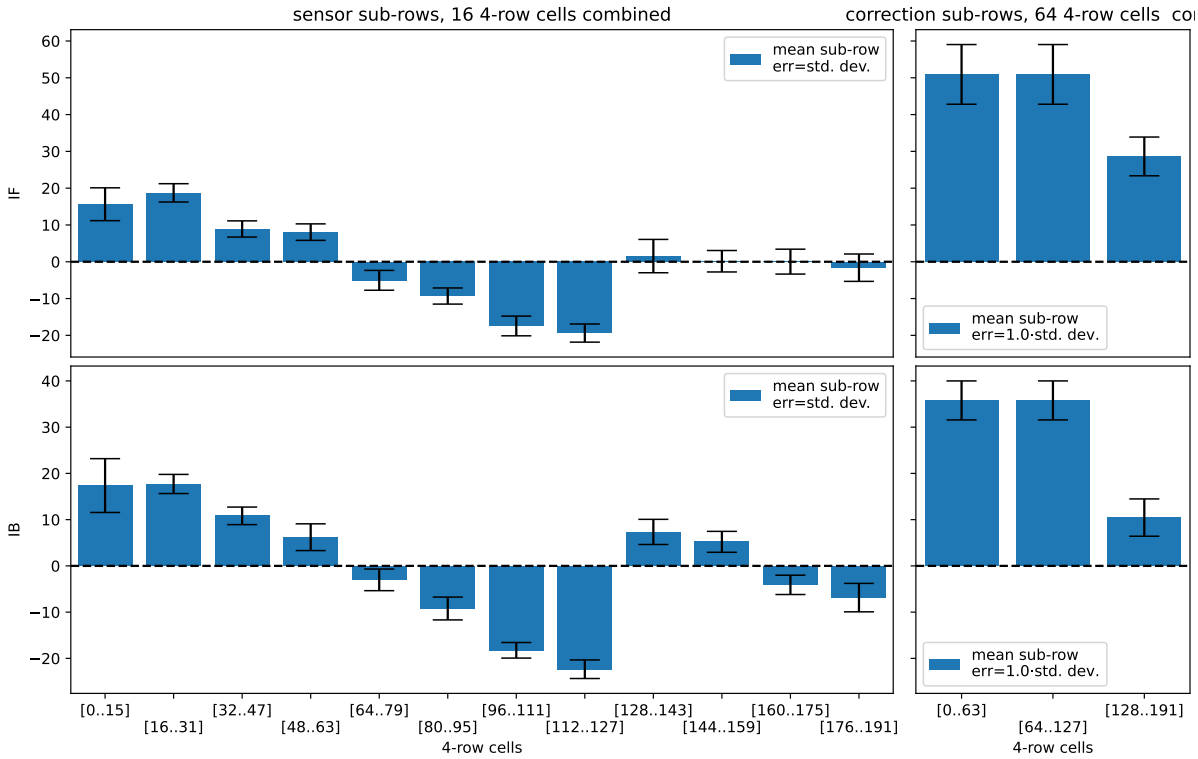


Figure A.34: W67 double-row effect magnitude $\eta_{\text{double-row}}$ of consecutive quad-rows for all sensors. The left column shows results of the calculation for each sensor with 16 quad-rows combined after periodic-row correction was applied. The right column shows the same analysis for the applied correction pattern. The black error bars represent the standard deviation of the combined values. Row 0 signifies the first row of the sensor's large pixel area, adjacent to the DCDs. Row 767 is the last row of the short pixel area at the far end of the module.

A.3 DCD column effect

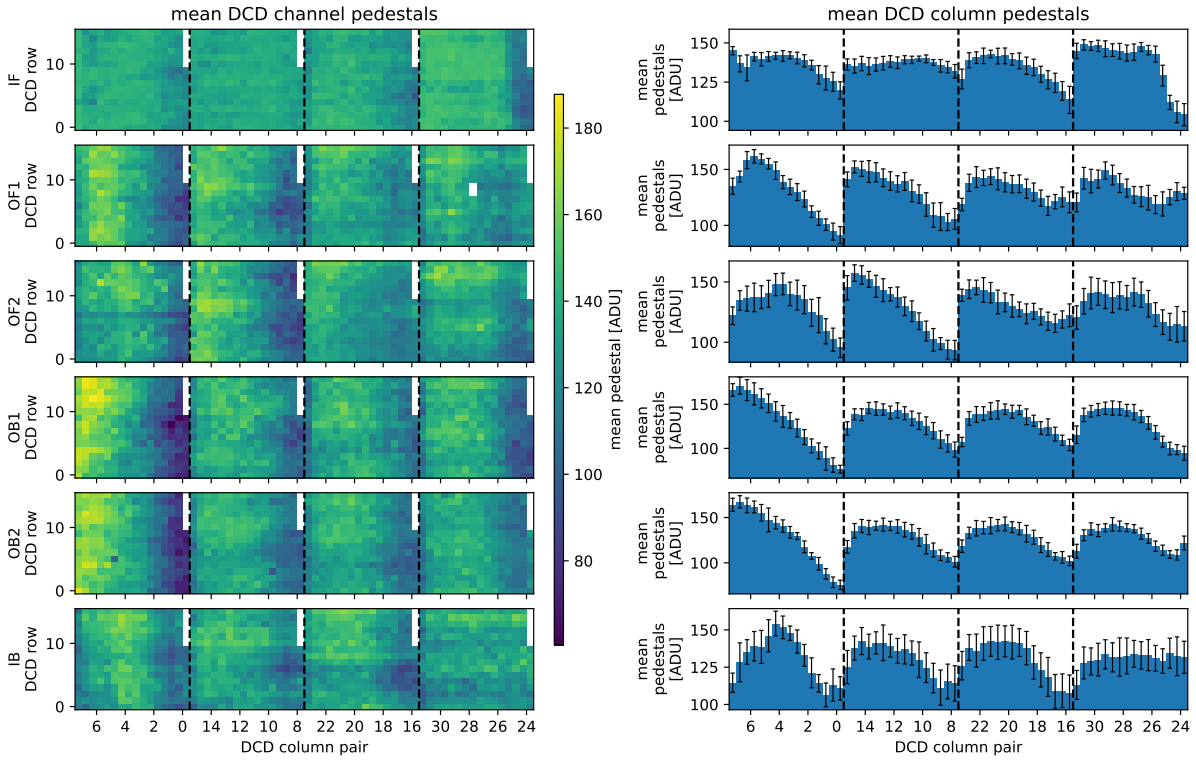


Figure A.35: Mean pedestals of DCD channels of wafer 46 and mean DCD column pedestals. The left column shows the mean DCD channel pedestals arranged according to their location on the module for each module. The right column shows the mean DCD column pedestals. The black error bars correspond to the standard deviation.

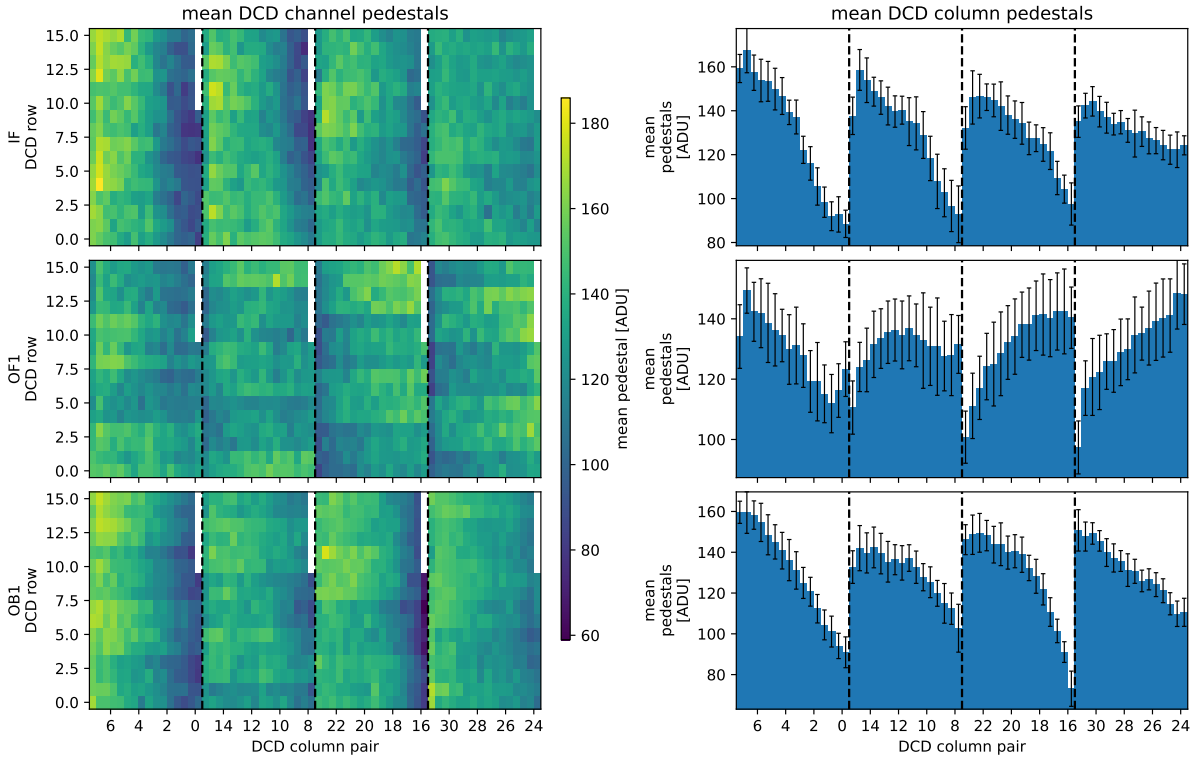


Figure A.36: Mean pedestals of DCD channels of wafer 46 and mean DCD column pedestals. The left column shows the mean DCD channel pedestals arranged according to their location on the module for each module. The right column shows the mean DCD column pedestals. The black error bars correspond to the standard deviation.

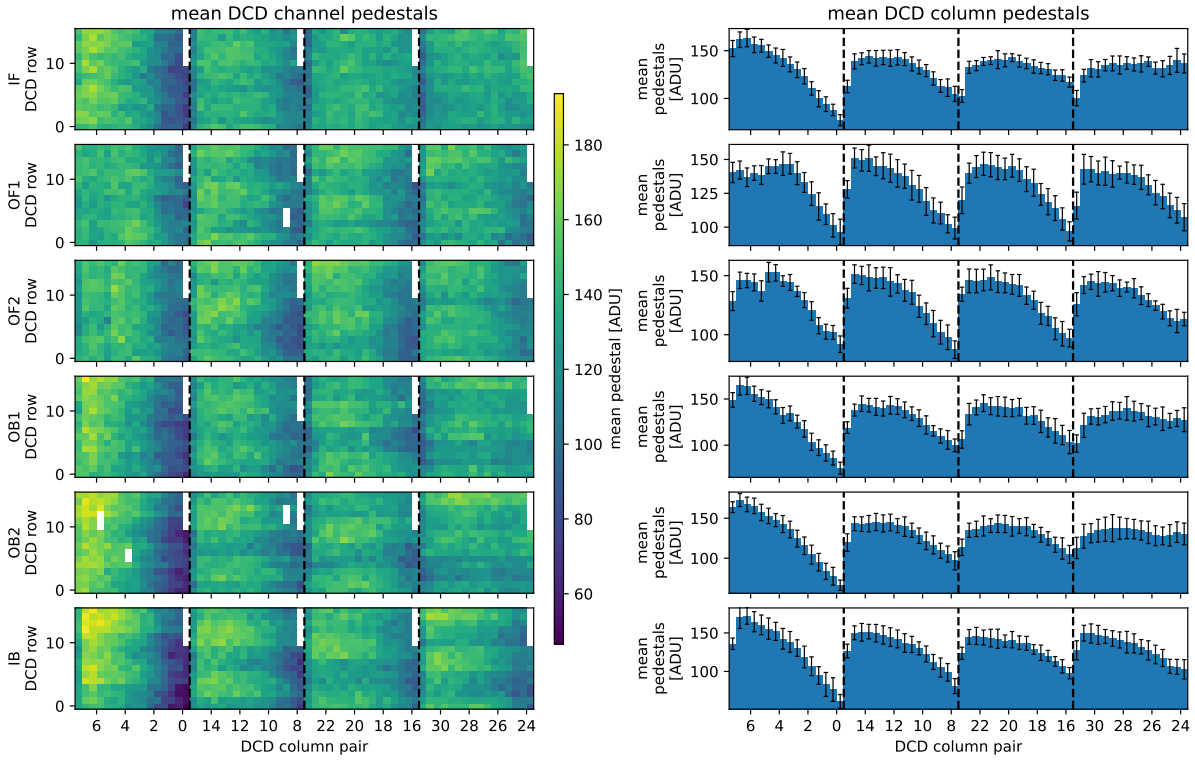


Figure A.37: Mean pedestals of DCD channels of wafer 46 and mean DCD column pedestals. The left column shows the mean DCD channel pedestals arranged according to their location on the module for each module. The right column shows the mean DCD column pedestals. The black error bars correspond to the standard deviation.

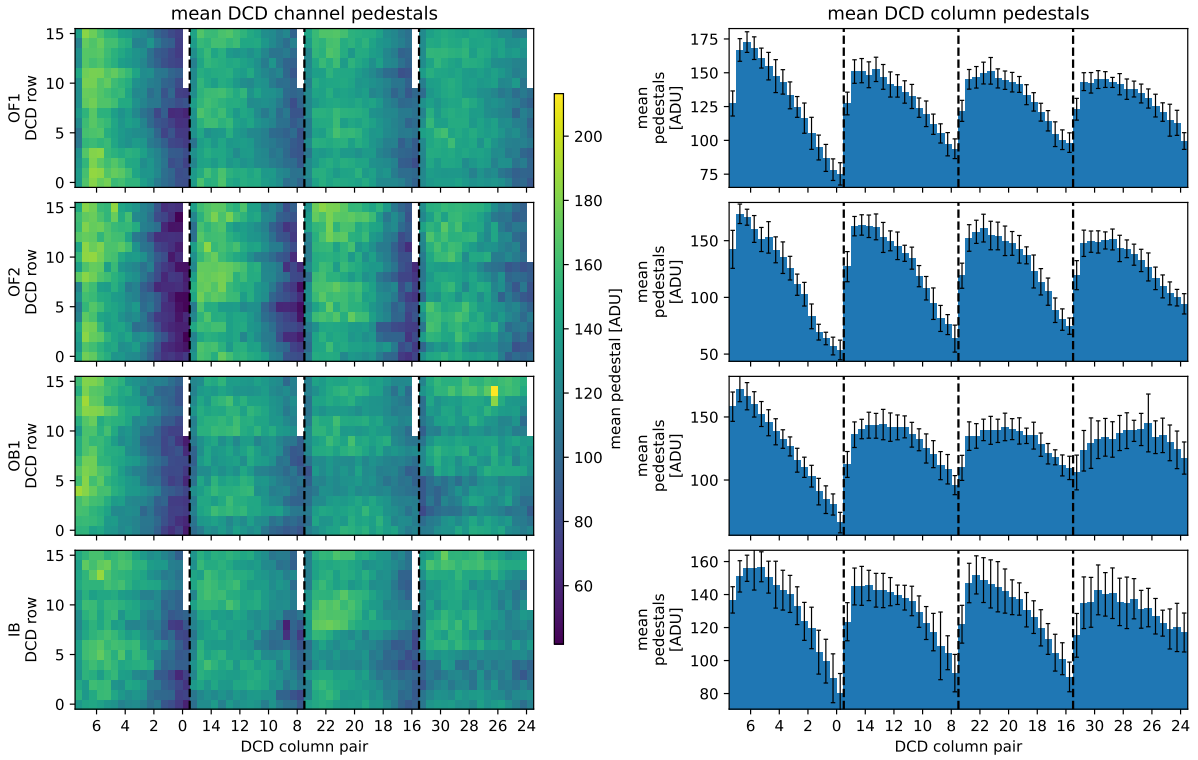


Figure A.38: Mean pedestals of DCD channels of wafer 46 and mean DCD column pedestals. The left column shows the mean DCD channel pedestals arranged according to their location on the module for each module. The right column shows the mean DCD column pedestals. The black error bars correspond to the standard deviation.

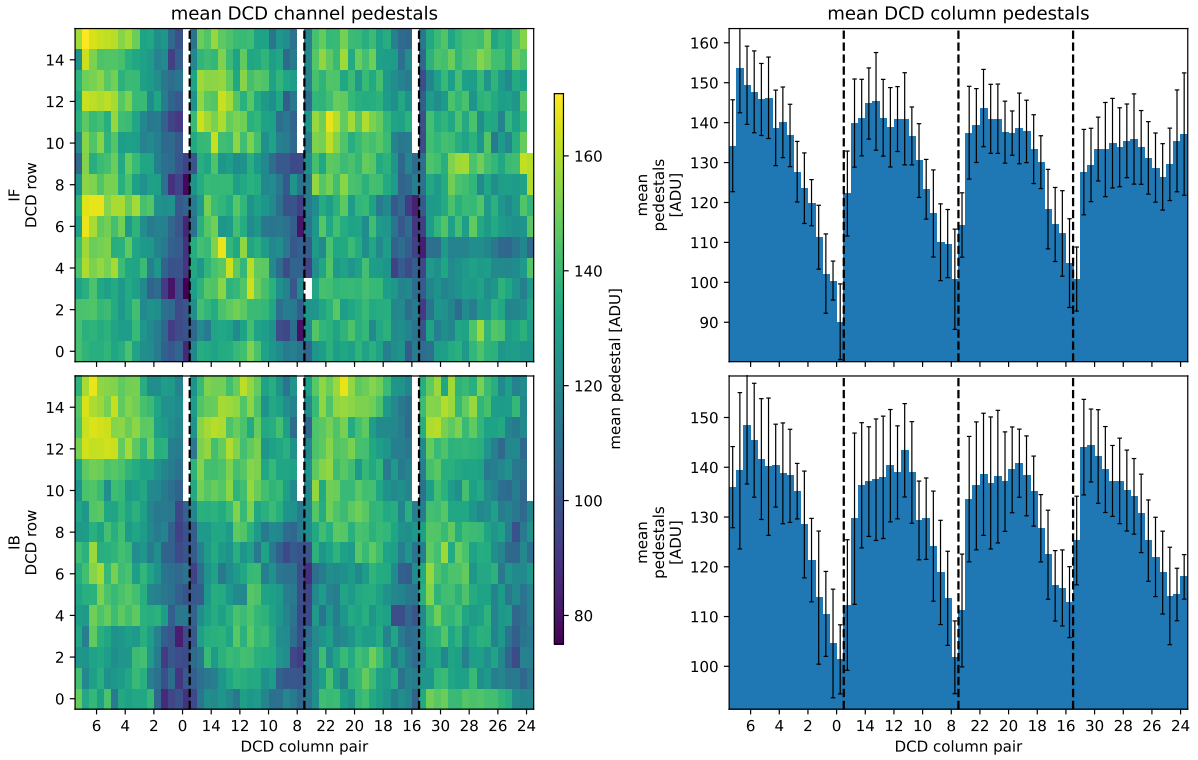


Figure A.39: Mean pedestals of DCD channels of wafer 46 and mean DCD column pedestals. The left column shows the mean DCD channel pedestals arranged according to their location on the module for each module. The right column shows the mean DCD column pedestals. The black error bars correspond to the standard deviation.

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