# Investigation of Breakdown Behaviour and Improvement of Spatial Resolution for Silicon Pixel Detectors

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**Sinuo Zhang**
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## Abstract

In high-energy physics, the demand for silicon pixel detectors is increasing due to the elevated particle collision rates in collider experiments, since silicon detectors can handle high particle fluxes and provide precise determination of particle tracks. Silicon pixel sensors fabricated using commercial CMOS technologies (passive CMOS sensors) offer an attractive alternative to conventional planar pixel sensors. Commercial CMOS technologies provide a well-tuned set of fabrication parameters and special features, such as multiple metal layers, ensuring the reliability of the final products. However, this advantage comes at the cost of limited customisability for doping profiles, making it difficult to transfer previous knowledge from planar sensors directly. The studies presented in this work focus on two crucial features of passive CMOS silicon pixel sensors: breakdown performance and spatial resolution. The breakdown voltage determines the upper limit of the operational voltage of silicon pixel detectors. It is influenced by the design of the implant structures in the area between the pixel matrix and the chip's edge, where a large voltage drop occurs. The goal of optimising the sensor design is to provide a smooth potential drop to suppress unexpected high electric fields. N-on-p passive-CMOS test structures were fabricated, measured, and simulated using TCAD to study the relationship between guard ring design and breakdown performance. In the second part of the thesis, a concept for improving spatial resolution using directional charge sharing between pixels is proposed and validated through dedicated simulations. Directional charge sharing can be achieved via subdivision of pixels and capacitive cross-couplings, which can be realised using commercial CMOS technologies. Results show an improvement in spatial resolution of approximately 30% compared to conventional pixel sensors with the same pitch size.

# Contents

CHAPTER 1

# Introduction

Collider experiments are the principal methods in High-Energy Physics (HEP) for studying elementary particles, fundamental interactions, and searching for new physics. These experiments utilise linear or circular accelerators, such as the LHC[1] at CERN[2] for protons, and SuperKEKB at KEK[3] for electrons/positrons, to accelerate particles to nearly the speed of light. At designated points along the accelerator, high-energy particles are steered into "head-on" collisions. These collisions generate new particles that scatter in all directions. Detectors, arranged in a cylindrical "onion-shell"-like configuration around the collision centre (e.g., ATLAS[4], CMS[5], and BELLE II[6] detectors), are used to track these particles for analysing their properties. A typical modern general-purpose particle detector includes:

- A tracking detector system, often made of silicon pixel/strip detectors and/or a time projection chamber, positioned close to the collision centre to accurately trace the produced particles. Due to their compact size, fast response, and high spatial resolution, silicon detectors are preferred for tracking charged particles.
- Calorimeters, which are constructed from materials with high atomic numbers and placed beyond the tracking detectors, to measure the energy of particles as they deposit their entire energy within these detectors.
- Muon spectrometers, positioned as the outermost layer of the detector. Muons, having minimal energy loss in materials, penetrate the entire detector.

The forthcoming upgrade of the LHC will significantly increase collision rates of protons, posing new challenges for the detectors. For instance, an upgrade of the ATLAS tracking detectors (inner tracker) is planned to include a larger area of silicon detectors, with increased number of readout channels/pixels and higher readout speed, to handle the increased particle flux and rate. This will

[1] Large Hadron Collider
[2] Conseil Europ'een pour la Recherche Nucl'eaire, Geneva, Switzerland.
[3] High Energy Accelerator Research Organization, Tsukuba, Japan.
[4] A Toroidal LHC ApparatuS, LHC.
[5] Compact Muon Solenoid, LHC.
[6] At the SuperKEKB.

feature approximately 180 $m^2$ of silicon detectors, tripling the size of the current tracking detector. Similarly, the CMS tracker will employ approximately 214 $m^2$ of silicon detectors, and plans for the Future Circular Collider (FCC) include about 430 $m^2$ of silicon detectors.

Silicon pixel sensors fabricated using commercial CMOS technologies (passive-CMOS) present a promising alternative to traditional planar sensor technologies. The widespread use and mature manufacturing process of CMOS sensors make them more cost-effective and allow for higher production volumes. Features unique to commercial CMOS technologies, such as multiple metal layers, polysilicon layers, and metal-insulator-metal capacitors, enable innovative sensor designs. Additionally, passive-CMOS sensors using high-resistivity wafers have been demonstrated to be radiation-hard.

This thesis focuses on two essential characteristics of silicon pixel sensors: their breakdown performance and spatial resolution. Although passive-CMOS offers many advantages, the predefined implant profile from the foundries might not meet the high bias voltage requirements of particle detectors. Thus, the breakdown performance of passive-CMOS in relation to the guard ring design becomes an urgent topic. Previous applications often used large areas for guard rings to ensure a high breakdown voltage, leading to space inefficiency. This work introduces guard ring structures that occupy a much smaller total area without compromising performance. In chapter 5, experiments and simulations have been conducted on passive-CMOS test structures equipped with various guard ring designs to evaluate their current-voltage behaviour until breakdown. Further investigations on guard ring optimisation and its impact on sensor design are presented in chapter 6, employing Technology Computer-Aided Design (TCAD) simulations.

Achieving high spatial resolution typically involves reducing pixel size, necessitating significant redesign or co-development of readout electronics. An alternative approach is enhancing the charge sharing between pixels. This thesis explores the use of sub-pixel cross-coupling to increase spatial resolution, presenting a model that employs commercial CMOS technology to facilitate directional charge sharing between pixels (chapter 7). The potential benefits of this model are demonstrated through dedicated simulation software.

CHAPTER 2

# Silicon-based Devices

As the most abundant (27.7%) element in the Earth's crust, silicon occurs mostly as compounds in nature, such as sand, whose major constituent is silica ($SiO_2$). This easily acquirable material has been playing a non-negligible role in our daily life throughout the history, from the stone knives and spears in ancient times to various glass products which are still being used today. Ever since the development of technologies that turn pure sand into monocrystalline silicon, this semiconductor material has triggered studies of its electrical properties and the possibilities for applications. Nowadays, silicon-based devices have dominated the electronic components in all the aspects of our lives, covering the computation technology, telecommunication, digital imaging, and even the frontier of scientific research.

## 2.1 Crystal Structure and Band Structure

Monocrystalline silicon has a diamond structure as the conventional unit cell, i.e., a face-centred cubic (fcc) lattice with two Si atoms as the basis at each fcc lattice point, as depicted in Figure 2.1. The formation of such a structure follows the $sp^3$ orbital hybridisation, where one Si atom is connected to four neighbouring Si atoms via covalent bonds, with a 109.9° intersection angle between bonds. The dimension of the unit cell is characterised by the lattice constant $a_{\mathrm{Si}} = 5.431$ Å (at 300 K) [1], and the cell is repeated in space to form the silicon crystal. Miller indices are used to represent the planes of different crystal orientations, as shown in Figure 2.2. Taking the intersection points between the axes and the corresponding atoms in terms of the lattice constant, and computing the ratio between them using the smallest integer, the miller index of each plane is represented by three integers enclosed in parentheses $(hkl)$ [3]. The silicon material with surface crystal orientation (100) and (111) (Figure 2.2) are commonly used in semiconductor manufactury [4].

The energy of electrons in solid crystals are arranged in bands which are separated by ***band gaps***. Figure 2.3 illustrates a schematic band diagram of silicon, where the energy is a function of the wave vector $\mathbf{k}$. The full band diagram can be calculated as described in [5]. The quantity of energy states of electrons within a band is described by the ***density of states*** (DOS) $N(E)$ as a function of

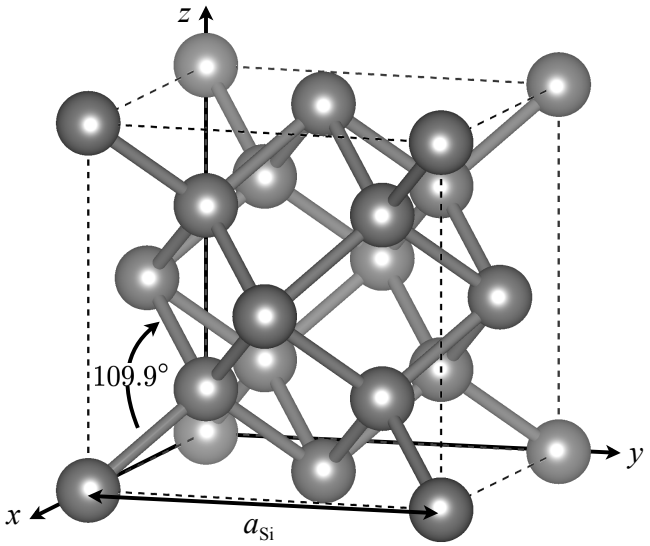



Figure 2.1: The unit cell of the silicon crystal. The silicon atoms are represented with the spheres, and the bonds between them are indicated as the bars. The location of the atoms can be defined by setting the Cartesian coordinate system, with $a_{Si}$ the edge length of the cubic cell. The figure is made with the help of software "VESTA" [2].

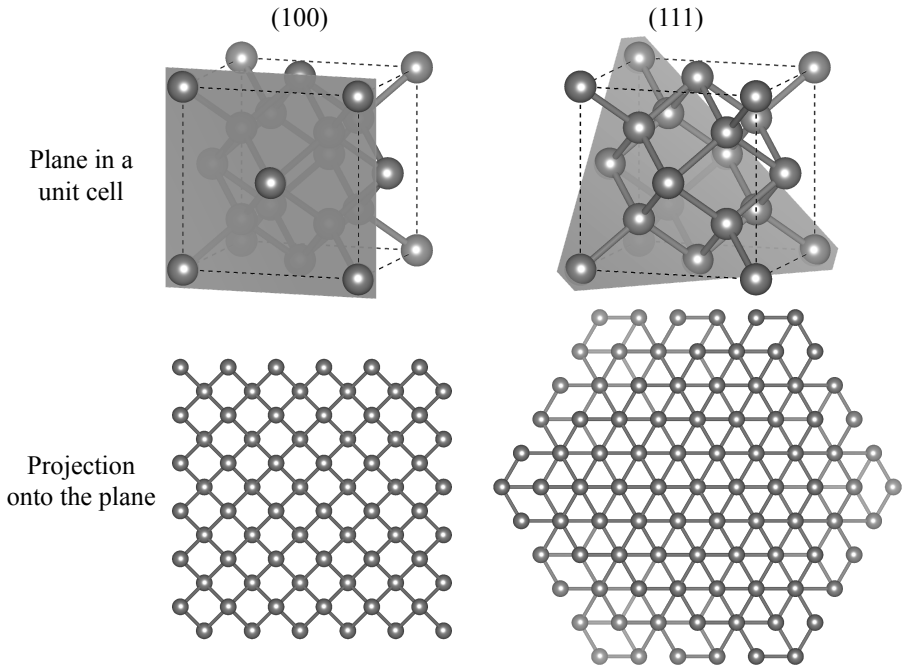



Figure 2.2: The planes (shaded area) in a unit cell of silicon crystal represented with the miller indices (100) and (111), and the view of the lattice when the atoms are projected onto the corresponding planes. The figure is made with the help of software "VESTA" [2].

energy. Adopting the free electron gas model, the energy-dependent density of states is given by

$$N(E) = \frac{1}{2\pi^2}\left(\frac{2m^*_{DOS}}{\hbar}\right)^{3/2}\sqrt{E}\,, \tag{2.1}$$

where $m^*_{DOS}$ is the ***density of states effective mass*** and is obtained from the curvature of the energy band.

According to the theory of Fermi and Dirac, the occupation probability of energy states by electrons follows the ***Fermi-Dirac statistics***. The ***Fermi-Dirac distribution***

$$f(E,T) = \left[1 + \exp\left(\frac{E-\mu}{k_B T}\right)\right]^{-1} \tag{2.2}$$

gives the occupation probability as a function of energy $E$ and temperature $T$, where $k_B$ is the Boltzmann constant and $\mu$ is the chemical potential of electrons. At $T = 0$ K, $f(E)$ is a step function with $f(E) = 1$ for $E \leq \mu$ and $f(E) = 0$ for $E > \mu$. In this case the chemical potential is also called ***Fermi energy*** $F$. The sharp edge of the distribution at $E = \mu$ is smeared with rising temperature, therefore, the probability to find an electron with energy greater than $\mu$ is increased. Usually, $\mu$ is also referred to as ***(quasi-) Fermi level*** and denoted as $E_F$. This nomenclature will be used in the rest of this work.

In semiconductors, $E_F$ is located in the gap between two bands. The upper one is called the "conduction band" with $E_c$ the energy of its lower bound, and the one below $E_F$ is called the "valence band" with $E_v$ the energy of its upper bound. The band gap energy $E_g$ is defined by the energy difference between the minimum of the conduction band and the maximum of valence band. Silicon is a so-called indirect semiconductor which has an indirect band gap, as illustrated in Figure 2.3, where the extrema of both bands are located at different $k$-vectors. According to Eq. (2.2), the valence band is fully occupied by electrons at $T = 0$ K, whilst the conduction band is empty. The unique electrical properties of semiconductors like silicon originates from the band gap with $E_g$ typically below 4 eV (Si: $E_g = 1.12$ eV). Due to the small $E_g$, external energy of several eV (e.g. thermal energy, particle traversing, or light illumination) can cause the excitation of electrons to the conduction band and leave positively charged "holes" in the valence band. Electrons in the conduction band and holes in the valence band (***electron-hole pair***, or ***e-h pair***) are charge carriers that can move through the semiconductor and contribute to the conductivity.

## 2.2 Intrinsic and Doped Silicon

A piece of pure monocrystalline silicon is an ***intrinsic semiconductor***, where the conducting charge carriers are purely caused by thermal excitation. In this case, the electron concentration $n_c$ in the conduction band and the hole concentration $p_v$ in the valence band can be calculated through integrating the product of the density of states (Eq.(2.1)) and the occupation probability based on the

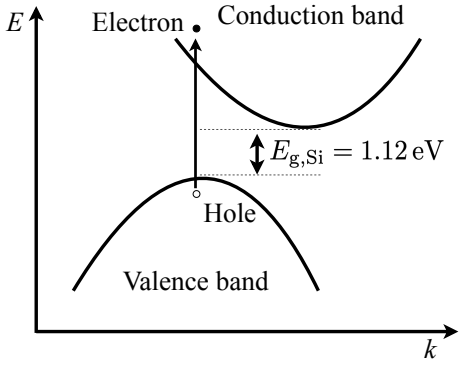



Figure 2.3: Illustration of a part of the silicon band diagram. The energy difference between the minimum pf conduction band and the maximum of the conduction band is the gap energy $E_g$. Electrons can be excited from the valence band to the conduction band, leaving a hole in the valence band. The abscissa represents the crystal momentum (k-vector) in the Brillouin zone.

Fermi-Dirac distribution (Eq. (2.2)), thus

$$\begin{aligned} n_c &= 2\left(\frac{m^*_{e,DOS} k_B T}{2\pi\hbar^2}\right)^{3/2} \exp\left(-\frac{E_c - E_F}{k_B T}\right) = n_c^{eff} \exp\left(-\frac{E_c - E_F}{k_B T}\right), \\ p_v &= 2\left(\frac{m^*_{h,DOS} k_B T}{2\pi\hbar^2}\right)^{3/2} \exp\left(-\frac{E_F - E_v}{k_B T}\right) = p_v^{eff} \exp\left(-\frac{E_F - E_v}{k_B T}\right). \end{aligned} \tag{2.3}$$

$n_c^{eff}$ and $p_v^{eff}$ are the effective density of states and they are weakly temperature-dependent. Thus, the charge carrier density is more sensitive to the distance between $E_F$ and $E_c$ (or $E_v$). Since $n_c = n_p$ in intrinsic semiconductors, the quasi-Fermi level is given by

$$E_F = E_v + \frac{1}{2}E_g + \frac{3}{4}k_B T \ln\frac{m^*_{h,DOS}}{m^*_{e,DOS}}. \tag{2.4}$$

At $T \approx 0\,K$ or $m^*_{e,DOS} \approx m^*_{e,DOS}$, the Fermi-level of an intrinsic semiconductor is located in the middle of the band gap, defining the intrinsic Fermi-level $E_i$ with $E_i = E_v + E_g/2$. Moreover, $n_c p_v$ is constant for a fixed temperature and gap energy, and it holds not only for intrinsic semiconductors. It is convenient to define the intrinsic charge carrier concentration $n_i$, with $n_i = \sqrt{n_c p_v}$. For silicon at room temperature $E_g = 1.12$ eV, $m^*_{e,DOS} = 1.08 m_e$ and $m^*_{h,DOS} = 0.65 m_e$, with $m_e$ the electron mass. Thus, the intrinsic charge-carrier density of silicon is $n_{i,Si} \approx 9.65 \times 10^9$ cm$^{-3}$ [1][8].

The intrinsic carrier density is too small for many applications. To increase the number of charge carriers at room temperature, impurity atoms (dopants) can be introduced to create ***doped*** or ***extrinsic semiconductors***. There are two types of dopants, donors and acceptors. For silicons, the donor is attributed to the elements with five valence electrons (e.g. phosphorus) that substitutes a silicon atom in the lattice, and the extra electron loosely bound to the donor atom has a low ionisation energy

[1] This value was cited in [6]. An older but also commonly used value is $n_{i,Si} \approx 1.01 \times 10^{10}$ cm$^{-3}$ which was determined in 1993 [7]. Prior to 1990s, $n_{i,Si} \approx 1.45 \times 10^{10}$ cm$^{-3}$ was used, see [7, 8]

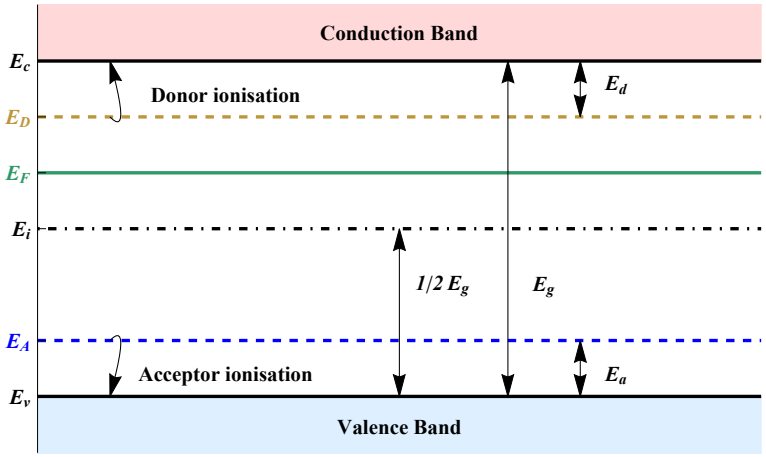



Figure 2.4: Simplified band scheme of a doped semiconductor. The vertical direction represents the energy. The introduction of dopants can be understood as adding extra energy levels $E_D$, $E_A$ in the band gap with respect to the ionisation energies $E_d, E_a$. With sufficient thermal energy, the electrons/holes can be excited from dopant levels to the conduction/valence band via ionisation.

$E_d$. At room temperature, the thermal energy is sufficient to ionise donors, so that they contribute electrons to the conduction band. After ionisation, the positively charged donor atom contributes a ***space charge*** which is fixed in the lattice. Similarly, the acceptors have three valence electrons (e.g. boron), contribute holes to the valence band, and have negative space charge. The semiconductor mainly doped with donors/acceptors is called "n-type"/"p-type", which is characterised by the doping concentration $N_D/N_A$. Typically, the doping concentration is several orders of magnitude higher than $n_i$.

A simplified energy band scheme, as shown in figure 2.4, is in many cases sufficient for discussing the electrical properties of semiconductor devices. $E_D$, $E_A$ represent the energy levels of donor and acceptor, and $E_d = E_c - E_D$, $E_a = E_A - E_v$ are the corresponding ionisation energies. In n-type silicon ($N_D >> N_A$), the electron is the majority charge carrier with $n_c \approx N_D$ for $k_B T \geq E_d$ assuming that all donors are ionised. Consequently, the Fermi level is also changed to $E_F \approx E_c - k_B T \ln\left(n_c^{eff}/N_D\right)$, which lies above the intrinsic Fermi-level $E_i$. It is analogous for p-type silicon.

## 2.3 Charge Carrier Transportation

The electric current is a result of the charge carrier transport, which is generally described by the ***continuity equations***

$$\begin{aligned} \frac{\partial n_c}{\partial t} &= \frac{1}{q}\nabla \cdot \mathbf{J}_n + G_n - R_n \,, \\ \frac{\partial p_v}{\partial t} &= -\frac{1}{q}\nabla \cdot \mathbf{J}_p + G_p - R_p \,, \end{aligned} \tag{2.5}$$

for electrons and holes with $q$ the elementary charge. These equations describe that the temporal change in the charge carrier densities $n_c/p_v$ for electrons / holes can be expressed as the divergence

of the current density $\mathbf{J}_{n/p}$ together with the generation rate ($G_{n/p}$) and recombination rate ($R_{n/p}$) of the charge carriers. A commonly used model to express the charge carrier current density in semiconductor is the ***drift-diffusion model***

$$\begin{aligned} \mathbf{J}_n &= \mathbf{j}_{\mathrm{D},n} + \mathbf{j}_{\mathrm{T},n} \,, \\ \mathbf{J}_p &= \mathbf{j}_{\mathrm{D},p} + \mathbf{j}_{\mathrm{T},p} \,. \end{aligned} \tag{2.6}$$

The total current density $\mathbf{J}_{\mathrm{n/p}}$ consists of the drift current density $\mathbf{j}_{\mathrm{D},n/p}$ and the diffusion current density $\mathbf{j}_{\mathrm{T},n/p}$. The motion of charge carriers driven by an electric field $\mathbf{E}$ presented in a semiconductor delivers the drift current. The total drift current density consisting of the electrons and holes is given as

$$\mathbf{J}_{\mathrm{D}} = q(n_c\mu_e + p_v\mu_h)\mathbf{E} = q(n_c\mathbf{v}_{\mathrm{D},e} + p_v\mathbf{v}_{\mathrm{D},h}) \,, \tag{2.7}$$

where $\mu_e = e\tau_{\mathrm{D},e}/m_e^*$ and $\mu_h = e\tau_{\mathrm{D},h}/m_h^*$ are the mobilities of electrons and holes with $\tau$ the mean free time and $m^*$ the effective mass. For silicon at $T = 300\,\mathrm{K}$, $\mu_e = 1400\,\mathrm{cm}^2/\mathrm{V}$ and $\mu_h = 450\,\mathrm{cm}^2/\mathrm{V}$ [9]. The mobilities can be treated as constant at low electric fields, so that the drift velocity $\mathbf{v}_{\mathrm{D}} = \mu_{\mathrm{D}}\mathbf{E}$ is proportional to the field strength. When the electric field is sufficiently high, the mobility of electrons depends nonlinearly on the electric field and the drift velocity starts to saturate. A phenomenological function of the drift velocity for electrons or holes is given as

$$|\mathbf{v}_{D,e/h}|(\mathbf{E},T) = v_{m,e/h}\frac{|\mathbf{E}|/E_{c,e/h}}{[1+(|\mathbf{E}|/E_{c,e/h})^{\beta_{e/h}}]^{1/\beta_{e/h}}} \,, \tag{2.8}$$

with temperature-dependent parameters: $v_{m,e/h} = 1.53\times10^9\times T^{-0.87}\,\mathrm{cm/s}$, $1.62\times10^8\times T^{-0.52}\,\mathrm{cm/s}$; $E_{c,e/h} = 1.01\times T^{1.55}\,\mathrm{V/cm}$, $1.24\times T^{1.68}\,\mathrm{V/cm}$; $\beta_{e/h} = 2.57\times10^{-2}\times T^{0.66}$, $0.46\times T^{0.17}$ [10]. Moreover, the drift velocity depends on the doping concentration, too. The phenomenological model of this can be found in [10, 11].

Besides drifting, the motion of charge carriers can also be caused by the density gradient, which is called diffusion. The total diffusion current density can be expressed using Fick's law, as

$$\mathbf{j}_T = q(D_n\nabla n_c + D_p\nabla p_v) \,, \tag{2.9}$$

with the diffusion constants $D_n = 36\,\mathrm{cm/s}^{-1}$, $D_p = 12\,\mathrm{cm/s}^{-1}$ for silicon at 300 K [9].
The generation and recombination of charge carriers have various origins, for instance, impact ionisation, and trapping or emission of charge carriers due to defect energy levels in the band gap. The occurrence of these effects can strongly influence the performance of the silicon devices in application.

## 2.4 p-n Junction

A p-n junction is formed at the interface of adjoined p-type and n-type semiconductors (Figure 2.5 (a)). The majority charge carriers in both types diffuse across the interface due to the density gradient, forming diffusion currents. These charge carriers undergo recombination processes, and leave a space charge zone (***depletion zone***) around the junction with positive charge on the n-type side and negative charge on p-type side. Space charges form an electric field (Figure 2.5 (b)), which drives the charge carriers and forms drift currents. At thermal equilibrium, the net current across the junction vanishes

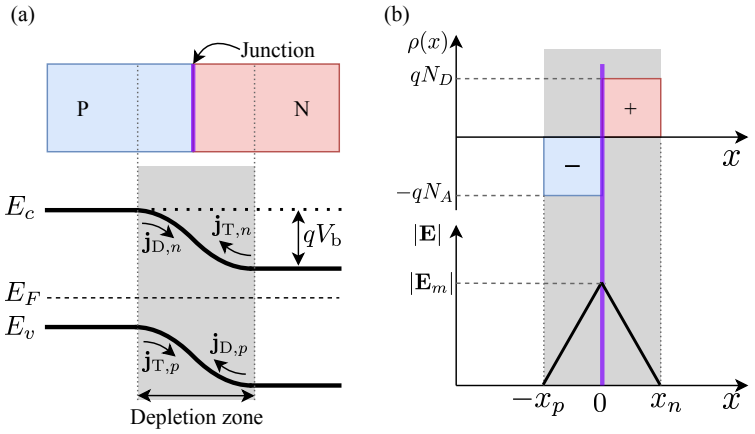



Figure 2.5: (a) p-n junction formed at the interface when n- and p-types of silicon are brought into contact. The Fermi-level is flattened at the thermal equilibrium, so that a band bending is created. The sum of the diffusion currents ($\mathbf{j}_{\mathrm{T},n}$ and $\mathbf{j}_{\mathrm{T},p}$) and the drift currents ($\mathbf{j}_{\mathrm{D},n}$ and $\mathbf{j}_{\mathrm{D},p}$) is zero in this condition. A depletion zone is formed around the p-n junction due to the recombination of charge carriers. A net leakage current is nevertheless present, due to the charge carrier generation in the depletion region. (b) The electric field ($|\mathbf{E}|$) in the depletion zone is determined by the space charge ($\rho(x)$), and it peaks at the p-n junction.

and leads to an overall constant $E_F$. This results in a band bending around the p-n junction, where the energy difference of the bands between the p and n side determines the so called ***built-in voltage*** $V_b$. Figure 2.5 (b) illustrates the space charge distribution and the electric field in the depletion zone for a one dimensional p-n junction. For simplicity, the space charge concentrations on the boundaries of the depletion zones (i.e. at $x = -x_n, x_p$) and at the junction are considered as step functions, whose gradients are finite in practice. Due to the charge neutrality of the material, the integral of $\rho(x)$ over the depletion region equals to zero. The electric field is calculated by integrating $\rho(x)$, according to the Poisson equation. The extremum of the field strength ($|\mathbf{E}_m|$) is located at the junction, where

$$|\mathbf{E}_m| = \frac{qN_A x_p}{\epsilon_r \epsilon_0} = \frac{qN_D x_n}{\epsilon_r \epsilon_0}, \tag{2.10}$$

with $\epsilon_r$ the relative, and $\epsilon_0$ the vacuum permittivity. The junction is biased after applying an external voltage (***bias voltage***) $V_{\mathrm{bias}}$. The froward bias (Figure 2.6 (a)) represents the condition that the potential at the p-side is higher than the n-side ($\phi_p > \phi_n$). The drift current of the majority charge carriers, driven by the external electric field, dominates the total current. As a result, the space charge region vanishes and a current flows across the junction. By reversing the polarity of the bias voltage ($\phi_p < \phi_n$, Figure 2.6 (b)), the reversed electric field leads to a depletion of majority charge carriers, and a growth of the space charge region. Therefore, there is only a small current across the junction, the ***leakage current***, due to the charge carrier generation processes taking place in the depletion zone. These basic properties of p-n junctions have helped to build the p-n diodes, bipolar transistors, etc., which are the building blocks of semiconductor electronics.

Silicon detectors for HEP make use of the reverse biasing condition of p-n junctions. The low charge carrier density, low current, and the electric field in the depletion region are beneficial for extracting the charge carriers generated by photons or charged particles. A monotonic electric field

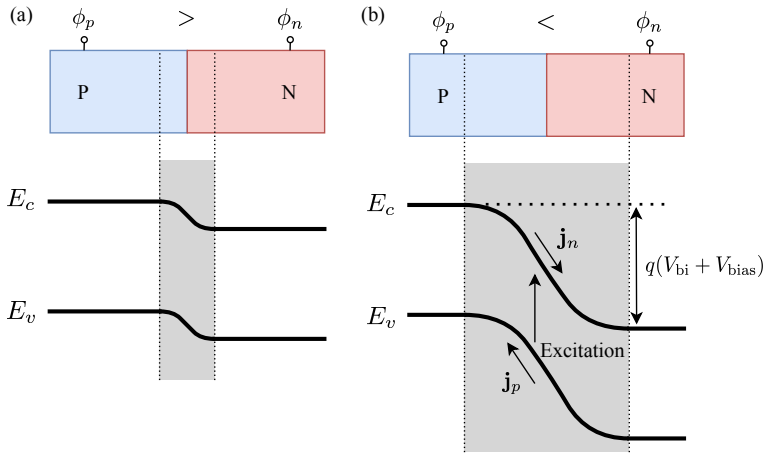



Figure 2.6: P-n junction after applying bias voltages. (a) forward bias, where the depletion region starts to decrease, in comparison with the thermal equilibrium. (b) reverse bias, with an increased depletion region. The net current (leakage current) across the junction is contributed by the electron-hole pair generation in the depletion region. The difference of the conduction band energy between both types of silicon is given as the sum of the build-in voltage and the bias voltage, with $V_{\text{bias}} = \phi_n - \phi_p$.

and a sufficiently large depletion region are usually preferred in the sensors. The generic design of a silicon sensor is a p-n junction with $N_D >> N_A$, which leads to $x_n << x_p$. Thus,

$$d \approx x_p \approx \sqrt{\frac{2\epsilon_r \epsilon_0}{e}(V_b + V_{\text{bias}})\frac{1}{N_A}} \tag{2.11}$$

gives the relation between depletion depth $d$ and acceptor doping concentration $N_A$ in p-type silicon [12]. The growth of the depletion zone under reverse biasing stops until the p-type silicon is fully depleted when the bias voltage reaches the ***full-depletion voltage*** $V_{\text{FD}}$. The junction is over-depleted if $V_{\text{bias}} > V_{\text{FD}}$, and it results in a higher electric field in the depletion region. A sufficiently high electric field strength can cause impact ionisation of charge carriers, and further cause avalanche breakdown [6, 12], which will be introduced in more detail in section 2.6.

## 2.5 MOS and MOSFET

MOS stands for the three-layer structure Metal-Oxide-Silicon [1], which is of great importance to the modern semiconductor devices due to its ability to modify the electrical property of the $Si/SiO_2$ interface. MOS capacitors are direct applications utilising the MOS structure, where a thin oxide layer separates the gate (metal) and the substrate (silicon). The capacitance can be varied by controlling the potential difference between the gate and substrate. The most popular application using the features of MOS structures is the Metal-Oxide-Silicon Field Effect Transistor (MOSFET).

Same as the discussion for p-n junctions, a constant $E_F$ across the three layers of MOS structure,

[1] The acronym "MOS" can refer to "Metal-Oxide-Semicondutor", as well. In general, the features that discussed in this section applies to Metal-Insulator-Semiconductor structures.

and a band bending of the silicon at the Si-$SiO_2$ interface are formed at thermal equilibrium (Figure 2.7 (a)). The characteristic parameters in such band diagram are

- the electron affinity $\chi_{Si,SiO_2}$, defined as the distance between $E_c$ and the vacuum level $E_0$ for both the silicon and silicon oxide;
- the work function $\psi_{Si,g}$, defined as the the distance between $E_F$ and $E_0$ for the silicon and metal gate.

The band bending will be flattened after applying a voltage between gate and substrate (gate voltage $V_g$) with the magnitude of $V_{fb} = \psi_g - \psi_{Si}$, namely the flat-band voltage of the flat-band condition (Figure 2.7 (b)). In general, the gate voltage can be written as the sum of the flat-band voltage $V_{fb}$, the surface potential $\phi_s$, and the oxide voltage $V_{ox}$, as

$$V_g = V_{fb} + \phi_s + V_{ox} \,. \tag{2.12}$$

This equation merely gives the relation between those values, where $V_{fb}$ is a material parameter, $V_g$ is an independent variabel which is steered in the application, and $\phi_s + V_{ox}$ is the response variable. In the flat-band condition, $\phi_s + V_{ox} = 0$. Further lowering $V_g$ beyond $V_{fb}$ leads to the surface accumulation condition (Figure 2.8 (a)). The majority charge carriers (holes) of the p-type substrate accumulate at the surface of the substrate, resulting in a hole concentration much larger than in the substrate. This effect reflected in the band diagram is an upwards bending of the silicon band structure and a negative $V_{ox}$ ($\phi_s + V_{ox} < 0$). Changing the polarity of $V_g$ ($V_g > V_{fb}$ and $\phi_s + V_{ox} > 0$) depletes the silicon surface, as the band bending increases the distance between $E_F$ and $E_v$ (Figure 2.8 (b)). When $V_g$ is sufficiently high, $E_c$ and $E_F$ are brought so close to each other, that the electrons accumulate at the surface of silicon (Figure 2.8 (c)). The accumulated electrons can be seen as a thin n-type layer beneath the oxide. The transition between surface depletion and inversion is characterised by

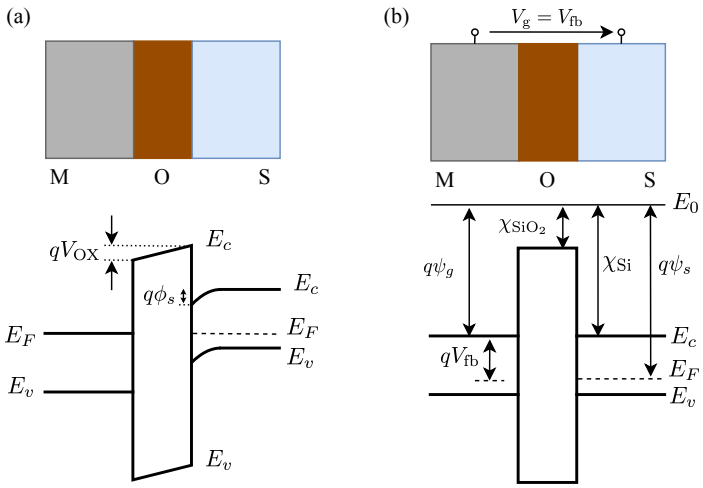



Figure 2.7: MOS structure and the band diagram at (a) the thermal equilibrium and (b) the flat-band condition. The above sketches shows the 3-layer Metal (M) - Oxide (O) - (p-type) Silicon (S) structure. In the band diagram below, the energies of the conduction band and the valence band are indicated for three materials. See the text for more details.

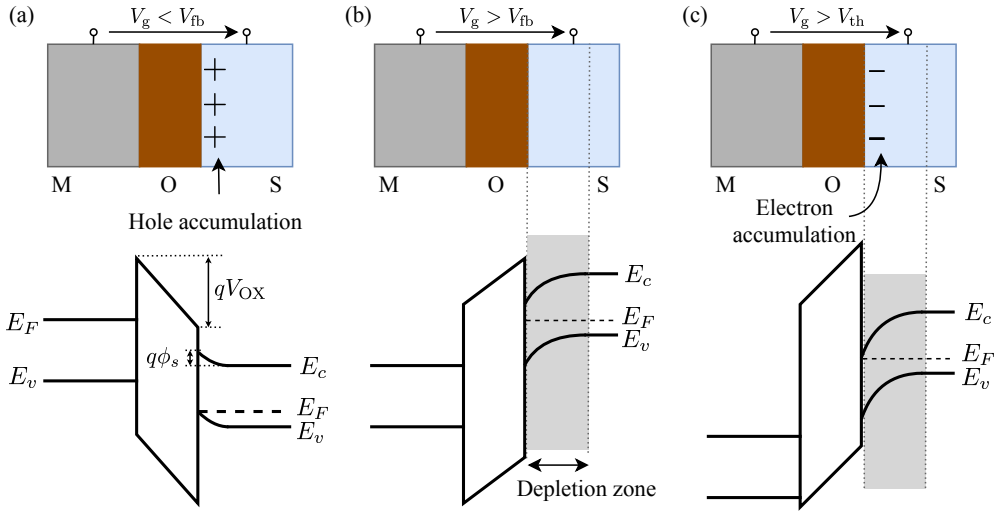



Figure 2.8: MOS structure and the band diagram at (a) the surface accumulation, (b) the surface depletion, and (c) the inversion condition.

the threshold voltage $V_{\text{th}}(= V_{\text{g}})$, at which the concentration of the accumulated electron equals the substrate doping concentration (i.e. the hole concentration in the substrate, assuming a full ionisation of dopants). This indicates that the surface potential $\phi_{\text{s}}$ must fulfil the condition

$$\phi_{\text{s}}^{\text{th}} = 2\frac{k_B T}{q} \ln\left[\frac{N_A}{n_{i,Si}}\right], \tag{2.13}$$

according to equation (2.3) and (2.4). At the same time, the depletion depth in the silicon substrate reaches the maximal value

$$W_{\text{max}} = \sqrt{\frac{2\epsilon_{Si}\phi_{\text{s}}^{\text{th}}}{qN_A}}. \tag{2.14}$$

Increasing $V_{\text{g}}$ beyond the threshold voltage results in a build up of electrons (inversion layer) in the silicon substrate at the interface. The charge of the inversion layer $Q_{\text{inv}}$ is proportional to $V_{\text{g}}$

$$Q_{\text{inv}} = -C_{\text{ox}}(V_{\text{g}} - V_{\text{th}}), \tag{2.15}$$

where the $C_{\text{ox}}$ is the capacitance of the oxide layer.

The schematic structure of an n-MOSFET [1] is illustrated in Figure 2.9 (a), where two n-type electrodes (source and drain) are located on both sides of an MOS structure on a p-type substrate. Taking the grounded source and substrate as the reference potential, the gate voltage $V_{\text{g}}$ can modulate the current between drain and source ($I_{\text{ds}}$) with an existing drain-source voltage $V_{\text{ds}}$ (Figure 2.9 (b)). $I_{\text{ds}}$ starts to increase with $V_{\text{g}}$ after passing the threshold $V_{\text{th}}$ of the MOS structure, since the inversion layer (a thin layer of electron) at the surface of substrate builds up a conductive channel for the n-type electrodes. Sweeping $V_{\text{ds}}$ for various $V_{\text{g}}$ values gives three different types of current responses (Figure

[1] The p- or n-type of MOSFET is named after the type of electrodes. A p-MOSFET has p-type electrodes, and the conductivity is mainly contributed by the holes.

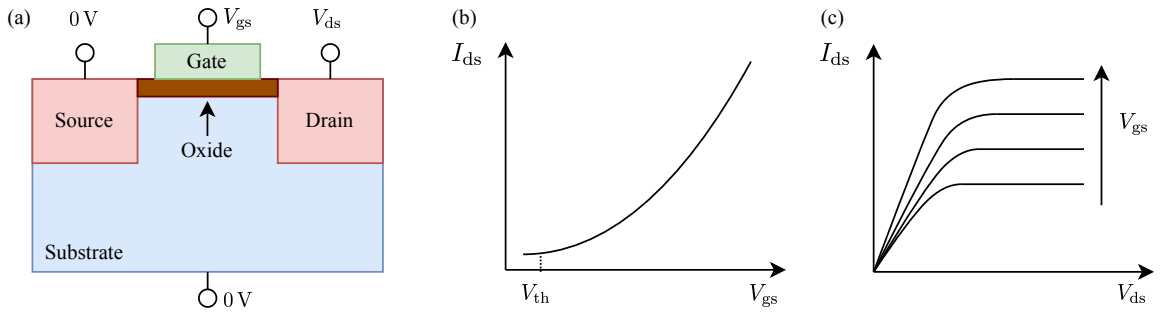



Figure 2.9: (a) The structure of an n-MOSFET, where the n-type electrodes (source and drain) are fabricated on a p-type substrate. The source and the substrate are at the ground potential, whereas $V_{gs}$ represent the gate voltage (relative to source), and $V_{ds}$ represent the drain-source voltage. (b) A sketch of the characteristic line, where the drain source current $I_{ds}$ is plotted as a function of $V_{gs}$. (c) A sketch of the characteristic lines for $I_{ds}$ as a function of $V_{ds}$ for various $V_{gs}$ values.

2.9 (c)): 1) linear region for small $V_{ds}$, 2) non-linear region with higher $V_{ds}$, and 3) saturation region. For small $V_{ds}$, the conducting channel with uniform electron concentration acts as a resistor, so that a proportionality between voltage and current is revealed. With increasing $V_{ds}$, the local potential distribution in the surface region between gate and drain starts to reduce the local charge concentration. Eventually, $V_{ds}$ is high enough to reduce the inversion charge at the drain end to zero (pinch-off point). Further increasing $V_{ds}$ causes a movement of pinch-off point towards the source, however, the number of charge carriers which moves from the source to the pinch-off point stays the same. Therefore, a constant current can be observed.

## 2.6 Generation and Recombination

In addition to the charge carrier transportation within the valence or conduction bands due to electric field or concentration gradient, the exchange of carriers across the band gap through generation and recombination processes is crucial for understanding the properties of semiconductors and developing semiconductor devices, as well. To excite an electron from the valence band requires an energy greater than the band gap, which is $E_g \approx 1.12\,\text{eV}$ for silicon. Such excitation processes can be realised via thermal (leakage current), optical (photon absorption), electrical field generation (impact ionisation) processes, or by high-energy charged particles or photons. The recombination of excited electrons and holes will lead to an emission of energy in the form of luminescence (photon emission) or phonon (non-radiative) [13, 14]. The first part of this section will introduce the recombination model for the process related to defect energy levels in the band gap (***Shockley-Read-Hall (SRH) recombination)***, which is the main process of non-radiative recombination [14], and crucial for the high energy particle detectors after radiation damage. Impact ionisation will be introduced in the second part of this section. It can trigger the so-called avalanche effect inside a semiconductor device with applied voltages, so that it is important for determining the operational condition or limit of devices. On one hand, the avalanche effect can cause the breakdown of devices (e.g. the p-n junctions). But on the other hand, such an effect can induce a larger amount of charge carriers, which can be beneficial for certain applications.

### 2.6.1 Shockley-Read-Hall Statistics

As the band structure and the band gap of semiconductors are the results of a periodic crystal structure, a large amount of imperfections in crystals can distort the periodicity and influence the electrical properties. The energy levels (defect levels) in the band gap are a result of the defects in crystal, and can increase the probability of the inter-band transition of charge carriers. The model of the SRH recombination adopts the SRH statistics, which is based on four processes [15, 16]: electron capture (trapping), electron emission (de-trapping), hole capture and hole emission as illustrated in Figure 2.10.

Considering one defect level with energy $E_t$ and concentration $N_t$, the concentration of the empty

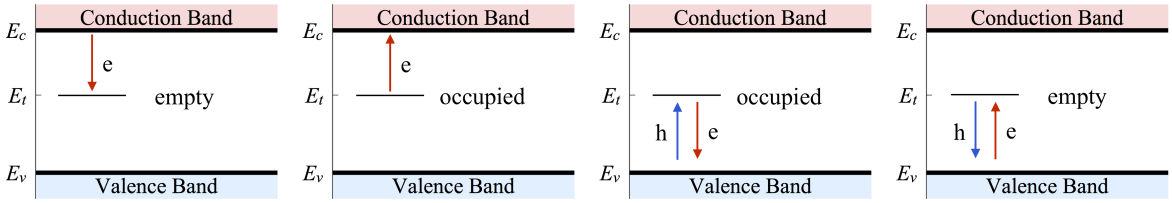



Figure 2.10: The basic processes involved in recombination through traps. The defect level is denoted by its energy $E_t$ and its status "empty" or "occupied" is in terms of the electron. (a): electron capture; (b): electron emission; (c): hole capture; (d): hole emission. Capturing/emitting an electron is equivalent to emitting/capturing a hole.

defect level in terms of electrons is given as $(1 - f_t)N_t = f_{pt}N_t$ with the Fermi-Dirac distribution $f_t = f(E_t, T)$. With an average single-electron capture rate per trap centre $c_n$ (i.e. capture coefficient), the total capture rate of electrons with concentration $n$ is obtained as

$$r_{n,c} = f_{pt}N_t c_n n \, . \tag{2.16}$$

The value of $c_n$ is determined by the thermal velocity $v_{\text{th}}$ and capture cross section $\sigma_n$ [2] through $c_n = v_{\text{th}}\sigma_n$, with the assumption that the thermal velocity is much higher than the drift velocity (see also [17]). Adopting a similar rule for the emission process, the total electron emission rate of level $E_t$ can be obtained as

$$r_{n,e} = f_t N_t e_n \tag{2.17}$$

with the emission coefficient $e_n$. Analogously, the capture ($r_{p,c}$) and emission ($r_{p,e}$) rate of holes are acquired as

$$\begin{aligned} r_{p,c} &= f_t N_t c_p p \, , \\ r_{p,e} &= f_{pt} N_t e_p \, . \end{aligned} \tag{2.18}$$

[2] In general, the capture cross section and capture rate are functions of electron energy [15].

Combining the recombination and generation rate in equation (2.6), a net recombination rate from the SRH model, $U_{n,p} = G_{\mathrm{SRH},n,p} + R_{\mathrm{SRH},n,p}$, can be defined as

$$\begin{aligned} U_n &= r_{n,c} - r_{n,e} \,, \\ U_p &= r_{p,c} - r_{p,e} \,, \end{aligned} \tag{2.19}$$

if only the trap is considered as the only significant source of generation and recombination. So, $U < 0$ indicates a net generation and $U > 0$ indicates a net recombination.

The emission rate in thermal equilibrium ($U_{n,p} = 0$) can be expressed as

$$\begin{aligned} -f_{pt} N_t c_n n + f_t N_t e_n = 0 \quad &\xrightarrow{(2.3)} \quad e_n = c_n N_t n_i \exp\left(\frac{E_t - E_i}{k_B T}\right), \\ -f_t N_t c_p p + f_{pt} N_t e_p = 0 \quad &\xrightarrow{(2.3)} \quad e_p = c_p N_t n_i \exp\left(-\frac{E_t - E_i}{k_B T}\right). \end{aligned} \tag{2.20}$$

At steady states, the net recombination rates of electrons and holes are the same, i.e. $U_n = U_p = U$. Thus by applying Eq. (2.20) and (2.19), the occupancy of defect level $E_t$ can be given by

$$f_t(E_t, T) = \frac{c_n n + c_p n_i \exp\left(\frac{E_i - E_t}{k_B T}\right)}{c_p \left[p + n_i \exp\left(\frac{E_i - E_t}{k_B T}\right)\right] + c_n \left[n + n_i \exp\left(-\frac{E_i - E_t}{k_B T}\right)\right]} \,, \tag{2.21}$$

as a function of parameters $c_{n,p}$ (assuming constant $e_{n,p}$ and $c_{n,p}$), $E_t$, and $T$.

According to Eq.(2.21), $U$ at steady states is given as

$$U = \frac{np - n_i^2}{\tau_{n0}\left[p + n_i \exp\left(\frac{E_i - E_t}{k_B T}\right)\right] + \tau_{p0}\left[n + n_i \exp\left(-\frac{E_i - E_t}{k_B T}\right)\right]} \,, \tag{2.22}$$

where $\tau_{n0,p0} = 1/(N_t c_{n,p})$ are defined as the lifetimes for electrons/holes in the very high doping p/n type silicon [15].

#### Dependence on Electric Field, Temperature, and Doping Concentration

The recombination rate calculated as Eq. 2.22 can be influenced by temperature, doping concentration, and electric field. The modelling of such effects can be integrated into the SRH recombination model by replacing $\tau_{n0,p0}$ in Eq. 2.22 with

$$\tau_{n,p} = \tau_{\mathrm{Doping},n,p} \frac{f(T)}{1 + g_{n,p}(\mathbf{E})} \,. \tag{2.23}$$

$g_{n,p}(\mathbf{E})$ denotes the field enhancement factor, $f(T)$ describes the temperature dependence, and $\tau_{\mathrm{Doping}}$ represents the doping concentration modified charge carrier lifetime [18]. The recombination of the charge carriers is assumed to be a multi-phonon process, where the charge carriers interact with

phonons and result in a vertical recombination path in the band diagram. The trap-assisted tunnelling (TAT) process is an essential concept in the field-dependent lifetime calculation. The high electric field enhances the generation and recombination of charge carriers through the tunnelling via trap levels within the band gap [19], which can be modelled by the Hurkx TAT model [20]. This is particularly interesting for simulating the reverse biased diode structure, where a high electric field can occur. The temperature-dependent factor $f(T)$ is derived from the zero-field condition of the expression for the charge carrier lifetime [19], showing a reciprocal relation between the lifetime and the temperature. The effect of the doping concentration originates from the solubility of a fundamental (unavoidable) acceptor-like defect level in silicon crystal, which is strongly correlated with the doping concentration [18, 21]. This effect in the model influences the lifetime $\tau_{n,p}$ disregarding the field and temperature effect, which is expressed by the Scharfetter relation [18].

### 2.6.2 Band to Band (B2B) Tunnelling

A direct tunnelling of charge carriers across the semiconductor band gap can take place when a high electric field occurs ($\gtrsim 7 \times 10^5$ V/cm [20]) across the p-n junction. In silicon, which has an indirect band gap, the most probable B2B tunnelling of charge carriers takes place between both extrema of the band edges, where multiple phonons are involved in this transition [22]. This effect is an important source of the current increase in a narrow p-n junction, where the doping concentration is greater than $5 \times 10^{17}\,\mathrm{cm}^{-3}$, representing a breakdown voltage lower than 5 V [20, 22].

However, in silicon, TAT often plays a more substantial role than B2B tunnelling at lower electric fields due to its higher probability under such conditions [22]. At lower doping concentrations, the generation of charge carriers is predominantly governed by impact ionisation [6].

### 2.6.3 Impact Ionisation and Avalanche Generation

As a fundamental mechanism of charge carrier generation, impact ionisation involves the transition of an electron from the valence band to the conduction band, a process termed ionisation. This transition results in the creation of a free electron in the conduction band and a corresponding hole in the valence band. The initiation of impact ionisation requires charge carriers to attain sufficiently high energy, typically facilitated by their acceleration in a high electric field. When the space charge region exceeds the mean free path between two ionising collisions, a cascade effect ensues, allowing both primary and secondary charge carriers to partake in further impact ionisation events. This phenomenon, known as avalanche generation or charge multiplication, significantly amplifies the number of charge carriers. The generation rate of impact ionisation is generally described as

$$G^{\mathrm{II}} = G_n^{\mathrm{II}} + G_p^{\mathrm{II}} = \alpha_n n |\mathbf{v}_{D,n}| + \alpha_p p |\mathbf{v}_{D,p}|\,, \tag{2.24}$$

where $\alpha_n$ and $\alpha_p$ denote the ***ionisation coefficient*** or ionisation rate of electrons and holes, respectively. [23]

The macroscopic effect of the impact ionisation is an increase in the current (density) of the semiconductor device. For a quantification, the ***multiplication factor*** of the impact ionisation is defined as

$$M_{n,p} = \frac{|\mathbf{J}_{n,p}^{\mathrm{final}}|}{|\mathbf{J}_{n,p}^{\mathrm{initial}}|}\,, \tag{2.25}$$

with the initial current density $\mathbf{J}_{n,p}^{\text{initial}}$ and the current density after the impact ionisation processes $\mathbf{J}_{n,p}^{\text{final}}$, for electrons and holes. Using the continuity equations, the relation between the multiplication factor and the impact ionisation coefficient can be derived as

$$M_n = \frac{1}{1 - \int_0^d \alpha_n \exp\left[-\int_0^x (\alpha_n - \alpha_p)\mathrm{d}x'\right]\mathrm{d}x}, \tag{2.26}$$

$$M_p = \frac{1}{1 - \int_0^d \alpha_p \exp\left[-\int_x^d (\alpha_p - \alpha_n)\mathrm{d}x'\right]\mathrm{d}x}, \tag{2.27}$$

for electrons and holes for a 1-dimensional p-n junction [24]. The integrals in these equations contain the ionisation rate of electrons/holes ($\alpha_{n/p}$), and the integration range is the full depletion width $d$. They represent the case that the charge carrier travels through the entire depletion region.

#### Modelling the Ionisation Coefficient $\alpha$

Studies of the impact ionisation in semiconductors started shortly after the first clear evidence of such an effect in 1953 [25] and continued over decades, providing a vast amount of models [26]. Various theories and experimental results have pointed to an exponential relation between $\alpha$ and the electric field $\mathbf{E}$. The so-called "Chynoweth's law" [27] gives a simple empirical expression of $\alpha(\mathbf{E})$, as

$$\alpha_{n,p} = \alpha_{n,p}^{\infty} \exp\left[-\frac{b}{|\mathbf{E}|}\right]. \tag{2.28}$$

$\alpha_{n,p}^{\infty}$ denotes the saturation ionisation rate for infinitely high electric fields; $b$ is the critical electric field (also denoted as $\mathbf{E}_{\text{i}}$) for impact ionisation. This model has been proven to describe the measurement results in many studies well [23]. Among them, the parameter set (Table 2.1) published by van Overstraeten and de Man [28], which was extracted based on the measurements of a large set of different diodes (electric field profiles), is widely used and seems to give the best simulation results [29].

| **Type** | $\alpha_{n,p}^{\infty}$ **(1/cm)** | $b_{n,p}$ **(V/cm)** | **Electric field range**(V/cm) |
|---|---|---|---|
| Electron | $7.03 \times 10^5$ | $1.231 \times 10^6$ | $1.75 \times 10^5 \leq \lvert\mathbf{E}\rvert \leq 6.0 \times 10^5$ |
| Hole | $1.582 \times 10^6$ | $2.036 \times 10^6$ | $1.75 \times 10^5 \leq \lvert\mathbf{E}\rvert \leq 4.0 \times 10^5$ |
| | $6.71 \times 10^5$ | $1.693 \times 10^6$ | $4.0 \times 10^5 \leq \lvert\mathbf{E}\rvert \leq 6.0 \times 10^5$ |

Table 2.1: The van Overstraeten – de Man model for the impact ionisation coefficients of electrons and holes in silicon. [28]

## 2.7 Junction Breakdown

The breakdown effect occurs when a sufficiently high electric field is applied across the p-n junction in the reverse biasing condition, creating a very large current and very rapid current increase via

the tunnel effect or avalanche generation. A few semiconductor devices, such as the Zener diode [30] (exploiting the tunnel effect for voltage regulation) and the Esaki diode [31] (utilising quantum tunnelling for negative resistance properties) , utilise this effect for specialised functionalities. For most devices, however, the breakdown of p-n junctions can cause malfunctions or even destroy the device. Characterising the breakdown condition of a semiconductor device is crucial for understanding the limit of sustainable operation voltage. For silicon pixel sensors, the breakdown voltage can be used to evaluate the upper bound of the applicable bias voltage of the sensor, since a large depletion region and a high electric field are preferred. Thermal instability, tunnelling, and avalanche effect are the basic mechanisms causing the junction breakdown [6].

In semiconductors, the thermal instability is a major effect causing the breakdown of the materials with a relatively small band gap. The leakage current in the high reverse bias voltage leads to heat dissipation, which increases the junction temperature. Subsequently, the leakage current is increased by the higher temperature. These effects forms a positive feedback loop, which results in a rapid increase of current (junction breakdown) and a high temperature (thermal instability or thermal runaway). If no special measure is implemented, for instance connecting a large resistor in series to limit the current, the diode can be destroyed by such an effect.

Usually, when the doping concentration of the p-type and the n-type semiconductor in the p-n junction is high, and the energy band at the junction is strongly bended under high reverse bias voltage (high electric field approaching $1 \times 10^6$ V/cm), the band-to-band tunnelling process of charge carriers takes place. Since such strongly bended energy band stretches the band gap in the junction region and results in a slim band gap (as a potential barrier for charge carriers), the tunnelling probability increases, and this will lead a significant current across the junction. Typically, the pure tunnelling effect will deliver a breakdown voltage less than $4E_g/q$ [6], depending on the gap energy of the material [3]. A bias voltage between $4E_g/q$ and $6E_g/q$ indicates a mixture of the tunnelling effect and the avalanche effect.

Avalanche effect or avalanche multiplication in semiconductors is caused by the impact ionisation of charge carriers in high electric field, where secondary charge carriers can further undergo the same process due to the high kinetic energy gained from the electric field, and cause an enormously large current. Due to the requirement of semiconductor sensors for HEP, the operating voltage (reverse bias voltage) of the p-n junction needs to be sufficiently high for a depletion depth from 10s to 100s of µm, which corresponds to a typical bias voltage much higher than $6E_g/q$. This makes the avalanche effect the most-important mechanism of the junction breakdown in pixel sensors. In the analytical perspective, the breakdown is defined as the multiplication factor $M_{n,p}$ approaching infinity, meaning that the integral in equations (2.26) and (2.27) approaches 1. By solving the integrals, the breakdown voltage can be obtained as a function of the maximum electric field and the doping profile of the considered p-n junction, which delivers estimations of the actual breakdown performance of devices [6]. The estimation of the breakdown performance can also be provided by numerical simulation of devices, by adopting the model of impact ionisation coefficient in the continuity equations.

[3] Approximately 4.48 V for silicon with $E_g = 1.12$ eV.

CHAPTER 3

# Silicon Pixel Detectors

Towards the late 1970s, the charm quark production studies in high energy physics (HEP) gave rise to demands particle detectors with a high spatial resolution, which should be able to provide identification and measurement of particles with short lifetimes [32]. After the first silicon detector for HEP was developed in 1980 [33], the semiconductor detector was continuously developed and employed as particle tracking detectors by a rising number of experiments. Silicon is the most preferred and well suitable among all kinds of semiconductor materials since its electrical properties are well-known and the mature manufacturing technology ensures a low cost as well as a mass production. A generic silicon pixel detector consists of the sensor part, a reversely biased p-n diode with finely pixelated electrodes, and the readout electronics using integrated circuits for each pixel. In comparison with gaseous detectors, silicon pixel detectors have more desired properties, such as high spatial resolution, small size and capability of high particle rate. Therefore, the pixel detector can be installed as close as possible to the centre of collision and is able to locate primary and secondary vertices of particle interactions.

## 3.1 Detection Mechanism

### 3.1.1 Interaction of Charged Particles with Matter

A relativistic charged heavy particle deposits energy in materials via ionisation or excitation of atoms or molecules. Since the energy deposition takes place along the particle track, the mean energy loss per penetration depth is adopted to quantify this phenomenon and expressed by the ***Bethe-Bloch formula***,

$$\left\langle -\frac{\mathrm{d}E}{\mathrm{d}x}\right\rangle = Kz^2\frac{Z}{A}\frac{1}{\beta}\left[\frac{1}{2}\ln\frac{2m_e c^2\beta^2\gamma^2 W_{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right], \tag{3.1}$$

as described in [34]. When specifying a material with density $\rho$, the ***linear energy transfer*** or **LET** (energy loss per centimetre) is calculated by $\langle -\mathrm{d}E/\mathrm{d}x\rangle \times \rho$. The Bethe-Bloch formula is valid with an accuracy of a few percent for charged particles with $0.1 \lesssim \beta\gamma \lesssim 1000$ [1] and charge $z$ that traverse

[1] $\beta\gamma = p/M$ is the ratio of the momentum $p$ and the mass $M$ of particles in natural unit. For instance, this range represents a momentum from approximately 0.01 GeV to 100 GeV for muons and pions, and for protons between approximately 0.1 GeV and 100 GeV.

materials with intermediate atomic number $Z$. The term with $\delta$ is the density correction that is important for high energies. Although the Bethe-Bloch formula depends on the types of materials and particles, the minimum value is generally found for $\beta\gamma \in [3, 3.5]$ with $\langle -\mathrm{d}E/\mathrm{d}x \rangle_{\mathrm{min}} \in (1, 2)$ MeV cm$^2$ g$^{-1}$.

Most relativistic particles have mean energy loss rates close to the minimum of the Bethe formula, thus they are named ***minimum-ionising particles*** or ***MIP's***. Considering a MIP traverses through silicon,

$$\mathrm{LET}_{\mathrm{MIP,Si}} = \left\langle -\frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle \Bigg|_{\mathrm{min,Si}} \times \rho_{Si} = -1.66 \, \frac{\mathrm{MeV\ cm^2}}{\mathrm{g}} \times 2.33 \, \frac{\mathrm{g}}{\mathrm{cm^3}} \approx -3.87 \, \frac{\mathrm{MeV}}{\mathrm{cm}} \tag{3.2}$$

is approximately the energy loss per centimetre at room temperature (i.e. $T = 300$ K) [12]. In semiconductors, this amount of energy will produce e-h pairs in clusters along the particle track. The number of the charge pairs is related to the mean energy needed for creating an e-h pair $E_{\text{e-h}}$. For silicon, $E_{\text{e-h}} \approx 3.65\,\mathrm{eV}$ [12].

At room temperature, the LET of a MIP in silicon is calculated by Eq. (3.2). With $E_{\text{e-h,Si}} = 3.65$ eV, a MIP will produce

$$N_{\text{e-h,Si}} = \frac{|\mathrm{LET}_{\mathrm{MIP,Si}}|}{E_{\text{e-h,Si}}} = \frac{3.87\,\mathrm{MeV/cm}}{3.65\,\mathrm{eV}} \approx 1.06 \times 10^6/\mathrm{cm} \tag{3.3}$$

e-h pairs within one centimetre, i.e. 110 e-h /µm [2].

The energy loss of charged particles in matter is a stochastic process, and the probability of deposited energy is described by the straggling function, the ***Landau distribution*** or Landau-Vavilov distribution [34, 35] (Figure 3.1). Due to the asymmetry of the Landau distribution, the used value to describe the energy loss is the most probable value (MPV) which is smaller than the mean value described by the Bethe-Bloch formula. According to measured data summarised in [34], the MPV of a MIP is $60 - 75\%$ of the mean energy loss for different thicknesses of silicon absorbers. More results from measurements and GEANT4 simulations [36] can be found in e.g. [37–39]. In practice, it is also common to use 80/µm to approximate the number of e-h pairs produced by a MIP in silicon [40].

### 3.1.2 Electrons and Photons

The mass of electrons (and positrons) ($\approx 0.5$ MeV) are much smaller than the masses of the other charged particles (e.g., $m_{\mathrm{muon}} \approx 106$ MeV), therefore the validity range of $\beta\gamma$ for the Bethe-Bloch formula represents the momenta between approximately 0.05 MeV and 500 MeV. The energy loss of high-energy electrons in matters is dominated by bremsstrahlung, which is also termed as radiative energy loss. In general, a ***critical energy*** $E_{crit}$ is defined to indicate the boundary between ionisation and radiative energy loss, where

$$\left\langle -\frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle_{\text{ionisation}} \Bigg|_{E=E_{crit}} = \left\langle -\frac{\mathrm{d}E}{\mathrm{d}x} \right\rangle_{\text{radiative}} \Bigg|_{E=E_{crit}} . \tag{3.4}$$

Beyond $E_{crit}$, the impinging particle predominantly exhibits radiative energy loss through bremsstrahlung, where photons are emitted from the interaction of impinging electrons with the nucleus of target

[2] In the field of detector physics, "µm" is preferred to be used as the unit of length since the size of semiconductor detector sensor is usually in the range of several hundreds of micrometres.

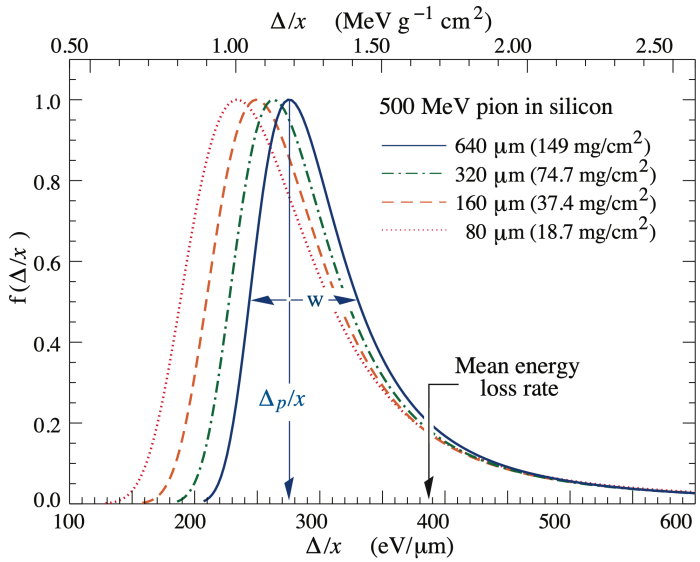



Figure 3.1: Straggling functions for 500 MeV pions in silicon with various thicknesses (mass per area). The distributions as a function of the energy loss rate ($\delta/x$) are normalised to unity at the most probable value (MPV) $\delta_p/x$. The quantity $w$ is the full width at half maximum. For the same particle beam, the mean energy loss rate is the same for all thicknesses. [34]

materials. The critical energy of electrons can be estimated as

$$E_c \approx \frac{610\,\text{MeV}}{Z + 1.24} \tag{3.5}$$

for solid and liquid targets [12], which yields a value for $E_{crit}$ in silicon ($Z = 14$) of approximately 40 MeV.

The energy of electrons decreases exponentially with the penetration depth $x$ in the target through bremsstrahlung, as

$$E(x) = E_0 \exp\left[-\frac{x}{X_0}\right] \tag{3.6}$$

with $E_0$ the initial energy of electrons, and $X_0$ the ***radiation length*** [34]. $X_0$ describes the travelling distance, after which the electron has $1/e$ of its initial energy. The radiation length is proportional to $1/\rho Z^2$ with $\rho$ the density of the target material, so it is also useful to characterise the thickness of the detectors in HEP [12].

Photons majorly exhibit three interactions in materials:

- **Photoeffect**: a photon with low energies (in the order of ~ keV) in materials predominately transfer their entire energy to atoms and release a shell electron. The interaction cross section of the photoeffect in general decreases with increasing photon energy (Figure 3.2). An abrupt jump of the cross section appears at $E_\gamma \approx 1.84$ keV indicating the K-shell edge of silicon atoms. This peak comes from the fact that the photons with energies slightly lower than the K-shell edge are not energetic enough to ionise the electrons in the K-shell. As long as the photon energy is sufficiently high (reaches the binding energy of electrons in the K-shell), the photoeffect

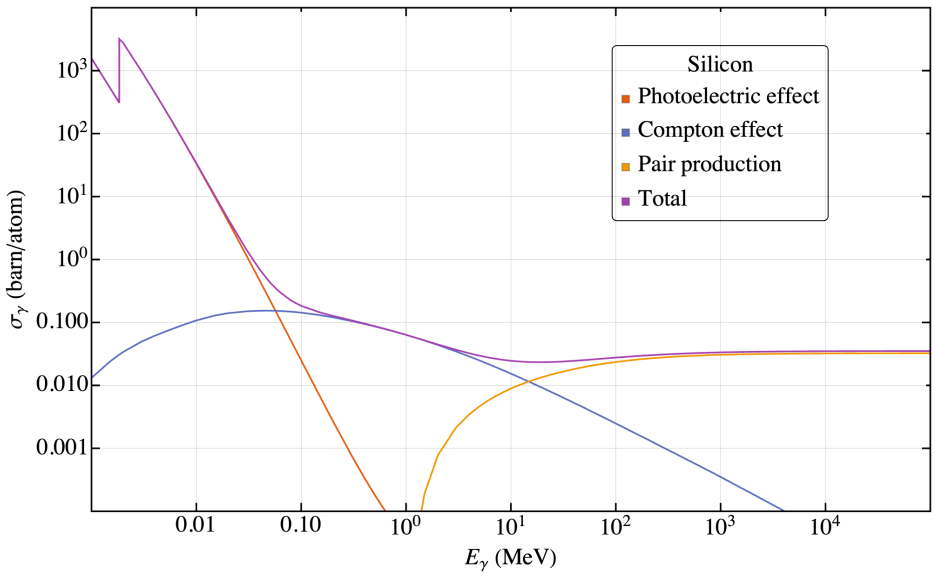



Figure 3.2: Interaction cross sections of photons with silicon. The contributions of 3 typical interaction types: photoeffect, Compton scattering, and pair production are presented in addition to the total cross section. Data obtained from [41].

for the K-shell takes place, and hence results in a high interaction cross section. The cross section of photoeffect is material (atomic number $Z$) and photon energy dependent ($E_\gamma$), and it is approximately proportional to $Z^n E_\gamma^{-k}$, with $n \approx 4\text{-}5$ and $k \lesssim 3.5$, depending on the photon energy [12].

- **Compton effect**: the elastic scattering between a photon and a shell electron leads to the energy transfer from the photon to the electron. As the cross section of photoeffect decreases with increasing $E_\gamma$, Compton scattering is significant for photons with energies around 1 MeV. The cross section of Compton effect is proportional to $ZE_\gamma^{-1}$ for $E_\gamma$ much larger than the electron mass.

- **Pair production**: for photon energies greater than approximately twice the rest mass of electron, an electron-positron pair can be created, when the photon is close to the nucleus of target materials. For high energies pair production is the dominating process and has a the cross section proportional to $Z^2$.

The energy transferred to the material is modelled by the attenuation of the intensity of photon beams as an exponential function of the penetration depth of photons $x$ (also known as the Beer-Lambert law)

$$I(x) = I_0 \exp\left[-\mu x\right], \text{ with } \mu = n\sigma_\gamma = 1/\lambda. \tag{3.7}$$

$\mu$ is the absorption coefficient, which is defined as the product of the target density $n$ and the interaction cross section $\sigma_\gamma$. The reciprocal of $\mu$ is the absorption length $\lambda$, meaning that the intensity at $x = \lambda$ is attenuated to $1/e$ of the initial intensity $I_0$.

### 3.1.3 Total Ionising Dose

The Total Ionising Dose (TID) describes the total amount of energy deposited by a particle that results in ionising the target material. In semiconductors, this energy deposition leads to the production of e-h pairs. Gray (Gy) and rad are the common units of TID, with

$$1\,\mathrm{Gy} = 1\,\mathrm{J/kg} = 0.01\,\mathrm{rad}\,. \tag{3.8}$$

### 3.1.4 The Charge Cloud Evolution

Apart from the electric field, along which the charges drift to the electrodes, the repulsion between charges, and the diffusion play important roles in the evolution of charge clouds. The charge density distribution of a spherical electron cloud created in the detector bulk can be modelled by a Gaussian distribution in spherical coordinates it is given by

$$\rho(t) = \frac{Ne}{2\pi\sigma(t)^2}\exp\left[-\frac{r^2}{2\sigma(t)^2}\right], \tag{3.9}$$

with the number of electrons $N$, the radius $r$. $\sigma(t)$ represents the time-dependent standard deviation, which indicates that the diameter of the spherical charge cloud changes with time due to repulsion and diffusion. The temporal evolution $\sigma(t)$ can be converted to a position-dependent form by using the relation between drift time and drift length. It gives

$$\sigma(z)_{\mathrm{n/p-substrate}} = d\sqrt{\frac{k_B T}{eV_{\mathrm{dep}}}}\sqrt{\pm\ln\left(1 \pm \frac{2}{d}\frac{V_{\mathrm{dep}}}{V_{\mathrm{bias}} \mp V_{\mathrm{dep}}}\right)}, \tag{3.10}$$

representing the charge cloud width when it reaches the collection electrode, with $z$ the distance from the initial electron charge cloud centre to the collection electrode, $d$ the depletion width, $V_{\mathrm{bias}}$ the bias voltage, and $V_{\mathrm{dep}}$ the full depletion voltage [38].

### 3.1.5 Signal Formation: Shockley-Ramo Theorem

According to the theory by W. Shockley and S. Ramo [42, 43], moving charges in an electric field induce charges on the electrodes. The induced charge and current at the electrode $i$ are given as

$$\begin{aligned} \mathrm{d}Q_{s,i} &= -q\mathbf{E}_w \cdot \mathrm{d}\mathbf{r}\,, \\ i_{s,i} &= q\mathbf{E}_w \cdot \mathbf{v}_D\,, \end{aligned} \tag{3.11}$$

for a particle with a charge $q$, an instantaneous drift velocity $\mathbf{v}_D$, and a minimal displacement $\mathrm{d}\mathbf{r}$. $\mathbf{E}_w$ is the ***weighting field***, which is the gradient of the weighting potential $\Phi_w$ ($\mathbf{E}_w = \nabla\Phi_w$). The weighting potential depends only on the geometry of the electrode arrangement [44].

The development of induced signals can be illustrated using a generic silicon sensor structure: a PIN diode [3] (Figure 3.3 (a)). It comprises a thin layer of heavily doped n-type ($n^+$) silicon, a thick layer

[3] The "P", "I", and "N" represent p-type, intrinsic, and n-type, respectively. In practice, the intrinsic region is a lightly doped n- or p-type semiconductor.

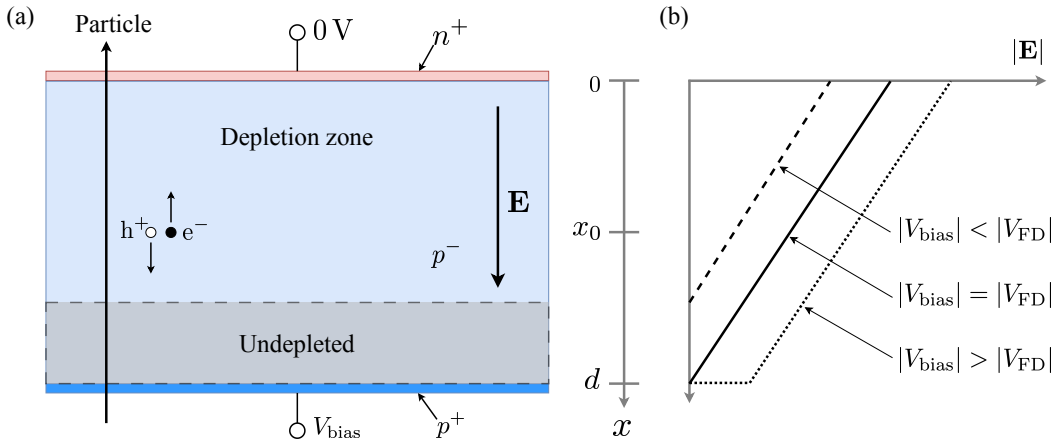



Figure 3.3: (a): creation of charge carriers in a reverse-biased silicon pad detector; (b): the electric field at different bias voltages. Figure based on [12].

of lightly doped p-type ($p^-$) silicon, and a thin layer of heavily doped p-type ($p^+$) silicon. Applying a reverse bias voltage (e.g., negative voltage at $p^+$, and ground $n^+$) to the diode results in the depletion of the $p^-$ region, and a linear electric field therein (Figure 3.3 (b)). When the entire sensing volume is fully depleted ($|V_{bias}| \geq |V_{FD}|$), the weighting field of such a geometry is given as $\mathbf{E}_w = -\mathbf{e}_x/d$, since it is independent of the stationary space charge. In a linear electric field, the drift velocity of an e-h pair created at position $x_0$ is an exponential function of time, i.e.

$$v_D^{e,h}(t) \propto 1/\tau_{e,h} \exp\left(\mp \frac{t}{\tau_{e,h}}\right). \tag{3.12}$$

$\tau_{e,h} = d^2/(2\mu_{e,h}V_{FD})$ is the characteristic time which depends on the mobility. Using Eq.(3.11), the time-dependent induced current at the $p^+$ electrode can be obtained as

$$i_s^{e,h} \propto 1/\tau_{e,h} \exp\left(\mp \frac{t}{\tau_{e,h}}\right). \tag{3.13}$$

When $|V_{bias}| < |V_{FD}|$, the motion of charges created in the undepleted region is dominated by diffusion (see Eq. (2.6). Due to the zero electric field, the velocity of charge carriers is much smaller [4] than that in the depletion zone.

The behaviour of the signal induced by a point-like charge cloud is illustrated in Figure 3.4 (a) and (b), where $i_s^e$ drops and $i_s^h$ rises exponentially (Eq. (3.13)). The arriving time for all electrons or holes are the same, and the signal stops, once they arrive the electrode or in an undepleted region. This is the reason for the sharp edges of the current and charge signals. Due to the fact that the electron drifts faster than holes in silicon, the signal in the first several nanoseconds is mainly contributed by electrons. If e-h pairs are homogeneously generated along a particle track, the signal is smoother, as shown in Figure 3.4 (c) and (d). Integrating the current signal over time results in the total charge

[4] Macroscopically, the diffusion of charges is slower than the drift process, however, the instantaneous thermal velocity of diffusing charge carriers is generally higher than the drift velocity.

collected by the electrode.

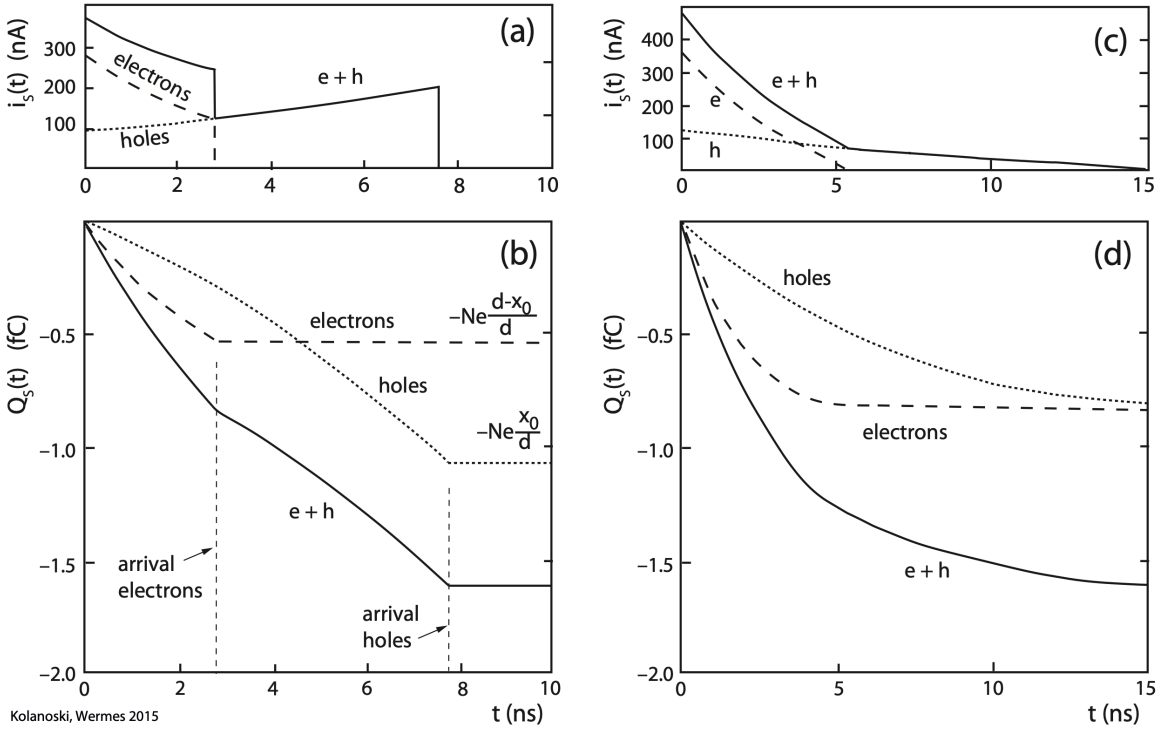



Figure 3.4: Signal development in a silicon pad detector. a) and b) illustrate the time-dependent signal of $N = 10^4$ e-h pairs created at $x_0 = (2/3)d$ with $V_{\text{bias}} = 150\,\text{V}$, $V_{\text{FD}} = 100\,\text{V}$ and $d = 300\,\mu\text{m}$. c) and d) are the signal development of e-h pairs equally distributed along the particle track at the same condition (Figure 3.3 (a)). [12]

## 3.2 Pixel Detectors

### 3.2.1 Sensor + Readout Electronics

The most essential advantage of a pixel detector is the ability to precisely determine the location where the impinging particle enters the detector. Such spatial information is achieved by dividing the electrode of a diode into pixels, and the depleted diode volume is effectively subdivided into pixel volumes, as depicted in Figure 3.5. The pixel size is defined not only as the size of electrodes, but also the region around it, so that the pixels equally share the sensor surface, and form a pixel matrix. The pixel size is determined by the "pitch", which is defined as the distance between the centres of two adjacent pixels. The charge cloud of electrons and holes created by the traversing particle moves to the corresponding electrodes following the electric field from the applied bias voltage. According to the Shockley-Ramo theorem, the charges induces current pulses at the electrodes, where the pixel volume with the highest amount of charge carriers has the strongest signal. The pixel electrode can be directly connected (DC coupled) to the readout electronics, or through a capacitor (AC coupled). The AC coupling has the advantage of filtering out the nearly constant leakage current from the depleted

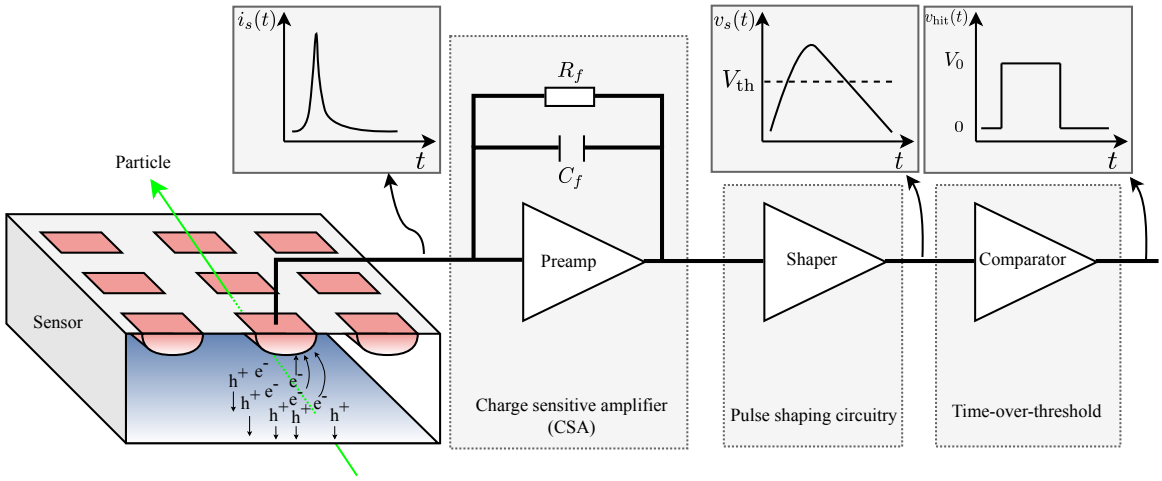



Figure 3.5: Schematic readout chain and the signal shapes at different stages. The charged particle produces a current pulse $i_s(t)$ at the input of the CSA. $i_s(t)$ is then integrated and shaped by the CSA and the pulse shaper, resulting in a triangular-shaped voltage signal $v_s(t)$ whose width is proportional to the collected charge. A threshold voltage is provided in the comparator to convert the $v_s(t)$ signal to logical states, where the part of $v_s(t)$ above $V_{\text{th}}$ is assigned to be logic 1 with the voltage $V_0$. The time over threshold (TOT) represents the amount of the collected charge by the time information, which can be obtained after a digitisation circuitry (not depicted).

sensor, but requires the implementation of a resistor (bias resistor) onto each pixel electrode to ensure a uniform potential across the pixel matrix.

A common method to read out the signal from the sensor is to use a charge sensitive amplifier (CSA, usually known as the pre-amplifier or preamp), which is an operational amplifier with a feedback loop consisting of a capacitor $C_f$ (integrates the current $i_s(t)$ to charge $Q_s$, resulting in a voltage signal $v_s(t)$) and a bleed resistor $R_f$ (discharges the capacitor). The bleed resistor can be substituted by a tuneable current source (e.g., in FE-I4 readout electronics for ATLAS pixel detectors [45]), which provides a constant slope of the charge and discharge process. The voltage signal after the preamp has a triangular shape, whose height is proportional to $Q_s$, since $v_s = Q_s \cdot C_f$ in ideal case. In the cases, where more than one signal (event) comes into the preamp within the discharging time, the output signal of each event after the preamp can overlap with each other (pile-up). Such an effect can be reduced by implementing a shaper (shaping amplifier) with high-pass and low-pass filters [12]. The frequency filtering contributes to the noise reduction, as well. In FE-I4, the shaping amplifier is realised with an amplifier with the same feedback loop as the preamp. The desired signal shape, a triangular signal with its width proportional to $Q_s$, can be achieved by tuning the feedback current. This signal is converted to a logic signal by using a comparator. By specifying a threshold voltage $V_{\text{det,thr}}$, the amplifier output signals $v_s(t)$ is compared with it. The resulting signal $v_{\text{hit}}(t)$ is a step function with

$$v_{\text{hit}}(t) = \begin{cases} V_0 & v_s(t) \geq V_{\text{det,thr}} \\ 0 & v_s(t) < V_{\text{det,thr}} \end{cases}, \tag{3.14}$$

where $V_0$ is a constant voltage. The duration of $v_{\text{hit}}(t) = V_0$ represents the charge created by the particle after the charge calibration [5]. Typically, the detector readout can provide a binary output, that a logical 1 will be delivered when a particle is detected by a pixel. This is also known as "binary readout".

On the one hand, a precisely acquired time information helps to precisely determine the charge, on the other hand, the determination of the rising edge of the signal provides the information of when the particle arrives the detector plane. Such time information becomes important in modern collider experiments, since the increasing rate of collision events requires a more precise method to separate one event from another.

### 3.2.2 Characteristics of Pixel Detectors

This section summarises a selection of the essential characteristics of pixel detectors. These factors play an important role in evaluating the performance of a pixel detector.

#### Spatial Resolution

Consider a scenario with the following conditions:

1. The pixel sensor has a pitch of $d_{\text{x}}$ and $d_{\text{y}}$ in two dimensions.
2. The signal is read out in a binary manner, where each pixel only indicates whether a particle has been detected.
3. A minimum ionising particle (MIP) strikes the pixel sensor with its track perpendicular to the sensor plane.
4. The charge cloud created by the MIP is much smaller in size compared to the pitch dimensions.

Figure 3.6 illustrates an example of hit reconstruction for such cases. A particle hits pixel 1, a signal is induced at the pixel, and the hit is reconstructed at the centre of a pixel. If the particle enters the sensor at the adjacent edge of pixels 1 and 2 (hit-B), the charge cloud created by the particle is shared by two pixels. As long as the charge collected by each pixel electrode is above the threshold of the discriminator, both pixels receive signals. Thus, the hit is reconstructed at the centre of the common edge. The difference between the actual hit position and the reconstructed position is the residual $\Delta x$ or $\Delta y$. In the x-direction, the probability that a particle hit is registered by a certain pixel is a uniform distribution with probability density $1/d_{\text{x}}$. Therefore, the uncertainty of the position reconstruction for pixel 1 along the x-direction is the standard deviation of the uniform distribution

$$\sigma_{\text{x}} = \sqrt{\int_{-d_{\text{x}}}^{0} \frac{(x + d_{\text{x}}/2)^2}{d_{\text{x}}} \mathrm{d}x} = \frac{d_{\text{x}}}{\sqrt{12}} \,. \tag{3.15}$$

This represents the maximum value of the spatial resolution bound by the pixel pitch. This relation is also valid for calculating the y-direction.

[5] Commonly, an injection circuit using known capacitors is implemented at the input of the preamp. By injecting the known amount of charge, the relation between charge and the duration of discriminator output can be determined. It is also common to use X-rays with known energies (e.g., from different targets) to obtain this relation.

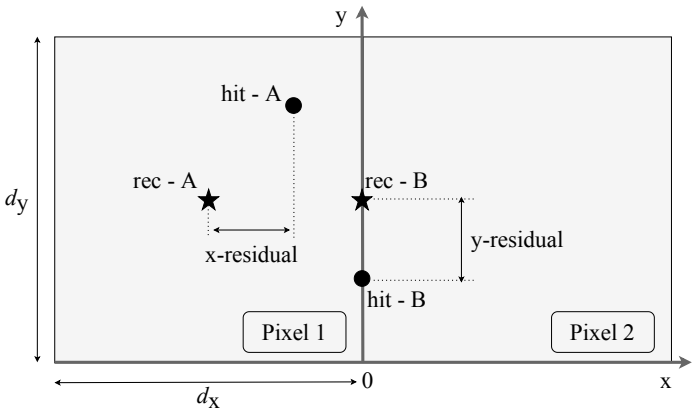



Figure 3.6: Example of hit-reconstruction for a pixel sensor with binary readout. Hit position A (hit-A) "●" represents a particle entering the Pixel 1, and this hit is reconstructed at the centre of the pixel (rec-A) "★". Hit position B (hit-B) is located on the adjacent edge of Pixel 1 and 2. The hit is reconstructed at the centre of the edge (rec-B).

Charge sharing between adjacent pixels takes place when the particle hits are close to their common edge, so that each pixel collects a part of the entire charge cloud. For instance, considering Figure 3.6, the charge sharing between both pixels is more pronounced when particles enter the sensor plane (the x-y plane) in the proximity of the y-axis. If a particle impinges at position $(\xi, \zeta)$, the charge cloud projection on the x-y plane can be modelled by a 2-dimensional Gaussian distribution [6]

$$\rho_{2D}(x, y) = \frac{Q_0}{2\pi\sigma_{2D}^2} \exp\left[-\frac{(x-\xi)^2 + (y-\zeta)^2}{2\sigma_{2D}^2}\right], \tag{3.16}$$

where $Q_0$ represents the total created charge, and the $\sigma_{2D}$ indicates the width. Figure 3.7 illustrates the amount of charge received by the pixel 1 with respect to the impinging location in x-direction $(\xi)$. More charge will be shared with the adjacent pixel if the impinging position is closer to the y-axis (i.e. $\xi = 0$), as a larger portion of the charge cloud enters the area of pixel 2. Therefore, a wider charge cloud also results in more significant charge sharing. Unlike the result from aforementioned discussions (Eq. 3.15), the impinging location of particles can be more precisely determined in the proximity of the pixel's edge, as long as the charge information is preserved.

In the 2-dimensional case, particles entering a single pixel can induce signals in nine pixels, which are the hit pixel and the eight surrounding pixels (i.e. a $3 \times 3$ matrix with the hit pixel in the centre). When the impinging position is close to the corners of a pixel, the charge sharing can take place among 3 or 4 pixels. Ideally, the charge information among the nine pixels can provide unique charge signatures of the particle hit position. However, due to the finite charge resolution in a realistic detector readout chain, particles entering a certain region of the pixel can deliver the same charge signature. Therefore, a physical pixel can be subdivided into "effective pixels" [46], as illustrated in Figure 3.8. Each effective pixel corresponds to a unique charge signature, so that hits with the same charge

[6] A more realistic approximation is detailed in Appendix A, but it is computationally more tedious, and the effect of charge sharing is already well illustrated using the simpler 2D Gaussian distribution.

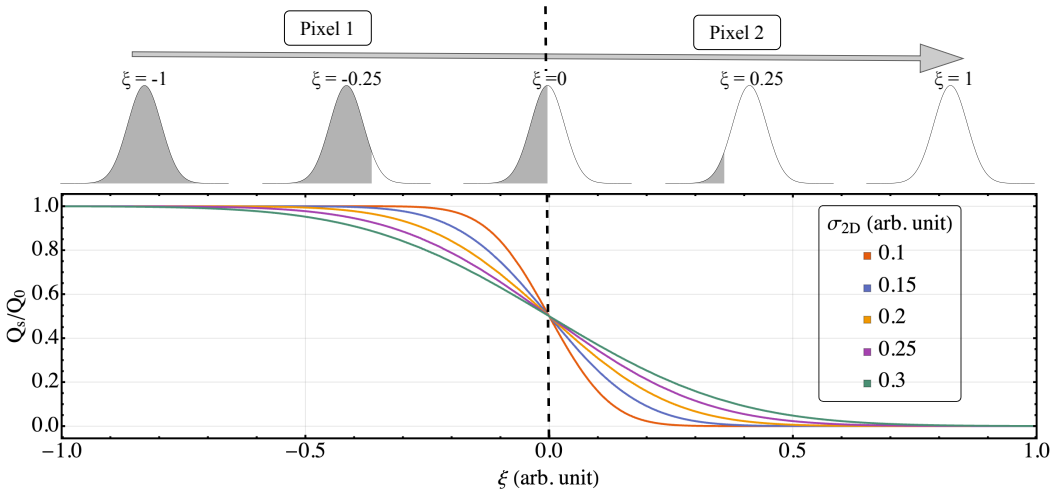



Figure 3.7: The diagram shows the position-dependent charge collection ($Q_s(\xi)$) of pixel 1 in Figure 3.6 for different widths of the charge cloud projection ($\sigma_{2D}$). The Gaussian distributions illustrate the distribution of charge density, where the shaded area represents the charge collected by pixel 1. $\xi = -1.0$ represents the case "hit-A" and $\xi = -0.0$ represents "hit-B". The effects of the electronics, e.g. related to the threshold, digitisation error, and the finite charge resolutions, are not considered here.

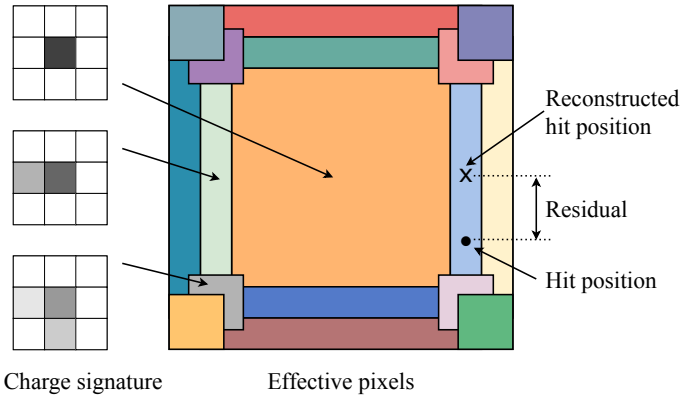



Figure 3.8: Schematic effective pixel layout of a pixel. Each coloured area represents a unique charge signature, which is schematically illustrated in the left part by the greyscale. The particle hit within an effective pixel is reconstructed at the centre of gravity of the effective pixel.

signature are reconstructed at the centre of gravity of the corresponding effective pixel. Given the preconditions listed at the beginning of this section, most particle hits lead to cluster size of one and are reconstructed at the centre of a pixel. More effective pixels, caused by more disjunct charge signatures, occur when the hit position is closer to the pixel boundaries. Practically, the charge signatures are also influenced by the threshold, digitisation errors, the total created charge, and the Landau distribution.

The overall RMS spatial resolution in one dimension can be obtained via

$$\sigma_{\mathrm{RMS},x} = \sqrt{\frac{1}{N}\sum_{i}^{N}(x_i - x_{i,\mathrm{rec}})^2}\,, \tag{3.17}$$

for $N$ random particle impingings, with the $i$-th particle reconstructed at $x = x_{i,\mathrm{rec}}$. Given $M$ effective pixels, and $n_j$ particles are found in the $j$-th effective pixel, there is $N = \sum_j^M n_j$. Equation 3.17 can then be reformulated as

$$\sigma_{\mathrm{RMS},x} = \sqrt{\sum_{j}^{M} \nu_j \sigma_{j,x}^2}\,, \tag{3.18}$$

with $\nu_j = n_j/N$ and $\sigma_{j,x}^2 = (\sum_k^{n_j}(x_k - x_{k,\mathrm{rec}})^2)/n_j$. It is easy to see that $\sigma_{j,x}$ represents the RMS resolution of the $j$-th effective pixel. When $N$ is sufficiently large, the factor $\nu_j$ approaches the ratio $A_j/A$, where $A_j$ is the area of the $j$-th effective pixel and $A$ the total area of the physical pixel. Such a reconstruction method is also applicable for binary readout, however, there will be much less unique charge signatures due to the missing charge information. When the charge cloud size is very small compared to the pixel size, the resulting resolution approaches the previously calculated value (Eq. 3.15).

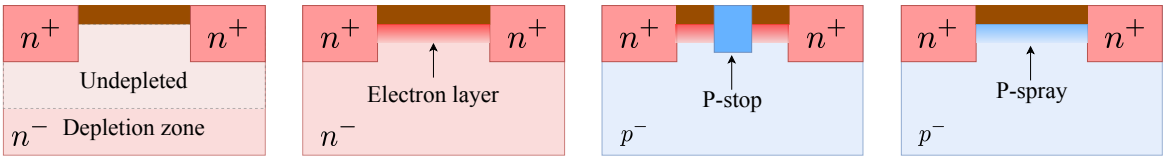
#### Inter-pixel Resistance

The calculation of the pixel resolution above assumes that all pixels (electrode implants) are perfectly electrically isolated during operation. Poor isolation, however, results in electrical charge sharing among the electrodes, causing a particle to trigger signals in more pixels than would be the case with sensors that have perfect isolation. If pixels 1 and 2 in Figure 3.6 are poorly isolated, hit-A will also cause a signal in pixel 2. Consequently, the spatial resolution in the x-direction is effectively doubled. Such unintended electrical coupling between pixels is referred to as *cross-talk*. In practice, cross-talk can arise from capacitive or resistive coupling between pixels and may originate from the electronics (electrical coupling between electronic components of pixels) or the sensor itself (insufficient isolation between pixel implants).

The inter-pixel resistance in a real sensor is influenced by the material properties and the design. In n-on-n sensors [7], the n-type electrodes are resistively coupled via the un-depleted n-type bulk when the bias voltage is below the full depletion voltage (see Figure 3.9 (a)). After full depletion, crystal defects at the $Si/SiO_2$ interface between pixel implants can also facilitate electron accumulation, which further connects the electrodes (for details, see section 3.4) as shown in Figure 3.9 (b). Conversely, in state-of-the-art n-on-p sensors, p-n junctions surrounding the electrodes provide natural isolation between pixels. However, electron accumulation can still create low-resistive connections between

[7] A sensor configuration that uses a low-doping n-type wafer as the sensor bulk, n-type electrodes for signal collection, and a p-type backside implantation to create depletion. Hence, n (n-type electrodes) on-n (n-type bulk).

pixels. These effects can be mitigated by introducing p-type implants between pixels, such as p-stop or p-spray techniques, as illustrated in Figure 3.9 (c) and (d) [47]. In n-on-n sensors, the p-type implants




(a) (b) (c) (d)

Figure 3.9: Illustrations of the inter-pixel structure. (a) n-on-n sensor with no inter-pixel isolation structure. With a bias voltage lower than the full depletion voltage, the electrodes are short circuited by the undepleted bulk. (b) The n-on-n sensor after full depletion, but an electron layer appears at the Si-$SiO_2$ interface, which short circuited the electrodes. (c) n-on-p sensor with a p-stop implant between the electrodes, which interrupts the electron accumulation layer. (d) n-on-p sensor with a thin layer or p-type implant in the inter-pixel region (p-spray), which isolates the pixel electrodes.

introduce p-n junctions in the inter-pixel regions, which enhances the depletion. Moreover, the high concentration of holes interrupts the electron accumulation layer at the surface, and increases the resistance.

#### Breakdown Voltage

Determining the bias voltage of a silicon pixel sensor requires the consideration of the resistivity of sensor bulk and the breakdown performance. Ideally, the bias voltage should be sufficiently high to achieve a full depletion, and a high electric field to provide a short drift time of charge carriers. The breakdown voltage limits the applied bias voltage, since the high current after the onset of the breakdown can strongly disturb the signal readout, or cause irreversible damage to the sensor structure due to heat emission.

The avalanche breakdown is the most interesting breakdown mechanism for pixel sensors, as the doping concentration of the sensor bulk is typically much smaller than the electrode implants. In pixel detectors using the planar technology [8], high electric fields often are located at the corners and the edges of an implant [6] (e.g. the pixel electrodes in Figure 3.5).

An appropriate breakdown voltage is crucial for detector operation. This can be achieved by optimising the potential and electric field at the implants, via modifying the geometry of implants, such as implementing guard ring structures.

#### Charge Collection Efficiency (CCE)

The CCE of a particle detector is used to evaluate particle detectors regarding their ability to collect the charge carriers produced by the traversing particle. An ideal detector has a CCE of 100%, meaning that all created charge carriers are collected by the readout electronics. However, in reality the CCE is influenced by the design and degradation of sensors.

Detectors using AC coupling between sensor and readout electronics lead to a systematically

[8] The devices are fabricated on the surface of a silicon wafer.

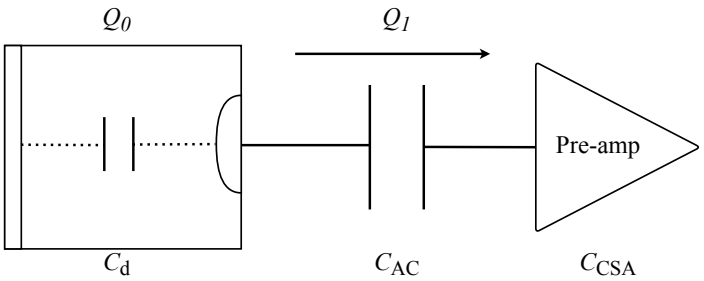



Figure 3.10: The capacitive equivalent circuit of a generic AC-coupled pixel consists of a detector (pixel) capacitance $C_d$, a coupling capacitance $C_{AC}$, and the effective capacitance of a pre-amp (CSA) $C_{CSA}$. When charge $Q_0$ is created in the sensor, $Q_1$ is actually collected by the pre-amp.

lowered CCE, which is determined by the ratio of the detector (pixel) capacitance [9] $C_d$, the coupling capacitance $C_{AC}$, and the effective capacitance of the pre-amp (CSA) $C_{CSA}$(Figure 3.10). The relation between the collected charge $Q_1$ and the created charge $Q_0$ is given by the $CCE_{sys}$, as

$$Q_1 = Q_0 \times CCE_{sys} = Q_0 \frac{C_{CSA+AC}}{C_{CSA+AC} + C_d} . \tag{3.19}$$

$C_{CSA+AC}$ represents the total capacitance of the serial connected coupling capacitor and the effective capacitance of the CSA. Equation 3.19 indicates that the $CCE_{sys}$ approaches 100% when the $C_{CSA+AC}$ is much larger than $C_d$. Typically, $C_d$ is in the order of fF, which is influenced by the pixel size [48]. $C_{CSA}$ depends on the feedback capacitance and the open-loop gain of the amplifier, therefore, it is typically in the order of pF. From this, $C_{CSA+AC}$ mainly depends on $C_{AC}$. Thus, the coupling capacitance is in the order of 100 fF or even pF to ensure a sufficiently high charge collection efficiency. The high $CCE_{sys}$ in a DC-coupled pixel is merely determined by the CSA and the pixel capacitance.

Another source of the lowered CCE is the trapping of charge carriers in sensors. The trapping effect usually means that the charge carriers are trapped by defect energy levels (traps) in the band gap, so that they will no longer contribute to the signal before they are released from the traps (de-trapping). Such effects are more pronounced after the sensor has received severe radiation damages (see chapter C). It is also possible that there is a potential extremum other than the collection electrode in the sensor, so that a portion of the charge carriers can be gathered at the potential extremum without drifting to electrodes.

The overall CCE is given by

$$CCE = CCE_{sys} \times CCE_{trap} , \tag{3.20}$$

which includes the systematic charge collection efficiency $CCE_{sys}$ and the efficiency from the trapping effect $CCE_{trap}$.

### Noise

There are various noise sources in the operation of silicon detectors, such as the statistical fluctuation of signal charges, the electronic noise in the signal processing, and quantisation noise in the digitisation

[9] This is contributed by the capacitance between the pixel implant and the backside plane of the sensor, and the capacitance between frontside implants (e.g., between pixel implants, pixel implants and p-stop).

process. Being a crucial contribution of noise in silicon detectors, the electronic noise originates from the voltage and current fluctuations in the electronic components of the readout electronics [12]. Three main types of the noise are:

- thermal noise (also known as Johnson noise, Nyquist noise, or white noise), caused by the fluctuation of the charge carrier velocity. The thermal noise is proportional to the temperature but independent of the frequency.
- shot noise denotes the fluctuation of the number of charge carriers when they overcome potential barriers, e.g., the emission of electron-hole pairs which needs to overcome the band gap. The shot noise is proportional to the expectation value of the current, and independent of frequency. A typical source of shot noise to the readout electronics is the leakage current of the silicon sensor.
- 1/f noise (also known as pink noise, flicker noise) is a frequency-dependent noise ($\propto 1/f^{\alpha}$), whose mechanism is still not completely understood. Such a noise pattern is not only found in electronic systems, but is also seen in the velocity of ocean currents, the frequency of the Earth rotation, the traffic flow, etc. In MOSFET structure of electronic systems, the 1/f noise is identified as the consequence of random trapping and releasing process of charge carriers with different time constants [12].

The noise of a readout chain is usually evaluated by the so-called ***Equivalent Noise Charge (ENC)***, which is defined as

$$\mathrm{ENC} = \frac{\text{noise output voltage (V)}}{\text{output voltage of a signal induced by 1 electron (V/e}^{-})} \,. \tag{3.21}$$

The ENC shows the noise level of a detector in the unit of the number of electrons, so that it is very intuitive and useful for characterising the detector performance. The noise of a generic readout chain using the pre-amp depends on the profiles of the electronic components (e.g., the geometry of the MOSFET, the transconductance, the feedback capacitance) and the capacitance directly coupled to the input of the amplifier. For a DC-coupled pixel, this capacitance is merely $C_{\mathrm{d}}$. For AC coupling, the coupling capacitor needs to be taken into account. Nevertheless, the coupling capacitance is typically much larger than $C_{\mathrm{d}}$, thus the pixel capacitance is still the most crucial factor. The ENC of such a system has contributions from all three types of noise, and is proportional to $C_{\mathrm{d}}$. This means that a large pixel capacitance results in higher noise.

### 3.2.3 Hybrid and Monolithic Detectors

***Hybrid pixel detectors*** are commonly used in high energy physics research. Its main part consists of a passive sensor chip with pixelated electrodes and a readout electronics chip (Figure 3.11). The readout electronics introduced in section 3.2.1 is arranged in a matrix and fabricated on silicon chip, so that each pixel in the sensor has an individual set of readout electronics. Bump bonding is a usual way to connect both chips, where each pixel of the sensor is electrically connected to the corresponding readout chain via a metal bump. Hybrid detectors allow for individual development paths of sensor and readout chips. A readout chip can be designed and tested without relating to any sensor, but it can be used with different sensors, as long as the pixelated geometry and features of the electronics match

the attached sensor. This feature of hybrid detectors offers a large flexibility in both the design and the field of application. Nevertheless, the assembly of hybrid detectors using bump bonding requires the flip-chip technique [47], which is usually labor-intensive, relatively low-yield and costly, since the sensor and readout chip need to be perfectly aligned and bonded. Moreover, the material budget from the thickness of hybrid detectors is difficult to be reduced, since a few 100 µm of thickness is usually required for handling the wafer.

***Monolithic pixel detectors*** are an attractive alternative to hybrid detectors for high precision tracking in high energy physics. Based on commercial CMOS [10] technology, the sensor and the readout electronics are integrated into a single silicon substrate. This reduces the material budget, gives access to large production volumes and provides comparable signal processing speed which is achieved by fully integrating the electronics in pixels. ***Monolithic Active Pixel Sensors*** (MAPS) have been successfully implemented in experiments with low radiation environments, such as ALICE ITS [11] [49]. However, their radiation tolerance is limited by the charge collection method which is through diffusion of charge carriers. ***Depleted Monolithic Active Pixel Sensors*** (DMAPS) were developed by using a high-resistivity (low doping) sensing volume, e.g., high-resistivity wafer or through epitaxial growth[12], to establish a substantial depletion and high electric field.

Figure 3.12 illustrates two typical designs of monolithic pixel detectors, namely the large (Figure 3.12 (a)) and small electrode[13] design (Figure 3.12 (b)). The readout chain is embedded inside the wells on the front side of the detector. In the large electrode case, the collection electrode is formed using very deep highly doped n-type silicon. Such a deep n-well can shield the electronic components

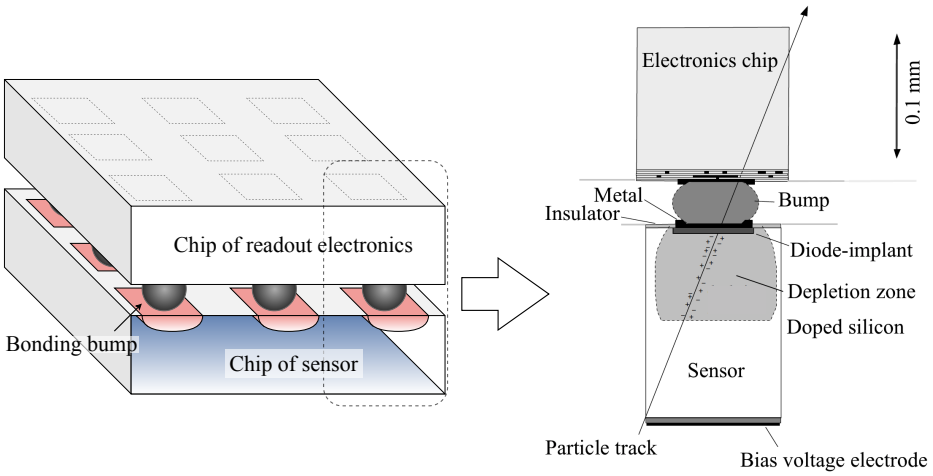


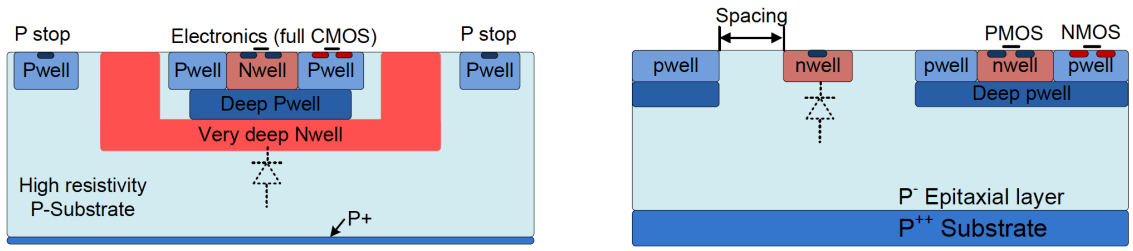

Figure 3.11: The sensor and readout are both designed in the manner of pixelated structures and are bonded via metal bumps, so that the signal received by one pixel in the sensor can be directly lead into the corresponding readout chain. The sketch on the right illustrates the cross section of one pixel during operation. (Figure based on [47])

[10] Complementary Metal-Oxide-Semiconductor: a technology to construct integrated circuits.

[11] ALICE: A Large Ion Collider Experiment, at the LHC; ITS: Inner Tracking System

[12] An IC processing technique for growing crystal (see [4]).

[13] It is also common to categorise these designs using the "large or small fill factor", where the fill factor is defined as the ratio of the pixel electrode size and the pixel size.




(a) (b)

Figure 3.12: Schematic cross-section of the pixel cell implantation with large electrode (a) and small electrode (b). [48]

(CMOS electronics) therein from the possibly high electric field in the substrate. On the contrary, the electronics in the small electrode design needs to be embedded in the region between collection electrodes, since the collection electrode cannot provide sufficient space. The electronics is shielded with deep p-type implants, so that a large p-well exists between electrodes.

## 3.3 Pixel Sensors Using Commercial CMOS Technology: Passive-CMOS

CMOS is the abbreviation of Complementary Metal-Oxide-Semiconductor, which is a widely used MOSFET fabrication process for commercial microelectronics. CMOS processes form complementary (and symmetrical) pairs of n-MOSFET and p-MOSFET on the same silicon substrate, featuring a low DC power consumption. The application of CMOS technology covers integrated circuits (IC), such as microprocessors, memory chips, and image sensors.

Using the commercial CMOS technology production line to fabricate particle detectors has been realised for monolithic detectors [49]. The mature production technology with well developed manufacturing techniques, the reliability of finial products, and the large throughput offers a great advantage for producing particle detectors with high yield and cost-efficiency. With the development of particle accelerator facilities targeting higher energies and higher luminosities, the demand of silicon detectors has become more significant. The upcoming upgrade of the inner tracking detectors of the ATLAS experiment has featured a silicon detector coverage of approximately 180 $m^2$ (14 $m^2$ is pixel detector, and the rest is strip detector), whereas the currently implemented silicon detector covers approximately 63 $m^2$ (pixel detector less than 2 $m^2$) [50–53]. Approximately 430 $m^2$ of silicon detectors has been planned for the Future Circular Collider (FCC) [54]. Since the size of a single piece of silicon sensor chip is in the order of several $cm^2$, a vast amount of detector modules need to be fabricated. In this situation, hybrid silicon detectors are facing the challenges of production yield and cost. DMAPS with integrated electronics are without doubt a promising alternative, however, their performance after severe radiation damage is still under extensive studies. Currently, the cost of producing hybrid detectors is mainly driven by the sensor production and the bump bonding process. The budget can be reduced by a factor of $3-4$, if the sensors are produced using commercial CMOS technologies, in comparison with the standard hybrid sensors [37]. Such sensors are termed ***passive-CMOS***.

The passive CMOS sensors are produced using CMOS technologies without implementing any

active electronics component (therefore the term “passive” is used). They were developed based on passive test structures for investigating sensor designs, including the charge collection efficiency and the breakdown performance. Being planar sensors, the electrode implants are formed on the surface of silicon wafers, using the implantation profiles of n- and p-wells for fabricating the p- and n-MOSFETs. In addition, commercial CMOS technologies provide access to special features not available elsewhere, such as

- multiple metal layers: enables more flexible designs, such as to form complex wiring geometries;
- metal-insulator-metal (MIM) capacitors: allows to form AC coupling capacitors;
- polysilicon layer: high-resistivity polysilicon resistors are used to form bias grids, and the low-resistivity polysilicon structures can be used to form overhang structures at the edge of implant, to modulate the electric field.
- stitching techniques: to produce sensors with a large size [37].

Commercial CMOS technologies also offer design tool kits for each specific process, which supports the design process. The passive sensors are typically less sensitive to the feature size of the technology, with respect to the electronics. Therefore, porting a design from one technology to another is less difficult.

### 3.3.1 Manufacturing a Passive CMOS Sensor

The generic workflow of manufacturing passive CMOS sensors is similar to typical planer technologies, including photolithography, etching, ion-implantation, thermal processes, etc (Figure 3.13). The sensor structure is made layer by layer with different patterns through masks, which are designed for the following wafer processes to form the final sensor.

- **Photolithography**:
  This process transfers the pattern of masks onto a silicon wafer. A layer of photoresist, which is

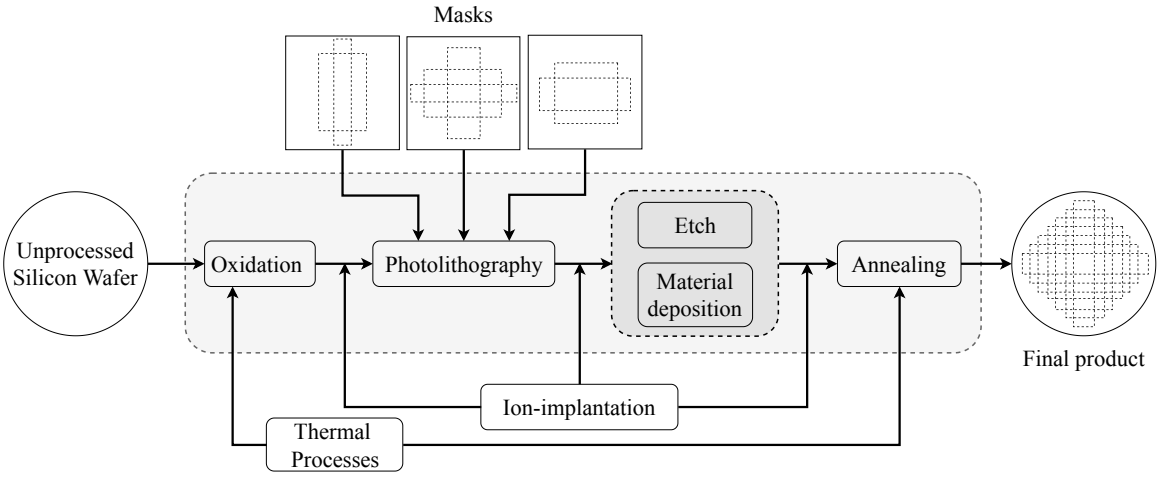



Figure 3.13: Flow chart of generic processing sequences.

photosensitive, is first spread on the wafer. After exposure to UV light [14] through a mask, the photoresist coating can be selectively removed according to the pattern. With this method, the wafer can be further processed with a desired pattern.

- **Etching**:
  Using chemical solutions (wet etching) or plasma (dry etching), silicon or other materials, such as oxides, nitrides and metals, can be removed from the wafer through chemical reactions. In combination with masks and photolithography, a selective etching process of certain areas can be achieved.

- **Material deposition**:
  Materials can be added on the wafer, for instance adding silicon by epitaxial deposition, or depositing metals. Epitaxial growth is a way to grow a layer of single-crystal silicon. In IC fabrication, Chemical Vapour Deposition (CVD) and Physical Vapour Deposition (PVD) are the common methods.

- **Ion-implantation**:
  The dopants are commonly introduced by ion-implantation in modern IC processes. The implantation process injects dopants into wafers through energetic ion beams. A certain profile of depth and doping concentration can be achieved by controlling the beam energy and dose. The ***channeling effect*** [15] can be suppressed by adding a thin oxide layer (screen oxide), and/or by injecting the beam with a tilt angle with respect to the normal of the wafer surface. Typically, the tilt angle is set to 7 degrees in IC fabrications [4].

- **Thermal process**:
  Silicon wafers undergo high-temperature (700 - 1200 $^{\circ}$C) processes multiple times during IC fabrication. Combining high temperature with different gas flows, the thermal processes is used for oxide layer growth, epitaxial silicon deposition, annealing process after ion-implantation, etc. Annealing process can increase lattice vibrations and increase the thermal energy of impurity atoms/ions. The post-implantation annealing process supports the re-formation of the damaged lattice structure and rearranges the dopants onto the lattice sites (Figure 3.14). This process is also referred to as activation of dopants.

These processes are often implemented multiple times in design sequences to achieve the desired device structure with appropriate electrical and mechanical properties. A more thorough and comprehensive introduction can be found in various books [4, 55].

#### Thinning and Backside Processing

Silicon wafers are usually sliced from the ingot targeting the smallest possible thickness. Nevertheless, the minimal thickness of a standard wafer depends on the size (diameter) of the wafer (or ingot),

[14] The choice of light source depending on the scale of patterns on masks, since interference can appear when the wavelength mismatches the size of the transparent parts on the masks.

[15] Since single-crystal silicon has orderly arranged atoms, many channels (straight paths between lattice atoms) can be seen from different angles. The injected ions penetrating through channels can have an unexpectedly large projection range in uncontrollable directions. (see e.g. [4])

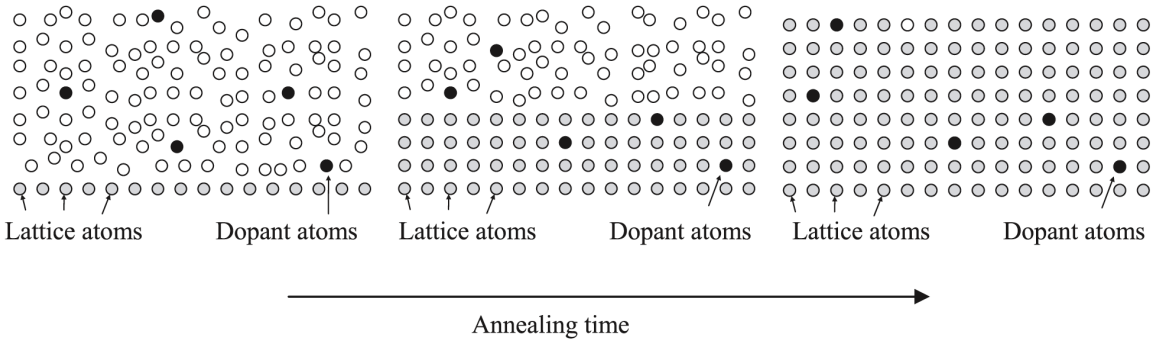



Figure 3.14: Annealing process after ion implantation.[4]

namely a larger wafer requires a larger thickness to sustain the mechanical handling in the processing [4]. "8 inch" wafers (diameter = 200 mm) are typically used in manufacturing passive CMOS sensors or DMAPS, and have a thickness of 725 µm. To achieve a lower material budget, sensors are usually thinned down to 100 µm – 150 µm after the sensor structure is fabricated on a wafer, by flipping the wafer and grinding the backside. The TAIKO [16] thinning process ensures that the thin wafer can be handled more easily. The thinned backside wafer undergoes polishing through e.g. wet or dry etching and chemical mechanical polishing (CMP) [17], which smoothens and planarizes the wafer surface. A backside implantation of a high-doping p-type layer is important for reducing the effects of crystal defects and applying bias voltage. The polished wafer surface can still contain crystal damages, which come from the sawing and grinding processes. Such defects can cause a non-negligible increase of leakage current after full depletion. The high-doping p-layer with a high hole concentration increases the recombination of electrons from the leakage current, and forms an ohmic contact with the metal layer after metallisation.

#### The LFoundry 150 nm Technology

The LFoundry [57] 150 nm technology is popular in HEP for developing CMOS detector prototypes, such as the CCPD-LF, the LF-CPIX [58], the LF-Monopix [59], and the RD50-MPW [60] for monolithic detectors, and the passive CMOS sensors [37, 61] developed for the hybrid detectors for ATLAS ITK. Figure 3.15 illustrates an example of the available features of the LFoundry 150 nm process (in a section view). This CMOS technology offers 4 to 6 aluminium layers with a minimum gate length of 150 nm, based on 8 inch substrate wafers. The p-type substrate resistivity can be chosen from several hundreds $\Omega \cdot$ cm to very high values with $\rho > 2\,\mathrm{k}\Omega \cdot$ cm. Besides the standard n-well (NW) and p-well (PW) for MOSFET structures, the LFoundry 150 nm technology offers implants with a larger depth: the standard deep n-well (NISO), very deep n-layer (DNW) using extra high energy implants, and the deep p-well (PSUB). The NISO and DNW have been employed to form isolation for the electronics in DMAPS as shown in 3.12(a). The electrodes are realised by forming the connection between high-doping silicon materials at the surface of the silicon wafer and the first metal layer M1, through the metal contact. Such high-doping regions indicate the electrically active

[16] A backside processing technique which leaves the rim of a wafer and grind only the inner region.[56]

[17] The CMP combines the chemical reactions and mechanical polishing to remove a layer of material on the surface of a wafer.[4]

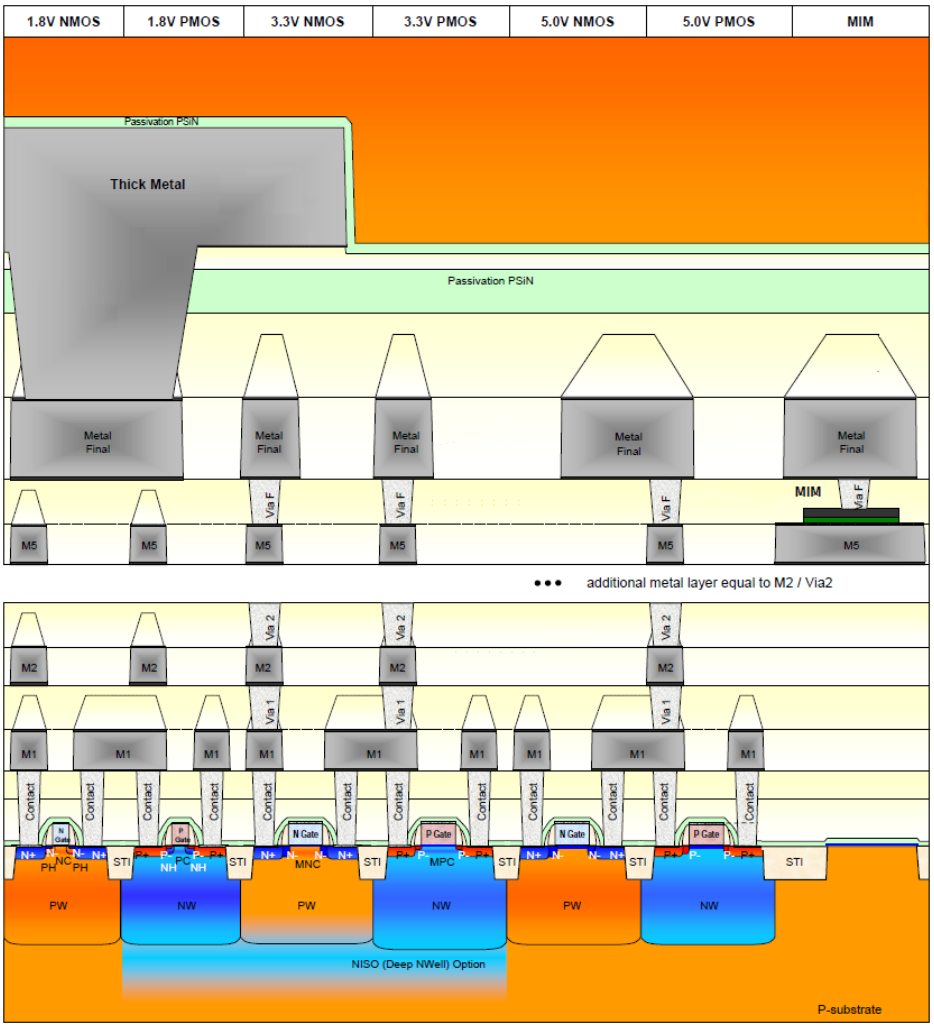



Figure 3.15: Schematic cross section of LFoundry 150 nm process. [62]

regions of a device or structure, and the active regions are separated by the widely spread Shallow Trench Isolation (STI) to prevent electric current leakage between adjacent structures. STI has a typical thickness of 400 nm and is commonly formed by $SiO_2$ before ion implantations. The multiple layers of metal offers the possibility to design more complex circuits and provides the implementation of MIM capacitors. Electrodes of active components on silicon wafers can be accessed from the top of the wafer by building a connection from the silicon surface and the top layer of the metal. The bump-bonding pads (the metal pads on the surface of chips for bump-bonding, see figure 3.11), or wire-bonding pads are implemented based on creating an opening in the passivation layer.

### 3.3.2 The Structure of Passive-CMOS using LFoundry 150 nm Technology

A passive CMOS sensor consists of a pixel matrix and a number of guard rings surrounding the matrix (Figure 3.16). The figure shows the layout of a test structure with a smaller matrix size, in comparison with the sensor for actual applications. Nevertheless, the pixel geometry, implantation profiles are the

same as in a full size sensor. The details of the layout design can be identified in Figure 3.17, showing the upper right corner of the sensor chip illustrated in Figure 3.16. Although various designs of the pixels and guard rings can be applied to passive-CMOS sensors, the "seal ring" is a universal structure of all the pixel sensors fabricated using CMOS processes. In CMOS ICs, the seal ring has a structure that protects the enclosed circuits and ensures product reliability. It is also present in passive-CMOS sensors, and usually indicates the dicing edge of a sensor chip.

### Pixel and Pixel Matrix

Arranging the pixels in a matrix form is the most straightforward way, since they are commonly designed to have a rectangular or square shape. The size of a pixel is referred as the pitch, which is illustrated in figure 3.18. In a typical n-on-p pixel sensor, the pixel matrix region consists of 1) n-type electrodes, which are located at the centre of pixels and 2) the p-type implant surrounding the electrodes. Standard n-wells (NW) are typically used to form the pixel electrodes of passive CMOS sensors for collecting electrons in a p-type substrate. Moreover, the deep n-well implants (NISO and DNW) offer the possibility to extend the depth of the charge collection nodes in passive sensors. The p-stops between n-type collection electrodes serve as an inter-pixel isolation structure, and are formed by the standard p-wells (PW) implant in the LFoundry 150 nm technology.

### Guard Rings

The guard rings in pixel sensors refer to the ring-shaped implants which surround the pixel matrix. From the inner side (pixel matrix side) to the edge (seal ring) of a pixel sensor, 8 ring structures

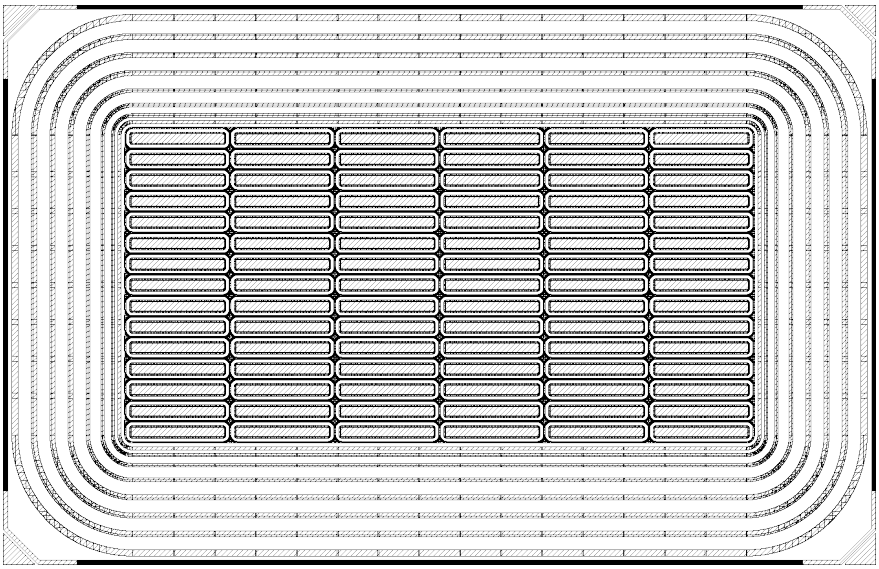


Figure 3.16: Generic layout of a passive CMOS sensor, where the implants are illustrated by the shaded areas. This is a layout of a passive CMOS test structure with elongated pixels (250 µm × 50 µm) forming a pixel matrix (15 × 6 pixels in the central area). Six guard rings are located in the periphery of the chip surrounding the pixel matrix. A full size passive-CMOS sensor consists of a much larger pixel matrix, for instance, up to 400 × 384 pixels with the total chip size of approximately $4 \times 4\,\mathrm{cm}^2$.

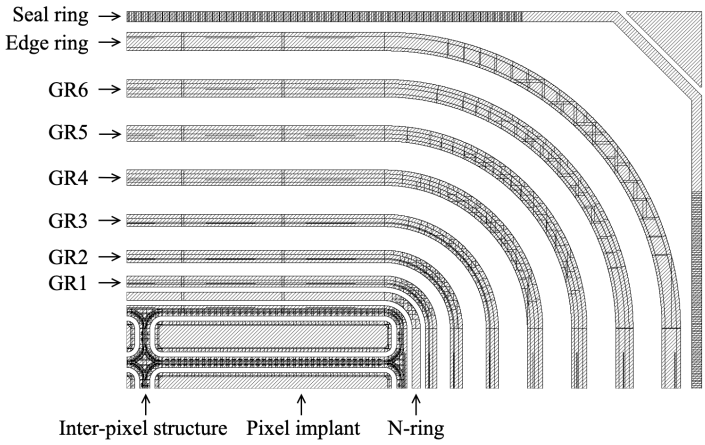



Figure 3.17: The top-right corner of figure 3.16 showing a more detailed layout of the implants in the pixel matrix and the guard ring region.

are placed in the given example (Figure 3.16 and 3.17): the “n-ring” (n-type implant), 6 floating guard rings “GR1” to "GR6" (p-type implant or combined p- and n-type implants), and the “edge ring”. During operation of the sensor, the potential difference between the pixel collection electrode (typically 0 V or a low voltage) and the seal ring is the bias voltage (typically a negative high voltage)[18]. Thus, a potential drop appears across the guard ring region, starting from the n-ring to the edge ring.

The n-ring is designed to be fabricated by using the same doping profile as for the collection electrode of the pixels, and to have the same constant electrostatic potential as the pixel electrodes

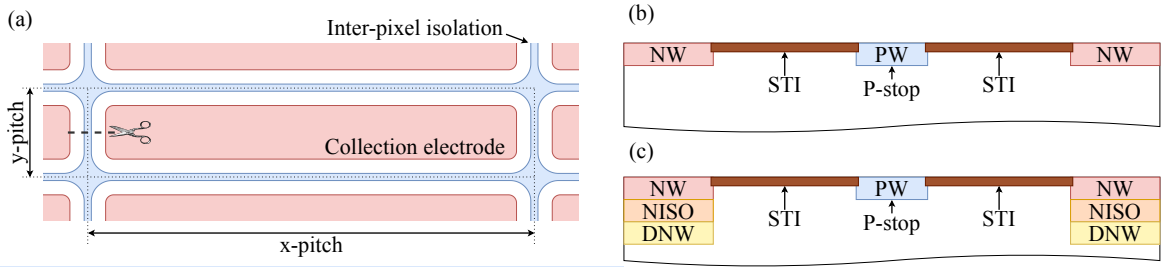



Figure 3.18: Generic layout of a single pixel and the cross section view of the inter-pixel region. (a): The top view of one pixel from the pixel matrix, showing the geometry of the n- and p-type implant. A pixel is defined as the area enclosed by the dotted line, where the collection electrode is located in the central region, surrounding by the inter-pixel isolation structure (p-stop as an example). The size of a pixel is typically characterised by the two pitch sizes, e.g. x and y-pitch. (b) and (c): the schematic section view represents the region indicated by the cut line in (a). Here, the implantation profile of the standard p-well (PW) is used for p-stop. The collection electrode can be made of the standard n-well (NW) in (b), or the deep n-well (combined NW, NISO, and DNW) in (c). The shallow trench isolation (STI) covers the area between p- and n-type implants.

[18] A high concentration of crystal damages is introduced when the chip is diced from a wafer, by using diamond saw. Consequently, the cutting edge of such a sensor chip is conductive, and the (p-type) implant of the seal ring is electrically connected with the backside implant/metal of an n-on-p sensor. Therefore, the bias voltage for operating pixel sensors can be applied between the seal ring and the collection electrode of pixels, as well.

during operation. This is used to shape the electric field under the pixels at the matrix edge (edge pixels), so that they will have the same electric field as the inner pixels and respond to the impinging particles in the same manner. Another functionality of the n-ring is to collect the leakage current from the region outside the pixel matrix, and prevent it from flowing into the edge pixels.

The edge ring is fabricated with the p-type implant, and electrically short-circuited with the seal ring. The geometry of the edge ring is designed to have a uniform distance to the outermost floating guard ring, to provide the similar electric field everywhere between these two rings.

Ideally, the potential drops smoothly both in the bulk and at the surface of the silicon ($Si/SiO_2$ interface) without floating guard rings (figure 3.19 (a)). Nevertheless, the impurities or defects at the $Si/SiO_2$ interface are hard to be avoided in real manufacturing processes, and these can cause a high surface leakage current. The application of floating guard rings for increasing breakdown voltages has been introduced in the late 1960s and has been studied over decades for high-voltage semiconductor power devices [63]. This concept has been implemented in silicon sensors for HEP and studied from the earlier n-substrate sensor and the current n-in-p sensors [47, 64, 65].

The basic design of the floating guard rings uses the p-well implant, which has the same profile as the p-stop. These rings breaks the electron accumulation layer under the STI and reduces the leakage current. Furthermore, the defects at the $SiO_2/Si$ interface may also cause unwanted electric field maximum, which can trigger the impact ionisation, and hence, early breakdowns. The floating guard rings will be at certain potentials during the depletion of the chip periphery, therefore, the potential at the silicon surface near the floating rings can be pinned to a fixed and more predictable value.

Guard ring designs, including the geometrical arrangements, the implants, and the overhang (see section 5.1), can significantly influence the breakdown performance, as they can modify the potential and electric field distribution of the chip periphery. The geometrical arrangement of rings refers to the width of the rings and the spacing between each ring implantation (a section view of guard rings is shown in Figure 3.19).

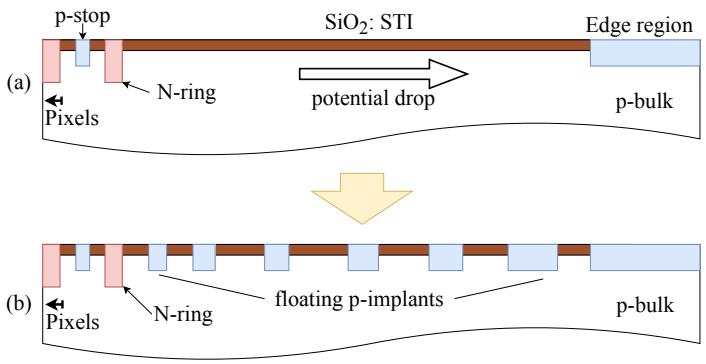



Figure 3.19: Section view of the periphery of a pixel chip consisting of the edge of the pixel matrix and the guard ring region. (a) shows the periphery without floating guard rings, the entire region (from the n-ring to the chip edge) is covered with STI. (b) shows a generic guard ring design, where the guard ring implants breaks the continuous STI. As the edge ring and the seal ring are short circuited, these two structures are merged to be the edge region.

## 3.4 Radiation Damage

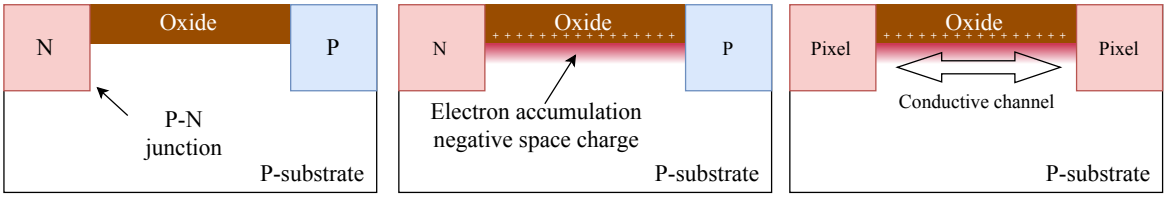
Silicon pixel detectors receive a high flux of high-energy particles, due to their small distance to the collision centre of particle colliders. This causes crystalline defects, as radiation damage, in the sensor material. As the defects accumulate during the operation of the collider and the detectors, the electrical property of silicon sensor is altered, and causes degradation of the detector performance. Therefore, studying the radiation damage is a crucial topic in developing silicon pixel detectors for high energy physics.

The radiation damage occurring in collider experiments is categorised into ***bulk damage*** and ***surface damage*** according to the locations of the defect sites. The bulk damage refers to the crystalline defects created in the silicon substrate of sensors, due to the particle-atom impact and the collision between the recoiling atom and other lattice atoms. The surface damage is associated with the defects in the proximity of the $Si/SiO_2$ interface, and it influences the electrical property of the silicon surface of sensors.

This section introduces the effect of the surface damage in silicon pixel detectors. A more detailed description of the radiation damage is given in appendix C.

### 3.4.1 Electron Accumulation

Surface damage includes the introduction of fixed positive charges in the $SiO_2$ layer, especially in the region of several nm from the $Si/SiO_2$ interface (oxide charge). The increasing positive charge results in the accumulation of electrons underneath the oxide (Figure 3.20 (a) and (b)). For electronics, this




(a) No surface damage (b) With surface damage (oxide charge) (c) Surface damage for pixels

Figure 3.20: The sketch of the influence from the surface damage. In a diode structure similar as in guard ring designs, the p-n junction of the case without surface damage is located surrounding the n-well (a). The oxide charge after surface damage causes an electron accumulation layer (b), which will be at the similar potential as the n-ring. Therefore, the n-well is effectively extended beneath the oxide closer to the p-well. When such an accumulation layer appears in the inter-pixel region (c), it will build up a conductive channel between the n-type pixel electrodes, when no isolation structures (e.g. p-stop) is implemented

effect typically results in a shift of the threshold voltage of a MOS device. Nevertheless, the oxide charge becomes less significant in modern ICs, due to the ever thinned gate oxide (typically in the order of 1 nm). The thick Field Oxide (FOX) is still widely spread on silicon chips, and it will be influenced by the oxide charge. In CMOS sensors, introduced in the previous section, the STI is a type of FOX with a typical thickness of approximately 400 nm.

The subsequent effect of the inversion layer built up underneath the FOX is the dramatic increase of the surface conductivity, due to the large number of mobile electrons. This gives rise to paths connecting n-type implants of devices (with electrons as the majority charge carrier), which should be separated. In the devices of ICs, such conductive paths can significantly increase the leakage

current. In CMOS sensors for particle detectors, although no active CMOS devices are implemented, an inversion layer can modify the conductivity and consequently the potential/electric field distribution between implants. For n-in-p sensors, the n-type pixel electrodes will likely be short circuited by the inversion layer, if no p-type implant (with high hole concentration) are utilised for isolation (Figure 3.20 (c)). Moreover, the inversion layers effectively act as a shallow n-type doping, which can extend the n-well sidewards, and possibly touch the p-well (Figure 3.20 (b)). In this case, the p-n junction is effectively moved closer to the highly doped p-wells, and creates a much narrower junction. This can potentially limit the high-voltage performance of sensors.

CHAPTER 4

# Characterisation and Simulation of Silicon Sensors

The characterisation of a pixel sensor often requires to mimic the operating condition of the sensor. The bias voltage $V_{\text{bias}}$ is applied between the pixel electrodes and the biasing electrode, which is the backside or the edge ring of a sensor (figure 4.1). In applications, the pixel electrodes are usually grounded (at 0 V potential or $\sim$ 1 V, since they are connected to the readout electronics). For measurements of passive sensors, a positive potential can also be applied to the pixel electrodes, whilst grounding the backside or the chip edge. The guard rings and the p-stop are floating, whereas specific tests can be performed by applying potentials at the contacts of the guard ring implants, when the contacts are available, e.g. in the passive-CMOS test structures studied in the following chapters.

This chapter highlights the methods to study the breakdown performance of passive-CMOS sensors through measurements and TCAD simulations.

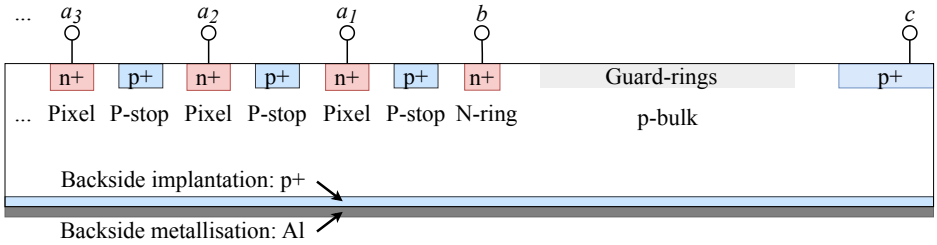



Figure 4.1: Schematic of the electrode contacts (labeled by the italic letters) on a passive-CMOS sensor based on the cross section view of a sensor edge region. $a_1, a_2, a_3, \ldots$ represent the contacts of the pixel electrodes, $b$ is the contact of the n-ring. Contact $C$ is the edge ring of a sensor chip for biasing at the edge (frontside biasing). If the sensor is backside-processed, i.e., with $p^+$ implant and metallisation, the contact $d$ can be used for backside biasing. Details of the guard ring structures are not shown in this schematic cross section.

## 4.1 Current-Voltage Behaviour

Also known as the "I-V curve", the current-voltage behaviour is one of the basic characteristics of silicon pixel sensors, which describes the leakage current response of the sensor to the bias voltage.

### Leakage Current

The leakage current from the bulk of a pixel sensor is the result of the thermal charge generation and the defect centres in the depletion region, where the electric field drives the electrons and holes towards the corresponding electrodes. Therefore, the leakage current increases with increasing bias voltage due to the growing depletion region. The leakage level reflects the signal current baseline of detectors, and contributes to the noise in the form of shot noise. In silicon pixel detectors, a too high leakage current can have a negative impact on the detection performance, namely higher shot noise. Therefore, a higher threshold voltage of the discriminator is necessary to distinguish the signals created by the actual particle from the noise. In such cases, events from particles producing small signals, which could be detected with a lower threshold voltage, will likely be filtered out. Such an upper limit of the leakage current is typically determined by the electronics design. For instance, the design goal of the monolithic detector prototype LFmonopix2 is approximately 5 nA per pixel.

The method to determine the sensor's total leakage current is to observe the current at the pixel electrodes, while sweeping the bias voltage until the nominal operating voltage is reached, at which the sensor is fully depleted.

### Breakdown Voltage

Based on the leakage current measurements, the breakdown behaviour can be observed when the bias voltage is sufficiently high to trigger the impact ionisation across the p-n junction in silicon sensors. The breakdown voltage can be determined by, for instance 1) analysing the slope of IV curve; 2) analysing the voltage behaviour across the diode whilst using a bias resistor; and 3) setting a current limit.

The first method can be applied by defining the onset of breakdown based on a certain slope. For example, a sensor can be defined as being in the breakdown regime when the current is increased by 20% within a 5 V change of the bias voltage.

The bias resistor method requires that the sensor is connected with a resistor, and the bias voltage is added across both parts during the breakdown measurement. This method has the benefit of protecting the sensor from damage due to high current around the onset of breakdown, since the current is limited by the resistor to a safe level. Before the breakdown of a reversely biased p-n junction, the leakage current is typically very small, due to the nature of the diode. The junction effectively has a very high "resistance" in this case. When a resistor, with a relatively small resistance, is connected with the diode in series, the voltage drop mostly takes place across the junction. Therefore, the leakage current of the diode can be measured. If the bias voltage exceeds the breakdown voltage of the p-n junction, the additional voltage will be loaded on the resistor whilst the voltage across the reversely biased diode remains unchanged. The total current flowing through both devices will follow the ohmic law with respect to the resistor. A theoretical explanation of this method is presented in Appendix B.

The current limit method is used in the TCAD breakdown simulations for extracting breakdown voltages. In this case, a current value in the breakdown regime of the IV curves is set as the reference, and the breakdown voltage is defined as the voltage where the leakage current reaches the reference. Due to the very large slope of the IV curve in the breakdown regime, the breakdown voltage obtained using this method will be very close to the actual onset of the junction breakdown. This method can be employed for comparing the sensors with similar leakage current levels, e.g., sensors having similar sizes of pixel matrices and thicknesses. As for comparing the sensors with dramatically different

leakage current levels or behaviour of IV curves, such as the comparison between non-irradiated and irradiated samples, as discussed in chapter 5.5, choosing different reference current values may deliver different results. For example, the reference current may be in the breakdown regime of one sensor, but not of the other sensor which has a higher leakage current level. Comparing the breakdown voltages of the typical breakdown regime requires a large reference current. If the leakage level of a sensor is too high, the detection performance may be significantly degraded even before the typical sensor breakdown occurs. By setting the reference current according to the performance of the electronics, the term "breakdown" is not only limited to the p-n junction breakdown in the sensors, but also reflects the upper limit of the detector's detection performance that is constrained by the leakage current in sensors.

## 4.2 TCAD Simulation

***Technology Computer-Aided Design*** (TCAD) is immensely influential within the semiconductor industry, serving as an indispensable tool for simulating device performance. This capability not only facilitates the design process but also significantly reduces both time and cost. Fundamentally, TCAD tackles the essential physical partial differential equations (PDEs) that delineate the physics of semiconductor devices. Through the application of the finite element method, these PDEs are evaluated across a mesh grid, enabling accurate modelling of device behaviours.

Within the sphere of detector physics and the study of radiation damage effects, TCAD is crucial for the design and optimisation of semiconductor detectors, as well as for modelling the impacts of radiation damage. In this work, Sentaurus TCAD, provided by Synopsys, is utilised to explore the breakdown performance for various guard ring designs. Sentaurus TCAD offers a suite of tools for various simulation purposes: `sprocess` is used to construct the sensor structure, whilst `sdevice` is employed to investigate the electrical properties of the device. Central to a breakdown simulation is the simulation of the current-voltage characteristics which is extracted and analysed. In addition, TCAD offers the visualisation of physical quantities, that are hard to access from measurements. As an example, the potential, electric field, and charge carrier current densities in the device provide insights for understanding the electrical performance.

### 4.2.1 Process Simulation

Typically, TCAD tackles the modelling of a certain electronic device in the integrated circuits, and hence only a slice of a wafer is constructed to contain the device to be studied. The generic procedure of the process simulation starts with initialising the simulation domain, including the thickness of the wafer and the wafer properties, such as the substrate doping level and lattice orientation. Mesh grids can be defined in 1D, 2D, and 3D, depending on the symmetry of the device geometry and the problems under study. A 2D simulation is typically sufficient for a qualitative study of a device with symmetrical geometry, since a 3D simulation usually requires a larger consumption of computing power and time. To establish the device structure, `sprocess` allows one to simulate the processing sequence introduced in section 3.3.1. By carefully defining the masks, the ion beam profiles, and the thermal treatment parameters, the device can be constructed by arranging the commands for implantations and annealing processes to imitate the actual manufacturing steps in the simulation

script. The device structure is finalised by regenerating the mesh grid to adapt to the device geometry (e.g. the gradient of implants and the interfaces between materials) and adding the electrical contacts to define the electrodes (Figure 4.2). The new mesh grid will be more suitable for the later device simulation, since the region with a larger doping gradient or near the interface requires a higher precision to correctly calculate the electrical properties, e.g. potential, electric field distribution, and charge carrier transportation.

### 4.2.2 Device Simulation

The electrical behaviour of devices is simulated by numerically solving Poisson's equation and the charge transportation equations. In this work, the drift diffusion model (Eq. (2.6)) and the continuity equations (Eq. (2.5)) are used. The key ingredient for simulating the avalanche breakdown is the modelling of the impact ionisation coefficient, where the van Overstraeten – de Mann model (equation (2.28) and Table 2.1) is implemented. The Shockley-Reed-Hall recombination model (section 2.6.1) is activated to include the influence of the surface damage. The trapping time further adopts the Scharfetter relation [18] for the doping dependence, the Schenk model [19] for temperature dependence, and the Hurkx trap-assisted-tunnelling model [20] for the field enhancement. In addition, the Hurkx band-to-band tunnelling model [20] are also considered in the simulation.

#### Breakdown Simulation

Unlike extracting the current voltage behaviour of a device in a standard operation condition (typically with low applied voltage and low current), the difficulty of the breakdown simulation is the rapid increase of the current when the applied voltage is approaching the breakdown regime. Such a sudden change of leakage current can cause convergence issues of the numerical simulation and leads to computation errors. The TCAD device simulation supports the breakdown analysis using

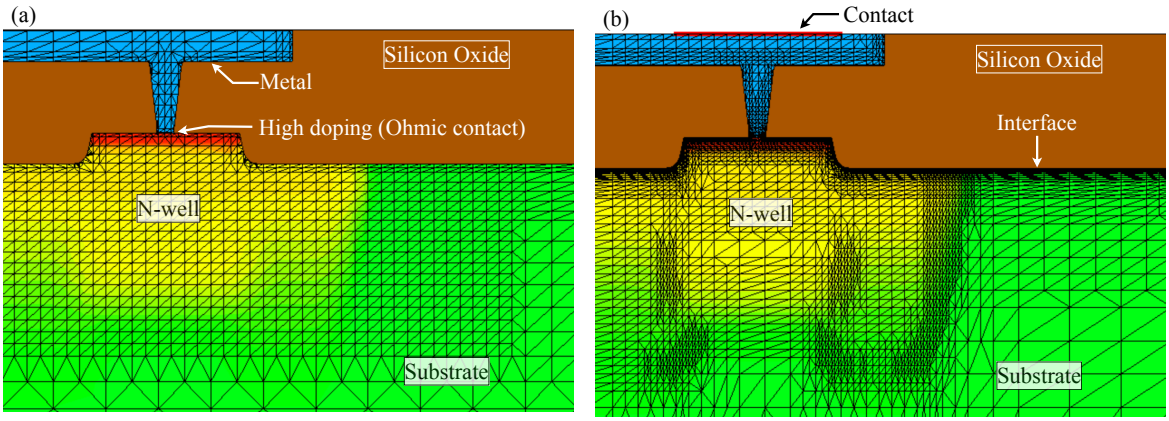



Figure 4.2: Finalising the simulation domain in the process simulation. (a): The structure before regenerating the mesh grid, where a uniformly fine grid (black lines) is established at the location of n-well for achieving a fine doping gradient.; (b): the new mesh grid features a finer grid at the region of large gradient and at the $Si/SiO_2$ interface. The metal is in contact with the high doping n-type layer at the n-well, forming an ohmic contact. The electrical contact for the upcoming device simulation is defined (placed) at the metal layer, which is electrically connected with the underlying n-well.

the ionisation integrals (the integral in equations (2.26) and (2.27)) by integrating them along the paths in the device. This method is purely based on the solution of Poisson's equation, which requires little computation effort. However, since it does not include the charge carrier transportation, no current voltage behaviour can be extracted for comparison with measurements. A more intuitive way is the "transient" method, where the electrodes (defining boundary conditions of the simulated device) for applying the bias voltage are ramped within the defined time window with a certain speed. By applying the avalanche generation in the transportation model, the current-voltage behaviour is preserved. The breakdown voltage can then be determined using the reference current method, so that comparisons between guard ring structures can be achieved.

### Surface Damage

The surface damage occurs at the $Si/SiO_2$ interface even before the device has received any irradiation. The model used in this work follows the "Perugia" surface damage model [66], where the pre-irradiated positive charges and the trapping levels are considered and the influence from ionising irradiations are modelled as a function of the received TID.

The set of passive-CMOS test structures studied in this work were not designed for characterising the surface condition, therefore a dummy model based on the results in [66] was used (Table 4.1). Besides

| **Type** | **Pre-irradiation** | **Function of TID** |
|---|---|---|
| $Q_{OX} = Q_{OX}^{pre} + \Delta Q_{OX}$ | $Q_{OX}^{pre} = 1.00 \times 10^{10}$ | $\Delta Q_{OX}(TID) = 3.74 \times 10^{11} + 6.20 \times 10^{10} \cdot \ln[TID]$ |
| $N_{acc} = N_{acc}^{pre} + \Delta N_{acc}$ | $N_{acc}^{pre} = 1.00 \times 10^{9}$ | $\Delta N_{acc}(TID) = 6.35 \times 10^{11} + 1.50 \times 10^{11} \cdot \ln[TID]$ |
| $N_{don} = N_{don}^{pre} + \Delta N_{don}$ | $N_{don}^{pre} = 1.00 \times 10^{9}$ | $\Delta Q_{OX}(TID) = 1.07 \times 10^{12} + 2.90 \times 10^{11} \cdot \ln[TID]$ |

Table 4.1: The surface damage model based on [66].

the oxide charge $Q_{OX}$ (/cm$^2$), this model features energy distributions of the acceptor-like $N_{acc}$ (/cm$^2$) and a donor-like $N_{don}$ (/cm$^2$) interface traps. Both types of trapping levels are distributed uniformly in the band gap, where: 1) for acceptor-like levels the distribution is centred at $E_{acc} = E_v + 0.84\,eV$ with a width of $E_{acc}^{sig} 0.56\,eV$; and 2) for donor-like levels the distribution is centred at $E_{don} = E_v + 0.60\,eV$ with a width of $E_{don}^{sig} 0.3\,eV$, according to the supplement material of [66]. As the distribution is on the energy scale, the energy density of the distribution $D_{acc,don} = N_{acc,don}/E_{acc,don}^{sig}$ is used for defining the trapping levels in the simulation.

CHAPTER 5

# Test Structures From a Multi-Project Wafer (MPW) Submission in 2016

The main content of this chapter has been published in the journal Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment in 2020 with the title *Breakdown performance of guard ring designs for pixel detectors in 150 nm CMOS technology* [67].

Six types of passive-CMOS test structures were designed and fabricated in 2016 for studying different guard ring designs and inter-pixel structures of a silicon pixel sensor. The generic layout of a test structure is illustrated in Fig. 3.16 and 3.17 in section 3.3.2, consisting of a pixel matrix with elongated pixels and a series of guard ring implants surrounding the matrix. Variations between test structures result from the combination of different guard ring designs and inter-pixel structures.

The test structure chips were fabricated by LFounrdy [57] using a commercial 150 nm CMOS process on high-resistivity substrates, which are Czochralski-grown p-type wafers with a foundry-specified resistivity of $4 \sim 5\,\mathrm{k\Omega \cdot cm}$ [68]. The original chip thickness was 725 µm, whereas the chips used for this thesis were thinned down to 200 µm with backside implantation and metallisation.

The passive-CMOS test structures are labelled with letters "A" to "F" [1], and located on the same die, as illustrated in figure 5.1. Metal bonding pads were fabricated for accessing each implant on the test structures for characterising the electrical properties, as previously introduced. The pads labelled with "N-well" and "N-single" are connected to the n-type charge collection electrode of all the pixels. One pixel inside the pixel matrix is connected to the "N-single" pad, whereas the collection electrodes for the remaining pixels are all short-circuited and connected to the "N-well" pad. The "N-ring" pad gives access to the n-ring implant surrounding the pixel matrix, and the "P-stop" pad is attributed to the inter-pixel isolation structure. The pads with the name containing "GR" are connected to the p-type implants of the guard rings. The bias voltage can be applied via the bonding pad labelled with "Bias".

In this chapter, the measurements and simulations of the breakdown performance with respect to the guard ring designs are presented.

[1] This set of labelling also indicates the corresponding guard ring and/or inter-pixel structure design.

## 5.1 Inter-pixel Structure and Guard Ring Designs

Zooming in on the pixel matrix, the generic layout of a single pixel is schematically illustrated in Figure 5.2 (a) and (b).The layout (a) is applied to the test structures A, B, C, D, and F. As an n-on-p sensor, the n-type implants are utilised to form electrodes for charge collections, and the p-stop using p-type implant is adopted to isolate the electrodes of adjacent pixels. Figure 5.2 (c) and (d) illustrate the schematic section views, showing the inter-pixel region indicated by the dashed cutline in (a). The cross section (c) represents the structure A, where the standard n-well (NW) is used to form the collection electrodes, and the p-stop was formed by using the standard p-well (PW). Attaching to the PW implant, 3 conductive layers, 1 polysilicon (Poly) and 2 metal layers (M1 and M2), above the silicon surface were implemented to construct the overhang structures. The edge of the overhang exceeds the edge of the p-stop, so that the electric field between the p-stop and the collection electrode is suppressed [69]. Test structures B, C, D, and F are also equipped with p-stop, which has the same layout of implant and overhang as the structure A, but the pixel electrodes are formed with a deep n-well which is a combination of NW, NISO, and DNW implants (Figure 5.2 (d)). Instead of using the p-stop, the structure E is equipped with the polysilicon field-plate placed above the STI as the inter-pixel structure, as depicted in Figure 5.2 (e). Voltages can be added to the field-plate via the bonding pad "p-stop" in Figure 5.1.

The guard rings of all test structures have a similar layout as presented in Figure 3.17 of section 3.3.2, and consists of an n-ring, floating guard rings, and an edge ring. The designs of the test structures

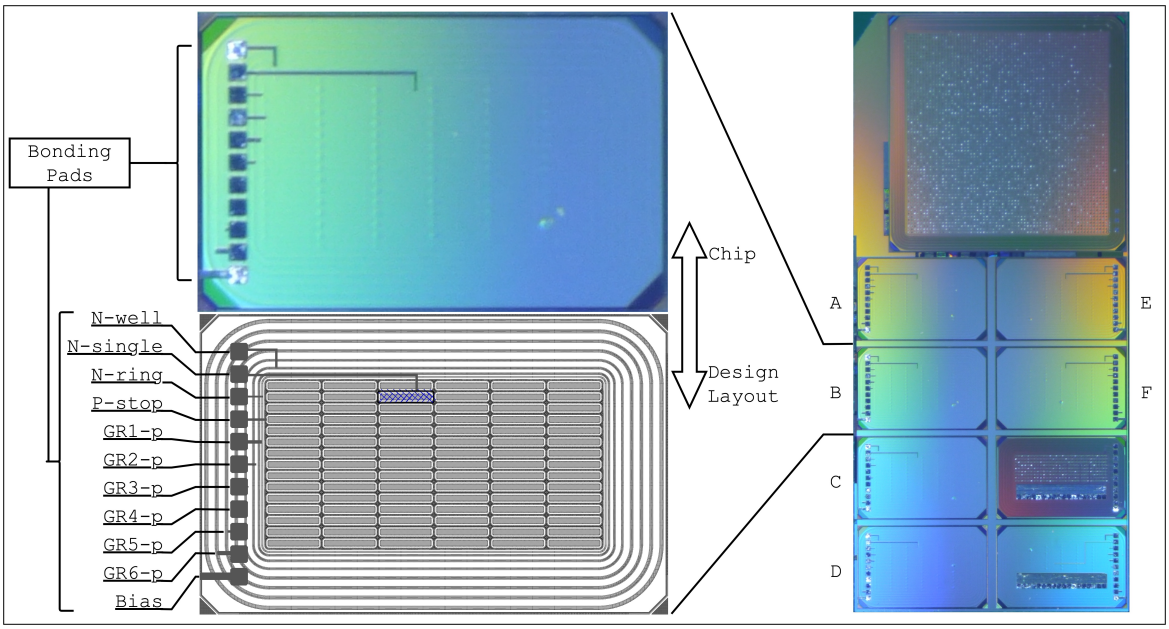



Figure 5.1: The chip of the test structures, and the bonding pads. The right part shows a photo of a single die where all the test structures ("A" to "F") are located. The rest of the part on the chip die is irrelevant for this thesis. A photo of structure "B" on the upper left shows the appearance of a test structure, from which we can identify the bonding pads arranged in an array. For comparison, the design layout of structure B is placed on the lower left. The pads are labelled according to the implants/parts of the structure, to which they are connected, and the "N-single" is connected to the dashed pixel in the pixel matrix.

differ in

- the implant of the n-ring (and collection electrode): standard n-well (NW) in structure A; deep n-well (NW + NISO + DNW) in structure B to F
- the number of floating guard rings: 6 rings in A, B, and D; 5 rings in C, E, and F
- the implant type of the guard rings: p-type rings in A and D; n+p type rings in B, C, E, and F
- the overhang of the floating guard rings: A to E with the edge of the overhang exceeding the edge of the implant's edge; F with the overhang within the width of the implant.

The section view of test structures is visualised in Figure 5.3. Structure A is the basic design of the test structure, where the PW implants are implemented for the floating guard rings and the edge ring. The distance between the n-ring and the p-stop at the edge of the pixel matrix has been set to have the same value as the distance between the collection electrode and the p-stop. Starting from the n-ring towards the edge ring, the width of the guard ring implants and the spacing between neighbouring ones gradually increases. Structure D adopts the identical guard ring geometry of A, except for the implant of the n-ring, which uses the same deep n-well implant as for the pixel electrodes. A variation of the guard ring structure based on structure D is implemented in structure B, where the floating guard rings are equipped with an extra NW implant on the outer side of each floating p-well ring (the "n+p" ring). The n-well at all the floating guard rings has the same width of 4 µm, and is placed

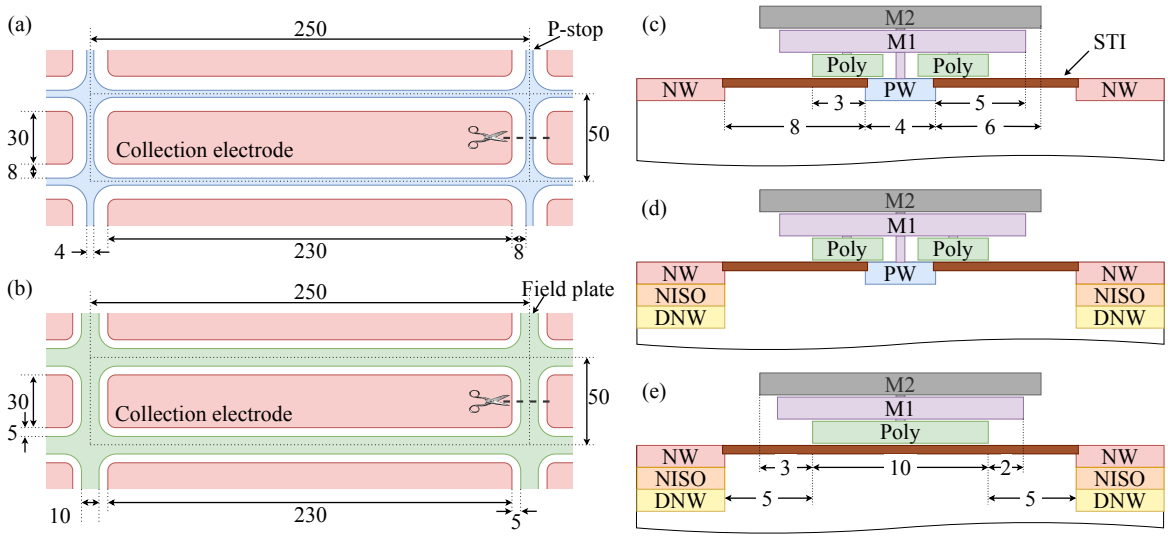



Figure 5.2: Pixel layouts and section view of the inter-pixel region, with the design parameters given in µm. The top view of one pixel (enclosed by the dotted lines) and the surroundings are illustrated in (a): n-type collection electrode and the p-type p-stop isolation structure, for structure "A", "B", "C", "D", and "F"; (b): n-type collection electrodes and polysilicon field-plate surrounding pixels for structure "E". The dashed cutline represents the inter-pixel region whose the section view are illustrated in (c) to (e). (c): structure "A", with standard n-well (NW) as the collection electrode. (d): structure "B", "C", "D", and "F", with deep n-well consisting of NW, NISO, and DNW implants. The overhang structures are identical for both cases, and formed with the polysilicon layer (Poly) and two metal layers (M1 and M2). (e): structure "E", with the polysilicon field-plate.

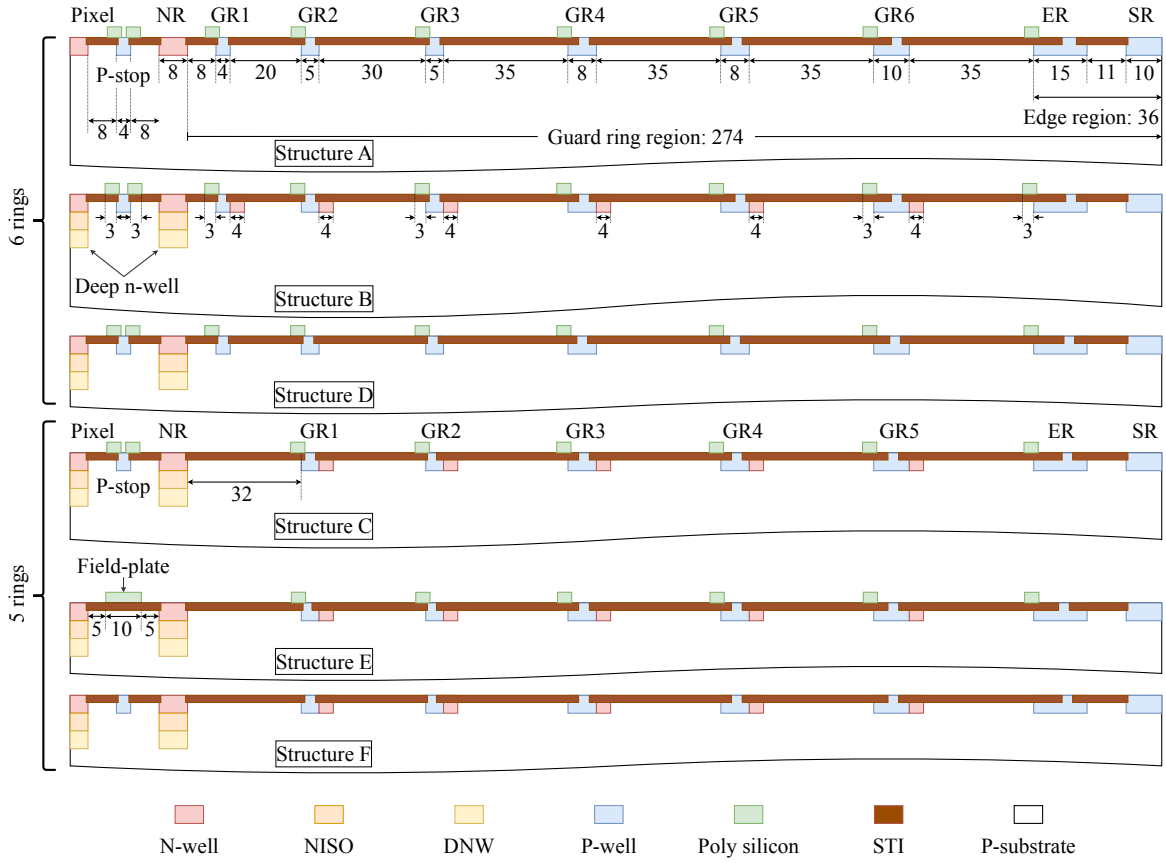



Figure 5.3: Schematic section view of the guard ring implants. The geometrical parameters are given in µm. From the matrix side (inner side) the cross sections include a part of the collection electrode of the pixel at the edge of the matrix (“Pixel”), the p-stop, the n-ring (“NR”), the floating guard rings (“GR1” to “GR6”/“GR5”), the edge ring (“ER”), and the seal ring (“SR”, the edge of the test structure). The edge ring and the seal ring are p-type implants for all test structures. The floating guard rings in “A” and “D” are formed with p-wells, having the identical geometry, whereas the n-ring and the pixels in “D” are formed with deep n-well. Structure “B” is designed based on structure “D”, where a floating n-well ring is attached besides each p-type guard ring (“n+p” ring). Structure “C”, “E”, and “F” are equipped with 5 n+p floating guard rings with identical implant geometry. The 5-ring configuration is designed by removing the innermost guard ring of structure “B”.

directly next to the p-well. Structures C, E, and F are equipped with a 5-guard ring structure with n+p rings. The 5-ring design is achieved based on removing the innermost guard ring of the 6-guard ring design for structure B. Therefore, the innermost guard ring in the 5-ring layout is the GR2 in the 6-guard ring layout. The distance between GR1 and n-ring in the 5-ring design becomes 32 µm.

Two types of overhang structures were designed for the test structures, as schematically depicted in Figure 5.4. Using the polysilicon layer and two metal layers, the overhang of the floating guard rings

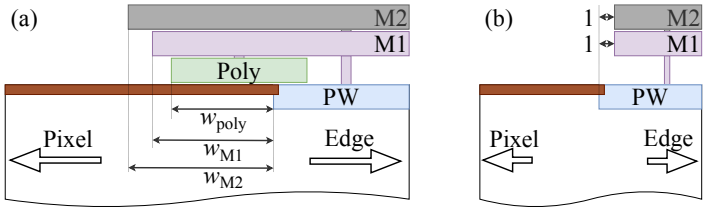



Figure 5.4: Section view illustrating the overhang design of the guard rings. The overhang is attached to the p-implant of the guard ring, and consists of the polysilicon layer (Poly) and 2 metal layers (M1 and M2). All the layers are electrically connected with the implant of the guard ring, so that they are at the same electrostatic potential. (a): Overhang design for structure "A" to "E", with the edge of the polysilicon and metal layers exceeding the edge of the p-well implant of the guard ring and facing towards the pixel matrix. For 6 guard ring test structures: $w_{poly}$ = 3 µm, $w_{M1}$ = 5 µm, $w_{M2}$ = 6 µm applies for GR1, and $w_{poly}$ = 3 µm, $w_{M1}$ = 10 µm, $w_{M2}$ = 13 µm for "GR2" to "GR6", and "ER". For 5-ring test structures, $w_{poly}$ = 3 µm, $w_{M1}$ = 10 µm, $w_{M2}$ = 13 µm is applied to all the floating guard rings and the ER. (b): No overhang in structure "F", where the polysilicon layer is removed and the edge of metal layers do not exceed the edges of the p-implant.

in A to E faces towards the pixel matrix, with the edge exceeding the edge of the p-well. These layers have electrical contact with the p-well, and will be at the same electrostatic potential as the implant (Figure 5.4 (a)). Structure "F", on the other hand, is not equipped with an overhang, as the polysilicon is absent, and the metal layers have a smaller width than the p-well 5.4 (b)).

The aforementioned characteristics of test structures are summarised in Table 5.1.

Table 5.1: Features of guard rings in the test structures. "GR1 gap" refers to the distance between the GR1 and the n-ring of each structure.

| Label | Implant | Overhang | # Rings (GR1 Gap) | Inter-pixel structure | Deep n-well |
|---|---|---|---|---|---|
| A | p | Yes | 6 (8 µm) | p-stop | No |
| B | n+p | Yes | 6 (8 µm) | p-stop | Yes |
| C | n+p | Yes | 5 (32 µm) | p-stop | Yes |
| D | p | Yes | 6 (8 µm) | p-stop | Yes |
| E | n+p | Yes | 5 (32 µm) | field-plate | Yes |
| F | n+p | No | 5 (32 µm) | p-stop | Yes |

## 5.2 Measurements and Simulations

The sensor breakdown of CMOS sensors fabricated in the LFoundry 150 nm CMOS process was studied using the test structures. Measurements of the breakdown voltage and the voltage at the floating guard rings were performed in the lab environment (room temperature, unless specified). The

device under test (DUT) was shielded from light during measurements, to ensure that the obtained (leakage) current was only from the thermal generation. TCAD simulations were established by adopting the design parameters, to facilitate a qualitative comparison with the measured data, search for the explanations of observed effects, and predict the performance of the sensors after introducing radiation damage.

### 5.2.1 Sensor Breakdown

Breakdown voltages of test structures were obtained by current-voltage measurements (section 4.1). A bias voltage was added between the collection electrodes and the seal ring, which means that the "N-well" and"N-single" pads in Figure 5.1 were connected to the low potential (ground), and a negative high potential was applied at the "Bias" pad. The DUTs were measured in two scenarios, with respect to two connection schemes of the n-ring:

- grounded n-ring: the pad "N-ring" is grounded together with the collection electrodes of the pixels;
- floating n-ring: the pad "N-ring" is not connected to any fixed potential during the measurements.

Using the designed voltage setting for operating chips, the directions of the electrostatic potential drop in the guard ring region are illustrated in Figure 5.5. The potential generally drops in two directions. The first one labelled with "(1)" in Figure 5.5 illustrates that the potential drops from the grounded n-ring and the pixel electrode towards the floating p-stop, because the floating potential at the p-stop is lower than the grounded n-ring and pixel, after full depletion of the sensor. The second direction is from the n-ring to the edge of the chip (at a negative high potential), across the floating guard rings, labelled with "(2)".

Changing to the floating n-ring effectively makes the p-stop (or the field-plate) and the n-ring the innermost floating "guard rings", as they become a part of the entire path of potential drop from the grounded pixels to the bias potential at the chip's edge (Figure 5.6). This change helps to understand the effect of the deep n-well and the field-plate on the breakdown performance. For structure E, an additional voltage can be applied at the polysilicon field-plate. Due to the MOS structure, such a voltage has an influence on the potential at the silicon surface beneath. A study in [70] used a similar structure and measurement setting showing a change in the breakdown voltage, but the field-plate was placed at the edge of an implant to modify the local potential distribution. This result inspired

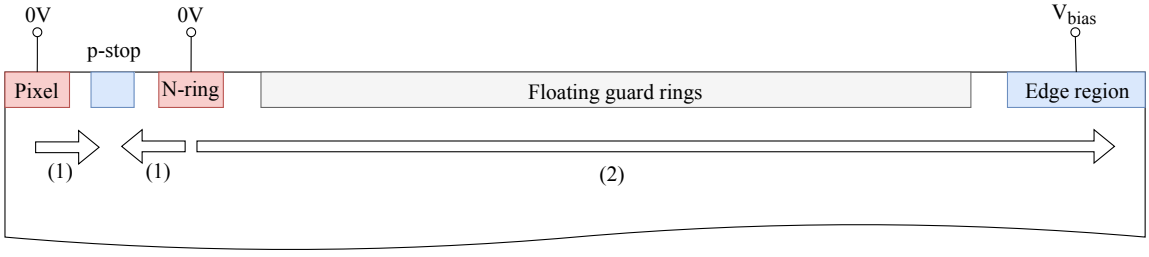



Figure 5.5: Schematic illustration of the potential drop at the guard ring region when the n-ring is grounded. Two parts of the potential drop exists in this voltage setting: (1) between pixel charge electrode/the n-ring and the p-stop; (2) between the n-ring and the pixel edge.

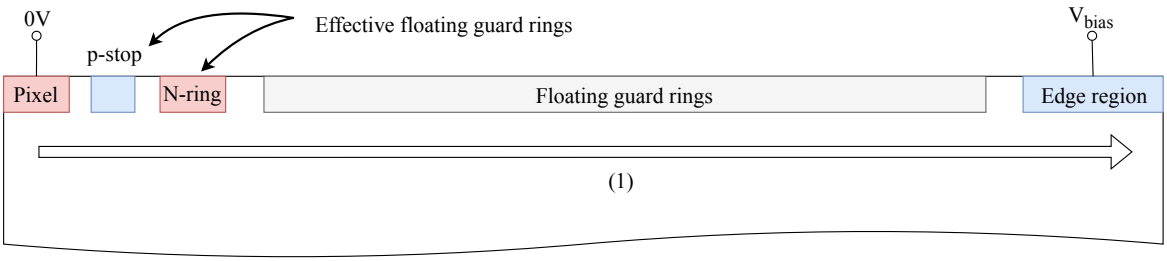



Figure 5.6: Schematic illustration of the potential drop at the guard ring region when the n-ring is floating. (1): the direction of the potential drop from the pixel collection electrode to the edge of the chip. The potential drop between the pixel collection electrode and the p-stop inside the pixel matrix is not illustrated.

the application of the overhang structure [71]. Here, the field-plate in structure E is used to study its influence on the overall potential distribution.

**X-ray Irradiation** The effect of TID was investigated using the X-ray irradiation machine in Bonn [72]. An X-ray tube, depicted in Figure 5.7, was used as the X-ray source. Thermally generated electrons are accelerated in the vacuum tube by a high voltage, and bombarded onto a metal target. The X-rays are emitted through the beryllium window and reach the DUT to be irradiated. The emitted beam intensity profile is depicted in Figure 5.8. Depending on the distance to the X-ray tube's emission window, the beam profile has different peak intensity and beam diameter (Figure 5.9), whilst the shape of the beam profile remains similar. The peak intensity indicates the TID rate that is received by the $SiO_2$ of the silicon sensors, i.e. a higher intensity for a small distance represents a higher dose rate. During irradiation, the sample was placed in a thermal insulation box made with plastic, with a Kapton window for transmitting the X-ray beam. Inside the box, the DUT carried by a printed circuit board was mounted onto a copper block, which is attached to the cooling facility, through thermal conductive adhesive. A mounting board connected to the carrier PCB was developed to provide sockets for the measurement (Figure 5.10). During the irradiation, a bias voltage of $-150\,\mathrm{V}$ was applied to the DUT, so that the sensor bulk was fully depleted to mitigate the operating condition of actual detectors.

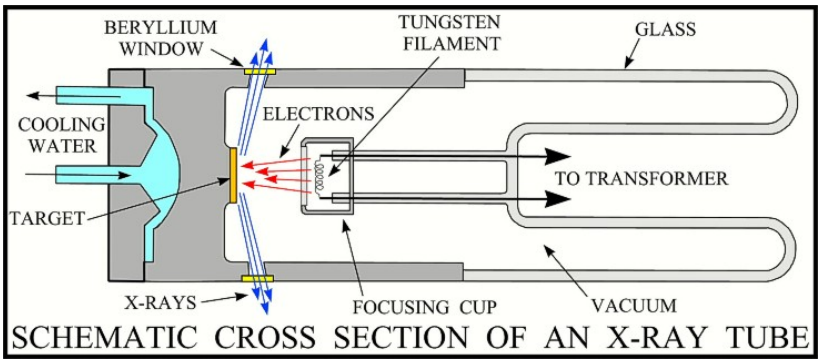



Figure 5.7: Schematics of the X-ray tube. [73]

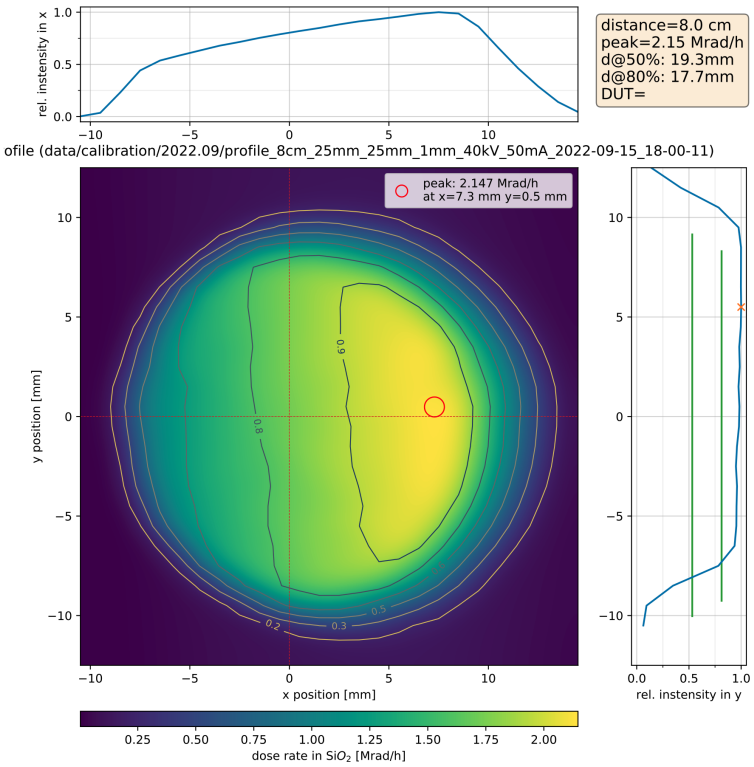



Figure 5.8: Beam profile of the X-ray tube in Bonn. This intensity distribution was obtained at a distance of 8 cm to the emission window tube, before starting to irradiate samples.

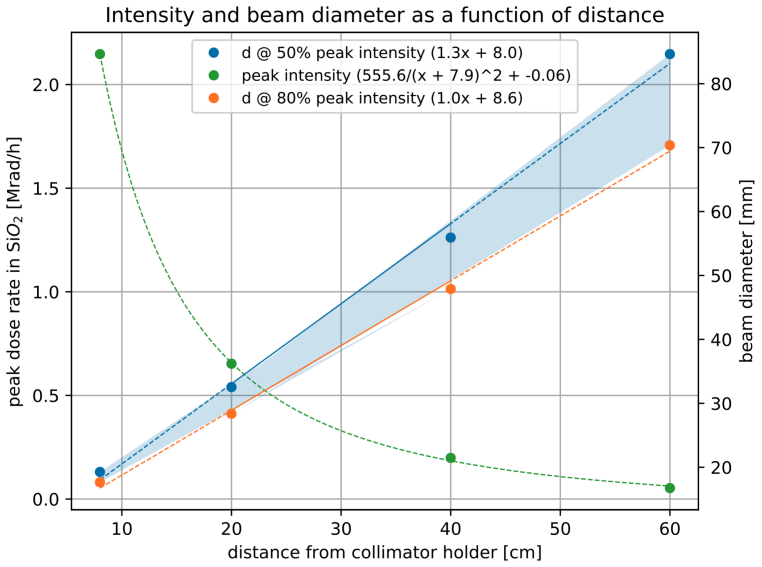



Figure 5.9: Beam diameter and peak intensity (converted to dose rate in $SiO_2$) as a function of the distance from the emission window of the X-ray tube.

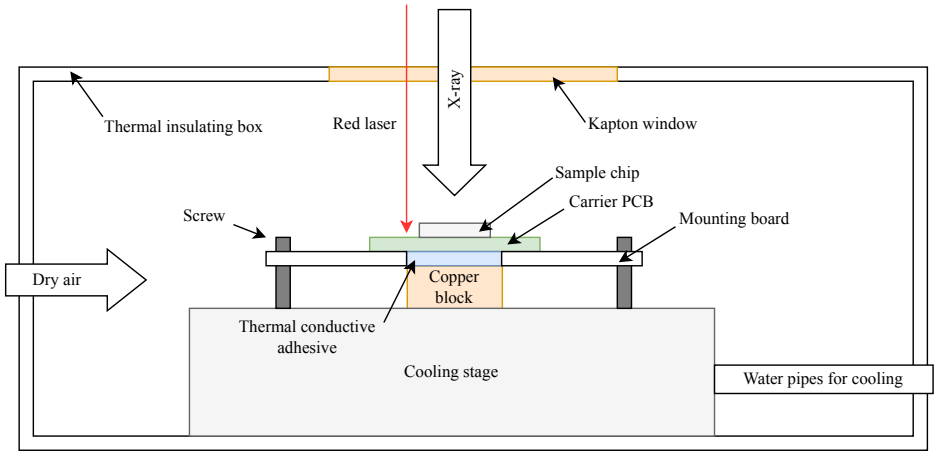



Figure 5.10: Schematic section view of the sample chip placement. The chip was mounted onto the cooling stage in a polymeric foam thermal insulating box via the mounting board, where the board was screwed onto the cooling stage. Dry air was used in the low temperature (−10 °C) ambient for reducing the humidity and prevent water condensation on the chip. The red laser mounted in the X-ray cabinet was used for aligning the chip according to the beam profile, before the irradiation process.

**Samples and Measurements** Seven samples (S1-S7) of the chip depicted in Figure 5.1 were utilised to measure the breakdown voltage of the test structures. The IV curves were obtained by ramping the bias voltage from 0 V until the current reached 10 µA under all measurement conditions. For irradiated samples, measurements were conducted in the X-ray cabinet at a temperature of −10 °C immediately following each irradiation step. The voltage at the floating guard rings in selected samples was probed at a bias voltage of −200 V. This was accomplished by probing the associated bonding pads shown in Figure 5.1 with respect to the ground. Additionally, the voltage at the p-stop and the n-ring (if floating) was also measured. Table 5.2 lists the samples and the passive-CMOS test structures that were measured for this thesis. Each test structure design was sampled from multiple chips, and the breakdown voltage of all the test structures was measured. Irradiation was performed on Structures C and F for Samples S4, S5, and S6. The samples S4 and S6 were placed 10 cm away from the emission window, so that they receive a TID rate of approximately 1.67 Mrad/hour. A lower intensity was applied for irradiating the sample S5 by increasing the distance to 20 cm, representing a TID rate of approximately 0.65 Mrad/hour. The voltage distribution in the guard ring region was obtained for Structures B, C, and F on samples S4, S5, and S6 before irradiation.

### 5.2.2 TCAD Simulation

The 2D simulation domain for TCAD is built according to the section views in Figure 5.3 for breakdown simulations, as shown in Figure 5.11. The simulation domain included the Si, the $SiO_2$, and the polysilicon and metal layers of the overhang structure. The geometry of the implants was implemented according to Figure 5.3 using process simulation. $SiO_2$, located at the top surface of the Si-bulk, served as the material for the STI and the dielectric filling the empty spaces between the overhang and the field-plate structures. In this context, only the polysilicon and the first metal layer (M1) were used to illustrate the influence of the overhang on the breakdown voltage.

Table 5.2: The samples and test structures for measurements.

| | | Test structure | | | | | |
|---|---|---|---|---|---|---|---|
| | | A | B | C | D | E | F |
| Sample | S1 | | BD-fNR BD-gNR | BD-fNR BD-gNR | BD-fNR BD-gNR | BD-fNR BD-gNR | BD-fNR BD-gNR |
| | S2 | BD-fNR BD-gNR | BD-fNR BD-gNR | BD-fNR BD-gNR | BD-fNR BD-gNR | | |
| | S3 | BD-fNR BD-gNR | | | | | BD-fNR BD-gNR |
| | S4 | | | BD-fNR BD-gNR V-probe TID | | BD-fNR BD-gNR | |
| | S5 | | BD-fNR BD-gNR | V-probe TID | BD-fNR BD-gNR | | V-probe TID |
| | S6 | BD-fNR BD-gNR | V-probe | | | | BD-fNR BD-gNR V-probe TID |
| | S7 | | | | | | BD-fNR BD-gNR |

BD-fNR BD-gNR V-probe TID

The electrical connection between the edge ring (ER) and the seal ring (SR) was implemented differently than in the produced test structure. In the chip design, these two parts were connected via a higher metal layer (the 4th metal layer, which was not used in the simulation). Nevertheless, using layer M1 still realised the connection. Another method to achieve the electrical connection was by using a p-well implant to fill the gap between the ER and SR. This method was also applied to the produced structure. Therefore, both the M1 and the p-well were implemented in the simulation to connect the ER and SR.

For the breakdown simulation, 0 V was applied to the pixel electrode (the leftmost deep n-well) and the n-ring (NR), while the voltage at the seal ring was ramped from 0 V to −1 000 V. The simulation stopped when the leakage current reached a fixed value, at which point a clear breakdown curve was visible (the leakage current increased by more than three orders of magnitude within several volts). In addition to the comparison with measurement data, the radiation damage effects were discussed based on the simulation results.

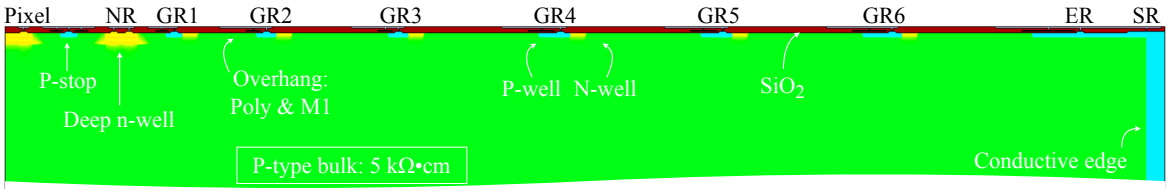



Figure 5.11: Simulation domain for investigating the breakdown voltage of test structure B. The $SiO_2$ is presented in brown colour at the top of the simulation domain, which includes the STI and the filling between the overhang. Silicon is located beneath the $SiO_2$, where the colour scale represents the doping types and concentration: yellow represents the high concentration n-type silicon; blue represents the high concentration p-type silicon; green is the and bulk represents the low concentration (high resistivity) p-type silicon. High doping p-type material is also applied at the edge of the domain, from the seal ring (SR) to the backside (not shown). This is used to model the conductive cutting edge of the chip.

## 5.3 Breakdown Performance

### 5.3.1 Grounded N-ring

The IV-curves for test structures A, B, C, D, and F, each with a floating n-ring, are depicted in Figure 5.12. Across all samples and test structures, the leakage current starts at approximately 0.1 nA and increases with the magnitude of the bias voltage $|V_{\text{bias}}|$. Initially, in the low voltage range, the current increase was gradual, with the leakage current remained within the same order of magnitude. For example, the leakage current for structure C remained below 10 nA for $|V_{\text{bias}}| \lesssim 400\,\text{V}$. However, a sharp rise in leakage current was observed as the bias voltage approaches the breakdown voltage of the sensor's p-n junctions. For instance, the leakage current in structure A increased by more than three orders of magnitude within a few volts after $V_{\text{bias}} \approx -170\,\text{V}$. The breakdown voltage for each structure, as determined from data points where the leakage current reached about 1 µA, varied, indicating different breakdown thresholds across the test structures.

Variations in the IV curves among the samples were noticeable, particularly in terms of breakdown voltage and leakage current levels. These discrepancies were likely caused by process variations during manufacturing, imperfections in the structure, or errors in the sample preparation. For example, the abnormal leakage current observed in structure F for samples S3 and S7—where the leakage current sharply increases at $V_{\text{bias}} \approx -100\,\text{V}$—was likely due to flaws in the backside processing [68, 74]. With a resistivity of $5,\text{k}\Omega \cdot \text{cm}$, the 200 µm thick sensor bulk was fully depleted at $V_{\text{bias}} \approx 100\,\text{V}$. The backside process introduced a thin, heavily doped p-type layer which prevented the depletion region from reaching the silicon surface, a site of high crystalline defect concentration. These defect centres

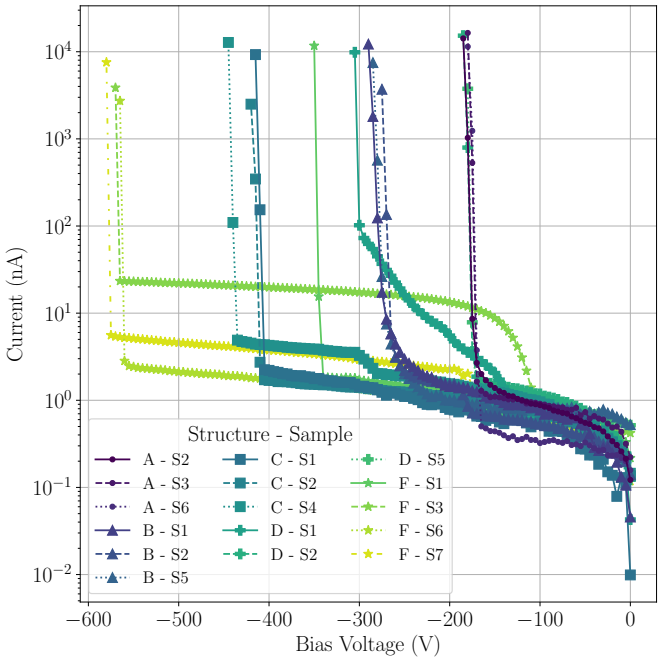



Figure 5.12: IV-curve for structure A, B, C, D, and F, with grounded n-ring. The markers indicates the test structures, and the samples are distinguished by the line style.

contributed to leakage current generation. When the depletion zone reached the damaged surface, the generated charges were accelerated by the electric field and collected by the electrodes. Meanwhile, the heavily doped layer inhibited further expansion of the depletion zone and, by concentrating charge carriers at the surface, increased the recombination rate, thus mitigating charge generation by surface defects.

An anomalously low breakdown voltage in structure F of sample S1, about 200 V lower than in other samples, was noted. This anomaly might have been linked to a fabrication error or an issue during sample preparation, such as the n-ring implant being detached from the ground potential (refer to section 5.3.2). Consequently, data from this sample was excluded from further analysis. Similarly, the exceptionally high breakdown voltage observed in structure D on sample S1 was omitted from analysis, as it exceeded that of other samples by more than 100 V. The cause of this deviation remains unexplained but could have the same origin of the exponential rise in leakage current from approximately −100 V to the breakdown voltage.

The IV curves derived from the breakdown simulations are illustrated in Figure 5.13. Since the leakage current is proportional to the depletion volume, the exact values from the 2D simulation are not directly comparable with the measured data. Therefore, the current axis has been scaled relative to the leakage current level prior to the onset of breakdown and is presented in arbitrary units. From Figure 5.13, it can be seen that structure A exhibits the lowest breakdown voltage of approximately −180 V, followed by structures D, B, C, and F. This sequence qualitatively mirrors the measurement results shown in Figure 5.12.

The breakdown voltages extracted from both measurements ($V_{\mathrm{BD,meas}}$) and simulations ($V_{\mathrm{BD,sim}}$) are presented in Table 5.3. Structures A and D, utilising 6 floating p-well guard rings, exhibited the

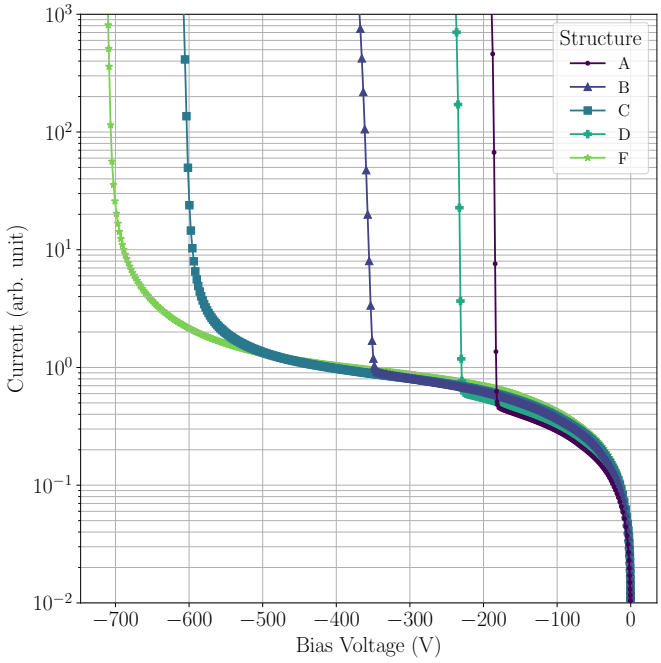



Figure 5.13: Simulated IV curves of test structures A, B, C, D, and F with grounded n-ring.

Table 5.3: Breakdown voltages of the test structures A, B, C, D, and F with grounded n-ring. $V_{BD,meas}$ represents the breakdown voltage obtained from measurements, and $V_{BD,sim}$ indicates the simulated breakdown voltage. The breakdown voltages were extracted using the "current limit" method. For measurements, the voltage corresponding to 1 µA leakage current is considered as the breakdown voltage. At such a voltage, all the test structures reached the breakdown regime. Since the simulation results are not quantitatively comparable with the measurements, the breakdown voltage was extracted when the leakage current reaches 10 (arb. unit), where the onset of the breakdown occurred.

| **Label** | $V_{BD,meas}$ **(V)** | $V_{BD,sim}$ **(V)** |
|---|---|---|
| A | $-175 \pm 4$ | $-188$ |
| B | $-279 \pm 5$ | $-344$ |
| C | $-424 \pm 13$ | $-572$ |
| D | $-180 \pm 4$ | $-235$ |
| F | $-569 \pm 7$ | $-672$ |

lowest breakdown voltages among all the test structures. The measured data indicate almost identical breakdown voltages for structures A and D, suggesting that the presence of a grounded n-ring and the incorporation of deep n-wells for the n-ring and pixels have minimal impact on the breakdown performance. However, the simulations showed that the breakdown voltage for Structure D, which included a deep n-well, was approximately 50 V higher than that for Structure A. The use of n+p guard rings resulted in an increase of about 90 V in breakdown voltage when comparing Structures B and D.

Significantly higher breakdown voltages were observed for structures employing a 5-guard ring design, specifically Structures C and F. The removal of the innermost floating guard ring in Structure B led to an improvement of about 160 V in the measurements and approximately 240 V in the simulation compared with Structure C. Further removal of the overhang at the guard rings in Structure C resulted in an additional 145 V improvement in the measurements and approximately 300 V in the simulation, establishing Structure F as having the highest breakdown voltage among the tested configurations. These observations are summarised in Table 5.4 and organised into four control groups, which are used to extract the beneficial design parameters for achieving higher breakdown voltages. A qualitative comparison revealed that the simulation results generally replicated the relationship of the breakdown voltages between each structure, despite a discrepancy between Structures A and D. The influence of the deep n-well observed in the simulations was less significant compared to the other control groups.

Structure E, equipped with a field-plate between pixels, was evaluated separately. Fixed voltages were applied to the polysilicon field-plate, $V_{poly}$, at settings of $0, -50, -100, -150$V. The extracted breakdown voltages are summarised in Table 5.5. The IV curves for samples S1 and S4 are depicted in Figure 5.14, and the simulated results were presented in Figure 5.15. For each sample, the

Table 5.4: Comparison between test structures with grounded n-ring.

| **Control Group** | **Compared Parameter** | **Condition for higher breakdown voltage** |
|---|---|---|
| A & D | Deep n-well | Meas.: similar (–); sim.: deep n-well (D) |
| B & C | size of GR1 gap | Larger spacing between n-ring and GR1 (C) |
| B & D | N-implant at the guard rings | With n-implant at the guard rings (B) |
| C & F | polysilicon overhang | Without polysilicon overhang structure (F) |

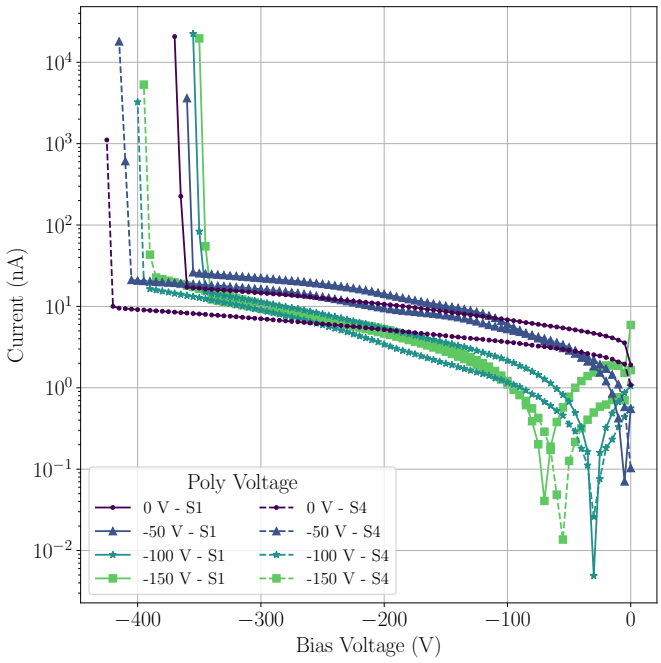



Figure 5.14: IV-curve for structure E with grounded n-ring.

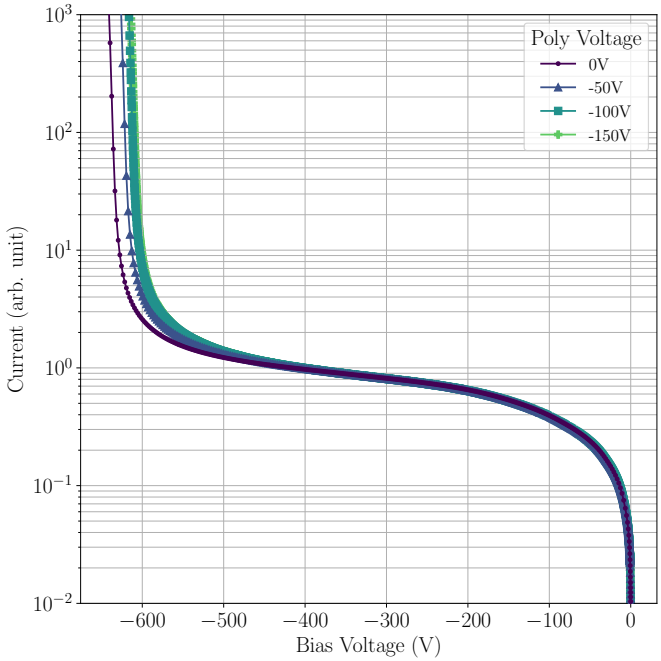



Figure 5.15: Simulated IV curves of test structures E with grounded n-ring.

Table 5.5: Simulated breakdown voltages of test structures with grounded n-ring. The values were extracted in the same manner as for Table 5.3.

| Label | $V_{poly}$ (V) | $V_{BD,meas}$ (V) | $V_{BD,sim}$ (V) |
|---|---|---|---|
| | 0 | $-395 \pm 30$ | $-628$ |
| | $-50$ | $-385 \pm 25$ | $-613$ |
| E | $-100$ | $-373 \pm 23$ | $-604$ |
| | $-150$ | $-365 \pm 21$ | $-601$ |

magnitude of $V_{bias}$ was reduced by several volts when an additional $-50$ V was applied to the field-plate. Variations between the samples were identified, with the results for sample S4 showing a shift in $|V_{BD}|$ by approximately 50 V. This discrepancy could be attributed to process variations during manufacturing, as the relationship between $V_{poly}$ and $V_{BD}$ was consistent across both samples in terms of leakage current levels and behaviour. Since structures E and C shared identical guard ring structures, the measured breakdown voltages for both test structures were approximately $-400$ V. The simulations qualitatively reproduced the reduction in breakdown voltage with each incremental increase of $|V_{poly}|$ by 50 V, and reflected a similar breakdown voltage as that observed for structure C.

### 5.3.2 Floating N-ring

The measured IV curves of test structures A, B, C, D, and F, each equipped with a floating n-ring, are depicted in Figure 5.16. Similar to observations in section 5.3.1, variations among the IV curves for the floating n-ring scenario were noted. The leakage current of Structure F on samples S3 and S7 exhibited a rapid increase for a bias voltage beyond $-100$ V, akin to the findings in Figure 5.12. A low breakdown voltage was observed for Structure D on sample S2, which was approximately 55 V lower than the other two samples. This was confirmed to be due to an unintended short circuit between the n-ring and the n-wells in the pixel matrix. Consequently, this data was excluded from further analysis.

For Structure F on sample S1, a breakdown voltage approximately 30 V lower was recorded, with no errors identified. This result closely mirrored the IV curve for the same structure and sample in Figure 5.12, suggesting that grounding the n-ring has little impact on the breakdown performance, which does not agree with the other samples. This outcome, differing from other structures and samples, implies that the n-ring implant might be disconnected from the ground potential due to manufacturing errors during sensor preparation. Despite this, the breakdown voltage for "F" on sample S1 remained similar to that of the other samples, indicating the deviation likely originated from production variations. The data for Structure D on sample S1, which still displayed the exponential part of the current increase, was also omitted from the analysis.

As summarised in Table 5.6, the breakdown performance of structures with a floating n-ring was shown to have a similar relationship to those with a grounded n-ring. A comparison is given in Table 5.7. Despite discrepancies between measurements and simulations, the simulated breakdown voltages of different guard ring structures still reproduced the relationships observed in the measurements (Table 5.6 and Figure 5.17). Structure A, which used the standard n-well for the n-ring and pixels, and 6 p-well floating guard rings, had the lowest breakdown voltage. Employing the same guard rings, Structure D had a breakdown voltage higher than A but lower than Structure B, which was equipped with n+p type floating guard rings.

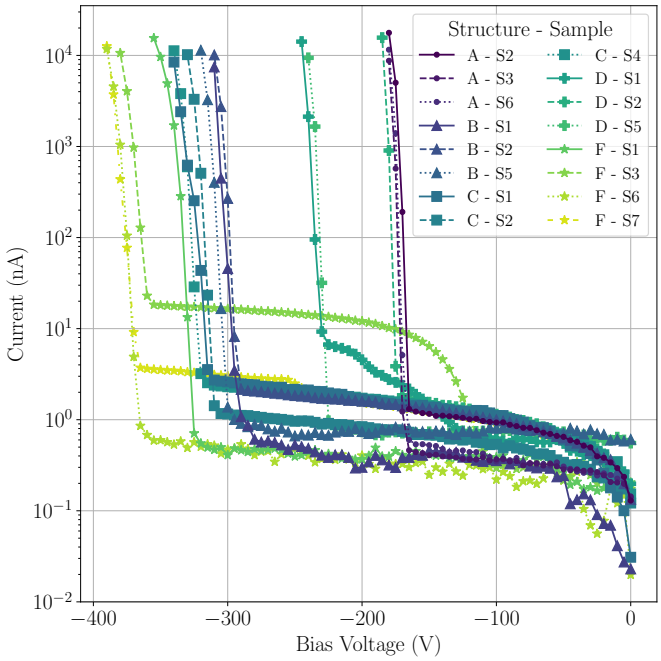



Figure 5.16: IV-curve for structure A, B, C, D, and F, with floating n-ring. The markers indicates the test structures, and the samples are distinguished by the line style.

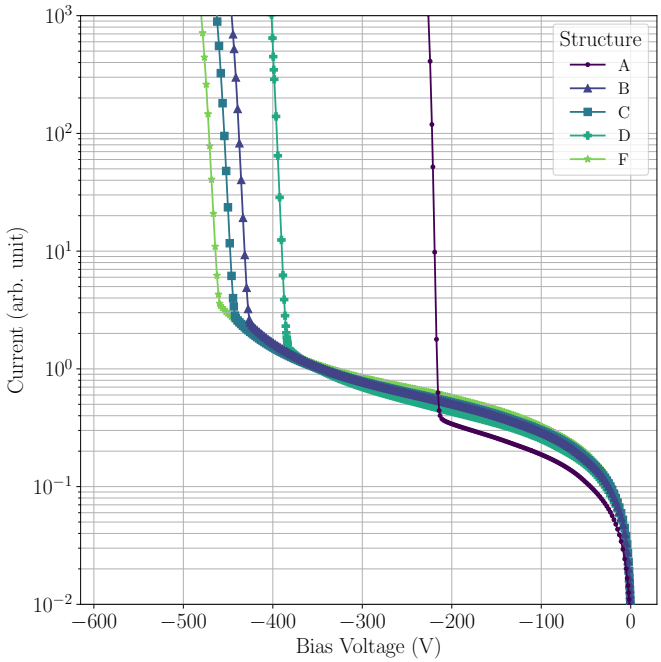



Figure 5.17: Simulated IV curves of test structures A, B, C, D, and F with floating n-ring.

The difference in breakdown voltage between A and D was more pronounced in the floating n-ring scenario (as compared in Table 5.3) in both measurements and simulations. This suggested that the deep n-well in the floating n-ring scenario had a stronger influence on improving the breakdown performance compared to grounding the n-ring. Comparing the $V_{BD}$ of D for both n-ring scenarios in measurements and simulations, using a floating n-ring revealed an increase in breakdown voltage by over 60 V. It was noted that the increase in $V_{BD}$ in simulations was larger than that observed in the measurements. This was likely due to the use of a dummy radiation damage model, since the test structures were not designed for determining the property of Si-$SiO_2$ interface.

A higher breakdown voltage was also observed for Structure B. However, this difference was smaller than the change observed in Structure D, resulting in a closer $V_{BD}$ between Structures B and D. Conversely, a clear reduction in $V_{BD}$ was found for Structures C and F, which both employed a 5-ring structure with n+p type implants. This reduction led to a smaller variance in the $V_{BD}$ across Structures B, C, D, and F.

Similar as in the previous section, the field-plate in structure E with a floating n-ring was applied with $V_{poly} = 0, -50, -100, -150$V. The measured IV curves for the two samples are depicted in Figure 5.18, the simulation results are shown in Figure 5.19, and the extracted breakdown voltages are listed in Table 5.8. In the floating n-ring scenario, $V_{BD}$ was more strongly influenced by $V_{poly}$ at the polysilicon field-plate. For $V_{poly}$ ranging from 0 V to −100 V, it was found that $\Delta|V_{poly}| = a \cdot \delta|V_{BD}|$, with the constant $a$. An $a \approx 1$ was observed for the experimental data, while an $a \approx 0.8$ was calculated from the simulation results. This trend halted when $V_{poly} = -150$ V, where $V_{BD}$ dropped to approximately −200 V in measurements and −483 V in simulations, indicating an early breakdown with such a voltage setting. The deviation between measured samples remained approximately 50 V in the breakdown voltage, suggesting that the discrepancy likely resulted from process variations in

Table 5.6: Breakdown voltages of the test structures A, B, C, D, and F with floating n-ring. $V_{BD,meas}$ represents the breakdown voltage obtained from measurements, and $V_{BD,sim}$ indicates the simulated breakdown voltage. The column "Compare" represents the change of the breakdown voltage with respect to the grounded n-ring scenario (Table 5.3), with "∼": similar; "↑": increased; "↓": decreased.

| **Label** | **$V_{BD,meas}$ (V)** | **$V_{BD,sim}$ (V)** | **Compare** |
|---|---|---|---|
| A | −174 ± 3 | −221 | ∼ |
| B | −308 ± 5 | −409 | ↑ |
| C | −329 ± 5 | −429 | ↓ |
| D | −235 ± 4 | −374 | ↑ |
| F | −367 ± 18 | −462 | ↓ |

Table 5.7: Comparison between structures with floating n-ring.

| **Control Group** | **Compared Parameter** | **Condition for higher breakdown voltage** |
|---|---|---|
| A & D | Deep implants | Deep implants at the pixels and n-ring (D) |
| B & C | Size of GR1 gap | Larger spacing between n-ring and GR1 (C) |
| B & D | N-implant at the guard rings | With n-implant at the guard rings (B) |
| C & F | polysilicon overhang | Without polysilicon overhang structure (F) |

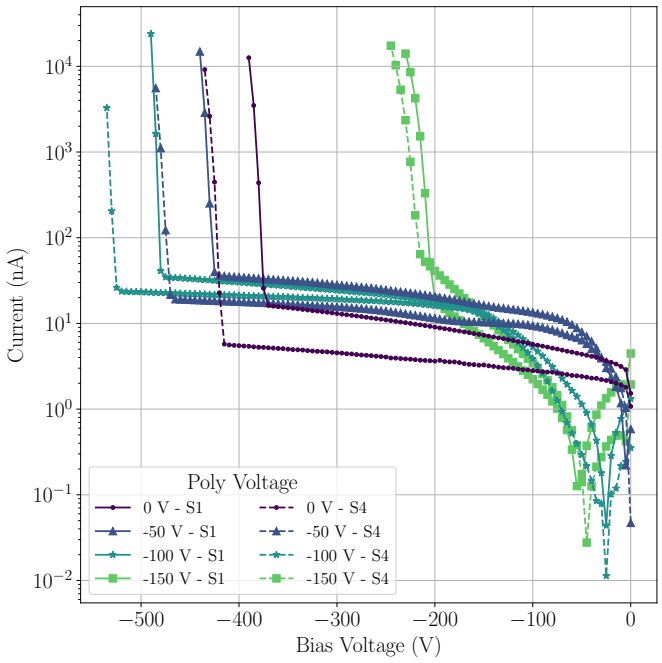



Figure 5.18: IV-curve for structure E, with floating n-ring.

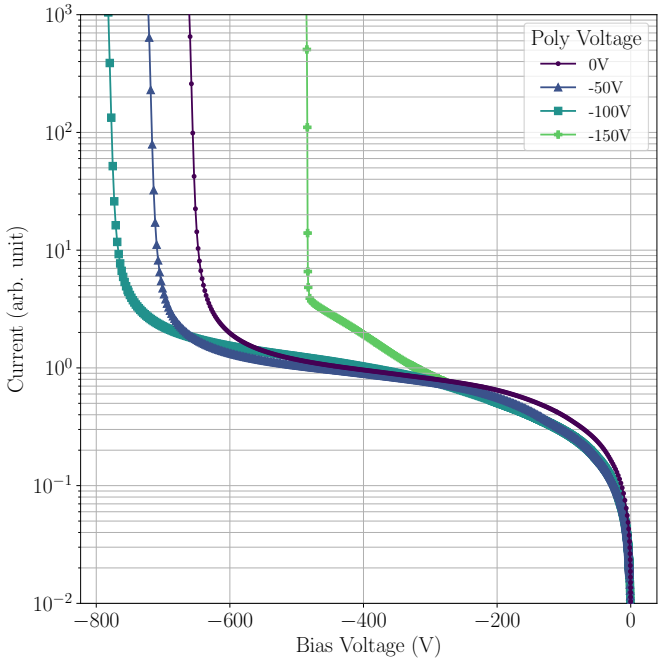



Figure 5.19: Simulated IV curves of test structures E with floating n-ring.

Table 5.8: Simulated breakdown voltages of test structures with floating n-ring.

| Label | $V_{poly}$ (V) | $V_{BD,meas}$ (V) | $V_{BD,sim}$ (V) |
|---|---|---|---|
| | 0 | $-400 \pm 25$ | $-647$ |
| | $-50$ | $-450 \pm 25$ | $-709$ |
| E | $-100$ | $-505 \pm 25$ | $-767$ |
| | $-150$ | $-208 \pm 6$ | $-483$ |

the manufacturing.

## 5.4 Influence of the Guard Ring Designs on the Breakdown Performances

Both the measurements and simulations revealed a relationship between the breakdown voltage and the guard ring design of silicon pixel sensors. To understand this relationship, further discussion is required on when and where the onset of breakdown occurs in a sensor and why it depends on the design.

The junction breakdown is closely related to the electric field within the sensor, making the maximum electric field strength a critical parameter for evaluation. However, the electrical measurement techniques used in this work do not support visualisation of the electric field distribution in the guard ring region of pixel sensors. On the measurement side, the potential distribution, which shows the electrostatic potential at each floating guard ring, provides indirect information about the field strengths. This potential distribution is obtained by probing the electrostatic potential at each floating guard ring/implant while ramping the bias voltage up to $-200$ V. Given the geometry of the implants, the electric field between each implant can be roughly estimated.

A more effective method to investigate the factors responsible for sensor breakdown is through TCAD simulation, which can illustrate the effects inside the sensor using various physical models. As demonstrated in the previous section, simulations are capable of qualitatively predicting the breakdown performance of test structures. The simulation results of the potential and electric field distribution within the same simulation domain are used for discussions in this section.

This section begins with the scenario of the grounded n-ring, as it is the designed operational setting. Simulations proceed to visualise the physical effects within the silicon and provide explanations for the findings from the previous section. Subsequently, the changes introduced by the floating n-ring scenario are discussed. Finally, the effects brought about by the voltages at the field-plate in Structure E are investigated in detail.

### 5.4.1 Grounded N-ring

The potential distribution in this scenario is visualised through simulation, as shown in Figure 5.20 (a). Near the silicon surface, the potential decreases from the n-wells towards the p-stop in the inter-pixel area (or between pixel n-well and n-ring) and from the n-ring towards the edge region (Figure 5.5). It is notable that the steepest potential gradient occurs within GR3 at a bias voltage of $-200$ V. From GR3 to the structure's edge, the potential remains close to the negative bias potential.

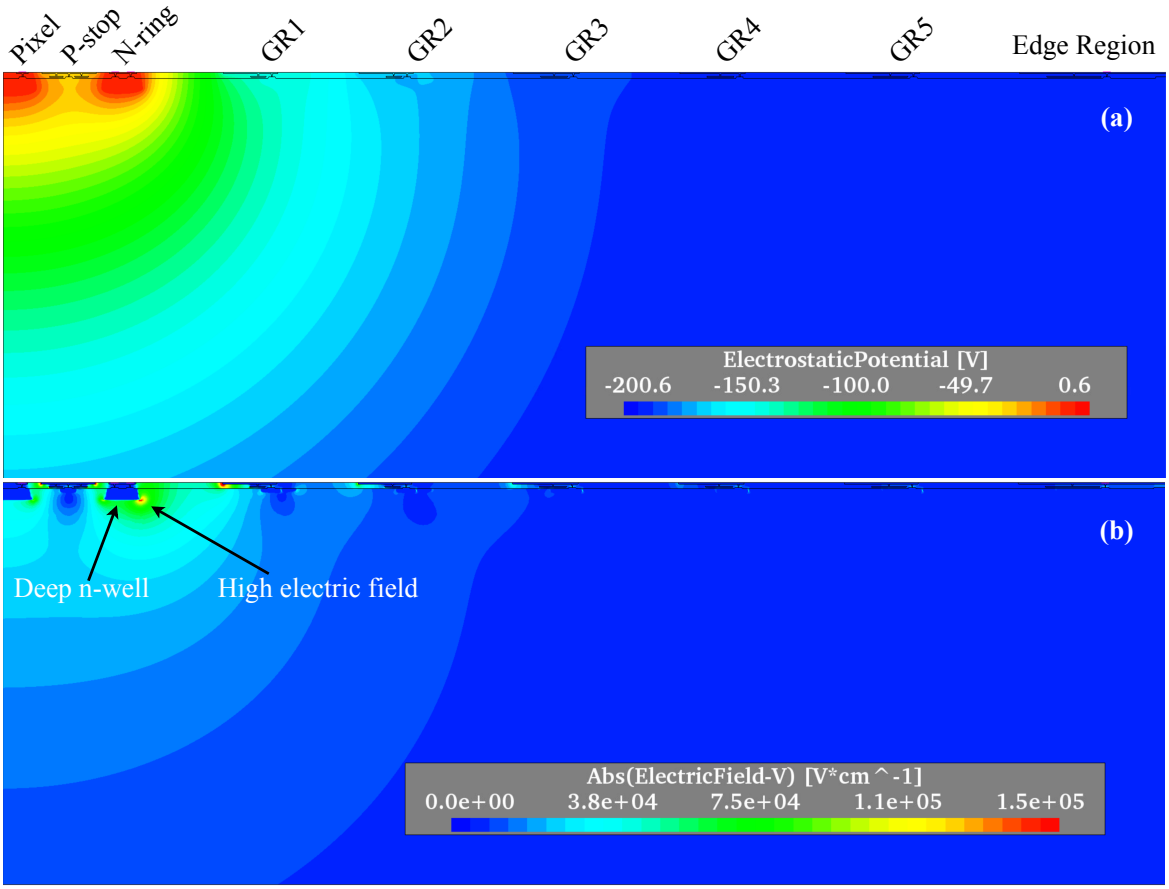



Figure 5.20: Potential/electric field distribution of structure C with grounded n-ring, and a bias voltage of −200 V. The upper part of the simulated structure is presented, and the colour code represents the value of the corresponding physical parameter, as indicated by the scale. (a): potential distribution; (b) electric field strength.

This results in a corresponding effect on the electric field strength (Figure 5.20 (b)), where a very small electric field appears outside the GR3 region. A high electric field is present between the n-ring and GR1, which is the first floating implant outside the ground potential, with the overall highest electric field observed at the lower edge of the n-ring implant. Since the implants of the pixels and rings have higher doping concentrations than the bulk, the electric field inside these implants is minimal. For example, the deep n-well of the n-ring is identifiable by the shape of the low field area highlighted in the figure. This is because the wells are mostly not depleted, since they have a higher doping concentration than the bulk.

The diagram in Figure 5.21 (a) illustrates the voltage distribution of Structures C and F from samples S4, S5, and S6. The voltages were obtained by probing each implant and are presented according to their positions in the guard ring region. The lateral position and the width of the plateaus indicate the position and size of the corresponding implants. The lines between the plateaus, sketched according to linear interpolations, do not hold physical significance but merely visualise the potential changes across the implants. As identified in the simulations, the steepest gradient of the potential

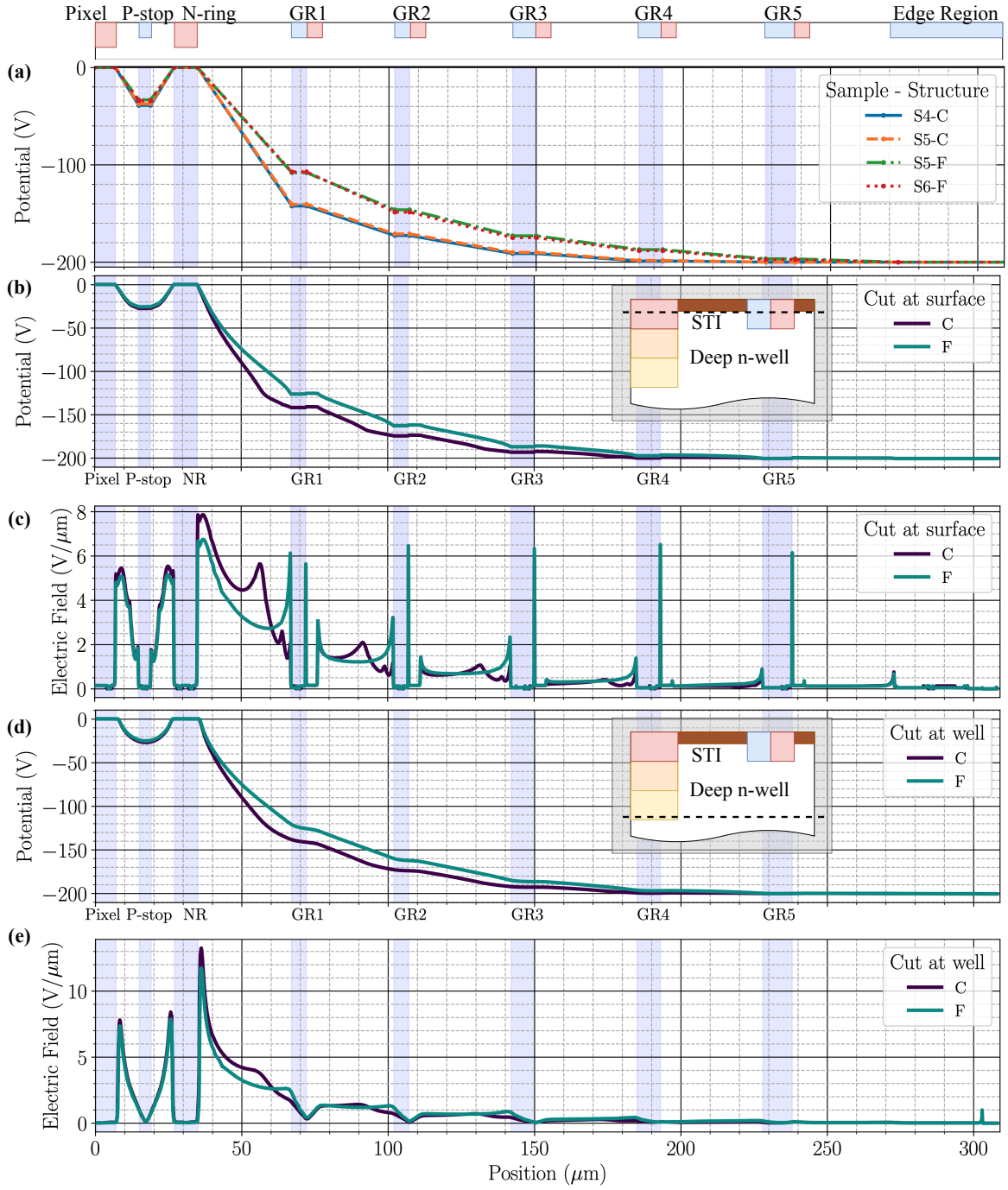



Figure 5.21: Potential/electric field distribution of structure C and F with grounded n-ring. The position of the implants are highlighted by the light blue pillars and the uppermost panel. (a): voltage probing, the plateaus represents the implants with a constant voltage, the lines in between are the linear interpolations to guide the eye. Simulation results are presented in (b)-(e). (b)/(c): the potential/electric field distribution at the surface of a sensor, the cutline is shown in the panel of (b). (d)/(e): the potential/electric field distribution at the deep n-well, the cutline is sketched in the panel of (d).

was located up to GR3, and the largest potential drop occurred between the n-ring and GR1 for both structures. Despite having a higher breakdown voltage (Table 5.3), the potentials at the floating guard rings in Structure F exhibited higher values than those in Structure C, resulting in a smaller voltage difference between the n-ring and GR1.

To compare the simulation results with the measurements, the potential distribution along a horizontal line was obtained by extracting the potential values from Figure 5.20 (a) along a horizontal cutline at the surface of the structure. The simulated potential distribution is depicted in Figure 5.21 (b), where the cutline is placed immediately beneath the STI (as seen in the panel of Figure 5.21 (b)). Comparing both diagrams, the simulation reproduces the potential gradient, including the largest potential drop between the n-ring and "GR1". Although there is an approximate 10 V discrepancy in comparison with the measurements, the relationship between the structures is clearly visible in the simulated potential distribution.

The electric field distribution with respect to the cutline is depicted in Figure 5.21 (c). The effect of the overhang at the guard ring is now identifiable from a different perspective, which will be further discussed in the ensuing part of this section. From the potential distribution, it can be deduced that the high electric field for both structures is located at the (outer) edge of the n-ring. This suggests that the impact ionisation, which triggers the junction breakdown, occurs at the n-ring in the grounded n-ring scenario. This behaviour of the potential and electric field distribution is also retained after moving the cutline to the lower edge of the deep n-well of the n-ring (Figures 5.21 (d) and (e)). Being further away from the sensor surface, the potential distribution in the floating guard ring region reveals a smoother curve, and the effect from the overhang is less significant in the electric field. By comparing the highest electric field of both sensors, it can be identified that Structure F has a lower field strength at the same bias voltage, which supports the observed better breakdown performance.

#### Location of the Junction Breakdown

Due to the significant potential drop from the n-ring to GR1, and the high electric field at the outer edge of the n-ring, the onset of breakdown is most likely to occur at the n-ring, where electrons undergo impact ionisation. Using TCAD simulations, the potential and electric field can be visualised at various bias voltages during voltage ramping, providing insight into how these physical quantities change following the onset of breakdown. Figure 5.22 depicts the potential and electric field distribution of Structure C at bias voltages from 0 V to −600 V in −100 V steps, extracted from the horizontal cutline at the deep n-well. The increasing $|V_{\text{bias}}|$ results in an overall reduction of the potential in the floating guard ring region and at the p-stop (see Figure 5.22 (a)). This leads to an almost linear increase in the potential difference between the n-ring and GR1, already the largest potential drop across the sensor. The electric field distribution (Figure 5.22 (b)) shows that the electric field becomes three times larger when $|V_{\text{bias}}|$ is increased threefold (e.g., compare cases at $V_{\text{bias}} = -200$ V and $V_{\text{bias}} = -600$ V). According to simulated breakdown voltages in Table 5.3, the junction breakdown has already occurred in Structure C at $V_{\text{bias}} = -600$ V. The electric field around the p-stop is lower than the maximum value, indicating that breakdown is unlikely to occur there.

A more intuitive perspective to examine the transition during breakdown is to visualise the charge carrier current density. Figures 5.23 and 5.24 show the current density maps for electrons and holes in Structure C, respectively. The greyscale indicates that a higher density of electron current generally occurs beneath the pixel matrix region (pixel, p-stop, and n-ring). At each floating guard ring, the

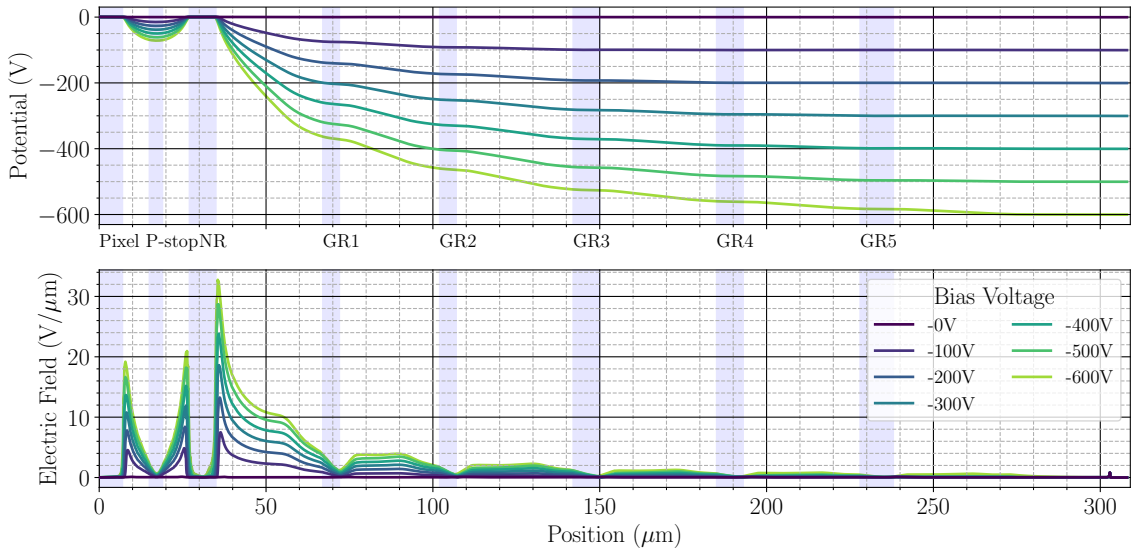



Figure 5.22: Simulated potential and electric field distribution at the bottom of the deep n-well implantation of structure C with grounded n-ring for various bias voltages.

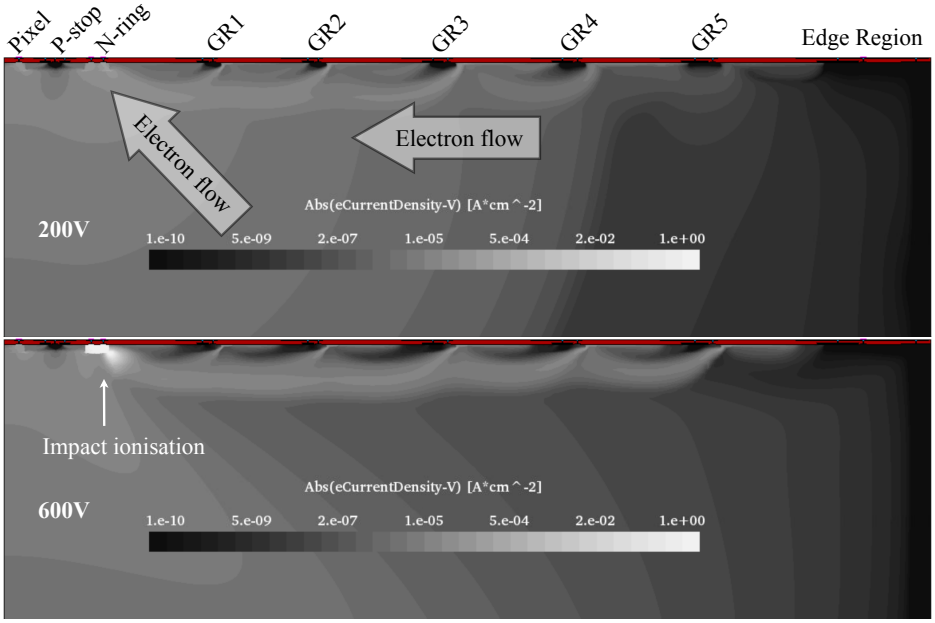



Figure 5.23: Electron current density map of the structure C with grounded n-ring at $V_{\text{bias}} = -200$ volt and $-600$ V. The magnitude of the electron current density is indicated by the greyscale. The general direction of the current flow is indicated by the arrows, and the details follows the potential distribution.

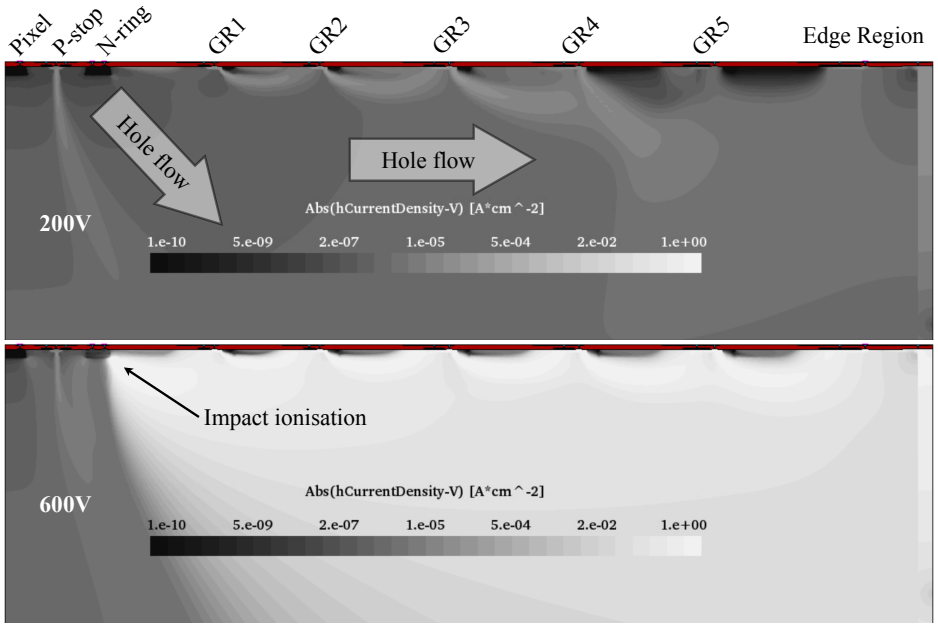



Figure 5.24: Hole current density map of the structure C with grounded n-ring at $V_{\text{bias}} = -200$ volt and $-600$ V. The magnitude of the hole current density is indicated by the greyscale. The general direction of the current flow is indicated by the arrows, and the details follows the potential distribution.

electron current flows from the n-well implant towards the n-ring, merging the electron streams from the guard ring region at the n-ring. Comparing the cases at $V_{\text{bias}} = -200$ V (before breakdown) with $V_{\text{bias}} = -600$ V (after breakdown), it is clear that the electron current density increases several orders of magnitude at and around the n-ring under breakdown conditions. Conversely, the hole current flows in the opposite direction, from the high potential at the pixels/n-ring to the edges and backside of the sensor. At $V_{\text{bias}} = -200$ V, the high current density region is typically beneath p-type implants, indicating that the hole current is flowing out of the p-type silicon into the depleted bulk. Upon reaching the breakdown regime ($V_{\text{bias}} = -600$ V), the hole current outside the n-ring dramatically increases, filling almost the entire guard ring region.

The physical picture of this transition can be deducted as follows:

1. Electrons flow from the guard ring region to the n-ring.

2. Upon reaching the breakdown voltage, the high electric field at the n-ring triggers impact ionisation of electrons.

3. The holes generated via impact ionisation flow towards the edge and the backside.

From simulating Structure C, it is concluded that the breakdown of sensors with a grounded n-ring is initiated by the p-n junction at the outer side of the grounded n-ring. This is supported by the electric field distribution and the current density map of the charge carriers. Nonetheless, the potential distribution remains a viable parameter for estimating breakdown performance, as it reflects the electric field through the potential drop in the guard ring region. The subsequent parts of this section

will discuss the test structure guard ring design and control groups [2] in more detail, as listed in Table 5.4.

### The Effect of the "n+p" Rings

To illustrate how the "n+p" ring influences the breakdown voltage, the potential and electric field distribution of Structures B and D were compared. The overall potential distribution in the guard ring region of the test structures is similar, typically decreasing from the n-ring to the chip edge, with the largest potential drop occurring in the GR1 gap. Therefore, it is sufficient to investigate the distributions only within the region of the inner guard rings, as presented in Figure 5.25. Both structures have six floating guard rings, but Structure B, with n+p rings, exhibits a higher electrostatic potential at the ring implants compared to Structure D, which has only p-well rings. Consequently, the n+p guard rings elevate the overall potential distribution, reducing the potential difference across the GR1 gap. This adjustment slightly increases the potential difference between GR1 and GR2 and the subsequent gaps, although the increase is not significant enough to impact the breakdown performance. The resulting electric field distribution highlights three distinct features introduced by using the n+p rings:

1. lowered maximum electric field

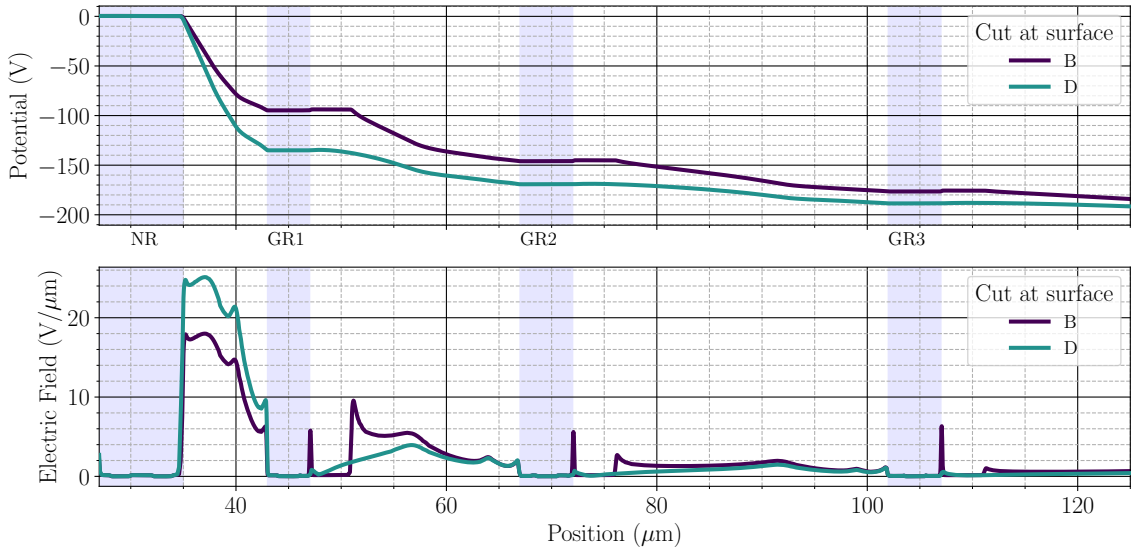



Figure 5.25: Simulated potential and electric field distribution at the surface of the Structures B and D with grounded n-ring. Distributions are obtained for $V_{\text{bias}} = -200\,\text{V}$, and presented for the region from the n-ring to the GR3, whose positions are indicated by the light blue shades. The n+p rings in Structure B delivers higher potential in the guard ring region than the pure p-well rings in Structure D.

[2] According to the measurements, the breakdown voltages of Structures A and D are similar when the n-ring is grounded. However, notable changes in the breakdown performance of both sensors are observed in scenarios where the n-ring is floating. Consequently, the discussion of this control group will be continued in the following section.

2. spikes at the intersection position of the n-well and p-well implant at each n+p rings (see Figure 5.21 the position of the n- and p-well)

3. higher electric field of the outer (right) side of the n+p rings (n-well implant)

These features are evident in the electric field map (Figure 5.26), where higher electric fields at the aforementioned locations occur. The first point can be explained by the reduced potential difference in

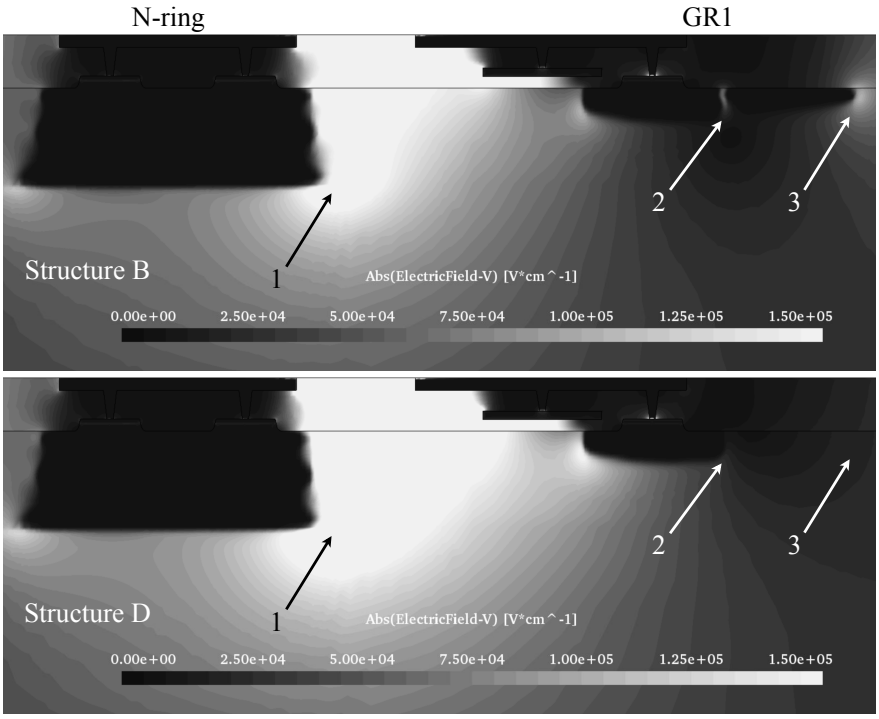



Figure 5.26: Electric field map of the region between the n-ring and GR1 in Structures B and D. The field strength is indicated by the greyscale. The arrows labelled with number "1", "2", and "3" highlight the changes of field strength introduced by the n+p rings.

the GR1 gap maintaining the same size, resulting in a smaller electric field. As depicted in Figure 5.22, the increasing $|V_{\text{bias}}|$ linearly increases the potential difference across the GR1 gap, and consequently, the electric field strength increases in the same manner. A reduced maximum field is beneficial for the breakdown performance by delaying the onset of the avalanche effect. This explains the observed results from both simulations and measurements, that the n+p ring configuration leads to a higher breakdown voltage compared to rings equipped solely with the p-well implant.

Although there is no evidence suggesting that the other two effects (points 2 and 3) are directly related to breakdown performance, investigating their origins is intriguing. Figure 5.27 sketches the potential gradient in an n+p ring after applying a bias voltage, which results in a higher potential on the left side of the p-well and a lower potential on the right side of the n-well. Given that both implants are floating and surrounded by low-doping p-type silicon, it can be analysed in a simplified manner by considering only the junctions on both sides of the n-well, namely the adjacent edge between the p-well and the n-well, and the right side of the n-well. Initially, it can be assumed that the p-well adopts a certain potential when applying the bias voltage to the sensor. As there is a potential difference on both

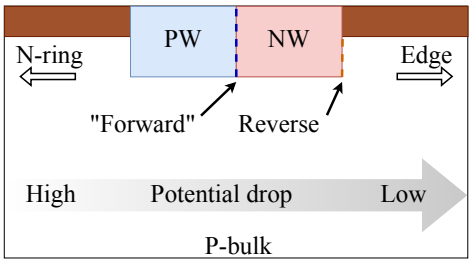



Figure 5.27: Illustration of the n+p ring and the introduced p-n junctions. The p-n junction on both sides of the n-well (NW) implant are highlighted using the dashed lines. After applying the bias voltage, the potential on the left hand side of the n+p ring is higher than the left hand side of it. Please see the text for the explanation to the labelling of junctions.

sides of the n+p ring, a potential difference should originally appear across the adjacent edge of the p- and n-well, leading to a forward bias of this p-n junction. In such a scenario, the excess holes from the p-well are injected into the n-well across the p-n junction. Since the n-well is floating, electrons can be extracted from the neutral part of the n-well and recombine with the holes coming from the p-well. Eventually, the p-n junction returns to thermal equilibrium from the "forward bias" condition. As a result, the potential at the n-well follows the potential at the p-well with a potential difference of the built-in voltage ($\lesssim 1$ V), which is also evident from the potential distribution in Figure 5.25. The spikes in the electric field between the p- and n-wells in the n+p ring result from this built-in voltage.

The p-n junction on the right-hand side of the n-well behaves more like it is in a condition of reverse bias. As the potential of the n-well is pinned to the potential at the p-well, the n-well exhibits a potential higher than the potential in the p-bulk on its right side. Since the p-bulk is connected to the chip's edge, which is at a fixed low potential, the potential difference creates depletion and consequently a higher electric field than in the structures without the n-implant.

#### The Effect of the GR1 Gap (the Number of Floating Guard Rings)

The comparison between the 5-ring and 6-ring layouts, specifically in terms of the GR1 gap size, was examined by considering Structures B and C. Both structures were equipped with n+p type floating guard rings, and a deep n-well was implemented for the pixel and the n-ring. Figure 5.28 illustrates the potential and electric field distribution around the surface of the inner guard rings at $V_{\text{bias}} = -200$ V. After the removal of the innermost guard ring in Structure B, the potential distribution showed a smoother decrease from the n-ring towards the edge. The plateau at the GR1 of Structure B transitioned to a continuous drop. However, the potential at the remaining floating guard rings changed minimally, as the curves for both structures largely overlapped.

It was evident that the same magnitude of potential drop across a larger GR1 gap (Structure C) resulted in a reduction of the maximum electric field. As depicted in Figure 5.28, the maximum electric field in Structure C was approximately half of that at the same position in Structure B. Such a reduction in the maximum electric field ensured a higher breakdown voltage.

Another aspect of the electric field distribution influenced by the larger GR1 gap was observed when examining the potential distribution along the bottom edge of the deep n-well (Figure 5.29). As previously discussed with reference to Figure 5.21, the overall maximum electric field in Structure C is located along the bottom edge of the deep n-well. However, in Structure B, the maximum electric

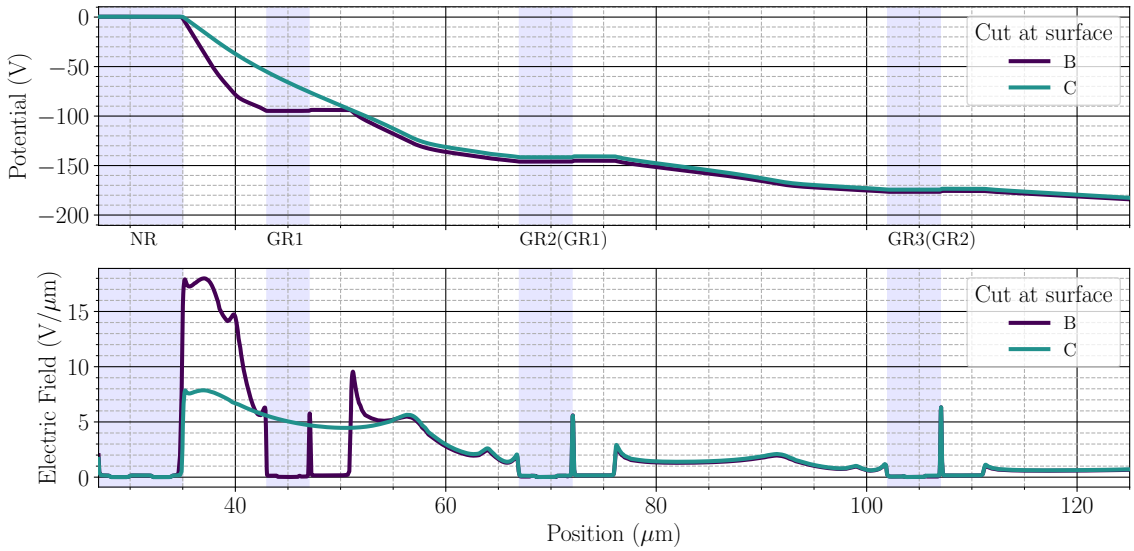



Figure 5.28: Simulated potential and electric field distribution at the surface of the Structures B and C with grounded n-ring. Distributions are obtained for $V_{\text{bias}} = -200\,\text{V}$, and presented for the region from the n-ring to the GR3, whose positions are indicated by the light blue shades. The label of the guard rings in brackets represents the guard ring number of Structure C.

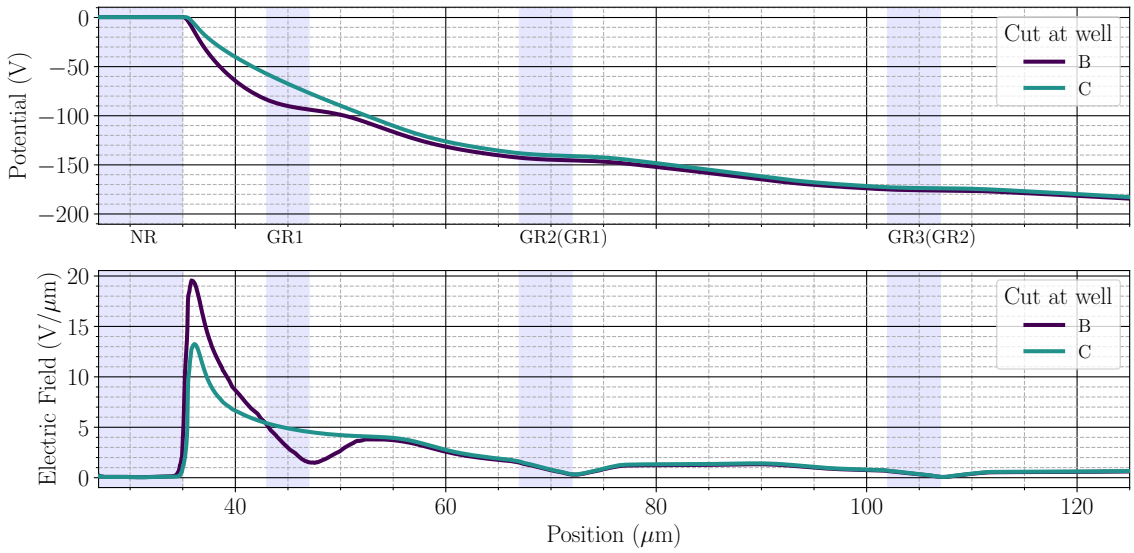



Figure 5.29: Simulated potential and electric field distribution at the bottom edge of the deep n-well in structure B and C with grounded n-ring. Distributions are obtained for $V_{\text{bias}} = -200\,\text{V}$, and presented for the region from the n-ring to the GR3, whose positions are indicated by the light blue shades. The label of the guard rings in brackets represents the guard ring number of structure C.

fields between the surface and the bottom edge of the deep n-well are very similar. This suggests that the larger GR1 gap not only relocates but also concentrates the maximum electric field towards the bottom of the deep n-well, as illustrated in Figure 5.30 (in comparison with the electric field map of Structure B in Figure 5.26). Considering the location of the maximum field in Structure C at the

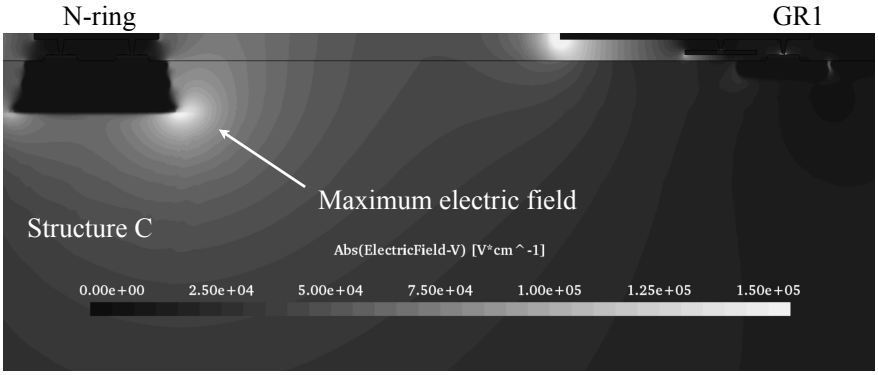



Figure 5.30: Electric field map of the region between the n-ring and GR1 in structure C. The field strength is indicated by the greyscale. The maximum field locates at the bottom right corner of the deep n-well for the n-ring.

bottom edge of the deep n-well, Structure B, with a smaller GR1 gap, still exhibits a lower breakdown voltage due to the higher electric field.

#### The Effect of the Overhang

As the overall potential and electric field distributions for Structures C (with overhang) and F (without overhang) have been presented in Figure 5.21, this part focuses on the detailed distributions between the n-ring and the innermost guard rings, as shown in Figure 5.31.

The conductive overhang structure at the floating guard rings is electrically connected to the p-well implant of the ring, ensuring that the overhang maintains the same potential as that of the guard ring. Since the potential decreases from the n-ring towards the edge, the overhang facing the n-ring (Figure 5.4) exhibits a lower potential than that at the silicon surface beneath it. This results in a suppression of the local potential near the $Si/SiO_2$ interface in the silicon, and also a reduced potential at the guard rings, as seen in the potential distribution around GR1 in Figure 5.31. Consequently, the overhang leads to a reduction in the potential at each guard ring and an increase in the potential difference between the n-ring and GR1, as identified from Figure 5.21.

The overhang also impacts the electric field distribution at the sensor surface by shifting the position of the electric field peaks, as illustrated in Figure 5.31. Consider the area between the n-ring and GR1: Structure F, without an overhang, shows two peaks in the electric field; whereas Structure C, incorporating three layers of conductive materials for the overhang, exhibits four peaks. In both structures, the first peak is located at the right edge (from the perspective of Figure 5.31) of the n-ring, and the last peak at the left edge of GR1. The electric field peaks in Structure C are labelled in Figure 5.31 with numbers “1” to “4”. It is evident that the peak at the edge of GR1 in Structure F transforms into three lower peaks at different positions in Structure C:

- peak “4”, locates at the edge of the GR1;

- peak “3”, locates approximately 2.5 µm from the GR1 edge, indicating the edge of the polysilicon layer in the overhang;
- peak “2”, locates approximately 10 µm from the GR1 edge, indicating the edge of the M1 layer in the overhang.

All three peaks have a lower field strength than the original peak in Structure F, with peaks “3” and “4”—closest to the GR1 edge—having a height approximately one-third of that in Structure F. Peak “3” is associated with the polysilicon layer in the overhang, which extends 3 µm beyond the left edge of GR1. Peak “2,” the highest of the three, correlates with the M1 layer in the overhang structure, as its width exceeds the GR1 edge by 10 µm. Since the M2 layer was not included in the simulation, its influence is not observed in the electric field distribution. Figure 5.32 illustrates the electric field map of Structures C and F with a grounded n-ring at $V_{\text{bias}} = -200$ V. In addition to noting that the maximum electric field is located at the bottom edge of the n-ring, modifications to the electric field distribution at the sensor surface due to the overhang are evident when comparing the highlighted positions (see Figure 5.31) of both structures. At the edge of the overhang layers (e.g., M1), a high electric field is generated inside the dielectrics, causing a peak in the electric field distribution at the sensor surface. The overhang structure has shown to degrade the breakdown performance of silicon pixel sensors, as observed in the test structures. However, these effects could provide a beneficial feature after the sensor sustains radiation damage at the Si-$SiO_2$ interface. This will be further discussed in section 5.5.

**Summary** After examining the potential and electric field distributions in the guard ring region with a grounded n-ring, it has been observed that sensor breakdown typically occurs at the outer edge of the

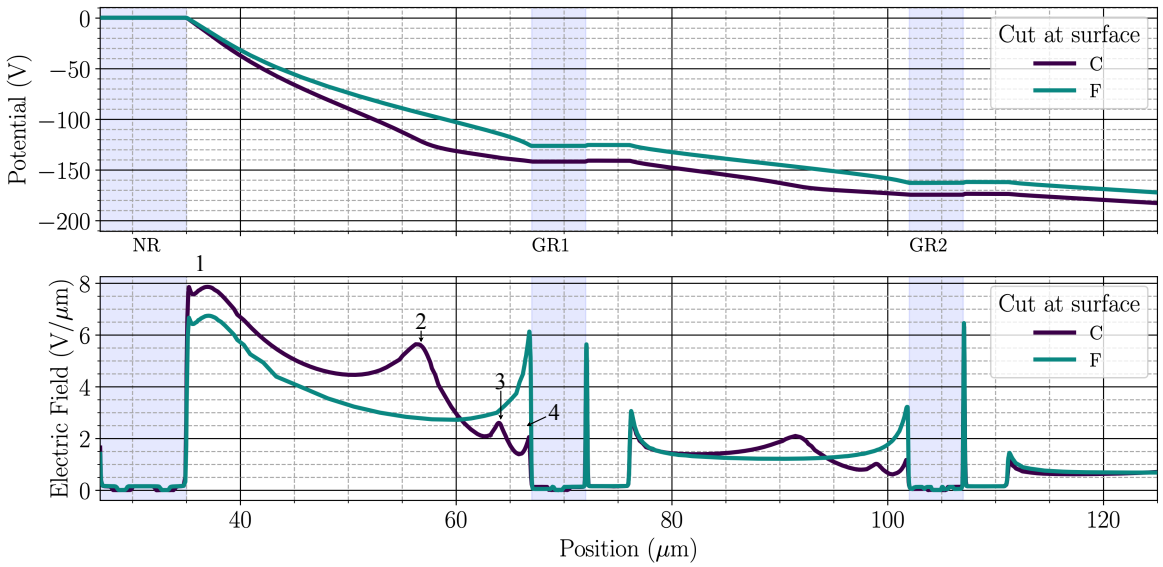



Figure 5.31: Simulated potential and electric field distribution at the bottom edge of the deep n-well in Structures C and F with grounded n-ring. Distributions are obtained for $V_{\text{bias}} = -200$ V, and presented for the region from the n-ring to the GR2, whose positions are indicated by the light blue shades. The peaks of the electric field distribution between the n-ring and the GR1 of Structure C are enumerated.

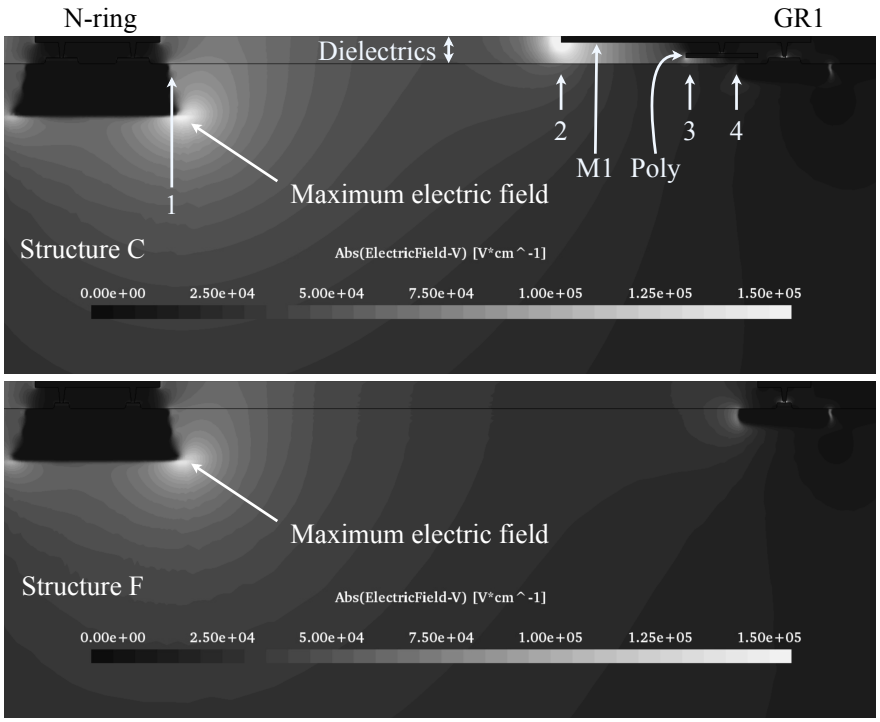



Figure 5.32: Electric field map of the region between the n-ring and GR1 in Structures C and F. The field strength is indicated by the greyscale. polysilicon (Poly) and M1 layers are fabricated inside the dielectric layer ($SiO_2$ in simulation) above the silicon. The position of the electric field peaks in structure C is highlighted and enumerated as in Figure 5.31.

n-ring, where the maximum electric field within the guard ring region is located. This high electric field stems from the fact that the greatest potential difference, within the potential drop from the n-ring (0 V) to the edge (negative potential), is found between the n-ring and the innermost floating guard ring (GR1). The potential at each floating guard ring changes almost linearly with the increasing bias voltage, thereby directly increasing the potential difference between the n-ring and GR1, as well as the electric field strength. Breakdown occurs when the maximum electric field is sufficient to initiate electron multiplication. The different breakdown performances and the guard ring designs are connected through the modification of the maximum electric field. This can be summarised into three design features which are beneficial for achieving a higher breakdown voltage:

1. *Large spacing between the n-ring and the nearest floating guard ring (GR1 gap)*
   - **Control group:** structure B & C
   - **Observation & Conclusion:**
     A large spacing results in a potential drop across a longer distance between the n-ring and the first floating guard ring. This leads to a smoother potential distribution in the region of the innermost guard rings, and consequently, a reduced maximum electric field. Therefore, a higher breakdown voltage is revealed for the guard ring design with a larger gap between the n-ring and GR1 (Structure C).
2. *N-implant at the floating guard rings ("n+p" rings)*

- **Control group:** B & D
- **Observation & Conclusion:**
  The implementation of the n-implant forming the "n+p" rings raises the potential at the floating guard rings after biasing the sensor structure. This reduces the maximum potential difference, which is the potential drop between the n-ring and GR1. As a result, the maximum electric field is lowered by such a modification. Therefore, a higher breakdown voltage is found for the guard ring design equipped with "n+p" rings (Structure B).

3. *No overhang structure at the floating guard rings*
   - **Control group:** C & F
   - **Observation & Conclusion:**
     The overhang structure has the same potential as that at the floating guard rings. After applying a bias voltage, both the local potential directly beneath the overhang structure and the potential at the floating guard rings are suppressed, compared with the design without the overhang structure. Consequently, the potential difference between the n-ring and GR1 is increased through the implementation of the overhang structure. Thus, a higher breakdown voltage is observed for the guard ring design without overhang (Structure F).

### 5.4.2 Floating N-ring

After switching from the grounded n-ring to the floating n-ring scenario, a change in the breakdown voltage was observed for most of the samples (see Table 5.6 in section 5.3). This suggests that the potential distribution in the floating n-ring scenario undergoes a change in the maximum potential difference or the maximum electric field compared to the grounded n-ring scenario for the same $V_{\text{bias}}$. Figure 5.33 displays the measured potential at the guard rings of Structures B and C with both floating and grounded n-rings at $V_{\text{bias}} = -200\,\text{V}$. The simulated potential distribution for the grounded n-ring scenario in Figure 5.28 mirrors the measured results, showing that removing the GR1 in Structure B leads to a potential drop with a gentler slope.

In the floating n-ring scenario, the p-stop and the n-ring can be considered as the innermost floating "guard rings", which now contribute to the overall potential drop from the pixel implant to the sensor edge. Consequently, the potential difference between the pixel and the p-stop is comparable to the potential drop from the n-ring to GR1 in both sensors. The n-ring exhibits a similar potential to the p-stop, and the rationale for this is as discussed in the previous section regarding the "n+p" guard rings. A secondary effect is that the potential at the original floating guard rings (GR1 to GR6) is lowered, which is more noticeable in the inner guard rings (GR1-GR3) at $V_{\text{bias}} = -200\,\text{V}$. These changes indicate that the maximum electric field is relocated to the region between the pixel and the p-stop, where impact ionisation may occur during sensor breakdown.

The simulation of the potential and electric field distribution for the inner guard ring region (from the pixel to GR2) in Structure C is depicted in Figure 5.34, facilitating a detailed comparison between two scenarios. The simulation has accurately reproduced the potential drop from the pixel to the edge, where the potential difference between the pixel and the p-stop becomes more pronounced and the potentials at the floating guard rings are lowered. The potential drop between the n-ring and GR1 remains the largest in Structure C, although the slope of this part is less steep than in the region around the pixel implant due to the narrow spacing between the pixel implant and the p-stop.

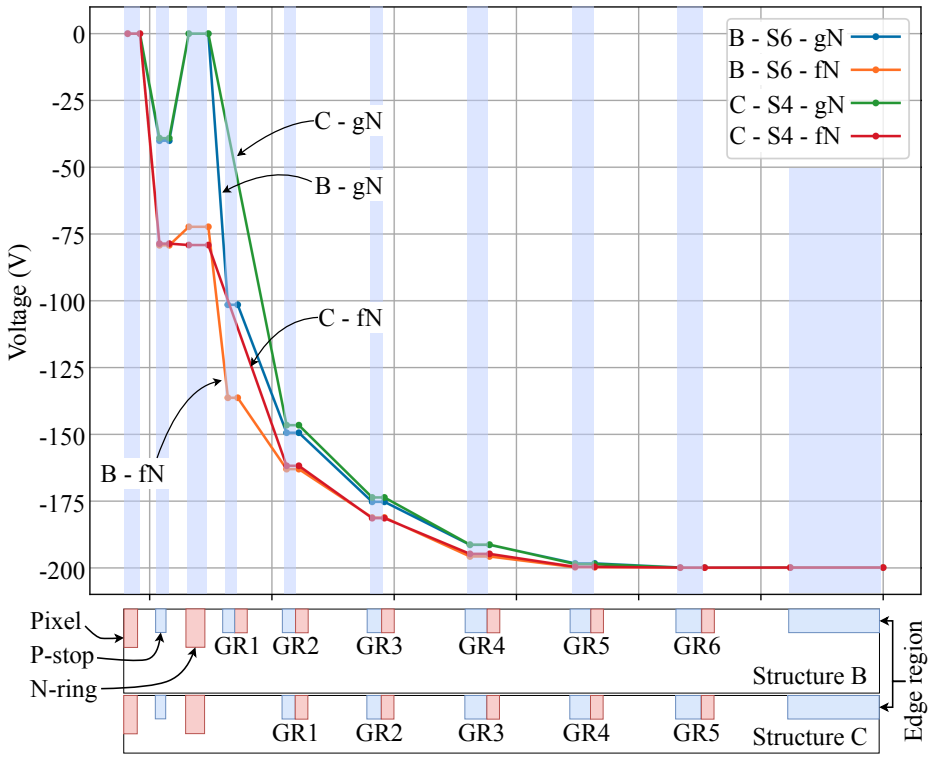



Figure 5.33: Potential at the guard rings of test structure B and C at $V_{\text{bias}} = -200\,\text{V}$. The present data are measured from sample S6 and S4 for the floating n-ring scenario "fN" and the grounded n-ring scenario "gN".

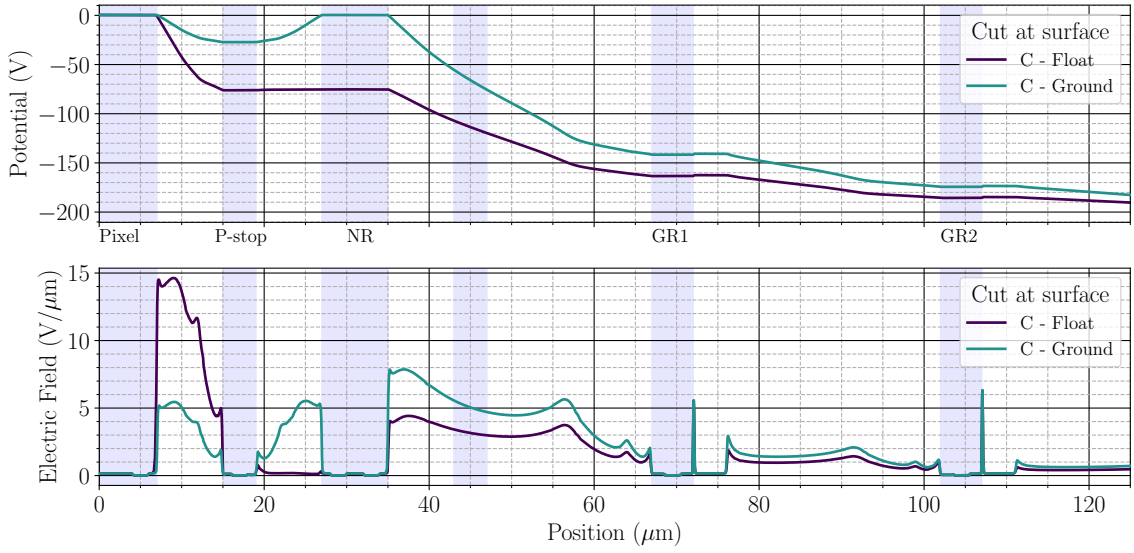



Figure 5.34: Simulated potential and electric field distribution of structure C with floating and grounded n-ring. The data shows the distributions between the pixel implant and the GR2.

Figure 5.35 illustrates the potential and electric field distribution at the surface for $V_{\text{bias}}$ ranging from 0 V to −500 V in a −100 V step. The potential at the p-stop scales approximately linearly with the increasing bias voltage before breakdown (from 0 V to −200 V), with the steepest potential drop occurring between the pixel and the p-stop. Consequently, the maximum electric field in Structure C with a floating n-ring has shifted to the edge of the pixel implant, indicating the site of impact ionisation. Based on these observations, it can be concluded that the reduction in the breakdown voltage of Structure C with a floating n-ring is initiated by the shifted and increased maximum electric field. A similar effect is observed for Structure F.

The simulation for Structure B similarly reproduces the measured potential distribution at the floating implants, as shown in Figure 5.36. Like in Structure C, the resulting electric field displays a pronounced peak in the area around the pixel implant due to the increased slope of the potential drop in this region. However, when comparing both scenarios, the highest value of the maximum electric field is still found in the grounded n-ring scenario. Thus, switching to the floating n-ring scenario for Structure B results in a lower maximum electric field and, consequently, a higher breakdown voltage. This effect is also evident in Structure D.

In the floating n-ring scenario, it is noticeable that the breakdown voltages of Structures B, C, and F range between −300 V and −400 V, showing less variation than in the grounded n-ring scenario. Similar consistency is observed in the simulation results, where the breakdown voltages for these structures lie between −400 V and −500 V. Figure 5.37 shows that at the same bias voltage, the potential distributions around the p-stop in all the structures almost overlap, with discrepancies only occurring outside the n-ring. The corresponding electric field distributions also show the maximum field strengths occurring at the same locations with similar peak values. Structure B exhibits a slightly higher electric field, resulting in the lowest breakdown voltage among these structures.

The reason for the similarity in potential, electric field, and breakdown voltages is the identical

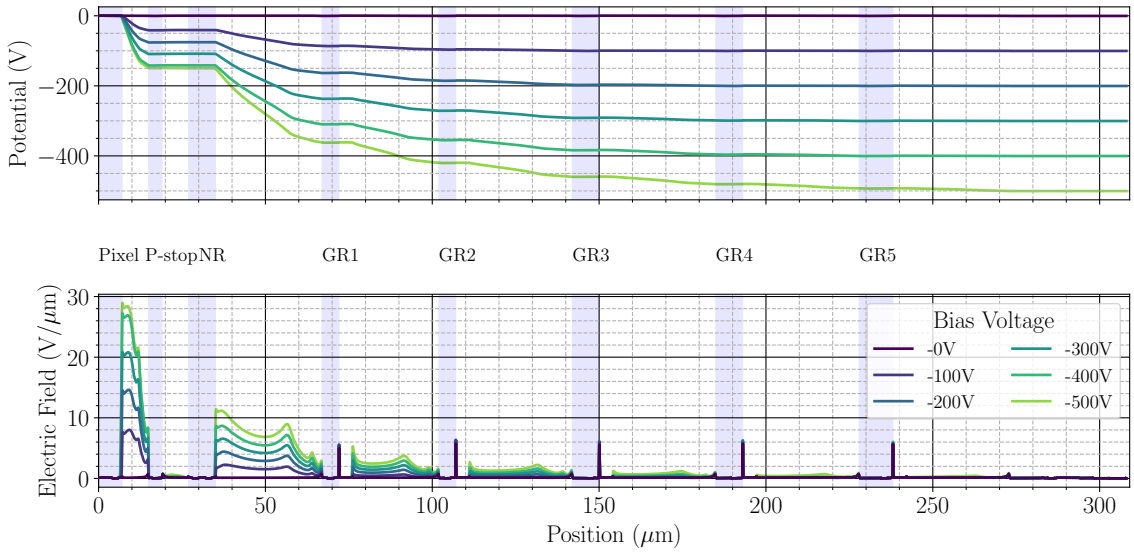



Figure 5.35: Simulated potential and electric field distribution along the cut line at the surface of structure C with floating n-ring for various bias voltages.

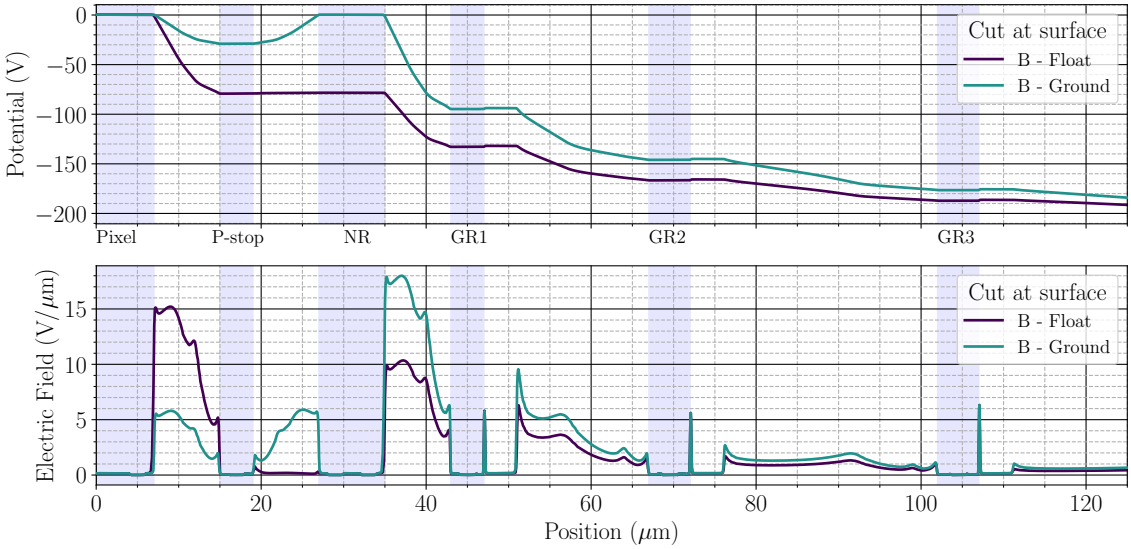



Figure 5.36: Simulated potential and electric field distribution of structure B with floating and grounded n-ring for $V_{\text{bias}} = -200\,\text{V}$. The data shows the distributions between the pixel implant and the GR3.

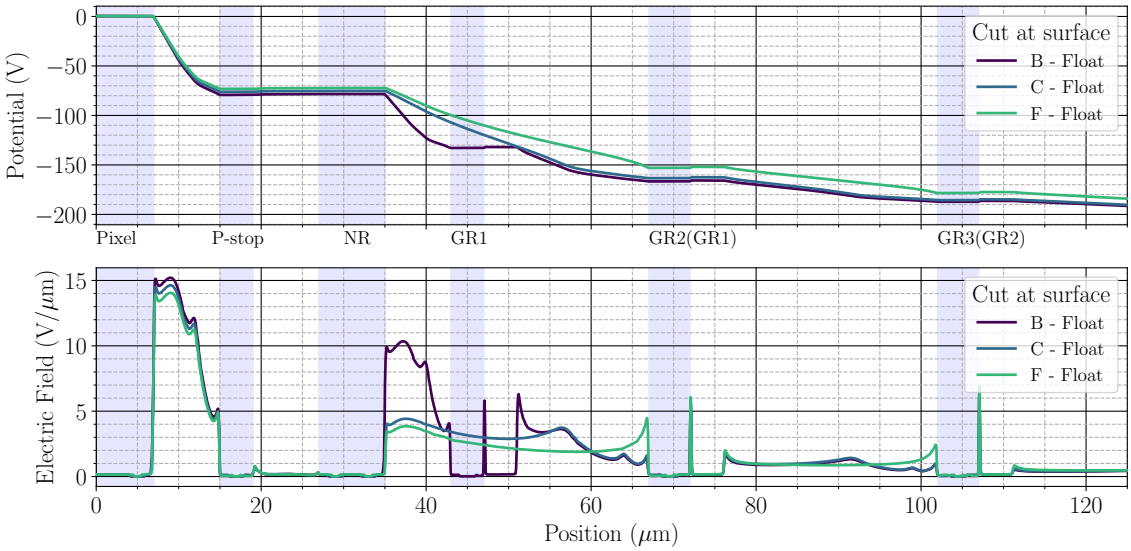



Figure 5.37: Simulated potential and electric field distribution of structure B, C, and F with floating n-ring for $V_{\text{bias}} = -200\,\text{V}$. The data shows the distributions between the pixel implant and the inner floating guard rings.

structure of the p-stop and the n-ring. Since the p-stop effectively acts as the innermost floating "guard ring," the maximum electric field is determined by the design geometry of its implant, similar to the cases discussed in the previous section for the grounded n-ring scenario, where GR1 was the determining guard ring. Therefore, with the same p-stop (and n-ring) design, the influence of the original floating guard rings on the breakdown performance becomes less significant.

An interesting effect observed is the influence of the n-ring implant on the breakdown voltage. Structures A and D differ in the implantation of the n-ring and pixel implant, where the standard n-well in A is replaced by a deep n-well in D. This alteration affects the potential distribution between the pixel and GR1 (Figure 5.38). With a deeper n-ring implant, both the p-stop and the n-ring acquire a higher electrostatic potential at the same bias voltage. Consequently, the maximum electric field in Structure D is reduced due to the smaller potential difference. As a result, Structure D exhibits a higher breakdown voltage than Structure A.

**Summary** Switching from the grounded to the floating n-ring scenario has revealed interesting effects on the breakdown performance of test structures. A significant difference between the two scenarios is the effective geometry of the floating guard rings. In the floating n-ring scenario, the p-stop and the n-ring serve as floating guard rings, and their electrostatic potentials contribute to the potential drop from the pixel implants to the sensor edge (Figure 5.6). This transition in breakdown performance is linked to changes in the maximum electric field within the guard ring regions, deduced from analyses of the simulated potential and electric field distributions. Two key conclusions have been drawn from the investigation of the floating n-ring scenarios and the comparison between the two:

1. *The first floating guard ring is the determining factor of the breakdown performance*

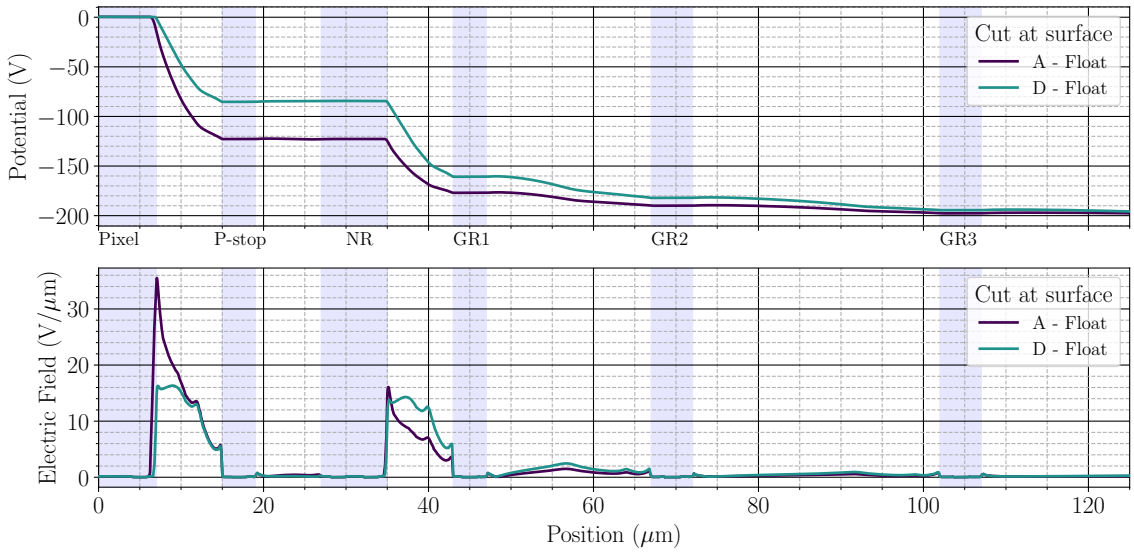



Figure 5.38: Simulated potential and electric field distribution of structure A, and D with floating n-ring for $V_{\text{bias}} = -200\,\text{V}$. The data shows the distributions between the pixel implant and the inner floating guard rings.

- **Control group:** structure B, C, and F
- **Observation & Conclusion:**
  The change in breakdown voltage is noted for most test structures when switching measurement scenarios. In the floating n-ring scenario, the potential distribution at the location of the maximum electric field (between the pixel implant and the n-ring) reveals a similar curve shape for all the structures in the control group. Thus, a similar maximum electric field is also observed. This indicates that the identical structure of the p-stop and the n-ring significantly influences the distributions, and consequently the breakdown voltage, more than the outer original guard rings.

2. *Floating deep n-well elevates the electrostatic potential*
   - **Control group:** structure A & D
   - **Observation & Conclusion:**
     As discussed previously, the "n+p" rings can elevate the potential at the floating guard rings. Similarly, the "p-stop + deep n-well" structure in the floating n-ring scenarios acts like the "n+p" ring. Investigation of this control group shows that the deep n-well can further elevate the potential of a floating implant compared to the standard n-well, thereby reducing the potential difference and electric field between implants.

Particularly in the floating n-ring scenario, the 2D simulation of the guard ring region is undoubtedly an oversimplification of reality. The p-stop, with a more complex layout than the floating guard rings, is clearly influenced by the pixel implants arranged in a matrix. However, simulating such a large-scale domain in TCAD is impractical due to potential extensive time and computing power requirements. Nonetheless, using 2D simulations of the guard ring region is already sufficient to qualitatively illustrate the influence of guard ring or, more generally, implant designs on the breakdown performance, as confirmed by various cross-comparisons between simulations and measurements.

### 5.4.3 Field-plate: Manipulating the Potential Distribution

The polysilicon field-plate in Structure E (see Figure 5.3) replaces the p-stop structure implemented in the other test structures. According to the breakdown measurements and simulations, only little difference in the breakdown voltage was observed for different field-plate voltages ($V_{\text{poly}}$), when the n-ring is grounded (Table 5.5).

Figure 5.39 presents the potential and electric field distributions at the surface of Structure E for various $V_{\text{poly}}$ settings.

Applying a negative $V_{\text{poly}}$ results in a lowered potential at the inter-pixel region (or the region between the pixel implant and the n-ring in this simulation domain), which reveals the same effect caused by the p-stop (see Figure 5.34 for Structure C). However, further lowering $V_{\text{poly}}$ didn't lower the potential beneath the field-plate, but increases the slope of the potential distribution there. Therefore, a higher electric field around the field-plate is achieved by applying a larger $|V_{\text{poly}}|$, but the electric field's maximum remains located at the right edge of the n-ring, consistent with observations in other test structures. As the designs of the floating guard-rings in Structures C and E are identical, the resulting breakdown voltages for both structures are similar for grounded n-ring scenario.

With a floating n-ring, the potential at the field-plate visibly influenced the potential distribution from the pixel implant to the GR1, as depicted in Figure 5.40. This provides a hint for the observations

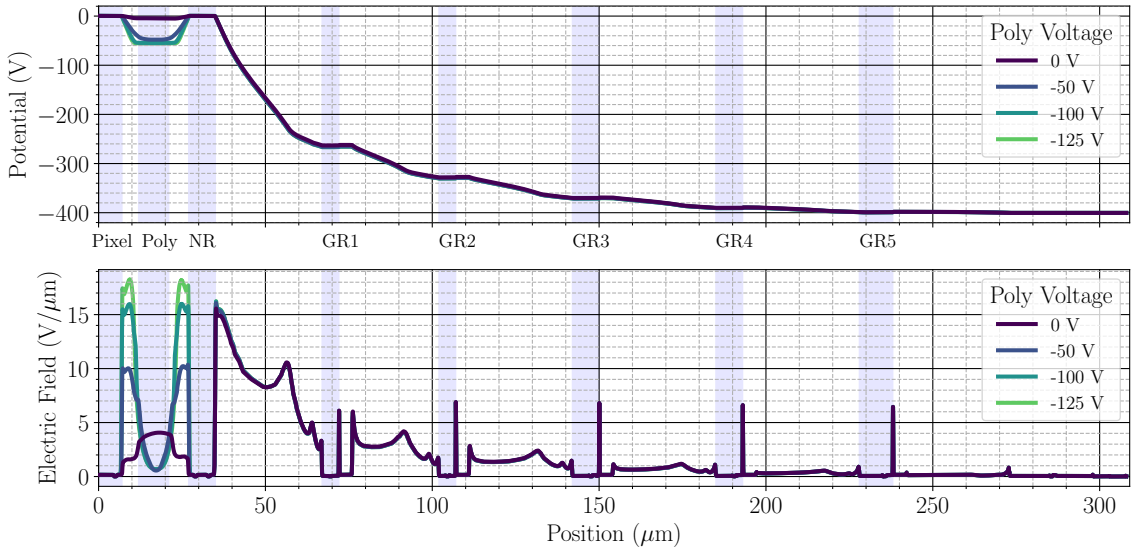



Figure 5.39: Simulated potential and electric field distribution of structure E with grounded n-ring for $V_{\text{bias}} = -400\,\text{V}$. The data shows the distributions between the pixel implant and the inner floating guard rings for various $V_{\text{poly}}$, as labelled in the figure.

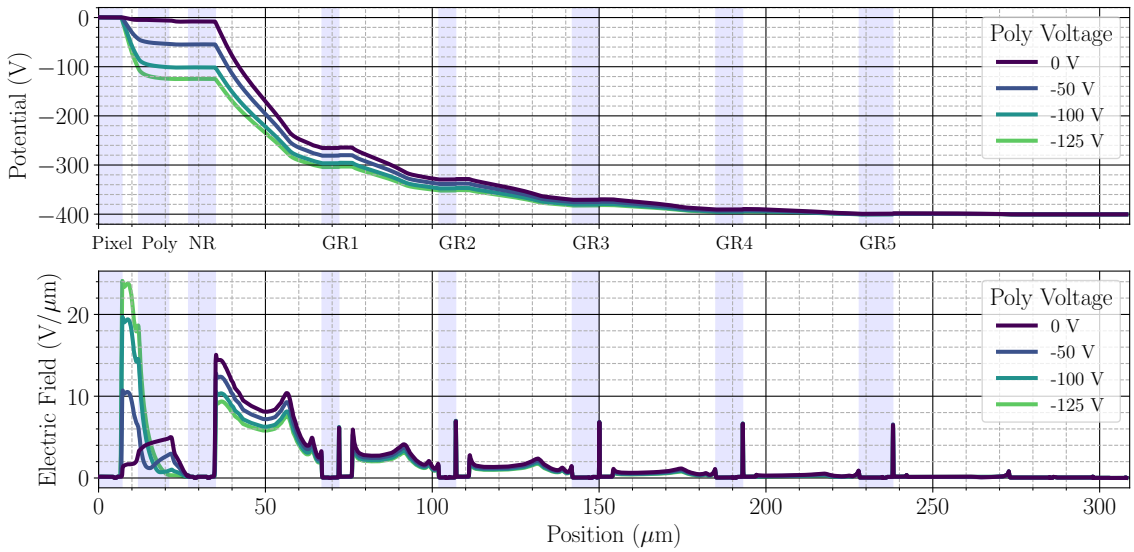



Figure 5.40: Simulated potential and electric field distribution of structure E with floating n-ring for $V_{\text{bias}} = -400\,\text{V}$. The data shows the distributions between the pixel implant and the inner floating guard rings for various $V_{\text{poly}}$, as labelled in the figure.

from the measurements and simulations, that the changes in $V_{poly}$ results in noticeable modifications to the breakdown voltage (Table 5.8). Similar to other test structures, the potential at the floating n-ring aligns with the potential of the region beneath the field-plate. With $V_{poly} = 0\,V$, the potential between the pixel and the n-ring remains nearly flat at the ground potential, positioning the maximum potential difference between the n-ring and GR1. Mirroring the similar condition as that of the grounded n-ring scenario, this voltage setting leads to a similar breakdown voltage. As $|V_{poly}|$ increases, the potential difference between the pixel and the field-plate rises, whereas it decreases between the n-ring and GR1. This alteration is reflected in the electric field distribution by changing the height of the electric field peaks. As $V_{poly}$ is ramped from 0 V to −50 V, the original maximum electric field at the edge of the n-ring decreases, while an electric field peak emerges at the edge of the pixel implant at $V_{poly} = -50\,V$, indicating a relocation of the maximum electric field. For $V_{poly} = -100\,V$, a further increase in the electric field is observed at the edge of the pixel.

It is intriguing to compare Structure C and Structure E (with $V_{poly} = -100\,V$) at a $V_{bias} = -200\,V$, particularly since the potential at the p-stop of Structure C with a floating n-ring was also approximately −100 V, as shown in Figure 5.41. The potential and electric field distributions indicate that the maximum electric field for both structures is located at the edge of the pixel implant, with Structure E exhibiting a higher electric field. Based on these distributions, one might naturally assume that Structure E, with such a $V_{poly}$, would have a lower breakdown voltage than Structure C. However, both the measurements and simulations revealed that Structure E has a breakdown voltage over 100 V higher than that of Structure C. The reason for this discrepancy becomes apparent when comparing the distributions for $V_{bias} = -500\,V$ for both structures, as depicted in Figure 5.42. At this bias voltage, the potential at the p-stop in Structure C was lowered by approximately 80 V, while little change was observed in the potential of the region beneath the field-plate in Structure E. Consequently, Structure

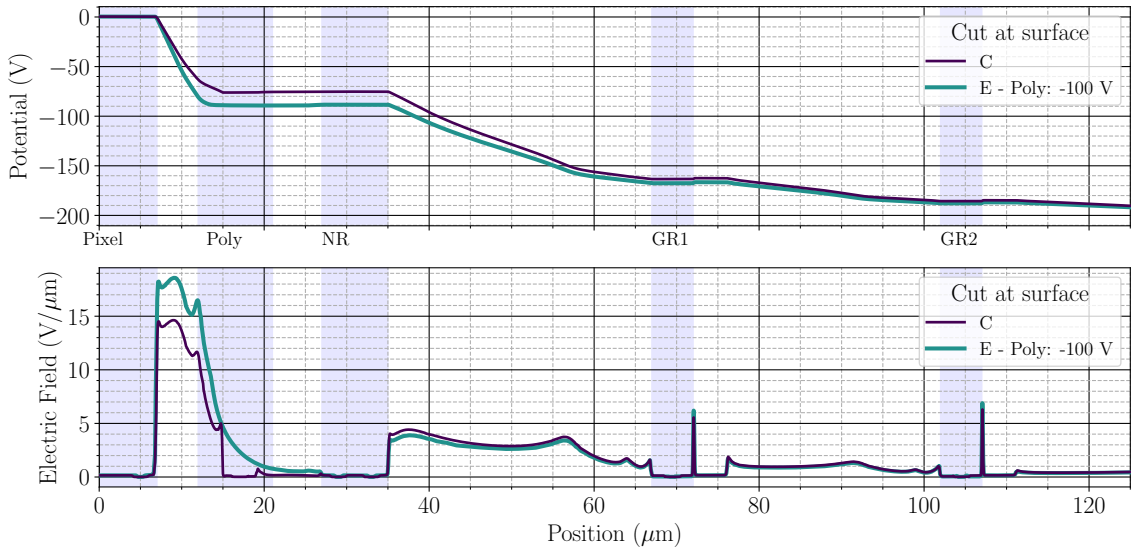



Figure 5.41: Simulated potential and electric field distribution of structure C and E with floating n-ring for $V_{bias} = -200\,V$. The data shows the distributions between the pixel implant and the inner guard rings. $V_{poly} = -100\,V$ is applied to the field-plate of structure E.

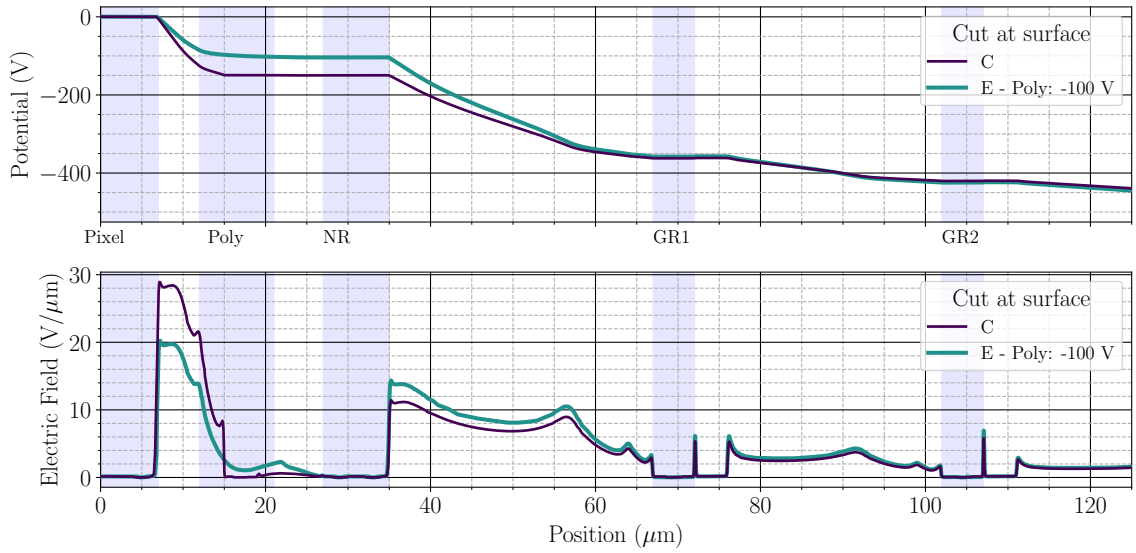



Figure 5.42: Simulated potential and electric field distribution of structure C and E with floating n-ring for $V_{\text{bias}} = -500\,\text{V}$. The data shows the distributions between the pixel implant and the inner guard rings. $V_{\text{poly}} = -100\,\text{V}$ is applied to the field-plate of structure E.

C exhibits a higher maximum electric field, leading to its worse breakdown performance.

In both the measurements and simulations, $V_{\text{poly}}$ was initially ramped to the desired value before applying the bias voltage. Figure 5.43 illustrates the potential distribution at the surface of Structure E with $V_{\text{poly}} = -100\,\text{V}$ for various $V_{\text{bias}}$ settings. During the ramping of $V_{\text{bias}}$ from 0 V to −800 V, the potential in the region beneath the field-plate gradually decreased to values around −100 V, which is the set $V_{\text{poly}}$. Only minor changes in the potential distribution were observed for $|V_{\text{bias}}| \gtrsim 300\,\text{V}$ until breakdown occurred. This demonstrates that $V_{\text{poly}}$ establishes a boundary for the potential in the region below the field-plate, thereby limiting the local potential differences and electric field to a narrow range. In this case, the electric field at the edge of the pixel implant was restricted to approximately 20 V/µm. However, the increasing bias voltage led to a higher electric field at the edge of the n-ring, whose peak value became comparable with that at the edge of the pixel for $V_{\text{bias}} = -700\,\text{V}$ and −800 V. According to the map of absolute hole current density (Figure 5.44), impact ionisation occurred at both the pixel implant and the n-ring, as indicated by the high hole current.

Up to now, applying a negative potential at the field-plate has shown benefits in increasing the sensor's breakdown voltage, due to the reshaping of the potential distribution by the field-plate. However, an early breakdown was observed at $V_{\text{poly}} = -150\,\text{V}$, where a clear degradation was recorded in both the measurements and the simulations. Given the short distance between the pixel and the field-plate, a slight increase in the potential difference can cause a significant increase in the electric field. Therefore, during the ramping of $V_{\text{bias}}$, the maximum electric field induced by $V_{\text{poly}} = -150\,\text{V}$ was already sufficiently high to trigger impact ionisation at the pixel implant, before the electric field at the edge of the n-ring reaches the threshold for breakdown.

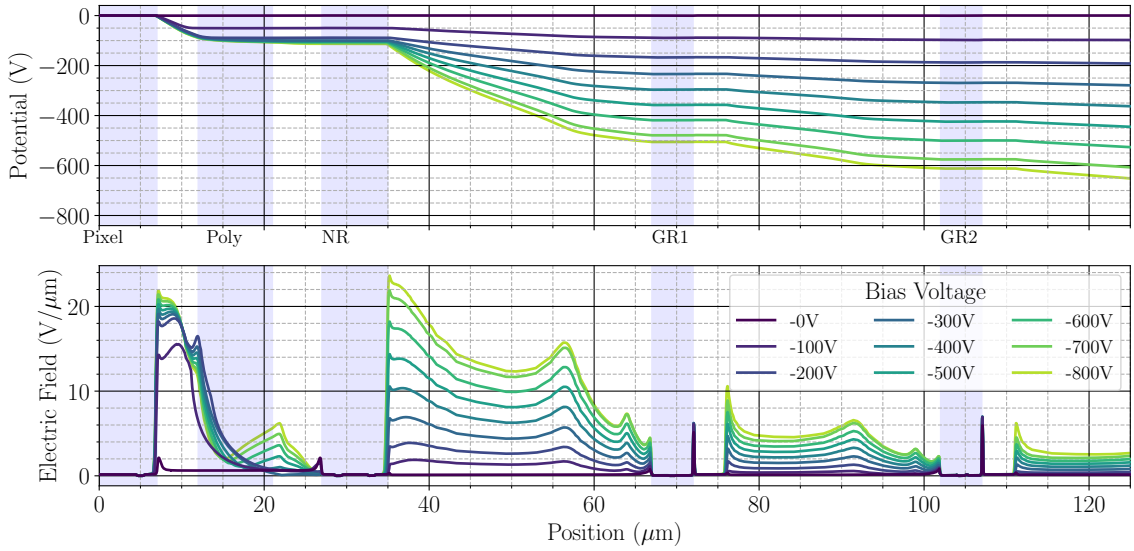



Figure 5.43: Simulated potential and electric field distribution of structure E with floating n-ring for $V_{poly} = -100\,V$. The data shows the distributions between the pixel implant and the inner guard rings for various $V_{bias}$, as labelled in the diagrams.

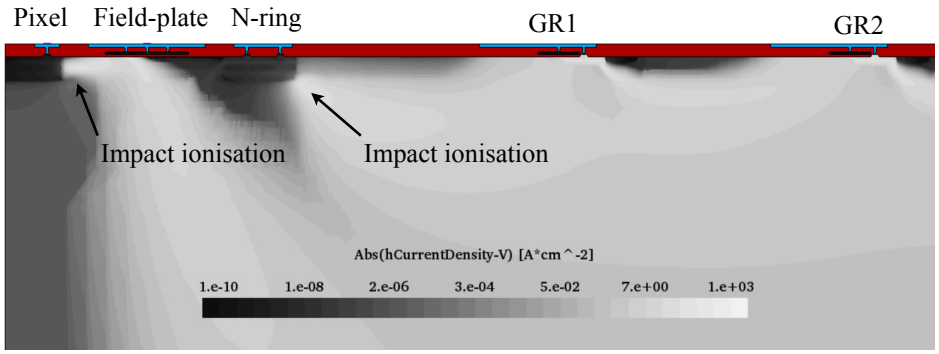



Figure 5.44: Simulated hole current density map of structure E with floating n-ring for $V_{poly} = -100\,V$. The data shows the region between the pixel implant and the GR1 for various $V_{bias} = -800\,V$.

**Summary** The polysilicon field-plate, as implemented in Test Structure E, enables control of the electrostatic potential at the surface of the silicon beneath the field-plate. When a fixed voltage $V_{\text{poly}}$ is applied, the potential beneath the field-plate and the n-ring is lowered to, and maintained at, approximately $V_{\text{poly}}$ while the bias voltage is ramped. This feature allows for the manipulation of the potential difference between the field-plate (or n-ring) and: 1) the grounded pixel implant; 2) the floating GR1, where the electric field maxima are likely to occur. Adjusting the potential distribution via $V_{\text{poly}}$ leads to a shift in the location and a change in the value of the maximum electric field. As a result, the breakdown voltage of the sensor is altered.

## 5.5 Influence from the Surface Damage and the Effects of Overhang

The influence from the surface damage on the test structures was examined for structure C and F, where the samples were irradiated by X-ray to different total ionising doses (TID), and the IV curves were obtained for various TID values. Then, TCAD simulations were employed to illustrate the effects from the surface damage.

### 5.5.1 Measurements

High-intensity irradiation with a high TID dose rate was adopted to allow the samples to receive a higher TID in a relatively shorter time, therefore, it was adopted for the measurements with larger TID steps. Figure 5.45 depicts the IV curves of Structure C from sample S4, and Structure F from sample S6, with a maximum TID of 25.0 Mrad [3]. Two effects were observed:

1. the elevation of the leakage current;
2. the change of the breakdown voltage.

For Structure C, a rapid increase of the current was visible at $V_{\text{bias}} \approx -300\,\text{V}$ for TID = 0.5, 1.0 Mrad and at $V_{\text{bias}} \approx -200\,\text{V}$ for TID = 25.0 Mrad. Beyond these bias voltages, the leakage current continuously increased by approximately 2 orders of magnitude until the onset of the breakdown, which can be identified by the very steep slope of the IV curves at $V_{\text{bias}} \approx -850\,\text{V}$. For the non-irradiated samples, the extraction of the breakdown voltage used the current limit method, where the voltage in the breakdown regime fulfils $I_{\text{leak}}(V_{\text{bias}}) = 1\,\mu\text{A}$. However, due to the high leakage current induced by TID, the Structure C with TID = 25.0 Mrad didn't reach the conventionally defined breakdown regime using such a criterion. In order to obtain the breakdown voltage which can represent the onset of the typical junction breakdown, a higher reference current e.g. 20 µA were adopted to obtain a voltage inside the typical breakdown regime, where the IV curve is almost vertical. Such an effect was more prominent for Structure F. For the non-irradiated case, the leakage current of Structure F is similar with that of Structure C. However, after receiving the same amount of TID, the increase of the leakage current in Structure F was more significant than in Structure C. Within $V_{\text{bias}}$ from approximately −300 V to −400 V, the leakage current of Structure F increased by more than one order of magnitude. For $|V_{\text{bias}}| > 300\,\text{V}$, the leakage current in Structure F is more than one order of magnitude higher than the leakage current in Structure C.

[3] A higher TID was not applicable to these samples, since both of them have undergone irreversible damages during the experiments.

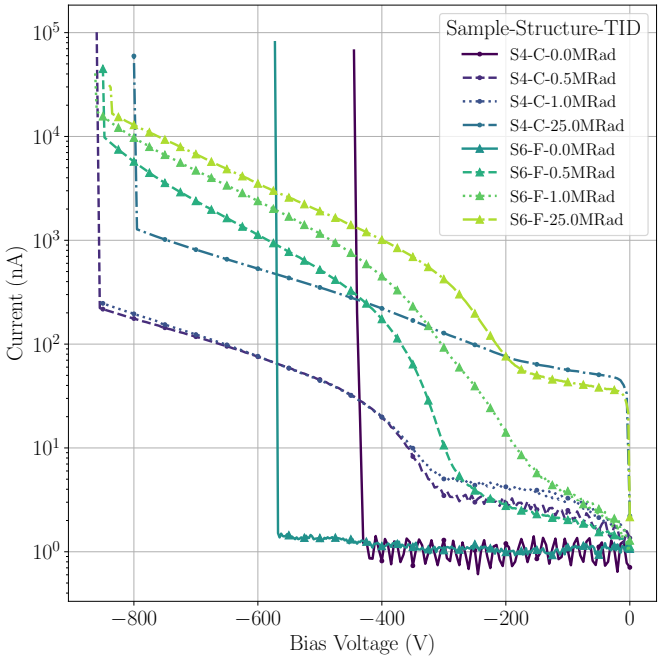



Figure 5.45: Measured IV-curves of structure C from irradiated sample S4 and structure F from irradiated sample S6.

The breakdown voltages extracted from the IV curves in Figure 5.45 are listed in Table 5.9. Two reference current values, 20 µA and 1 µA, were considered for evaluations. The higher reference current value is found in the typical breakdown regime of the IV curves, where a very steep slope occurs. It can be seen that for both structures, the breakdown voltages increased by more than 300 V after receiving 0.5 Mrad of TID. Consequently, Structures C and F exhibited a similar breakdown voltage of approximately −850 V. The IV curve of Structure C, irradiated to TID = 1.0 Mrad, was incomplete, as the breakdown regime was not registered by the measurement device. This was likely due to a too rapid increase in the leakage current, which exceeded the current limit set on the measurement device. Nevertheless, this still suggests that the breakdown voltage for TID = 1.0 Mrad

Table 5.9: Measured breakdown voltages of structure C and F with ground n-ring after TID. The values are extracted from the IV curves in Figure 5.45 by setting the reference current as 1 µA ($V_{\mathrm{BD,1\,\mu A}}$), and 20 µA ($V_{\mathrm{BD,20\,\mu A}}$). Errors are estimated to be ±1 V, because the voltage was ramped in the step of 1 V. The IV curve of structure C with TID = 1.0 Mrad is not listed, since the IV curve of the breakdown regime is not complete.

| **TID (Mrad)** | $V_{\mathrm{BD,1\,\mu A}}$ **(V)** | | $V_{\mathrm{BD,20\,\mu A}}$ **(V)** | |
|---|---|---|---|---|
| | C | F | C | F |
| 0.0 | −443 | −571 | −443 | −571 |
| 0.5 | −858 | −584 | −858 | −848 |
| 1.0 | – | −481 | – | −861 |
| 25.0 | −748 | −398 | −798 | −836 |

is similar to that for TID = 0.5 Mrad. For Structure F, a 1.0 Mrad TID resulted in a further increase in the breakdown voltage by approximately 13 V. When the TID reached TID = 25.0 Mrad, the breakdown voltage decreased by approximately 40 V in Structure C and by approximately 30 V in Structure F, compared to the lower TID levels.

Although $V_{\mathrm{BD,1\,\mu A}}$ in this case does not indicate the typical junction breakdown for all the presented cases in Figure 5.45, such voltages can be used for evaluating the upper limit of the operation voltage of the detectors, whose sensor exhibits a high leakage current level (see section 4.1). In comparison with the cases with reference current of 20 µA, visibly lower voltages were required to reach 1 µA on the irradiated structure F. With increasing TID, $V_{\mathrm{BD,1\,\mu A}}$ was firstly increased by approximately 10 V at TID = 0.5 Mrad, then decreased for higher TIDs. At TID = 25.0 Mrad, the $V_{\mathrm{BD,1\,\mu A}}$ of structure F is approximately 200 V smaller than the non-irradiated case. The changes in structure C are similar to those for structure F but less significant, due to the smaller leakage current.

X-ray irradiation at a lower dose rate was conducted on Structures C and F of Sample S5 for TID within 1.0 Mrad. The IV curves for the non-irradiated case and the TIDs of 0.1 Mrad, 0.25 Mrad, 0.5 Mrad, and 0.75 Mrad are displayed in Figure 5.46 to illustrate changes in the leakage current and the breakdown voltage at finer TID steps. Measurements at higher TIDs were not possible, as the

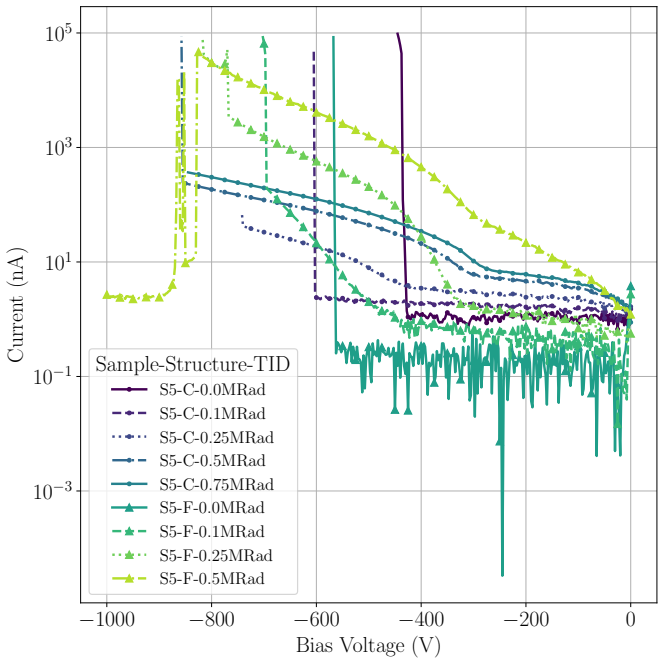



Figure 5.46: Measured IV-curves of structure C and structure F from irradiated sample S5.

sample had undergone irreversible damage during the experiment. This is evidenced by the IV curve of Structure F after receiving 0.75 Mrad of TID, where abnormal leakage current behaviour occurred after applying a bias voltage beyond −800 V. Excluding this special case, the behaviour of the leakage current in both structures exhibited similar effects as shown in Figure 5.45. The typical breakdown effect in the IV curves shifted towards higher $|V_{\mathrm{bias}}|$ with increasing TID, accompanied by a rapid increase in leakage current prior to breakdown. Given that this irradiation setting employed finer TID

steps, it clearly demonstrated that the breakdown voltage and leakage current level increased in both test structures for TID < 1 Mrad.

It is evident that surface damage induced by X-ray irradiation can cause an increase in leakage current and a change in the breakdown voltage of passive CMOS sensors. This is identifiable from the measured IV curves of Structures C and F, where:

- **Leakage current level increases with TID:**
  - **Common effect:** There is a rapid increase in leakage current before the onset of the typical junction breakdown.
  - **Difference:** The leakage current level of Structure F is noticeably higher than that of Structure C.
- **Breakdown voltage changes with TID:**
  - **Low TID:** At TIDs less than 1 Mrad, the breakdown voltage increases as surface damage accumulates.
  - **High TID:** The breakdown voltage decreases when TID reaches 25 Mrad.

Given that the design of the pixel matrix is identical in both test structures, the differing behaviours are likely derived from differences in the guard ring design. Structure C is equipped with an overhang structure, whereas Structure F is not.

### 5.5.2 Simulations

Figure 5.47 and Figure 5.48 display the simulated IV-curves of Structures C and F for TIDs ranging from 0 to 1000 Mrad. An increase in leakage current with rising TID was observed for both guard ring designs. In Structure C, the increase in leakage current becomes more pronounced when TID exceeds 1 Mrad, and the IV-curves steepen for $|V_{\text{bias}}| \gtrsim 750$ V. The leakage current in Structure F elevates more significantly than in Structure C, resulting in orders of magnitude higher leakage current for the same TID. Although exact values of the current differences vary, such behaviour aligns with the measurements. As for breakdown voltages (Table 5.10), both increases and decreases with TID are replicated in the simulations. For Structure C, there is a distinct rise in the simulated breakdown voltage for TID up to 75 or 100 Mrad. Higher TID values result in a gradual decrease in the breakdown voltage. However, the breakdown voltage for Structure F reaches its maximum at TID = 0.1 Mrad and gradually decreases with higher TIDs.

Comparing the simulations with the measurements, it was found that:

- The increase in leakage current level with growing TID is replicated for both structures, and the higher leakage in Structure F is accurately captured. However, the simulation results are still not sufficient for a quantitative prediction of sensor performance.
- The increase in the breakdown voltage with TID is demonstrated in the simulations, but the turning point (where it starts to drop) is inaccurately predicted. In measurements, the drop in breakdown voltages occurred at TID = 25 Mrad, whereas in simulations it does not happen until TID = 75 Mrad. For Structure F, the only noticeable increase in breakdown voltage occurs at the lowest TID of 0.1 Mrad considered in this simulation setting.

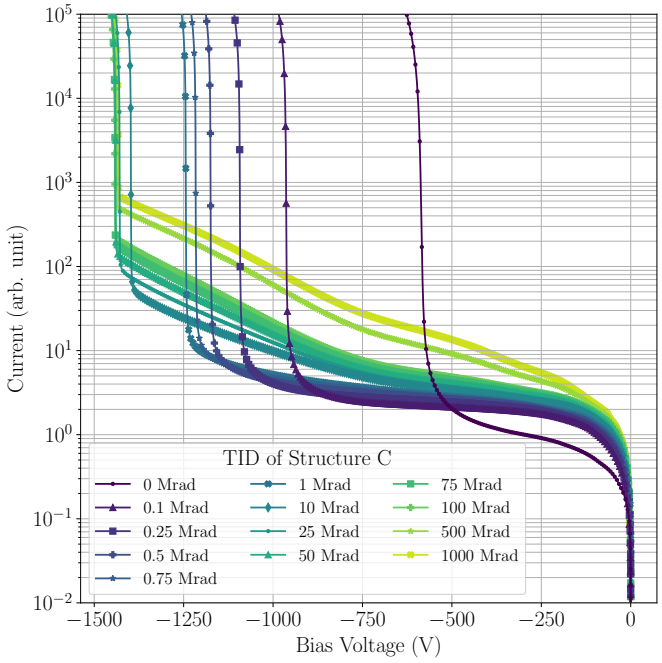



Figure 5.47: Simulated IV-curves of structure C for TIDs from 0 to 1000 Mrad.

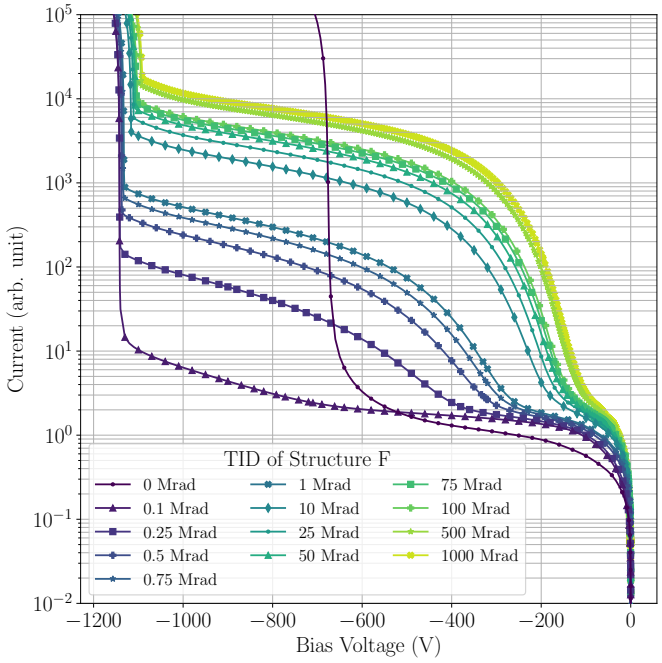



Figure 5.48: Simulated IV-curves of structure F for TIDs from 0 to 1000 Mrad.

Table 5.10: Simulated breakdown voltages of structure C and F for various TIDs. The values were extracted by using a reference current of $5 \times 10^4$ (arb. unit), which lies in the breakdown regime of all IV-curves in Figures 5.47 and 5.47.

| **TID (Mrad)** | $V_{BD}$ **(V)** | |
|---|---|---|
| | C | F |
| 0.00 | −611 | −692 |
| 0.10 | −975 | −1149 |
| 0.25 | −1101 | −1148 |
| 0.50 | −1181 | −1143 |
| 0.75 | −1222 | −1140 |
| 1.00 | −1249 | −1138 |
| 10.00 | −1403 | −1122 |
| 25.00 | −1434 | −1116 |
| 50.00 | −1445 | −1112 |
| 75.00 | −1447 | −1110 |
| 100.00 | −1447 | −1108 |
| 500.00 | −1441 | −1099 |
| 1000.00 | −1437 | −1095 |

The reason for such discrepancies could be an uncalibrated surface damage model. Since surface damage is sensitive to the processing method and the properties of the silicon substrate wafer, the model can vary from device to device, necessitating a calibration of the surface damage model used in this work. However, such a calibration step was not feasible using the considered sensor test structures of pixel sensors. Despite this, the simulations still reveal differences in the increase in leakage current between the two test structures, as well as the rise and fall of the breakdown voltage with increasing TID. Investigating such effects provides insight into how surface damage may affect the breakdown performance of a guard ring design. In the following part of this section, behaviours replicated by the simulations will be discussed in more detail based on the influence of surface damage on the electrical properties of the $Si/SiO_2$ interface, with a particular focus on the different performances caused by the overhang structure through comparisons between Structures C and F.

#### Leakage Current

Three physics models used in the simulations can influence changes in leakage current: the Shockley-Reed-Hall (SRH) statistics, impact ionisation (II), and band-to-band (B2B) tunnelling, as introduced in section 2.6. The SRH model simulates the generation and recombination of interface states included in the surface damage model. The II and B2B models, which depend on electric field strength, enable charge carriers to be generated at high electric fields through ionisation (II) and tunnelling (B2B) processes. To determine the origin of the increasing leakage current in the simulations with TID, simulations were performed with one or more of these generation models deactivated. Figure 5.49 displays various IV curves of Structure F, whose leakage current significantly responds to TID.

These IV curves are divided into two main categories: TID = 0 Mrad and TID = 100 Mrad. The SRH model was active in all cases, controlling the generation and recombination of charge carriers by interface traps influenced by TID. Curves with both II and B2B models active represent the standard

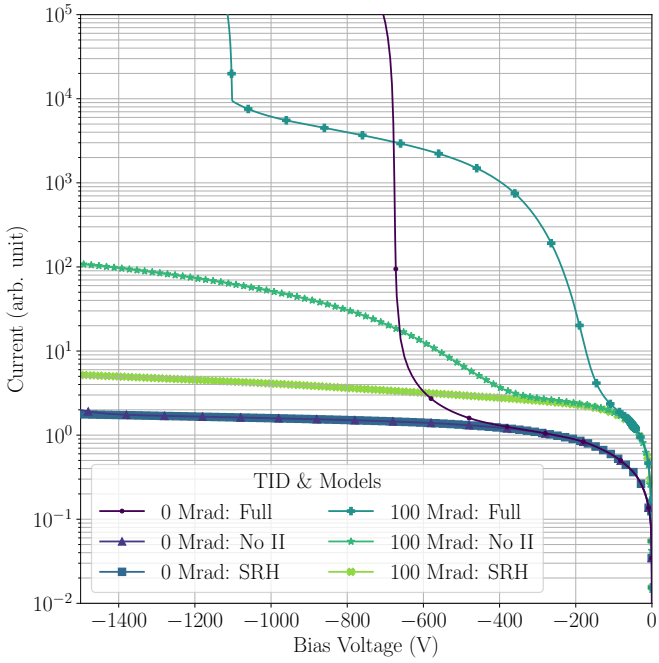



Figure 5.49: Simulated IV curves of structure F for TID = 0, 100 Mrad, and with deactivated charge carrier generation models. The labels in the legends indicates the activated models, where the "Full" represents the standard setting, the "No II" represents deactivated van Overstraeten - de Man impact ionisation model, and the "SRH" represents only activating the SRH recombination.

setting used in the breakdown simulations, consistent with those in Figure 5.48 for corresponding TID levels. At TID = 100 Mrad, the rapid increase in leakage current and the junction breakdown regime disappear after deactivating the II model. Instead, a smaller current increase (by approximately one order of magnitude when the bias voltage is beyond −1 000 V) becomes evident when the bias voltage reaches approximately −500 V. This effect originates from the B2B tunnelling mechanism and thus disappears after deactivating the B2B model. Nevertheless, as the current increase caused by B2B tunnelling is significantly smaller than that caused by the II effect and occurs only at higher voltages, the pattern of rapid leakage current increase introduced by surface damage predominantly results from impact ionisation. Conversely, the influence of interface states becomes more pronounced when comparing the two TID levels after deactivating the II and B2B models. The case with TID = 100 Mrad shows an elevation in leakage current starting at $V_{\text{bias}} \approx 0$ V, compared to TID = 0 Mrad. Similar observations were made for Structure C, where the IV curves using the same simulation settings as for Structure F are shown in Figure 5.50. The increase in current was still predominantly caused by impact ionisation, although the effect was less significant than in Structure F. Again, B2B tunnelling induced a current increase at high bias voltages, and interface traps elevated the leakage current across the entire voltage range.

From these observations, it can be inferred that impact ionisation is the dominant cause of increased leakage current in the guard ring region following surface damage. Consequently, the TID-induced surface damage likely results in high electric fields, which can be mitigated by the overhang structure

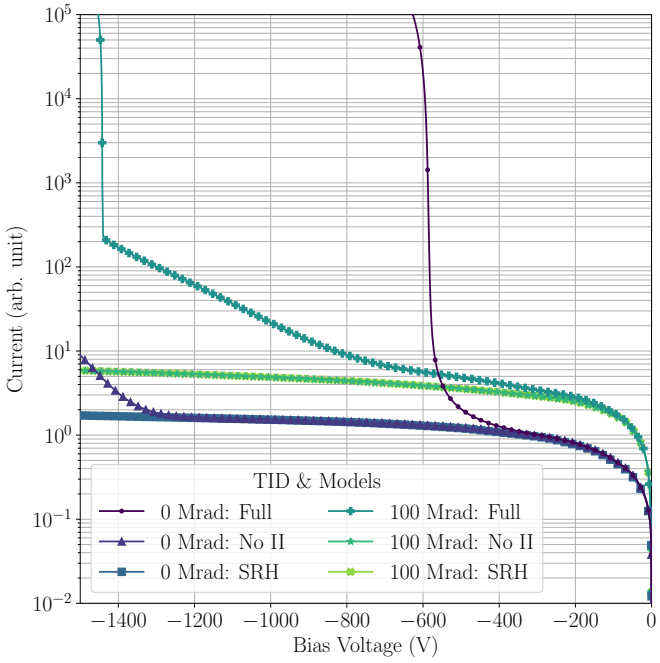



Figure 5.50: Simulated IV curves of structure C for TID = 0, 100 Mrad, and with deactivated charge carrier generation models. The labels in the legends indicates the activated models, where the "Full" represents the standard setting, the "No II" represents deactivated van Overstraeten - de Man impact ionisation model, and the "SRH" represents only activating the SRH recombination.

at the floating guard rings as employed in Structure C. Figure 5.51 illustrates the potential and electric field distribution at the surface of Structure F for various TIDs.

Interface traps and oxide charges increase surface conductivity by accumulating electrons underneath the STI between each implant. This leads to an elevation in the potential at the silicon surface between implants, starting at the edge of the n-ring when TID = 0 Mrad. With increasing TID, the potential between these implants mostly remains at the level of the n-ring, only beginning to drop near the GR1 implant. Although the potential drop is more uniform between floating guard ring implants, the steep potential gradient near each implant results in high electric fields.

The presence of an overhang at the floating guard rings in Structure C, as discussed previously, suppresses the potential underneath. As shown in Figure 5.52, this smoothes the potential distribution near the guard ring implant compared with the case without overhang (see Figure 5.51). This results in a reduced electric field at the edge of the guard ring implant (e.g., compare the peak height at the left edge of the GR1 between Figures 5.51 and 5.52). However, when TID is sufficiently high, the overhang starts to lose its effectiveness in shaping potential distribution, resulting in high electric fields similar to those in Structure F, and consequently a more noticeable increase in leakage due to avalanche generation.

A more intuitive illustration of such avalanche generation of the current and the effect of the overhang structure can be given by the hole current density distribution. The electrons are more susceptible than holes to undergo impact ionisation due to their higher mobility. Therefore, the

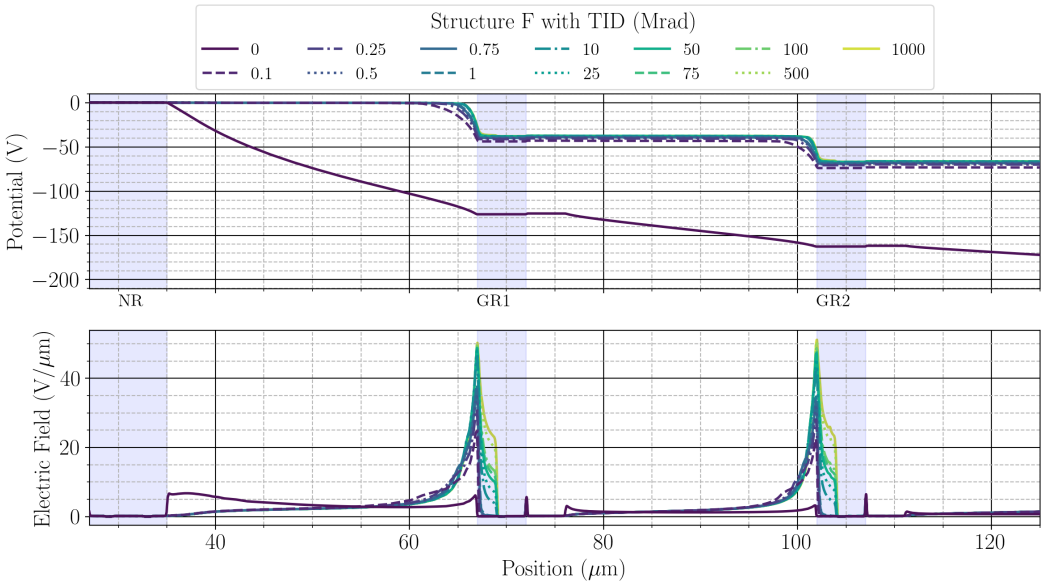



Figure 5.51: Simulated potential and electric field distributions at the surface of structure F for $V_{\text{bias}} = -200\,\text{V}$ and various TID.

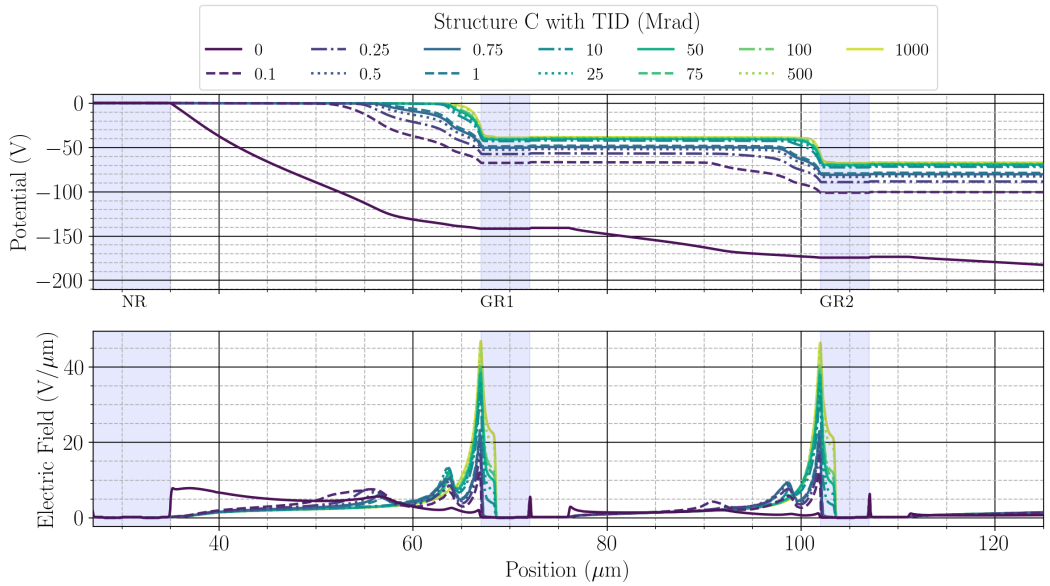



Figure 5.52: Simulated potential and electric field distributions at the surface of structure C for $V_{\text{bias}} = -200\,\text{V}$ and various TID.

secondary hole current will be generated via such a process and flow into the silicon bulk, which is easier to identify. Figure 5.53 illustrates the hole current density map of the area between the n-ring and the GR1 in both structures at a bias voltage of −500 V. When TID = 0 Mrad, the high

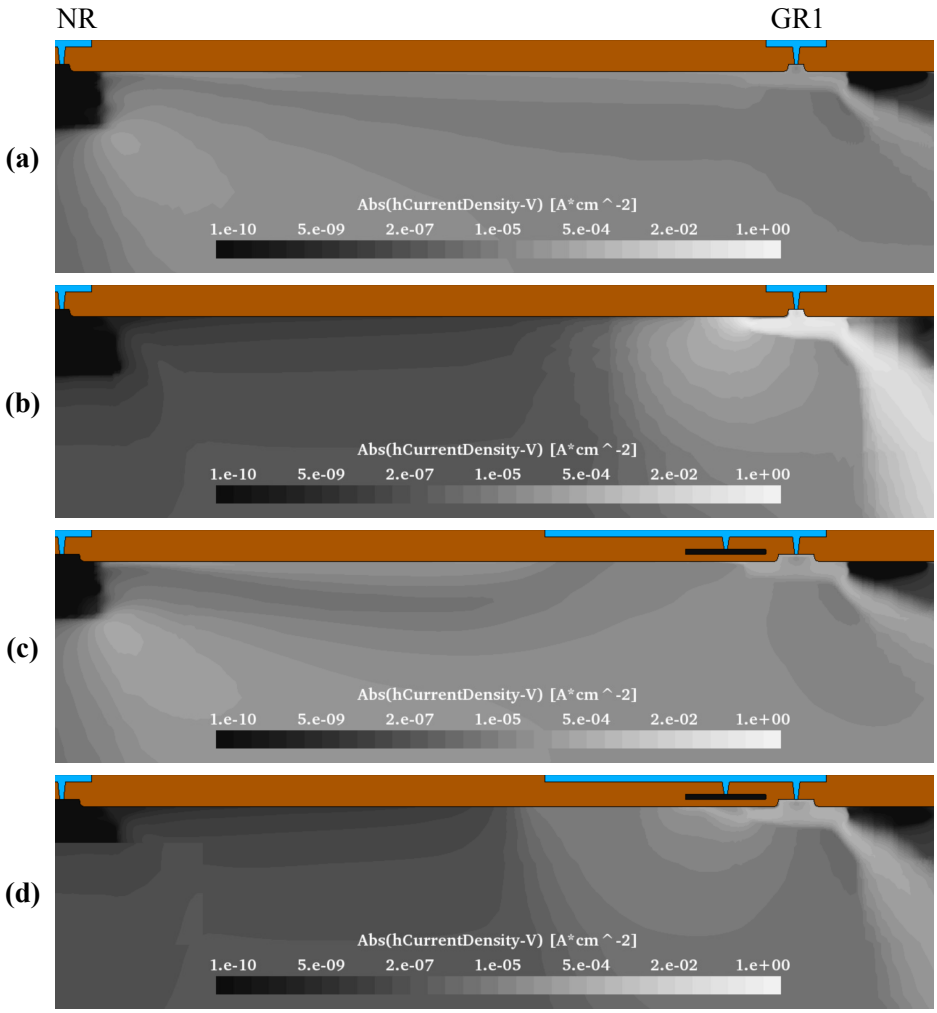



Figure 5.53: Hole density distribution of the region between the n-ring and the GR1, for $V_{bias}$ = −500 V. (a): structure F with TID = 0 Mrad; (b): structure F with TID = 100 Mrad; (c): structure C with TID = 0 Mrad; (d): structure C with TID = 100 Mrad.

hole currents are mainly found at the n-ring and the p-type guard ring implant, as indicated by the greyscale in Figures 5.53 (a) and (c). After adding the surface damage with TID = 100 Mrad, the hole currents in both structures are concentrated at the guard ring implant (Figures 5.53 (b) and (d)). It can be deduced that the impact ionisations take place at the guard ring implant, therefore inducing higher leakage current. The overhang structure, which suppresses the electric field at the guard ring implant, results in a smaller (hole) current (compare the (b) and (d) in Figure 5.53). This explains the smaller leakage current in Structure C, compared with that in Structure F.

### Breakdown Voltage

The role of impact ionisation at the edges of guard rings in increasing leakage current during bias voltage ramping has been identified. A key point of interest is determining the origin of the actual breakdown in the structures, particularly using Structure F as a case study. The hole current density maps for this structure, with a TID of 100 Mrad and for bias voltages ranging from −600 V to the breakdown regime (−1 128 V), are illustrated in Figure 5.54. This figure is directly comparable to Figure 5.53 (b), as both are plotted using the same greyscale. At −600 V, the current density map closely resembles earlier cases, where hole current predominantly emits from the p-type implant, with contributions from GR2 also depicted. As the bias voltage increases to −800 V, a smaller hole current begins to emerge at the edge of the n-ring implant on the silicon surface. This current's magnitude visibly enhances by −1 000 V, as indicated by the greyscale. Although this hole current at the n-ring's upper edge becomes comparable to that from the guard rings, it contributes primarily to the high leakage current levels, as the breakdown regime indicated in Figure 5.48 has not yet commenced at this voltage. After the breakdown (−1 128 V), a new hole current source appears at the n-ring's bottom edge. The evolution of hole current density across different bias voltages suggests that the location and intensity of the high electric field in the guard ring region continuously evolve with increasing bias, shifting from near the silicon surface to the bottom of the deep n-well implant as breakdown approaches.

Figure 5.55 displays the potential and electric field distribution at Structure F's surface for various bias voltages from 0 V to the breakdown regime (−1 128 V). With increasing bias voltage, the previously almost flat potential between guard ring implants begins to develop a gradient, intensifying the electric field in these areas, particularly near the grounded n-ring. Consequently, the potential slope at the n-ring's edge sharpens, and the electric field increases correspondingly. This change is also evident when observing the potential distribution at the bottom of the deep n-well implant of the n-ring (Figure 5.56), where the electric fields near the floating guard ring implants initially exceed those at the n-ring's edge. However, as the bias voltage exceeds −600 V, a significant increase in the electric field occurs at the n-ring's edge, forming a high electric field that aligns with the evolution of the hole current density discussed earlier.

Similar electric field dynamics are observed in Structure C. The difference between these two guard ring structures primarily lies in the potential distribution between the implants, influenced by the overhang. Figures 5.57 and 5.58 depict the potential and electric field distributions at the surface and at the bottom of the n-ring in Structure C for a TID of 100 Mrad and bias voltages up to the breakdown regime. As the simulated breakdown voltage of Structure C is higher than that of Structure F, the breakdown voltage is indicated at −1 465 V. The overhang structure suppresses the potential on the right side of the guard ring implants, resulting in a smoother potential drop compared to Structure F. Nonetheless, the overhang also elevates the electric field beneath it, creating peaks at its edges, as previously shown. With increasing bias voltage, the peak No.2, caused by the overhang, grows more rapidly beyond −600 V. The peak No.1, at the n-ring's edge, emerges as the bias voltage reaches the breakdown regime. These electric field peaks are also evident in the distributions extracted at the bottom of the n-ring, where the peak No.1 grows with increasing bias voltage but only becomes the highest peak when the bias exceeds −1 000 V. This evolution of the electric field reflects the dynamics observed in the hole current density map (Figure 5.59), where high electric fields generated by impact ionisation occur predominantly at the bottom edge of the n-ring when the bias voltage reaches levels sufficient for junction breakdown.

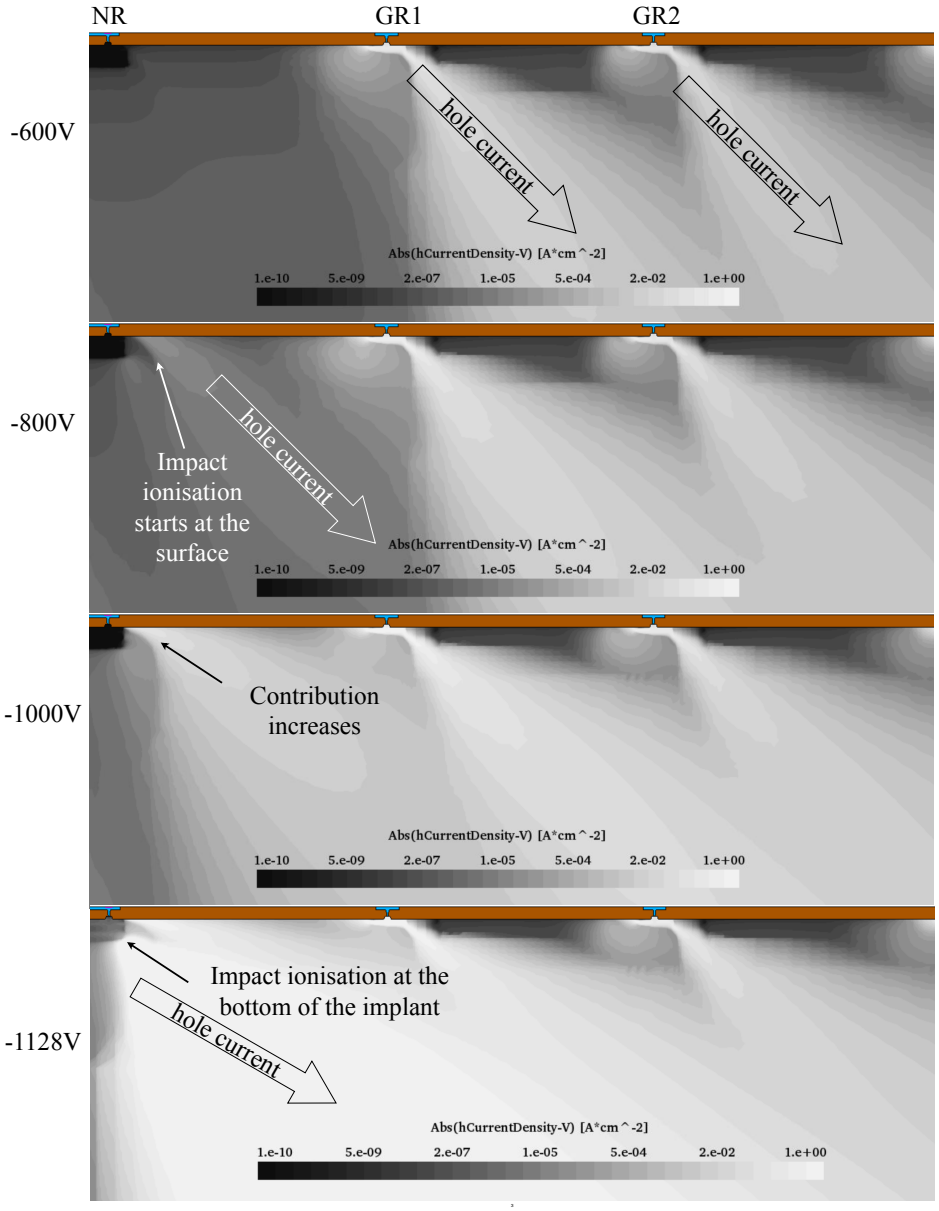



Figure 5.54: Hole current density of the structure F of the region between the n-ring and the inner most guard rings for $V_{\text{bias}} = -600\,\text{V}, -800\,\text{V}, -1\,000\,\text{V}, -1\,128\,\text{V}$ (in the breakdown regime). The greyscale represents the magnitude of the current density, which uses the same scalar as in Figure 5.53 for a direct comparison. The flow of the hole current and the junction responsible for the avalanche breakdown are indicated by the corresponding arrows.

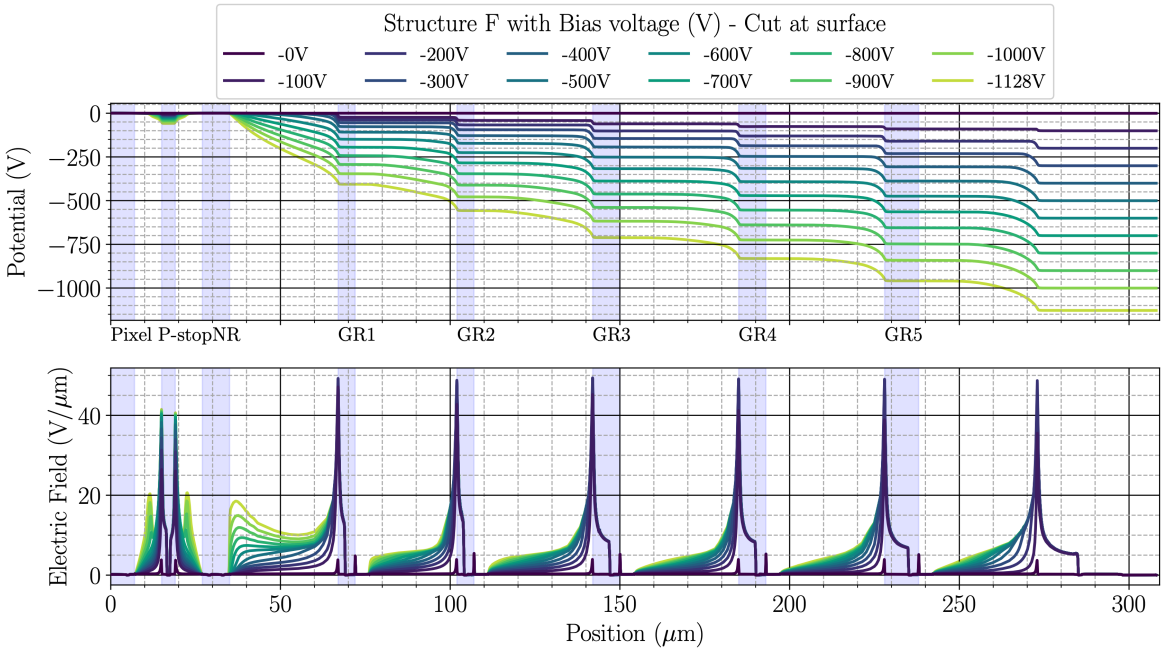



Figure 5.55: Simulated potential and electric field distribution at the surface of structure F with TID = 100 Mrad for $V_{\text{bias}}$ = 0 V, −200 V, −400 V, −600 V, −800 V, -1 000 V, -1 128 V.

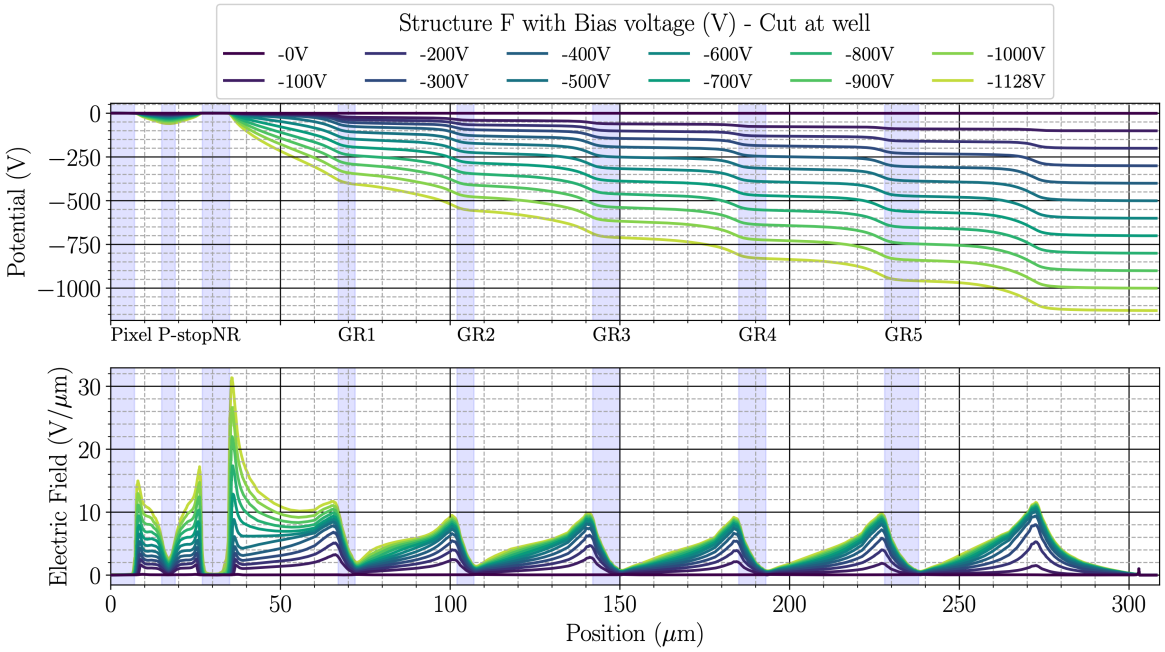



Figure 5.56: Simulated potential and electric field distribution at the bottom of the deep n-well implant of structure F with TID = 100 Mrad for $V_{\text{bias}}$ = 0 V, −200 V, −400 V, −600 V, −800 V, -1 000 V, -1 128 V.

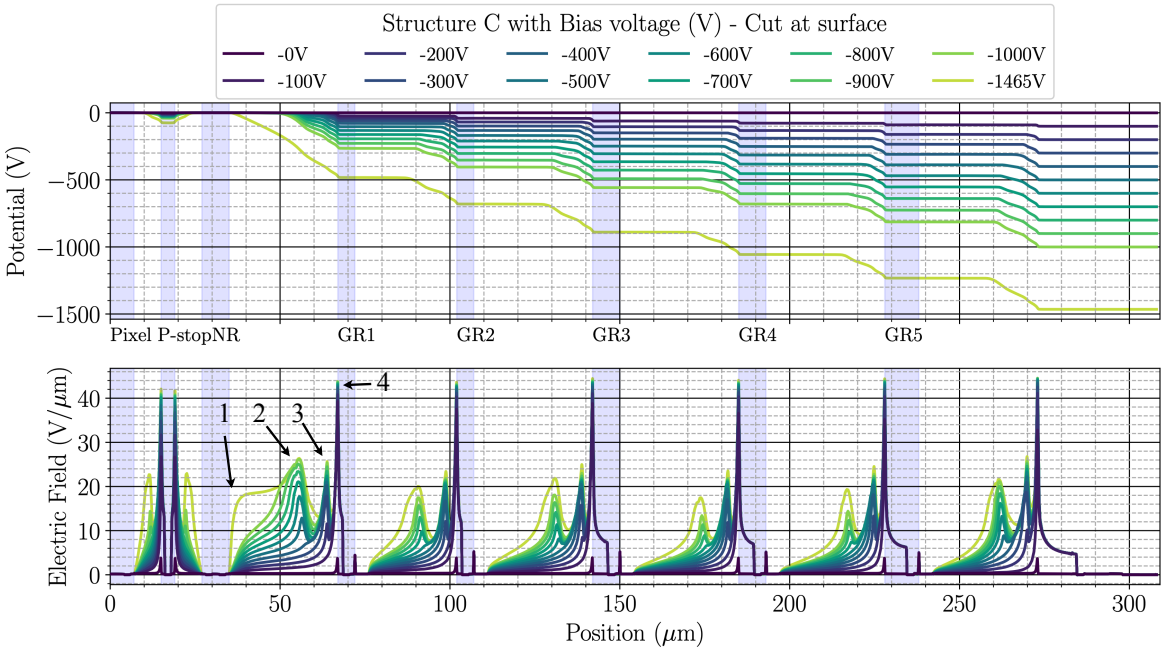



Figure 5.57: Simulate potential and electric field distribution at the surface of structure C with TID = 100 Mrad for $V_{\text{bias}}$ = 0 V, −200 V, −400 V, −600 V, −800 V, -1 000 V, -1 465 V. The numbers label the peaks of the electric field in the same manner as for Figure 5.31.

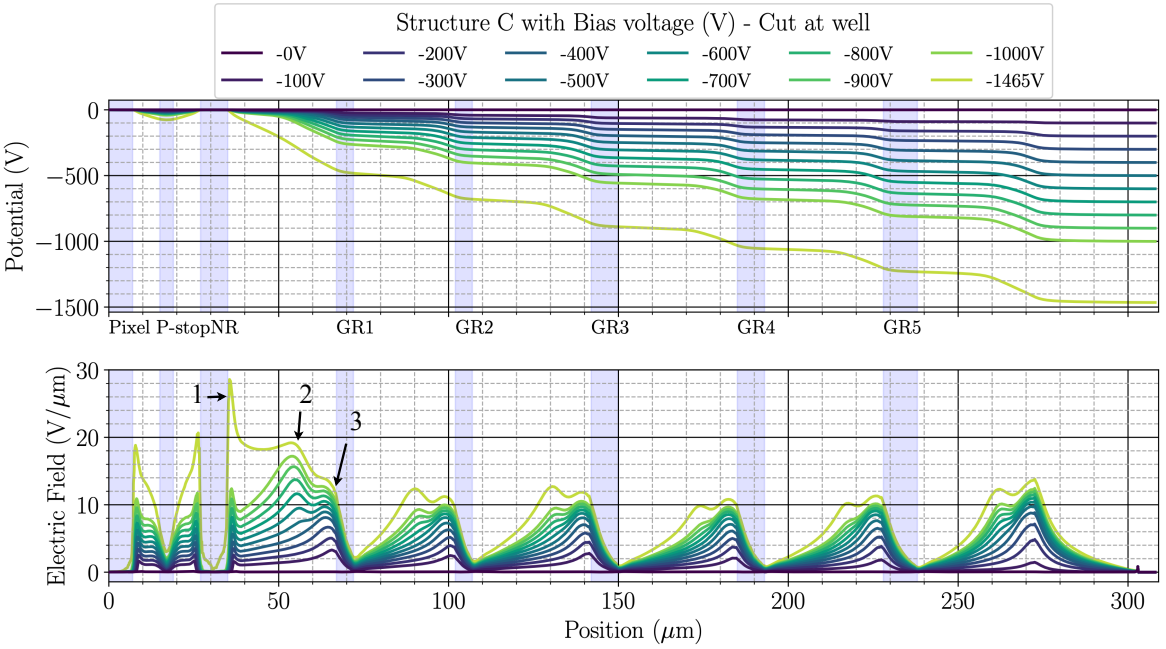



Figure 5.58: Simulate potential and electric field distribution at the bottom of the deep n-well implant of structure C with TID = 100 Mrad for $V_{\text{bias}}$ = 0 V, −200 V, −400 V, −600 V, −800 V, -1 000 V, -1 465 V.

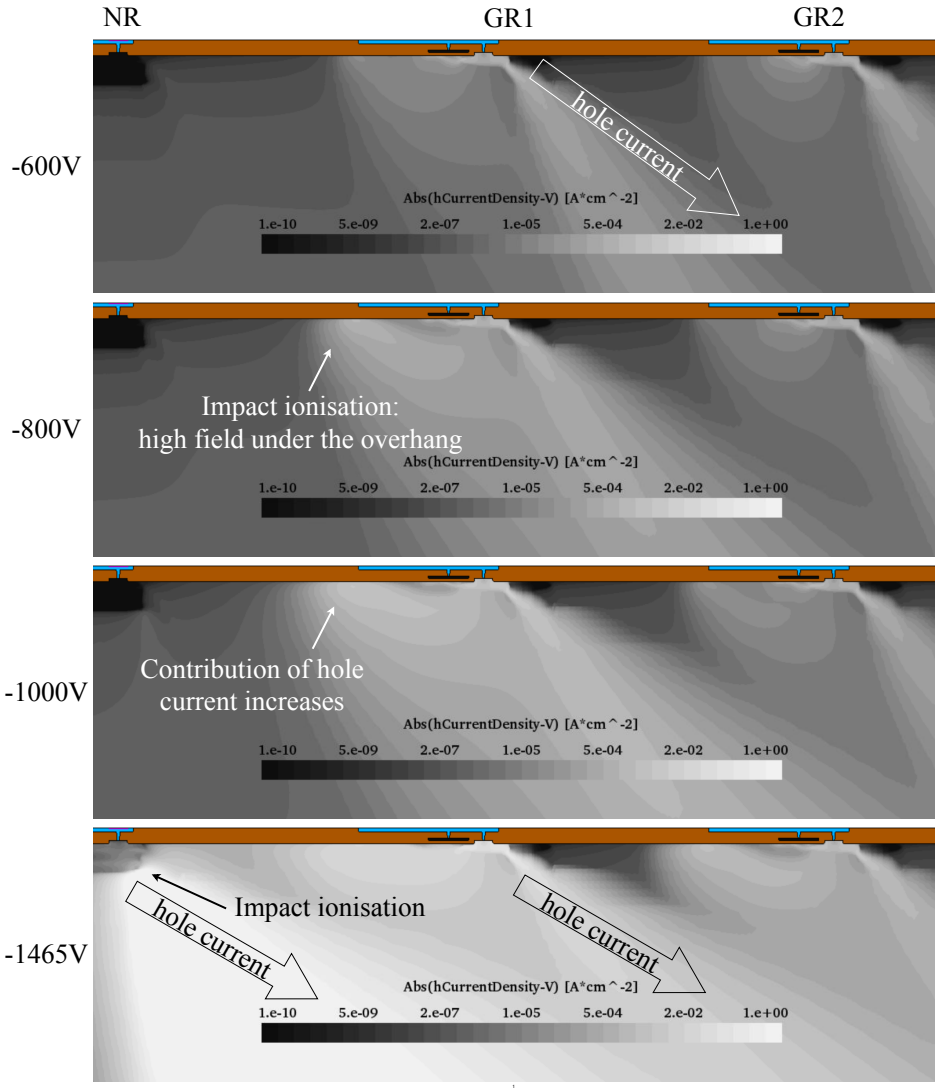



Figure 5.59: Hole current density of the structure C of the region between the n-ring and the inner most guard rings for $V_{\text{bias}} = -600\,\text{V}, -800\,\text{V}, -1\,000\,\text{V}, -1\,465\,\text{V}$ (in the breakdown regime). The greyscale represents the magnitude of the current density, which uses the same scalar as in Figure 5.53 and 5.54 for a direct comparison. The flow of the hole-current and the junction responsible for the avalanche breakdown are indicated by the corresponding arrows.

From these simulations, it is evident that the breakdown effect is closely associated with the high electric field (and subsequent impact ionisation) at the edge of the n-ring implant. In irradiated cases, the electric field at the n-ring becomes significant only at high bias voltages, unlike in unirradiated scenarios where the highest electric field typically occurs at the n-ring due to a large potential drop. Consequently, the breakdown voltage of the guard ring structures increases after incorporating the TID effect.

According to Table 5.10, the simulated breakdown voltages ($V_{BD}$) for Structures C and F exhibit different behaviours. The breakdown voltage for Structure C initially increases with increasing TID but begins to decrease after reaching a TID of 75 Mrad or 100 Mrad. For Structure F, the breakdown voltage peaks at the lowest TID value considered in this simulation set and declines with increasing TID. This behaviour is explicable by examining the potential and electric field distributions, as done for the unirradiated cases, though now at higher bias voltages since the electric field responsible for the breakdown at the n-ring only becomes significant under such conditions. At $V_{bias} = -800$ V, the potential and electric field distributions at the well-depth of Structures C and F are depicted in Figures 5.60 and 5.61, respectively. The electric peak at the n-ring in Structure C decreases with increasing

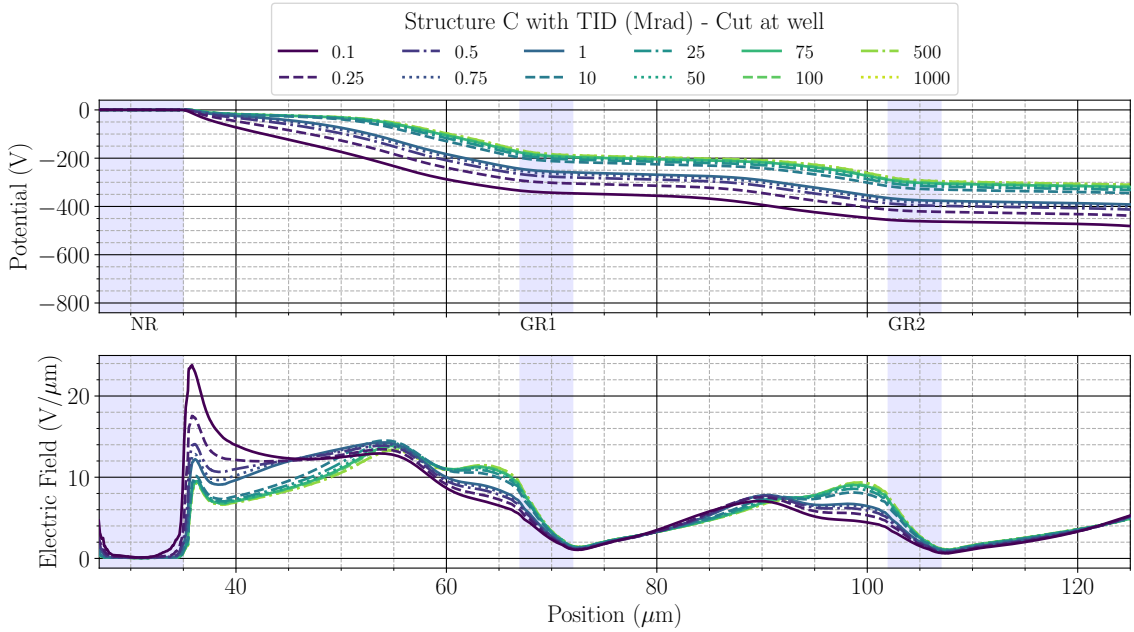



Figure 5.60: Simulated potential and electric field distribution of the structure C at the well-depth. The data is extracted for $V_{bias} = -800$ V and various TID values.

TID, requiring a higher bias voltage to intensify the field sufficiently to trigger the breakdown. This reduction in the electric field becomes less noticeable for TIDs greater than 10 Mrad, corresponding to the less significant increase in the breakdown voltage noted in Table 5.10. As the resolution of the simulation is limited in both the mesh grid and the numerical solution of the physical equations, meaningful discussions on breakdown voltage differences of several volts or the nearly overlapping curves when the TID exceeds 10 Mrad in Figure 5.60 are challenging. The reduction in the breakdown voltage of Structure F with increasing TID is also reflected in the electric field distributions. Unlike

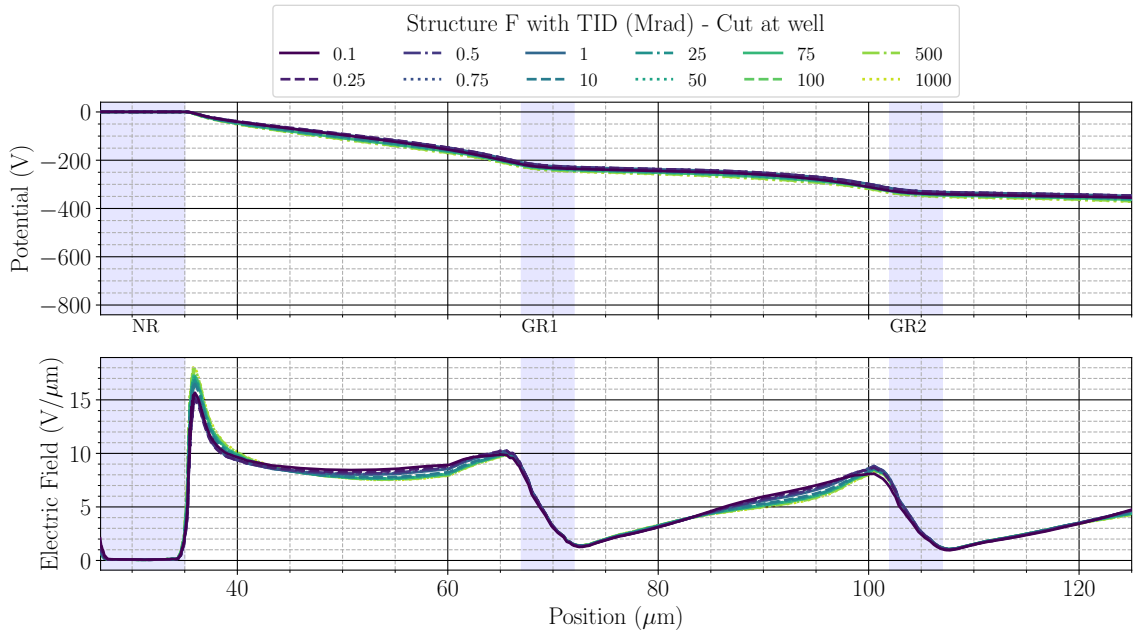



Figure 5.61: Simulated potential and electric field distribution of the structure C at the well-depth. The data is extracted for $V_{\text{bias}} = -800$ V and various TID values.

in Structure C, the TID has a weaker influence on these distributions, especially at the edge of the n-ring implant. Consequently, the differences between curves in Figure 5.61 are minor. However, by comparing the smallest and largest TIDs considered in this simulation set, it is still evident that the peak height increases with the TID, indicating that a lower bias voltage is required to trigger the junction breakdown at the n-ring implant.

**Summary** Two different guard ring designs, test structure C (with overhang) and F (without overhang), were subjected to x-ray irradiation at various TID to induce surface damage, and their current-voltage behaviours were analysed for each TID value. Compared to the un-irradiated state, the surface damage at the SI/$SiO_2$ interface led to an increase in the leakage current level and changes in the breakdown voltage. A rapid escalation in leakage current was observed as the bias voltage increased, with higher TID values correlating with higher leakage currents. At the same TID and bias voltage, structure C exhibited a noticeably lower leakage current than structure F, suggesting that the overhang structure effectively reduces leakage current in the sensor post-irradiation. Following irradiation, the typical breakdown curve of the sensors occurred at a higher bias voltage. For low TIDs, such as below 1 Mrad, the breakdown voltage initially increased with TID, but a decrease was observed at 25 Mrad.

TCAD simulations were conducted using the same simulation domain for structures C and F as in previous sections, incorporating the Perugia surface damage model to assess the effect of TID. Due to the model's lack of calibration specific to the substrate properties of the samples, discrepancies arose between the simulation and measurement results. Although a direct quantitative comparison was not feasible, the simulations demonstrated key effects of TID, specifically the increase in leakage

current level and the fluctuation of breakdown voltage. According to the simulations, the potential and electric field distributions are altered by surface damage, which explains the observed changes in current behaviour and breakdown voltage. Post-irradiation, high electric fields form at the edges of the floating guard ring implants, leading to a surge in leakage current through impact ionisation. The overhang in structure C mitigates the electric field, resulting in lower leakage currents compared to structure F. Regarding breakdown performance, the onset of avalanche breakdown likely occurs at the n-ring implant, as suggested by the hole current density map in the simulation domain. The surface damage necessitates a higher bias voltage to generate a sufficiently high electric field at the n-ring for triggering breakdown, relative to the un-irradiated scenario. The variation in breakdown voltage with increasing TID can also be elucidated by examining the electric field distribution as the bias voltage approaches the breakdown threshold.

## 5.6 Chapter Conclusion

As the high voltage exists between the grounded pixel electrodes and the chip's edge of a silicon pixel sensor, the floating guard rings, which are located in this area, play an important role in regulating the potential distribution to ensure a sufficiently high breakdown voltage. In this chapter, six types of guard ring designs were studied based on the measurements of the n-on-p test structures and simulations of the guard ring structures using TCAD.

Being part of the entire potential drop from the grounded pixels (or the n-ring surrounding the pixel matrix) to the sensor's edge at the negative bias potential, the floating guard rings assume certain potentials. Thus, potential differences are established between the guard ring implants, where those closer to the pixel matrix have higher potentials, and those closer to the edge have lower potentials. The design of the guard rings, including the spacings between implants, the type of doping, and the overhang structures, influences the potential distribution at the sensor's surface. For un-irradiated p-substrate sensors, the most crucial part of the potential distribution is between the grounded n-ring and the innermost guard ring, where the largest potential difference is located. Therefore, the highest electric field typically occurs at the edge of the n-ring, where the avalanche breakdown occurs when the bias voltage is sufficiently high. Modifying the guard ring designs can regulate the potential distributions and therefore affects the breakdown performance.

It has been found that a larger gap between the n-ring and the innermost guard ring or adding an n-type implant at the outer side of the p-type guard ring can help smooth the potential distribution and reduce the electric field. Increasing the gap size reduces the steepness of the potential drop, and adding the n-type implant can elevate the potential at the guard rings so that the potential difference can be reduced. A further increase in the floating potential at the guard rings can be achieved by employing the deep n-well, which will be explored in more detail in the next chapter. By considering these features, the breakdown voltage of a pixel sensor can be improved. Another interesting effect is that applying voltages at a polysilicon field-plate located on top of the silicon oxide can control the breakdown voltage. The field-plate can modify the potential at the surface of the silicon and, hence, manipulate the potential distribution as well. This method can be further investigated to optimise the breakdown performance of sensors.

The overhang structure implemented on the guard rings in this work was found not to be beneficial for improving the breakdown performance of un-irradiated sensors because it suppresses the potential at the guard rings, hence increasing the potential difference in the region between the n-ring and

the innermost guard ring. However, the benefit of the overhang is observed in the presence of surface damage. The surface damage increases the surface conductivity due to electron accumulation. Consequently, the location of the high electric field shifts from the outer side of the n-ring to the inner side of the floating guard rings. The high electric field at the guard rings triggers impact ionisations and leads to a rapid current increase during the ramping of the bias voltage. From the measurements of irradiated samples of the test structures with and without overhang, it is found that the overhang structure helps suppress the leakage current generation because the overhang suppresses the local electric field at the guard rings. The breakdown voltage initially increases with the total ionising dose (TID) and then drops at high TID values. The final avalanche breakdown also occurs at the n-ring, where the electric field is influenced by the TID and only becomes significant when the bias voltage is sufficiently high (approaching the breakdown).

CHAPTER 6

# Sensor Developments Related to the RD50 MPW Monolithic Pixel Detector Prototypes

The term RD50-MPW refers to the High-Voltage CMOS (HV-CMOS) n-on-p Depleted Monolithic Active Pixel Sensor (DMAPS) prototypes developed by the CERN-RD50 CMOS group. These prototypes were manufactured via LFoundry Multi-Project Wafer (MPW) submissions [75–77]. From 2017 to 2023, the RD50-MPW prototype underwent four development iterations (RD50-MPW1 to RD50-MPW4). During the RD50-MPW3 submission, five test structures with varied floating guard ring structures were designed by the author to explore the breakdown performances, particularly the effects of the deep n-well implant implemented for the floating guard rings. The university of Bonn joined the CERN-RD50 CMOS group leading the optimisation of the breakdown performance of the fourth-generation detector prototype (RD50-MPW4), whose design was finalised and submitted in May 2023.

The subsequent sections will discuss the designs, TCAD simulations, and breakdown measurements of the test structures for the RD50-MPW3 submission, followed by the optimisation of the RD50-MPW4 prototype sensor using TCAD simulations.

## 6.1 Guard Ring Test Structures for the RD50-MPW3 Submission in 2021

The depth profile of the floating n-well attached to the guard ring modifies the potential distribution and the maximum electric field in the guard ring region, consequently affecting the breakdown performance of a silicon pixel sensor. The deep n-well implant used in the LFoundry 150 nm CMOS process has demonstrated the capability to elevate the potential and thus increase the breakdown voltage, as explored in chapter 5. The primary objective of the test structures is to investigate the impact of the deep n-well by incorporating it into the floating guard rings. The guard ring design of structure F (Figure 5.3) serves as a baseline for new designs due to its high breakdown voltage prior to radiation damage. Building on this foundation, new guard ring structures were conceptualised and examined initially through TCAD simulations of the guard ring region cross-sections. Subsequently, test structures featuring these new guard ring designs were fabricated and the simulation results were corroborated through empirical measurements.

The RD50-MPW3 prototype and the test structures were manufactured on p-type Czochralski-grown silicon wafers with resistivities specified by the foundry at 1.9 k$\Omega \cdot$ cm and 3.0 k$\Omega \cdot$ cm. The wafers

were thinned to 280 µm and underwent no backside processing or metallisation. A 6-metal layer process was selected to accommodate the numerous electronic interconnections required by the monolithic detector prototype. The configuration of the 6 metal layers is consistent with that depicted in Figure 3.15, with metal layers M1 to M5 situated between the silicon surface and the top metal layer. In the design of the test structures, only metal layers M1, M2, and the top layer were employed to construct the overhang structure and the measurement pads. The remaining metal layers were excluded from the design and automatically generated by the foundry to avoid interference with the intended structures.

This section details the design of the guard rings in the test structures, the 2D TCAD simulations assessing breakdown performance, and the measurements conducted on the fabricated chips.

### 6.1.1 Design Layout of the Test Structures

Five distinct guard ring designs were incorporated into diode-like test structures for fabrication. Figure 6.1(a) illustrates the layout of these five test structures (labelled "V1" to "V5"). At the center of each test structure, a square n-type implant (214 µm × 214 µm deep n-well) functions as the diode electrode on the p-type substrate. This electrode is encircled by guard ring implants. Figure 6.1(b) presents a photograph of a fabricated silicon chip, while Figure 6.1(c) zooms into the corner of structure V1, showcasing the arrangement around the n-type diode electrode, which includes: 1) a p-well implant resembling the p-stop structure in a pixel matrix (as depicted in Figure 3.17 and 5.2(d)); 2) an n-ring crafted from the deep n-well; 3) five n+p floating guard rings labelled "GR1" to "GR5"; and 4) a p-type edge ring. These components are enclosed by a seal ring delineating the edge of the test structure/chip. The principal distinctions between the test structures lie in the doping profile, geometry, and the overhang structure of the floating guard rings, which will be elaborated upon later.

Two rows of bonding pads are evident in each chip's photograph (Figure 6.1(d)), with the upper [1] row designated for the p-type implants and the lower for the n-type implants. Differing from the test structures described in chapter 5, the n-type implants of the floating guard rings are also linked to bonding pads, such as "GR1-n" denoting the n-type implant of guard ring "GR1." Conversely, the p-wells of the floating guards connect to pads labelled "-p." A 75 µm × 75 µm opening in the metal layers is positioned at the center of the diode electrode. This allows for the application of a red laser beam, which can be utilised for further studies [2].

Figure 6.2 presents the cross-sectional views of the guard ring implants in the test structures. Structure V1 is used as the baseline, employing the guard ring configuration from structure F as detailed in chapter 5. Structures V2 and V3 incorporate a "full deep n-well" for all floating guard rings, diverging from the standard n-well used in V1. These designs are distinct in their overhang structures. As depicted in Figure 6.3, structure V3 includes an overhang on all floating guard rings, unlike structure V2, which lacks any overhangs, consistent with other structures.

Structure V4 differs from V1 in the geometry of the corners as illustrated in Figure 6.1 (a). Instead of curved corners, all implants in V4 feature chamfered corners extending from the n-type diode electrode to the edge ring. Structure V5 is distinct in its use of the deep n-well, which is applied only to the two innermost guard rings (GR1 and GR2). The third guard ring (GR3) utilizes an intermediate

[1] The orientation is marked by the label on the right side of each test structure.

[2] Laser beams serve as important tools in characterising silicon sensors for particle detectors, with the Transient Current Technique (TCT) typically employing a red laser (wavelength approximately $\lambda \approx 660$ nm) to generate charge carriers at the sensor surface.

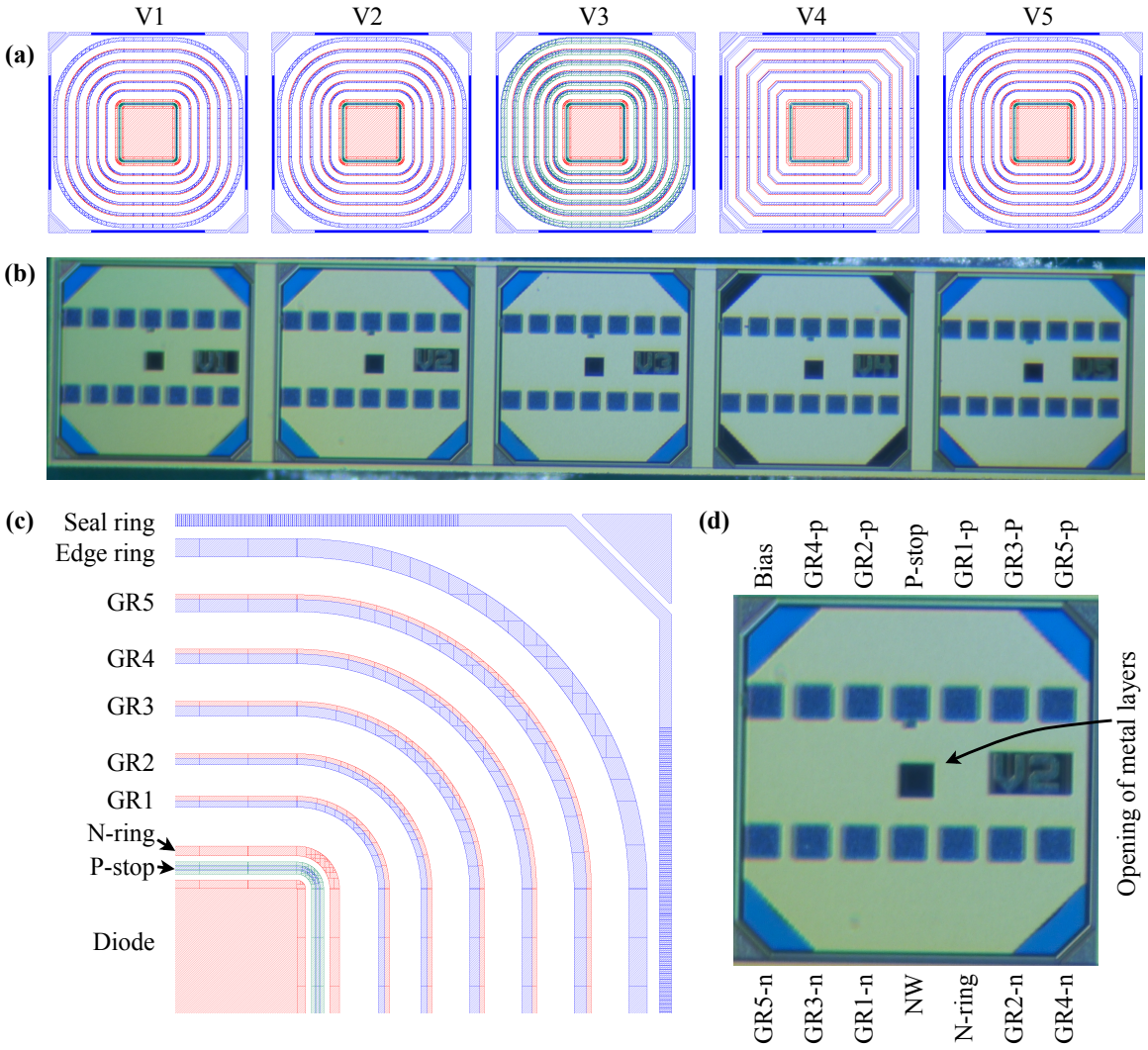



Figure 6.1: The test structures for the RD50-MPW3 submission. (a): The design layout of the test structures V1 to V5. The n-well, p-well and polysilicon layer are shown to indicate the geometry of the implants. (b): the photo of a fabricated chip containing the test structures. (c): the layout of the upper right corner of V1 showing the common design of the implants in all test structures. (d): the photo of V2 on the fabricated chip, where the two rows of bonding pads are labelled according to the connected implant. See the main text for detailed descriptions.

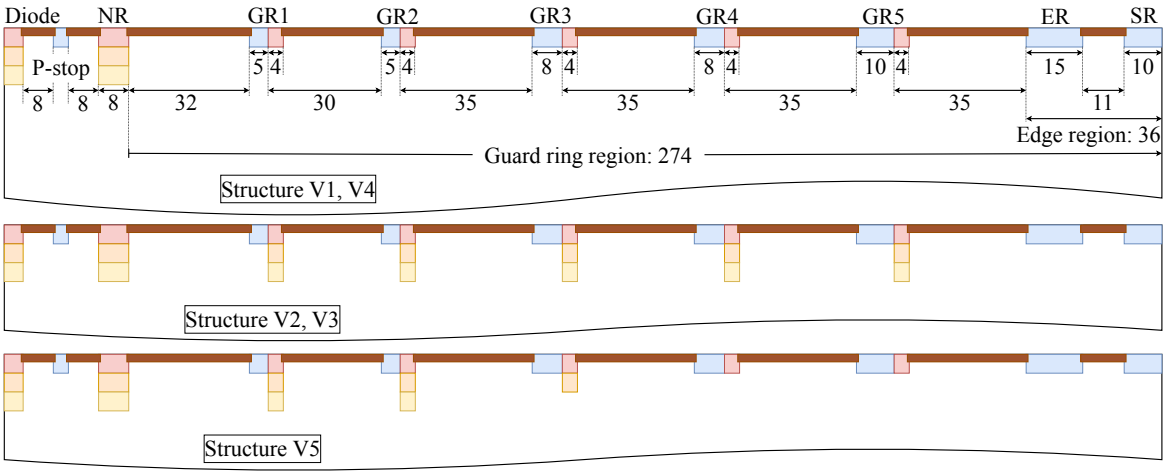



Figure 6.2: The schematic section views of the guard ring implants in the test structures. The geometrical parameters are given in µm. Each section view include a part of the diode electrode ("Diode"), the p-stop, the n-ring ("NR"), the floating guard rings ("GR1" to "GR5"), the edge ring ("ER"), and the seal ring ("SR"). The width of the implants, and the distances between implants are identical in all test structures.

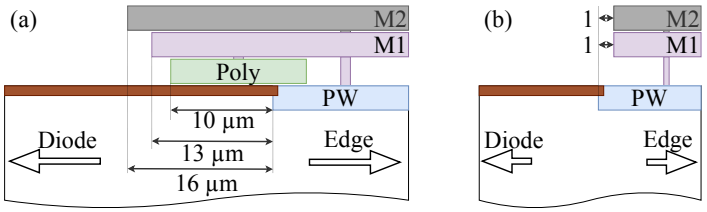



Figure 6.3: The overhang structure of the floating guard rings in test structures. (a): In V3, the edge of the polysilicon layer, and the metal layers M1 and M2 exceed the edge of the p-well implant. (b): In the remaining test structures, the polysilicon layer is not implemented and the edge of the M1 and M2 layers does not exceed the edge of the p-well.

depth achieved by employing only the standard n-well and the NISO implant, while the outermost guard rings (GR4 and GR5) use the standard n-well.

Characteristics of the test structures are detailed in Table 6.1, enabling the definition of three control groups to assess the impact of design variations on breakdown performance:

1. **Structures V1, V2, & V5:**
   Investigating the impact of the deep n-well.

2. **Structures V2 & V3:**
   Assessing the influence of the overhang.

3. **Structures V1 & V4:**
   Evaluating the effects of corner design.

Subsequent sections will focus on the breakdown simulation results for Structures V1, V2, V3, and V5. Each structure's breakdown performance will be elucidated through analyses of the potential and

Table 6.1: Features of the guard ring designs in the test structures for the RD50-MPW3 submission. The column "Deep n-well" indicates whether the floating guard rings are equipped with the deep n-well implant: "No" stands for the use of standard n-well, "Full" stands for the use of deep n-well for all guard rings, "Gradient" for structure V5 represents that the deep n-well is applied to the inner rings and shallower n-wells are used for the outer rings.

| Label | Deep n-well | Corner | Overhang |
|---|---|---|---|
| V1 | No | Rounded | No |
| V2 | Full | Rounded | No |
| V3 | Full | Rounded | Yes |
| V4 | No | Chamfered | No |
| V5 | Gradient | Rounded | No |

electric field distributions, following methodologies outlined in the preceding chapter. Measurement outcomes will also be discussed to provide comparative insights alongside the simulation data.

### 6.1.2 Simulation of the Breakdown Effect, Potential and Electric Field Distributions

The 2D simulation domain for the breakdown performance of different guard ring designs was constructed based on the section views presented in Figure 6.2. A substrate thickness of 280 µm with resistivities of $1.9, \mathrm{k\Omega \cdot cm}$ and $3.0, \mathrm{k\Omega \cdot cm}$ was considered for these simulations. Given that all test structures share the same p-stop and n-ring design, the analysis primarily focuses on the impact of floating guard rings on breakdown performance under a grounded n-ring scenario.

The simulated IV curves for structures V1, V2, V3, and V5, each with a bulk resistivity of $1.9, \mathrm{k\Omega \cdot cm}$, are displayed in Figure 6.4. The breakdown voltages of these structures are grouped into two categories: V1 and V3 with $|V_{\mathrm{BD}}| < 600\,\mathrm{V}$, and V2 and V5 with $|V_{\mathrm{BD}}| > 700\,\mathrm{V}$. When compared to structure V1, structures V2 and V5 exhibit an increase in breakdown voltage exceeding 100 V. Only a marginal difference of about 10 V in breakdown voltage is observed between V2 and V5. Despite having implant profiles identical to those of V2, structure V3, which incorporates overhang structures, shows a lower breakdown voltage similar to that of V1.

As previously discussed, analysing the potential and electric field distributions within the guard ring region—especially the maximum electric field strength—is crucial for understanding the variance and similarities in the breakdown voltages across the structures. Referencing Figures 5.21, 5.28, and 5.29, it is noted that the maximum electric field typically occurs at the lower right edge of the n-ring, particularly in structures with a deep n-well at the n-ring and a significant GR1 gap (e.g., Structures C and F from the previous chapter). It is therefore insightful to assess the potential and electric field distributions along the bottom edge of the deep n-well ("cut at well" in Figure 5.21) for these newly designed guard ring structures.

The simulated potential and electric field distributions for the four guard ring designs from the RD50-MPW3 submission are depicted in Figure 6.5. With the n-ring grounded, a bias voltage induced a potential drop from the n-ring towards the chip's edge horizontally. In all designs, the largest potential drop occurred between the n-ring and the innermost floating guard ring (GR1), where the maximum electric field was also located.

Upon comparing the potential distributions of V1 and V2, it was observed that the deep n-well at the guard rings elevated the potential at these implants, reinforcing the findings discussed in section 5.4.2. Consequently, the maximum potential drop in structure V2 was reduced compared to that in V1,

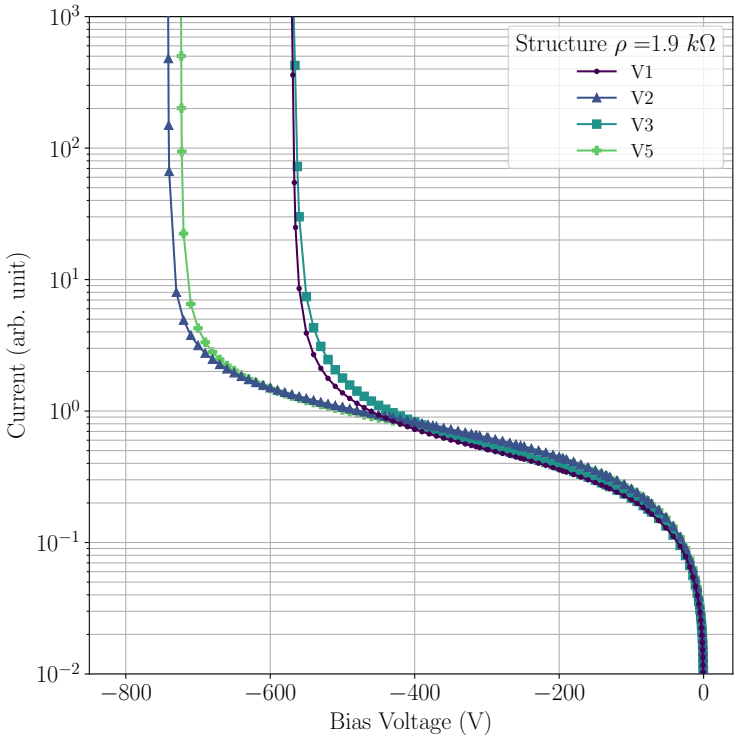



Figure 6.4: Simulated IV curves of test structures V1, V2, V3, and V5 with grounded n-ring. The resistivity of the sensor bulk is 1.9 k$\Omega \cdot$ cm

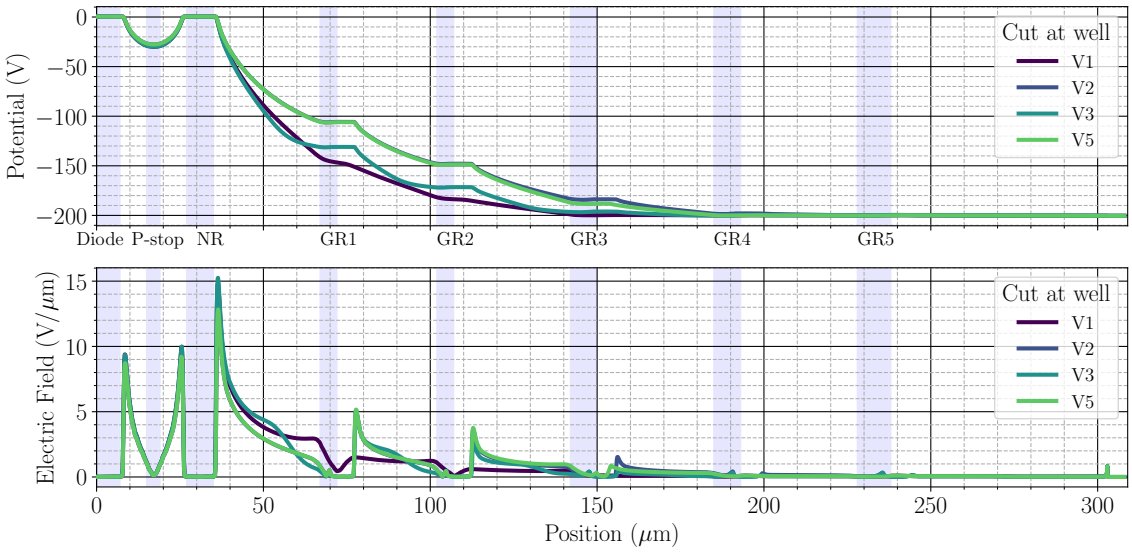



Figure 6.5: Simulated potential and electric field distribution at the deep n-well of structure V1, V2, V3, and V5 with the resistivity of 1.9 k$\Omega \cdot$ cm. The position and the width of the implants are indicated by the shaded pillar in the diagram. The diagrams are obtained for grounded n-ring, and $V_{\text{bias}} = -200$ V.

which similarly affected the maximum electric field. Further examination of the region of the inner guard rings (Figure 6.6) revealed that the maximum electric field in V1 was clearly higher than in V2. The elevation of the electrostatic potential in the innermost guard rings plays a crucial role in breakdown performance. Comparing structures V5 and V2, the similar breakdown voltages result from analogous maximum electric fields. By incorporating the deep n-well at guard rings GR1 and GR2 in V5, its potential and electric field distributions nearly align with those of V2 up to GR2. Beyond this point, the distributions diverge due to the decreasing depth of the n-well implant from GR3 in V5, resulting in a lower potential at GR3 compared to V2, as shown in Figure 6.5. At a bias voltage of −200 V, differences in the electrostatic potential at the outer rings GR4 and GR5 are not apparent, since the region near these guard rings has not yet fully depleted. However, at higher bias voltages, the influence of the deep n-well becomes apparent, elevating the potential at the outer guard rings of V2 above those of V5.

The impact of the overhang on the floating guard rings was discussed in the previous chapter; the polysilicon and metal overhang structures suppress the electrostatic potential at the floating implants, leading to a more subdued overall potential distribution in the guard ring region compared to guard rings without overhangs. This effect is similarly observed in the comparison between the potential and electric field distributions of structure V2 (without overhang) and V3 (with overhang) shown in Figure 6.6. Despite this data being taken at the bottom edge of the deep n-well, the influence of the overhang on the electric field distribution remains evident (compare with Figure 5.31). The potential in the silicon beneath the overhang is notably suppressed, reducing the electrostatic potential. This is particularly significant between the n-ring and GR1, where the reduced potential near GR1 sharpens the potential slope at the edge of the n-ring. This steeper slope increases the maximum electric field, thereby reducing the breakdown voltage compared to structure V2. Consequently, for

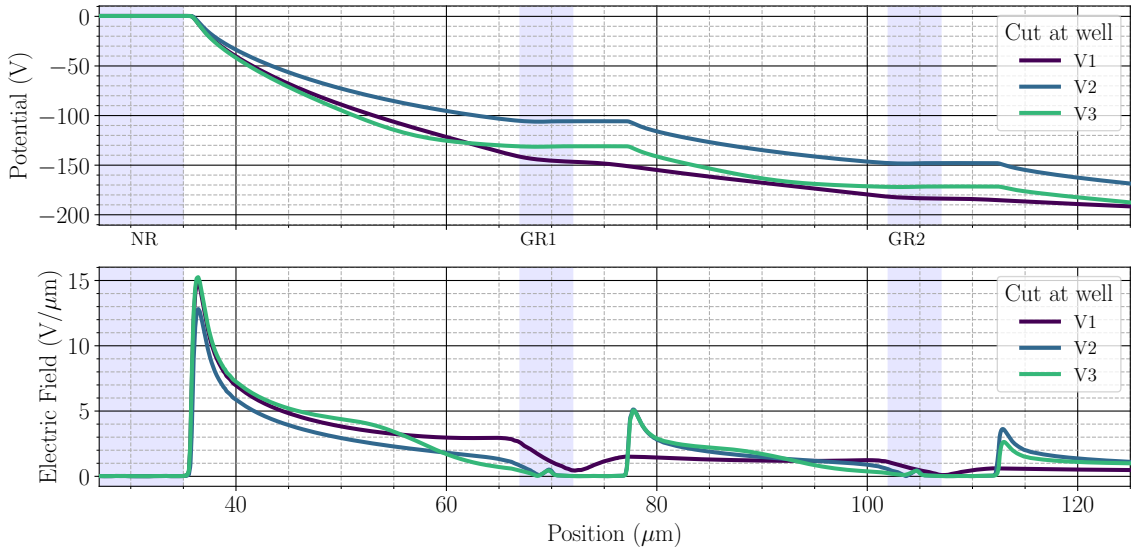



Figure 6.6: Simulated potential and electric field distribution at the deep n-well of structure V1, V2 ,and V3 with the resistivity of 1.9 kΩ · cm. The n-ring is grounded and $V_{\text{bias}} = -200$ V. The region of guard ring GR1 and GR2 is presented for a better inspection of the maximum electric field.

the non-irradiated cases, the overhang structure diminishes the breakdown performance of structures equipped with a deep n-well at the guard rings. Comparing V3 with V1, the similarity in the maximum electric field values leads to analogous breakdown voltages.

For a substrate resistivity of $3.0\,\mathrm{k\Omega \cdot cm}$, the simulated IV curves across the various guard ring designs (see Figure 6.7) exhibit a consistent pattern. Specifically, structures V2 and V5 display higher breakdown voltages compared to V1 and V3. Additionally, an increased substrate resistivity correlates with higher breakdown voltages for identical designs when compared to those with a lower substrate resistivity. This correlation is highlighted by the breakdown voltage data for both resistivities listed in Table 6.2, illustrating the direct impact of substrate resistivity on the device's breakdown voltage.

With a resistivity of $3.0\,\mathrm{k\Omega \cdot cm}$, the breakdown voltages ($|V_{\mathrm{BD}}|$) for all designs are approximately 100 volts higher than those at $1.9\,\mathrm{k\Omega \cdot cm}$. Examining structure V2 as an illustrative case, Figure 6.8 depicts the potential and electric field distributions at both resistivity levels. The data shows that resistivity significantly influences the potential at the floating guard rings, where higher resistivity results in greater potential at each guard ring implant compared to the lower resistivity. This yields a reduced potential difference between the n-ring and GR1, thereby suppressing the maximum electric field. As the bias voltage increases, the maximum electric field in structures with lower bulk resistivity reaches the threshold for junction breakdown more quickly.

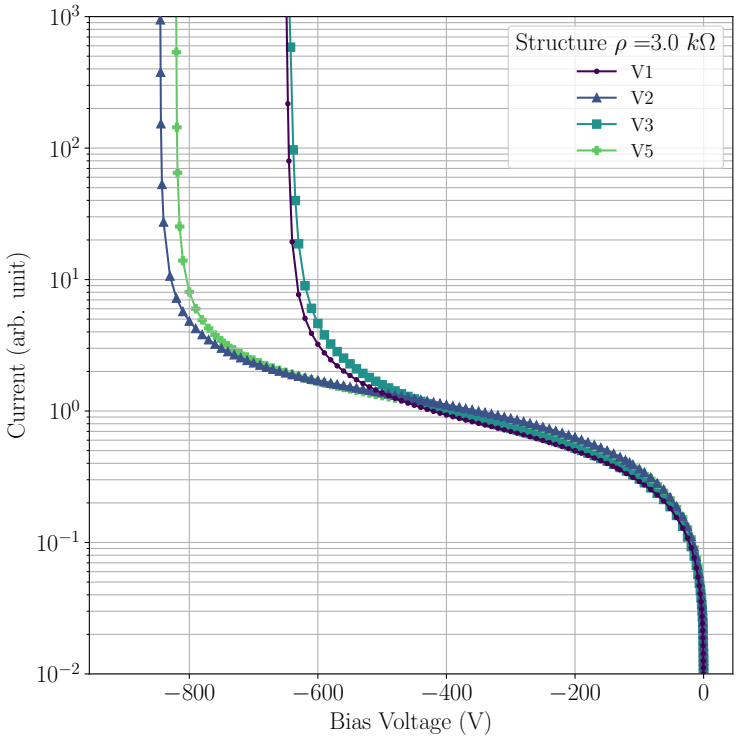



Figure 6.7: Simulated IV curves of test structures V1, V2, V3, and V5 with grounded n-ring. The resistivity of the sensor bulk is $3.0\,\mathrm{k\Omega \cdot cm}$

Table 6.2: Breakdown voltages of the test structure V1, V2, V3, and V5 with grounded n-ring. $V_{\mathrm{BD},1.9}$ represents the breakdown voltage of the simulated structure with a bulk resistivity of $1.9\,\mathrm{k\Omega \cdot cm}$, and $V_{\mathrm{BD},3.0}$ represents the breakdown voltage for the bulk resistivity of $3.0\,\mathrm{k\Omega \cdot cm}$. The values are the voltages where the leakage current reaches 10 (arb. unit) in Figure 6.4, and 6.7.

| **Label** | $V_{\mathrm{BD},1.9}$ **(V)** | $V_{\mathrm{BD},3.0}$ **(V)** |
|---|---|---|
| V1 | −561 | −632 |
| V2 | −730 | −829 |
| V3 | −551 | −621 |
| V5 | −712 | −804 |

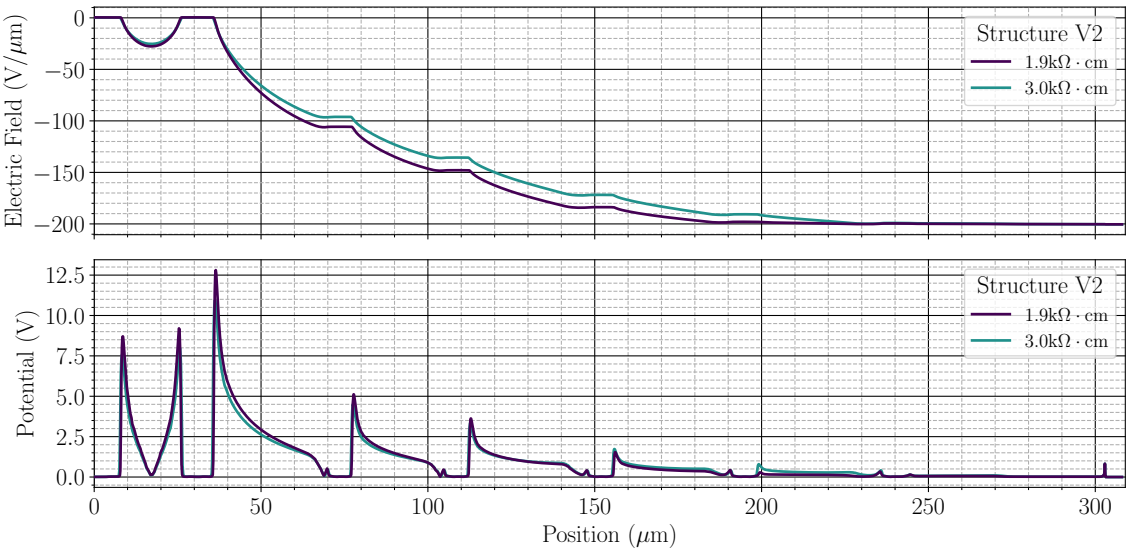



Figure 6.8: Simulated potential and electric field distribution at the deep n-well of structure V2 with the resistivity of $1.9\,\mathrm{k\Omega \cdot cm}$ and $3.0\,\mathrm{k\Omega \cdot cm}$. The n-ring is grounded and $V_{\mathrm{bias}} = -200\,\mathrm{V}$. The region of guard ring GR1 and GR2 is presented for a better inspection of the maximum electric field.

**Summary** According to the observations made during the measurement and simulation of the test structures submitted in 2016 (chapter 5), the presence of a floating deep n-well at the guard ring implant is hypothesised to increase the breakdown voltage. Test structures V1, V2, V3, and V5, derived from the previous structure F, were designed to investigate this hypothesis. Structure V1, serving as the reference, replicates the guard ring design of the earlier structure F. Structures V2, V3, and V5, adapted from V1, incorporate the deep n-well into their guard rings. TCAD simulations were employed to forecast their breakdown performances, leading to these conclusions:

1. *The effect of the deep n-well*
   - **Control group:** V1 & V2 & V5
   - **Conclusions & Predictions:**
     Implementing the deep n-well on the floating guard rings led to a reduction in the potential drop between the guard ring implants, smoothing the potential distribution within the guard ring region. This reduced the maximum electric field, enhancing the breakdown voltage compared to designs lacking the deep n-well. Given the largest potential drop and electric field occurs between the n-ring and GR1, utilising the deep n-well on the innermost guard rings is crucial for improved breakdown performance.
     Predicted breakdown voltage relationship: V1 < V5 $\lesssim$ V2
2. *The effect of the overhang with a deep n-well*
   - **Control group:** V2 & V3
   - **Conclusions & Predictions:**
     The overhang reduces the overall electrostatic potential in the guard ring region and alters the local potential distribution near the guard ring implants. This increase in the maximum electric field strength leads to a lower breakdown voltage, similar to structures with a standard n-well.
     Predicted breakdown voltage relationship: V3 < V2
3. *The influence of bulk resistivity*
   - **Control group:** 1.9 k$\Omega \cdot$ cm & 3.0 k$\Omega \cdot$ cm Bulk resistivity
   - **Conclusions & Predictions:**
     A higher bulk resistivity correlates with a higher breakdown voltage for the same guard ring design, due to a reduced maximum electric field.
     Predicted breakdown voltage relationship: $V_{\mathrm{BD},1.9} < V_{\mathrm{BD},3.0}$

The 2D simulation of structure V4 (shown in Figure 6.1) is not applicable due to differences in the layout of the corners. However, a related study on the electric field at corners of ring-shaped implants [78] using TCAD 3D simulations found that chamfered corners exhibit higher electric fields than rounded corners. Since V4's implant structure is identical to V1's, it is predicted that V4's breakdown voltage will be lower than V1's reference structure. Thus, according to simulation results summarised in Table 6.2, the predicted relationship between the breakdown voltages of the different guard ring designs is

$$(\mathrm{V4} <)\mathrm{V3} \lesssim \mathrm{V1} < \mathrm{V5} \lesssim \mathrm{V2}\,.$$

Measurement results on the fabricated test structures will be presented in the next chapter to validate these predictions.

### 6.1.3 Measurements of the breakdown voltage

Four samples (GRD1 and GRD2 with bulk resistivity of 1.9 kΩ · cm, GRD3 and GRD4 with bulk resistivity of 3.0 kΩ · cm) were used to assess the breakdown performance of the guard ring designs. Figures 6.9 and 6.10 show the IV curves of test structures V1, V2, V3, and V5. The leakage current remained stable below 1 nA until the bias voltage reached approximately −300 V to −400 V, where a rapid increase in current was observed. For a bulk resistivity of 1.9 kΩ · cm, the swift rise in current for structures V1 (reference) and V3 (full deep n-well with overhang) occurred at $V_{\text{bias}} \approx -350$ V, marking the breakdown voltage.

For structures V2 (full deep n-well) and V5 (deep n-well at inner guard rings), the rise in current comprised two phases. The initial phase began at $V_{\text{bias}} \approx -400$ V with leakage currents increasing by approximately three orders of magnitude to about 1 µA. Further ramping of the bias voltage led to a change in the slope of the IV curve, indicating a more rapid increase in leakage current and marking the second phase. This two-phase increase in current was even more evident in samples with a 3.0 kΩ · cm bulk resistivity. In these samples, the initial current rise for structures V2 and V5 started at $V_{\text{bias}} \approx -300$ V, reaching around 10 µA. Additionally, structure V1 also exhibited this two-step current increase.

10 µA can serve as the reference current for extracting breakdown voltages (Table 6.3), given that this current level corresponds to the nearly vertical portion of the IV curves for all test structures. The correlation between the breakdown voltages of the test structures in the table corroborates the simulation predictions discussed previously. Voltage probing at the floating guard rings at $V_{\text{bias}} = -200$ V also corroborates the potential distributions simulated by TCAD. Figure 6.11 presents the measured

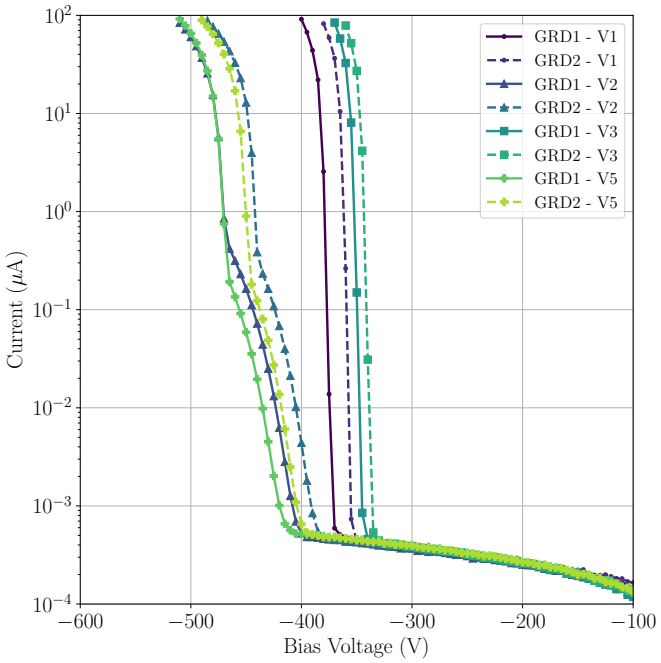



Figure 6.9: Measured IV curves of the guard ring test structures of the RD50-MPW3 submission on the wafer with 1.9 kΩ · cm substrate resistivity.

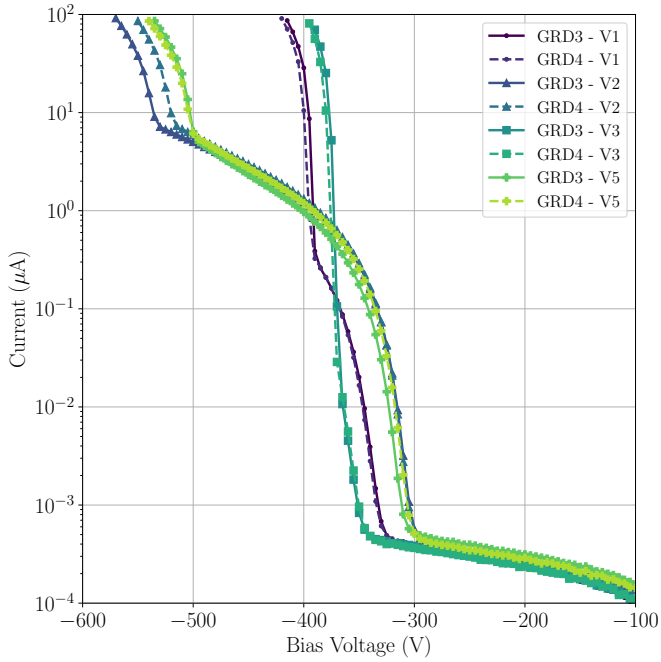



Figure 6.10: Measured IV curves of the guard ring test structures of the RD50-MPW3 submission on the wafer with 3.0 kΩ · cm substrate resistivity.

Table 6.3: Measured breakdown voltages of the test structure V1, V2, V3, and V5 with grounded n-ring. $V_{\mathrm{BD,1.9}}$ represents the breakdown voltage of the test structures with a bulk resistivity of 1.9 kΩ · cm, and $V_{\mathrm{BD,3.0}}$ represents the breakdown voltage for the bulk resistivity of 3.0 kΩ · cm. The values are the voltages where the leakage current reaches 10 µA in Figure 6.9 and 6.10.

| **Label** | $V_{\mathrm{BD,1.9}}$ **(V)** | $V_{\mathrm{BD,3.0}}$ **(V)** |
|---|---|---|
| V1 | −373 ± 11 | −398 ± 5 |
| V2 | −463 ± 16 | −530 ± 9 |
| V3 | −353 ± 7 | −378 ± 5 |
| V5 | −468 ± 11 | −503 ± 5 |

potential distribution. As anticipated by the simulations (Figure 6.6), the floating guard rings equipped with deep n-wells exhibit a heightened potential relative to those with standard n-wells, as evidenced by the comparison between structures V1 and V2. The resultant potential distribution following the implementation of deep n-wells is more smooth, with a notably reduced potential drop between the n-ring and GR1. The dampening effect of the overhang structure is evident when comparing structures V2 and V3. Despite the use of deep n-wells across all guard rings in V3, the potential distribution more closely resembles that of structure V1, where only standard n-wells are utilised. Structure V5, which features deep n-wells on the innermost two guard rings, also shows an elevated potential at these rings. When compared to structure V2, the potentials in the inner section of the guard ring region are similar. Nonetheless, as one progresses towards the outer part of the guard ring region, the potentials in V5 drop below those in V2 due to the diminished depth of the n-well implantation. These characteristics of the potential distributions across these guard ring designs elucidate the observed relationships in breakdown voltages.

Although the TCAD simulation here successfully predicted the relations between the breakdown voltages and the potential distributions of the guard ring structures, the 2-stage current increase observed for V2 and V5 is not reproduced. As discussed in section 5.5.2, the increase in leakage

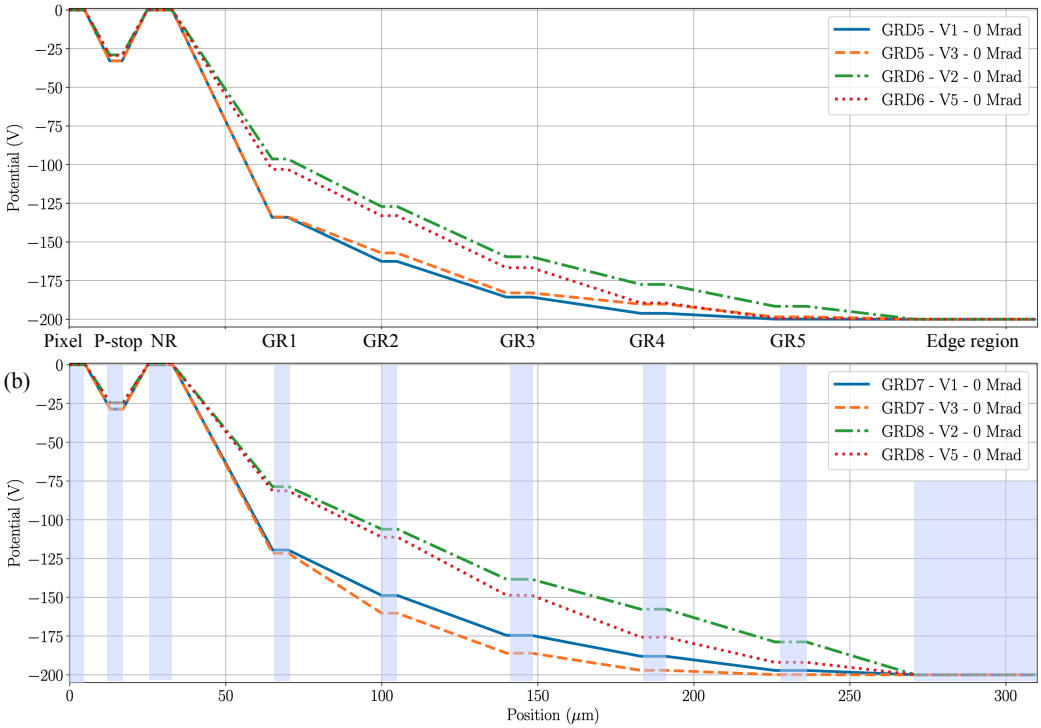



Figure 6.11: Measured potential distributions of structure V1, V2, V3, and V5 with the resistivity of 1.9 kΩ · cm and 3.0 kΩ · cm. The voltage probing only provides the potential at the guard ring implants, which are indicated by the plateaus, and the position and the width of the implants are indicated by the shaded pillar in the diagram. The inter-plateau lines are only for guiding the eye. The diagrams are obtained for grounded n-ring, and $V_{\text{bias}} = -200\,\text{V}$.

current in TCAD simulations can typically be explained by impact ionisation, carrier tunnelling, and carrier generation via defect energy levels in the band gap. Since the measured potential distributions align well with the simulations and the sample is unirradiated, the 2-stage increase in leakage current observed in the measurements is unlikely to be caused by the above physical effects. A possible source of the discrepancy is the lack of backside processing. It was introduced in section 5.3.1 that an unprocessed or imperfectly processed backside of the chip can cause such a current increase when the sensor bulk is fully depleted. The sign associated with the backside problem is the different bias voltage at which the first stage of the current increase occurred for both resistivities. The hypothesis for the 2-stage current rise is that the first stage represents the leakage current from the untreated backside when the depletion region extends to the backside, and the second stage represents the actual junction breakdown.

According to equation 2.11, the full depletion voltage for the test structure (with a 270 µm thick sensing volume [3]) is about 394 V for $\rho = 1.9\,\mathrm{k\Omega \cdot cm}$ and 249 V for $\rho = 3.0\,\mathrm{k\Omega \cdot cm}$. For the low resistivity case, the bias voltage at which the first stage of current rise begins matches the calculated full depletion value quite closely. However, for the high resistivity case, the current rise occurs at a higher bias voltage than the full depletion voltage. To further investigate this effect, it would be interesting to determine whether this current originates from the diode's guard ring region. The current from the diode and the grounded n-ring were measured separately and simultaneously on two samples, whose IV curves are shown in Figure 6.12. In the direct breakdown test structures (V1 and V3), the total current is predominantly composed of the n-ring current, indicating that the breakdown occurs in the guard ring region. This result is consistent with the conclusion from the simulation that the breakdown occurs at the n-ring when it is grounded. However, in the guard ring structures

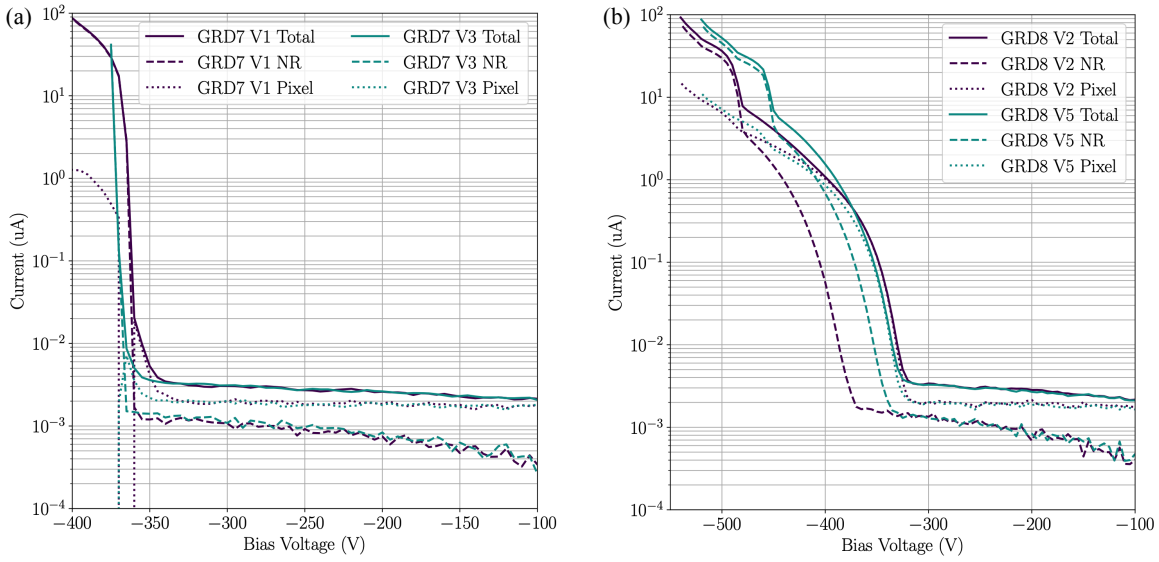



Figure 6.12: Measured IV curves (a) for direct (V1 and V3) and (b) 2-stage (V2 and V5) current increase. The total current, n-ring current, and diode current of the test structures on high resistive substrate are presented in the diagrams.

[3] The total thickness is 280 µm, and the thickness of the sensitive volume (to be depleted) can be estimated by subtracting the implants and metal layers, approximately 10 µm

with a 2-stage current rise (V2 and V5), the total current in the first stage of the current rise consists mainly of the diode current. Comparing the current contributions from the N-ring and the diode at the same bias voltage, a difference of approximately one order of magnitude can be identified. When the leakage current reaches the second stage, the contribution from the n-ring begins to dominate. Eventually, the total leakage current in the second stage is primarily driven by the n-ring current, while the diode current remains about an order of magnitude smaller. Therefore, the second stage (or, by assumption, the actual junction breakdown) also occurs at the n-ring.

Further analysis suggests that the current contributions from the diode and the n-ring can be explained by the growth of the depletion zone. As shown in Figure 6.13, the depletion zone expands in a hemispherical shape (visualised as a semicircle in cross-sectional view), with the area beneath the diode experiencing the deepest depletion as the bias voltage increases. Assuming that the entire backside of the sensor is uniformly covered with lattice defects, which enhance carrier generation, the carriers are predominantly recombined in the undepleted bulk before the depletion region reaches the backside. When the bias voltage approximates the full depletion voltage, the depletion region beneath the diode reaches the backside first, causing the initial stage of leakage current to rise as the electric field in the depletion zone draws defect-generated carriers from the backside surface. However, the depletion depth below the n-ring and the guard ring region still does not reach the backside, thus the generated carriers are not collected by the n-ring. With increasing bias voltage, the depletion zone in the guard ring region expands and eventually reaches the backside of the sensor, leading to an increase in current at the n-ring after a similar effect has occurred at the diode. When the bias voltage is sufficiently high, impact ionisation begins at the n-ring, culminating in junction breakdown, which marks the second stage of current rise.

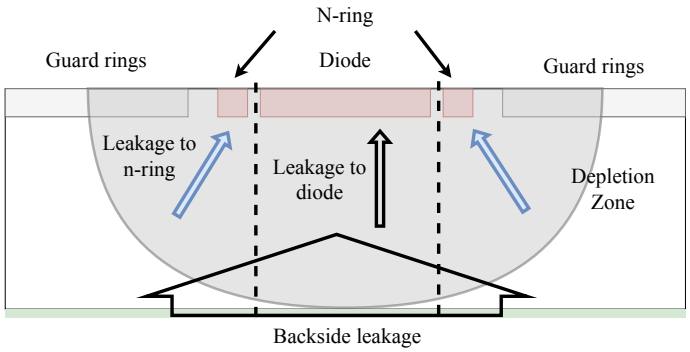



Figure 6.13: Assumption for the origin of the 2-stage current increase.

**Summary** Measurements of the current-voltage characteristics and potential distribution of the guard ring test structures validated the conclusions of the TCAD simulations. Specifically, the implementation of the deep n-well at the floating guard rings, particularly at the innermost guard rings, effectively smoothed the potential distribution across the guard ring area. Consequently, the deep n-well has proven to be advantageous for enhancing the breakdown voltage of passive CMOS test structures. However, an anomalous two-step current increase was noted in the measured IV characteristics. This phenomenon is influenced by the guard ring design and substrate resistivity and is suspected to stem from the unprocessed backside of the sensor, which may contain a high density of crystal defects generating charge carriers.

## 6.2 Improve the Breakdown Performance of the DMAPS prototype RD50-MPW3: Towards RD50-MPW4

In the DMAPS prototype RD50-MPW3, the bias voltage was designed to be applied between the p-stop and the deep n-well charge collection electrode. Given the proximity (several µm), the breakdown voltage of this sensor was limited to approximately −150 V [79]. With a thickness of 280 µm and substrate resistivity of $\leq 3.0\,\mathrm{k\Omega \cdot cm}$, it is not possible to fully deplete the sensitive volume of the RD50-MPW3 before reaching breakdown, which could significantly impair the signal detection during particle interaction. Enhancing the breakdown voltage is thus crucial for achieving full depletion in the RD50-MPW3 prototype.

The principal challenge with the RD50-MPW3 lies in its biasing method. As explored in the preceding chapter on passive CMOS test structures, employing an edge/frontside bias allows the potential drop to occur predominantly over the guard ring region. Consequently, the potential difference between the p-stop and the pixel implants remains minimal over a short distance, while the depletion region extends considerably due to the elevated breakdown voltage. This biasing strategy has been adopted in the development of its successor, the RD50-MPW4 DMAPS prototype. During the design phase of the RD50-MPW4, the sensor architecture of the RD50-MPW3 was meticulously reviewed to assess the viability of utilising edge biasing and to identify design elements that could potentially limit breakdown performance. Improvements were explored through TCAD breakdown simulations.

### 6.2.1 The Floor Plan of RD50-MPW3: Inspection of the Layout

The RD50-MPW3 chip comprises a 64 × 64 pixel matrix along with its digital periphery as part of the readout chain. As illustrated in Figure 6.14, the main body of the chip is encircled by an irregular-shaped floating p-well, which hosts the bonding pads and several on-chip test structures. The sensor's guard ring, also known as the chip ring, forms the outermost boundary of the chip. The

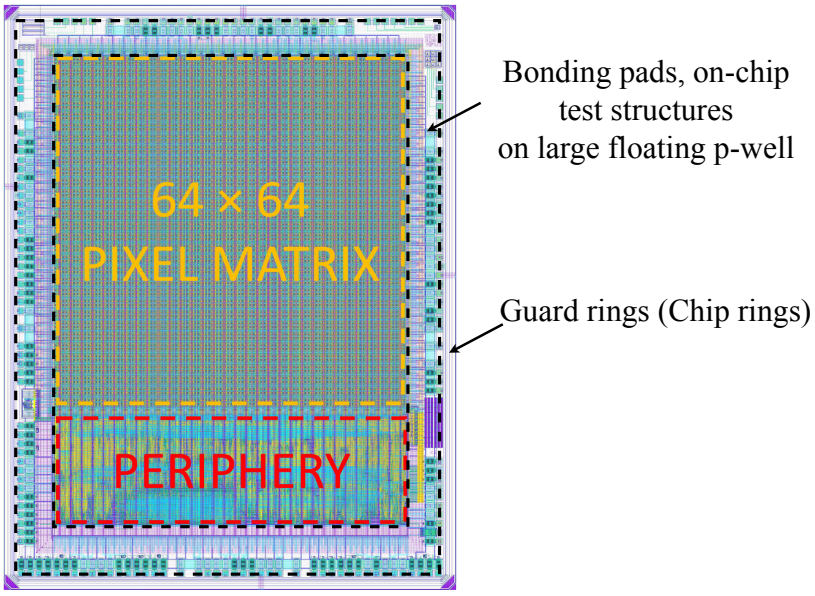



Figure 6.14: The floor plan of the DMAPS prototype RD50-MPW3.

principal analysis involved evaluating the potential distribution from the pixel matrix's collection electrode to the chip's edge to ascertain the viability of edge biasing for achieving adequate breakdown voltage. The primary goal in design optimisation was to modulate the potential distribution by altering the implant layout to mitigate high electric fields.

Among various design elements that could limit breakdown voltage under edge biasing, the most notable feature in the RD50-MPW3's passive design is the expansive floating p-well and the surrounding guard ring. Excluding the bonding pads and in-chip test structures, Figure 6.15 provides a sectional view of the typical region between the pixel matrix and the chip's edge. Unlike the configurations discussed in the previous chapter, the n-ring is separated with the pixel matrix by the p-stop and the floating p-well. Two n-ring biasing scenarios were assessed during the tests, with breakdown voltages of approximately $-120$ V for the grounded n-ring and approximately $-150$ V for the floating n-ring [79]. The potential drops for these scenarios, derived from the simulation results of the previous chapter, are indicated by arrows in Figure 6.15. In the floating n-ring scenario, the potential descends from the grounded pixel collection electrode to the sensor's edge, which is at the bias potential. Conversely, in the grounded n-ring scenario, a potential sink exists at the floating p-well, and the potential declines from the n-ring to the sensor's edge.

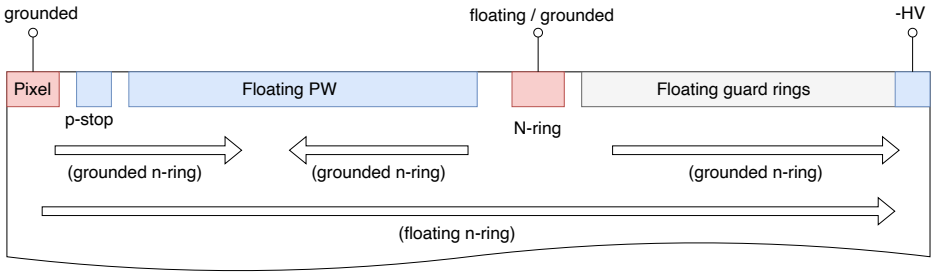



Figure 6.15: The section view of the region between the pixel matrix and the chip's edge of RD50-MPW3.

The potential and electric field distributions for the structure depicted in Figure 6.15 were obtained using TCAD simulations. The distributions at the surface of the structure for a $V_{\text{bias}} = -100$ V, with both floating and grounded n-ring configurations, are illustrated in Figure 6.16. In the scenario with the floating n-ring, the potential abruptly falls to the bias potential just outside the p-stop implant, suggesting that the sensor bulk beneath the large floating p-well and the guard ring region remains undepleted. This rapid potential transition induces a peak in the electric field at the edge of the pixel implant, which is a likely site for breakdown. Grounding the n-ring elevates the potential beneath the guard ring region, establishing a potential gradient that declines from the n-ring implant to the sensor's edge. Despite this, the floating p-well remains at the bias potential, and a significant electric field develops at the edge of the n-ring due to the guard ring's configuration.

The simulated IV curves in Figure 6.17 show that the breakdown voltage for the floating n-ring is higher than that for the grounded n-ring. The reason for this can be deduced from the electric field distribution (Figure 6.16), where the maximum electric field in the grounded n-ring case is higher than that in the floating n-ring case. Therefore, as the bias voltage increases, the electric field at the grounded n-ring will be the first to reach the avalanche generation threshold and trigger the junction breakdown. These observations show that the guard ring design and the floating p-well create a high electric field that limits the breakdown voltage of the sensor.

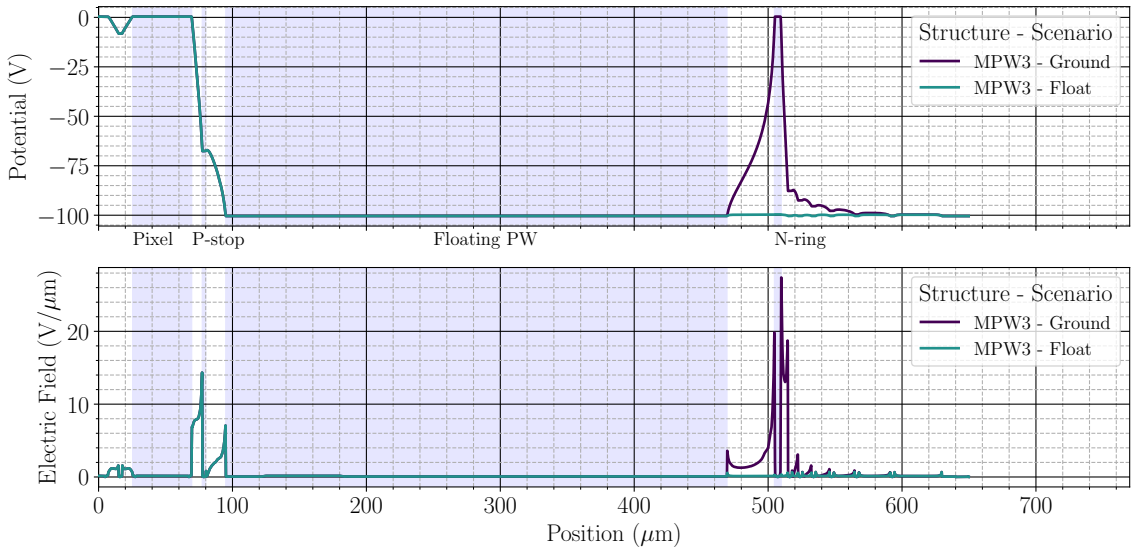



Figure 6.16: Simulated potential and electric field distribution at the surface of the RD50-MPW3 sensor structure. The 2D simulation domain is similar to that depicted in Figure 6.15, and is established according to the design data. The distributions are obtained for $V_{\text{bias}} = -100\,\text{V}$ with a floating and grounded n-ring scenarios (indicated in the legend).

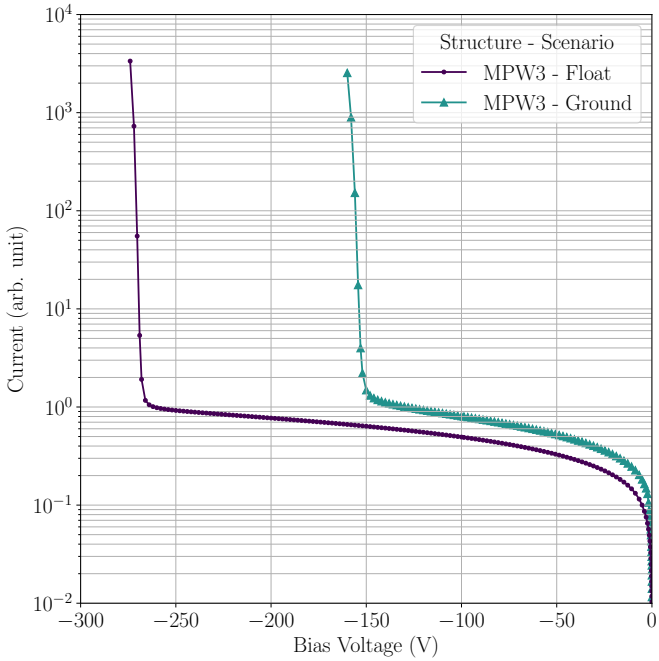



Figure 6.17: Simulated IV curve of the RD50-MPW3 structure with floating and grounded n-ring.

### 6.2.2 Guard Ring Design

The limitations of the original guard ring design were highlighted in the previous section. The narrow gap between the N-ring and the first guard ring, the exclusive use of p-type implants, and the chamfered corners of the guard rings resulted in a steep potential drop and a high electric field at the N-ring, subsequently restricting the breakdown voltage. To address these issues, guard ring design V5, depicted in Figure 6.2, was implemented.

Figure 6.18 displays the simulated potential and electric field distribution for the MPW3 periphery structure incorporating the V5 guard ring design. With the n-ring grounded, this new guard ring configuration effectively smoothes the potential distribution across the guard ring region, significantly mitigating the initially high electric field. Nevertheless, the large floating p-well consistently aligns with the bias potential in all scenarios (as also shown in Figure 6.16), indicating that the area beneath the p-well remains undepleted. Consequently, regardless of the guard ring design or the n-ring's connection status, there persists a peak in the electric field at the pixel implant. The simulated IV curves (Figure 6.19) verify that while the new guard ring design can enhance the breakdown voltage for cases where the n-ring is grounded, the ultimate breakdown voltage is still constrained by the potential at the floating p-well. Hence, the resultant breakdown voltage parallels that of the original guard ring design with a grounded n-ring (Figure 6.17).

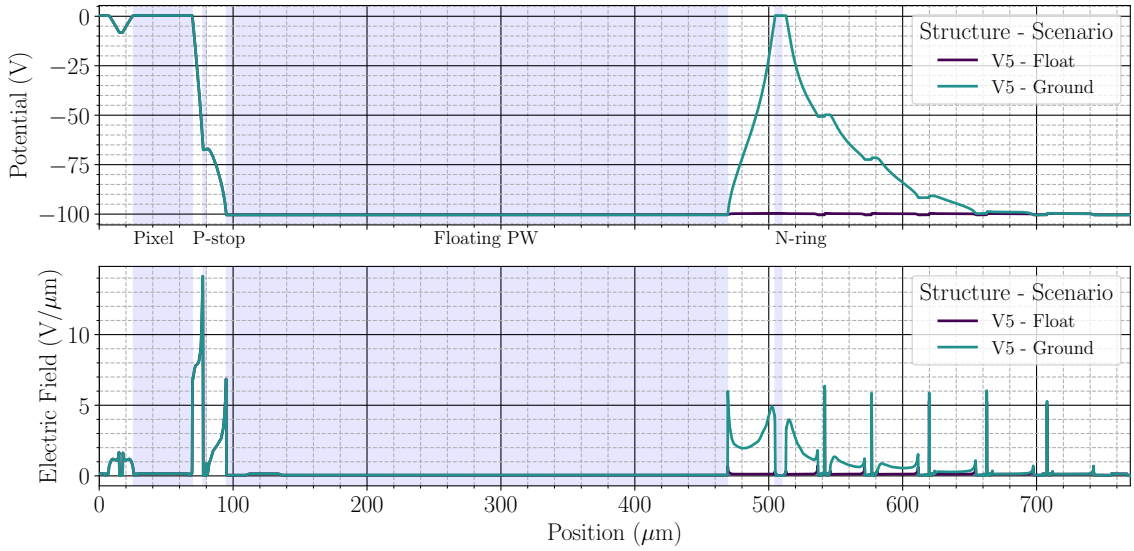



Figure 6.18: Simulated potential and electric field distribution at the surface of the RD50-MPW3 sensor structure with guard ring structure V5 in Figure 6.2. The 2D simulation domain is similar to that shown in Figure 6.15 and is constructed according to the design data. The distributions are obtained for $V_{\text{bias}} = -100\,\text{V}$ with floating and grounded n-ring scenarios (indicated in the legend).

### 6.2.3 Influence of the Floating PW

As detailed in the previous chapter, the floating p-well (guard ring), positioned between the n-ring/pixel and the sensor's edge, assumes a specific potential once an adequate bias is applied. This potential is

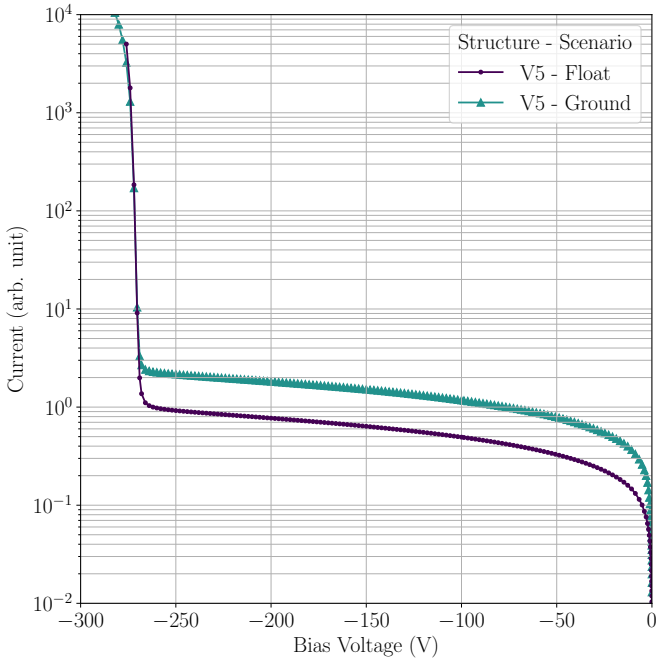



Figure 6.19: Simulated IV curve of the RD50-MPW3 structure using the guard ring design V5 with floating and grounded n-ring.

integral to the total potential drop at the pixel matrix's periphery and plays a crucial role in determining the maximum electric field, which in turn impacts the breakdown performance. During the simulation of the RD50-MPW3 sensor design, it was observed that the potential at the large floating p-well is difficult to alter from the bias potential, resulting in a steep potential drop between the floating p-well and the grounded pixel electrode. This behaviour suggests that the potential at a floating p-well is influenced by the size of the implant. Figure 6.20 illustrates the potential distribution for a dummy sensor periphery structure, analogous to that in RD50-MPW3, featuring various floating p-well widths. When the n-ring is left floating, a wider p-well width results in a lower potential at the same bias voltage. This configuration steepens the potential drop between the grounded pixel implant and the p-well, consequently increasing the electric field at the pixel. Despite grounding the n-ring in the given simulation geometry, the potential of the varying floating p-well remains generally elevated. Nonetheless, the relationship between the potential and the width of the p-well persists. This explains the observed difficulty in depleting the region beneath the large p-well in simulations of the RD50-MPW3 sensor, even with a grounded n-ring.

Eliminating or reducing the size of the p-well isn't a viable option for transitioning from RD50-MPW3 to MPW4, as this area is necessary for bonding pads and metal routing for the electronics components. Instead, the optimisation approach focused on modifying the implantation in this region while minimally altering the prototype's floor plan. The goal is to increase potential and enhance depletion, thereby reducing the potential difference and electric field. Given the necessity for bonding pads in this region, employing a large grounded deep n-well proves to be an effective solution for maintaining a smoother potential distribution. Additionally, the bonding pads benefit from the

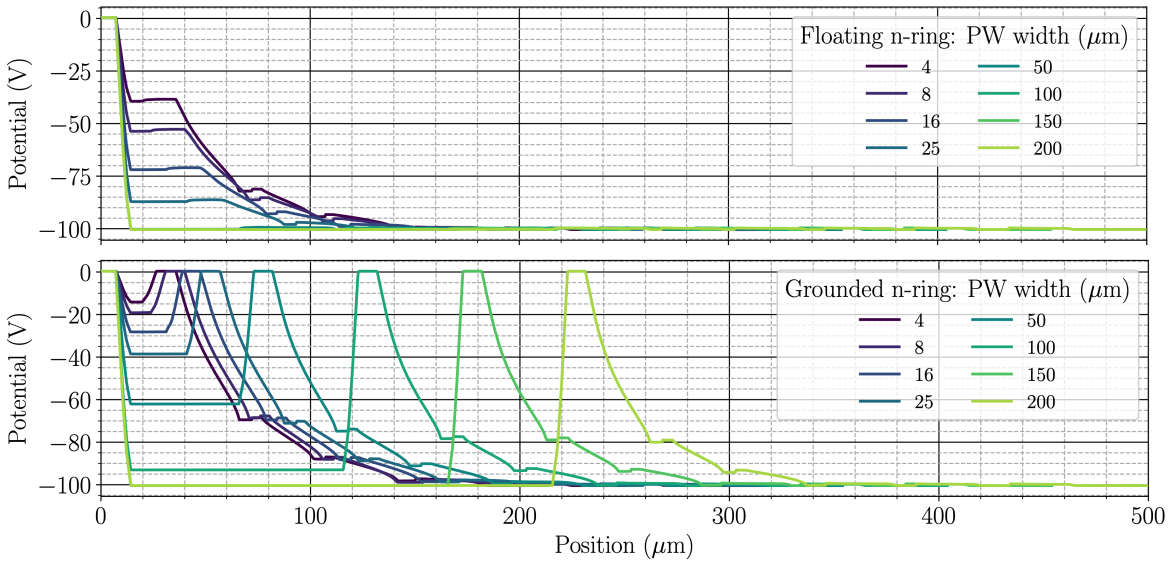



Figure 6.20: Simulated potential distribution of a sensor periphery structure with floating (top) and grounded n-ring (bottom). The distributions are obtained at $V_{\text{bias}}$ for different p-well widths. This diagram can be interpreted based on Figure 6.16. The guard ring structure V1 (Figure 6.2) is used for demonstration. A lower potential is found at a wider floating PW for both scenarios. It means that the region beneath a large floating PW is harder to be depleted in comparison with smaller PW, so that a larger potential drop is formed between the grounded pixel implant and the PW.

shielding provided by the deep n-well. Figure 6.21 depicts the schematic section view of the sensor periphery region designed for the RD50-MPW4, where a deep n-well replaces the floating p-well in the MPW3 prototype. This deep n-well is set at the same potential as the pixel electrode during operations. The potential distribution for this modification is shown in Figure 6.22. With a grounded large deep n-well and a grounded n-ring, the electric field is significantly reduced compared to the case with a floating p-well, resulting in the potential drop primarily occurring in the guard ring region.

The breakdown simulation provides IV curves for both the modified design (featuring grounded DNW, grounded n-ring, and new guard rings) and the existing structure in MPW3, as illustrated in Figure 6.23. Under identical simulation conditions, the breakdown voltage shows significant enhancement with the new periphery design compared to that of the RD50-MPW3 chip.

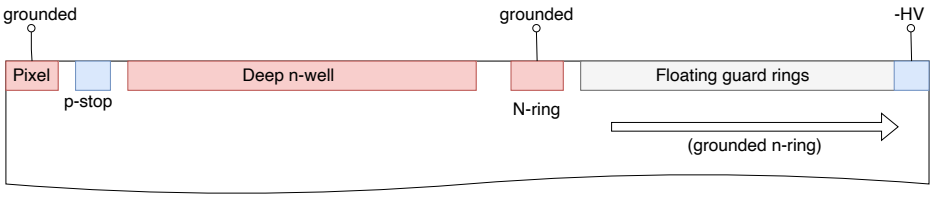



Figure 6.21: The section view of the region between the pixel matrix and the chip's edge of RD50-MPW4.

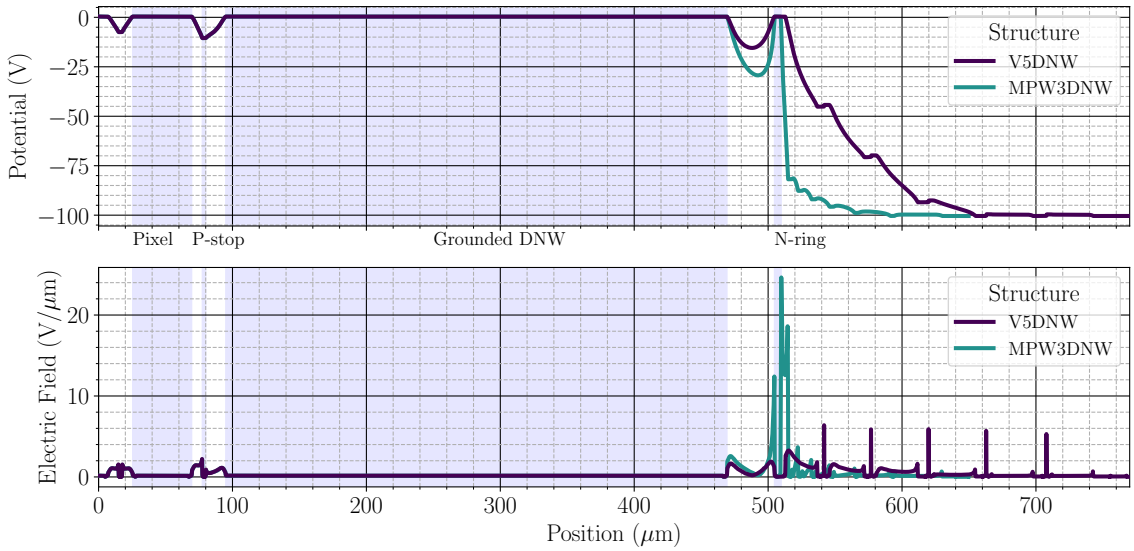



Figure 6.22: Simulated potential and electric field for the structure with floating p-well and grounded deep n-well.

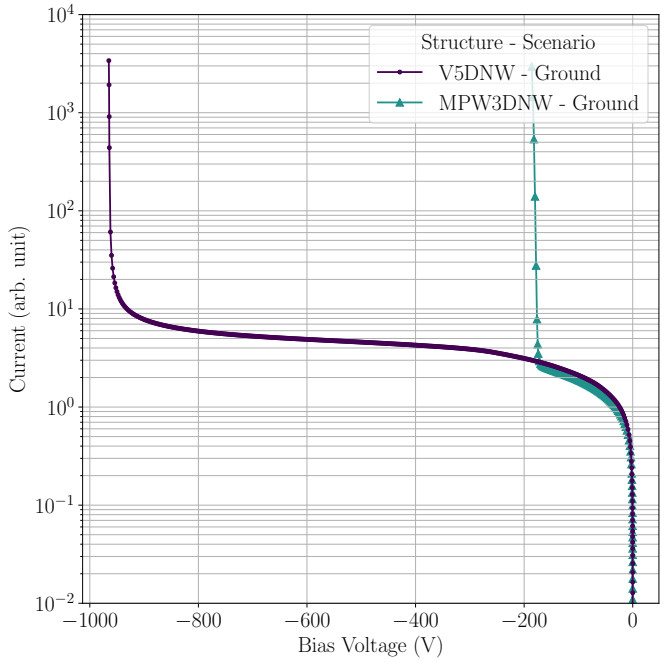



Figure 6.23: Simulated IV curves for the structure with floating p-well and grounded deep n-well.

## 6.3 Chapter Conclusion

The sensor development linked to the RD50-MPW submissions encompasses two primary objectives: exploring guard ring designs and advancing the DMAPS prototype RD50-MPW4 to enhance breakdown voltage. Building upon insights from Chapter 5, this chapter focused on evaluating the effects of deep n-wells (DNW) on the breakdown performance of silicon pixel sensors. TCAD simulations illustrate that DNWs at floating guard rings significantly elevate their electrostatic potential compared to standard n-well implants. This elevation leads to a smoother potential transition from the ground potential at the pixel or n-ring to the high negative voltage at the sensor's edge, effectively reducing the electric field at crucial junctions, particularly between the n-ring and the innermost guard ring. Guard ring designs incorporating DNWs fully (structure V2) and only in the inner two rings (structure V5) show similar breakdown voltages, about 200 V higher than designs with standard n-wells, a finding supported by empirical data from fabricated test structures.

The DMAPS prototype RD50-MPW3 suffers from a low breakdown voltage ($\lesssim 150$ V), insufficient for fully depleting the sensor substrate. This limitation stems from two design choices: the method of applying bias voltage at the p-stop implant between pixels, which restricts the breakdown voltage due to narrow spacing, and an ineffective peripheral design for edge biasing which could otherwise permit a higher breakdown voltage. Examination and simulation of the sensor layout identified high electric fields generated by the guard ring design and the extensive floating p-well surrounding the chip's main body. Notably, it's challenging to deplete the substrate beneath this large p-well, resulting in a steep potential gradient between the pixel implant and the p-well. To address these issues, the guard ring structure V5 from test structures has been adopted, and the floating p-well has been replaced with a deep n-well aligned in potential with the pixel electrode during operation. These modifications have markedly diminished the electric field strength, as demonstrated in the potential and field distributions, and have been incorporated into the RD50-MPW4 prototype.

CHAPTER 7

# Improving Spatial Resolution through Sub-pixel Cross-coupling

The main content of this chapter has been published in the journal Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment in 2020 with the title *Improving the Spatial Resolution of Silicon Pixel Detectors through Sub-pixel Cross-coupling* [46].

Thin planar silicon sensors are at the forefront of technology for next-generation pixel detectors due to their minimal material use, low power consumption, and high radiation tolerance. The ongoing upgrades of the ATLAS and CMS experiments incorporate sensors with thicknesses of 100 µm and 150 µm for hybrid pixel-detectors [80, 81], while a 50 µm sensor is being explored for the future Compact Linear Collider (CLIC) [82]. However, a notable drawback of reducing sensor thickness, while maintaining the same pixel pitch, is the decreased cluster size, which compromises spatial resolution [83]. In thin sensors, the shorter drift distance of charge carriers generally results in shorter drift times compared to thicker sensors, reducing lateral charge diffusion and suppressing charge sharing between adjacent pixels. This issue is exacerbated after extensive radiation exposure, where charge carrier trapping and increased readout thresholds further diminish cluster size. Addressing this issue by reducing pitch size entails substantial redesign of readout electronics and faces physical limits from charge digitisation electronics integration (both hybrid and monolithic detectors) and the minimum bump-bonding pitch (for hybrid detectors). A novel approach for strip sensors involves buried, highly doped n- and p-type implants between strips to enhance lateral electric fields and guide charge carriers sideways, known as Enhanced LAteral Drift (ELAD) sensors [84], though their fabrication requires complex specialized processes not aligned with standard commercial CMOS processes. Additionally, exploiting capacitive coupling between readout electrodes for charge distribution has been extensively explored for strip detectors [85, 86] and recently for pixel detectors [87, 88].

This chapter introduces a concept to improve the spatial resolution of pixel detectors by enabling directional charge sharing between sub-divided pixels through sub-pixel cross-couplings. Here, the design employs a $3 \times 3$ pixel matrix, each with a pitch of $50\,\mu\text{m} \times 50\,\mu\text{m}$, to investigate the impact on spatial resolution from varying charge sharing strengths. The sensor assumes a 100 µm thick p-type substrate with a resistivity of $2\,\text{k}\Omega \cdot \text{cm}$, which is consistent with the specifications for

the inner tracker upgrades of the ATLAS and CMS experiments at the LHC. Simulations consider charge-cloud evolution, energy-loss straggling, electronic noise, and charge detection thresholds. Despite simplifying assumptions like perpendicular particle tracks and absence of gaps between charge-collection electrodes, the results show a potential improvement in spatial resolution by up to approximately 30% compared to conventional pixel layouts. Additionally, the feasibility of this directional charge sharing concept using AC-coupling between (sub-) pixels is discussed.

## 7.1 The Model of the Sub-pixel Cross-coupling

The sub-pixel concept involves subdividing the charge collection electrode of a conventional pixel cell into four isolated electrodes, as illustrated in Figure 7.1 (a). The model assumes no gaps between these electrodes, equating to a fill factor of 100% with parallel electric field lines. Each sub-pixel's collected signal within a pixel cell is transmitted to the pixel's readout electronics for further processing. Thus, the total charge processed by the readout electronics for each conventional pixel cell equals the sum of the charges collected by its sub-pixels. The objective of cross-coupling is to directionally distribute the charge collected by a conventional pixel to its adjacent pixels, where "directionally" implies that the charge sharing reflects the position of the incident charge cloud. This coupling is executed between a sub-pixel of one pixel cell and the adjacent sub-pixel of an adjacent cell, enabling the charge sharing configuration shown in Figure 7.1 (b). For example, if a charge cloud ($Q_0$) forms at the sub-pixel E-1 of pixel cell E, the charge is shared exclusively with sub-pixel D-3 through cross-coupling by the "charge sharing fraction" $k$. Consequently, $(1-k)Q_0$ is collected by E-1, and $kQ_0$ by D-3.

In a realistic scenario, the dimension and evolution of the charge cloud are critical, particularly when a finite-width charge cloud covers multiple sub-pixels, as depicted in Figure 7.2 for demonstration with a significantly large charge cloud. For simplicity, the charge cloud is assumed to originate from a minimum ionising particle (MIP) traveling perpendicularly to the sensor plane, ignoring delta-electron effects. The drift time of the charge carriers depends on their creation distance from the collection

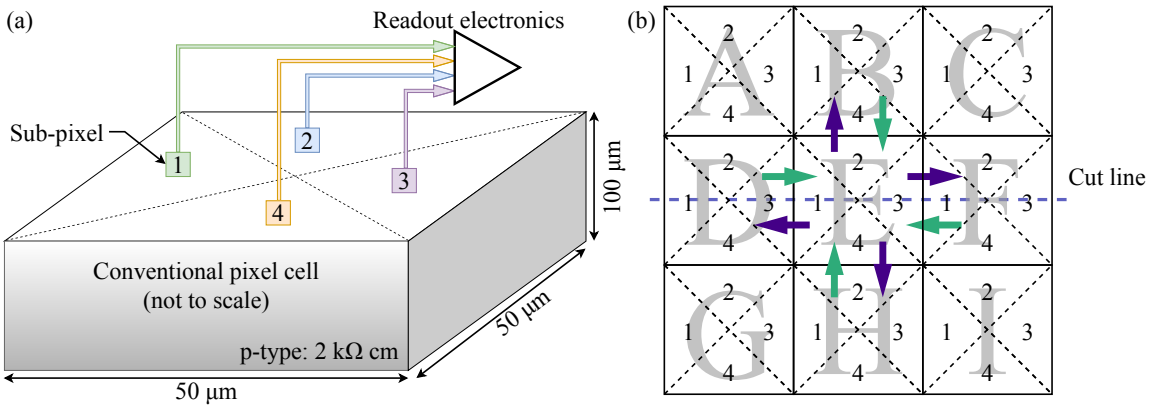



Figure 7.1: The model of the sub-pixel cross-coupling. (a): The signal from the sub-pixels (labelled with "1" to "4") within a single pixel cell are collected by the same readout node of the pixel cell. (b): The pixel cells in a $3 \times 3$ matrix are labelled by the letters "A" to "I". The cross-coupling takes place between the adjacent sub-pixel of the adjacent pixel cell, and the charge is shared between the coupled sub-pixels (indicated by the arrows). The "Cut line" indicates the position of the section view which is presented in the next section.

electrode, hence the charge cloud evolution is governed by equation 3.10. Assuming a symmetrical 2D Gaussian distribution for the charge cloud (equation 3.16), the effective width of the charge cloud is calculated as

$$\bar{\sigma} = \frac{1}{d}\int_0^d \sigma(z)\mathrm{d}z \,. \tag{7.1}$$

The charge collected by each sub-pixel is estimated by integrating the charge cloud distribution over the sub-pixel area after drift, described as

$$Q_{\text{sub-pix.}} = \int_{\text{area}} \text{CCE}\cdot\rho\,\mathrm{d}x\,\mathrm{d}y \tag{7.2}$$

$$\text{with } \rho = \frac{Q_0}{2\pi\bar{\sigma}^2}\exp\left[-\frac{(x-\xi)^2+(y-\zeta)^2}{2\,\bar{\sigma}^2}\right] . \tag{7.3}$$

Here, $Q_0$ is the total charge generated by a MIP at position $(\xi, \zeta)$, and CCE is the charge collection efficiency introduced in section 3.2.2. Referring to Figure 7.2, the charge cloud overlaps sub-pixels D-3, E-1, E-2, E-3, and E-4. Without cross-coupling, only pixels D and E collect the charge, computed by summing charges across their sub-pixels per equation 7.2. With bidirectional cross-coupling, a portion of charge $kQ_{\text{E-1}}$ from E-1 is shared with D-3, and $kQ_{\text{D-3}}$ from D-3 is transferred to E-1. Such a sharing also applies to other coupled sub-pixels, for instance between E-2 and B-4.

Hence, generalising the charge sharing process between two coupled sub-pixels ("sub-pix.1" and "sub-pix.2"), the collected charge of a sub-pixel can be calculated as

$$Q_{\text{total,sub-pix.1}} = (1-k)Q_{\text{sub-pix.1}} + kQ_{\text{sub-pix.2}} \,. \tag{7.4}$$

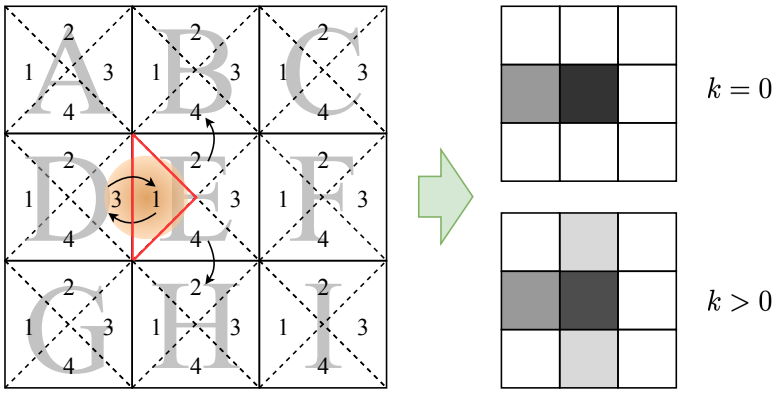



Figure 7.2: A charge cloud with a finite width created among sub-pixels (left), and the resulting collected charge at the readout channel of each conventional pixel (right). The charge cloud projected onto the sensor plane is indicated by the shaded circle. The part of the charge cloud that overlaps with the highlighted triangle (sub-pixel E-1) is considered to be the initial charge that will be collected by E-1, and the same is applied to other sub-pixels. The directional charge sharing via the cross-coupling is indicated by arrows. The resulting charge signature in this $3 \times 3$ matrix is illustrated by the greyscale. The cross-coupling ($k > 0$) increases the cluster size, in comparison with conventional pixel sensors ($k = 0$ ).

$Q_{\text{total,sub-pix.1}}$ represents the charge that is eventually collected by one sub-pixel, after the charge sharing process, consisting of:

1. the remaining portion of the initial charge $(1-k)Q_{\text{sub-pix.1}}$ after sharing the amount of charge $kQ_{\text{sub-pix.1}}$ to "sub-pix.2", where the $Q_{\text{sub-pix.1}}$ represents the charge which should be collected by the "sub-pix.1" if no cross-coupling were implemented;

2. the charge contributed by the "sub-pix.2" $kQ_{\text{sub-pix.2}}$, where the $Q_{\text{sub-pix.2}}$ is the charge initially collected by the "sub-pix.2".

The sub-pixel division and cross-coupling enhance the directional charge sharing between conventional pixels, making charge detection more sensitive to the location of the incident particle compared to a standard pixel sensor (without sub-pixel cross-coupling, where $k = 0$). Consider the charge cloud example in Figure 7.2 the charge collection of all pixels in this model with sub-pixel cross-coupling are calculated as

$$
\begin{aligned}
Q_{\text{B}} &= \sum_{i=1}^{4} Q_{\text{total,B-i}} = Q_{\text{total,B-1}} = kQ_{\text{E-2}}\,, \\
Q_{\text{D}} &= \sum_{i=1}^{4} Q_{\text{total,D-i}} = Q_{\text{total,D-3}} = (1-k)Q_{\text{D-3}} + kQ_{\text{E-1}}\,, \\
Q_{\text{E}} &= \sum_{i=1}^{4} Q_{\text{total,E-i}} = (1-k)(Q_{\text{E-1}} + Q_{\text{E-2}} + Q_{\text{E-4}}) + kQ_{\text{D-3}}\,, \\
Q_{\text{H}} &= \sum_{i=1}^{4} Q_{\text{total,H-i}} = Q_{\text{total,H-2}} = kQ_{\text{E-4}}\,.
\end{aligned}
$$

Since the charge cloud only overlaps with pixel E and sub-pixel D-3, the charge collections of pixel B, F, H are a result of the cross-couplings with the sub-pixels in pixel E. For the sub-pixels D-3 and E-1, the charges are shared bidirectionally, because both of the sub-pixels have received the charge from the charge cloud. The array, summarising pixels A to H, $(0, Q_{\text{B}}, 0, Q_{\text{D}}, Q_{\text{E}}, 0, 0, Q_{\text{H}}, 0)$ represents the charge signature of this model, and the pixels without collecting any charge is represented by "0". Due to the triangular shape of the sub-pixels, a small shift of the charge cloud position within the sub-pixel can lead to a different charge collection at the sub-pixels (see Equation (7.2)), disregarding the detection thresholds, charge fluctuations, etc. A standard pixel sensor's charge signature for the same charge cloud, when $k = 0$, would include only components for pixels D and E. In such a scenario, the movement of the charge cloud along the adjacent edge of pixel D and E affects the charge signature only if it overlaps with other pixels.

The sensitivity of the charge signature to the charge cloud's position also depends on the relative size of the charge cloud and the pixel pitch. For instance, if the charge cloud is significantly smaller than the pixel pitch [1], as illustrated in Figure 7.3, it is likely confined within a single conventional pixel cell or even a sub-pixel. Consider three different charge cloud positions:

- *a*: within sub-pixel E-1;

[1] The example in Figure 7.2 shows the case that the charge cloud diameter is comparable with the pixel pitch.

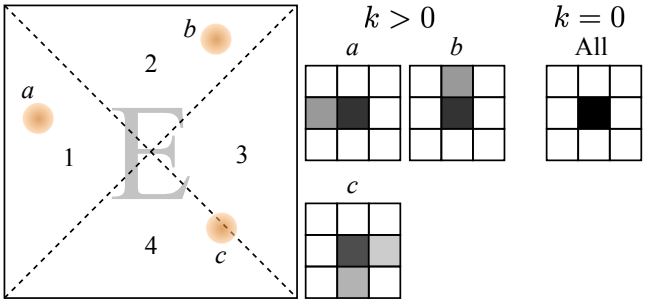



Figure 7.3: The charge signatures for a small charge cloud. A charge cloud (circle in figure) is created at 3 different positions *a*, *b*, and *c* on pixel E. For the case with sub-pixel cross-coupling ($k > 0$), three cases reveal different charge signatures in the $3 \times 3$ pixel matrix, where the amount of the charge is represented by the greyscale. However, all three charge cloud positions give only one charge signature, if no directive charge sharing is implemented ($k = 0$).

- *b*: within sub-pixel E-2;
- *c*: at the adjacent edge between sub-pixels E-3 and E-4.

In a conventional pixel sensor ($k = 0$), only the readout for pixel E [2] will register the total charge of the charge cloud for all cases. This makes distinguishing the three positions impossible. With $k > 0$, the charge at position *a* affects pixel D, and similarly, position *b* impacts adjacent pixels. For a charge cloud at position *c*, both sub-pixels E-3 and E-4 receive signals, and both pixels F and H register some charge due to sharing, allowing for distinct detection of different creation positions.

## 7.2 Simulating the Spatial resolution

A $3 \times 3$ matrix of $50\,\mu m \times 50\,\mu m$ pixels as depicted in Figure 7.1 was used for the simulation. Calculating the charge cloud dimension also requires the electric field properties, so that the drift time can be estimated. Therefore, it was assumed that the pixel matrix is on a p-type silicon substrate with a resistivity $\rho = 2\,k\Omega\,cm$ and a thickness $d = 100\,\mu m$, representing a full-depletion voltage $V_{dep}$ of approximately 50 V. Such features are consistent with the inner tracker upgrades for the ATLAS and CMS [80, 89] experiments at the future High-Luminosity Large Hadron Collider.

The simulation of the spatial resolution needs to consider three different topics:

1. charge collection with directional charge sharing,
2. hit position reconstruction,
3. estimation of the spatial resolution.

Assuming a bias voltage $V = 80\,V$, with which the sensor is fully depleted, the width of the charge cloud projection is given as $\bar{\sigma} \approx 1.6\,\mu m$, according to Equation (7.1). As introduced in the previous section, the charge collection of all pixels can then be simulated by generating the charge cloud

[2] The labelling of the pixels and sub-pixels refers to Figure 7.1 (b).

projection at certain positions on the pixel matrix. For a more realistic approach, charge fluctuations according to the Landau distribution, electronic noise, and detection threshold of the sensor and electronics were taken into account. The most probable value of the Landau distribution $Q_{0,\mathrm{MPV}}$ was considered as a reference for the total charge. A Gaussian noise with a standard deviation of 5% $Q_{0,\mathrm{MPV}}$ was added to each pixel. The detection threshold was set to 10% $Q_{0,\mathrm{MPV}}$ and 20% $Q_{0,\mathrm{MPV}}$ for illustrating the impact of the threshold on the spatial resolution. In an actual silicon pixel detector, if the collected charge is above the threshold, the charge information from the sensor undergoes digitisation according to the parameters defined by the readout electronics, as e.g. shown in [87]. This was also included in the simulation, with a charge discretisation error of 10% $Q_{0,\mathrm{MPV}}$. These values are comparable to the performance of existing pixel detectors, e.g., of the ATLAS and CMS experiments [50, 90].

The hit position reconstruction in this work adopts a template-based algorithm, similar to the technique introduced in [91]. Cluster shapes and charge information of pixel hits are pre-computed as a function of the particle hit position (referred to as templates or charge signatures), as introduced in section 3.2.2. This is used during hit-position reconstruction. The pre-computation of the template was done by simulating one million charge cloud creations from MIPs across the pixel matrix at random positions and calculating the corresponding charge signature. Despite the charge fluctuations, the thresholds, etc., the charge signatures or the layout of effective pixels can also be affected by the sub-pixel cross-coupling, where the cluster size can be increased due to directional charge sharing.

The spatial resolution was assessed via Monte Carlo method, with which one million charge depositions within a pixel are simulated. The charge signatures after digitisation were calculated and the positions were reconstructed at the centre of gravity of the corresponding effective pixel. Due to simulated electronic noise the charge signature may not exist, in which case the reconstructed position is set to the pixel centre. Therefore, the overall RMS in x or y direction for the hit positions can be calculated with Equation (3.17).

## 7.3 Realisation by Using AC-coupling and Simulation Results

A straight-forward implementation of the cross-coupling in the proposed concept is to use capacitors, i.e. AC-coupling between sub-pixels. This also requires an AC-coupling between the sub-pixels to the readout electronics of the corresponding conventional pixel cell. An equivalent circuit model is illustrated in Figure 7.4, which is sketched according to the section view of pixels along the cut line labelled in Figure 7.1. The sub-pixels within a conventional pixel cell, for instance 1 and 3 (2 and 4 are not depicted), are individually connected to the readout via coupling capacitor $C_{\mathrm{AC}}$. Therefore, the sum of their signals is received at the input of the readout electronics. The cross-coupling is realised via "inter-pixel capacitances" $C_{\mathrm{int}}$. Capacitive charge sharing also takes place between all sub-pixels via parasitic capacitance $C_{\mathrm{p}}$ and $C'_{\mathrm{p}}$. The capacitances to the backside (detector capacitance or pixel capacitance) $C_{\mathrm{d}}$ and the parasitic capacitances can be confined to small values ($\sim$ fF) by controlling the size and depth profile of the electrode implants [48]. As introduced in section 3.2.2, a high charge collection efficiency of an AC-coupled readout requires a large $C_{\mathrm{AC}}$ in comparison with $C_{\mathrm{d}}$. For instance, $C_{\mathrm{AC}}$ is typically in the order of $\sim$ 100 fF or even a few pF. Therefore, the inter-pixel capacitance must be sufficiently large to induce enough charge on the adjacent readout channel.

The relation between the charge sharing fraction $k$ and the inter-pixel coupling capacitance $C_{\mathrm{int}}$ was be estimated via analytical calculations and SPICE [92] transient simulation. As depicted in Figure

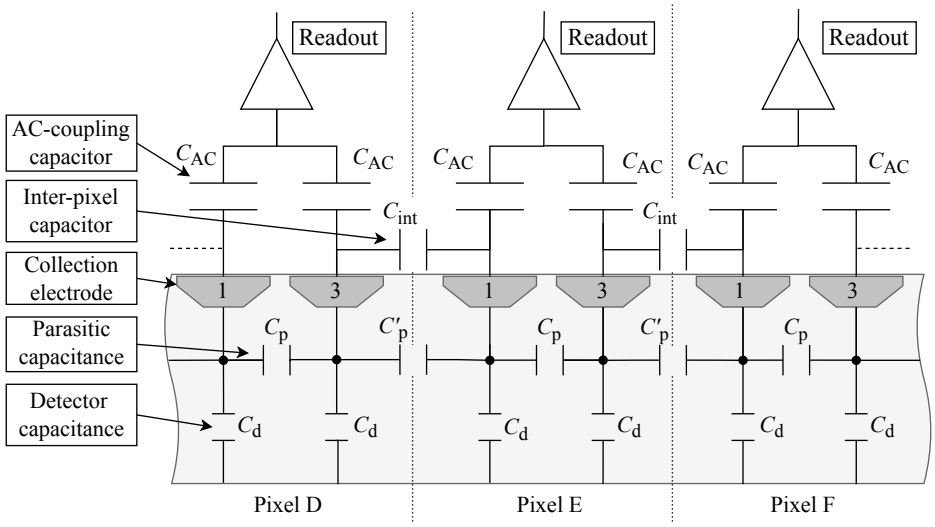



Figure 7.4: Equivalent circuit model for the sensor depicting inter-pixel and parasitic coupling capacitors in the sensor together with the pixel readout. The design is shown along the cut line given in Figure 7.1.

7.5, a simple, first-order model is implemented considering one pair of AC-coupled sub-pixels (e.g. sub-pixel D-3 and sub-pixel E-1 in Figure 7.1), disregarding the parasitic capacitances. The sensor is represented by a parallel circuit containing the sensor capacitance $C_d$, a resistor $R_d$ for a DC-current working point, and a current source ($I_{s1}$ or $I_{s2}$) that simulates the current pulse induced by an incident particle. The readout electronics is a charge-sensitive amplifier (CSA) with a feedback capacitor $C_f$ and a large bleeder resistor $R_f$. The CSAs were modelled using an ideal voltage dependent current source with transconductance $g_m$, a capacitor $C_o$ and a parallel resistor $R_o$ leading to an open-loop gain of $a_o = 500$. Hence, the effective capacitance of the CSA is given as

$$C_{CSA} = C_f(a_o + 1) \approx 2.5\,\text{pF}. \tag{7.5}$$

The AC-coupling capacitor between each sub-pixel and the CSA was set to be $C_{AC} = 500\,\text{fF}$, which together with the serial connected $C_{CSA}$ delivers the total capacitance $C_{CSA+AC} \approx 417\,\text{fF}$. The circuit in Figure 7.5 can be reduced to a capacitance net (Figure 7.6), with which the charge sharing between pixels can be calculated. Assuming a total charge of $Q_0$ is generated by the current pulse $I_{s1}$ at the sub-pixel 1, and no current is generated at the sub-pixel 2, the initial charge $Q_0$ will be distributed into three parts by such a capacitance net, according to the capacitances:

- $C_d$: sensor capacitance of sub-pixel 1,
- $C_{CSA+AC}$: total capacitance of the CSA and AC-coupling capacitance of sub-pixel 1,
- $C'_{int}$: the "effective inter-pixel capacitance" which is the total capacitance of $C_{int}$, $C_{CSA+AC}$ and $C_d$ of sub-pixel 2.

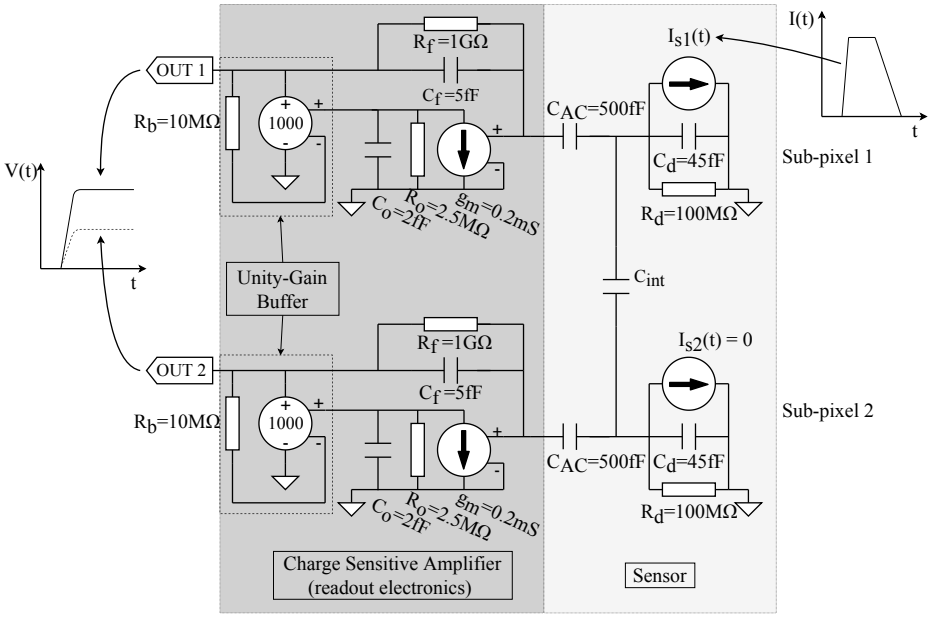



Figure 7.5: Simulation circuit of two sub-pixels which are coupled with an inter-pixel capacitor $C_{\text{int}}$. The current pulse is injected in the sensor and integrated by the readout for a voltage signal.

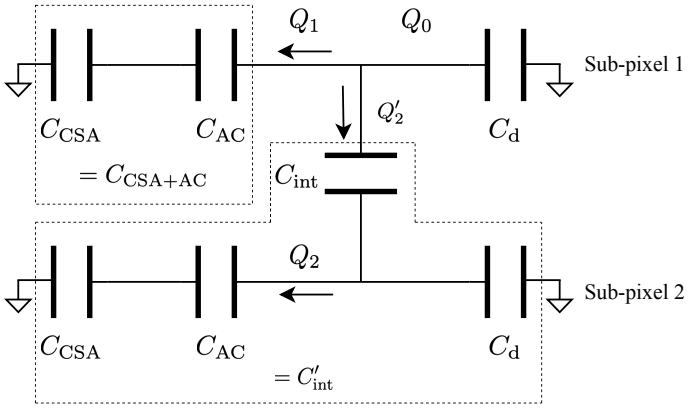



Figure 7.6: Capacitance net of the 2-sub-pixel model, based on Figure 7.5. The arrows labelled with $Q$ in the net circuit represent the charge distribution among different parts of the circuits. See the main text for details.

The amount of charge $Q_1$ is registered by the readout electronics of sub-pixel 1 through the $C_{\text{AC}}$, and the rest of the charge $Q'_2$ is shared to the sub-pixel 2 through $C_{\text{int}}$. The calculation gives

$$Q_1 = Q_0 \cdot \frac{C_{\text{CSA+AC}}}{C_{\text{CSA+AC}} + C_{\text{d}} + C'_{\text{int}}}, \tag{7.6}$$

$$Q'_2 = Q_0 \cdot \frac{C'_{\text{int}}}{C_{\text{CSA+AC}} + C_{\text{d}} + C'_{\text{int}}}, \tag{7.7}$$

$$\text{with } C'_{\text{int}} = \frac{(C_{\text{CSA+AC}} + C_{\text{d}}) \cdot C_{\text{int}}}{C_{\text{CSA+AC}} + C_{\text{d}} + C_{\text{int}}}. \tag{7.8}$$

The charge received by the CSA of sub-pixel 2 ($Q_2$) can be calculated by considering the charge division between the $C_{\text{CSA+AC}}$ and the $C_{\text{d}}$, as

$$\begin{aligned} Q_2 &= Q_2' \cdot \frac{C_{\text{CSA+AC}}}{C_{\text{CSA+AC}} + C_{\text{d}}} \\ &\overset{(7.7)}{=\!=} Q_0 \cdot \frac{C_{\text{int}}'}{C_{\text{CSA+AC}} + C_{\text{d}} + C_{\text{int}}'} \cdot \frac{C_{\text{CSA+AC}}}{C_{\text{CSA+AC}} + C_{\text{d}}} \\ &\overset{(7.8)}{=\!=} Q_0 \cdot \underbrace{\frac{C_{\text{int}}}{C_{\text{CSA+AC}} + C_{\text{d}} + 2C_{\text{int}}}}_{\text{charge-sharing fraction: } k} \cdot \underbrace{\frac{C_{\text{CSA+AC}}}{C_{\text{CSA+AC}} + C_{\text{d}}}}_{\text{CCE}} . \end{aligned} \tag{7.9}$$

The sub-pixel 2 receives a charge of $Q_2$ purely via capacitive coupling with the sub-pixel 1. The charge collection efficiency (CCE) is determined by the property of AC-coupling readout scheme, as described by Equation (3.19). For the aforementioned capacitance profiles, the CCE of this model is approximately 90%. The charge sharing fraction $k$ can be expressed as a function of the inter-pixel coupling capacitance $C_{\text{int}}$, indicating the portion of charge that is shared to the coupled pixel. It is not hard to validate the logic behind the cross-coupling scheme by considering the relation between $Q_1$ and $Q_2$. The sum of $Q_1$ and $Q_2$ gives the total charge $Q_0 \cdot \text{CCE}$ which is collected by this ideal system. In an extreme case, $C_{\text{int}} = 0$, meaning no inter-pixel coupling is implemented ($k = 0$), there are

$$\begin{aligned} Q_1 &\overset{(7.6)}{\underset{C_{\text{int}} \to 0}{=\!=}} Q_0 \cdot \frac{C_{\text{CSA+AC}}}{C_{\text{CSA+AC}} + C_{\text{d}}} = Q_0 \cdot \text{CCE} , \\ Q_2 &\overset{(7.9)}{\underset{C_{\text{int}} \to 0}{=\!=}} 0 . \end{aligned}$$

This indicates that this simulation model is also valid for a conventional pixel sensor. When $C_{\text{int}}$ is sufficiently large, the charge sharing fraction approaches 0.5, according to Equation (7.9).

The SPICE simulation used the circuit and the parameters presented in Figure 7.5. A typical current pulse shape is used for the MIP generated signal at the sub-pixel 1 $I_{\text{s1}}(t)$, which has a rise time of 0.2 ns, peaks at 0.7 µA for 1 ns, and has a fall time of 1 ns. The current source of sub-pixel 2 is set to constant $I_{\text{s2}} = 0$. The value of $k$ is determined by the ratio of output voltages of the CSAs as

$$k = \frac{V_{\text{OUT2}}}{V_{\text{OUT1}} + V_{\text{OUT2}}} . \tag{7.10}$$

The charge sharing fraction $k$ is determined for various $C_{\text{int}}$ from 0 to 500 fF, and depicted in Figure 7.7 together with the calculated expression of $k$ (Equation (7.9)). $k$ up to approximately 0.35 can be reached with the aforementioned parameters in this model. The maximum $k$ up to 0.5 can be approached through a larger $C_{\text{int}}$ and/or smaller $C_{\text{CSA+AC}}$, according to the asymptotic behaviour of Equation (7.9).

The stated coupling capacitor values are reachable in CMOS processes (typically 2 fF/µm$^2$) given the pixel pitch of 50 µm in either dimension. The total required area for the capacitors consists of four $C_{\text{AC}}$ (1 000 µm$^2$) and four $C_{\text{int}}/2$ ($C_{\text{int}}$ [µm$^2$]), because the space an inter-pixel capacitor can be shared by two adjacent pixels.

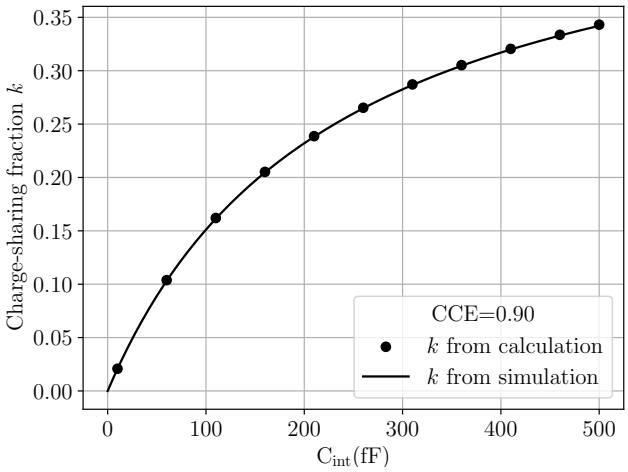



Figure 7.7: The charge-sharing fraction $k$ as a function of $C_{\text{int}}$ is obtained for one sub-pixel current injection with a charge-collection efficiency of 90%. The analytical calculation from Equation (7.9) is presented for comparison.

### Results: Spatial Resolution

The spatial resolution was simulated by adopting the CCE of 90% according to the simple network, and two detection thresholds of $10\%Q_{0,\text{MPV}}$ and $20\%Q_{\text{MPV}}$ for comparing the performances. The charge-sharing fractions $k$ used in the simulation is from 0 to 0.5, which covers the range from the SPICE simulation of the example circuit ($k$ up to 0.35) and higher values (0.35 to 0.5) to investigate the effects by a more significant charge sharing. The results are depicted in Figure 7.8, where the normalised x-/y-resolution for various thresholds is shown as a function of $k$. The resolution is normalised by the nominal resolution of a binary readout scheme, which is given by equation 3.15 as

$$\text{RMS}_{\text{binary}} = \frac{50\,\mu\text{m}}{\sqrt{12}} \approx 14.4\,\mu\text{m}. \tag{7.11}$$

Because of the symmetry of the square pixel, the calculated/simulated resolution values applies to both x- and y-directions. For $k = 0$ the resolution starts at a value close to the binary resolution, and then decreases (is improved) with increasing $k$ until the lowest value at $k \approx 0.4$ for non-binary readout. A significant improvement over the conventional pixel design ($k = 0$) by approximately 30% occurs when the shared charge exceeds the detection threshold. For instance, with a threshold of $10\%Q_{0,\text{MPV}}$, the normalised resolution is 0.6 at $k \approx 0.2$, which is higher than the threshold. The similar effect is found for the threshold of $20\%Q_{0,\text{MPV}}$. Consider the case of conventional pixels, i.e. $k = 0$, the charge sharing is merely due to the diffusion. Given the small charge-cloud width (1.6 µm) comparing with the pixel pitch, the cluster size is mostly one, corresponding to a large effective pixel (Figure 7.9 (a)) which covers almost the total pixel area. Consequently, the spatial resolution is close to the maximal value bound by the $\text{RMS}_{\text{binary}}$. Since this central effective pixel for cluster size one is independent of the charge resolution and dominates the RMS calculation, one does not observe large differences in spatial resolution between binary and non-binary readout. The influence of the

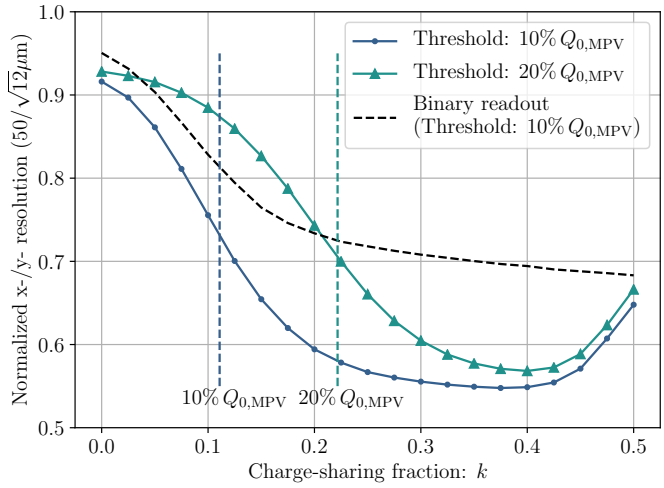



Figure 7.8: Normalized spatial resolution in x and y as functions of the charge-sharing fraction $k$. The results are normalised to $50/\sqrt{12}\,\mu$m. The solid curves presents the cases with a threshold of 10% $Q_{0,\mathrm{MPV}}$ and 20% $Q_{0,\mathrm{MPV}}$. The dashed curve indicates the binary readout case with threshold of 10% $Q_{0,\mathrm{MPV}}$. The vertical lines indicate the cases "shared charge = threshold".

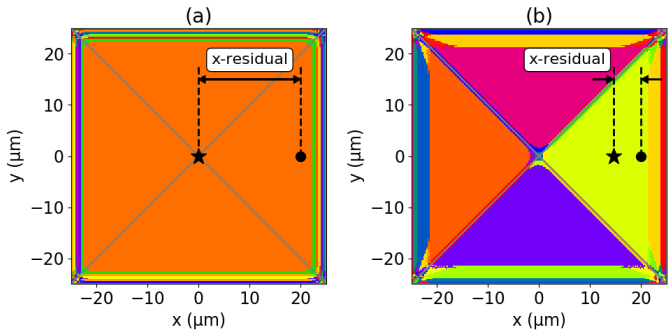



Figure 7.9: Layouts of effective pixels as different coloured areas from a fixed total deposited charge for a charge-sharing fraction $k = 0$ (a) and $k = 0.25$ (b) with a threshold of 10% $Q_{0,\mathrm{MPV}}$. "●" is the simulated particle's incident position, which is identical for both cases. "★" represents the reconstructed position for the corresponding charge-sharing fraction. The residuals in x are illustrated as the distances between the dashed lines.

increasing $k$ on the spatial resolution can be interpreted from Figure 7.9 (b), which shows the effective pixel map for $k = 0.25$. Here, the charge signatures with larger cluster sizes encode the position of the cross-coupled sub-pixels leading to a finer division into effective pixels. The dominating four triangular effective pixels are the result of the sub-pixel geometry. Consequently, the residual distribution (Figure 7.10) results in a smaller RMS, in comparison with the conventional pixel design ($k = 0$) whose residual distribution is similar as a uniform distribution. The spatial resolution of a binary readout is considered as the limiting case for reference, as shown in Figure 7.8. Although the absence of the charge information, and the sub-pixels are encoded in the cluster size, there is still an improvement in the resolution of approximately 20% at $k \approx 0.2$.

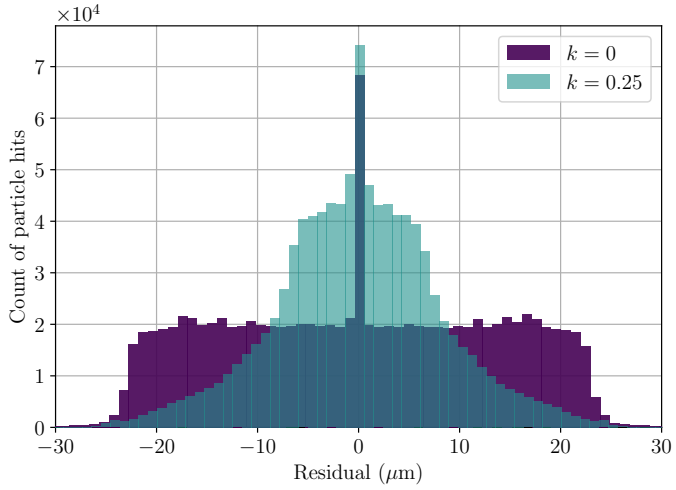



Figure 7.10: Residual distributions for a charge-sharing fraction $k = 0$ and $k = 0.25$ with a threshold of 10% $Q_{0,\mathrm{MPV}}$.

When $k$ approaches 0.5, the resolution degrades and approaches the resolution given by the binary readout. $k = 0.5$ indicates that a half of one sub-pixel will be shared to the coupled sub-pixel and *vice versa*. The consequence of this is that both sub-pixel will have the same amount of charge. Hence, the charge information is lost, which is the same as the binary readout.

The alternation of charge, originating from noises and energy-loss straggling, can lead to the calculation of unknown or wrong charge signatures that in further consequence can lead to a worse hit position reconstruction. By choosing 1 million charge depositions to pre-compute the charge signatures the likelihood of having a signature during reconstruction that was not pre-computed is below 2%.

## 7.4 Extending the Capacitance Network

The simple 2-sub-pixel model used in the SPICE simulation was an ideal case for estimating the relation between the inter-pixel cross-coupling capacitance and the charge sharing fraction. However, when the design is implemented in the sensor, the capacitive network will be extended to the entire pixel matrix. Therefore, the electronics property of the circuit, and the performance figures of such a connection scheme will be altered. Figure 7.11 illustrates the schematics of the extended circuit based on the 2-sub-pixel model. The connection to the other three sub-pixels and their coupling connections are included as the "branch 1". As a part of the branch 1, the cross-coupling from the other sub-pixels via $C_{\mathrm{int}}$ is labelled as branch 2.

The complexity of the capacitance network gets enormously high when it comes to silicon pixel detectors for actual applications, since there can be several thousands of pixels. To analyse such a network, approximations need to be made. It can be assumed that the entire branch 1 of this circuit possesses a capacitance $C_{\mathrm{rest}}$, meaning the capacitance of the rest of the circuit apart form one sub-pixel (Figure 7.12 (a)). In the same manner, the entire branch 2 possesses an effective capacitance of $C_{\mathrm{eff}}$. Such a schematic shows a property of self-similarity, i.e. the branch 1 of a pixel contains branch 2 of

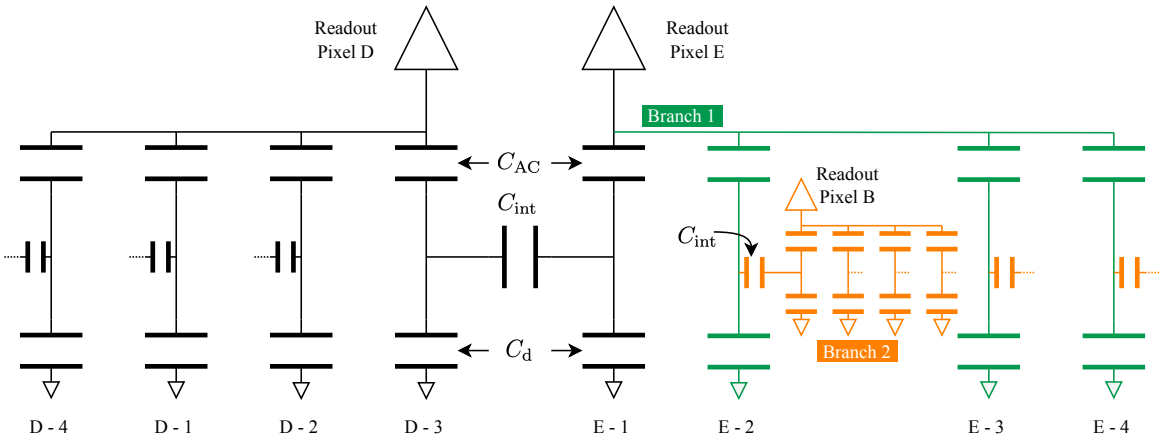



Figure 7.11: The schematics of the extended capacitance network for the sub-pixel cross-coupling using the AC-coupling method. The pixels D and E depicted in Figure 7.1 are considered as the starting point of the capacitance network, where the cross-coupling between sub-pixel D-3 and E-1 is presented in the centre. The network is extended by including the connection to the remaining sub-pixels (branch 1) and their couplings network to the other pixels (branch 2). An example of the circuit branches is explicitly given for pixel E, and the same applies to D and other pixels in the complete network. The connection to the rest of the network is indicated using dotted lines to reduce the complexity of the schematics.

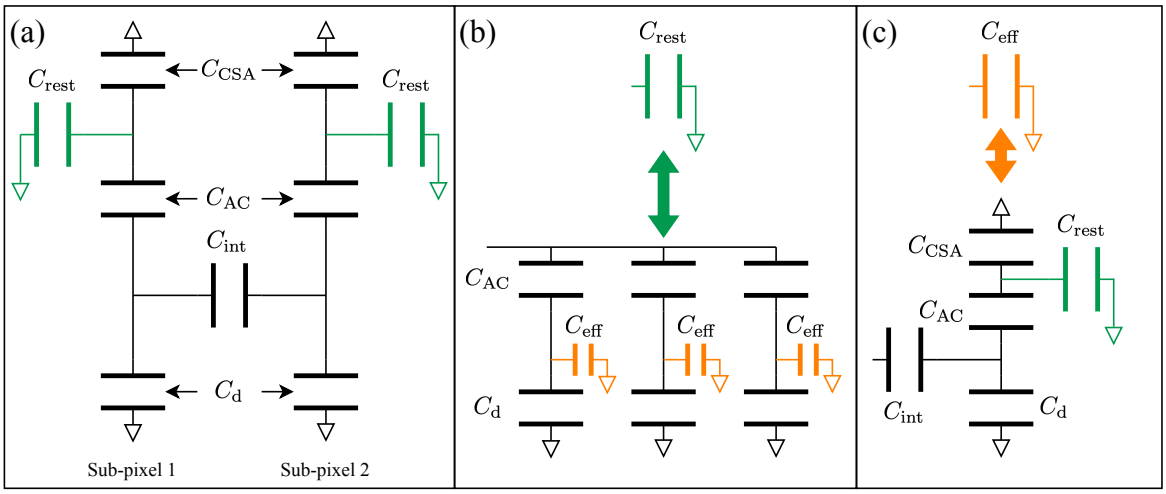



Figure 7.12: The reduced schematics of the extended capacitance network (a), with implementing the effective capacitances $C_{rest}$ (b) and $C_{eff}$ (c). The CSA is represented with its effective capacitance $C_{CSA}$

the sub-pixels (Figure 7.12 (b)), and the branch 2 contains the branch 1 of another sub-pixel (7.12 (c)), and so on. Comparing Figure 7.12 (a) with the circuit of the simple model (Figure 7.6), it can be seen that $C_{rest}$ acts as a competing capacitance to the CSA ($C_{CSA}$). This means that the charge collection efficiency degrades, and the charge sharing fraction $d$ is influenced by $C_{rest}$ as well. The estimation of such an effect is similar to the calculations of the simple model by equations (7.6) to (7.9). For

convenience, the total capacitance of $C_{\mathrm{AC}}$, $C_{\mathrm{CSA}}$, and $C_{\mathrm{rest}}$ of the part of the circuit can be written as

$$C_{\mathrm{CSA+AC+rest}} = \frac{C_{\mathrm{AC}}(C_{\mathrm{CSA}} + C_{\mathrm{rest}})}{C_{\mathrm{AC}} + C_{\mathrm{CSA}} + C_{\mathrm{rest}}} . \tag{7.12}$$

Again, with a charge deposition $Q_0$ at the sub-pixel 1 and no charge deposition at sub-pixel 2, the charge collected by both sub-pixels can be calculated as

$$Q_1 = Q_0 \cdot \underbrace{\frac{C_{\mathrm{CSA+AC+rest}}}{C_{\mathrm{CSA+AC+rest}} + C_{\mathrm{d}} + C_{\mathrm{eff}}}}_{\text{fraction towards } C_{\mathrm{AC}}} \cdot \underbrace{\frac{C_{\mathrm{CSA}}}{C_{\mathrm{CSA}} + C_{\mathrm{rest}}}}_{\text{fraction collected by } C_{\mathrm{CSA}}} , \tag{7.13}$$

$$Q_2 = Q_0 \cdot \underbrace{\frac{C_{\mathrm{eff}}}{C_{\mathrm{CSA+AC+rest}} + C_{\mathrm{d}} + C_{\mathrm{eff}}}}_{\text{fraction towards } C_{\mathrm{int}}} \cdot \underbrace{\frac{C_{\mathrm{CSA+AC+rest}}}{C_{\mathrm{CSA+AC+rest}} + C_{\mathrm{d}}}}_{\text{fraction towards } C_{\mathrm{AC}}} \cdot \underbrace{\frac{C_{\mathrm{CSA}}}{C_{\mathrm{CSA}} + C_{\mathrm{rest}}}}_{\text{fraction collected by } C_{\mathrm{CSA}}} . \tag{7.14}$$

The charge collection efficiency (CCE) of such a circuit is then calculated as

$$\mathrm{CCE} = \frac{Q_1 + Q_2}{Q_0} = \frac{C_{\mathrm{CSA+AC+rest}}}{C_{\mathrm{CSA+AC+rest}} + C_{\mathrm{d}}} \cdot \frac{C_{\mathrm{CSA}}}{C_{\mathrm{CSA}} + C_{\mathrm{rest}}} . \tag{7.15}$$

The CCE is less sensitive to the first term, since $C_{\mathrm{CSA+AC+rest}}$ is typically much larger than $C_{\mathrm{d}}$. Therefore, Equation (7.15) is mainly influenced by the ratio $C_{\mathrm{CSA}}/C_{\mathrm{rest}}$. A high CCE can be achieved when $C_{\mathrm{rest}}$ is small. The charge sharing fraction is given by

$$k = \frac{Q_2}{Q_0 \cdot \mathrm{CCE}} = \frac{C_{\mathrm{eff}}}{C_{\mathrm{CSA+AC+rest}} + C_{\mathrm{d}} + C_{\mathrm{eff}}} . \tag{7.16}$$

It is easier to start with calculating the capacitance $C_{\mathrm{eff}}$ for estimating $C_{\mathrm{rest}}$ and deriving $k$. Considering Figure 7.12 (c), $C_{\mathrm{eff}}$ can be expressed as

$$\begin{aligned} C_{\mathrm{eff}} &= \left( \frac{1}{C_{\mathrm{int}}} + \left( C_{\mathrm{d}} + \frac{C_{\mathrm{AC}}(C_{\mathrm{CSA}} + C_{\mathrm{rest}})}{C_{\mathrm{AC}} + C_{\mathrm{CSA}} + C_{\mathrm{rest}}} \right)^{-1} \right)^{-1} \\ &= \left( \frac{1}{C_{\mathrm{int}}} + \left( C_{\mathrm{d}} + \frac{C_{\mathrm{AC}}}{\frac{C_{\mathrm{AC}}}{C_{\mathrm{CSA}} + C_{\mathrm{rest}}} + 1} \right)^{-1} \right)^{-1} . \end{aligned}$$

Based on typical parameters for such an AC-coupled readout (as discussed in previous sections), $C_{\mathrm{CSA}}$ is usually larger than $C_{\mathrm{AC}}$ due to the large open-loop gain of the CSA and the limited size of the pixel pitch for fabricating the coupling capacitor. Therefore, $C_{\mathrm{AC}}$ is the upper bound of the following term in the above equation

$$\frac{C_{\mathrm{AC}}}{\frac{C_{\mathrm{AC}}}{C_{\mathrm{CSA}} + C_{\mathrm{rest}}} + 1} \; (\lesssim C_{\mathrm{AC}}) .$$

Hence, the upper bound of the $C_{\text{eff}}$ can be estimated as

$$C_{\text{eff}} \lesssim \frac{C_{\text{int}}(C_{\text{d}} + C_{\text{AC}})}{C_{\text{int}} + C_{\text{d}} + C_{\text{AC}}} . \tag{7.17}$$

According to Figure 7.12 (b), the upper bound of $C_{\text{rest}}$ is given as

$$\begin{aligned} C_{\text{rest}} &= 3\frac{C_{\text{AC}}(C_{\text{eff}} + C_{\text{d}})}{C_{\text{AC}} + C_{\text{eff}} + C_{\text{d}}} \\ &\lesssim 3\frac{C_{\text{AC}}(C_{\text{AC}}C_{\text{d}} + C_{\text{d}}^2 + C_{\text{AC}}C_{\text{int}} + 2C_{\text{d}}C_{\text{int}})}{(C_{\text{AC}} + C_{\text{d}})(C_{\text{AC}} + C_{\text{d}} + 2C_{\text{int}})} . \end{aligned} \tag{7.18}$$

Inserting the upper bound of $C_{\text{eff}}$ and $C_{\text{rest}}$ together with the parameters used for the simple model into equations (7.15) and (7.16) delivers

$$\text{CCE}(C_{\text{int}}) = \frac{1\,250\,000\,\text{fF}^2(545\,\text{fF} + 2C_{\text{int}})}{791\,612\,500\,\text{fF}^3 + 3\,655\,000\,\text{fF}^2 C_{\text{int}}} , \tag{7.19}$$

$$k(C_{\text{int}}) = \frac{C_{\text{int}}(927\,862\,500\,\text{fF}^3 + 4\,155\,000\,\text{fF}^2 C_{\text{int}})}{(545\,\text{fF} + 2C_{\text{int}})(791\,612\,500\,\text{fF}^3 + 3\,905\,000\,\text{fF}^2 C_{\text{int}})} . \tag{7.20}$$

They are plotted in Figure 7.13 and 7.14, together with the corresponding functions of the simple model. The CCE in the extended network is a decreasing function of $C_{\text{int}}$, similar to what was derived from the simple model. The case of $C_{\text{int}} = 0$ can be interpreted as a conventional pixel cell having an electrode which is 4 times larger than that of a sub-pixel, corresponding to a capacitance of $4C_{\text{d}}$. Therefore, the CCE in the extended network reveals a smaller value than in the ideal simple model. An increase of $C_{\text{int}}$ leads to a larger $C_{\text{eff}}$ (Equation (7.17)), and consequently a larger $C_{\text{res}}$ (Equation (7.18)). As discussed earlier, this will reduce the CCE (Equation (7.15)). For large $C_{\text{int}}$, the CCE

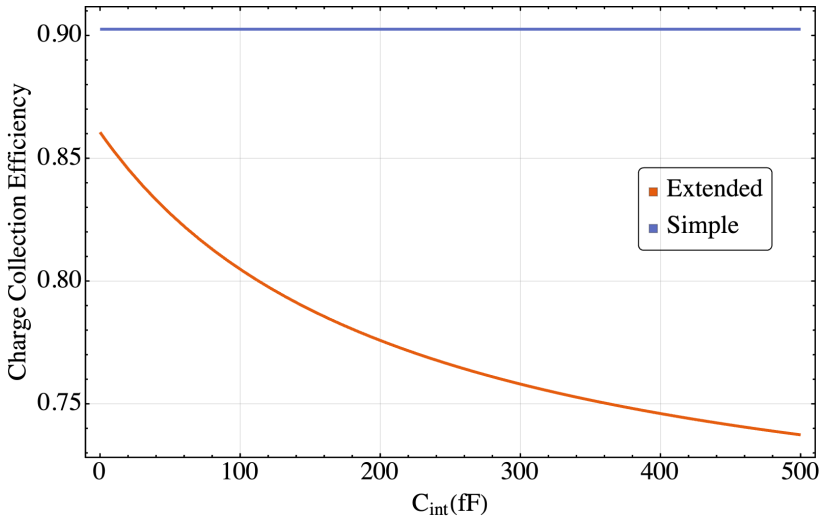



Figure 7.13: Charge collection efficiency of the simple coupling model and the extended capacitance network, as a function of $C_{\text{int}}$.

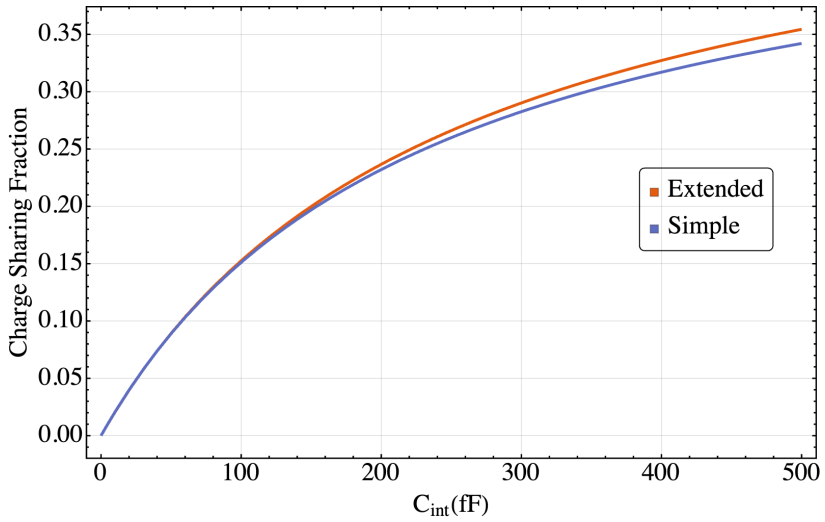



Figure 7.14: Charge sharing fraction of the simple coupling model and the extended capacitance network, as a function of $C_{\text{int}}$.

saturates at approximately 0.68, under the aforementioned approximations. On the contrary, the behaviour of the charge sharing fraction of the extended network is similar to that of the simple model. The introduction of $C_{\text{rest}}$ actually increases the effective inter-pixel capacitance $C_{\text{eff}}$, in comparison with $C'_{\text{int}}$ in the simple model (Equation (7.8)). Therefore, more charge will be shared with the coupled pixel. The asymptotic value of $k$ for a sufficiently large $C_{\text{int}}$ saturates at approximately 0.53.

### Input Capacitance

Another interesting and useful quantity is the capacitance which is connected to the input of the CSA (input capacitance), after implementing the sub-pixel cross-coupling. As mentioned in section 3.2.2, the equivalent noise charge increases linearly with $C_d$ in a DC-coupling detector. In the case of AC-coupled readout, the input capacitance is important for estimating the electronic noise of the readout electronics.

The conceptional sub-pixel cross-coupling sensor and the conventional pixel sensors with the same pixel pitch can be compared by using the same charge-sensitive amplifier (CSA) with an effective capacitance of $C_{\text{CSA}} \approx 2.5\,\text{pF}$ as introduced before. Figure 7.15 shows the schematics for both cases. The pixel capacitance of the sub-pixel is $C_{\text{d}} = 45\,\text{fF}$. It can be further assumed the ideal case that the capacitance of the conventional pixel is 4 times the sub-pixels, i.e. $C_{\text{d}}^{\text{conv}} = 4 \times C_{\text{d}} = 180\,\text{fF}$. For the cross-coupling case, the inter-pixel capacitance is set to $C_{\text{int}} = 150\,\text{fF}$. For the extended network, this corresponds to CCE $\approx 0.79$ (Figure 7.13) and $k \approx 0.2$ (Figure 7.14). By setting a detection threshold of $10\%Q_{0,\text{MPV}}$, the spatial resolution of the cross-coupling sensors should be visibly improved, since the shared charge $k \cdot \text{CCE} \cdot Q_{0,\text{MPV}} \approx 0.16Q_{0,\text{MPV}}$ is greater than the threshold value. To ensure a similar condition for comparison, the CCE of the conventional pixel is set to 0.79, which requires an AC-coupling capacitor with $C_{\text{AC}}^{\text{conv}} \approx 930\,\text{fF}$, according to Equation (3.19). The general expression for

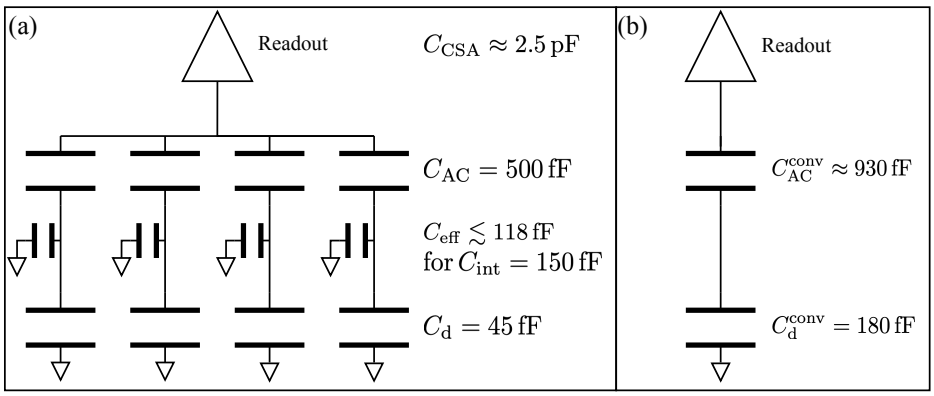



Figure 7.15: The capacitance schematics for one pixel cell of (a) the sub-pixel cross-coupling model, and (b) the conventional pixel sensor. The value chosen for the shown capacitances ensures the same CCE = 0.79.

$C_{\mathrm{AC}}^{\mathrm{conv}}$ having the same CCE as the cross-coupling sensor is obtained by solving

$$\mathrm{CCE}_{\text{equation (7.15)}} \stackrel{!}{=} \frac{C_{\mathrm{CSA}} C_{\mathrm{AC}}^{\mathrm{conv}}}{C_{\mathrm{CSA}} + C_{\mathrm{AC}}^{\mathrm{conv}}} \,. \tag{7.21}$$

Inserting the upper bound of $C_{\mathrm{rest}}$ and $C_{\mathrm{eff}}$ yields

$$C_{\mathrm{AC}}^{\mathrm{conv}} = 4 \frac{C_{\mathrm{AC}} C_{\mathrm{CSA}} C_{\mathrm{d}} (C_{\mathrm{AC}} + C_{\mathrm{d}} + 2C_{\mathrm{int}})}{C_{\mathrm{AC}} C_{\mathrm{CSA}} C_{\mathrm{d}} + 3C_{\mathrm{AC}}^2 C_{\mathrm{int}} + C_{\mathrm{CSA}} C_{\mathrm{d}} (C_{\mathrm{d}} + 2C_{\mathrm{int}})} \,. \tag{7.22}$$

Neglecting parasitic capacitances, the input capacitance of the conventional pixel and the cross-coupling model are given as

$$C_{\mathrm{input}}^{\mathrm{conv}} = \frac{C_{\mathrm{AC}}^{\mathrm{conv}} C_{\mathrm{d}}^{\mathrm{conv}}}{C_{\mathrm{AC}}^{\mathrm{conv}} + C_{\mathrm{d}}^{\mathrm{conv}}} \tag{7.23}$$

$$= 4 \frac{C_{\mathrm{AC}} C_{\mathrm{CSA}} C_{\mathrm{d}} (C_{\mathrm{AC}} + C_{\mathrm{d}} + 2C_{\mathrm{int}})}{C_{\mathrm{CSA}} (C_{\mathrm{AC}} + C_{\mathrm{d}})^2 + (3C_{\mathrm{AC}}^2 + 2C_{\mathrm{AC}} C_{\mathrm{CSA}} + 2C_{\mathrm{CSA}} C_{\mathrm{d}}) C_{\mathrm{int}}} \,, \tag{7.24}$$

$$C_{\mathrm{input}} = 4 \frac{C_{\mathrm{AC}} (C_{\mathrm{eff}} + C_{\mathrm{d}})}{C_{\mathrm{AC}} + C_{\mathrm{eff}} + C_{\mathrm{d}}} \tag{7.25}$$

$$= 4 \frac{C_{\mathrm{AC}} (C_{\mathrm{AC}} (C_{\mathrm{d}} + C_{\mathrm{int}}) + C_{\mathrm{d}} (C_{\mathrm{d}} + 2C_{\mathrm{int}}))}{(C_{\mathrm{AC}} + C_{\mathrm{d}})(C_{\mathrm{AC}} + C_{\mathrm{d}} + 2C_{\mathrm{int}})} \,. \tag{7.26}$$

The expression of $C_{\mathrm{input}}$ is derived by using the upper bond of $C_{\mathrm{eff}}$. Inserting the example values given in Figure 7.15 into Equations (7.23) and (7.25) yields that $C_{\mathrm{input}}^{\mathrm{conv}} \approx 150\,\mathrm{fF}$ and $C_{\mathrm{input}} \approx 491\,\mathrm{fF}$. The input capacitance of the pixels using sub-pixel cross-coupling is approximately 3 times higher than the conventional pixel.

A more general expression for such a comparison can be obtained by considering equations (7.24)

and (7.26) as functions of $C_{\text{int}}$. The ratio of $C_{\text{input}}$ and $C_{\text{input}}^{\text{conv}}$ is then given as

$$\frac{C_{\text{input}}}{C_{\text{input}}^{\text{conv}}}(C_{\text{int}}) = (C_{\text{AC}}(C_{\text{d}} + C_{\text{int}}) + C_{\text{d}}(C_{\text{d}} + 2C_{\text{int}}))\cdot \\ \cdot \frac{C_{\text{CSA}}(C_{\text{AC}} + C_{\text{d}})^2 + (3C_{\text{AC}}^2 + 2C_{\text{AC}}C_{\text{CSA}} + 2C_{\text{CSA}}C_{\text{d}})C_{\text{int}}}{C_{\text{CSA}}C_{\text{d}}(C_{\text{AC}} + C_{\text{d}})(C_{\text{AC}} + C_{\text{d}} + 2C_{\text{int}})^2} . \tag{7.27}$$

Using the given capacitance values, the behaviour of the ratio is depicted in Figure 7.16. For $C_{\text{int}} = 0$, the input capacitance of a cross-coupled pixel is identical to that of a conventional pixel, since the capacitive coupling between sub-pixels vanishes. With growing inter-pixel capacitance, the input capacitance of the cross-coupled pixel rises monotonically, because the upper bound of $C_{\text{eff}}$ is an increasing function of $C_{\text{int}}$. Considering the example value $C_{\text{int}} = 150\,\text{fF}$, the input capacitance of a readout channel for cross-coupled pixels is approximately 3 times higher than that for a conventional pixel sensor. The asymptotic behaviour of the ratio for sufficiently large $C_{\text{int}}$ shows a saturation at approximately 8.

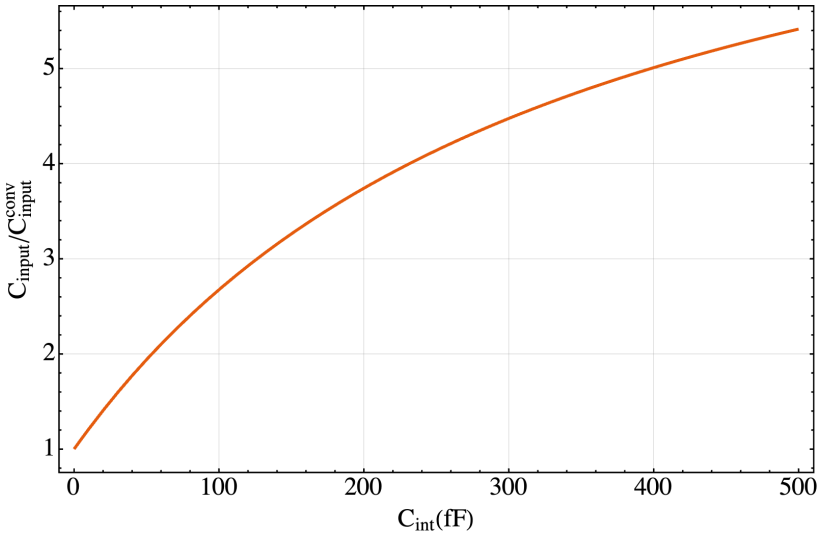



Figure 7.16: The ratio $C_{\text{input}}/C_{\text{input}}^{\text{conv}}$ as a function of $C_{\text{int}}$. The function is valid when the considered conventional pixel and cross-coupling pixel have the same CCE.

## 7.5 Chapter Conclusion

The concept of improving spatial resolution in pixel detectors by introducing directional charge sharing through sub-pixel cross-coupling was demonstrated using simulations. It offers a possibility to further enhance the spatial resolution while maintaining the pixel pitch and the density of the readout electronics. The impact of charge-sharing on the spatial resolution was studied considering a $50\,\mu\text{m} \times 50\,\mu\text{m}$ pixel sensor with $100\,\mu\text{m}$ thickness and assuming perpendicular particle tracks.

It is found that the spatial resolution is improved when increasing the charge sharing fraction $k$. A significant improvement occurs when the charge shared with adjacent sub-pixels is above their

detection threshold. The reason is the finer division of effective pixels, which represents distinct charge signature, through the sub-pixel cross-coupling. The maximum improvement in spatial resolution of approximately 30% with respect to standard planar pixel sensor-layouts can be achieved at $k \approx 0.4$, independent of the detection threshold. However, the spatial resolution is worsened when $k$ approaches 0.5.

An ideal model coupling scheme using AC-coupled, triangular readout electrodes, was presented as a possible implementation. Charge-sharing fractions of up to 35% can be achieved with inter-pixel capacitors below 500 fF, based on a first-order model. However, the more realistic model – the extended capacitance network – revealed a degradation in the charge collection efficiency (CCE) with increasing $k$. Using an inter-pixel coupling capacitor with 150 fF ($k \approx 0.2$) changed the CCE from 0.90 to 0.79, which leads to a less improvement of the spatial resolution, in comparison with the ideal model. In addition, it comes at the cost of a considerably increased input capacitances that, depending on the CSA design, worsens the noise and timing performances or increases power consumption. This has a potentially negative impact on the in-time hit-detection performance.

CHAPTER 8

# Conclusion

This thesis focused on improving the breakdown performance and the spatial resolution of silicon pixel detectors. The breakdown voltages with respect to various guard ring designs were investigated combining measurements on produced test structures and TCAD simulations. Apart from the guard rings, the knowledge gained from this study was applied to improve the sensor design of the CERN-RD50 MPW CMOS detector prototype for achieving a higher breakdown voltage. A concept of sub-pixel cross-coupling was proposed and studied using a dedicated simulation software. It aims to artificially enhance the charge sharing between pixels through electrical couplings, in order to improve the spatial resolution of pixel detectors without reducing the pixel size. An AC-coupling scheme, which can be realised using commercial CMOS technologies, was presented and discussed.

## Breakdown of Sensors

The design of multi-guard-ring structures plays an important role in determining the breakdown performance of silicon pixel sensors. A well-designed guard ring structure acts as a buffer zone of the large voltage drop to the sensor's edge, and ensures that the potential is gradually lowered from the grounded pixel matrix over the multiple floating rings. Therefore, high electric fields can be avoided during the sensor operating. The passive CMOS test structures studied in this thesis are equipped with various space-efficient guard ring designs, featuring 5 to 6 rings placed within the 274 µm gap between the pixel matrix and the sensor's dicing edge. The guard ring designs further differ in the type of implants and the use of polysilicon overhang.

Breakdown measurements of unirradiated samples revealed that distinct guard ring geometries delivered various breakdown voltages ranged from approximately 180 V to over 500 V. The follow-up TCAD simulations successfully reproduced the experimentally determined relation between guard ring designs, and provided insights on the potential, electric field, and current density distributions. From these, the relation between the design and breakdown performance can be established. It is found that the potential drop is not uniform between each pair of neighbouring floating guard rings. The highest potential drop is always located at the innermost ring, where the electric field is maximum. The guard ring designs which delivered a higher breakdown voltage shows a visible smoothing of the potential distribution. It has the features:

- Large spacing between the grounded electrode and the innermost floating guard ring. Increasing

the spacing does not reduce the potential difference, but results in a smoother potential distribution which corresponds to the electric field.

- N-well implant attached besides the default p-type guard rings. The n-well visibly elevated the floating potential at the guard ring, so that the potential differences and electric field (especially at the innermost guard ring) is reduced.

- Deep n-well substituted the standard n-well, mentioned in the previous bullet point. The n-well with a greater depth can more significantly elevate the floating potential and reduce the electric field.

The polysilicon overhang was shown to have a negative impact on the breakdown performance of un-irradiated samples, due to the suppression of floating potentials. However, for the case after TID irradiation, the overhang structure can visibly reduce the leakage current by suppressing the high electric field at the guard rings.

The polysilicon field plate, which acts as the gate in a MOSFET, showed the ability to modify the local potential distribution by applying various voltages.

Treating the field plate that surrounds the grounded electrodes as a guard ring structure, the potential distribution can be altered by varying the field plate voltage, and the breakdown voltage is can be tuned. Further studies of the field plate should be proceeded by fabricating a test structure with polysilicon guard rings. By tuning the voltages on them, an optimum potential distribution may be obtained. Moreover, the optimised field plate voltages can possibly be achieved by introducing a resistive voltage division circuit.

Determining the potential distribution and the location of the maximum electric field is the key for evaluating the breakdown performance of guard ring designs. Using this information, the field properties can be regulated by adjusting the implant geometries or using additional structures like overhang or field plate to improve the breakdown performance. The same methodology was applied to diagnose the premature breakdown of the DMAPS prototype RD50-MPW3, and optimise its sensor geometry. Besides a new guard ring, the sensor periphery was modified to significantly reduce the potential differences, so that the sensor can sustain a higher bias voltage.

## Sub-pixel Cross-coupling

The spatial resolution of a silicon pixel detector is primarily determined by the pixel size. In addition, the incident position of a particle is also encoded in the charge information when the created charge carriers are shared between adjacent pixels. Improving the spatial resolution is challenged by the considerable effort for redesigning the readout electronics to reduce the pixel size, and the limited charge sharing in state-of-the-art thin sensors. The concept of sub-pixel cross-coupling aims to enhance the charge sharing to improve the spatial resolution, whilst keeping the pixel size unchanged. Sub-dividing the conventional pixel electrodes and establishing electronic coupling within the pixel matrix, is able to create a directional charge sharing which reflects the locations of impinging particles.

A 3-by-3 pixel matrix with $50\,\mu m \times 50\,\mu m$ pixels was studied using simulations. Assuming the MIP injection with the track to be perpendicular to the detector plane, the spatial resolution can be improved by up to 30% with respect to the conventional pixel sensor design. The requirement is a sufficiently large charge-sharing fraction, so that the collected charge in adjacent sub-pixels is above

the detection threshold. A model coupling scheme using AC-coupled, triangular readout electrodes, is used as a possible implementation. Charge-sharing fractions up to 35% are achieved with inter-pixel capacitors below 500 fF, based on a first-order model. However, such coupling schemes come at the cost of a considerably increased input capacitances that, depending on the CSA design, worsen noise and timing performance or increase power consumption. This has a potentially negative impact on the in-time hit-detection performances. There are alternatives for implementing the directional charge sharing, such as a different cross-coupling mechanism and sub-pixel geometries to be studied. Nevertheless, due to the interdependence of process and design in combination with the readout electronics, such performance figures are difficult to access with simulations, especially after radiation damage, and thus require measurements with produced devices.

APPENDIX A

# Approximate Projection of the Charge Cloud

A minimum ionising particle (MIP) traversing through a silicon pixel detector will deposit its energy into the silicon crystal along the track. Assuming that the particle track is perpendicular to the detector plane, a simple method to simulate the charge sharing between the pixels is to consider its projection onto the detector surface, where the charge collection electrodes are located. The motion of the created charge cloud does not only have a drift component, which is caused by the electric field, but also expand in all directions due to diffusion. The effect of diffusion is more visible in the transverse plane, i.e. the plane perpendicular to the drift direction, because the drift velocity is macroscopically larger than then diffusion [1]. Subsequently, the longer the drift time (the larger distance between the electrode and the creation position of the charge cloud), the larger is the width of the charge cloud (equation 3.10). To include the expansion of the charge cloud by MIP requires more calculations or approximations, since the charges are not generated at one location, but at various places along the track as clusters with different distances to the detector surface. Therefore, the projection of the charge cloud is a sum of all the charge clusters.

The simplest approximation of the charge cloud projection is merely assuming the charge cloud projection is a 2D Gaussian distribution using the average charge cloud width, calculated with equation (7.1). This was also used in this work, because it significantly simplified the calculations and reduced the computing time for simulations.

Nevertheless, it is also interesting to consider a more realistic case in which the line deposition of the charge cloud is considered. Figure A.1 illustrates the final width of the charge clusters created along the MIP track. Each cluster is indicated by a circle plate perpendicular to the particle track, where the charge distribution is expressed by a 2D gaussian distribution neglecting the diffusive expansion in the z-direction. The final width $\sigma(z)$ represents the transversal width of the charge cluster when it reaches the detector surface. Additionally, the distances between each cluster is defined as $\Delta z$. The projection of the charge clouds produced by a mip injected at position $(\xi, \zeta)$ is, therefore, given as

$$\rho_{2D}(x, y) = \sum_{i=1}^{n} \frac{Q_i}{2\pi\sigma(z_i)^2} \exp\left[-\frac{(x-\xi)^2 + (y-\zeta)^2}{2\sigma(z_i)^2}\right], \tag{A.1}$$

[1] In the microscopic point of view, the thermal velocity is considered for the diffusion process, and it is higher than the macroscopic drift velocity. However, diffusion is a stochastic process where the directions of charge carriers are random.

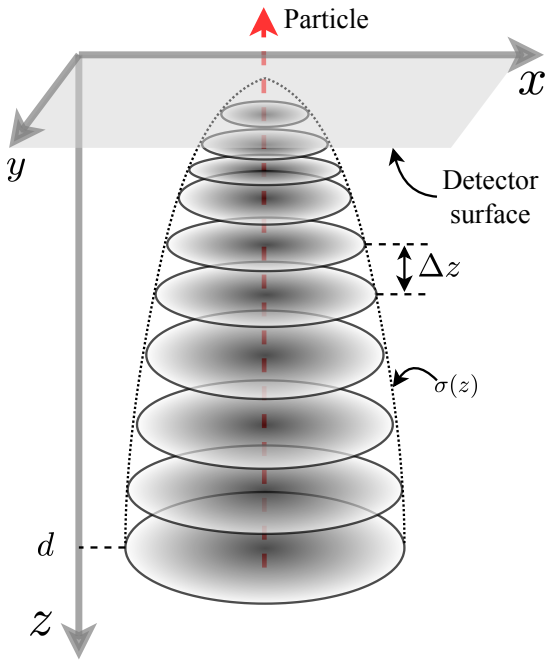



Figure A.1: The final width of the charge clusters produced at various distances along the MIP track. Each cluster is represented with the circle plate parallel to the x-y plane. The widths are calculated based on the location of creation with respect to the detector surface, where the collection electrodes are located.

summing the 2D gaussian distributions of all the clusters (planes) with $Q_i$ the total charge and $z_i$ the distance to the detector surface. Further assuming that the charge creation is continuously taking place along the track ($\Delta z \rightarrow \mathrm{d}z$), equation (A.1) turns into an integral

$$\rho_{2\mathrm{D}}(x,y) = \int_{z_0}^{d} \frac{Q_0}{d} \frac{1}{2\pi\sigma(z)^2} \exp\left[-\frac{(x-\xi)^2+(y-\zeta)^2}{2\sigma(z)^2}\right] \mathrm{d}z\,, \tag{A.2}$$

with $Q_0$ the total charge, $d$ the thickness of the depleted region in the sensor, and $z_0$ a minimum distance which merely gives a non-zero initial value of $\sigma(z)$ to avoid the singularity.

## High Voltage Approximation

An analytical expression for the results of equation (A.2) is still hard to obtain using the expression of $\sigma(z)$ from equation (3.10). Therefore, an approximation for the case that the bias voltage is much larger than the full depletion voltage ($V_{\mathrm{bias}} >> V_{\mathrm{dep}}$) can be derived from the Taylor expansion of equation (3.10) [38]. Taking the first term, it gives

$$\sigma_{\mathrm{HV}}(z) = \sqrt{\frac{2k_B T d}{eV_{\mathrm{bias}}}} z \tag{A.3}$$

as the high voltage approximation. Inserting equation (A.3) into equation (A.2) delivers

$$\rho_{2D}(x,y) = \frac{eQ_0V_{\text{bias}}}{4k_B\pi Td^2}\left[\Gamma\left(0, \frac{eV_{\text{bias}}(x^2+y^2)}{4k_BTd^2}\right) - \Gamma\left(0, \frac{eV_{\text{bias}}(x^2+y^2)}{4k_BTdz_0}\right)\right], \tag{A.4}$$

assuming $(\xi, \zeta) = (0, 0)$ for simplicity. The $\Gamma(s, x)$ represents the incomplete gamma function defined as

$$\Gamma(s,x) = \int_x^\infty t^{s-1}\exp[-t]\mathrm{d}t\,. \tag{A.5}$$

The simple approximation using the 2D Gaussian distribution delivers

$$\rho_{2D}^{\text{Gauss}}(x,y) = \frac{Q_0}{d}\frac{1}{2\pi\bar{\sigma}_{\text{HV}}^2}\exp\left[-\frac{x^2+y^2}{2\bar{\sigma}_{\text{HV}}^2}\right], \tag{A.6}$$

where the mean width $\bar{\sigma}_{\text{HV}}$ is calculated using equation (A.3) as

$$\bar{\sigma}_{\text{HV}} \overset{\text{eq. (7.1)}}{=\!=} \frac{2}{3}d\sqrt{\frac{2k_B}{eV_{\text{bias}}T}}\,. \tag{A.7}$$

The parameters in Table A.1 are used for computing the distribution of the charge cloud projections. Figure A.2 shows that the method of integrating the charge clusters along the MIP track results in a larger spike at $(0, 0)$ than the gaussian distribution. This means that the charges are more localised around the particle track. The cumulative distribution function (CDF) of both distributions (Figure

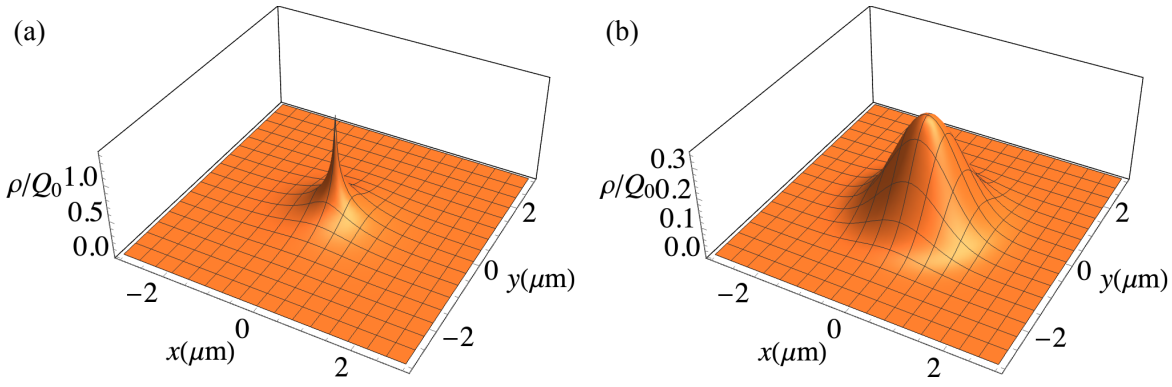



Figure A.2: Normalised distribution of the charge cloud projection using high voltage approximation. (a) The result using the integration (equation (A.4)); (b) the result using the 2D Gaussian distribution (equation A.6).

Table A.1: Example parameters for calculations of the charge cloud.

| **Substrate** | $Q_0$ (C) | $d$ (µm) | $T$ (K) | $V_{\text{dep}}$ (V) | $V_{\text{bias}}$ (V) |
|---|---|---|---|---|---|
| p-type | $1.137 \times 10^{-15}$ | 100 | 300 | 51 | 500 (high voltage)<br>100 (intermediate voltage) |

A.3) also shows the same conclusion. The distribution from the integration method shows a larger

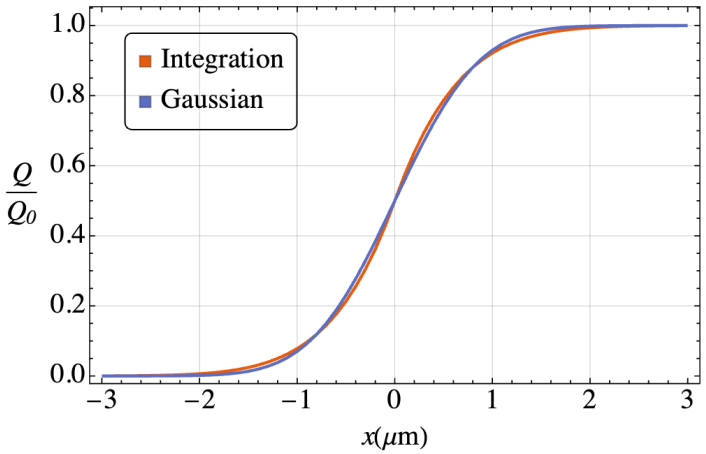



Figure A.3: CDF of the charge cloud projection distributions using the integration method and the 2D Gaussian method. The CDF is obtained by $\int_{100}^{x} dx' \int_{-100}^{100} dy \rho(x', y)$.

spread when the distance from the MIP track ($x = 0\,\mu m$) than approximately $0.8\,\mu m$. When it gets closer to the track, the increase of the charge density becomes higher, which is indicated by the larger slope of the CDF for $x \in (-0.8\,\mu m, 0.8\,\mu m)$. Nevertheless, almost all the charges are concentrated within approximately $2\,\mu m$ from the MIP track.

## Intermediate Bias Voltage

For intermediate bias voltages, such as $V_{bias} = 100\,V$, the equation (7.1) needs to be used to calculate a more accurate charge cloud width. Using the parameters in Table A.1, the charge cloud projection can be computed numerically (Figure A.4 (a)). As a comparison, the approximation using the Gaussian distribution is also calculated (Figure A.4 (b)). Both methods reveal a larger spread of the charge, due

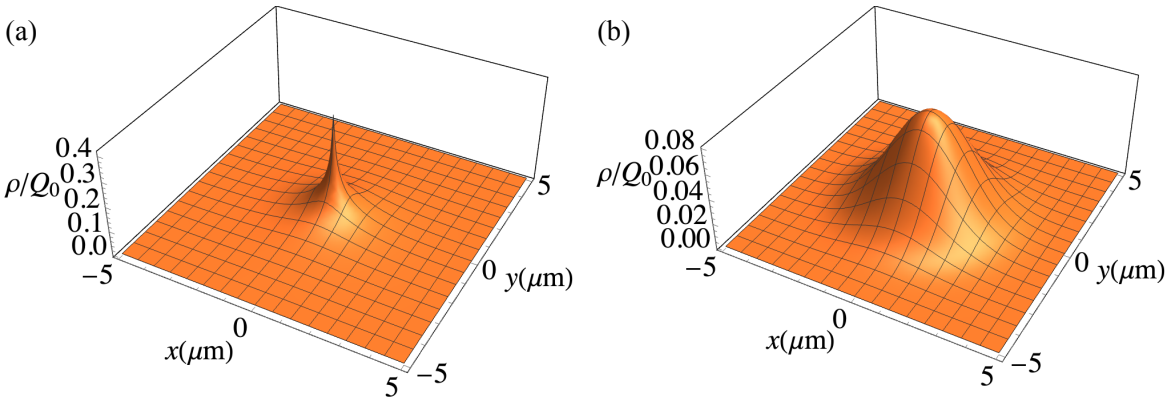



Figure A.4: Normalised distribution of the charge cloud projection for an intermediate voltage. (a) The integration method; (b) the 2D Gaussian with mean charge cloud width.

to the lower bias voltage (smaller electric field). Therefore, the drift time of the charge cloud to the

sensor surface is larger than in the high voltage case, and the transverse diffusion is stronger. Again, the integrated distribution delivers a more spiky peak than the Gaussian distribution. The CDF of both methods are computed in the same manner as in the previous section, and they are depicted in Figure A.5 for comparison. The relation between the two curves are the same as in the high voltage case (Figure A.3). Moreover, it can be identified that the most of the charges are concentrated within approximately 5 µm distance from the particle track, indicating the increased spread of the charge.

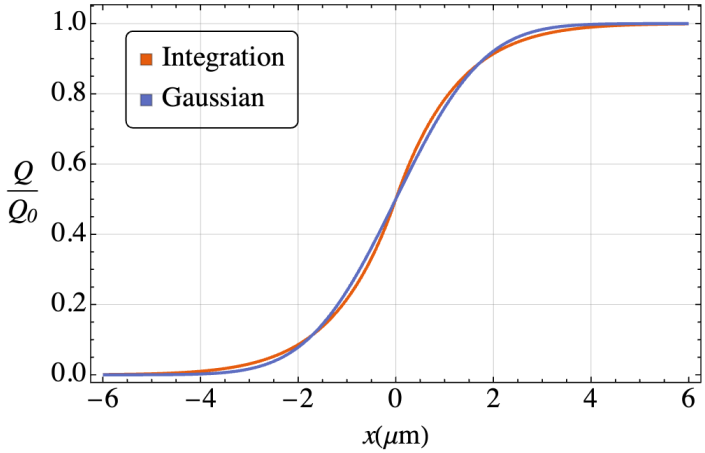



Figure A.5: CDF of the charge cloud projection distributions using the integration method and the 2D Gaussian method. The CDF is obtained by $\int_{100}^{x} \mathrm{d}x' \int_{-100}^{100} \mathrm{d}y \rho(x', y)$.

# APPENDIX B

# Determine the Breakdown Voltage Using Bias Resistors

A typical IV curve of such a measurement is illustrated in Figure B.1 (a). The slowly increasing current before the onset of breakdown indicates a resistive behaviour of a reverse biased sensor with an effective resistance much larger than the bias resistor. Plotting the voltage across the sensor as a function of the bias voltage (figure B.1 (b)) provides a different perspective, that the total voltage is almost entirely added on the sensor, giving $V_{\text{bias}} \approx V_{\text{sensor}}$. Whereas, the resistance of the sensor in the breakdown regime effectively vanishes, and the the IV curve follows the resistance of the bias resistor. This leads to a plateau in $V_{\text{sensor}}(V_{\text{bias}})$, indicating that the voltage starts to be loaded on the bias resistor. The $V_{\text{sensor}}$ at the turning point of the slope indicates the breakdown voltage.

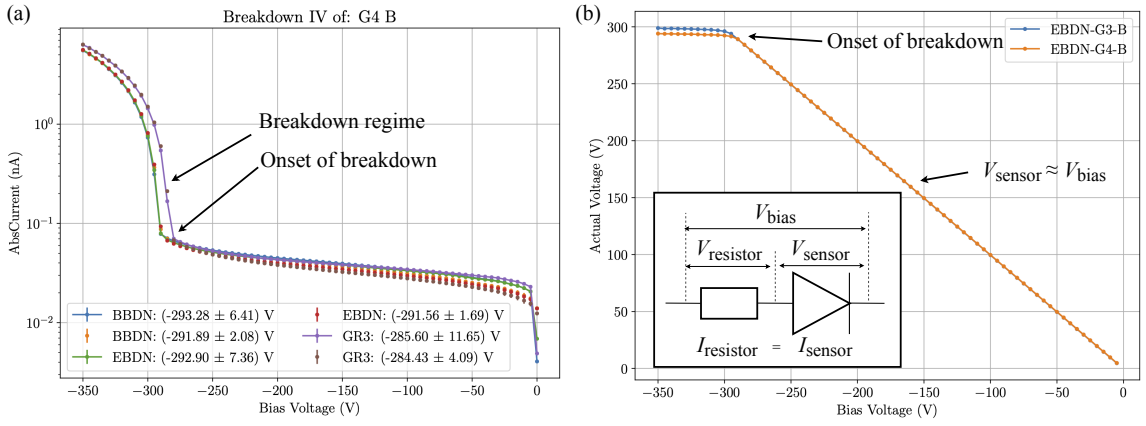



Figure B.1: Determine the breakdown voltage using bias resistor. (a): a typical IV curve of a silicon sensor with illustrating the breakdown regime. Before the onset of breakdown, the leakage current increases slowly within an order of magnitude. By using a bias resistor with resistance $R$, the slope of the IV curve is changed to $1/R$ after the onset of the sensor breakdown. (b): The plot of $V_{\text{diode}}$ vs. $V_{\text{bias}}$ calculated according to the voltage distribution $V_{\text{bias}} = V_{\text{sensor}} + V_{\text{resistor}} = V_{\text{sensor}} + IR$. Due to the large effective resistance of sensors, and the choice of the resistance, the voltage drop across the diode dominates the total bias voltage before the onset of breakdown. After that, $V_{\text{diode}}$ is merely unchanged with increasing $V_{\text{bias}}$.

To gain a better understanding of the bias resistor method, we can use analytical functions to model the current and voltage behaviour of the measurement circuit. We treat the sensor as a diode, and model the IV curve as

$$I_{\text{diode}} = \frac{V}{R_{\text{d}}} + I_0 \exp\left[a(V - V_{\text{BD}})\right] . \tag{B.1}$$

The linear term $V/R_{\text{d}}$ models a slow linearly increasing current before breakdown with the effective resistance $R_{\text{d}}$, and the breakdown regime is modelled using an exponential function with a nominal breakdown voltage $V_{\text{BD}}$, a constant parameter $I_0$, and a parameter $a$ to adjust the steepness of the curve. The modelled diode IV curve is plotted together with a resistor (with a resistance $R$) IV curve in figure B.1 (a). For the examples in this section: $R_{\text{d}}/R$ is set to be 1000, modelling a resistance difference of 3 orders of magnitude; $I_0$ is set to be $V_{\text{BD}}/R_{\text{d}}$, so that $I_{\text{diode}} = 2V_{\text{BD}}/R_{\text{d}}$; $a = 3$ is used in the example, which merely provides a steep increase of the current; and $V_{\text{BD}} = 200\,\text{V}$. The setting of the parameters in this section is merely modelling a generic IV behaviour of the diode for understanding. Since the

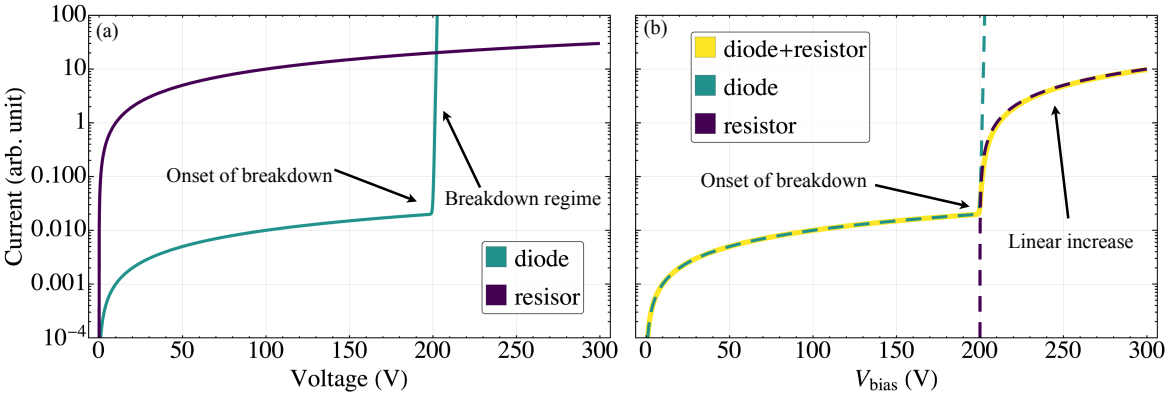



Figure B.2: (a): The modelled IV curve of a diode and a resistor. (b): the IV curve of the serially connected diode and resistor is a combination of the diode IV curve and the linear behaviour of the resistor after the breakdown. The IV curve of the resistor is shifted by the nominal breakdown voltage.

currents are the same in the serial configuration $I = I_{\text{resistor}} = I_{\text{diode}}$, the total current flow through the can be calculated by

$$I = \int_0^{V_{\text{bias}}} \frac{\mathrm{d}I}{\mathrm{d}V'_{\text{bias}}} \mathrm{d}V'_{\text{bias}} = \int \frac{1}{R_{\text{total}}} \mathrm{d}V'_{\text{bias}} , \tag{B.2}$$

Because the resistance of a diode is not defined, we can treat the derivative $\dfrac{\mathrm{d}V_{\text{diode}}}{\mathrm{d}I_{\text{diode}}}$ as $R_{\text{diode}}$, and

$$R_{\text{diode}}(V_{\text{diode}}) = \left(\frac{\mathrm{d}I_{\text{diode}}}{\mathrm{d}V_{\text{diode}}}\right)^{-1} = \frac{1}{1/R_{\text{d}} + I_0 \exp\left[a(V_{\text{diode}} - V_{\text{BD}})\right]} \tag{B.3}$$

is a function of the voltage across the diode. From the current and voltage relations we can derive that the total resistance is the sum of $R_{\text{diode}}$ and the resistor $R$, i.e., $R_{\text{total}}(V_{\text{diode}}) = R_{\text{diode}}(V_{\text{diode}}) + R$. The

relation between $V_{\text{bias}}$ and $V_{\text{diode}}$ is derived from the voltage relation and equation B.3, as

$$\begin{aligned} V_{\text{bias}}(V_{\text{diode}}) &= \int \frac{\mathrm{d}V_{\text{bias}}}{\mathrm{d}V_{\text{diode}}}\mathrm{d}V_{\text{diode}} \\ &= \int \left(1 + \frac{\mathrm{d}V_{\text{resistor}}}{\mathrm{d}V_{\text{diode}}}\right)\mathrm{d}V_{\text{diode}} \\ &= \int \left(1 + \frac{R}{R_{\text{diode}}(V_{\text{diode}})}\right)\mathrm{d}V_{\text{diode}} \\ &= \left(1 + \frac{R}{R_{\text{d}}}\right)\cdot V_{\text{diode}} + RI_0 \exp\left[a\cdot(V_{\text{bias}} - V_{\text{BD}})\right]. \end{aligned} \tag{B.4}$$

Hence the inverse function is given as

$$V_{\text{diode}}(V_{\text{bias}}) = \tilde{V} - \frac{1}{a}W\left[\tilde{a}\exp\left[a\cdot(\tilde{V} - V_{\text{BD}})\right]\right], \tag{B.5}$$

with $\tilde{V} = V_{\text{bias}}R_{\text{d}}/(R + R_{\text{d}})$, $W(x)$ the "Lambert W function", and $\tilde{a} = aRR_{\text{d}}I_0/(R + R_{\text{d}})$. Inserting equation B.5 into equation B.2 delivers the expression of the total current as the function of the bias voltage

$$I(V_{\text{bias}}) = \frac{\tilde{V}}{R_{\text{d}}} + \frac{1}{aR}W\left[\tilde{a}\exp\left[a\cdot(\tilde{V} - V_{\text{BD}})\right]\right] + C, \tag{B.6}$$

with a constant $C = W[\tilde{a}\exp[-aV_{\text{BD}}]]/aR$ approaching 0. The total current (eq. B.6) is plotted in figure B.2 (b), along with the IV curve of a diode and a resistor. From equation B.5 we can obtain the $V_{\text{bias}}$-$V_{\text{diode}}$ relation from the perspective of the analytical model (figure B.3), showing the same voltage behaviour from the breakdown measurement. Equation B.5 contains a linear part and a Lambert $W$

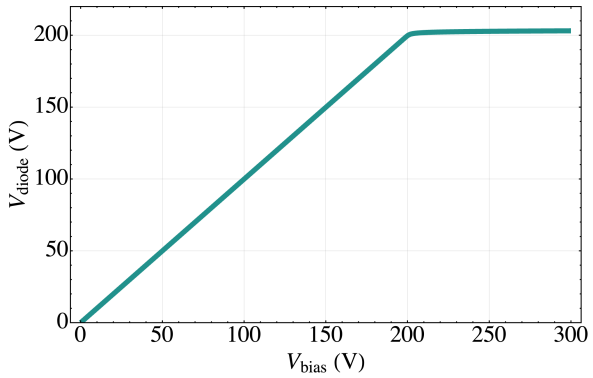



Figure B.3: The $V_{\text{bias}}$-$V_{\text{diode}}$ relation is reproduced using analytical models for I-V behaviour.

function part. For $V_{\text{bias}} < V_{\text{Bd}}$, the exponential term $\exp\left[a\cdot(\tilde{V} - V_{\text{BD}})\right]$ in $W$ function approaches to zero very fast, therefore, the value of the $W$ function approaches 0 as well. Hence, before the breakdown voltage, the linear term $V_{\text{diode}} \approx V_{\text{bias}}$ ($\tilde{V} \to V_{\text{bias}}$ for $R_{\text{d}} \gg R$) dominates, meaning that the total voltage is loaded on the diode. The same exponential term increases drastically for $V_{\text{bias}} > V_{\text{BD}}$, and the $W$ function is a monotonic increasing function. Therefore, both terms in equation B.5 start to cancel out, and the result is a very slowly changing curve. The turning point of the slope in the

diagram agrees with the predefined breakdown voltage of the model, which provides a theoretical explanation of the bias resistor method for breakdown measurement.

APPENDIX C

# Radiation Damage

Due to the small distance to the collision point of high energy colliders, silicon pixel detectors employed in the HEP experiments usually receive an enormous flux of high-energetic particles. Interactions between the sensor material and the continuously impinging particles can cause an accumulation of crystalline defects, which is originated from various interactions. Unlike doping processes, which also introduce crystalline defects in silicon, the defects caused by the radiations at high energy colliders is uncontrollable and usually not beneficial to the sensor performance. Studying the radiation damage in silicon particle detector is crucial for sensor design and detector handling, in order to mitigate the negative effects of radiation damage.

Two types of the radiation damage are categorised and named according to their locations in silicon sensors:

- ***Surface damage***:
  in the proximity of the $Si/SiO_2$ interface, which is at the surface of the silicon substrate.
- ***Bulk damage***:
  in the bulk of silicon substrate.

The surface damage is caused by the ***Ionising Energy Loss*** (IEL) of particles in the $SiO_2$. Electrons and holes can be produced by charged particles and photons in $SiO_2$, as introduced in section 3.1. Due to the large difference in the mobility of electrons and holes in $SiO_2$, electrons can be rapidly swept out under small electric field before recombining with holes. The slowly propagating holes are more likely to interact with intrinsic defects in the oxide, and forms electrically active defects. The dominating effects of such interactions is a build-up of locally fixed positive charges (***oxide charge***) in the proximity of the $Si\text{-}SiO_2$ interface, and the creation of extra energy levels in the silicon band gap at the interface (***interface traps***). Macroscopically, the interface traps causes an increase of leakage current (surface leakage) and charge carrier trapping. The positive charge at and close to the interface induces the electron accumulation at the surface of silicon, and causes an increase of surface conductivity.

When particles or neutral hadrons with sufficiently high energy penetrate through silicon, the contribution of non-ionising interactions, such as Rutherford scattering, nuclear elastic and inelastic scattering, will become considerable. Such interactions are categorised as ***Non-Ionising Energy Loss*** (NIEL), which causes the bulk damage in silicon substrate. The non-ionising interaction of incident

particles with silicon will cause phonon production and ***lattice atom displacements***. A vast amount of crystalline defects caused by NIEL in the silicon bulk introduces extra energy levels in the silicon band gap. Depending on the relative position of such levels to the mid-band gap energy, an increase in the leakage current (bulk leakage) can occur, and the charge carriers which generate the signals can be trapped. The NIEL can also provoke the deactivation of the dopants by forming defect complexes (donor/acceptor removal), so that the effective doping concentration of the sensor bulk is altered. The defects accumulate in the silicon sensor after long-term operations, and they can introduce extra energy levels in the band gap of the silicon substrate and introduce fixed charge in the $SiO_2$.

The general defect types and the mechanism of their formation are summarised in Figure C.1. As the radiation damage is a complex, and still an on-going topic in various field of research, this appendix is designed to offer a brief (but self-consistent) overview of the key defect formation mechanisms, the crucial impacts on silicon devices, and to provide a link to the dedicated literature.

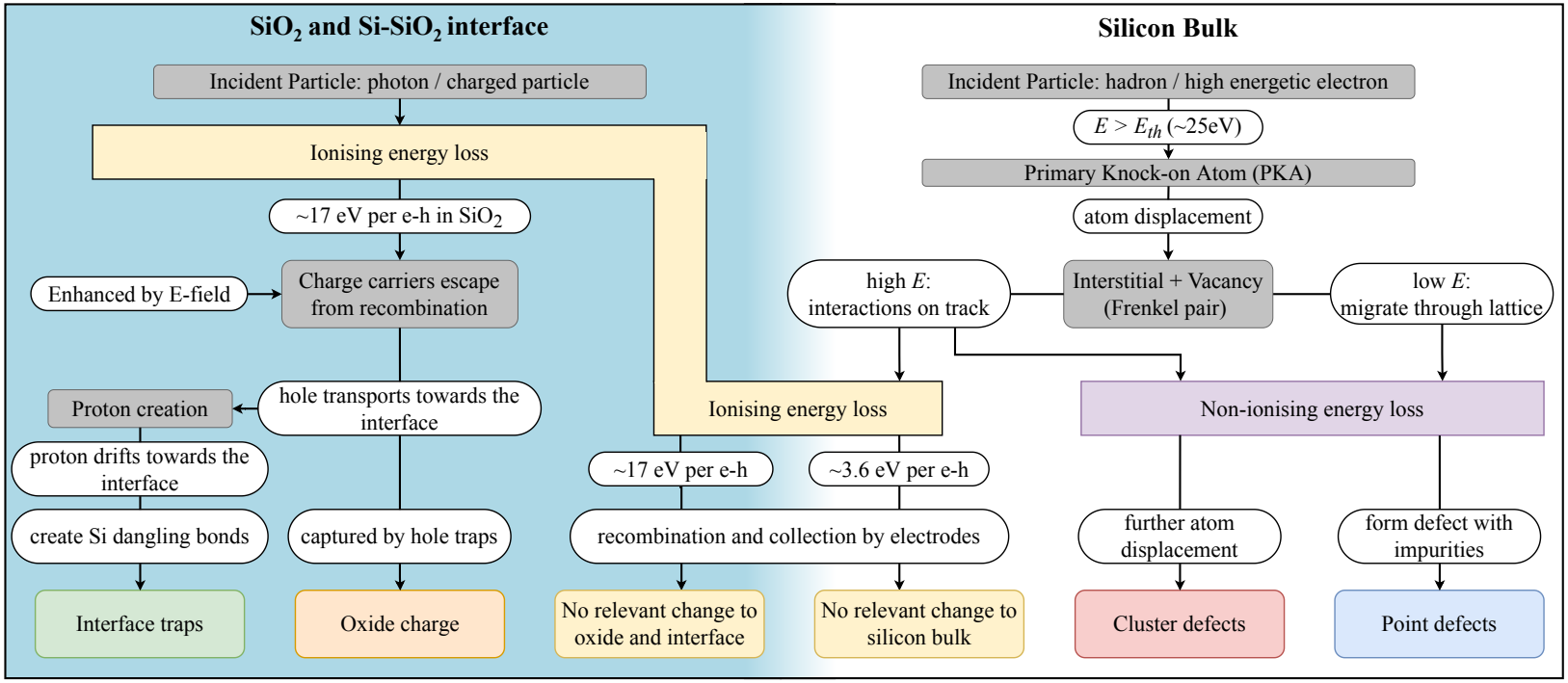



Figure C.1: Basic radiation-damage mechanism.

## C.1 Bulk Damage of Silicon Sensors

### C.1.1 Displacement Damage mechanism and NIEL

The damage by high energetic particles is originally caused by the displacement of the ***Primary Knock-on Atom*** (PKA). A threshold energy $E_{\text{th}} \approx 25\,\text{eV}$ is required to be transferred to the silicon atom by the impinging particle, in order to knock a silicon atom out of its lattice site. The transfer of kinetic energy depends on the mass of the incident particle, e.g., a neutron/proton needs an energy of approximately 185 eV, and an electron needs a kinetic energy of about 255 keV [93]. Vacancies and interstitials are mobile in silicon for temperature $T \geq 150\,\text{K}$ [94]. Therefore, they can migrate through the material, interact with each other or with other impurity atoms. Except for recombination, the migrating vacancies and interstitials produce localised defect structures. With sufficiently high recoil energy, the PKA can further interact with lattice atoms while penetrating, namely undergo IEL or NIEL. The NIEL of PKAs can cause further atom displacements and form a cascade. A large amount of energy can be deposited by the PKA at the end of the track, where a disordered region (defect cluster) can be formed. The formation of defect clusters requires a minimum energy transfer of approximately 5 keV to a silicon lattice atom. This corresponds to a minimum energy of 35 keV for neutrons/protons, and 8 MeV for electrons [93]. High energetic photons, for instance the gamma ray from $^{60}$Co with an energy in the order of 1 MeV, are able to produce displacement of a lattice silicon atom. However, it is not possible the create defect clusters, because the dominating interaction is the Compton effect, which cannot energise the secondary electrons up to the sufficient energy.

The quantification of the bulk damage uses the ***NIEL hypothesis***, which assumes that the lattice damage is scaled linearly with the NIEL and can be traced back to the abundance of the primary defects, independent of their initial energy and spatial distributions. Equivalently, can be scaled with the ***displacement damage cross section*** $D(E)$, with [93]

$$D(E) = \sum_i \sigma_i(E_{kin}) \int_0^{E_{R,max}} f_i(E_{kin}, E_R) P(E_R) \mathrm{d}E_R \,. \tag{C.1}$$

The displacement damage cross sections takes all possible interactions (summing over $i$ interactions) into account, with $\sigma_i(E_{kin})$ the interaction cross section and $f_i(E_{kin}, E_R)$ the probability of having a collision of a particle with kinetic energy $E_{kin}$, and transferring a recoil energy $E_R$. The Lindhard partition function $P(E_R)$ describes the portion of the PKA's energy available for displacing further lattice silicon atoms. It is nowadays a standard to scale the NIEL received by silicon detectors with respect to the NIEL caused by 1 MeV neutron. Therefore, the fluence received by the detector with spectrum $\Phi(E)$ can be scaled to the ***neutron equivalent fluence*** $\Phi_{\text{neq}}$ (or the equivalent fluence of 1 MeV neutron) , as

$$\Phi_{\text{neq}} = \kappa \int \Phi(E) \mathrm{d}E \,, \tag{C.2}$$

with the particle specific ***hardness factor***

$$\kappa = \frac{\int D(E)\Phi(E)\mathrm{d}E}{D(E_{\text{neutron}} = 1\,\text{MeV}) \int \Phi(E)\mathrm{d}E} \,. \tag{C.3}$$

Practically, the neutron equivalent fluence is used to indicate the bulk damage status of silicon detectors. However, the NIEL hypothesis can't be applied universally. The NIEL scaling is more suitable to be applied for hadron irradiation [95, 96] and citations therein.

#### Defect Annealing

Not only the radiation but also the lattice motion will alter the damaged crystalline structure. This phenomenon is called defect annealing. This process is normally achieved by keeping the irradiated silicon sensor at a certain temperature (usually higher than room temperature) for a certain time. Due to the increase in thermal energy in the crystal, the diffusion of the vacancies and interstitials is enhanced. The lattice defects can be repaired due to the migration and recombination (e.g. Vacancy + $Si_{interstitial} \rightarrow Si_{lattice}$), therefore it is possible to attempt to compensate the sensor degradation via annealing (***beneficial annealing***). Nevertheless, the larger defect clusters can be dissolved into smaller components, so that new and more defects can also be introduced in the annealing process. This process is the so-called ***reverse annealing*** that will lead to a degradation of the sensor performance. Besides, there exists the ***stable damage*** which can hardly be affected by thermal processes. For studying the radiation damage effects, the devices under test (DUTs) are usually annealed at 60 °C for 80 minutes after irradiation [94]. This standard annealing process reduces the leakage current level, in comparison with the condition immediately after irradiation, and prevent the effect from the annealing at room temperature. The irradiated or annealed DUTs are usually stored in a long temperature ambient to slow down the annealing process, so that the performance figures can be maintained for a long term storage.

### C.1.2 Defects Classification and Identification

The crystalline defects in irradiated silicon sensors are found to be generally classified into ***point defects*** and ***cluster defects***, according to the dimension and structure of the defect sites.

#### Point Defect

A point defect is a crystal distortion that associates only with a single lattice point. In radiation damage, point defects are also known as isolated defects due to the fact that they have small sizes and large distances between each other. Figure C.2 illustrates a number of point-like crystalline damages. The impurity substitute is a defect where a silicon atom on the lattice site is substituted by a different element. The dopant in doped silicon is a typical case of impurity substitute. The impurities, such as oxygen and carbon, are introduced in the manufacturing of crystalline silicon, and the atoms locate between lattice points. This type of defect is known as impurity interstitial. The defect types mentioned above can interact with each other, forming more complex structures. Some common examples are di-vacancies $V^2$ that are formed by two adjacent vacancies, or vacancy-impurity complexes such as a vacancy-oxygen (VO) complex. The impurities can also bond with each other, such as a carbon-oxygen complex (CO).

#### Cluster Defect

As agglomerations of defects, the properties of cluster defects are still not well understood [97]. Experiments and numerical simulations have been employed to understand the nature of cluster

damage (see [96, 98] and the citations therein). According to the Molecular-Dynamics simulation, the cluster is revealed to be a local amorphous volume with size $\lesssim 5$ $\mu$m that is caused by the melting of silicon at the end of a PKA track, due to a large energy deposition in a small volume [98]. Another interpretation suggests that the defect cluster is, instead, an agglomeration with high-concentrated $I-V$ bond defects [99]. Such a distorted region consists of interstitials, vacancies, and I-V pairs that have various combinations, configurations, and concentrations.

Studies have shown that the ratio of point and cluster defect production depends on the type of the incident particle (see [98] and citations therein). Considering only the PKA recoil energy, the ratio of deposited energies $E_{\text{cluster}}/E_{\text{point}}$ stays around 0.59 for $E_{\text{PKA}} \geq 20$ keV [98]. The ratio holds for proton irradiation if the proton produces high-energetic PKA. For low-energetic protons, the Coulomb interaction leads to a direct production of point defects. The ratio was obtained to be $\sim 0.35$ for low energetic proton irradiation. This means that the proton produces more point defects than cluster defects. On the contrary, neutron-atom interaction is dominated by elastic scattering, which has a higher mean energy transfer in comparison with the Rutherford scattering for the proton-atom interaction [100]. Therefore, for low energetic neutrons, the production of point defects is limited. The investigation of the sensor that is radiated by high-energetic electrons has shown energy-dependent populations of defect points and clusters [96].

### Defect Identification

In the microscopic point of view, the defects change the local crystalline structure and thus change the local energy feature. Associating the knowledge of the doped semiconductor (section 2.2), it can be interpreted that the general electrically active crystalline defects can introduce extra energy levels (***defect levels***) in the semiconductor band gap. Therefore, the identification of defects is essentially determining their energy levels, concentrations as well as chemical structures. The energy levels of these defect levels can be measured through the Deep Level Transient Spectroscopy (DLTS) or the Thermal Stimulated Current (TSC) [94], and a Transition Electron Microscope (TEM) can be adopted to see the chemical composition [101].

The energy levels of defects can be labeled by their distance to valence band, conduction band, or

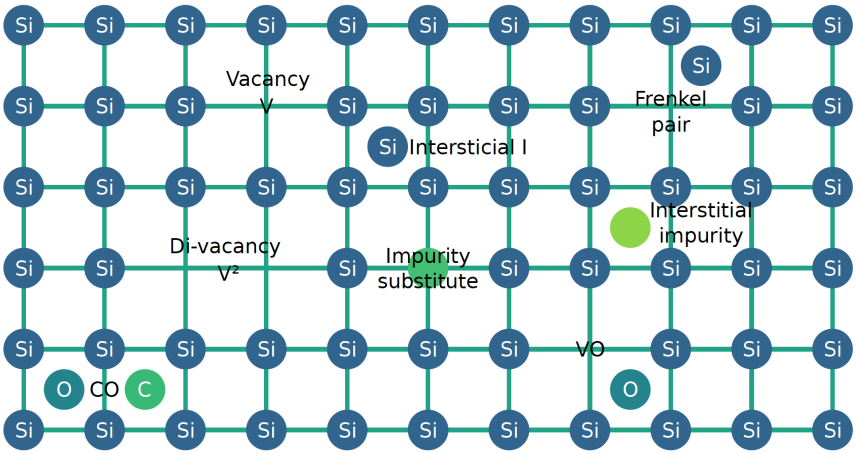



Figure C.2: Conceptional illustration of point defects in silicon. [38]

the intrinsic Fermi level. For example, a defect with energy $E_t$ will be labelled as $E_t = E_C - \Delta E_t$ or $E_t = E_V + \Delta E_t$, with $\Delta E_t = |E_{C,B} - E_t|$. Depending on the position of the energy level, defects can be further classified into the following groups:

#### 1. Shallow and Deep levels

The shallow level refers to the defect with a small $\Delta E_t$. In other words, the shallow levels are located near the conduction band or valence band. The deep level refers to the defect with $\Delta E_t \approx E_g/2$. The exact range of the shallow or deep levels' energy is not strictly defined. It is common that the defects which can be ionised at room temperature are attributed to shallow levels. However, the charge state of defects are also influenced by the Fermi-level of the material [94]. Thus the definition of shallow and deep levels can vary for different materials.

#### 2. Electron and Hole Traps

Intuitively, defect levels are commonly treated as "traps" for charge carriers because electrons and holes have the possibility to "drop" onto these levels from the conduction band or valance band. The electrons or holes in these defect levels don't contribute to the charge transportation until they are released again after a certain time. Thus the trapping of electrons and holes will lead to the altering of electrical properties of the sensor (see next section). The trapping ability of traps is primarily characterised by the ***capture cross section*** $\sigma_{n,p}$. A more frequently used characteristic parameter the ***trapping time*** $\tau_{e,h}$, which is closely related to $\sigma_{n,p}$, will be introduced in more detail later.

#### 3. Acceptor and Donor levels

The defect levels change electrical properties not only through the charge carrier trapping but also the change of their own charge states during capture and emission processes. Typically, a donor level will be neutral if it captured an electron (occupied) and will be positively charged after emitting an electron (empty); an acceptor level will gain negative charge if it's occupied, and will be neutral if it's empty. For convenience, the charge states of a defect level are labeled by symbols "+", "∘" and "-" to indicate a positive, neutral and negative charge state, respectively. Examples of defect levels and their charge states are illustrated in Figure C.3. The boron dopant (analogous for phosphorus) denoted by $B_s$ [1] is a typical acceptor level that is ionised (occupied by an electron / emits a hole) at room temperature, and has a negative charge state of one elementary charge. The deeper levels such as $VO_i$ [2] and $C_iO_i$ are not ionised at room temperature. Therefore, the change of their charge states will only depend on capture and emission of electrons. In addition, defects like the Thermal Double Donor [3] ($TDD$) has more than two charge states. Besides, the di-vacancy $V_2$, known as amphoteric level, it can have three different energy levels depending on the structure. Therefore, a $V_2$ defect can be either donor or acceptor.

[1] The subindex "*s*" indicates the substitute impurity atom.

[2] The subindex "*i*" indicates the interstitial impurity atom.

[3] The thermal donor is a defect of oxygen impurities. Depending on the number of oxygen atom and structure, the defect has distinct properties. The thermal donors are normally introduced during the manufacturing process, or precisely the thermal process since the formation rates depend strongly on temperature. With special care on temperature, the thermal donor population can be suppressed. (see e.g. [94] and citations therein)

### C.1.3 Phenomena and Modelling of Macroscopic Effects

The most relevant macroscopic effects after irradiation are: increase of leakage current, decrease of charge collection efficiency, change of the effective doping concentration, and change of the space charge distribution (electric field distribution). In this section, the phenomenological models as well as the models based on SRH statistics are introduced for these effects.

#### Bulk Leakage Current

In a silicon detector under reverse bias, the leakage current (or dark current) refers to the small current mainly caused by the thermal generation of e-h pairs. Defect levels introduced by the radiation damage enhance the charge generation. From Eq. (2.22), the net generation rate $G = -U$ in the space charge region ($n, p \approx 0$) leads to

$$G(T) \approx N_t c_t n_i \left( 2 \cosh\left( \frac{E_i - E_t}{k_B T} \right) \right)^{-1} , \tag{C.4}$$

where the capture coefficients $c_{n,p}$ are assumed to have the same value $c_t$. At a certain temperature, $G(T)$ reaches the maximum when $E_t = E_i$ and decreases when $\Delta_t = |E_i - E_t|$ increases. In other words, the defect levels which locate close to mid-gap have higher generation rates than the ones closer to edge of energy bands. For a higher temperature, $G(T)$ decreases more slowly with $\Delta_t$. Thus more defect levels can possibly contribute to the leakage current. On the contrary, at lower temperatures, the charge generation will be dominated by the levels with very small $\Delta_t$.

Considering several different defect levels $E_{t,j}$, the total bulk leakage current can be calculated as

$$I_{\text{leak}} = eV \sum_j G_j , \tag{C.5}$$

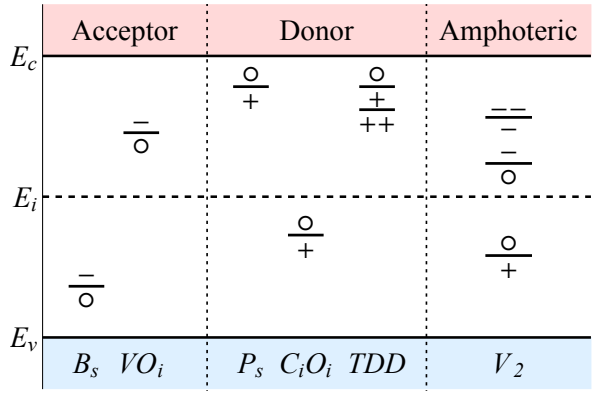



Figure C.3: Schematic energy levels and charge states of a selection of defects. The defect levels are represented by horizontal bars. It can be simply interpreted that the charge state will change to the upper one when capturing an electron and *vice versa*. As for the $TDD$, the charge states can be understood as capturing/emitting multiple electrons. A more formal interpretation of the change of charge states is that when Fermi-level lies above the defect level, the level will have the upper charge level and *vice versa*. (This figure is modified from the figure in [94].)

with $e$ the elementary charge, $V$ the volume of depletion region. Assuming the concentration of defects increases linearly with $\Phi_{\text{neq}}$, the concentration $N_{t,j} = \eta_j \times \Phi_{\text{neq}}$ with the ***introduction rate*** $\eta_j$. Thus, a fluence-dependent leakage current can be formulated according to Eq. (C.4) and (C.5) as

$$I_{\text{leak}} = e \sum_j \frac{\eta_j c_{t,j} n_i}{2\cosh[(E_i - E_{t,j})/k_B T]} w A \Phi_{\text{neq}}. \tag{C.6}$$

From various experiments (see e.g. [102]), the relation

$$\Delta I_{\text{leak}} = \alpha V \Phi_{\text{neq}} \tag{C.7}$$

with a linear dependence on $\Phi_{\text{neq}}$ is obtained. $\Delta I_{\text{leak}}$ is the increase in leakage current, and $\alpha$ is the ***current-related damage factor*** which defines the proportionality. This relation is independent of the type of silicon (impurity or doping and their amount) and the type of damaging radiation (neutron, proton, etc.) for a certain temperature and annealing history. Following the standard annealing process, 60 °C for 80 min, the universal factor $\alpha_{80/60} = (3.99 \pm 0.03) \times 10^{-17}$ A cm$^{-1}$ is obtained [94]. $\alpha$ decreases exponentially in terms of the annealing time and annealing temperature for a short term annealing procedure. For a long term annealing, the factor grows logarithmically in annealing time at room temperature. The generation rate derived from SRH statistics reveals a temperature dependence of the leakage current, as well. The derivation from the equation (C.4) leads to the relation

$$I_{\text{leak}}(T) \propto T^2 \exp\left(-\frac{E_{\text{eff}}}{2k_B T}\right), \tag{C.8}$$

as shown in [103]. $E_{\text{eff}}$ is an effective value that contains the temperature dependent band gap energy of silicon. It has been determined in [103] that $E_{\text{eff}} = (1.214 \pm 0.0014)$ eV for both p- and n-type silicon with $\Phi_{\text{neq}}$ up to $10^{15}$ cm$^{-2}$. This value can be translated to a 10% change in leakage current per degree for $-20\,^{\circ}\text{C} < T < 20\,^{\circ}\text{C}$ [38]. The charge generated by defect levels dominates the leakage current in an irradiated sensor. Therefore, the operation temperature of irradiated sensors needs to be sufficiently low to suppress leakage current.

#### Charge Collection

The trapping of charge carriers by defect levels causes the lost of charges, and hence, affects the charge collection ability of silicon detectors. The effect of charge carrier trapping associated with defect levels can be parametrised as $Q(t) = Q_0 \exp(-t/\tau_{\text{eff}})$, with $Q_0$ the initial amount of the excess charge, $\tau_{\text{eff}}$ the ***effective trapping time*** [4]. The effective trapping time for e/h is defined by considering multiple levels as

$$\tau_{e,\text{eff}}^{-1} = v_{\text{th},e} \sum_j \sigma_{n,j} N_{t,i} (1 - f_t(E_{t,j}, T)) \qquad \tau_{h,\text{eff}}^{-1} = v_{\text{th},h} \sum_j \sigma_{p,j} N_{t,i} f_t(E_{t,j}) \,. \tag{C.9}$$

Although the formulae above are originally for equilibrium states, they are also presumed valid with the existence of an external electric field, since the drift velocity is much smaller than thermal velocity [104]. It is evident that the electron/hole trapping will be dominated by the defect levels close to

[4] The inverse of it is also known as effective trapping probability

the conduction band/valence band due to the difference in trap occupancy $f_t(E_t)$. Analogous to the treatment for Eq. (C.6), a linear dependence of $\Phi_{\text{neq}}$ can be deduced for effective trapping time. This is in agreement with the parametrisation of $\tau_{\text{eff}}$ according to experiments (e.g. [104]), that the inverse of trapping time is linear in $\Phi_{\text{neq}}$

$$\tau_{\text{eff}}^{-1} = \tau_{\text{eff},0}^{-1} + \beta\Phi_{\text{neq}}. \tag{C.10}$$

$\tau_{\text{eff},0}$ is the effective trapping time before irradiation and $\beta$ is the proportionality factor. With a weak dependence on material type, $\beta_e$ has values from 4 to $6 \times 10^{-16}$ cm$^2$/ns and $\beta_h$ has values of $5 \sim 8 \times 10^{-16}$ cm$^2$/ns. Typically, the effective trapping time is in the order of several nanoseconds for $\Phi_{\text{neq}}$ above $10^{14}$ cm$^{-2}$. Thus, if the drift time of the charge carriers is comparable or longer than the $\tau_{\text{eff}}$, the resulted signal will be reduced considerably. The characteristic time for de-trapping has, however, a scale of $\mu s$ which is much longer than the integration time of silicon detectors [105]. Therefore, the de-trapping of charges is normally neglected.

The temperature dependence of $\beta$ can be deduced by comparing Eq.(C.9) and (C.10). The derivation in [104] has shown that

$$\beta_{e,h}(T) = \beta_{e,h}(T_0)(T/T_0)^{\kappa}_{e,h} \tag{C.11}$$

with constant parameter $\kappa_e = -0.86 \pm 0.06$ and $\kappa_h = -1.52 \pm 0.07$ for all types of particles. The constant $T_0$ came from a model of capture coefficients $c_{n,p}$ in [106]. Concerning annealing effects, *Kramberger et al.* [107] have shown the change of $\beta$ with respect to annealing time and temperature. The study revealed an increase/decrease of effective trapping probability for hole/electron respectively after various annealing processes.

### Space Charge

The space charge in the depletion region reflects the ***effective doping concentration*** ($N_{\text{eff}}$), which determines the electric field distribution, and the full depletion voltage $V_{\text{FD}}$. Three effects can alter the space charge: occupation of donor/acceptor levels, ***donor/acceptor removal***, and charge carrier trapping through deep levels.

Consider the donor and acceptor levels with concentration $N_{\text{t,D}}$ and $N_{\text{t,A}}$,

$$N_{\text{defects}} = e \sum_{\text{Donors}} N_{\text{t,D}} f_{t,D}(E_{t,D}) - e \sum_{\text{Acceptors}} N_{\text{t,A}} f_{\text{t,A}}(E_{\text{t,A}}) \tag{C.12}$$

can describe the contribution of these defects to $N_{\text{eff}}$.

The donor/acceptor removal can be attributed to the circumstance that the existing dopant impurities are deactivated by forming complexes with other defects. Studies [100] on the irradiated silicon sensors using n-type substrate has shown, that the vacancy-phosphorus (V-P) and vacancy-boron (V-B) complex induced by neutron irradiation deactivate the dopants, and hence leads to a change in $N_{\text{eff}}$. The defect V-B complex is unstable at room temperature, therefore, the irradiated n-type silicon eventually exhibits a decreasing number of activated phosphorus atom (donor removal), due to the remaining V-P complex. In addition to the donor removal, most of the defects created by irradiation possess a negative charge state, which results in a net negative space charge after high irradiation. This effect is termed as the ***Space Charge Sign Inversion*** (SCSI).

A ***Double Peak*** (DP) shaped electric field has been found in the silicon sensors after neutron irradiation. Such an effect is explained by the model of non-uniform space charge distribution caused

by the free charge carrier trapping through deep levels [108]. The formation of the double peak electric field is illustrated in Figure C.4, considering a fully depleted sensor with $n^+$ and $p^+$ as the electrodes. If the bias voltage is lowered, the region near the electric field's minimum will be lowered and eventually be undepleted. In this case, the sensor has effectively two junctions and an undepleted area between them. Thus, the DP effect is also known as Double Junction effect. It is indicated in [110] that improving the depletion via raising voltage can cause a high electric field near the electrode, which increases the possibility of avalanche breakdown.

The evolution of space charge after irradiation can be concluded as

$$N_{\text{eff}}(z) = N_{\text{dopants}} + N_{\text{defects}} + N_{\text{freecharge}}(z) \,, \tag{C.13}$$

where $N_{\text{dopants}}$ is the contribution from ionised dopants and donor/acceptor removal, $N_{\text{defects}}$ is from the occupancy of shallow donor-/acceptor-like defects and the position dependent $N_{\text{freecharge}}(z)$ is the effect from the deep level free charge carrier trapping.

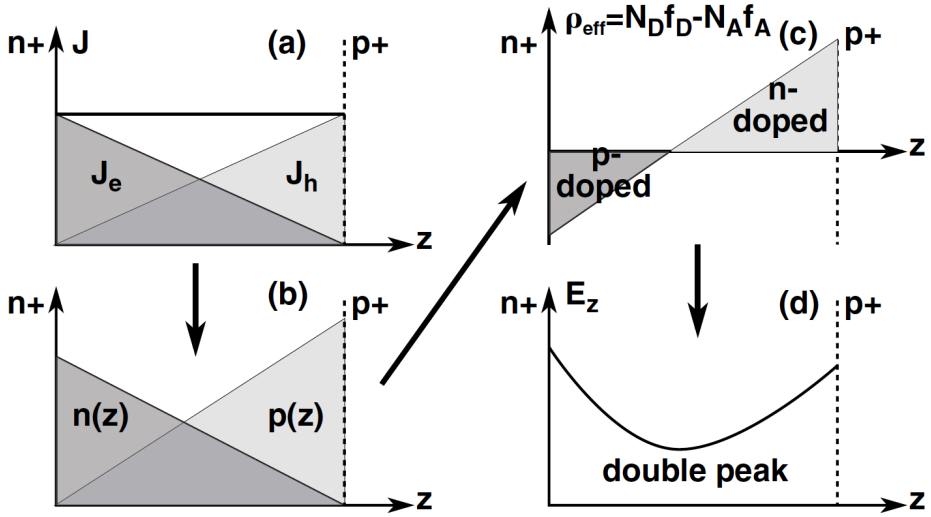



Figure C.4: Sketch of the deep-level trapping caused electric field with double-peak [109]. (a): the thermally generated current $J$ is uniformly distributed in the depletion region. The electron and hole component are linear functions of the depth $z$ in sensor, according to the continuity equations. (b): the stationary charge density $n(z)$ and $p(z)$ distribute linearly in $z$. The slightly different shape is the result of the different mobility. (c) after considering the charge carrier trapping, the occupancies of the donor- and acceptor-like deep levels cause a position-dependent space charge distribution, since the local deep level occupancy is affected by the free charge concentration (see Eq. (C.12) and (2.21)). (d): a parabolic electric field distribution with two peaks on both ends of the sensor bulk is obtained through integrating the space charge distribution.

## C.2 Surface Damage

### C.2.1 The Formation of Damage in $SiO_2$ and at the Si-$SiO_2$ Interface

High energy charged particles and photons undergo the ionising energy loss in the material, as introduced in section 3.1. The required average energy to create an e-h pair in $SiO_2$ is $(17 \pm 1)$ eV [111], which is much higher than the necessary energy for Si crystal, due to the larger band gap $E_{g,\,SiO_2} = 8.06\,\text{eV}$ of the thermal $SiO_2$ grown on Si determined at room temperature [112]. Unlike the radiation damage caused by NIEL, the formation of the surface damage is originated from the interactions between the ionised charge carriers and the intrinsic crystalline defects in the $SiO_2$ and at the $SiO_2$-Si interface, so that the existing defects become electrically active. The major effects introduced by the surface damage are the build-up of positive charge and the increase of leakage current [113]. The Total Ionising Dose (TID) is a quantity being used to evaluate "how much damage" a semiconductor device has received from the IEL after the exposure of ionising radiations.

#### Intrinsic Defect

Contaminations and intrinsic lattice defects in $SiO_2$ are introduced in the manufacturing processes. The contamination of mobile alkali ions (e.g. $Na^+$, $Ka^+$) can cause a stability problem of a semiconductor device under high electric field and high temperature ($> 100\,°C$) operations, due to the increased mobility[6]. Nevertheless, the modern oxidation technology ensures a low contamination of such ions[114]. Chemical compounds containing hydrogen, such as $H_2$, $H_2O$, and HCl, are common ingredients for the oxidation or related processes [4]. Hydrogen related impurities in the $SiO_2$ layer can be mobile (in the form of ions) or bonded with the crystal structure of $SiO_2$. A number of intrinsic defects in $SiO_2$ are summarised in [115, 116], including the lattice defect, e.g., trivalent silicon [5] $O_3{\equiv}Si\cdot$, the oxygen vacancy $V_O$ (or $O_3{\equiv}Si{-}Si{\equiv}O_3$), the interstitial oxygen $O_I$, and the hydrogen related defects, e.g. $O_3{\equiv}Si{-}H$. The defects in $SiO_2$ are predominately donor states, which can contribute to a positive space charge after interactions with charge carriers. Although the defect sites locate through out the $SiO_2$ layer, the region in the proximity of the Si-$SiO_2$ interface (within several nm in $SiO_2$ [117]) has a much larger concentration of defects (especially oxygen vacancies), due to the lattice mismatch, the out-diffusion of oxygen atoms [113], or the incomplete oxidation [118]. The lattice mismatch at the Si-$SiO_2$ interface results in the trivalent silicon atom bonded with three other silicon atoms $Si_3{\equiv}Si\cdot$ with a dangling bond extending into the oxide, which is electrically active. The dangling bond can be passivated through forming $Si_3{\equiv}Si{-}OH$ [115] or $Si_3{\equiv}Si{-}H$ [119]. Researches [120] have shown another perspective, suggesting that the original lattice distortion at the interface is the weak Si-Si bond (as $Si_3{\equiv}Si{-}Si{\equiv}Si_3$), which can be transformed to two (passivated) trivalent Si via hole trapping or interacting with $H_2$.

#### IEL Induced Defects

According to the effects, as the charge build-up and the increase of leakage current, the defects in the oxide and at the interface can be categorised into 5 types [121, 122]:

- **Mobile ionic charge** This is generally not an issue for modern semiconductor devices.

[5] A silicon atom having 3 covalent bonds and a nonbonding electron. The chemical notation of this chapter: a dash " – " denotes a covalent bond, and a dot " · " denotes a nonbonding electron

- **Oxide trapped charge** Electrons and holes can be trapped by defects in the bulk of the $SiO_2$ layer of semiconductor devices. After trapping, the defects site can be negatively or positively charged, depending on the type of the trap and the type of the trapped charge carrier. For instance, a hole trap will contribute a positive space charge after trapping a hole.
- **Fixed oxide charge** Because of the higher concentration of the intrinsic defects in the in the region of $SiO_2$ near the $SiO_2$-Si interface, the concentration of oxide charge is higher in this region than in the oxide bulk. Especially, deep level hole traps in such region provides stable positive space charges after trapping the holes.
- **Interface trapped charge (interface traps)** Dangling bonds at the interface introduces a continuous distribution of defect levels in the silicon band gap. Due to the special location, the charge carriers from the silicon bulk can interact with the traps according to the potential configuration across the interface. Such traps can contribute to space charges via trapping as a part of the oxide charge, or act as generation centres of leakage current.
- **Border traps** Within $\sim 3\,\text{nm}$ (border region) from the interface, there exists traps in $SiO_2$ can also interact with the charge carriers, which tunnel from the silicon bulk. Due to the longer distance for tunnelling process, the responding time is typically slower than the interface traps.

The location of these defect types are schematically illustrated in Fig. C.5. Besides the classification based on the spatial location (labelled as "traps"), the defects can be categorised based on the electrical properties (labelled as "states"). The interface traps and the border traps, which can directly communicate with the silicon bulk, are named as "switching states", whereas the rest of traps in the silicon oxide bulk are labelled as "fixed states" [123].

#### Formation Mechanisms and Flow

To understand the underlying physical and chemical mechanisms, which forms the aforementioned defects, models have been proposed, experiments have been conducted to gain the full picture of the surface damage. After decades of study, the major physical processes of the defect formation has become more and more clear. Commonly, the formation of the radiation damage is discussed based on a MOS structure, as shown in Figure C.5. A positive voltage at the metal gate (potential at the metal layer is higher than at the silicon) creates an electric field across the oxide layer, where the holes transport towards the Si-$SiO_2$ interface.

**Charge Yield** Prompt recombinations of electrons and holes takes place as the charges are created by ionising irradiations, and the recombined charges will not contribute to the formation of defects. The portion of the charge which escape from the recombination is described by the fractional charge yield $f_y$, which depends on the electric field strength and the type of impinging particles (Figure C.6). Electrons are less interesting than holes for the formation of surface damage, since they will be quickly removed by the metal electrode, due to the higher mobility [6].

[6] The mobilities of electrons and holes in $SiO_2$: $\mu_{e,SiO_2} \approx 20\,\text{cm}^2/\text{Vs}$, $\mu_{h,SiO_2} \approx 2 \times 10^{-5}\,\text{cm}^2/\text{Vs}$ [93]. Typically, the total drift time of electron in the oxide is in the order of picoseconds, whereas the holes needs seconds or longer time to reach the surface of the oxide [118].

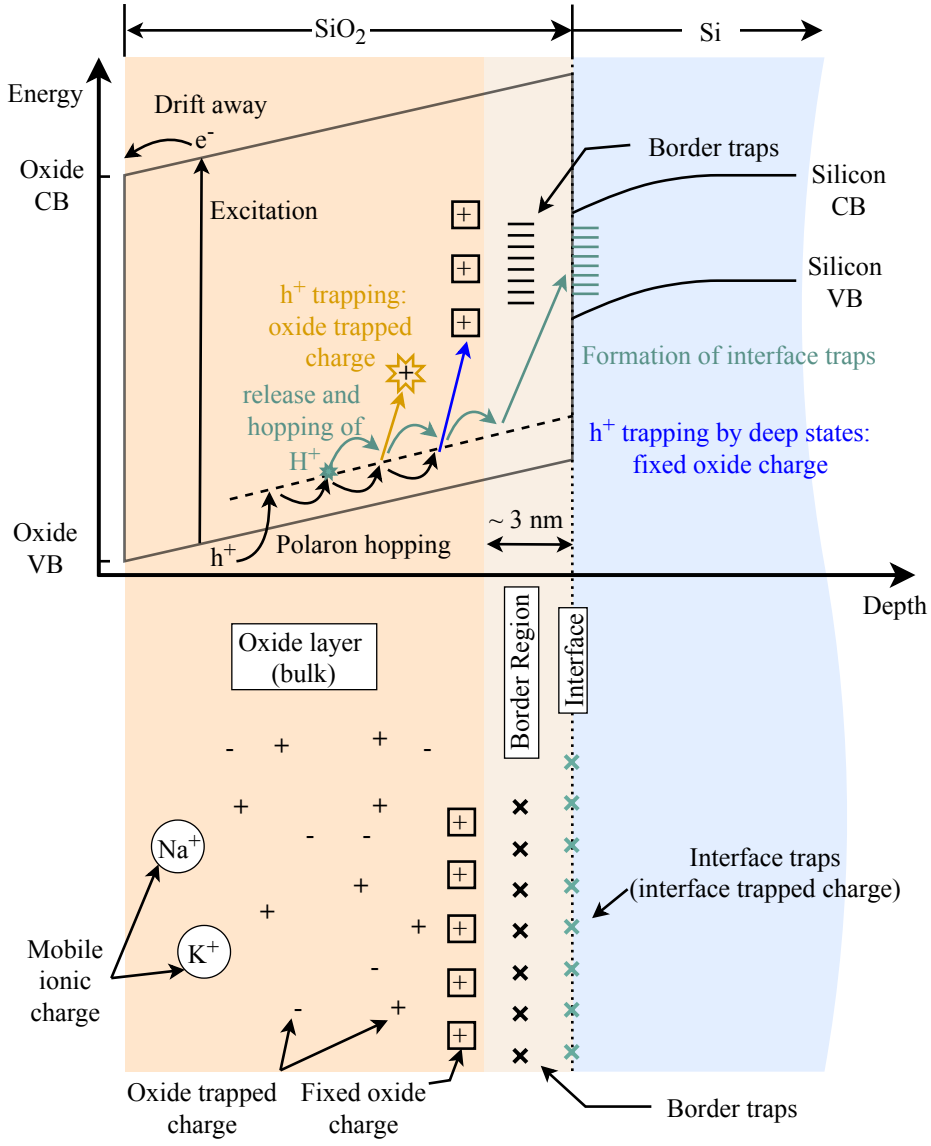



Figure C.5: IEL caused defects and their formation. The metal layer is on the left hand side of the $SiO_2$, and it is not illustrated here. The upper part of the figure indicates the major physical processes of the defect formation based on a schematic band diagram between the $SiO_2$-Si interface. The lower part of the figure schematically illustrates the location/types of the charges/states in the oxide and at the interface. (Made according to the figures and information in [113, 118, 121, 123–125])

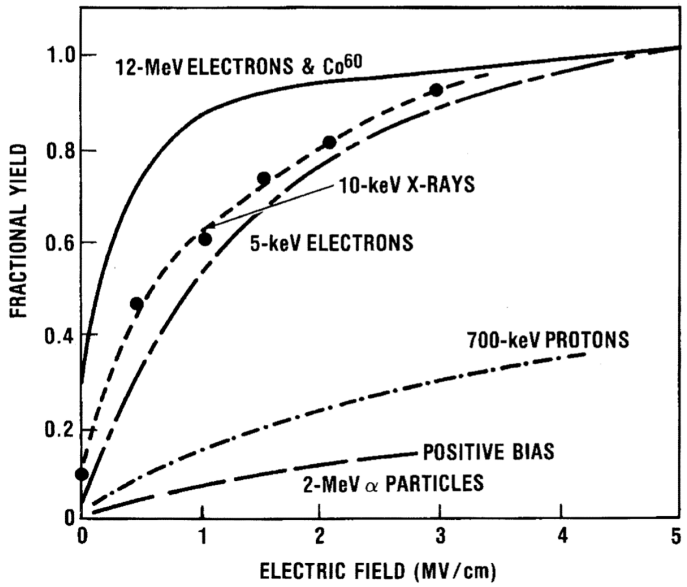



Figure C.6: Fractional charge yield of $SiO_2$ for different particles as a function of the electric field strength. [118]

**Hole Propagation** The nature of the hole propagation in $SiO_2$ has been found to be highly dispersive, electric field and temperature activated [126]. The transport can take place over decades in time (i.e. the time scale spreads over orders of magnitudes), revealing a very slow propagation, which cannot be explained by the simple model considering a uniform concentration of holes of the same mobility [127]. By providing the best overall descriptions of the hole transport properties ([118] and citations therein), the hole transport data has been well modelled by the Continuous-Time Random Walk (CTRW) hopping transport formalism [7] [118], where small polarons [8] formed by holes and the induced local defect are driven by the electric field. The highly activated transport for temperature above 140 K is the strongest evidence of the hopping process. Due to the slow propagation, the excess holes in oxide bulk contribute to the positive space charge, similar as the trapped holes which form oxide trapped charge. Thus the sweeping out process of the holes gives a rise of a time dependent flat-band/threshold voltage shift in a MOS device (Fig. C.7 curve section (2) and (3)) after exposure of a short irradiation pulse.

**Interaction of Holes with Defects** A portion of holes can be trapped by the hole trapping centres during the transport, and contribute to localised positive space charges. The amount of the trapped

[7] The "multiple-trapping model" is another model for understanding the hole transport phenomenon, where the holes are continuously trapped and released by various trapping levels all across the oxide [128]. This model explains many features of the experimental data, as well [118].

[8] Charges like holes in $SiO_2$ interact strongly with the lattice atoms in their immediate vicinity causing a local lattice polarisation and distortion, which can be intuitively understood as a cloud of virtual phonons surrounding the charge carrier. Such a local distortion creates a potential basin and traps the holes [129]. The size of polarons is classified by the radius of the phonon cloud. A large polaron has a radius larger than one lattice constant, whereas a small polaron has a radius within a unit cell [129]. The charge and the phonon cloud form a polaron, which increases the effective mass and reduces the mobility of the charge carriers.

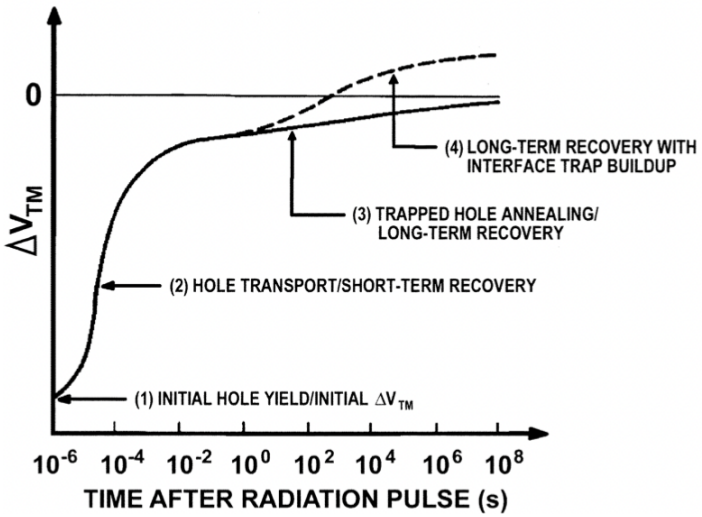



Figure C.7: A typical recovery curve of the threshold voltage of an n-channel MOSFET. The y-scale represents the relative difference between the pre- and post-irradiated condition. The time dependent threshold shift indicates the development of the space charge in the $SiO_2$ and its interface to the Si substrate. In this example, the initial positive threshold shift represents the excess of positive charge. This diagram is not obtained from measurement data, therefore, merely represent a typical case of the space charge effect on the threshold shift.[118]

holes is determined by the capture cross section, which is electric field dependent and fabrication process sensitive[113]. In the microscopic point of view, hole traps are most likely connecting to the $E'$-centres associated with the oxygen vacancy[118, 130], because a strong correlation between between the positive space charge and $E'$-centre concentration has been found using the CV and ESR (Electron Spin Resonance) measurements[125]. The $E'$-centre is a group of lattice defect sites associated with trivalent silicon and oxygen vacancies[116, 118, 130]. Among various types of $E'$-centres listed in [116], the $E'_\gamma$- and $E'_\delta$-centres are the major contributors of the positive space charge [124]. The formation of $E'_\gamma$-centres is given as

$$O_3{\equiv}Si{-}Si{\equiv}O_3 + h^+ \rightarrow O_3{\equiv}Si\cdot\ {}^+Si{\equiv}O_3\ (E'_\gamma)\,, \tag{C.14}$$

where the oxygen vacancy $O_3{\equiv}Si{-}Si{\equiv}O_3$, existing in the thermal oxide prior to irradiation, is the precursor of the $E'_\gamma$-centre [116] [9]. The $E'_\delta$-centre is a result of the hole capturing at a silicon interstitial/oxygen vacancy complex, consisting of 5 neighbouring silicon atoms[116, 131–133]. From the energy point of view, the energy levels of $E'_\gamma$-centres are found to be at least $\sim 3.5\,eV$ higher than the valence band of $SiO_2$, whilst the energy levels of $E'_\delta$ centres are distributed up to $\sim 1.0\,eV$[134]. This indicates that the $E'_\gamma$-centre is a deeper hole trap than the $E'_\delta$-centre, and reveals a more stable space charge. Although the $E'$-centres populate all across the oxide layer, it's found that the region

[9] There exists different models to explain the formation of the positive space charge. For instance, [115] has introduced a model considering only one trivalent silicon with a nonbonding electron interacting with the radiation, as $O_3{\equiv}Si\cdot + rad \rightarrow O_3{\equiv}Si^+ + e^-$.

near[10] the Si-$SiO_2$ interface contains a visibly higher density of $E'$-centres [125]. Due to the higher stability, the space charge results form the deep hole traps in this region is usually identified as the fixed oxide charge[11] (Fig. C.5). The trapped holes undergoes annealing (or neutralisation) process via combining[12] the electrons from either 1) the Si via tunnelling effect, for the traps close to the interface, or 2) thermal excitation inside the $SiO_2$ bulk, for the trap levels close to the $SiO_2$ valence band. This results in the curve part (3) in Fig. C.7. However, this may not bring a complete recovery of the threshold voltage (zero oxide charge condition), as there exist radiation induced space charge which is hard to be neutralised.

**Formation of Interface Traps** The interface traps are mainly linked to the so-called $P_{b0}$- and $P_{b1}$-centres[13] at the Si-$SiO_2$ interface[125, 138, 139]. The $P_{b0}$-centre is found in all types of wafer orientations, whereas the $P_{b1}$-centres exist at the interface of (100) silicon [138]. These defect centres are assigned as trivalent silicon atoms at the interface with a dangling bond pointing towards the oxide part, and contribute to a distribution of energy levels (continuum) in the silicon band gap[139]. Despite the identity and the effects of the interface traps, the mechanism of their formation has been a debatable topic for decades [126, 140]. Nevertheless, a consensus has emerged, that the formation of the interface traps is related to breaking the ≡Si−H bond via irradiation [118, 126]. The most popular model [14] which is probably the dominant process of the trap formation, is a two-stage process originally proposed in [141]:

1. $h^+$ interacts with the hydrogen related defects in $SiO_2$ bulk while hopping, and releases $H^+$ (proton);
2. $H^+$ hops towards the interface in a similar manner as $h^+$, and breaks the ≡Si−H bond.

Evidences have been introduced in [135], showing the validity of this semi-empirical 2-stage model. Nevertheless, the mechanism of the reactions taking place in both stages remain uncertain, various models have been proposed to interpret the measurement results (see footnote 7 and [135]). Simulation studies [140, 142] using the Density Function Theory (DFT) have argued that the exact reaction of stage 2 is most likely a direct reaction between the $H^+$ and $Si_3$≡Si−H, as

$$\equiv Si-H + H^+ \rightarrow \equiv Si^+(P_{b0}^+) + H_2\,, \tag{C.15}$$

[10] As an example, the etch-back experiment by [125] has shown a ∼ 10 nm range of high $E'$-centre concentration in a 1 100 nm thick thermal $SiO_2$.

[11] The location of the fixed oxide charge with high density is found to be as close as possible to the interface (e.g. as border traps illustrated in [135]), as introduced in [136]. Nevertheless, the discussion there is not based on the radiation damage. The fixed oxide charge contributed by the $E'_\gamma$-centre should be outside the border region, according to [124, 137].

[12] Experimental data has been interpreted by modelling two simultaneously happening annealing mechanisms, the compensation effect and the "true" annealing [137]. The compensation effect is a temporary charge compensation of electrons and trapped holes without altering the defect structure, whilst the "true" annealing can reverse the $E'$-centre to its precursor.

[13] Note that the $P_b$ should not be the only contribution to the interface traps, according to quantitative studies of the relationship between the density of defect levels of all interface traps and the density of levels from $P_b$ centres. [138]

[14] There are a number of proposed models listed in [126], including the hydrogen models, one of which is briefly introduced here. The other two categories of the models are: 1) the injection model, featuring a formation of defects through the recombination of $e^-$ from the Si with the $h^+$ trapped at the interface; 2) the stress model, where the $h^+$ from IEL releases the oxygen of the strained Si−O close to the interface, so that the dangling bond is created via the reaction of O at the interface.

leaving a positively charged $P_b^+$ centre and a hydrogen molecule, because it is energetically favoured. This contradicts to the previously widely considered model (various literatures, e.g. [126]), where the ≡Si−H bond reacts with the neutral H atom, which is formed by the $H^+$ capturing an electron (tunnels from the Si) close to the interface prior to the reaction. Although the interface traps initially contributes to positive space charge at the interface in this model, the interface traps can exhibit different charge states, donor, neutral, or acceptor states, as they creates widely distributed energy levels within the Si band gap [139, 143], and are able to rapidly exchange charge carriers with the Si substrate depending on the position of $E_F$ in Si. Under the positive gate bias condition for a p-type Si substrate, the initial interface trap will capture 2 electrons and contributes to a negative interface charge[142]. If the negative charge compensates the positive oxide charge, and even results in a net negative total charge, the curve part (4) in Fig. C.7 will occur (super recovery effect [144]). Unlike the oxide traps, whose neutralisation process can start immediately after the creation, the annealing of interface traps normally requires temperatures above ~ 100 °C.

**Properties of the Border Trap** The border traps on one hand locates inside the oxide layer, but on the other hand can still communicate with the Si substrate (the switching states that are oxide traps), i.e., exchanging charge carriers through tunnelling effect. Such traps communicates with the substrate semiconductor in a broader time scale, which typically slower than the interface traps for Si[145]. Studies introduced in [126] have shown that the border traps are likely consisted of the defects having various structures, including the $E'_\gamma$-centres[120] introduced earlier. The $E'_\gamma$-centres locate in the border region can temporarily combine with an electron, and form a dipole. For instance, after switching the polarity of the electric field, the electron can be released again. Therefore, border traps in MOS devices has been linked with the 1/f noise, whose low frequency component is primarily contributed by the border traps[145].

### C.2.2 Electron Accumulation and Surface Conductivity

As introduced in section 2.5, the MOS structure has different electrical conditions at the Si-$SiO_2$ interface according to the band bending of Si at the interface. Apart from the voltage across the oxide layer, the oxide charge and the charge trapped at the interface modifies the band bending as well. This, subsequently, causes a shift in the flat band voltage and the threshold voltage. In a MOS device, the shift of the flat band voltage $\Delta V_{fb}$ is given by [136]

$$\Delta V_{fb} = -\frac{1}{C_{ox}} \int_0^{d_{ox}} x \rho_{ox}(x) \mathrm{d}x \,, \tag{C.16}$$

with $d_{ox}$ the thickness of the oxide layer, and $\rho_{ox}$ the volume density of the positive space charges in the oxide. Moreover, the $C_{ox}$ represents the capacitance per unit area of the oxide layer, which is given as $C_{ox} = \epsilon_{ox}/d_{ox}$. The oxide charge density $\rho_{ox}$ generally consists of, the mobile ions, the slowly propagating holes, the trapped holes, the fixed oxide charge, and the interface trapped charge. As the defect centres mostly locate close to the interface, and the most stable contribution is from the fixed oxide charge, it is common to model the oxide charge as a charge sheet $Q_{ox}$ at the Si-$SiO_2$ interface. Thus, the shifted flat band voltage can be given as

$$V_{fb}^{new} = V_{fb} + \Delta V_{fb} = V_{fb} - \frac{Q_{ox}}{C_{ox}} \,. \tag{C.17}$$

Taking the MOS device with p-substrate with initially negative $V_{fb}$ as an example, the new flat band voltage will be shifted to the negative direction, requiring a larger gate voltage to reach the flat band condition. The threshold voltage for p-substrate is greater than the flat band voltage ($V_{th} > V_{fb}$, e.g. $V_{th} > 0$ and $V_{fb} < 0$). Therefore, such a shift in the flat band voltage provides a shift of the threshold voltage in the negative direction with the magnitude of $Q_{ox}/C_{ox}$, as well (eq. (2.12)). This indicates that a gate voltage, which equals to the initial threshold voltage, can already cause the electron accumulation, due to the oxide charge. In the ICs consisting of MOSFETs, constant standard gate voltages is utilised for opening and closing the conductive channel between source and drain electrodes (e.g. turning on and off the device). With a shift in the threshold voltage, it is possible that the standard gate voltages will not be able to switch the state of the MOSFET, causing a device malfunctioning.

In modern CMOS technologies, the utilisation of very thin gate oxides (e.g. thinner than 10 nm) has suppressed the effects from the build up of positive oxide charges [113, 118]. However, the omnipresent field oxides (FOX), which separate the active devices/components, are much thicker than the gate oxide (e.g. STI is a type of FOX, and has a typical thickness of approximately 400 nm). Considering the charge neutrality at the Si-$SiO_2$ interface of the FOX, the positive oxide charge can cause the depletion and the electron accumulation at the silicon surface, as illustrated in Fig.C.8. The

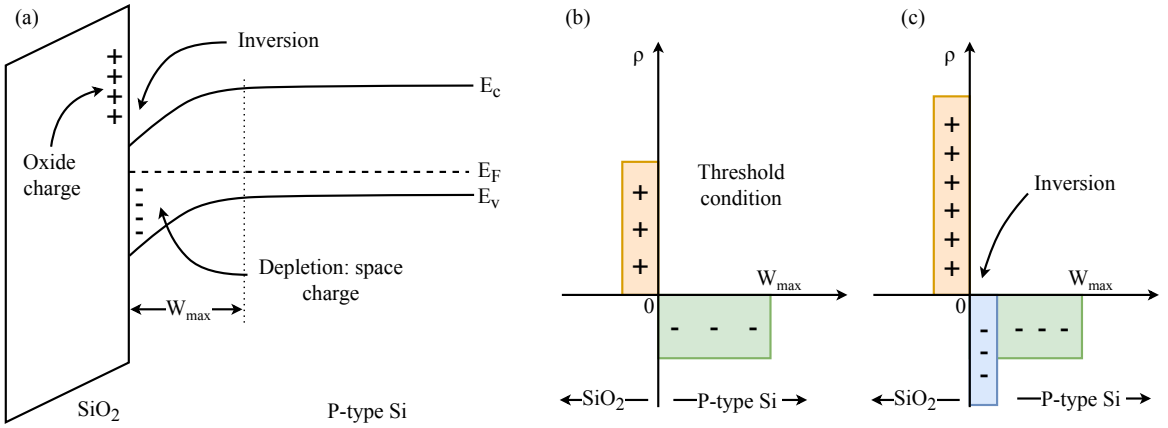



Figure C.8: (a) the band diagram of the Si-$SiO_2$ interface with the presence of positive oxide charges close to the surface. The surface depletion and inversion of a p-type silicon substrate can occur with positive oxide charge. (b) The space charge distribution of the interface at threshold condition. Due to the charge neutrality, the total integral of the charge distribution across the interface equals to zero. (c) The charge distribution for oxide charge with higher density, where the excess oxide charge is compensated by the inversion layer.

threshold condition similar as in the discussion for MOS structures can be achieved when the surface potential reaches the threshold condition, which means that the depletion depth reaches the maximal value. Thus the threshold condition for the oxide charge $Q_{ox}^{th}$ can be calculated as

$$Q_{ox}^{th} = \int_{W_{max}} eN_A dx \overset{(2.13)\ (2.14)}{=\!=\!=} 2\sqrt{\epsilon_{Si} k_B T N_A \ln\left[\frac{N_A}{n_i}\right]}, \tag{C.18}$$

where the right-hand-side represents the integration of the space charge over the depletion region. An inversion layer occurs when the oxide charge density is higher than $Q_{ox}^{th}$ with the inversion charge proportional to the excess oxide charge, as $Q_{inv} = -(Q_{ox} - Q_{ox}^{th})$.

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