Front-End Readout Circuit Design for DEPFET Pixel Detectors in 65-nm CMOS

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***Abstract*—This work presents a differential readout integrated circuit for DEPFET pixel matrices, with a systematic evaluation of trade-offs among key performance metrics such as power consumption, noise, and silicon area. Each readout channel integrates a cascode transimpedance amplifier followed by a compact single-ended-to-differential conversion stage, optimized to fully drive the input range of a high-speed, low-power analog-to-digital converter (ADC). The proposed readout architecture is designed in an advanced 65-nm CMOS technology and is designed to interface seamlessly with such ADCs, enabling a system that meets stringent constraints on power density and pixel pitch while delivering the precision required for future high-rate, high-resolution experiments. The circuit targets DEPFET matrices operated in rolling-shutter mode, supporting a minimum input current of 2 μA and a signal range of interest extending up to 8 μA (4 MIPs about 20,000 electrons). The readout operates with a total power consumption of 900 μW per channel and an input-referred noise of 80 nA, corresponding to approximately 200 electrons. The achieved noise performance ensures a comfortable signal-to-noise margin across the full dynamic range.**

***Index Terms*—readout, DEPFET, transimpedance amplifier, single-ended to differential conversion, front end**

I. Introduction

The continued evolution of particle-physics experiments places increasing demands on the performance, efficiency, and integration density of readout electronics [1]. As detector systems grow in channel count and data rates increase, high-quality, low-noise readout chains become essential to preserve the precision of the exploited sensor technology.

DEPFET (Depleted P-channel Field Effect Transistor) pixel sensors play an important role in this context [2]. Although the technology was first proposed in the late 1980s, DEPFETs remain highly relevant due to their combination of in-pixel amplification, full depletion, and intrinsically low noise [3]. This allows for excellent signal-to-noise ratios while preserving an exceptionally low material budget. Ongoing research and development has enabled the successful deployment of DEPFET-based sensors in a wide range of demanding applications, delivering high frame rates (WFI at NewAthena), accurate position resolution (PXD at Belle II), Fano-limited energy resolution (MIXS at BepiColombo), or maximized dynamic range for TEMs (EDET) [4]. These examples show the versatility of DEPFET technology through application-specific optimization of both pixel design and readout architecture.

In DEPFET pixel matrices, a rolling shutter readout scheme is commonly used, where rows of pixels are activated and read out sequentially rather than simultaneously [5]. This allows the readout electronics to handle one or a few rows at a time, reducing the instantaneous data bandwidth and power requirements. Each pixel's drain current, which is proportional to the collected charge, is first fed into a transimpedance amplifier (TIA) in the front-end. While this configuration is promising, it is accompanied by a significant increase in drain-line input capacitance, estimated at approximately 50–100 pF. The TIA converts the small current signal into a voltage while providing sufficient gain, ensuring that weak signals can be measured accurately despite noise or common-mode disturbances. The amplified voltage is then digitized by an analog-to-digital converter (ADC), which converts the continuous analog signal into a digital code suitable for further processing (Fig. 1). In modern readout systems, the ADC can be implemented using several architectures (i.e., cyclic, successive approximation, or pipeline schemes) [6]–[8]. Additionally, since the output voltage of the transimpedance amplifiers is susceptible to common-mode disturbances such as power supply fluctuations, temperature variations, and radiation-induced offsets [9]–[11], a differential input ADC can effectively reject these common-mode effects, reducing noise and improving overall performance [12]–[14]. Moreover, differential architectures suppress substrate coupling and mitigate errors from charge injection by the system's switches. Since the TIA output is typically single-ended, a single-ended to differential conversion is necessary to drive the ADC inputs effectively and utilize the full input range. In this context, a single-ended to differential (SDC) circuit can achieve high differential accuracy and minimal output common-mode voltage drift, ensuring that the ADC receives a well-balanced signal [15], [16].

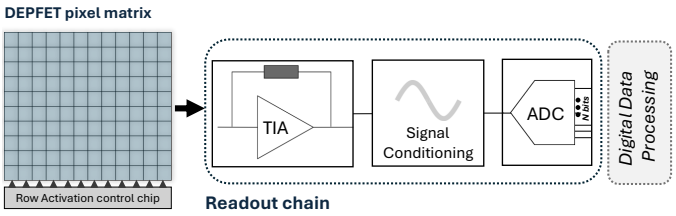

Fig. 1. Block diagram of a analog front-end readout chain.

This work presents a low-power, low-noise, readout for DEPFET matrices, implemented in a state-of-the-art 65-nm CMOS process. Scaling to a smaller feature size improves power and area efficiency while maintaining low noise perfor-

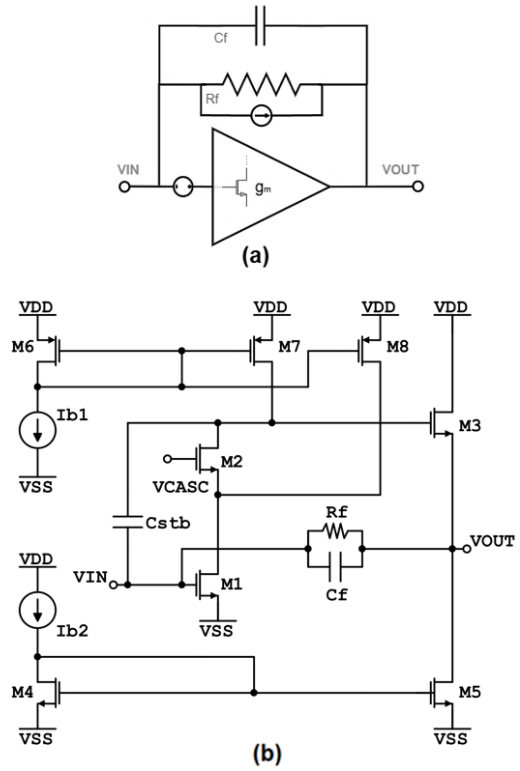

Fig. 2. Transimpedance amplifier: (a) shunt implementation concept (b) cascode topology.

mance. Each channel integrates a cascode TIA and a compact single-ended-to-differential (SDC) stage, optimized to fully drive the input range of a high-speed, low-power ADC. The paper provides an extensive analysis of these building blocks, addressing the challenges and exploring trends in critical performance metrics.

II. Front-End Building Blocks: Design Considerations

To design a high-performance analog front-end, the transimpedance amplifier and the single-ended-to-differential stage must be carefully designed. Optimizing the performance and co-integration of these building blocks is essential to achieve a robust and efficient front-end design.

A. TIA design

The front-end TIA is the most critical component of the channel affecting both the noise-sensitivity and the speed of the overall system. In this case, the chosen topology must balance transimpedance gain, input-referred noise, bandwidth and power consumption, which are interdependent and require careful trade-offs to optimize overall performance [17].

The transimpedance amplifier receives the DEPFET drain current $I_{\rm in}$ and converts it into an output voltage $V_{\rm out}$. The feedback loop holds the input node at a constant potential, resulting in a linear current-to-voltage relationship given by,

$$V_{\rm out} = -I_{\rm in} \cdot R_f \tag{1}$$

The block level of the shunt-feedback TIA under discussion is shown in Fig. 2(a). The detector capacitance C_d and the input capacitance of the voltage amplifier $C_{\rm amp}$ will appear in parallel and can be combined into a single equivalent capacitance $C_{\rm in}$. The voltage amplifier is modeled with a single-pole transfer function

$$A(s) = \frac{A_0}{1 + s/\omega_p}, \tag{2}$$

where A_0 is the DC gain and ω_p is the dominant pole frequency. The amplifier is assumed to have infinite input resistance and zero output resistance. Based on analysis provided in [18], the achievable transimpedance gain is fundamentally constrained by the classical transimpedance limit, which arises from the trade-off between feedback resistance, total input capacitance, and required bandwidth,

$$R_{tot} \leq \frac{A_0 f_A}{2\pi(C_{in} + C_f) \cdot BW^2} \tag{3}$$

where the effective transimpedance is given by $R_{tot} = \frac{A_0}{A_0+1} \cdot R_f$. The amplifier's gain-bandwidth product $A_0 f_A$ is approximately equal to the transit frequency f_T of the technology process.

For this application, the TIA implementation is based on a cascode TIA with resistive–capacitive (RC) shunt feedback and an NMOS input transistor. An additional current branch is connected directly to the input transistor to provide the required bias current without degradation of the cascode output impedance (Fig. 2(b)). Considering power consumption, an important design parameter is the bias current of the input device (M1), which is typically operated close to moderate inversion. This current contributes significantly to the overall power consumption of the chip and must therefore be evaluated together with the noise performance. The M1 NMOS gate length is chosen to minimize the excess noise factor, which increases in short-channel devices. Beyond the optimal length, further increases do not reduce noise and instead increase the gate area, degrading overall noise performance.

B. SDC design

An active single-ended-to-differential converter is an effective solution for driving differential ADCs and fully exploiting their input range in DEPFET readout systems. Passive SDC approaches often require large capacitances, which are incompatible with the strict pixel pitch constraints of modern arrays. Furthermore, resistive-based differential drivers require higher power consumption and also add extra noise to the chain.

For this application, a switched capacitor SDC is designed, as depicted in Fig 3(a). A folded-cascode (FC) operational amplifier is employed as the core of the SDC (Fig 3(b)) to provide a larger output swing - compared to the telescopic configuration - high gain, and strong noise immunity. A dynamic switched capacitor common-mode feedback (CMFB) circuit is used to continuously adjust the output common-mode level of the fully differential amplifier, ensuring stable operation (Fig 3(c)). The FC amplifier core is designed for

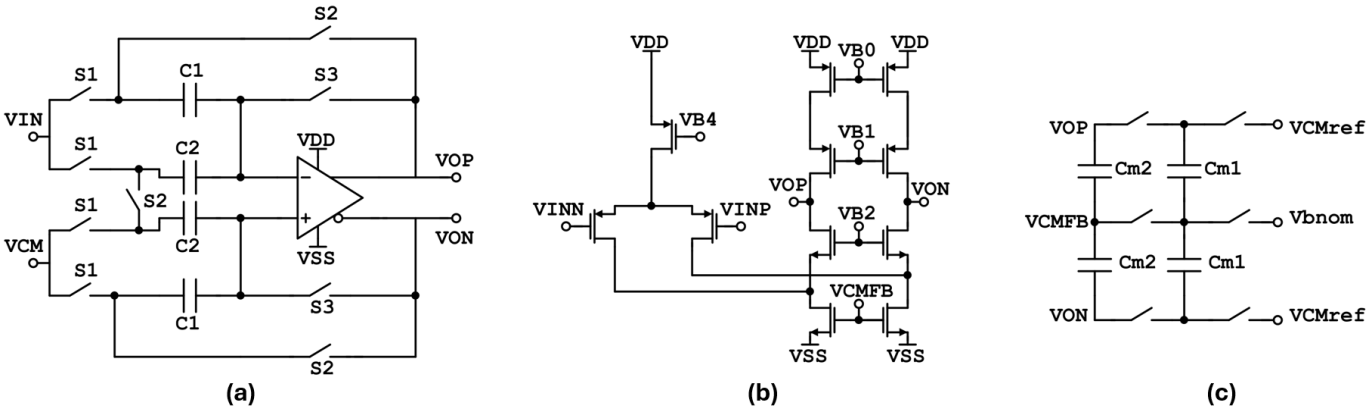

Fig. 3. Switched-capacitor single-ended-to-differential converter: (a) top level (b) folded cascode differential amplifier (c) CMFB topology.

low-power operation while maintaining sufficient bandwidth (over 10 MHz), according to,

$$f_{t(\text{Folded})} = \frac{g_{m_{in}}}{2\pi c_L} \tag{4}$$

where C_L is the output capacitance that the op-amp must drive. This capacitance is set to be 1 pF per output and corresponds to the load of a SAR ADC.

The size of the unit capacitor for C1 and C2, C_{fm}, has a direct impact on the noise of the circuit. The thermal noise introduced by the capacitor is approximately given by $v^2_{\text{n,rms}} \approx kT/C$, indicating that larger capacitances reduce noise but increase area and limit the maximum switching frequency f_s. The settling behavior is determined by the RC time constant $\tau = R_{\text{on}}C$, where R_{on} is the on-resistance of the switches; accurate charge transfer requires $\tau \ll 1/f_s$. The effective output current of the SDC is set by the charge transferred per clock cycle, approximately $I_{\text{out}} \approx Cf_s\Delta V$, where ΔV is the voltage swing across the capacitor. Larger capacitance or voltage swing increases the required current to achieve full settling within a clock period, while higher switching frequency allows smaller capacitances or voltage swings for the same effective current, at the cost of slightly increased thermal noise.

III. Front-End Performance Trends

The front end readout circuit is designed and simulated in a 65 nm CMOS process and is implemented for operation with a 10 MHz rolling-shutter DEPFET matrix as illustrated in Fig. 1. The input capacitance is estimated at 100 pF, emulating the worse case scenario.

A. TIA performance

The TIA is designed based on the analysis presented in Section II. The input transistor is sized at 500 μm / 0.2 μm. The input current ranges from a minimum of 2 μA (MIP = 5,000 e) to a maximum of 8 μA (4MIP = 20,000 e) and is emulated using a piecewise-linear (PWL) current source that provides a step-function. The feedback network consists of a 14.5 kOhm resistor and a 210 fF capacitor. The additional bias current (I_{casc}), provided by M8 transistor, dissipates 220 μA. Figure 4 shows the transient output voltage of the TIA as well as its frequency response under the aforementioned conditions. The transimpedance gain is 14.43 kOhms, with a cutoff frequency of 22 MHz. With this configuration, the input-referred noise is calculated at 80 nA. For a minimum expected input of 2 μA, the resulting signal-to-noise ratio (SNR) is 25. The total power consumption of the TIA block is 480 μW.

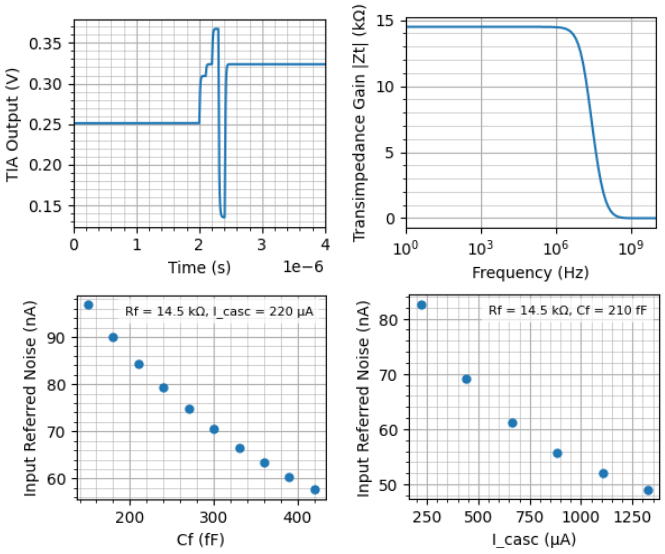

Fig. 4. Transimpedance amplifier performance analysis.

The TIA's bandwitdh can be extended at the cost of increased noise. Alternatively, to keep noise low, additional power can be used. Figure 4 shows the noise trade-off as a function of feedback capacitance and cascode current consumption. Increasing the feedback capacitance reduces noise, and higher power consumption also lowers noise. However, since hundreds or thousands of channels must be integrated, keeping both silicon area and power consumption low is critical. Therefore, a careful trade-off must always be made.

B. SDC performance

Based on the analysis presented above, the SDC shown in Fig.3(a) is implemented with a switching frequency of 10 MHz and a capacitor ratio of $C_2/C_1 = 8$, performing single-ended to differential conversion and amplification simultaneously.

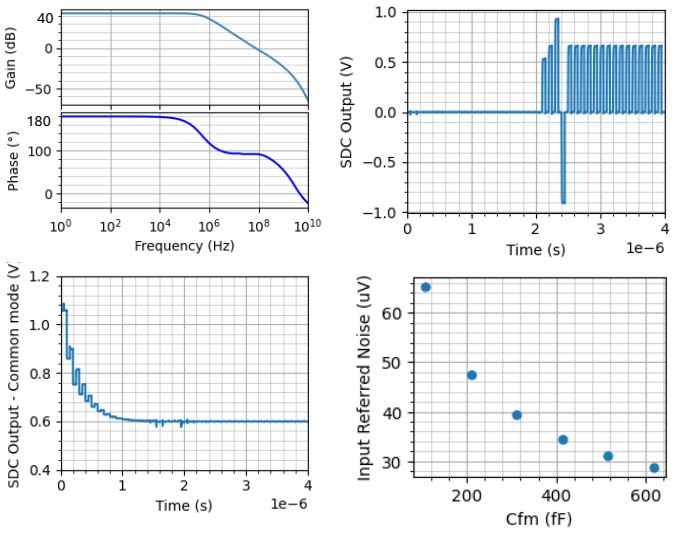

Fig. 5. Performance analyses of single-ended-to-differential converter.

This allows full exploitation of the 1.2 V input range, which is also expected to match the input range of an ADC implemented in this process node. The CMFB is designed with a reference voltage that ties the output of the folded-cascode amplifier to 600 mV ($V_{\mathrm{DD}}/2$). The switches are implemented with transmission gate switches. In Fig.5(a), the gain and phase of the SDC core amplifier are extracted using periodic-state stability (PSTB) analysis. As presented, there is sufficient phase margin to allow amplification within the SDC loop. The differential mode and common-mode voltages are also shown, indicating that the common mode remains at 600 mV (after initialization), while the differential output provides the amplified signal with an actual achieved ratio of 7.8. The total power consumption of the SDC is 420 μW. The input-referred noise is critically dependent on the size of the unit capacitor, a larger capacitance reduces noise but significantly increases the total silicon area.

Fig. 5(d) shows the relationship between capacitance and input noise. The input-referred noise of the SDC must remain lower than the output noise of the TIA, which is already achieved with the chosen capacitance.

IV. Conclusions

A differential readout integrated circuit for DEPFET pixel matrices is presented, along with trends of critical performance metrics. The design, implemented in 65-nm CMOS, supports a minimum input current of 2 μA and achieves an input-referred noise of 80 nA (approximately 200 electrons). Each channel consumes less than 1 mW, while capacitor usage, and therefore silicon area, is minimized, maintaining sufficient SNR even with a large input capacitance of 100 pF and an operating frequency of 10 MHz. Future work will include evaluation of the complete readout chain, including the ADC interface and further analyses of the front end design.

V. Acknowledgements

This project has received funding from the European Union's Horizon 2024 Research and Innovation programme under the Marie-Sklodowska-Curie grant agreement No. 101209036 (NexGenRE).

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