# The Pixel-TPC: A feasibility study

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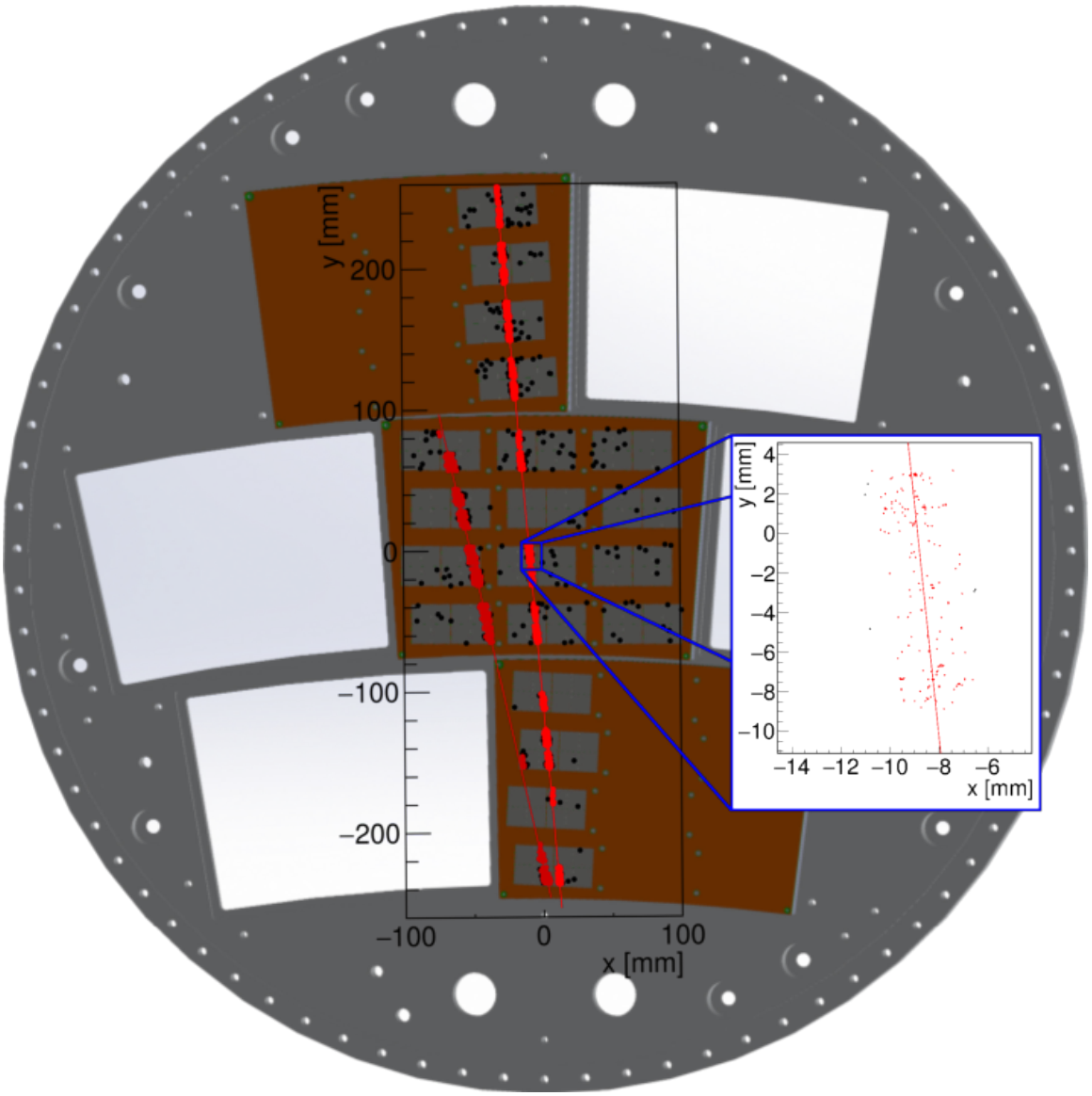

# The Pixel-TPC: A feasibility study

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## Summary

The Time Projection Chamber (TPC) as a detector system in particle physics offers continuous tracking with low material budget and therefore is considered in the design of the International Large Detector (ILD) at the planned International Linear Collider. Different readout concepts are currently studied, of which one is the Pixel-TPC. It combines micro-pattern gaseous detectors with pixelised readout. A Micromegas is post-processed on the Timepix chip to form a so called InGrid. However the chips only have a small size such that several have to be placed next to each other to read out a TPC.
The construction and operation of a Pixel-TPC with 160 InGrids was carried out in this dissertation as a feasibility study. Therefore, a new readout system was designed based on the Scalable Readout System from the RD51 collaboration at CERN. The firmware has been developed together with a data acquisition software and electronic boards. A final test beam campaign has been performed at the Large Prototype of the LCTPC Collaboration at DESY in 2015, in which the complete system was successfully tested. In a preliminary analysis of parts of the collected data, detector properties are demonstrated and evaluated to provide starting points for further developments in view of a design for an ILD Pixel-TPC.

## Zusammenfassung

Die Zeitprojektionskammer (TPC) als Detektorsystem in der Teilchenphysik ermöglicht eine ununterbrochene Spurbeobachtung bei geringem Materialbuget und wird daher für das Design des International Large Detectors (ILD) am geplanten International Linear Collider in Betracht gezogen. Derzeit werden verschiedene Auslesekonzepte untersucht, wovon eines die Pixel-TPC ist. Es kombiniert mikrostrukturierte gasgefüllte Detektoren mit einer pixelierten Auslese. Ein Micromegas wird auf einen Timepix Chip post-prozessiert um ein sogenanntes InGrid zu bilden. Diese Chips haben lediglich eine kleine Fläche, weshalb mehrere nebeneinander platziert werden müssen, um eine TPC auslesen zu können.
Als eine Machbarkeitsstudie wurde in dieser Dissertation eine Pixel-TPC mit 160 InGrids gebaut und betrieben. Dafür wurde ein neues Auslesesystem basierend auf dem Scalable Readout System der RD51-Kollaboration am CERN entworfen. Die Firmware wurde zusammen mit einer Datennahmesoftware und elektronischen Platinen entwickelt. Eine finalen Strahlzeitkampagne wurde am Large Prototype der LCTPC-Kollaboration am DESY im Jahr 2015 mit dem vollständigen System erfolgreich durchgeführt. In einer vorläufigen Analyse eines Teils der gesammelten Daten werden Detektoreigenschaften demonstriert und ausgewertet, um Anhaltspunkte für die weitere Entwicklung im Hinblick auf den Entwurf einer ILD Pixel-TPC zu liefern.

# Contents

CHAPTER 1

# Introduction

High energy particle physics requires new technology to increase the precision of measurements in order to expand our knowledge. As a feasibility study, the goal of this thesis was to construct and operate a new type of detector that was devised more than ten years ago: the Pixel-TPC. A main challenge for the final realisation was the development of the electronics to read out this device, which has never been built so far. Hence, a large part of the thesis deals with the design of the readout system. In total however, the scope extends to the design of the whole detector. This large task, herein often called the *project*, was supported by several diploma, master and bachelor theses and embedded in an international collaboration. The relevant contributions are referenced.

The second chapter briefly introduces particle physics with a focus on the measuring equipment used in this field of research. Gaseous detectors are explained in greater detail, as also the Pixel-TPC is of that type of measuring equipment. Also the physics processes to understand the principles of operation are outlined.

A third chapter summarises the technology necessary for the construction of the Pixel-TPC and especially the readout system. The knowledge is important to understand the choices in detector and readout design explained in later chapters. The originality of the Pixel-TPC and its unique features are expressed.

In Chapter 4 and 5, the technological developments for the realisation of the project are outlined. These are the firmware for the readout system, the electronic boards and the computer software to operate the detector.

The verification of the functionality of the readout, also in comparison to similar designs, is shown in Chapter 6.

The final proof of the developments has been done in an environment similar to where they would be applied in particle physics experiments. Therefore, two test beam campaigns have been carried out. An intermediate stage test is explained in Chapter 7 together with an analysis of the detector performance. The final test beam with the complete system is explained in Chapter 8. Also for this campaign, first preliminary analysis results are shown.

A discussion of the results and the capabilities of the Pixel-TPC conclude the thesis. The next steps necessary for a complete data analysis are indicated. Further developments necessary for an application in particle physics are pointed out.

CHAPTER 2

# Particle physics and detectors

The science of particles physics aims to explain our universe by breaking it down to a set of fundamental particles and forces between them. This approach has shown to be very successful and a mathematical theory, called the Standard Model of particle physics, has been found to describe the matter which surrounds us. The development of this model took many decades and was an intense interplay between theory and experiments. On the one hand, theoretical physicists constructed different mathematical descriptions to explain experimental results. The theories also predict what has not been observed so far. On the other hand, the experimentalists confirmed or excluded such theories by observations, but from time to time also offered surprising and unexpected results, which then demanded extensions of the present theory. Section 2.1 gives a general introduction into the basics of the Standard Model by omitting the mathematical details.

In order to explore the content of our universe, particle physicists have to look deeply inside matter. The length scale at which fundamental particles can be found is below the size of an atom. Moreover, most of the particles are unstable and nowadays only rarely produced in nature. This is because the energy density in the universe has constantly decreased since the Big Bang and hence, it became more and more unlikely that enough energy is accumulated to create particles from the vacuum. Additionally, the binding energy inside nucleons holds elementary particles together, such that they are no longer observed as free particles.

In order to provoke the creation of such particles for a short time, tools have been developed to increase the energy density in a tiny spot. Stable particles are accelerated to almost the speed of light and hence gain energy. Then they collide with other particles and in this concentration of energy, different particles, even heavier than the original ones, can be produced following the famous formula of Einstein: $E = mc^2$. The machines necessary to produce such high energy densities have increased with the evolution of the theory. With the time, heavier and heavier particles were found and the technology to achieve their production was always at the edge of what humankind could provide.

The currently most advanced and largest tool, the Large Hadron Collider (LHC), is briefly explained in Section 2.2, followed by a section of the planned next generation tool, the International Linear Collider (ILC) in Section 2.3.

Developments of tools for particle physics had to and still do extend the standard of technology. This does not only hold for the accelerators, but also for the instruments, which are used to measure the properties of the particles produced. As those particles only exist for a very short time after the collision, they cannot be observed directly. They almost instantaneously decay into other particles by respecting

the rules of physics, as for example energy and momentum conservation. So by accurately measuring the properties of the decay particles, the properties of the originally produced particles can be reconstructed. The instruments used in particles physics are called detectors. Not all properties of the decay particles can be measured by a single detector system. Hence, there are different subdetectors specialised to measure only certain properties, which then can be combined in an experiment. An example for a complete particle physics detector is given in the ILC section, with particular emphasis on a special type of subdetector, the Time Projection Chamber (TPC). The technology used in this instrument are gaseous detectors, which are explained in Section 2.4 in more detail, as the aim of this thesis was the advancement of exactly that technology. An overview of the basic principle, physics processes exploited for the detection (Section 2.4.1) and current status of technology (Section 2.4.3) is given with a focus on the starting points for the further development performed during the project described in this thesis.

## 2.1 The Standard Model

All elementary particles discovered and their interactions are summed up in the Standard Model [1–4]. This quantum field theory describes the particles as discrete quantum fields and their interaction as gauge symmetry. In a less mathematical way, the particles can be grouped by one of their quantum number, the spin, into fermions and bosons.

The fermions with spin ½, also referred to as the matter particles, can be further sub-divided into six quarks and six leptons. Quarks carry one or two third of electric elementary charge, while leptons carry electric charge one or zero. Always two leptons and two quarks form a generation of particles. The two quarks of the first generation, one with electric charge $2/3$ and the other with $-1/3$, are called up and down quark. The leptons of this generation are the electron and the electron neutrino. The stable matter which surrounds us can be described by the particles of the first generation and its interactions only. The second and third generation particles are exact copies of the first generation particles. Apart from the neutrinos, where the mass hierarchy is not known yet, the higher generation particles just have a higher mass. They are unstable and decay into particles of the lower generation.

The bosons with spin 1 are the four force carrier particles: the photon, gluon, Z boson and W boson. There is a fifth boson with spin 0 (the only scalar particle), the Higgs boson, which has just been discovered by the LHC [5, 6]. This particle is special in a sense that it is the representative of a field, which interacts with other particles to give them what we call mass. The representation of the fundamental particles, including some of the quantum numbers, is shown in Figure 2.1.

Antimatter, which is also included in the Standard Model, is another copy of the particles mentioned above and depicted in Figure 2.1, just with the inverse charge quantum number.

Despite the fact that the Standard Model is a successful and very precise theory, it is not complete. It is still not able to describe the universe in total, as the gravitational force cannot be included yet. Astrophysical experiments have shown that only about 5 % of the content of the universe consists of matter described by the Standard Model, while about 26 % is so called Dark Matter and 69 % is made of Dark Energy [8]. Moreover, it is still unclear why after the Big Bang more matter was left over than antimatter [9]. Another observation not explained by the Standard Model so far is the neutrino oscillation and the non zero mass of these particles. Thus, the Standard Model can only be part of a more general theory, which still has to be found. Theoreticians already have many possible extensions on-hand, so it is again the duty of experiments to exclude some of them or to find evidence for new physics beyond the Standard Model. A more comprehensive overview of the Standard Model can be found in [9] or [10].

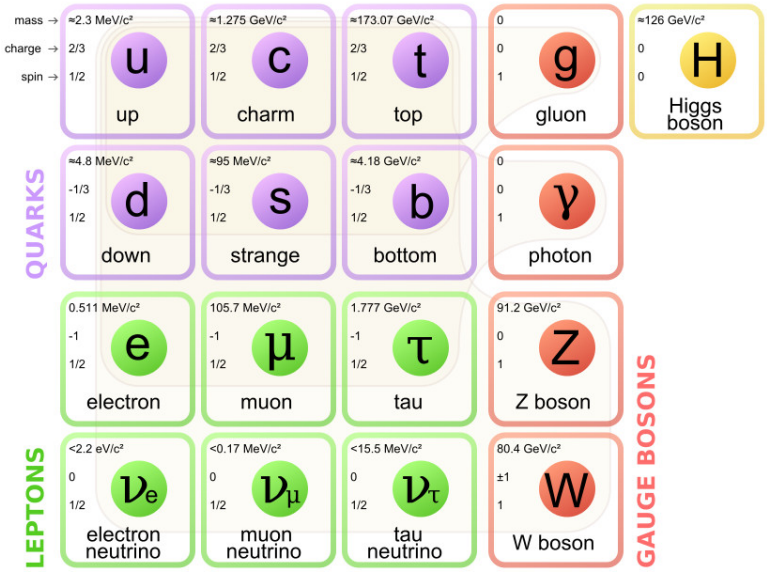



Figure 2.1: Fundamental particles of the Standard Model, from [7].

## 2.2 The Large Hadron Collider

As mentioned before, the concentration of energy in a small space point is necessary to produce unstable particles. One way to explore the unknown is to increase the amount of energy of the colliding particles and at some point pass the threshold to transform the collision energy into the mass of a particle not discovered so far. The conservation of quantum numbers for some particles requires the production of several particles and the production probability becomes a function of the energy and the colliding particles, the cross section $\sigma$. Apart from the cross section, the number of produced particles per time depends on the luminosity of the accelerator. It is defined as

$$\mathcal{L} = \frac{n \cdot N_1 \cdot N_2 \cdot f}{A} \tag{2.1}$$

with $n$ being the number of bunches in the particle beam, $N_1$ and $N_2$ being the particles in the colliding bunches, $f$ being the revolution frequency of the collider and $A$ being the effective beam cross section. The unit of $\mathcal{L}$ is $\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

The currently most powerful experiment in particle physics concerning energy and luminosity is the LHC [11] at the European Organization For Nuclear Research (CERN) in Geneva, Switzerland. In the tunnel of the former Large Electron-Positron Collider (LEP) with a circumference of about 27 km, the proton-proton collider accelerates particles in each beam to currently 6.5 TeV in the run period since April 2015. At four points in the tunnel, particle bunches in each beam are brought to collision every 25 ns. The design luminosity is $1 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. Despite the fact that bunches are packed with about $10^{11}$ protons, only a few particles interact in a way, such that a hard collision occurs (inelastic scattering). Because of the fact that protons are not elementary particles but consist of quarks and gluons, only the fraction of energy carried by the involved particle is available for the production of new particles. Each of the four interaction points is equipped with a particle physics detector. There are the two multi-purpose detectors A Toroidal LHC Apparatus (ATLAS) [12] and Compact Muon Solenoid (CMS) [13], the Large Hadron Collider Beauty (LHCb) [14] experiment specialised in the investigation of hadron

decays including b and c quarks and A Large Ion Collider Experiment (ALICE) [15], designed for the study of quark gluon plasma.
Already in the year 1994, CERN Council announced that the LHC would be built. At the end of 2009, the first data run was started. The beam energy and luminosity were constantly increased for the following run periods until in February 2013, the accelerators and experiments stopped for maintenance and improvements. From the first moment on, physicists from all over the world started to analyse data with the help of a computing grid. Many results have been published of which certainly the rapid confirmation of the Standard Model with a so far unattained precision and the discovery of a new particle [5, 6] are the most relevant ones. This new particle is certainly a Higgs boson, as until now it shows all properties expected by the Standard Model. Such a particle was already proposed in 1964 by theoreticians [16–19], of which Peter Higgs and François Englert were awarded with the Nobel Prize in Physics in 2013 [20].
Because of its energy, the LHC is often called a "Discovery Machine" and the potential to detect new particles or deviations from the Standard Model has increased with the start of the new run with a higher beam energy.

## 2.3 The International Linear Collider

The Standard Model is able to make predictions even up to energies, which can currently not be reached with human-built accelerators. In order to achieve this, the accessible parameters of the theory have to be measured with high precision. This approach is called the "Precision Frontier" in contrast to the "Energy Frontier", where the accelerator energy is increased in order to directly discover effects occurring at higher energies. The LHC has some limitations on the precision side, as the initial state of the colliding proton fragments is unknown. This has for example direct impacts on the total Higgs decay width measurement [21].
For that reason, lepton colliders have been built in the past to explore physics by the precision approach, despite their center of mass energy was lower than the one of previous hadron colliders. In order to accelerate a particle, it needs to be charged. The only stable lepton is the electron. The last lepton-lepton collider at the energy limit was the electron-positron collider LEP at CERN with a center of mass energy of 209 GeV at the end of its operation. It was a circular storage ring collider. Among others this type of colliders have the advantage that particles in a bunch return to the collision points after a revolution if they did not interact. A drawback of such type of colliders is that the particle beams have to be bent by magnetic fields in order to follow the circular path, which causes the emission of synchrotron radiation. The energy loss $\Delta E$ of a particle with mass $m_0$ and energy $E$ per revolution on a circle with radius $r$ is given by

$$\Delta E \propto \frac{E^4}{m_0^4 \cdot r}. \tag{2.2}$$

The ratio of energy loss between electrons and protons for the same energy is $10^{13}$! As an example, for LEP at 100 GeV per beam, the energy loss per revolution per particles was about 2 GeV with a total radiation power of about 18 MW for the beam [22]. For comparison, at the LHC with a design energy of 7 TeV per beam, the energy loss per particle is 10 keV per revolution and the total radiation power of the beam is about 6 kW [23]. There are three possibilities to continue research at the "Precision Frontier" with collider physics:

- Use leptons with a higher mass, e.g. muons, which is studied in the Muon Accelerator Project [24], but on the technological side not advanced well enough to be built yet.

- Increase the radius of the storage ring, which is not possible in the current tunnel of LEP at CERN and hence would require the construction of a new tunnel.
- Build a linear collider, which does not store the beam in a ring, but only uses each particle for a single shot.

According to the state of technology, only the last two options can be realised in the near future. Concerning the construction costs, a linear collider is preferred for center of mass energies higher than about 300 GeV. Still, there are projects at different stages of new circular electron-positron colliders at CERN [25] and in China [26].
On the side of the linear colliders, there are two projects combined in the Linear Collider Collaboration. One is the Compact Linear Collider (CLIC) [27] project, which aims to study the construction of a 3 TeV linear collider with a concept of a low-energy, high-intensity drive beam, which transfers its energy to the main beam to achieve an accelerating gradient of 100 MV/m.
The other one is the ILC [28], which uses superconducting radio frequency cavities with an accelerating gradient of 31.5 MV/m. This technology is well established and already used at the European X-Ray Free-Electron Laser (XFEL) [29]. The accelerator could be built in stages to achieve a center of mass energy $\sqrt{s}$ of 250 GeV, 500 GeV and 1 TeV. More details on the ILC accelerator can be found in [30].

### 2.3.1 ILC physics

The physics program at the linear colliders is in many aspects complementary to the one at the LHC and an interplay of both can significantly extend the current knowledge in the field [31]. Especially the recently discovered Higgs boson opens up a new era of high precision physics as it can be used at the ILC to probe the Standard Model and in particular the mechanism of Electroweak Symmetry Breaking (EWSB). This section will introduce only two examples of physics at the ILC following the argumentation in [32]. For more details and the achievable resolutions, the reader is referred to [33].
As an electron-positron accelerator collides elementary particles, the collision energy can be precisely tuned and the initial state is well defined. Still for some measurements, the resolution is limited by the beam-energy spread. In addition, there is no background due to a fragmentation of the colliding particles. For the ILC, the most important background source are photon-photon collisions from the colliding beams. Therefore, the relevant physics processes happen in a more clean environment and the radiation dose, to which the detectors have to withstand, is significantly smaller than at the LHC. The beam structure of a pulsed beam allows for a complete readout of the detector between bunch trains. The polarised beams can be used to suppress processes, which can have the same final state as the interesting ones.

#### Higgs physics

In a first stage of $\sqrt{s} = 250$ GeV and below, the physics program includes high precision measurements of the W boson mass and the use of the ILC as a Z boson factory. At about $\sqrt{s} = 250$ GeV, the Higgs boson production through Higgsstrahlung (see Figure 2.4) reaches its maximum.
Figure 2.2 shows the Feynman diagram of the process. It describes the annihilation of an electron and a positron from which a Z boson is formed. The Z boson then radiates off a Higgs boson (H). In short, the process is described by $e^+e^- \to Z \to ZH$. From this process, properties of the Higgs boson, especially a model independent determination of the branching ratios and a precise measurement of the Higgs mass can be performed. Due to the clearly defined initial state, this can be done by measuring the decay products of the Z boson only and thus reconstruct the "recoil" mass. The Higgs mass $M_H$ is then given

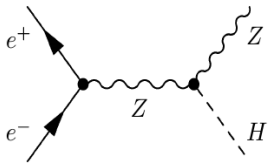



Figure 2.2: Feynman diagram of Higgs production through Higgsstrahlung.

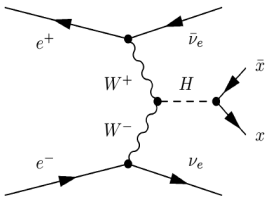



Figure 2.3: Feynman diagram of Higgs production through WW fusion.

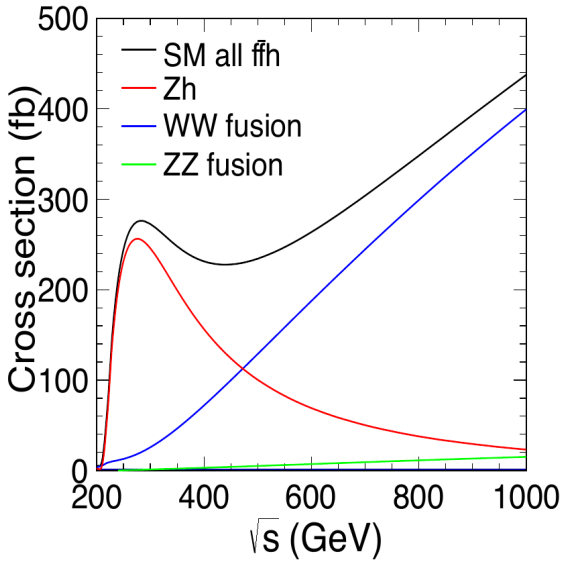



Figure 2.4: Higgs production cross section in dependence of the center of mass energy, from [34].

by $M_H^2 = s + M_Z^2 - 2E_Z\sqrt{s}$, where $s$ is the initial state center of mass energy, $M_Z$ is the Z boson mass and $E_Z$ is the energy of the Z boson [35]. $E_Z$ has to be reconstructed from the decay products of the Z boson, for example in the processes $Z \to e^+e^-$ or $Z \to \mu^+\mu^-$. Figure 2.5 shows a simulation of the reconstructed recoil mass spectrum.

At about $\sqrt{s} = 350\,\text{GeV}$, the Higgs production through WW fusion ($e^+e^- \to \nu_e\bar{\nu}_e H$, Feynman diagram in Figure 2.3) becomes dominant, see Figure 2.4. With this process, the absolute Higgs couplings and model independent total Higgs width can be measured. For example, the Higgs coupling to the W boson $g_{WWH}$ can be obtained when $g_{ZZH}$ has been measured in Higgsstrahlung before from the relationship

$$\frac{\sigma(e^+e^- \to ZH) \times BR(H \to b\bar{b})}{\sigma(e^+e^- \to \nu_e\bar{\nu}_e H) \times BR(H \to b\bar{b})} \propto \left(\frac{g_{HZZ}}{g_{HWW}}\right)^2, \tag{2.3}$$

where $\sigma$ denotes the production cross section and $BR$ the branching ratio of the process in brackets. Instead of the decay to $b$ quarks, other decays can be compared as well. However, the highest precision can be obtained with the $b$ quark.

From a center of mass energy of 500 GeV on, the trilinear Higgs self-coupling can be accessed. An observation at a level of $5\sigma$ significance is at the edge of what can be done with the ILC, see [34] and [33] for more details.

### Top physics

The scan of beam energies can be used to measure particle masses by a threshold scan. One example is the top pair production ($e^+e^- \to t\bar{t}$) at the threshold energy $\sqrt{s} = 2m_t$ to determine the top mass $m_t$ and the total width $\Gamma_t$. Therefore, the effective cross section for top pair production is measured for different center of mass energies to compare the data to the theoretical calculations which can be seen in Figure 2.6.

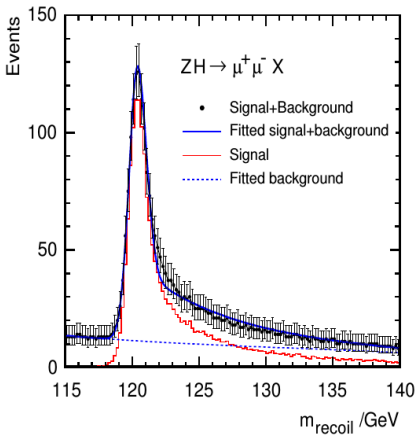



Figure 2.5: Simulated result of the Higgs recoil mass measurement in the $\mu^+\mu^-$ final state, from [34].

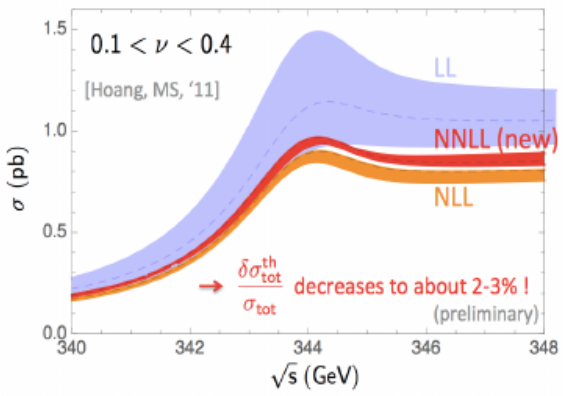



Figure 2.6: Accuracy of the prediction of the top pair production cross section at the threshold as achieved with different calculations, from [33].

### Detector benchmarks

The physics program of the ILC also defines the detector design. Some specific processes were selected as benchmarks for the detectors (benchmark processes, see [36]). One example is the measurement of the Higgs coupling to the W boson $g_{WWH}$, for which the final state with $b$ quarks gives the highest precision. Therefore, the detector has to have a sufficient capability to recognise those particles (b-tagging). Constrains for the vertex detector can be derived from the event topology.
Another example is the recoil mass measurement, from which the required momentum resolution of the tracking system was derived. As has been shown before, the reconstructed Higgs mass is determined by the energy of the Z boson $E_Z$, which itself is derived from the decay particles, for example in the $\mu^+\mu^-$ final state. The simulated result for the mass measurement is shown in Figure 2.5. For the real experiment, the precision depends on how precisely the muon momentum can be measured. Figure 2.7 shows the simulated results for two different momentum resolutions of the tracking system. From the required precision, a benchmark of $\sigma(1/p_t)$ better than $2 \times 10^{-5}$ /GeV/c [34, 37] was set for the tracking system.

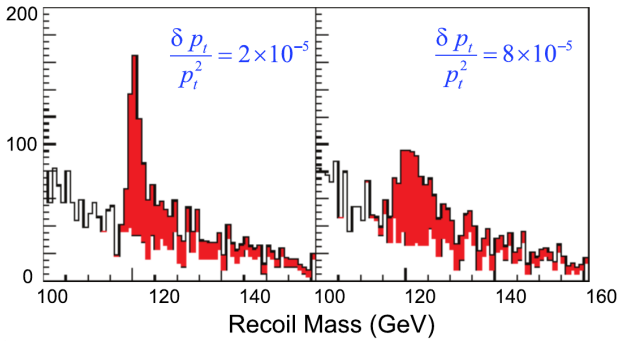



Figure 2.7: Simulated result of the Higgs recoil mass measurement in the $\mu^+\mu^-$ final state for two different tracking resolutions, from [37].

There are several more benchmark processes, which define the required precision for other subdetectors, see [36], [38] and [34].

### 2.3.2 ILC detectors

Two detectors [34] are foreseen for reasons of cross check, which can be exchanged at the single interaction point. The main difference between the two detectors is that the Silicon Detector (SiD) uses an all-silicon tracker, while the International Large Detector (ILD) is designed with a TPC (see Section 2.4.2). As a typical particle physics detector at an interaction point of an accelerator, the ILD is depicted in Figure 2.8. These types of detector follow an onion shape design with a barrel and two end caps. Each layer holds a subdetector with different tasks. The rotation axis of the barrel is the beam pipe, with the interaction point in the center of the detector. From inside to outside in Figure 2.8, the subdetectors are:

- The vertex detector (pink), which aims to measure the position of the interaction point and hence is closest to the center. It typically consist of several layers of silicon pixel detectors, which are able to register passing particles released from the interaction point with a precision of a few micrometers, when they pass through the detector material. With this detector, it is also possible to identify particles released from the interaction point with such a long lifetime,that they decay along their flight path. Long in that sense means that they decay some tens of micrometers from the primary vertex.

- The inner tracking system (yellow), which aims to measure the trajectory of particles in a magnetic field $B$, as they traverse the detector material. The physics of particle interaction in matter is explained in Section 2.4.1. For charged particles, the transverse momentum[1] $p_t$ can be calculated from the curvature $r$ of the track by inserting the numbers in the correct units:

$$p_t[GeV/c] = 0.3 \cdot B[T] \cdot r[m] \tag{2.4}$$

  For the ILD, a TPC was chosen as tracker. The concept and advantages of this type of detector are explained in the following section.

- The electromagnetic calorimeter (blue), which aims to measure the energy of particles mainly interacting by the electromagnetic force. Those particles are electrons, positrons and photons. They are ideally stopped by this detector and deposit their energy, which is then measured.

- The hadronic calorimeter (green), which aims to measure the energy of particles mainly interacting by the strong force. Those particles are all particles containing quarks and called hadrons.

- The muon system (brown), which aims to measure the tracks of muons. It is the outermost detector, as muons can penetrate all other subsystems with only little interaction. These leptons are not stopped by this detector and continue their path outside.

- Not an instrumented subsystem, but also an important part of the detector is the magnet (grey). It is needed to generate the magnetic field, in which charged particles are bent depending on their charge sign and momentum, see Section 2.4.2. In case of the ILD, a solenoid magnet with a field of 3.5 T was chosen.

The detector is specially designed to allow particle flow calorimetry [39]. The impact on the detectors are a fine grained calorimeter system and a low material budget for the main tracker to prevent scattering and energy loss. Together with a large tracking volume for particle separation and a good pattern recognition in dense track environments, these features are provided by a TPC. The requirements for the TPC

[1] the momentum perpendicular to the magnetic field

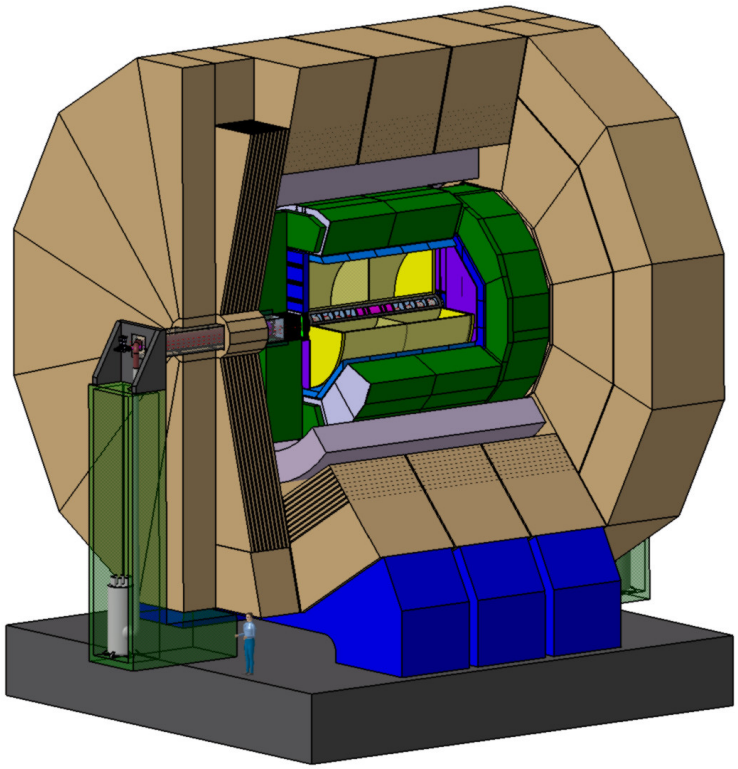


Figure 2.8: Schematic view of the ILD, from www.desy.de/flc. The different subdetectors are colour coded. They are from inside to outside the vertex detector (pink), inner tracking system (yellow), electromagnetic calorimeter (blue), hadronic calorimeter (green) and muon system (brown).

alone are a double hit resolution better then 2 mm in the endplate plane and 6 mm in the drift direction, an energy loss measurement $\delta E/\delta x$ of about 5 % precision and a momentum resolution $\sigma(1/p_t)$ better than $10^{-4}$ /GeV/c ($2 \times 10^{-5}$ /GeV/c for the whole tracking system). The latter can be translated to a spatial resolution better then 100 µm in the endplate plane ($\sigma_{r\phi}$) and 500 µm in the drift direction ($\sigma_z$) for conventional readout methods. More details about the ILD can be found in the Technical Design Report [34]. Such a high accuracy is challenging and requires new techniques and technologies. They will be explained in the next section.

## 2.4 Gaseous detectors

Large scale gaseous detectors for particle physics have already been invented in the 1970s and experienced a revival with the introduction of micro-structuring techniques. In Section 2.4.3, some examples of modern gaseous detectors are given. When gaseous detectors came up, they revolutionised particle tracking. In particular the Multi-Wire Proportional Chamber (MWPC) [40], for which George Charpak was awarded with the Nobel Prize in 1992, had an impact on the way data is taken and analysed. With this detector, tracks were for the first time recorded electronically. Before that, photos of tracks in bubble or spark chambers were state of the art and the analysis was done by eye.
A special concept for a gaseous tracking detector, the TPC, is explained in Section 2.4.2 with special emphasis on the ILD TPC mentioned in the previous section. There, the principles of operation and background for understanding how to improve that type of detector are provided. Beforehand, the

physics principle of gaseous tracking detectors will be described. It is based on the interaction of charged particles with gas atoms. The interaction of photons with matter, which are the photo effect, Compton scattering and pair production will not be addressed here and explanations can for example be found in [41]. But it has to be mentioned that there are many applications of gaseous detectors in that field summarised for example in [42].

### 2.4.1 Interaction of charged particles with matter

When a charged particle traverses matter it interacts through the following processes:

- Elastic scattering on electrons
- Excitation or ionisation of atoms
- Deflection in the coulomb field of atoms
- Elastic scattering and recoil on the nucleus
- Inelastic scattering with the nucleus
- In case the particle is faster than the speed of light in the medium, Cerenkov light is emitted

The energy loss per path length due to excitation and ionisation $\left(\frac{dE}{dx}\right)_{heavy,io,ex}$ is described by the Bethe formula [41] for relativistic heavy charged particles with mass $m >> m_e$:

$$\left(\frac{dE}{dx}\right)_{heavy,io,ex} = \frac{Z_1^2 \cdot e^4 \cdot n_e}{4 \cdot \pi \cdot \epsilon_0^2 \cdot v^2 \cdot m_e} \cdot \left[\ln\left(\frac{2 \cdot m_e \cdot v^2}{\langle E_b \rangle}\right) - \ln\left(1-\beta^2\right) - \beta^2\right] \tag{2.5}$$

where $Z_1$ is the charge of the particle, $e$ is the electron charge, $n_e$ is the electron density in the medium, $\epsilon_0$ is the dielectric constant, $v$ is the velocity of the particle, $m_e$ is the electron mass, $m_e$ is the electron mass, $\beta = v/c$ and $\langle E_b \rangle$ is the mean binding energy of the electrons in the medium. An approximation was found by Bloch: $\langle E_b(Z) \rangle \approx 16 \cdot Z^{0.9}$ eV.
The energy loss is slowly falling for heavy particles with rising energy. It depends on $(1/E) \cdot \ln(E/E_B)$ for low energies. With the energy expressed in terms of $\beta\gamma$ it reaches a minimum at $\beta\gamma \approx 3-4$ and then rises again due to the other terms. It can be shown that the position of the minimum only weakly depends on the absorber material. In gases, the energy loss is about 2 $\frac{\text{MeV}}{\text{g cm}^2}$ at that point. Particles with about this energy loss are called Minimum Ionising Particles (MIPs).
For light particles such as electrons with $v << c$ scattering due to coulomb interactions with the electron shell of the atoms has to be taken into account. For this case, Bethe found an approximation for the energy loss through ionisation

$$\left(\frac{dE}{dx}\right)_{light,io} \approx \frac{Z_1^2 \cdot e^4 \cdot n_e}{4 \cdot \pi \cdot \epsilon_0^2 \cdot v^2 \cdot m_e} \cdot \ln\left(\frac{m_e \cdot v^2}{2 \cdot \langle E_b \rangle}\right). \tag{2.6}$$

For low energies, positrons have to be treated in a different way because they can annihilate. Comparing with equation 2.5, the energy loss per track length is similar for particles with the same velocity. For the same energy however, the energy loss of an electron is suppressed by the factor $m_e/m_s$, where $m_s$ is the mass of the heavy particle. For relativistic particles, the difference in energy loss between electrons and heavy particles is small. For higher energies $O(100\,\text{m}_\text{e})$, bremsstrahlung dominates the energy loss.

The relationship is almost linear and can be integrated, such that the energy of the electron $E_e$ can be calculated in dependence of the path length $x$ in the medium.

$$E_e(x) = E_e(0) \cdot e^{-x/x_s}, \tag{2.7}$$

where $x_s$ is the radiation length. It corresponds to the distance, after which the energy of the electron has fallen to $1/e$. The value depends on the material and is in the order of 100 m for argon and 600 m for helium. An experimental result of an energy loss measurement for different particles is shown in Figure 2.11

It has to be mentioned that the energy loss is a statistical process where the Bethe formula only describes the mean energy loss per path length. In a single interaction of the traversing particle with a particle of the medium, the energy loss varies around this mean value. Especially in thin absorbers as gases, the distribution has a long tail, which is more prominent than described by a Landau distribution [43]. This means that a large amount of energy can be transferred from the traversing particle to an ionised electron. This electron, called delta, can subsequently start secondary processes and travel macroscopic distances of about 100 µm depending on the radiation length in the gas.

### 2.4.2 The Time Projection Chamber

The interaction of charged particles with a gas can be used to detect their flight path through the medium. It can be accessed through the ionised gas atoms, i.e. the ions and electrons. Naturally, they would recombine after some time due to the electromagnetic attraction. In a TPC however, an electric field prevents them from recombining. The ions are attracted to the cathode and the electrons to the anode, which generate the electric field. This already gives an idea of the TPC. It consists of a large gas volume enclosed in a chamber, with one wall being the cathode and the opposite wall being the anode. Apart from that, the geometry is in principle arbitrary. For the general onion shape design of a particle physics detector, a cylindrical shape is preferred with a cathode in the center and two anodes at each end cap. An inner cylinder holds the beam pipe and vertex detector. So in principle, such a device consists of two TPCs.

Figure 2.9 shows a schematic drawing of the ILD TPC. If a charged particle traverses the gas, it ionises the atoms along the track. The charges are separated in the electric field and drift towards the endplates. The barrel of the cylinder is designed as a field shaper to provide a uniform electric field in the gas volume, such that the field lines are precisely perpendicular to the endplates. This is necessary as only in this case, a projection of the track is mapped as a two-dimensional image on the endplates. As the electrons drift much faster then the ions and are more easy to amplify, the anode is used to register the signals. For that reason, it is segmented to resolve the projection of the track. The readout also measures the arrival time of the electrons and hence can reconstruct the primary ionisation position and the particle track. However, only the relative timing can be measured. To obtain the absolute path of the track, an external reference point is necessary, which is provided by the other tracking systems of the ILD.

The registration of single electrons from the primary ionisation is not directly possible, because the signal would be too weak for the electronics. For that reason, gas amplification structures with a high granularity are placed at the anode, see Section 2.4.3. The slower ions drift to the cathode and are neutralised there. A magnetic field parallel to the electric field bends the charged particles such that their momentum can be calculated by Equation 2.4 from the curvature. In addition, the presence of that field increases the point resolution at the anode, as is shown in a following section, which follows the argumentations outlined in [44] and [45].

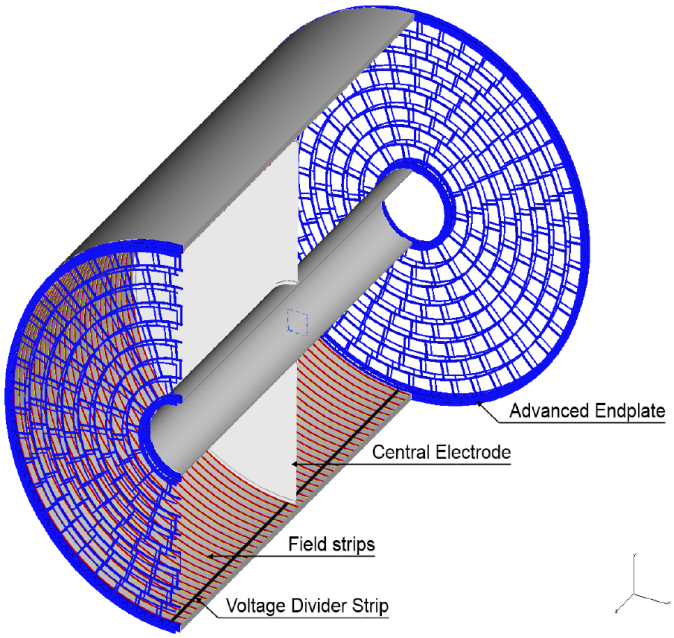



Figure 2.9: Schematic of the ILD TPC, from [46]. The inner and outer walls are shown in grey, the endplates in blue. The field shaping strips are displayed on the outer wall in red. The inner wall is also equipped with such strips (not shown). The beam pipe with the central vertex and inner detector are placed in the volume inside the inner wall.

### Drift

In the presence of an electric and magnetic field, the equation of drift for a charged particle, e.g. an electron, is given by

$$m\frac{d\vec{v}}{dt} = e\left(\vec{E} + \vec{v}\times\vec{B}\right). \tag{2.8}$$

In matter, an additional term caused by the friction force $\vec{f}$ must be added because the electrons of mass $m$ collide with the gas particles with a mean collision time $\tau$ [47]. The force is assumed to be proportional to the velocity of the electrons: $\vec{f} = -m\cdot\vec{v}/\tau$. In the equilibrium, the drift velocity $\vec{v}_d$ is constant and Equation 2.8 reads

$$\frac{\vec{v}_d}{\tau} - \frac{e}{m}\vec{v}_d\times\vec{B} = \frac{e}{m}\vec{E}. \tag{2.9}$$

Moreover, as the drift velocity is constant, the drift distance $l_d$ is a linear function of the drift time $t_d$:

$$l_d = v_d\cdot t_d \tag{2.10}$$

being the key formula for the working principle of a TPC. By this equation, the z-position of primary charges can be reconstructed by measuring their arrival time at the endplate. The Langevin formula is the solution for $\vec{v_d}$:

$$\vec{v}_d = \frac{e}{m}\tau E\frac{1}{1+\omega^2\tau^2}\left(\hat{e}_E + \omega\tau\left(\hat{e}_E\times\hat{e}_B\right) + \omega^2\tau^2\left(\hat{e}_E\cdot\hat{e}_B\right)\hat{e}_B\right) \tag{2.11}$$

with $\hat{e}$ being the unity vectors of the fields and $\omega = (e/m)B$ being the cyclotron frequency. For typical magnetic field strengths of $O(1\,\mathrm{T})$, $\omega\tau$ is small and $\hat{e}_E$ and $\vec{v}_d$ have almost the same direction. Without

magnetic field, the drift velocity is given by

$$\vec{v}_d = \frac{e}{m}\tau\vec{E} = \mu\vec{E} \tag{2.12}$$

with $\mu = e\tau/m$ being called the mobility. With magnetic field, the amplitude of $\vec{v}_d$ is given by

$$|\vec{v}_d(\omega)| = \frac{1 + \omega^2\tau^2\cos(\phi)}{1 + \omega^2\tau^2} \cdot |\vec{v}_d(0)|, \tag{2.13}$$

with $\phi$ being the angle between the electric and magnetic field. In case both are parallel, as it is in a typical TPC setup, the drift velocity is not reduced.
The mobility $\mu$ depends on the cross section of the ions or electrons drifting through the gas. For ions, it is almost constant, whereas for electrons, there is no simple formulation. Simulation software as for example `Magboltz` [48] is used to evaluate $v_d(E)$. In general, due to the mass terms, the electron drift velocity is three orders of magnitude higher then the drift velocity of ions. Figure 2.10 shows the measured and simulated drift velocity (displayed as black line `W`) of electrons in so called T2K gas (95 % Ar, 3 % $CF_4$, 2 % $iC_4H_{10}$) for different magnetic fields.

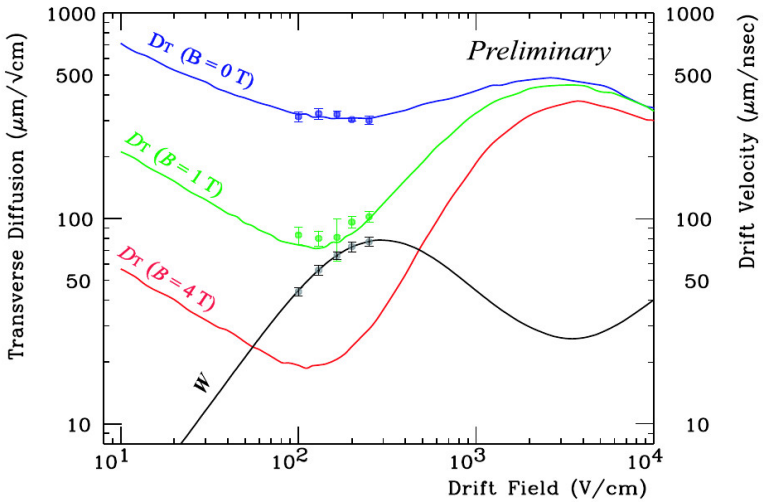



Figure 2.10: Transverse diffusion constant $D_T$ and drift velocity $W$ measured in T2K gas. The solid lines are simulated with `Magboltz`, from [49].

### Diffusion

A point-like electron or ion cloud in a gas diffuses with time due to the thermal movement. With additional drift, the center of the cloud will be at the position $\left(0, 0, z_{drift} = t \cdot v_d\right)$ assuming an electric field in z-direction and a start position at the origin. If the diffusion is the same in all directions, the cloud will have a Gaussian shape with

$$n(r,t) = \left(\frac{1}{4\pi D_c t}\right)^{3/2} \cdot \exp\left(-\frac{r^2(t)}{4D_c t}\right), \tag{2.14}$$

where $r^2(t) = x^2 + y^2 + (z + v_d t)^2$). The width of the cloud is characterised by $\sigma_i^2 = 2D_c t$, where $D_c$ is the diffusion coefficient. From [44], it can be found that $\sigma_i^2$ can also be calculated from the microscopic

picture. Then, $D_c$ is given by $2\epsilon\mu/3e$ with $\epsilon = mu^2/2$ the average energy of the drift particles. $u$ is the mean drift velocity and $\mu$ the mobility. Expressing the drift time as $t = z_{Drift}/\mu E$ (see Equation 2.12), one gets

$$\sigma_i = D\sqrt{z_{Drift}}. \tag{2.15}$$

$D = \sqrt{\frac{2D_c}{\mu E}} = \sqrt{\frac{4\epsilon}{3eE}}$ is the diffusion constant. The energy of the drifting particle is given by the sum of the kinetic and thermal energy:

$$\epsilon = \epsilon_{kin} + \epsilon_{therm} = 1/2mv_d^2 + 3/2k_BT, \tag{2.16}$$

where $k_B$ is the Boltzmann constant and $T$ is the gas temperature. Therefore, the diffusion constant cannot be lower than

$$D_{min} = \sqrt{\frac{2k_bT}{eE}}. \tag{2.17}$$

For an electric field of 100 V/cm at room temperature, this translates into $D_{min} \approx 230\,\mu\text{m}/\sqrt{\text{cm}}$ and for 1 kV/cm into $D_{min} \approx 70\,\mu\text{m}/\sqrt{\text{cm}}$. Gases, in which the total energy is close to the thermal energy are called cold gases. In these gases, the electrons cannot achieve high velocities due to the fact that they loose energy to the gas. Vibrational or rotational energy levels absorb the energy. For those gases, the drift velocity is limited. For hot gasses, the total energy is dominated by the kinetic energy of the particles. In this case the diffusion constant is given by

$$D = \sqrt{\frac{2mv_d^2}{3eE}}, \tag{2.18}$$

but a simple relation between $v_d$ and $E$ cannot be found, as has been explained in the previous section. Looking at the diffusion constant, one can see that it depends on the mobility, which itself depends on the mean time between collisions. In direction of drift, collisions are more probable and hence, the diffusion constant is different in longitudinal ($D_L$) and transverse ($D_T$) direction. The electron cloud has a different width in the xy-direction compared to the z-direction:

$$\sigma_{xy} = D_T\sqrt{z} \qquad \text{and} \qquad \sigma_z = D_L\sqrt{z} \tag{2.19}$$

Figure 2.10 shows the transverse diffusion $D_T$ in dependence of the electric field.

For a TPC, the diffusion in xy-direction and z-direction should be as low as possible to increase the resolution. It was shown that this depends on the gas, but can also be improved by a magnetic field pointing in the same direction as the electric field. This decreases the diffusion at least in the xy-direction. Similar to Equation 2.13, the transverse diffusion can be expressed as ($\phi = 90°$)

$$D_T\omega = \frac{D_T(0)}{1 + \omega^2\tau^2}. \tag{2.20}$$

But the drift velocity shall be high as well to increase the bunch crossing rate the TPC can sustain. These two requirements are contradictory for a single gas. For that reason, gas mixtures are used, in which the drift velocity and diffusion become a more complex function of the electric field. For the T2K gas mixture, the drift velocity has its maximum at approximately the same electric field strength where the diffusion has its minimum, see Figure 2.10.

### Gas amplification

The primary electrons from the ionisation of a particle track arrive at the endplate and form a projection of the track. In the optimal case, every primary electron should be registered with a high timing precision. However, it is not possible to directly detect a single electron, because the currently available electronics is not sensitive enough[2] . Hence, the charge has to be amplified. For a TPC, the same medium as in the drift cylinder is used, namely the gas. A second region is formed by electrodes directly in front of the endplate with the charge sensitive electronics. In this region, called the amplification region, the electric field is large enough that the primary electrons are accelerated up to energies, where they themselves ionise gas atoms and create secondary electrons. Those are also accelerated and an avalanche is formed to create a signal, which can be registered by the electronics. The theory of gas amplification is complex and the reader is referred to books like [51] or original publications like [52] or [53]. The key elements of the theory are:

- The gas amplification is a statistical process and the number of electrons produced from a single electron can vary significantly. The distribution can be approximated by the Polya distribution. It has a long tail and the mean value of the distribution is often referred to as the gas gain.
- The mean gas gain depends on the potential difference within the gas amplification structure. Typically the devices are operated in the proportional counter mode at a gas gain of about $10^3$ - $10^5$. For higher fields, a single primary electron can cause a discharge of the amplification structure, which resembles the streamer mode. At a gain of about $10^8$ the Raether limit [54] is reached and continuous gas discharges occur.
- In the proportional mode, the mean gain rises exponentially with the electric field in the amplification structure.
- In the gas avalanche, the same amount of ions as electrons is created. They would cause enormous field distortions in the drift region of the TPC if they are not neutralised in the amplification structure or otherwise. For that reason, another structure, called a gating device, can be placed close to the amplification structure. By changing the potential of this structure, it can prevent the ions from entering the drift region. In this configuration, the primary electrons can not pass the gate as well. Thus in case a gate is applied, the TPC has to be operated in a pulsed mode and continuous readout of the drift region is not possible. The amplification structures introduced in the next section already have a low intrinsic ion back drift rate compared to MWPC.
- Photons can also be generated in the amplification process. They can themselves ionise the gas and leave the avalanche. This leads to an unstable operation and secondary avalanches. To suppress this unwanted effect, a low fraction of a different gas (for example isobutane: $iC_4H_{10}$), is mixed into the main mixture, called the quenching gas. It absorbs the photons through the excitement of rotational or vibrational modes, which do not lead to ionisation.

For the gas amplification, different technologies are used, of which one is the already mentioned MWPC, for example at the ALICE TPC [55]. In the 1990s, new technology was introduced taking advantage of the micro-structuring technique. These Micro-Pattern Gaseous Detectors (MPGDs) have some advantages, which will be shown in Section 2.4.3 by looking at two types, the Gas Electron Multiplier (GEM) [56] and the Micro-Mesh Gaseous Structure (Micromegas) [57].

[2] The minimal detectable charge depends on the detector capacitance and therefore, no general number can be given. For the GdSP chip developed for pad-based TPC readout, the noise level is at about 1000 electrons [50].

### TPC measurements

For a TPC as tracking detector, the first goal is to measure the path of charged particles as precise as possible. In Section 2.4.1 it was shown that the interaction of the charged particle causes the ionisation, which gives access to this measurement. However, the interaction leads to an energy loss of the particle itself. It was shown that the mean energy loss per path length is described by the Bethe formula for electrons (Equation 2.6) and heavier particles (Equation 2.5). For different particle types with the same momentum, the energy loss differs due to the difference in mass. So if the momentum and the energy loss can both be measured, this can give a hint on the particle type. Figure 2.11 shows the energy loss of different particles in dependence of their momentum. The populations of the individual particles can be identified. However there are regions, in which the assignment is not explicit. The electron shows a different behaviour compared to the heavier particles.

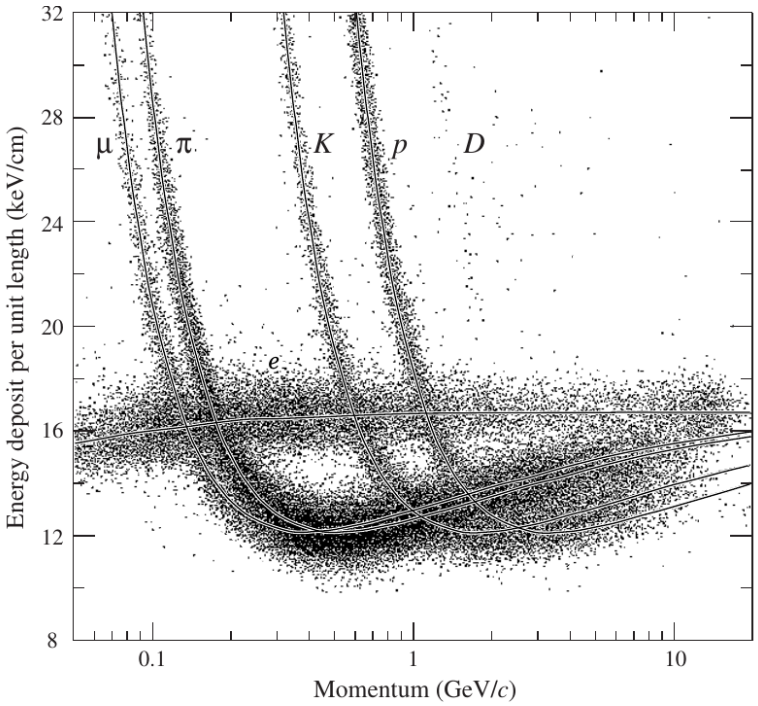



Figure 2.11: Energy loss $dE/dx$ in dependence of the particle momentum in Ar/$CH_4$ 80/20 at 8.5 bar, from [58].

The energy loss can be accessed by the ionisation density along the track. The number of ionised electrons depends on the ionisation potential of the gas $I_0$ and the mean energy $W$ needed to create an electron ion pair. Secondary processes play an important role, which means that the number of atoms $\eta_P$ directly ionised by the traversing particle only makes up about one third of the finally released primary electrons $\eta_T$. These values are listed in Table 2.1 for different gases together with the energy loss $dE/dx$. In addition, the radiation length $X_0$ is displayed.
If every single primary electron can be registered, counting the number of electrons per track length gives direct access to $dE/dx$. As the gas amplification is in the proportional mode, the signal height from several amplified primary electrons can also be used. However, this method is influenced by the statistical fluctuations of the gas gain.
For the measurement of momentum, the motion of the charged particle in the magnetic field is used. Due to the Lorentz force, the general trajectory is given by a helix. It can be separated into a circular motion in the plane perpendicular to the field and a straight line in direction of the field. It was shown in

| **Gas** | $I_0$[eV] | $W$[eV] | $dE/dx$[keV/cm] | $\eta_P$[1/cm] | $\eta_T$[1/cm] | $X_0$[m] |
|---|---|---|---|---|---|---|
| He | 24.5 | 41 | 0.32 | 4.2 | 8 | 745 |
| Ne | 21.56 | 36.3 | 1.56 | 12 | 43 | 345 |
| Ar | 15.7 | 26 | 2.44 | 23 | 94 | 110 |
| Xe | 12.1 | 22 | 6.76 | 44 | 307 | 15 |
| $CF_4$ | 15.9 | 54 | 7 | 51 | 100 | 92.4 |
| $C_4H_{10}O_2$ | 10.0 | 23.9 | 3.9 | 55 | 160 | 222 |
| $CO_2$ | 13.7 | 33 | 3.01 | 35.5 | 91 | 183 |
| $CH_4$ | 15.2 | 28 | 1.48 | 25 | 53 | 646 |
| $C_2H_6$ | 11.7 | 27 | 1.15 | 41 | 111 | 340 |
| $iC_4H_{10}$ | 10.6 | 23 | 5.93 | 84 | 195 | 169 |

Table 2.1: Parameters important for the energy loss measurement (most probable value given) for different gasses at 20 °C and 1013.25 mbar for minimum ionising particles, from [59].

Equation 2.4 that by knowledge of the magnetic field magnitude it is sufficient to measure the radius of the track to have access to the fraction of the momentum perpendicular to the field. The fraction parallel to the magnetic field can be extracted from the z position of the hits on the helix. The sign of the charge can already be extracted from the direction of bending.

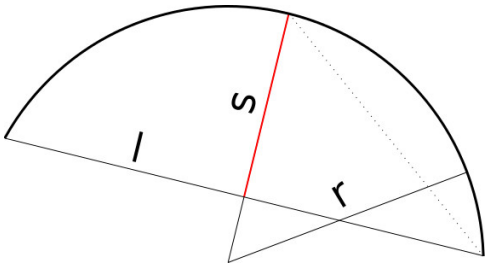



Figure 2.12: Definition of the sagitta $s$ for a circle with radius $r$, of which only a part of the circle arc with half length $l$ is given.

However, this method can only be applied to tracks with such a low momentum that they don't leave the TPC. The most interesting tracks have such a high momentum that they almost leave a straight line of ionisation in the detector. For those tracks, the curvature has to be measured by the sagitta $s$ (see Figure 2.12) in the xy-plane and for a total momentum measurement, the track angle towards this plane has to be known. When $l$ is the half length of the arc, then $L = 2l$ is the complete track length and $s$ can be approximated for $s << L$ by

$$r^2 = l^2 + (r-s)^2 \Rightarrow s = r - \sqrt{r^2 - l^2} \Rightarrow s \approx \frac{l^2}{2r} = \frac{L^2}{8r} \Rightarrow r = \frac{L^2}{8s}. \tag{2.21}$$

Using Equation 2.4 together with Equation 2.21 we get the accuracy of the momentum measurement:

$$\frac{\sigma_{p_t}}{p_t} = \frac{\sigma_r}{r} = \frac{8p_t \cdot ds}{0.3BL^2}. \tag{2.22}$$

From this equation, one can see that the momentum resolution depends linearly on the momentum and the accuracy on the sagitta. It is also inversely proportional to the bending power $BL^2$. The increase of the lever arm has the highest effect, as $L$ goes quadratically into the equation. However in practice,

the increase of this value is the most significant cost driver. This holds not only for a TPC, but also for the whole detector and especially the magnet and calorimeters, which have to enclose the TPC. For practical purposes, the formula can be rewritten with typical units as

$$\frac{\Delta p_t}{p_t} \approx 0.25 \left(\frac{\Delta s}{100\,\mu\text{m}}\right) \cdot \left(\frac{1\,\text{m}}{L}\right)^2 \cdot \left(\frac{1\,\text{T}}{B}\right) \cdot \left(\frac{p_t}{100\,\text{GeV}}\right). \tag{2.23}$$

The uncertainty of the sagitta measurement depends on the precision of the single point measurement $\sigma_{xy}$. For $N$ measurement point at equal distance, the Gluckstern equation [60] describes the momentum resolution:

$$\left(\frac{\sigma_{p_t}}{p_t}\right)_{sag} = \frac{\sigma_{xy} p_t[GeV]}{0.3BL^2} \sqrt{\frac{720}{N+4}} \tag{2.24}$$

A similar equation can be obtained for the resolution of the track angle towards the xy-plane. The factor 720 reduces to 320, if one end of the track is well known. This is for example the case if the vertex is measured with high precision. Gluckstern also noted that it is not important to measure the hits along the whole track. The best precision can be achieved if $N/4$ points are measured at the beginning and the end of the track arc and $N/2$ at the center. In this case, the factor under the square root becomes $256/N$. In addition to the sagitta measurement, multiple scattering has an influence on the precision of the momentum measurement. This is due to the fact that the charged particles undergo elastic scattering when traversing the gas and do not fly along a straight path. Every interaction leads to a small deviation of the original direction. The change of angle is a Gaussian distribution following the central limit theorem of statistics. The width of the distribution transforms into an uncertainty of the curvature given by [61]

$$\sigma_\theta = \frac{13.6\,\text{MeV/c}}{\beta p} \cdot \sqrt{\frac{L}{X_0}} \cdot \left[1 + 0.038 \cdot \ln\left(\frac{L}{X_0}\right)\right], \tag{2.25}$$

where $X_0$ is the radiation length. Using

$$\frac{\sigma_{p_t}}{p_t} = \frac{\sigma_r}{r} = \frac{\sigma_\theta}{\theta} \quad \text{as} \quad r = L/\theta \tag{2.26}$$

and dropping the logarithmic term (for TPCs $X_0 \gg L$), one gets

$$\left(\frac{\sigma_p}{p}\right)_{MS} = \frac{13.6\,\text{MeV/c}}{\beta p} \cdot \sqrt{\frac{L}{X_0}} \cdot \frac{r}{L} = \frac{13.6\,\text{MeV/c}}{\beta p} \cdot \sqrt{\frac{1}{LX_0}} \cdot \frac{p}{eB}. \tag{2.27}$$

For relativistic particles ($\beta \approx 1$) this can be approximated [62] when inserting the numbers in the correct units by

$$\left(\frac{\sigma_p}{p}\right)_{MS} \approx 0.054 \frac{1}{B[T]} \sqrt{\frac{1}{L[m]X_0[m]}}. \tag{2.28}$$

If the factor $\beta$ is neglected, the relative momentum resolution from multiple scattering is constant. The total momentum resolution is the sum of both, momentum resolution and multiple scattering:

$$\left(\frac{\sigma_{p_t}}{p_t}\right)^2 = \left(\frac{\sigma_{p_t}}{p_t}\right)^2_{sag} + \left(\frac{\sigma}{p}\right)^2_{MS} \tag{2.29}$$

For a pad-based ILD, the foreseen parameters are:

- Inner radius: 329 mm, outer radius: 1808 mm $\Rightarrow L_{min}$ (if the track is perpendicular to the beam

pipe): $\approx 1.5\,\mathrm{m}$

- Number of pad rows $N = 200$
- Magnetic field $B = 3.5\,\mathrm{T}$
- Pad resolution $\sigma_{xy} = 100\,\mu\mathrm{m}$
- Gas radiation length (for simplicity just for argon) $X_0 = 110\,\mathrm{m}$

Inserting those into the equation, one gets

$$\left(\frac{\sigma_p}{p}\right)_{MS,ILD} = 1.2 \cdot 10^{-3} \qquad \text{and} \qquad \left(\frac{\sigma_{p_t}}{p_t}\right)_{sag,ILD} = 7.95 \cdot 10^{-5} \cdot p[GeV]. \tag{2.30}$$

Additionally, the $p_t$ resolution depends on the angle, as the track length in the TPC increases for increasing angle. For more details on this, the reader is referred to the literature [61]. For the ILD, the required performance is typically quoted as $\sigma_{1/p} = \sigma_p/p^2$. For low momenta, the resolution is limited by multiple scattering to about $10^{-3}\,\mathrm{GeV}^{-1}$ at 1 GeV, then falling as $1/p$ to reach the maximum at $7.95 \times 10^{-5}\,\mathrm{GeV}^{-1}$. In fact, one can see in Figure 2.13 that the momentum resolution performance follows this behaviour. The figure is taken from the ILD Letter Of Intent [38] with slightly different numbers than quoted for the current ILD design. For the design study, the required resolution was driven by physics, as was discussed at the end of Section 2.3. From the required resolution, the single point resolution $\sigma_{xy}$ was deduced.

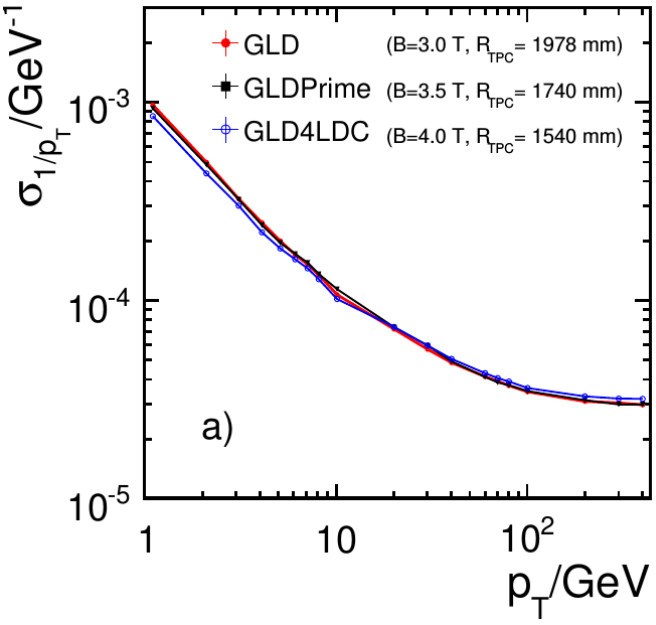



Figure 2.13: Momentum resolution as function of the transverse momentum of different ILD models for simulated muons perpendicular to the beam axis, from [38].

The track model also has effects on the momentum resolution. In the previous discussion, the track curvature was measured by its radius or the sagitta. This assumes that the curvature is constant along the track. However, the particle looses energy and hence, this assumption is not correct. More complex algorithms also take the energy loss into account as for example the Kalman filter [63].

As can be seen by Equation 2.24 and 2.28, the resolution of a TPC can mainly be improved by increasing the lever arm $L$ and hence the size of the subdetector. As the TPC has to be embedded in the magnet and is surrounded by the calorimeters, which would also have to increase, this is not an option due to the costs. An increase of the magnetic field can also increase both parts of the resolution. The technological advancement of gaseous detectors themselves, which is also the topic of this thesis, comes through an improved single point resolutions $\sigma_{xy}$ and granularity with more measurements $N$. Details on how this can be achieved are shown in Section 2.4.3 and 3.2.

#### Comparison to other tracking detectors

The tracking detector to compare the TPC with is an all-silicon tracker. Such a detector subsystem consists of $O(10)$ concentric layers of silicon detectors. Charged particles from the vertex pass through the material and leave a signal, which can be localised with a precision $O(10\,\mu\text{m})$. As the particle has to penetrate solid material, a radiation length of about 10-15 % $X_0$ is reached for the central region and 20-25 % $X_0$ in the endcap region in total [34]. The signal is fast and the time stamping precision can reach $O(10\,\text{ns})$. Due to the costs, the lever arm of silicon trackers is typically smaller than the one for a TPC, as the surface equipped with the expensive silicon sensors increases with $r^2$. However, this reduces the costs of the calorimeters and the magnets. The SiD [34], the other detector planned at the ILC, is designed with an all-silicon tracker.
Clearly, a TPC is not that fast. Due to the electron drift time of about 50 µs to cover the maximum drift distance, the collision rate is limited if all tracks from a single collision shall be read out. This does not necessarily have to be the case. For example the ALICE TPC will be operated with a collision rate of 50 kHz (LHC Run 3, [64]) with tracks from several interactions filling the TPC volume. For the ILC, the beam parameters are such that there is enough time to read out the complete volume between two bunch trains (199 ms). Several collisions within one bunch train of 1 ms length are integrated in the ILD concept. However the ions, which drift by far slower, will not reach the cathode and there will be about three ion discs from the amplification region which could cause large field distortions. To minimise them, the ion feedback of the amplification structure has to be minimised. The radiation length of the detector material, the gas, is less than 1 % $X_0$ and including the barrel consisting of field cage and strengthening it is smaller than 5 % $X_0$ for the ILD design. At the endplates with the gas amplification and readout, the design foresees less than 25 % $X_0$ [34]. This feature is especially helpful for the particle flow concept, in which the calorimeters play an important role. They receive the primary particles with almost their complete energy and original direction. The scattering and pair production is reduced as well.

### 2.4.3 Micro-pattern gaseous detectors

As explained before, an amplification of the primary electrons at the enplates is necessary to get a measurable signal. In Section 2.4.2 it was shown that this can be achieved by gas amplification in a high electric field. For reasons of fast signal generation, the amplification structures have to be small and should not release the ions from the amplification process into the drift region even if the ion back flow can be decreased with a gating device in case of the ILC. The two most commonly used structures are explained in this section. The intrinsic spatial resolution of gaseous detectors is limited by the segmentation of the amplification structure. Due to the progress in micro-structuring, the devices can be processed to have an intrinsic segmentation of $O(1 - 100\,\mu\text{m})$. This does not directly translate into the final spatial resolution of the endplate, because it also depends on the segmentation, technique of the readout and the gas properties as diffusion.

### GEMs

A GEM is a foil of isolating material with a thin metallic layer on both sides, see Figure 2.14. It was invented by Fabio Sauli in 1996 [56]. Typically, it is made of 50 µm Kapton and a copper coating. In a regular pattern, holes are drilled or etched through the foil such that an optical transparency of about 20 % is reached. A potential difference is applied between the two sides to achieve gas amplification within the field inside the holes. If the shape of the holes is optimised, the transparency for the primary electrons can reach values close to 100 % in a wide range of the ratios between drift and amplification field. The gas amplification reaches values of about 10-1000, which is at the edge of what can be detected by electronics. For the highest gains, the discharge probability increases. Then, the stability decreases and the GEM can even permanently be destroyed. Several layers of GEM foils can be placed on top of each other as a stack with transfer fields between them. The readout is placed below the last GEM with another transfer field called the induction field, see Figure 2.15. By tuning the different fields and shifting the different GEMs with respect to each other, the ion back flow can be minimised [65]. This will also affect the transparency and gain. By still acceptable values of the latter, the number of ions flowing back into the ionisation region can be reduced to $\mathcal{O}(0.2)$ % of the number of secondary electrons.

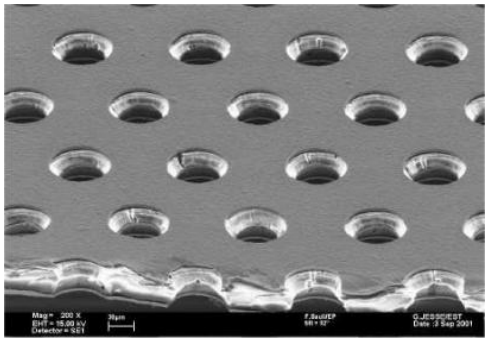


Figure 2.14: Scanning Electron Microscope (SEM) image of a GEM foil of 50 µm thickness with holes of 70 µm diameter and a distance of 140 µm, from http://gdd.web.cern.ch/GDD.

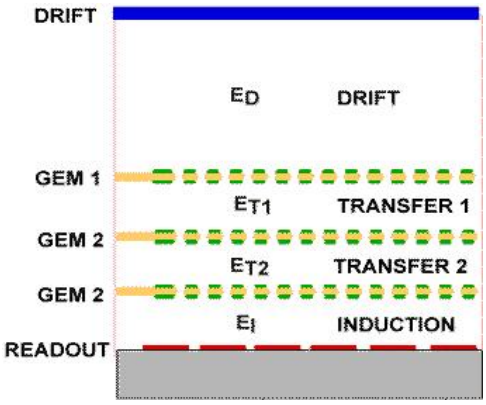



Figure 2.15: Schematic of a triple GEM stack, from http://gdd.web.cern.ch/GDD/.

### Micromegas

The Micromegas was invented in 1995 by Yannis Giomataris [57]. In this concept, a thin metallic grid separates the drift from the amplification region. The grid is on a high potential with respect to the readout anode, which is 10 to 100 µm below. In this gap, gas amplification takes place when a primary electron enters through a hole. A simulated avalanche is shown in Figure 2.16. This has the advantage that the avalanche electrons immediately arrive at the readout in about 1 ns. A disadvantage is that sparks can damage the electronics. The ions are collected within 30 to 100 ns, which allows for a high rate. Typical gains of a Micromegas are a few thousands, but also up to $10^5$ were achieved. As the amplification gap is small, the final electron signal ends up on a narrow area at the readout. The amplification and drift field are uniform, see Figure 2.17, except for the area around the grid holes. By tuning the field ratio and grid parameters, a transparency to primary electrons of close to 100 % can be achieved by an ion back flow of $\mathcal{O}(0.2\ \%)$ [66]. A special type of Micromegas, the InGrid, is shown in Section 3.2.

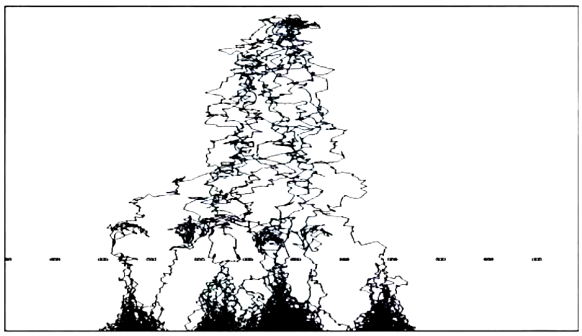


Figure 2.16: Simulation of the avalanche process of several primary electrons in a Micromegas. The primary electrons enter the region of high electric field through the holes in the mesh and are amplified, from [66].

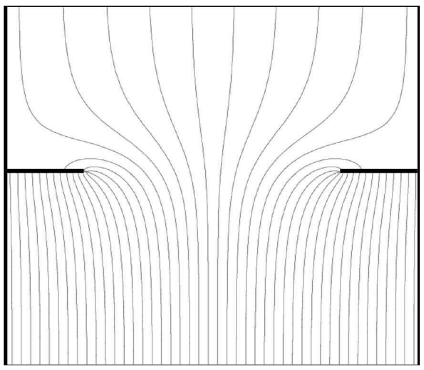


Figure 2.17: Field lines in the region of a hole in the grid of a Micromegas with the drift field at the top and the amplification field at the bottom, from [44].

CHAPTER 3

# Hardware background

After the physics background to understand the principles of the TPC and the measurements that can be performed with the detector have been introduced in the last chapter, the tools necessary for the further development will be explained in this chapter. It has to be mentioned that those tools have not been developed within the scope of this thesis, but were mainly just used. For some components however, especially the Scalable Readout System (SRS) explained in Section 3.5, the work done within this thesis provided significant input.
As the main aspect was the development of a readout system for the Pixel-TPC, the device to be read out needs to be explained as well as the technology for achieving this task. It has been tried to keep the technical details to a minimum. However, to understand the challenges, which a readout system has to face, at some points a general summary would not be sufficient.
First of all, the Timepix chip will be explained in Section 3.1. It is the front-end chip that is read out and controlled by the readout system to be built. The InGrid, a special type of Micromegas with pixel readout, will then be described in Section 3.2. With this fragile, but high-precision device, a large area detector was constructed. As the Timepix readout system is based on a Field Programmable Gate Array (FPGA), the largest part of this chapter introduces these chips and how they can be programmed (Section 3.3). Towards the end of the chapter in Sections 3.6 and 3.5, the boards are introduced, on which the FPGAs are placed. They make up the core of the readout system. Finally in Section 3.7, some basics of network communication will be provided.

## 3.1 The Timepix chip

The Timepix Complementary Metal-Oxide-Semiconductor (CMOS) Application Specific Integrated Circuit (ASIC) [67] [68] is an imaging chip, shortly called Timepix or Timepix chip. It was derived from the Medipix2 chip [69], a high spatial and high contrast resolving single photon counting chip, on behalf of the EUDET[1] collaboration. Medipix2 is used in medical applications to detect X- and gamma-rays and was designed by the Medipix collaboration at CERN. As a converter material, silicon sensors are bump-bonded onto the chip. In the scope of this thesis research, gases are used to convert photons or tracks of charged particles into an electrical signal. The idea to combine a pixelated readout with a gaseous detector was already validated in 2004 [70], when a Medipix2 chip was combined with a

[1] The EUDET project was supported by the European Union in the 6th Framework Programme structuring the European Research Area. The subject was detector R&D towards the International Linear Collider, see www.eudet.org.

Micromegas. For a TPC environment, the properties of the Medipix2 chip were not sufficient. EUDET requested the Timepix chip in 2006 with mainly one additional feature with respect to Medipix2: The capability to measure the arrival time of charge. It was submitted for production in 250 nm technology at IBM in July of that year. The first twelve wafers arrived at CERN in September 2006. After some minor modification to the available Medipix readout systems, it was successfully tested [71]. In 2007, it was used the first time in a test beam with a triple GEM amplification structure [72]. Since September 2013, the successor of the chip, called Timepix3, is available. Over the intervening years, pioneering research has been carried out and the Timepix chip is still used in experiments.
Remark: The Timepix partly is a digital chip, which means that the binary states 1 and 0 are used to encode information. Those states are realised in electronics as for example different voltage potentials. Often, a state is defined as binary 1, if the potential is equivalent to the supply voltage. Similarly, a potential equivalent to ground(`GND`) defines the binary state 0. Often, the states or potentials are simply called high (1) and low (0).

### 3.1.1 Surface characteristics

Like the Medipix2, Timepix consist of a 256 × 256 pixel matrix and a periphery. Each pixel has a size of 55 µm × 55 µm and hence the total active area is 14.08 mm × 14.08 mm. The sensitive area on each pixel is an octagon with 10 µm edge length. Including the periphery, the total surface of the chip is 227.5 $mm^2$. On the periphery side, 127 bonding pads, alignment marks, snake pads and a fuse register for unique chip identification are placed. The in- and output signals of the chip are listed in Table 3.1.

| Signal name | Type | Route | Description |
|---|---|---|---|
| ENABLE_INC | CMOS | Input | Falling edge starts operation if `Reset` and `Shutter` aren't active (High). Internally pulled down with a 5 kΩ resistor. |
| PENABLE_IN<br>NENABLE_IN | LVDS | Input | Falling edge starts operation if `Reset` and `Shutter` aren't active (High). Internally pulled down with a 5 kΩ resistor. |
| ENABLE_OUTC | CMOS | Output | High: Resetting, counting or performing any operation. Low: End of operation. |
| PENABLE_OUT<br>NENABLE_OUT | LVDS | Output | High: Resetting, counting or performing any operation. Low: End of operation. |
| PFCLOCK_IN<br>NFCLOCK_IN | LVDS | Input | Fast Clock input. Clk_Count input. |
| PFCLOCK_OUT<br>NFCLOCK_OUT | LVDS | Output | Fast Clock output. |
| PDATA_IN<br>NDATA_In | LVDS | Input | Timepix serial port input. |
| PDATA_OUT<br>NDATA_OUT | LVDS | Output | Timepix serial port output. |
| DOUT<0:31> | CMOS-HiZ | Output | Timepix parallel port output. When not used is at HiZ state. |
| RESET | CMOS | Input | Low: Resets the chip Input/Output (I/O) Counters and Fast Shift Register (FSR). High: Any I/O Operation or Counting can be done. |
| SHUTTER | CMOS | Input | Low: Chip is in counting mode if `Reset` is High. High: Any IO Operation can be done. |
| M0 | CMOS | Input | Operation Select Bit0. |

| Signal name | Type | Route | Description |
|---|---|---|---|
| M1 | CMOS | Input | Operation Select Bit1. |
| P_S | CMOS | Input | High: Parallel Readout. Low: Serial Readout. |
| SPARE_FSR | CMOS | Input | Not used in Timepix. |
| POLARITY | CMOS | Input | High: Pixel is set to collect positive charges (holes). Low: Pixel is set to collect negative charges (electrons). |
| PBUS_ACCES | CMOS-HiZ | Output | When High the Parallel Readout Bus is being accessed. |
| ENABLE_-TPULSE | CMOS | Input | High: Enables the pixel Test. Low: Disables the pixel Test. |
| ENABLE_CST | CMOS | Input | High: Enables the charge sharing test. Low: Disables the charge sharing test. |
| | | | |
| EXTDAC_IN | Analogue | Input | External Digital-Analogue Converter (DAC) input to set any of the 13 DACs. |
| TEST_IN | Analogue | Input | Voltage step input used to test the pixels. |
| DAC_OUT | Analogue | Output | Analogue buffered output to measure one of the 13 DACs voltages output. |
| VGB_EXT | Analogue | Input | External reference voltage for the DACs. To set to 1.1604V. |
| SELECT_VGB_-EXT | Analogue | Input | High: Selects internal Band Gap reference voltage. Low: Selects the external `VBG_EXT` reference voltage. |
| ANALOG_OUT-<0:1> | Analogue | Output | AnalogOut of pixel (121,0) and (122,0). |
| THL_OUT<0:1> | Analogue | Output | THLOut of pixel (121,0) and (122,0). |
| | | | |
| VDDLVDS | Analogue | Input | Low Voltage Differential Signalling (LVDS) positive supply, connected to 2.2 V. |
| CSSLVDS | Analogue | Input | LVDS negative supply, connected to 0 V. |
| SUBLVDS | Analogue | Input | LVDS substrate supply, connected to 0 V. |
| SUB | Analogue | Input | Substrate supply, connected to 0 V. |
| VDD | Analogue | Input | Digital positive supply, connected to 2.2 V. |
| VSS | Analogue | Input | Digital negative supply, connected to 0 V. |
| VDDWELL | Analogue | Input | Digital well supply, connected to 0 V. |
| VDDA | Analogue | Input | Analogue positive supply, connected to 2.2 V. |
| VSSA | Analogue | Input | Analogue negative supply, connected to 0 V. |
| VDDAWELL | Analogue | Input | Analogue well supply, connected to 0 V. |

Table 3.1: Timepix in- and output signals, from [67]. CMOS is a unipolar signal type with a high level of 2.2 V for the Timepix chip. The LVDS signal is differential.

### 3.1.2 Pixel logic

Each pixel containing 549 transistors has a size of 55 µm × 55 µm. The logic can be divided into two basic parts. The analogue side contains the pixel pad, test pulse input, charge sensitive preamplifier and discriminator, while the digital side features the Timepix Synchronisation Logic (TSL), 14 bit shift register and overflow control, see Figure 3.1. These components are explained more detailed in [67].

| DAC | Bits | Description | Code |
|---|---|---|---|
| IKrum | 8 | The preamplifier is designed in the Krummenacher scheme for a fast return to zero. The p-Channel Metal-Oxide Semiconductor (PMOS) feedback transistor of this design is controlled by this DAC. | 1111 |
| Disc | 8 | Controls the current for the Fast Discriminator Logic (FDL) and Operational Transconductance Amplifier (OTA). | 1011 |
| Preamp | 8 | Controls the current for the preamplifier | 0111 |
| BuffAnalogA | 8 | Bias control for the unitary gain buffers. | 0011 |
| BuffAnalogB | 8 | Bias control for the unitary gain buffers. | 0100 |
| Hist | 8 | A hysteresis can be generated at the output of the discriminator to avoid glitches. His also reduces the effective threshold of the system, since the gain is improved. | 1001 |
| THL | 10+4 | It sets the threshold voltage of at the discriminator and consist of two parts. The first 10 bits are the THL fine setting, while the last 4 bits are THL coarse. A step in THL coarse is equivalent to 372 THL steps. One THL step changes the threshold about 25 $e^-$. | 0110 |
| Vcas | 8 | This DAC controls a cascode to reduce the input capacitance of the preamplifie, which improves the Signal-To-Noise Ratio (SNR) but reduces the dynamic range of the output coltage. | 1100 |
| FBK | 8 | The Direct Current (DC) output voltage of this DAC controls a node in the preamplifier circuit to enlarge the dynamic range whether the chip is set to measure positive or negative input charge. | 1010 |
| GND | 8 | Controls the ground voltage inside the chip. | 1101 |
| THS | 8 | To minimise the spread of thresholds in the discriminator due to minor differences in the production of each individual pixel, four current sources can be applied to each pixel The output value if these sources is set by this DAC. In each pixel, there are 4 threshold adjustment bits that can select from those current sources. This behaves as if each pixel holds a 4 bit current DAC. | 0001 |
| BiasLVDS | 8 | Sets the bias voltage in the LVDS drivers. | 0010 |
| RefLVDS | 8 | Sets the bias voltage in the LVDS drivers. | 1110 |

Table 3.2: Timepix DACs.

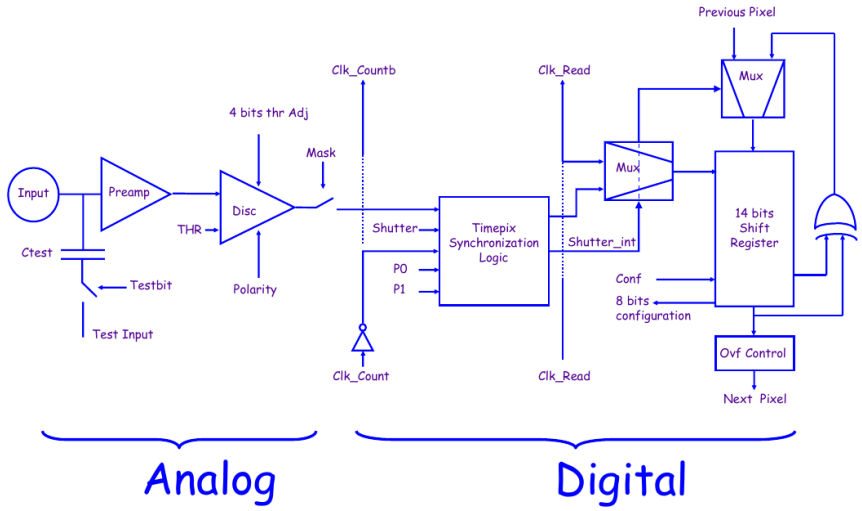



Figure 3.1: Timepix pixel cell block diagram, from [67].

The digital electronics can be tuned by eight current and five voltage DACs (Digital-Analogue Converter), which can be set on the chip. They are listed in Table 3.2. These DACs are set globally for the complete chip in the periphery. Their value can be loaded into the chip by writing to an FSR (Fast Shift Register). It is 256 bits long and also used to serialise the data from the individual pixels. To set the DAC values, only 174 bits are used. Besides the 110 bits for the DACs there are 12 for the Column Test Pulse Register (CTPR), 4 for the `DAC_CODE` signal and 1 for `Sense_DAC` and `Ext_DAC_SEL`, respectively. The exact position of the bits for each value can be found in [67]. The two single bits `Sense_DAC` and `Ext_DAC_SEL` enable or disable special features. When `Sense_DAC` is enabled, the level of the DAC selected by `DAC_CODE` is applied to the analogue `DAC_OUT`. The `Ext_DAC_SEL` overwrites the output of the DAC selected by `DAC_CODE` with the analogue input signal `EXT_DAC`. The selection of DACs by `DAC_CODE` refers to the last column in Table 3.2. To minimise the distortions between neighbouring columns in the test pulse mode, bits in the CTPR can be enabled or disabled. Each bit controls 8 columns spaced by 32 columns. As an example, the lowest bit of CTPR enables the columns 0, 32, 64, 96, 128, 160, 192 and 224 for test pulses.
If a charge moves towards the Timepix surface, a signal is induced in the pixels. The same can be achieved for testing, when a voltage signal with fast falling or rising (depending on the polarity to be tested) edge is put on the `Ctest` capacitor in a pixel, see Figure 3.1. In this case, the global `ENABLE_TPULSE` and the pixel specific `Testbit` have to be enabled. The charge is collected in an integration capacitance of the preamplifier. The output signal is a voltage signal with a fast rising edge. Its Equivalent Noise Charge (ENC) is around $100\,e^-$. The time constant of the falling edge can be adjusted between 90 ns and 140 ns by the `IKrum DAC`. The discriminator compares the voltage signal with the threshold set by the `THL DAC`. The first component of the discriminator circuit is a multiplexer. Depending on the polarity the chip is set to (register positive or negative charge), it can interchange the preamplifier output with the threshold. The output of the discriminator is a digital signal that is high for the time, the preamplifier signal is over threshold. If the `SHUTTER` signal was low, the TSL will perform one of the following operations, depending on the mode, the pixel was programmed to, see Figure 3.2:

- Medipix mode: Within the time the shutter is low, each transition of the discriminator signal from low to high increases the counter by one. This way, the number of arriving charges higher than the threshold during the shutter time is counted.

- Time over threshold (TOT) mode: The number of FCLOCK cycles is counted as long as the discriminator signal is high within the shutter window. The length of the falling edge of the preamplifier depends on the absolute charge collected. By calibrating this number to the known input charge influenced at Ctest, a charge measurement is possible in this mode. If the discriminator signal is high for several intervals within one shutter window, the number of clock cycles is added resulting in an integration of the arriving charge.
- Time of arrival (TOA) mode: In the Medipix chip family, this mode is unique for the Timepix chip. It was particularly requested by the EUDET collaboration to measure the arrival time of charge in order to reconstruct the drift time of charge in a TPC. The FCLOCK cycles are counted from the first rising edge of the discriminator signal until the end of the shutter window. This way, the arrival time can be calculated, when the timing of the closing shutter is know. If there are several rising edges of the discriminator signal within one shutter window, only the first one will have an effect.

  To avoid glitches in the counting logic, both the discriminator signal and the global shutter are synchronised to a reference clock in each pixel. The phase of this reference clock is alternated from column to column with respect to FCLOCK to minimise the digital power coupling [67]. Therefore, the quantisation error of the time measurement can be up to two clock cycles [68].
- 1st hit mode: In this mode, the pixels will only give a binary information whether a pixel was hit during the shutter time or not. The first rising edge increases a counter to one, any further rising edge has no influence.

The rise time of the preamplifier signal is not infinitely short. It depends on the absolute charge of the signal, as can be seen from Figure 3.3. So for different amounts of charges registered at the same time, the measured time in the Time Of Arrival (TOA) mode is different. This effect is called time walk. It can be calibrated by using the input charge from Ctest and could be corrected for, if the amount of charge in the pixel would be known as well. With the successor chip, Timepix3 [73], this will be possible.

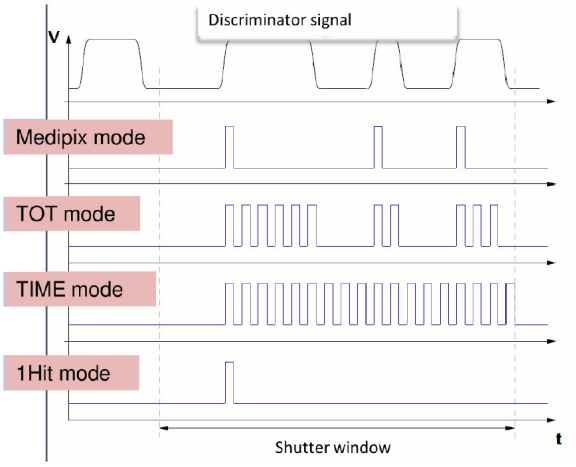



Figure 3.2: Different operation modes of the Timepix chip, from [74].

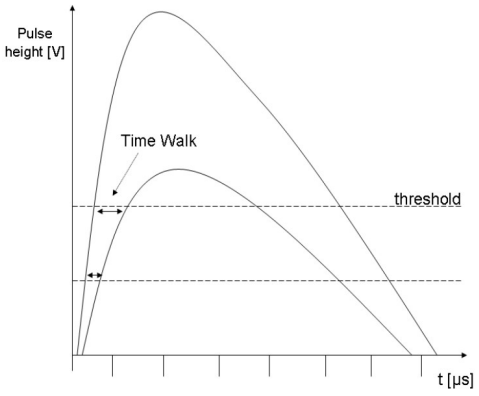



Figure 3.3: Time walk effect, from [75].

Depending on the synchronisation between the hit and the clock, the number of Time Over Threshold (TOT) or TOA counts can vary for the same charge signal by one or two clock cycle, respectively. Additionally, the clock is buffered in each pixel and propagated from the periphery through each column.

This adds a delay of about 200 ps per row. The last pixel receives the clock approximately 50 ns after the pixel closest to the periphery. Therefore, the clock has to be applied to the chip before the global SHUTTER is opened. The counter itself is realised as a 14 bit pseudo-random counter with an overflow logic that stops at 11810 clock cycles. Before counting, a reset signal or read out sequence is necessary to not lock the counter in a state where it cannot start counting, see [67]. For readout, the counter acts as a 14 bit shift register connected to the next and previous pixel. That way, a 3584 bit register is generated by each column. The value each pixel holds has to be transformed with a Lookup Table (LUT) to the real value of counted clock cycles.
As mentioned before, each pixel can be programmed to one of the four counting modes. The 14 bit register is also used for this purpose as a 8 bit configuration register. Two bits called P0 and P1 select the mode of the pixel, see Table 3.3. Additionally there is a mask bit Mask to prevent the pixel from counting and a test bit Test bit to activate the input capacitance for test pulses, see Figure 3.1. The four other bits Thr Bit 0 - Thr Bit 3 activate the current sources controlled by the THS DAC (see Table 3.2) to compensate for pixel-to-pixel threshold variations. The complete list of bits and how they fit into the 14 bit register is shown in Table 3.4.

| Mask | P1 | P0 | Pixel Mode |
|---|---|---|---|
| 0 | X | X | Masked |
| 1 | 0 | 0 | Medipix |
| 1 | 0 | 1 | TOT |
| 1 | 1 | 1 | 1st hit |
| 1 | 1 | 1 | TOA |

Table 3.3: Pixel configuration modes, from [67].

| b0 | b1 | b2 | b3 | b4 | b5 | b6 | b7 | b8 | b9 | b10 | b11 | b12 | b13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| not used | not used | not used | not used | not used | not used | P1 | Mask | Thr Bit 0 | P0 | Thr Bit 2 | Thr Bit 3 | Thr Bit 1 | Test bit |

Table 3.4: Pixel configuration register, from [67].

### 3.1.3 Timepix operations

The Timepix chip works as an imaging detector, which is set to different states one after the other, required to record data. There is one state to configure the chip, another to take the data and another one to read it out. The information collected from the pixels in one such cycle is called a frame. Those states are induced by control signals. The two main ones are M0 and M1, by which four distinct states can be selected: The Read/Write FSR, the Set Matrix, the Counting and the Readout Matrix state. Additionally, there is the TRESET signal for a reset of the chip and P_S to select the readout method. In a typical setup, the method of readout is defined by the design of the readout system and the P_S pin of the chip is fixed to either 2.2 V (VDD) or 0 V (VSS or GND) to select either the parallel or the serial readout method. Regardless of the status of all other signals, a low level of TRESET causes a reset of the chip. The control signals set the chip in the state of a certain operation. The operation, however, is executed only if the clock FCLOCK is fed through the chip, ENABLE_IN is on the correct level and, in case of the

counting state, the SHUTTER is low. For that reason, the signals M0, M1 and TRESET, together with the POLARTIY signal, are slow control signals. FCLOCK, ENABLE, DATA and with some restrictions SHUTTER need to be fast, as they directly trigger an operation at the chip and have to be set exactly at a desired time as precise as one FLCOCK cycle. Table 3.5 summarises the operations, while the exact timing of all signals can be found in [67] and Section 3.1.4.

| M0 | M1 | ENABLE_IN | SHUTTER | TRESET | P_S | In-/Output | FCLOCK num (per chip) | Operation |
|---|---|---|---|---|---|---|---|---|
| X | X | X | X | 0 | X | I | X | General reset of chip |
| 1 | 1 | X | 0 | 1 | X | X | X | Counting |
| 0 | 0 | 0 | 1 | 1 | 0 | I/O | 917768 | Serial readout matrix (slow reset matrix) |
| 0 | 0 | 0 | 1 | 1 | 1 | I/O | 28688 | Parallel readout matrix (fast reset matrix) |
| 0 | 1 | 0 | 1 | 1 | X | I | 917768 | Set matrix |
| 1 | 0 | 0 | 1 | 1 | X | I/O | 264 | Write/Read FSR (DACs and CTPR) |

Table 3.5: Timepix I/O operation modes, from [67].

### 3.1.4 Data structure

To write to and read from the chip, the structure of the individual bits in the data stream has to be known as well as the timing of the different control signals. In the chip, the binary data of the DATA_IN LVDS signal is sampled with FCLOCK. The output data DATA_OUT is produced in the chip at the falling edge of FCLOCK in the serial readout mode. As the readout system designed in the scope of this thesis only uses the serial data port of the Timepix chip, the parallel mode will not be discussed here. The Timepix chip is designed to be daisy chained, which means that several chips can be connected to each other. Then, they are read out serially. More precisely, DATA_OUT of one chip is connected to DATA_IN of the next chip, FCLOCK_OUT to FLCOCK_IN and ENABLE_OUT to ENABLE_IN. All other signals have to be provided to each individual chip. The ENABLE signal plays an important role in this case, as it enables each chip to pick its data out of the stream or push it into the stream.
If N chips are connected to each other, the first chip of the row receives N times the amount of data and clock cycles as for a single chip and forwards all FCLOCK cycles to the whole chain. When the ENABLE_IN signal is pulled to a low potential at the input of the first chip by the readout, it can pick up the data from DATA_IN or fill the output stream at DATA_OUT. The ENABLE_OUT signal of the first chip, however, stays high until the first chip has counted as many FCLOCK cycles as need for the operation. During this time, the second chip receives an ENABLE_IN high signal and the data is just forwarded to the DATA_OUT ports. Hence, this data is fed through the whole chain to DATA_OUT of chip N and back to the readout system. When the first chip has received or transmitted all data, ENABLE_IN goes low at its output, which is the input of the second chip. It starts to pick up its own data or fill the stream, while it keeps ENABLE_OUT high until completion. This way, all chips pick up their data from the stream or fill it until at the very end, the ENABLE_OUT signal at chip N goes low.

**Read/Write FSR** The most simple operation, apart from a reset, is to write to the FSR, which by design implies an automatic read-out of the Chip ID. Before this operation starts, the control signals

have to be assigned correctly to set the chip into the Write/Read FSR state: M0 has to be high and M1 low. Exactly at the beginning of the data stream, ENABLE_IN has to go to low. As mentioned before, the FSR has 256 bits. The data stream to the chip hence contains 256 bits, each bit one FCLOCK cycle long. In addition a preload of 8 clock cycles has to be sent. FCLOCK has to fulfil 264 cycles in total and afterwards, the DAC, CTPR, DAC_CODE, Sense_DAC and Ext_DAC_SEL values are latched into parallel registers and set in the chip periphery and ENABLE_OUT goes low. At a defined position in the stream of DATA_OUT, the bits of the chip ID come out of the chip. If several chips are connected to each other, the output also contains the preload and 256 bits for each of the FSRs of the following chips. The 8 bit preload only has to be set once for the first.

**Set matrix** As shown in Table 3.5, it takes 917768 FCLOCK cycles or data bits to set the matrix of a single chip. This number arises from the 256 × 256 pixels of the matrix and the 14 bits each pixel configuration register contains, see Table 3.4. This adds up to 917504 bits of information to set the register in each pixel. In order to change one bit of the matrix, the complete process has to be performed. Additionally there are 8 bits preload at the beginning and 256 bits postload at the end of the data stream. At the beginning of the sequence, M0 and M1 have to be set to logic low and high, respectively. When ENABLE_IN goes low, DATA_IN and FCLOCK start. In a chain of several chips, the ENABLE signals are controlled the same way as in the Write/Read FSR operation. The data stream has to contain pre- and postload for every chip. The data structure in the matrix data stream to set the configuration bits is as follows:

- The first bit is the Most Significant Bit (MSB) of the 14 bit pixel configuration register of the right bottom pixel.
- The second bit is the MSB of the 14 bit pixel configuration register of the second to right bottom pixel...
- The 256th bit is the MSB of the 14 bit pixel configuration register of the left bottom pixel.
- The 257th bit is second MSB of the 14 bit pixel configuration register of the right bottom pixel...
- The 3329th bit is the Least Significant Bit (LSB) of the 14 bit pixel configuration register of the right bottom pixel, which completes the information for this pixel...
- The 3584th bit is the LSB of the 14 bit pixel configuration register of the left bottom pixel, which completes the information for this pixel and the bottom row.
- The 3585th bit is the MSB of the 14 bit pixel configuration register of the right pixel in the second lowest row...
- The 917504th bit is the LSB of the 14 bit pixel configuration register of the left pixel in the top row, which completes the information for this pixel, the top pixel row and hence the complete chip.

**Serial readout matrix** This operation follows the same data structure as setting the matrix, just the control signals have to be assigned differently, as shown in Table 3.5. 917768 (8+256·256·14+256) FCLOCK cycles have to be sent to the chip together with ENABLE_IN going low. The information of the pseudo-random counters in each pixel comes out of the chip as a binary data stream at DATA_OUT following the same structure as just explained for setting the matrix. The counter values have to be

reconstructed by the readout system or Data Acquisition (DAQ) software. It has to be mentioned that only after the 3329th bit, the complete information of the first pixel has arrived in the readout system, which then can analyse whether the pseudo-random number of the pixel counter refers to a non-zero entry or not. After 917768 FCLOCK cycles ENABLE_OUT will go low, such that a second chip, if present in the row, starts to fill the data stream.

The readout method provided by the Timepix chip does not allow for a fast readout, in case only a few pixels on the chip were hit. In all cases, the complete matrix has to be read out. The maximum FCLOCK frequency is in the order of 100 MHz to 150 MHz. For a frequency of 100 MHz, it takes about 9.2 ms to read out the 917768 bits of the complete pixel matrix in serial mode. As always all bits have to be read out, the maximum frame rate at 100 MHz is about 100 Hz. If the chip is read out in parallel mode, 32 output data lines of CMOS signals have to be managed. These signals cannot be transmitted over long distances. The maximum frame rate would increase to about 3.2 kHz at 100 MHz clock frequency in this case. If N chips are connected to a chain, the maximum frame rate decreases by a factor N in the serial mode.

### 3.1.5 Calibration

In Section 3.1.2, the THS DAC to regulate the current source for the four threshold adjustment bits in each pixel has been mentioned. The first step to calibrate a Timepix chip is finding an optimal value for the THS DAC. There are algorithms implemented in the control software of the chip to find the optimum value. After this has been done, the four threshold adjustment bits for each pixel can be set in the pixel matrix, such that the minor production differences of the discriminators are compensated and all pixels have a similar response characteristic to the global THL DAC. These procedures only use the noise level in each pixel. Before the threshold equalisation, the threshold variation of the pixels is about 240 $e^-$ and can be decreased to 35 $e^-$. The minimal detectable charge decreases from about 1600 $e^-$ to about 650 $e^-$.

It has already been mentioned in Section 3.1.2 that there is an input capacitance Ctest in the analogue part, parallel to the input pad of each pixel. The capacitance is 8 fF and can be accessed with the analogue input pad TEST_IN. To activate the test pulses in general, ENABLE_TPULSE has to be active. To activate the pixel row for test pulses, the appropriate bit in the CTPR has to be active. Finally, to connect Ctest in the individual pixel the Test_bit has to be set. The TEST_IN pad has to be connected to a voltage pulse generator. A rising edge of the input voltage refers to a positive charge from the pixel, whereas a falling edge refers to a negative charge. As the capacitance of Ctest is 8 fF, a voltage edge of $\Delta V$ is equivalent to an input charge *Qtest* of

$$Qtest[e^-] = \Delta V[V] \cdot 50000 \tag{3.1}$$

Due to internal buffers, it is possible to pulse several pixels simultaneously, which speeds up the calibration process. The input charge simulates an event at the charge sensitive pixel pad, but with a known amount of charge. Hence, the number of TOT or TOA counts can be calibrated to the input charge. The results are a TOT and time walk calibration. In addition, a so called S-Curve scan calibrates the THL DAC value into number of electrons and gives access to the ENC. There are algorithms explained in [68], [76], [75] and [77] to perform theses operations. They are implemented in the DAQ software and call sequences of the simple Timepix operations mentioned above.

### 3.1.6 Powering

The chip is powered by three different voltage lines, as can be seen from Table 3.1, each at typically 2.2 V. The power consumption of an individual pixel is 6.5 µW in the analogue part and 7 µW in the digital part at a FCLOCK frequency of 80 MHz and when the pixel is counting. When a pixel is not hit, the digital power consumption is negligible. The total current consumption is about 200 mA in the analogue part and only a few mA in the digital part when no pixel is counting. The distribution of the FCLOCK signal to the pixels which are counting needs about 210 mA for a short time. For a single chip, the fluctuations in power consumption is not critical. If several chips are connected to a chain, the consumption multiplies by the number of chips. In this case, the supply voltage drops and can reach a critical value at which the chips cannot be operated reliably. A detailed study about the powering of multi-chip systems can be found in [78].

## 3.2 The InGrid

The Timepix chip, or pixel ASICs in general, cannot directly be used as a detector for charged particles or photons. The threshold of a pixel is in the order of 500 $e^-$. Signals of that strength can only be achieved by an amplification of the original event. For that reason, the Medipix family provides pads that can be bump bonded to silicon sensors. In such a semiconductor, charge is set free by ionisation of a charged particle or photon entering the material. When a bias voltage is applied to a semiconductor diode, a single ionisation leads to a signal strong enough to exceed the threshold. More information about silicon detectors in particle physics can be found in [79] or [80]. Another method to achieve an electric signal that exceeds the threshold are the gaseous detectors mentioned in Section 2.4. In this case, the bump bond pad on the pixel surface is used as one of the two electrodes for an electric field to attract charge to the pixels. When the pad is an anode, electrons are collected in the pixels. Moving charge in the weighting field of the pixel induces a signal in the pixel electronics and can, if strong enough, exceed the threshold. Again, in most of the cases, the primary ionisation signal is not big enough, so the charge has to be amplified.
An InGrid detector is a combination of a Micromegas (see Section 2.4.3) and a pixel readout. The gas amplification takes place directly above the chip in the gap between the grid and the pixels, which are used as anode. A bare Timepix chip is post-processed by photolithography to build up a protection layer against sparks and the grid supported by insulating pillars. The processes to build an InGrid will be explained in Section 3.2.3. The holes of the grid can be precisely aligned to the pixels by this technology that was developed over several years, see Section 3.2.2. To be operated as a Micromegas, the grid is set to a negative potential with respect to the chip to form the amplification gap with a high electric field. Above the grid, a second weak electric field attracts the electrons to the grid (drift region). When an electron from the primary ionisation in that drift region enters a hole of the grid, it gains energy in the strong field of the amplification gap and can itself cause ionisation. Charge amplification takes place and the avalanche of secondary electrons induces a signal strong enough to cross the threshold in the pixel underneath the hole. An SEM image of an InGrid is shown in Figure 3.4. The height of the pillars was designed such that the charge cloud of the secondary electrons does not spread to the neighbouring pixel. In a typical gas with $D_T = O(100)\ \mu m/\sqrt{cm}$, the electron cloud has a vertical size of less than 10 µm when it reaches the protection layer 50 µm underneath the hole, compared to a pixel pitch of 55 µm. Only if the amplification becomes large, the spread of the charge on the protection layer can induce a signal on the neighbouring pixels. Before the fabrication of an InGrid is explained in Section 3.2.3, a motivation why those devices can be helpful and a short summary of their history will be given. Therefore, the arguments published in [81] are picked up.

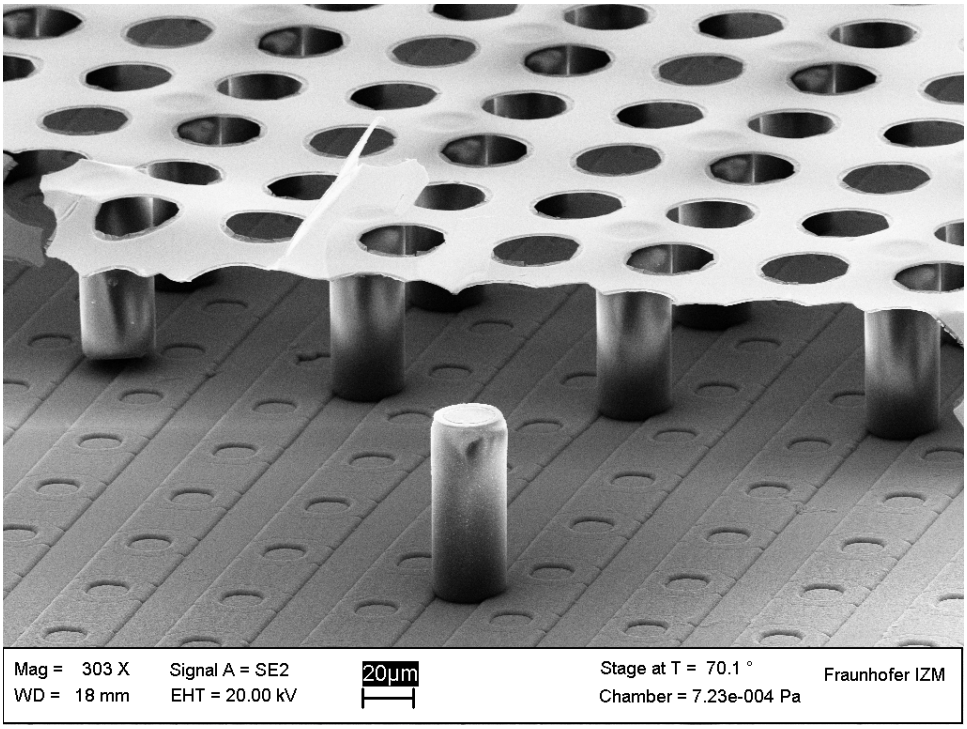



Figure 3.4: SEM image of an InGrid with partly removed grid made by the IZM Berlin. The height of a pillar is 50 µm.

### 3.2.1 Motivation

In Section 2.4.3, we have seen that the invention of MPGDs led to a revolution in the field of gaseous detectors in particles physics. The spatial resolution could be increased from several 100 µm to the order of 10 µm, as the dimensions of the amplification structure also decreased by a factor 10-100. The hole-to-hole distance in a Micromegas, for example is in the order of 10 µm, while the distance between wires in a MWPC is in the order of 1 mm. As readout, traditionally segmented anodes with pads or strips are used. Due to the etching technology and the amount of electronics needed to process the signals, the smallest size these structures can have is about 1 mm. Still, a spatial resolution of about 10 µm is achievable, despite the resolution of a 1 mm wide pad is given by

$$\frac{1\,\text{mm}}{\sqrt{12}} = 0.29\,\text{mm}. \tag{3.2}$$

This is only possible, if the induced charge signal is spread over several pads and each of the analogue pulses on the pads is analysed. By measuring properties like the height of the signals, additional information about the position of the primary charge causing the gas amplification can be gained. In [82], where this method was used for the first time, a spatial resolution of about 200 µm is reported for a MWPC with strips whose centres lie 8 mm apart. This improvement to measure the position is called `centre-of-gravity method` [83], [84]. For a Micromegas, the pad plane can be covered by a high resistive layer of several µm thickness. The weighting fields of adjacent pads overlap, hence the charge of the avalanche from one primary electron induces a signal on several pads. Additionally, the resistive layer protects the pads and electronics from sparks.
A pad of 1 mm$^2$ is covered by some tens of holes in the grid. If several primary electrons enter these

holes, the avalanche signal on the underlying pad becomes larger. However, as the gas amplification is a statistical process, the number of electrons cannot be reconstructed by the signal. This type of detector has no single electron detection capability. The spatial structure of primary electrons, which is intrinsically still present after the amplification if only one electron enters a hole in the grid, is lost. $\delta$ electrons, for example, cannot be resolved and only leave more charge on the pad. Moreover, if the centre-of-gravity method is applied, the calculated position is the mean position of all electrons, which e.g. in presence of a $\delta$ electron reduces the detector resolution.
For an InGrid detector, the readout cell size is matched to the granularity of the grid. To manage the matching, an ASIC has to be used in order to achieve the µm pitch for the anode segments. The pixels of the chip are aligned to the holes of the grid, such that every pixel monitors one hole. The amplification gap height is 50 µm. It has been optimised together with other parameters like the hole size and shape [44].
Due to the fine granularity, it can be applied as a planar detector with a thin drift region to achieve a high spatial resolution. In this case, the limiting factor is the diffusion constant $D_T$ of the gas. A typical drift gap for such a detector is about 1-10 mm. In such a thin planar tracking detector, a high energetic traversing particle perpendicular the chip surface ionises the gas in a single interaction and creates $O(10)$ primary electrons that drift towards the amplification region. In a gas with $D_T = O(100)\,\mu m/\sqrt{cm}$ the electron cloud would have a size $O(30)$ µm. A single point resolution $O(10)$ µm is achievable with such a type of detector.
As the InGrid has among others the unique feature to resolve $\delta$ electrons on charged particle tracks, it is a candidate for the readout of a TPC. Due to the fine granularity, the double-track resolution should be better than for a pad-based readout and the resolution should not depend on the angle of the track, as it does for rectangular pads. As the InGrid is sensitive to single electrons, the energy loss dE/dx of a particle is directly accessible through counting the hit pixel density along the reconstructed track.
The imaging capability also helps in case of X-ray detection. With the InGrid, it is possible to distinguish between photons, minimum ionising particles and alpha particles by analysing the pattern of hit pixels on the chip, the ionisation density and the energy deposition.

### 3.2.2 History

The idea to combine an MPGD with an ASIC was first discussed in two publications the years 2003/2004. Bellanzzini and Spandre [85] had a setup of a GEM with 60 µm hole-to-hole distance and an ASIC with 200 µm pixel pitch. They noted: "*The real challenge with this class of detectors is the design of the read-out system which should not spoil the intrinsic performance of the device.*" In the other publication[86], results from the combination of the Medipix2 chip with a triple GEM stack or a Micromegas are reported. The idea to build an InGrid, at that time called TimePixGrid was announced for the first time. The Timepix chip, however, was not available at that time, see Section 3.1 and the technology to build a monolithic integrated Micromegas still had to be developed.
In 2005, the single electron detection efficiency of the Medipix Micromegas detector was measured to be better than 90 % [70]. In the dataset of tracks from cosmic particles, also $\delta$ electrons could be identified. The same year, first tests of a technique to build a Micromegas grid on top of a silicon wafer were undertaken [87]. In a Helium/Isobutane as well as in an Argon/Isobutane 80/20 gas mixture, charge amplification could be monitored, when the grid was put to 400 V. A cathode 10 mm above the grid was put on 1400 V and the structure was irradiated with an $Fe^{55}$ source. The spectrum showed a clear separation of the photo- and escape peak. In a following, more detailed study [44], different hole sizes, gap heights and grid thickness were tested.
Due to the fact that the charge amplification takes place in a high electric field directly on top of the

readout, the anode has to be protected from sparks. Especially in case of an ASIC as anode, such a discharge destroys several pixels or even the complete chip. The unprotected Medipix chips used for the first tests did not survive very long in their test environment. The idea to build a protection layer of amorphous silicon, following the technique in [88] was proposed in 2006 [89].
Finally, in 2007, the first Timepix chips with a protection layer and an integrated Micromegas were built and tested [90]. The gas gain and detection efficiency was proven to be uniform over the whole sensitive surface. First results on the ion backflow fraction are also presented in this publication. To increase the active area, an array of $2 \times 4$ InGrids was proposed in [91] as a first step towards a larger system and to be tested at the Linear Collider TPC (LCTPC) Large Prototype (LP) at the Deutsches Elektronen-Synchrotron (DESY), see Section 3.8
The InGrid was tested in a test beam at PS/T9 at CERN in 2008 [92]. Some new devices using the same technology as for the InGrid production, like a GEMgrid or Twingrid [92], were also produced and tested. A new protection layer of silicon-rich nitride SiRN (SiProt) was introduced and showed a better performance than the amorphous silicon.
After the PhD thesis [44] of Maximilien Chefdeville, the development of the technology to build an InGrid and the optimum parameters were concluded. The study of physics properties like the gas amplification, single electron detection efficiency, charge spread and energy resolution were investigated and later continued in [74] and [93] supported by simulations [94]. In [74], beside other results, it was found out that the SiProt layer charges up due to the avalanches and hence reduces the rate capability of InGrid detectors. The $2 \times 4$ InGrid Detector, called Octopuce, proposed earlier was constructed and tested. A detailed study of the spark protection and the Gas On Slimmed Silicon Pixel (GOSSIP) was conducted in [93].
Meanwhile, the InGrid is used as detector in several experiments and R&D projects. The applications will be discussed in Section 3.2.5.

### 3.2.3 Production

The first InGrid were built in 2007 on a single chip level at MESA+ at the University of Twente. At most nine chips could be processed in the clean room in one step, which took a long time [96]. The handling of a complete 8 inch wafer with 107 chips was not possible at that institute. The Fraunhofer IZM in Berlin could offer all machinery needed, apart from one for the deposition of silicon nitride for the protection layer. Meanwhile, also this step is possible in Berlin. The production was transferred to that institute in 2011. Still with the new machinery, several test runs were necessary to achieve InGrids of the same quality as before in Twente [97], [98]. The runs are called IZM-N, starting with IZM-1. The last production was IZM-6. To form an InGrid on top of a Timepix wafer, several steps are necessary. For all of them, the alignment of wafer and masks has to be assured. In Figure 3.5, the most important ones are shown. They are:

1 Cleaning of the bare wafer to cast off dust on the surface. The early production runs, especially IZM-2, suffered from cracks and defects in the protection layer due to a badly grown protection layer and surface pollutions.

2 Deposition of the silicon-rich nitride layer to protect the pixel bump bond pads from sparks within the amplification region. SiRN is lately used, which is a high resistive material. Depending on the application, the thickness of this layer is 4 µm or 8 µm. To keep the bonding pads on the periphery side of the chip free from SiRN, they are covered with a polyimide, which is removed later.

3 To build the 50 µm amplification gap, a negative photoresist is deposited on the wafer. SU-8 has been chosen.

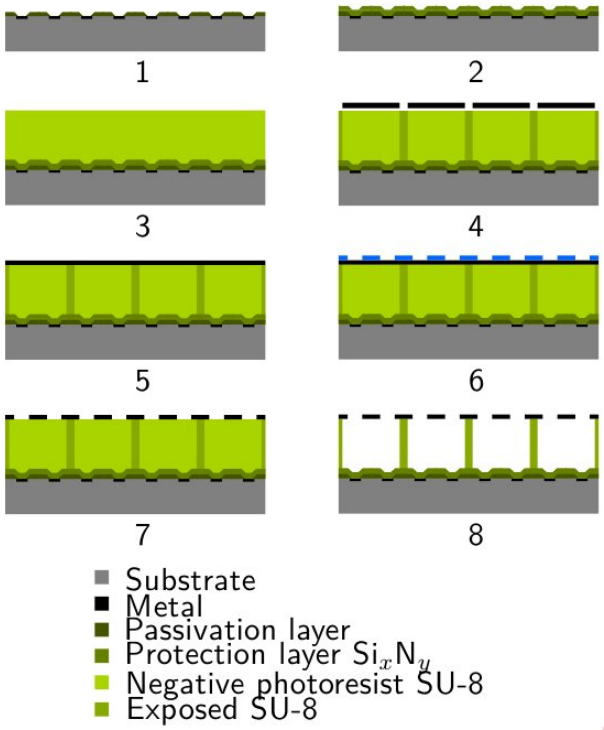



Figure 3.5: The eight main steps for the wafer scale the InGrid production, from [95].

4 At the positions where the pillars should support the grid, the SU-8 is exposed with UV light. A mask to cover the rest of the surface needs to be put in place beforehand.

5 The most critical step is the sputtering of the aluminium layer for the grid, as this heats up the SU-8 and can also expose the complete surface. The grid could be cross-linked to a thin layer of exposed SU-8 underneath, which locks the holes. To avoid that, the built-up of an 1 µm layer is done in several runs with intermediate cooling breaks. This procedure consumes a lot of time and will be avoided in the future with a new machine, which can cool the wafers in the sputtering process.

6 On top of the still uniform aluminium layer another layer of photoresist is applied and exposed such that the positions were the holes in the grid should be can be washed out.

7 The exposed photoresist of the previous step serves as a mask to protect the aluminium from etching. Only at the positions for the grid holes, the aluminium is removed.

8 In order to not destroy the grid, the wafer is diced into individual chips before the final cleaning steps. Afterwards, a special oxygen cleaning removes cross-linked SU-8 underneath the grid.

The IZM-3 production with one wafer was the first completely successful run with a good grid and protection layer quality, see [98] p. 47ff. The SiProt layer on these InGrids is 8 µm thick.
Unfortunately, the following production planned to be the first mass production with four wafers failed. Two wafers (one with 4 µm and one with 8 µm SiProt) broke and the other two (4 µm and 8 µm SiProt) were overbaked during the aluminium deposition, such that the SU-8 was completely developed and cross-linked. Still, these wafers could be reused if the complete structure was removed and the wafers were not already diced.

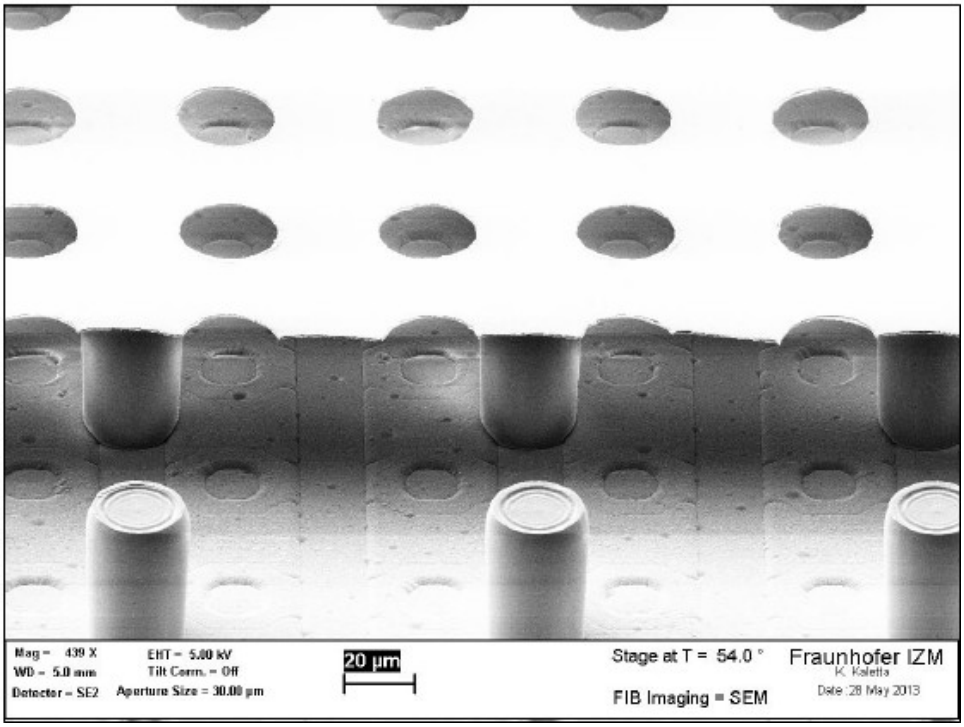
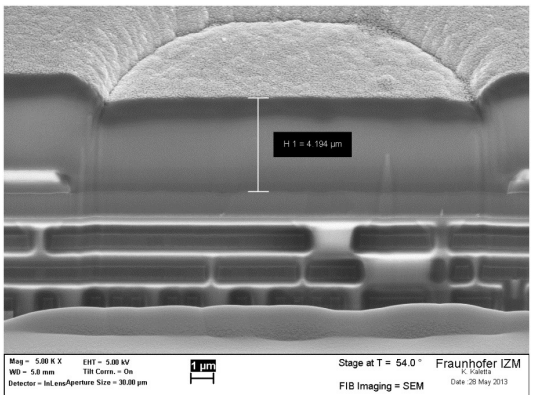
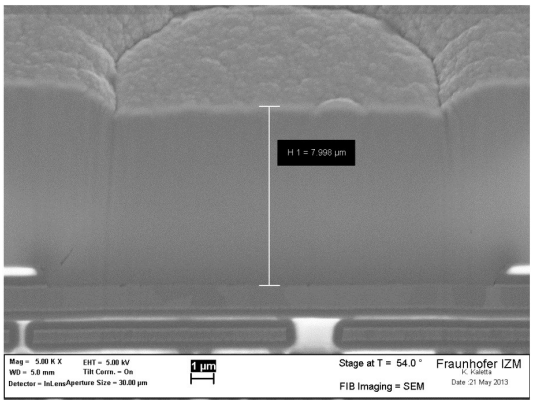



Figure 3.6: SEM image of an IZM-5 InGrid with partly removed grid. Some defects in the SiProt layer are visible due to dust on the wafer surface before the silicon nitride was deposited, from [99].

The next production, IZM-5 included one wafer with 4 µm and one wafer with 8 µm silicon protection layer. Figure 3.7 shows SEM images of a cut through the processed wafer and especially the protection layer. For the 4 µm layer (Figure 3.7a) as well as for the 8 µm layer (Figure 3.7b), small vertical cracks are visible above the pixel pad. Still a chip from this run with 8 µm SiProt survived the operation for several months in an Argon/Isobutane 97.7/2.3 gas mixture with 290 V grid voltage.
The following production, IZM-6 (three wafers with each 8 µm SiProt) was especially done for the 96 chip module project described in this thesis. As the number of chips needed by the project was extended to 160, most of the chips with an acceptable quality had to be used to build the modules. The first chip bonded on a single chip carrier was operated for several months in Argon/Isobutane 97.7/2.3 with a grid voltage of 300 V and is still operational. The SiProt layer could be produced without difficulties and is of good quality. The knowledge of the previous productions has been taken into account to avoid cracks or SU-8 cross linking. The grids themselves however, are not as plain as for previous productions. This is a result of an extended treatment with chemicals in the cleaning process to resolve residues from slightly overbaked SU-8. During the construction of octoboards from the IZM-6 grids, electrical shorts inside the Timepix chips have been discovered. The origin of those is still unknown. Moreover, scratches on the bonding pads have been observed on several chips, see Section 4.3.3.
The InGrid production has become a standard procedure since IZM-5 and mass production on wafer scale is available with a yield better than 80 %. A last step for a complete post processing is to test the new machine for the deposition of the SiProt layer at IZM in Berlin. In addition, a new machine for aluminium sputtering is available. It includes a wafer cooling. For the InGrid production, this can speed up the process and result in a better grid quality. One wafer of InGrids completely processed in Berlin for the first time will be the IZM-7 production. New structures are still a prospect of ongoing development and there are some ideas [100]. One of them is the all-ceramic grid, depicted in Figure 3.8. The applic-




(a) SEM image of a cut through an IZM-5 InGrid with 4 µm SiProt layer.




(b) SEM image of a cut through an IZM-5 InGrid with 8 µm SiProt layer.

Figure 3.7: SEM images of a cut through IZM-5 InGrids to investigate the SiProt layer thickness and quality. Some thin inhomogeneities above the pixel sensitive area are still present in the silicon layer, from [99].

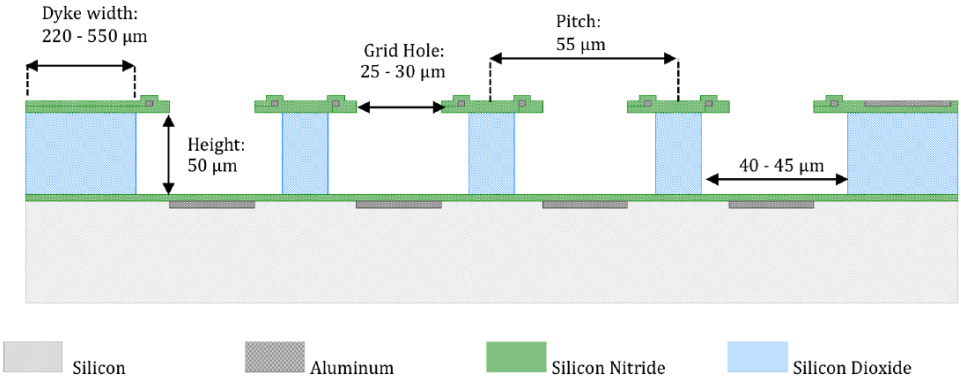



Figure 3.8: Schematic view of an all-ceramic grid, from [100].

ation of SiRN on the anode as well as on the grid is an advantage of the design. The discharge strength is reduced, as the high resistivity prevents the charge on the grid to completely discharge through the spark. The capacity of the detector is also reduced, which decreases the detectors intrinsic noise.

### 3.2.4 Advantages and disadvantages

As mentioned in the previous section, the technology to build InGrids has been established. Apart from the application in a TPC presented in this thesis, the device found application in several fields of physics over the last years. Before a short excerpt of them will be presented, some of the features given by the design of the InGrid are summarised. It will be outlined that each has advantages as well as disadvantages.

The need of an ASIC as anode makes the detector expensive and only as large, as the chip itself is. The compact electronics comprised in the pixel and periphery, however, allows for a direct digitisation of the analogue charge signals with an extremely high channel density, which improves the spatial resolution and allows for single electron detection. This requires a larger amount of power, resulting in a production of heat towards the gas volume, what is not desired. A cooling mechanism hence has to

be implemented on the carrier structure. Due to the small size and thin structures, handling is a difficult task if one does not want to destroy the grid. Large arrays are difficult to build and cannot cover 100 % of the area, as the chip has to be bonded to the carrier board. Hence, an insensitive area cannot be avoided. At the edges or gaps between chips, field distortions can deteriorate the detector performance. As the chip is a gaseous detector, the converter material is exchangeable and free of ageing effects. The InGrid can be combined with other charge amplifying structures or a gating grid to reduce the ion backflow. But as for all gaseous detectors, sparks can harm the chip. The SiProt layer has shown to solve this problem in a reliable way, but reduces the rate capability. For physics measurements with the device, the high channel density with 3D imaging capabilities in combination with a high single electron detection efficiency opens new prospects for example for the detection of recoils from Weakly Interacting Massive Particles (WIMP) interactions, short tracks from a double $\beta$ decay, $\delta$ electrons on tracks or direct dE/dx measurements by cluster density counting. So all technological aspects of the InGrid have their advantages and disadvantages. The goal of the projects presented is always to use the new possibilities for physics measurements by keeping the negative aspects to a minimum. Also this thesis has, besides other aspects, to show that despite the handling of the chips is difficult, the constructing a large area InGrid detector is possible and allows to improve the measurements of physics properties.

### 3.2.5 Applications

The InGrid was proposed in 2009 as an option for an upgrade of the ATLAS inner tracker under the name GOSSIP [101], but the project was finally stopped. Therein it should have been used as the readout of a thin planar detector aimed at high spatial resolution to register traversing particles. Even on a short drift distance of 1 mm, the capability to detect short 3D tracks and not only a 2D hit is a clear advantage to the layers of silicon detectors currently used in the inner tracker. Disadvantages like the limited rate capability, breakdown due to discharges and ageing effects due to the particular gas in combination with too slow advancement of the technology lead to a suspension of the project [98].
In the field of WIMP dark matter searches, an application of the InGrid within the DARWIN project is studied. The goal is to use the InGrid as a readout of a dual-phase noble liquid TPC. The feasibility study has been carried out in 2011 [102], [103]. It has been shown that the application in a pure Argon gas and especially at −180 °C in the ArDM cryostat is very demanding for the protection layer. Due to different thermal expansion coefficients, the grid did not withstand such low temperatures and peeled off. The test in pure Xenon is still to be done. For that reason, a dual-phase Xenon TPC will be built at NIKHEF. To increase the stability of the grid, new geometries for the support structure underneath are studied [104].
At the University of Bonn, an InGrid-based detector for the detection of low energy X-rays has been developed [105]. The project was supported by studies of the field distortion and energy resolution in different Argon/Isobutane gas mixtures [106] and a background reduction by analysing the signal from the grid [107]. Due to the high granularity, it is possible to distinguish between MIPs, alpha particles and photons by the shape of the event. The detector demonstrated to reduce the background to a low rate and is capable to detect X-rays down to 277 eV [108]. It is successfully operated at the CERN Axion Solar Telescope (CAST) experiment since the 2014 data taking run.
Other feasibility studies demonstrated the possibility to measure photon polarisation [109], the general capabilities to detect photons [110] and the application in tumour proton therapy [111]. To summarise, the InGrid device is used for a wide variety of utilisations not only in the field of particle physics. Still, the full applicability in all these fields has to be proven and some advancements in the design for the different needs have to be done in the production.

## 3.3 The Field Programmable Gate Array

The Timepix readout system was developed for two different sets of hardware: The SRS and the Xilinx ML605 evaluation board. For both, an FPGA is the key component that controls the system. An FPGA [112] is a programmable electronic device realised as an integrated circuit, in which every digital logic can be implemented. As its name suggests, it consists of a gate array, where the interconnections can be modified "in the field", i.e. without reassembling the device. This guarantees modification and development of the logical functionality of the device. An FPGA consists of many Configurable Logic Blocks (CLBs), interconnects, connection blocks and I/O pins to connect to the outside world. The components are placed in a two dimensional array as can be seen in Fig. 3.9.

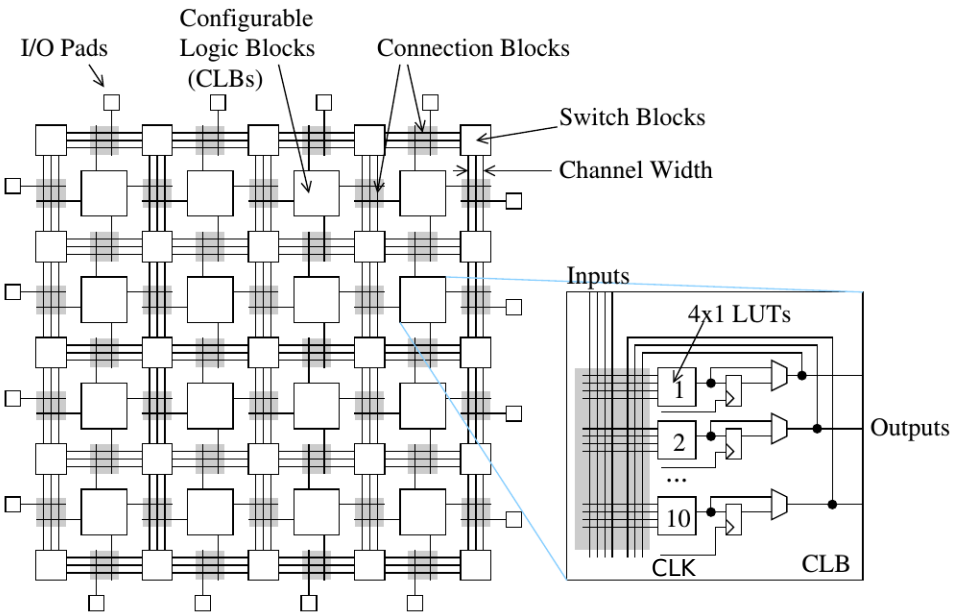



Figure 3.9: Simplified schematic view of the components inside an FPGA, from [113].

To understand the functionality of an FPGA, the most important components are listed below. In a real FPGA they would not be uniformly distributed but are organised in blocks that can fulfil more complex operations.

- The interconnects or wires are short signal lines that connect adjacent components inside the FPGA with each other. There are dedicated wires for signals that need to be transmitted on long distances, as for example a global clock signal.
- The I/O pins or I/O pads can be used to connect the FPGA to the outside world. However, only digital information is available at these pins. They can be configured e.g. to accept or transmit single ended CMOS level signals (2.5 V for a logic 1, 0.0 V for a logic 0) or a pair of pins can be used for LVDS signals.
- The connection blocks and switch blocks are used to connect different wires such that complex signal paths are generated to connect components not directly side by side.
- The CLBs hold the main logic of the FPGA. In the enlarged part of Fig. 3.9, they consist of a LUT with 4 inputs and one output connected to a Flip-Flop (FF), which is driven by a clock signal. The

LUT is used to perform logic operations as for example a simple “AND” operation, the FF can be used to store the output or synchronise it with the clock signal.

- Besides these simple components modern FPGAs hold a lot of dedicated components as for example internal memory, DDR memory controllers, clock multipliers or dividers, Phase Locked Loops (PLLs), high-speed multi gigabit receivers and transceivers, gigabit Ethernet controllers, PCI-express interfaces and even microprocessors.

The configuration of all these components is volatile, which means that after each power down of the FPGA, the configuration has to be reimplemented. For that reason, there usually is an Electrically Erasable Programmable Read-Only Memory (EEPROM) on the same board. From this memory, the code is loaded onto the FPGA on power-up.
The advantages of FPGAs in comparison to ASICs or microcontrollers are the number of I/O pins, the simple implementation of logic functionality, the parallel processing of data and primarily the possibility to change the design at any time. Disadvantages are the price per single piece, power consumption, the tools needed for the design of the firmware and the complexity of the board the FPGA is hosted on.

## 3.4 Firmware implementation

The behaviour of the FPGA is determined by the code with which it has been programmed. This code is called the firmware, as it is a software embedded inside the hardware. The designer specifies the behaviour of the FPGA in program code that is then processed and finally uploaded to the FPGA as a bit stream, see Fig. 3.10. In this section the different steps will be explained.

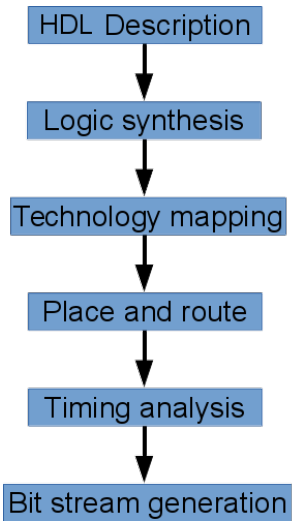



Figure 3.10: FPGA code processing steps.

### 3.4.1 Hardware description language

Generally, the programming language for an FPGA is called Hardware Description Language (HDL). It consists of code that describes the behaviour of hardware. The two most widely used programming languages are Verilog and Very High Speed Integrated Circuit Hardware Description Language (VHDL), which will be focussed on here, as it was mainly used for this thesis. There are many other HDLs,

like for example SystemVerilog or the LabView environment. Recently, also higher-level languages like C/C++ can be used to describe hardware as an embedded system design [114]. However, this method has not been used for this thesis.
Initiated by the US government in 1980, VHDL is meanwhile defined under the IEEE standard 1076-1987 and 1076-1993. There are many resources to learn VHDL. As an introduction [115] and [116] are helpful. More detailed information can e.g. be found at [117] and [118]. The code is an abstraction of hardware and in reality will be executed in parallel, which is different to programming languages like for example C++. There are three main levels of abstraction VHDL can be written in:

**Structural model** The system is described as gates and component blocks connected by wires to perform the operation the designer wants. It reflects a graphical representation or can be understood as soldering together small less "smart" components. Hence, this model can only describe the connections between components, but no logic operation. The following code example shows a structural design of a half adder. The logic functionality is achieved by connecting two components that need to be defined elsewhere. The components are generated in the first part of the code, together with their ports. In the second part, after the `Begin` statement, the ports of the components are connected to the ports of the half adder.

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

entity half_adder is
port (A,B:in std_logic;S,C:out std_logic);
end half_adder;

architecture struct of half_adder is

Component ANDGATE
port(X,Y:in std_logic; Z:out std_logic)
End component;

Component XORGATE
port(U,V:in std_logic; W:out std_logic)
End component;

Begin
A_inst : ANDGATE port map(
        X => A,
        Y => B,
        Z => C
);
X_inst : ORGATE port map(
        U => A,
        V => B,
        W => S
);
End struct;
```

**Behavioural model** The behaviour of components can be described best with this model. The designer can define how input signals interact to create an output signal, for example with a mathematical operation. This can happen on Register Transfer Level (RTL), where the data flow in the system is described or on algorithmic level, with instructions as a sequence of operations. In that way, also a sequential logic can be implemented. The code example shows again the half adder, this time in the behavioural model on algorithmic level. The code in that case looks much more compact. In fact for such a simple logic, a structural approach would not be appropriate.

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

entity half_adder is
port (A,B:in std_logic;S,C:out std_logic);
end half_adder;

architecture behav_algo of half_adder is
Begin
    Sum : process(A,B)
    Begin
        If (A=B) then
            S<='0';
        else
            S<=(A or B);
        end if;
    End process;
    Carry : process(A,B)
    Begin
        case A is
            when '0' =>
                C <= A;
            when '1' =>
                C <= B;
            when others =>
                C = '0';
        End case;
    End process;
End behav_algo;
```

An even shorter description is the following code that is on RTL.

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

entity half_adder is
port (A,B:in std_logic;S,C:out std_logic);
end half_adder;
```

```
architecture behav_RTL of half_adder is
Begin
    S <= A xor B after 5 ns; -- output delayed by 5 ns
    C <= A and B after 5 ns;
end behav_RTL;
```

**Dataflow model** The flow of data can be defined with this model. For example a variable `y` can be assigned to another variable `x` (`x <= y` in VHDL) and this will be executed every time `y` changes. The code description in the last example is in fact also a data flow description.

Usually all models are combined in code, but it makes sense to use for example only a structural model to connect components that have been defined in a behavioural model before. This allows VHDL to become modular. The code for a counter logic with two inputs (`clk` and `reset`) and one output `something` is shown below. This code can be saved in a VHDL file and would compile using a HDL software environment. Additionally an implementation constraints file or ucf file will be necessary to specify the connection of these signals to the FPGA pins and other constraints. In the following sections the processing of this code in the `Xilinx ISE environment`[2] will be shown.

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
Use ieee.numeric_std.all;

entity counter is
port (clk,reset:in std_logic;something:out std_logic);
end counter;

architecture behav of counter is

signal cnt : unsigned(3 downto 0);
signal i : integer range 0 to 15 := 0; -- initial value 0
Begin
    count : process(clk,reset)
    begin
         if reset = '1' then
            cnt <= to_unsigned(2,cnt'length); -- cnt <= "0010";
        elsif (clk = '1' and clk'event) then
            cnt <= cnt + 1;
        else
           cnt <= cnt;
        End if;
        something <= std_logic(cnt(3));
        i <= to_integer(cnt);
    End process;
End behav;
```

[2] For this thesis, FPGAs and development software of the vendor Xilinx were used. Xilinx is one of the main vendors on the FPGA market. Others are for example Altera, Actel and Lattice.

**Behavioural simulation** Simulating the program code with a behavioural simulation is an essential part of the hardware description. The code is transformed into a model that includes all signals described in the code. If needed the designer can step through every single operation and monitor the value of each variable at any time. Complex test benches can be written to evaluate the result of complex processes. This way any difference between the desired and implemented behaviour can be explored. The simulation software in the `Xilinx ISE` environment is `Xilinx ISIM`.

### 3.4.2 Logic synthesis

Contrary to writing HDL code, logic synthesis needs a special software tool. The program transforms the behaviour or structure that has been described in code, into a design implementation consisting of FFs, LUTs and connections called “netlist”. In Fig. 3.12 the synthesis result for the counter code within the `Xilinx ISE` environment is shown, Figure 3.11 shows the environment itself. In 3.12a the component “counter” with its inputs and output is shown. The expanded view of the content of this component can be seen in 3.12b. The counter consists of some LUTs, FF and the connections between them. Additionally there are buffers for the in- and output signals. All these components have been created by the software tool in order to achieve the functionality that has been described in the code.

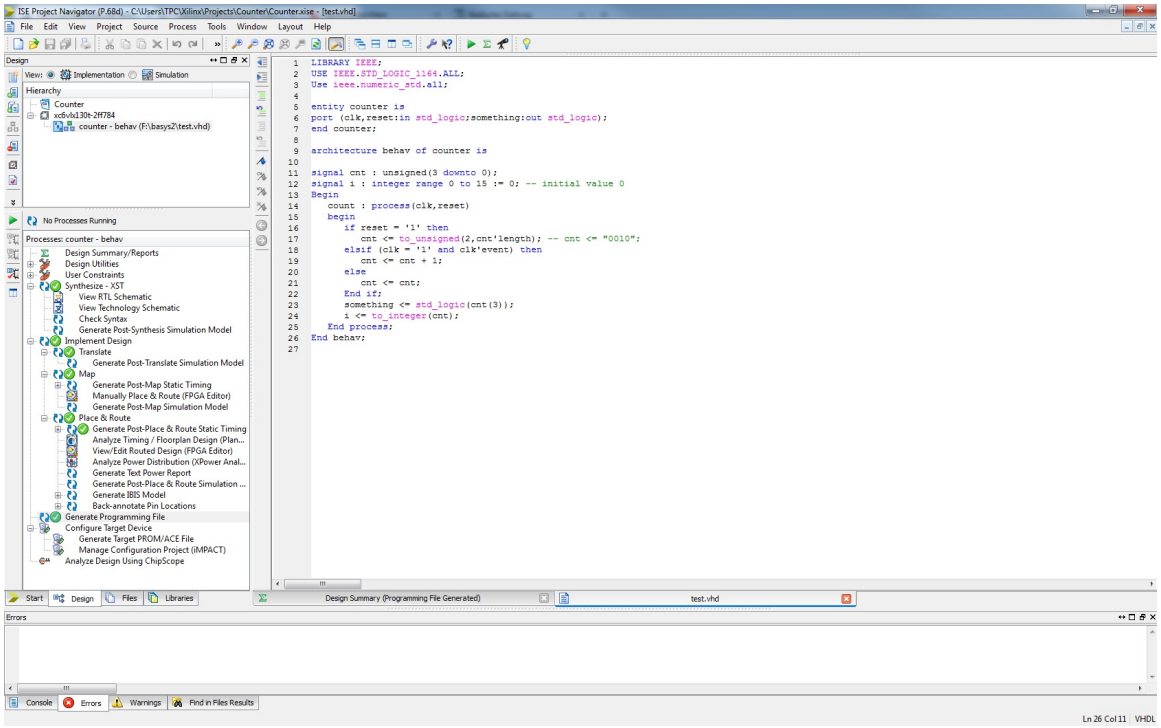
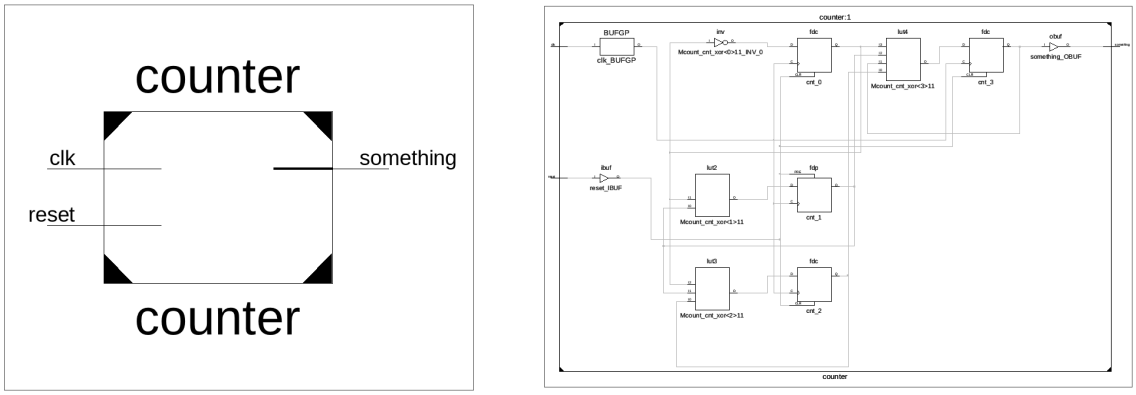



Figure 3.11: `Xilinx ISE` environment. In the main body on the right, the file test.vhd is open. It includes the code for the counter. In the window at the top left, the hierarchical structure of the code is displayed. It includes in this case just the entity counter. The lower left window shows the compiler steps. In this case all steps have a green label that indicates that no warning appeared in the different steps.The window at the bottom of the page is the compiler output window. Errors, warnings or just the progress of the compilation can be inspected there.




(a) Structural view of the component counter

(b) Implementation of basic components

Figure 3.12: RTL schematics of a counter.

### 3.4.3 Technology mapping

After the code has been transformed into an electronic circuit, the mapping evaluates how many components are needed. A list is generated that also includes the connections. Technology mapping is the first process step that also takes the specific FPGA into account on which the design will be implemented. A library with the available resources is used. The components are fitted into the floorplan of the FPGA. An optimisation of the arrangement is done in the next step.

### 3.4.4 Place and route

The placer has to decide which of the many resources inside the FPGA will be used. There are several constraints which have to be fulfilled, as for example the signal propagation between two components. A typical problem with large designs is the propagation of time critical signals. In a complex logic, simultaneous operations at the edge of a system clock are desired. Hence, the clock signal needs to be applied to all components of this network, which can be distributed over the complete FPGA. In order to keep the simultaneity, the propagation delay of the clock signal has to be smaller than the period. The designer can specify a maximum delay for signals as a constraint. It is also possible to define the specific resource of the FPGA, a certain component of the code shall be implemented in. There are many algorithms available optimised for different parameters. These are for example area minimisation, delay minimisation or power minimisation. Finally the router decides the signal paths between components and sets the LUTs for the connection and switch blocks. In Figure 3.13 and 3.14, the result of the place and route process for the counter code is shown.

### 3.4.5 Timing analysis

When all components and signal lines are fixed a timing analysis is performed and a report about the propagation time on all wires is produced. If the place and route routine could not achieve the required propagation delays, the compiler will report an error or warning and details about the specific components that lead to this failure. In this case the designer can use a different routing algorithm, reinvestigate the code or lower the clock frequency. Besides the timing report there are many other reports of the different processing steps available in the `Xilinx ISE environment`.

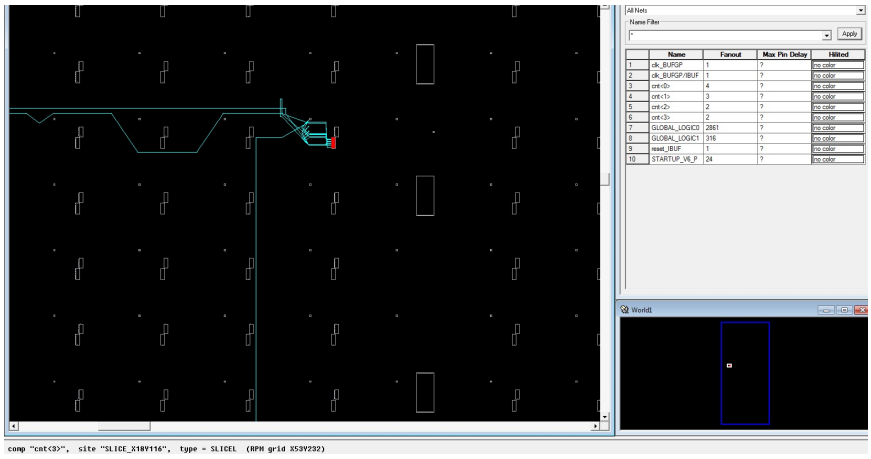


Figure 3.13: FPGA schematics with placed and routed counter logic, zoomed view on the slice used to implement the counter logic.

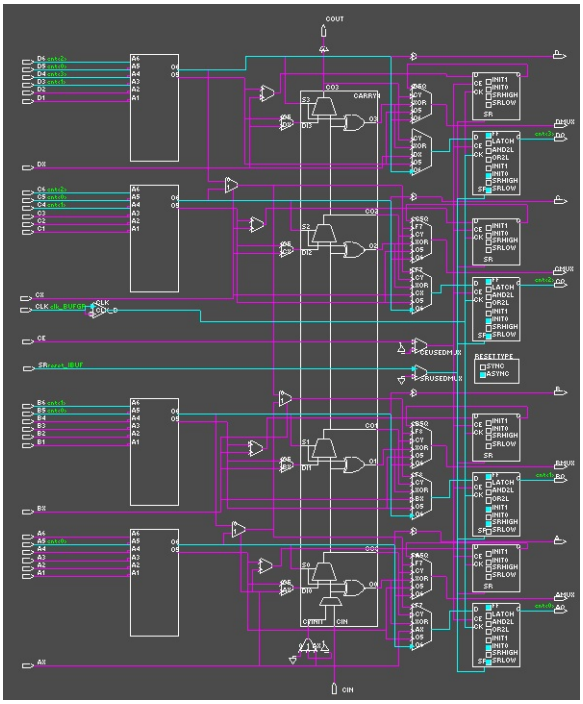


Figure 3.14: FPGA schematics with placed and routed counter logic, view inside the slice used to implement the counter logic.

### 3.4.6 Bitstream generation

Finally, the list of components and nets that is now fixed to the FPGA resources is converted into a binary file. This file is then transferred to the FPGA as a bitstream. The bits for the configuration memory define the states inside the connection and switch blocks. Other parts of the file contain the information for the LUTs in the CLBs.

## 3.5 The Scalable Readout System

The SRS [119] [120], developed by the RD51 collaboration at CERN, is a general purpose multi-channel readout system, designed to host different detectors. It was designed in 2009 taking into account the large variety of requirements by different readout systems. In order to fulfil the needs of many users, the following general properties guided the design:

- Common chip link interface for the different readout chips at the detector.
- Scalability from small test systems with a few channels up to large systems for an LHC experiment.
- Integration of commercial standards to set up a cheap system and to minimise the components a user has to design.
- A default data acquisition system that is supported and robust.
- Flexibility to allow a user specific trigger scheme or readout architecture.

The SRS consists of a modular structure. It can be adapted to different front-end chips. The central part of the system is the Front-End Concentrator (FEC) that can be connected to a user-specific adapter board by Peripheral Component Interconnects (PCIs), an industrial standard connector. Most of the PCI pins are directly connected to the FPGA on the FEC. To connect the adapter card with the specific front-end chip, most of the users choose the High Definition Multimedia Interface (HDMI) standard cable because of suitable characteristics (see Section 4.2.5), with a self defined pinout. Data handling and slow control for the front-end chip can be managed by a dedicated firmware operating at the FPGA. The communication between FEC and DAQ system is provided by commercial 10 gigabit Ethernet on an Small Form-Factor Pluggable (SFP) plug. Several FECs can be connected to one DAQ computer by a Scalable Readout Unit (SRU) that can in first order be understood as an Ethernet switch. This way, a bus system, which is prone to failures, could be avoided. The SRS also provides DAQ and slow control software based on ALICE Data Acquisition And Test Environment (DATE) [121] as a default option. An overview of the SRS logical architecture can be seen in Figure 3.15.

Several front-end chips have been implemented in the SRS. In an industrialisation process, the system is transformed to the Advanced Telecommunications Computing Architecture (ATCA) standard. An overview of the latest developments and the supported front-end chips can be found in [123].

The SRS FEC comes in two different versions. The FEC3 holds a `XC5VLX50T FFG665` Virtex®-5 FPGA, while the FEC6 (see Figure 3.16) holds a `XC6VLX130T FFG784` Virtex®-6 FPGA. These FECs are arranged in a Eurocrate chassis that also includes a standard ATX PC power supply.

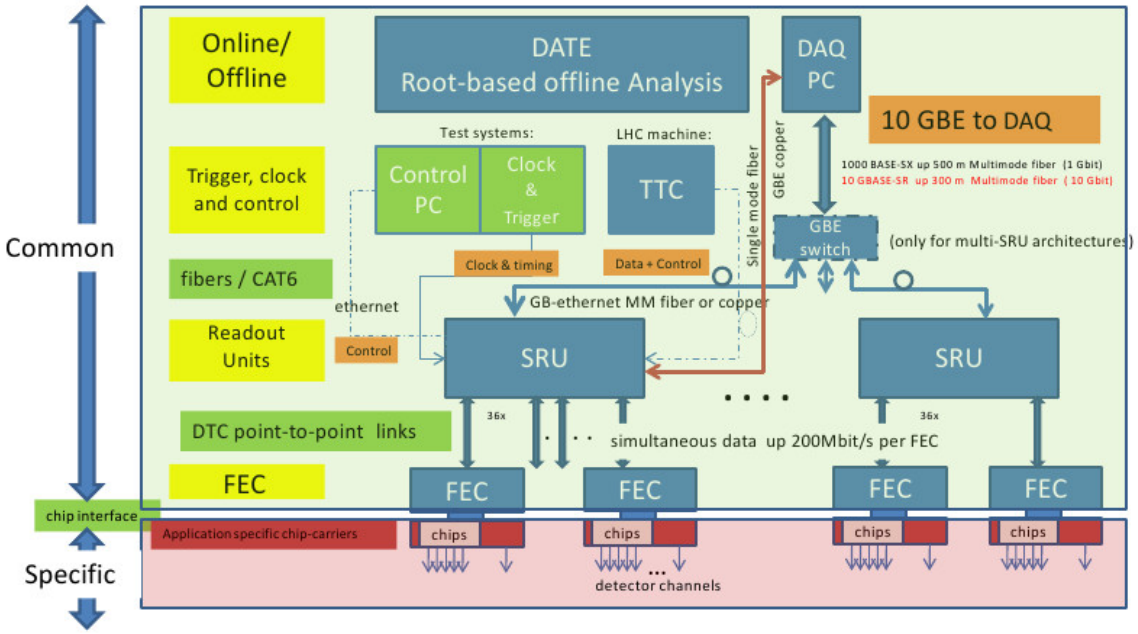



Figure 3.15: Logical overview of the SRS architecture, from [122]

## 3.6 The Xilinx ML605 evaluation board

The Xilinx ML605 board (see Figure 3.17) is part of the Virtex®-6 FPGA ML605 Evaluation Kit [124] [125] and holds a `XC6VLX240T-1FFG1156` FPGA of the Virtex®-6 family [126] [127]. The board is designed for development and testing of firmware for the particular FPGA. It includes many components commonly used in an embedded processing system. These are for example Double Data Rate (DDR) memory and flash EEPROM, gigabit Ethernet, Light Emitting Diodes (LEDs) and push buttons. Additionally, there are many connectors i.e. general purpose I/O pins and FPGA Mezzanine Card (FMC) connectors that are directly routed to the FPGA. The latter can especially be used to connect secondary user designed boards to the FPGA or other ML605 components. The whole kit is delivered with many user guides and sample programs that can serve as a good starting point for the development of new firmware.

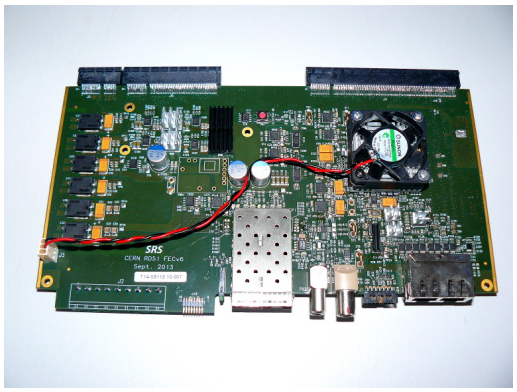


Figure 3.16: SRS FEC6.

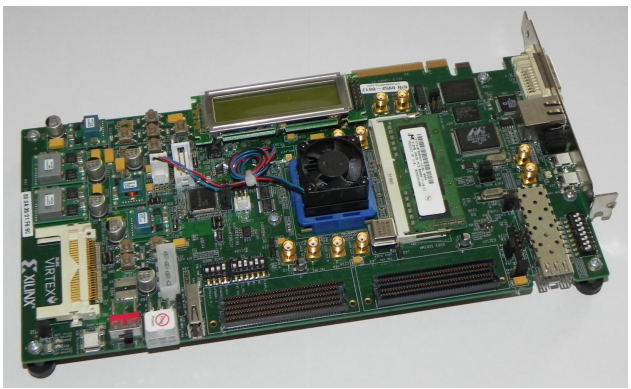


Figure 3.17: Xilinx ML606 board.

## 3.7 Network communication

The FPGA boards mentioned in Section 3.5 and 3.6 both hold industrial standard network connectors. For the communication between the readout system implemented in these boards and the DAQ software on the computer, the `1000Base-T` Gigabit Ethernet standard normed under `IEEE 802.3` has been chosen. Before the properties and protocols of Gigabit Ethernet will be explained, a short summary about the network model will be given.

### 3.7.1 Network models

In order to communicate between different systems, a network can be set up by connecting these devices. For the transfer of data, several protocols have to be taken into account, which are structured in layers. The fundamental idea is that those layers serve each other only from bottom to top. Examples are the Department Of Defence (DOD) layer model or the Open Systems Interconnection (OSI) model. The later is an International Organisation For Standardisation (ISO) standard. The highest layer, the application, can call the lower layers to serve it, which are in this order the presentation, the session, the transport, the network, the data link and the physical layer. For communication between two applications on different devices, the data generated in an application uses the layers below. Each layer adds a header and sometimes also footer to the information it has received from the layer above. At the end, all information is passed to the physical layer, for example Digital Subscriber Line (DSL) or Universal Serial Bus (USB) and transmitted to the other device, where the application uses the lower layers to encode the information. On every step upwards, the layers header and footer is analysed and removed, before being passed upwards.

### 3.7.2 Gigabit Ethernet layer model

Gigabit Ethernet describes the communication with $10^9$ bits per second. Strictly speaking, Ethernet only describes the two lowest layers in the OSI model, the data link and physical layer. In the `IEEE 802.3` standard, the basic transfer unit is called a packet or frame. In order not to confuse with the dataset from one readout of a complete matrix from the Timepix chip, which is also called a frame, the unit will be called packet hereafter. The two layers are divided in sublayers which fulfil different operations. The most important one in the data link layer is the Media Access Controller (MAC) for the media specific access. An Ethernet package has one header and sometimes a footer for each layer to pass through the different layers. The headers consist of special bits needed to transfer the data to the correct destination and hold additional information arranged as defined by a protocol.
The first eight bits of an Ethernet frame are a preamble with an alternating bit sequence for synchronisation between different network devices. Then, the Ethernet header starts with six bytes for the destination address and six bytes for the source address. An example of an Ethernet packet recorded with the network protocol analyser `wireshark` is shown in Figure 3.18. The destination MAC address, in this case the Xilinx FPGA on a FEC, is highlighted. The Ethernet header is followed by the Internet Protocol (IP) header, which holds the destination and source as IP addresses, together with other information, for example the protocol type of the next header, which is User Datagram Protocol (UDP). The innermost part of the packet is the user data, in this case with a length of 154 bytes. At the bottom of the `wireshark` window, the whole packet is displayed in hexadecimal numbers. Again, the destination MAC address is highlighted. The setup of a packet with these protocols is only one way of communication. In most of the commercial application and especially for internet communication for example, the Transmission Control Protocol (TCP) is used instead of the UDP, as with this protocol, packets lost in

the network can be deteted and recovered.
The addressing in the network is done by the physical address, which is the MAC address of the device. On the higher layers, the different devices are accessed, however, with the IP address and the port. The physical address is not known in this layer. The advantage of this model is that applications do not send their data directly to a device, but to an abstract IP address, which then can be assigned to a physical device. In case the destination application is moved to another device or the network adapter at the destination computer is exchanged, the source application does not need to be changed. The operating system in a computer holds a list with the assignments of IP to MAC addresses, defined by the Address Resolution Protocol (ARP). If an application for the first time establishes connection with an application on a different device in the network of which the MAC address in unknown, it sends out an ARP request. Therefore, the requesting computer sends out a broadcast to all devices in the network with its own MAC and IP address and the IP address it is searching for. The computers in the network then check, weather the IP address searched for is identical to their own IP address and send out an ARP answer with their MAC address. Now, both computers can add the other device to their ARP list. It is also possible to manually add an ARP entry to a computers list, in case a destination device is not able to answer ARP requests, but the user knows the device's MAC address.

## 3.8 The large TPC prototype and test beam area at DESY

In the scope of this thesis, two test beam campaigns have been carried out to test the Pixel-TPC prototypes. A setup at DESY was used.
Since the end of 2008, the LCTPC collaboration operates the LP, a prototype for the ILD TPC at DESY [128]. It consists of a field cage with a diameter of 75 cm and a length of about 56 cm. The endplate is a cut out of the final ILD TPC and can host seven modules, see Figure 3.19. The TPC is installed in a 1.25 T magnet called PCMAG, which can be rotated, lifted and shifted by a movable stage, see Figure 3.20. The whole setup is placed at a test beam area T24 at the DESY II accelerator which provides electrons or positrons with an energy up to 6 GeV, see next section. It includes a gas system to connect pre-mixed gas bottles. From a test beam hut directly besides the area, the experiment is remotely controlled. This includes the high voltages, magnet, stage positioning motors, gas system, beam shutter, collimators and momentum selection magnet.
For testing different MPGDs technologies, the different groups in the collaboration build modules and perform test beam campaigns at the LP. The modules used for the studies presented in this thesis will be introduced in Section 4.3.

## 3.9 The DESY II synchrotron

The beam provided at the test beam area T24 is generated by the DESY II synchrotron. DESY II has a circumference of 292.8 m and accelerates a single bunch of up to $3 \times 10^{10}$ positrons or electrons from an injection energy of 450 MeV to a maximum energy of 6 GeV. The particles are provided for the PETRA III storage ring and the test beam areas. For PETRA III, they are directly ejected. For the test beams, the beam is provided via two conversions. First bremsstrahlung is created in a 10 µm thin carbon fibre in the beam. From the photons, electron-positron pairs are then generated in a copper or aluminium target. By tuning a magnet particles with a defined energy can be selected to pass though a collimator. A sketch with the simplified setup is shown in Figure 3.21. The maximum energy of the particles at the test beam is 6 GeV. The intensity strongly depends on the energy as bremsstrahlung has a $1/E$ dependence [129].

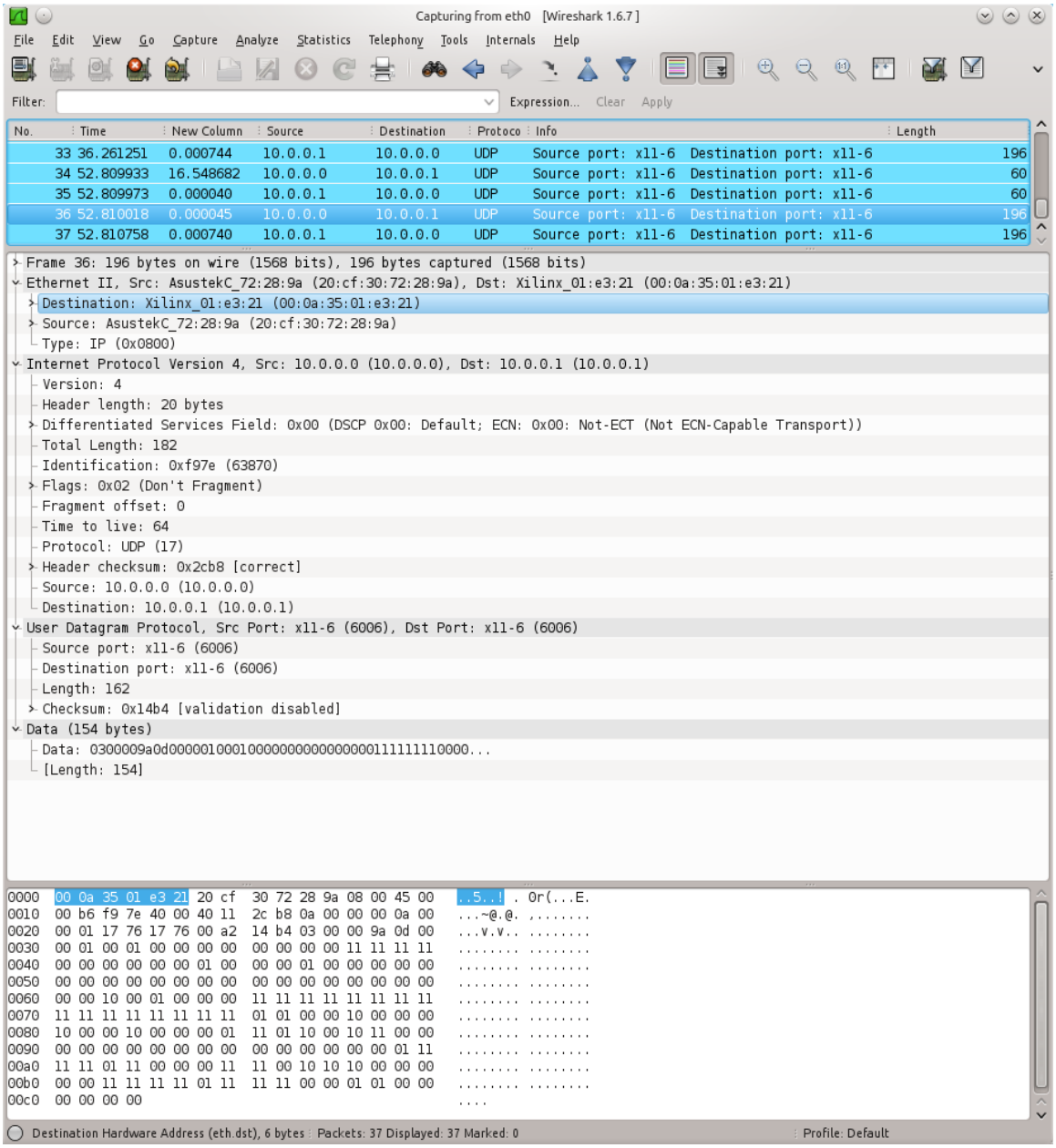



Figure 3.18: Example of an Ethernet frame with Ethernet, IP UDP header and user data recorded with the network protocol analyser `wireshark`.

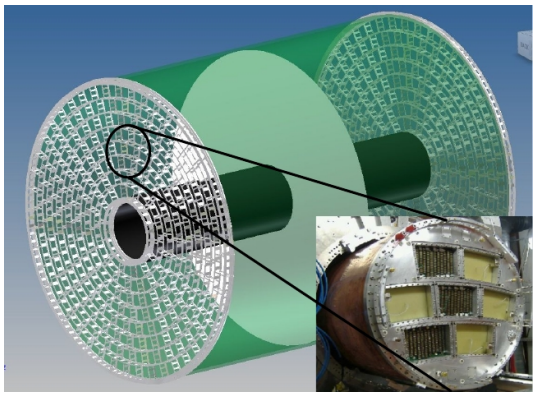


Figure 3.19: Schematic of the ILD TPC with illustration of the LP.

Figure 3.20: Image of the complete LP setup at DESY.

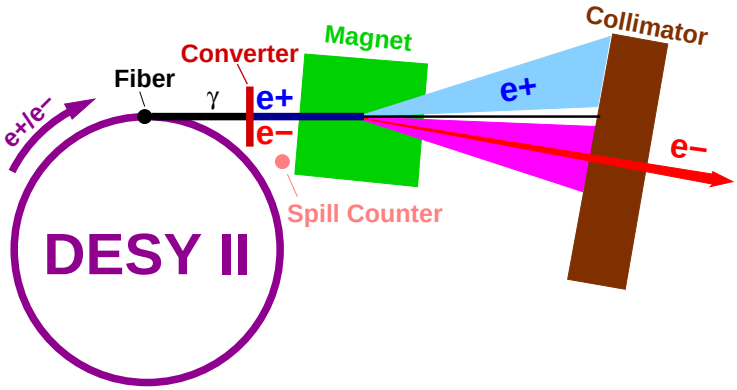



Figure 3.21: Schematic layout of a test beam at DESY, from [130].

CHAPTER 4

# Hard- and software developments

After the technical aspects of the tools have been explained in the previous chapter, the tools developed to realise the Pixel-TPC will be introduced. The main goal of the project was the development of a readout system which can handle many Timepix chips at once. Before the start of the project, there were only two systems available, the USB interface [131] and the Medipix Universal Read-Out System (MUROS) [132] shown in Figure 4.1, which could read out a few chips at the same time. For both of


Figure 4.1: USB interface (left) and MUROS (right), not same scale, from [133].

them, the Pixelman software package [134] is used as DAQ software. The USB interface is directly connected to a carrier board holding a single Timepix chip via a Very-High-Density Cable Interconnect (VHDCI) connector. Cables between the device and the carrier board are not foreseen, despite only the serial readout mode is implemented. For the connection to the computer, a USB cable is used. 10 MHz, 20 MHz, 40 MHz or 80 MHz can be selected by the user for the FCLOCK frequency. Still, the maximum readout rate is five frames per second. With the MUROS, up to eight chips in a chain can be read out in the serial mode. The FCLOCK frequency can be tuned with a potentiometer up to 240 MHz. The maximum theoretical readout rate is about 50 frames per second, but in realistic applications about 10 frames per second can be reached. For the connection with the Timepix chip carrier, a VHDCI cable of up to 3 m length can be used. The MUROS is connected to a type DIO-653X National Instrument card with a special cable as interconnect. Unfortunately, this card is commercially not available any more. Also the MUROS itself is not produced any more. In test beam campaigns, the MUROS was used as a readout of a double quadboard (two synchronised MUROS) [135] and an octoboard [74]. For a

larger number of Timepix chips, no readout system was available. For further developments of detectors which use Timepix chips, adequate readout systems are necessary. The MUROS is discarded due to the non-availability, the USB interface cannot handle more than a single chip and is slow. At that time, it was clear that the next step in the field of pixelated gaseous detectors has to be the development of a new readout system. Besides the project described in this thesis, there are different designs of readout systems for the Medipix2 and Timepix chips, which also follow strategies for different applications.

- In cooperation with PANalytical, NIKHEF has designed the Relaxd [136] readout. One Relaxd device can read out up to four chips in serial mode, with a speed close to the theoretical maximum. The system consists of two boards connected in a T-shape. The carrier board holds four chips, while the other boards supplies currents and control signals. An FPGA on the second board processes the data and communicates with the computer via Gigabit Ethernet. Several of the T-shaped structures can be placed side by side to increase the active area. A variation of this system can handle four single chips, which are connected to the second board with cables, such that the system becomes the shape of a spider with four legs and the FPGA board as body. Because of the participation of commercial partners to the project, the source code of the FPGA is not publicly available.

- As a successor of the USB interface, the FITPix [137] has been developed at the Technical University of Prague. This system is also based on an FPGA. The connection to the computer still is USB, but was improved to the 2.0 standard and can power the whole system. The readout speed could be increased to 90 frames per second for a single chip in the serial readout mode. For the connection between chip carrier board and FITPix, again the VHDCI connector was chosen. FITPix is also able to handle several chips in a chain, but needs external powering in this case.

- At the University of California, the Berkeley Quad Timepix detector [138] has been developed. This device, designed for the detection of neutrons with a Micro-Channel Plate Detector (MCP) read out by Timepix chips, consists of a quad array read out in the parallel mode. Hence, the frame rates is much higher than with the previous systems and reaches up to 1 kHz. Three different boards are necessary to achieve such a high frame rate. The first one is the carrier board of the four chips and the MCP on top. There are two Interface Boards connected to the carrier by 100 pin connectors, each with an FPGA to collect the data from the CMOS parallel ports, store and rearrange it, convert it to LVDS and send it via a 40 twisted pair cable to another FPGA on the ROACH board. The connection to the computer is provided on this board via 10 Gigabit Ethernet.

- Another system based on the parallel readout of the Timepix chip with an FPGA has been developed at the European Synchrotron Radiation Facility. The readout interface, called Parallel Readout Image Acquisition For Medipix (PRIAM) [139], can host up to five Medipix2 or Timepix chips and achieves a frame rate up to 1.4 kHz for a single chip. It is implemented in a photon counting detector called Multichip Area X-Ray Detector Based On A Photon-Counting Pixel Array (MAXIPIX) [140].

The readout system built in the scope of this thesis is in many aspects different to those mentioned above. Primarily, many Timepix chips should be read out, where many means around 100. The readout speed was not the primary goal, but also taken into account. Scalability also is a key element, such that the system could in principle also read out even more chips. This way, the demonstration that the readout of a Pixel-TPC is possible can be achieved. As the design of a completely new FPGA board was out of the capabilities of our group, existing technology had to be used and adapted for our special needs. As an ideal candidate because of the features it provides, the SRS (see Section 3.5) became available at

the same time. More as a side product for the advancement of the development, but finally as a readout system which finds application for smaller systems, the Timepix readout based on the Xilinx ML0605 Evaluation board was designed.
In general, the readout system consists of a chain of different components that have the aim to allow for communication between a computer running a dedicated software and one or several Timepix chips. To have a flexible design, the following components are needed in a chain starting from the computer side:

- The computer has connectors for commercial cables, hence it is preferable, to use one of the standards as for example the USB interface does. For a faster communication with higher load, the Ethernet standard is the optimal choice. It has the advantage that long cables are available, as well as network components to bundle data from several readouts. As all those are standard components used in everyday life, they are also cheap.

- The readout system needs algorithms, which can handle the data coming from the chip and generate the control signals. As has been seen in Section 3.3, FPGAs are a tool, which can be programmed to fulfil this task. Moreover, they are available on boards, which can be connected by Ethernet on one side and provide a wide variety of connectors on the other side, see Section 3.5 and 3.6.

- It would be possible to design a board, which can be connected directly to the FPGA board. However, this would decrease the flexibility. It is desirable to have another cable between the readout system and the frontend chip for many reasons. In any case, an adapter board is necessary to connect the FPGA board with a cable or the chip. Such a board is specific in design and not commercially available.

- Both the adapter board and the Intermediate boards are self designed. Therefore, the choice of the cable in between is completely free. For the MUROS, VHDCI cables were used, which have several disadvantages as will be explained in this chapter. A setup for that cable and another one for HDMI cables were designed.

- To interface the cable to the Timepix chip, another self designed board is required, it is called the Intermediate board.

- For reasons of convenience, the Timepix chip is not directly glued and bonded to the Intermediate board, but on a chip carrier board. In principle, this board can also be connected to the Intermediate board by a cable, what is not foreseen in the design presented herein.

The different hardware components developed for the readout chain are explained in this chapter.
Temporally, the development started on basis of a basic readout system designed at the University of Mainz [141]. Based on the predecessor of the ML605, the Xilinx ML506 Evaluation board, this system is able to read out a single Timepix chip close to the FPGA board. As a first step, the system was transferred to the newer board by adapting the firmware and designing an adapter board for the connectors. The main firmware developments were then performed on the ML605, still after the SRS became available. As a completely functional Timepix readout system, this system is used at the CAST experiment at CERN and at the Universities of Siegen and Bonn. Another transfer to the FEC3 and finally to the FEC6 completed the implementation of the Timepix chip in the SRS. Different flavours of readout designs were built during the development phase, for example one which allows MUROS users to change to the SRS-based readout by keeping their setup the same. The step to a large system for an arbitrary number of chips was then performed on the FEC6. Figure 4.2 shows a time line with the different systems, the split to final versions and where they are applied.

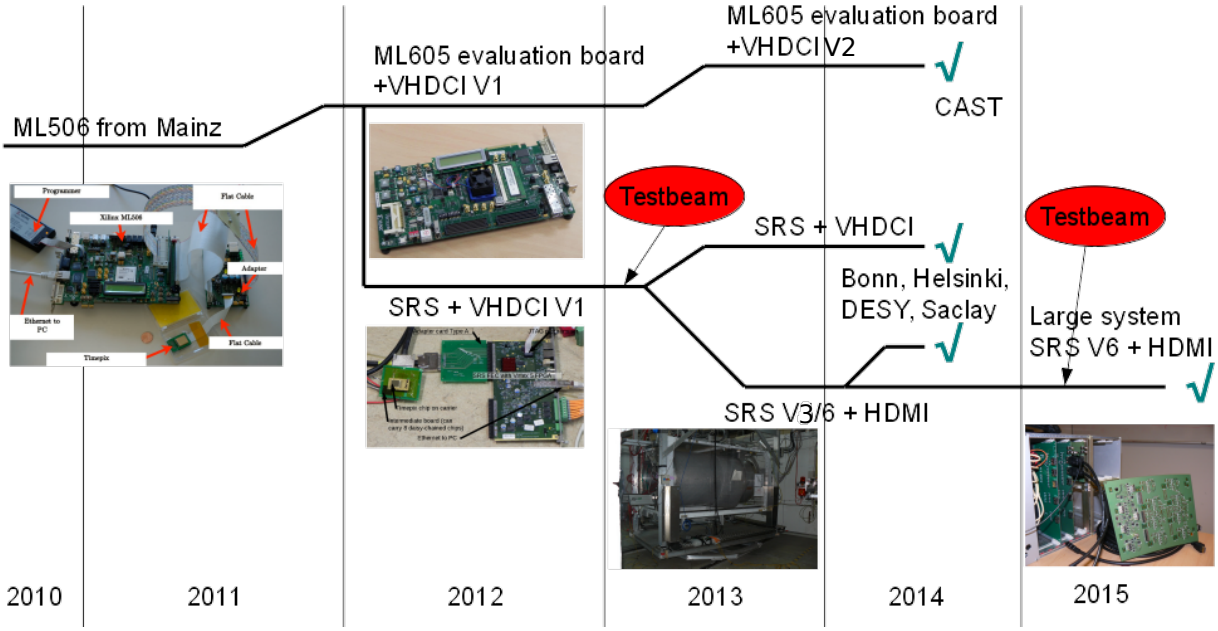



Figure 4.2: Time line of the ML605 and SRS-based Timepix readout development.

The following sections give an overview of the two system and their flavours from the hardware side, while in the next chapter, the FPGA firmware will be explained. The results from the two test beams depicted in Figure 4.2 will be shown in Chapter 7 and 8.

## 4.1 ML605-based Timepix readout system

At the very beginning of the project, the SRS was not available, so the firmware development started on Xilinx evaluation boards. These systems are appropriate devices for prototype systems, as they provide a good documentation by Xilinx, such that also beginners of FPGA programming can handle them. An excellent starting point was the Timepix readout based on the Xilinx ML506 Evaluation board developed by Michael Zamrowski for his Diploma Thesis [141], shown in Figure 4.3.

### 4.1.1 Design choices

The design of the Xilinx evaluation board Timepix readout systems was first driven by the fact that those systems are just an intermediate step towards the SRS-based system. So a simple and easy to build setup was preferred to rapidly test the functionality of the firm- and software. The first prototype with the ML605 board simply used an adapter for the flat cable connector to the ML506, such that the flat cables, adapter board and Timepix chip on another flat cable could be reused. With this setup the transfer of the firmware to the new FPGA was verified. Afterwards, the design of new hardware components for a more advanced readout system started. The Gigabit Ethernet link for the communication between computer and FPGA board has proven to be fast and reliable. For the connection in direction to the Timepix chip, the flat cables are not very handy. A longer cable towards the chip was preferred to allow for more flexibility. The only connector on the board, which provides enough pins for all signals to and from the Timepix chip are the two FMC connectors. As these connectors are designed for a direct connection of secondary Printed circuit Boards (PCBs) to the FPGA board, a direct long cable

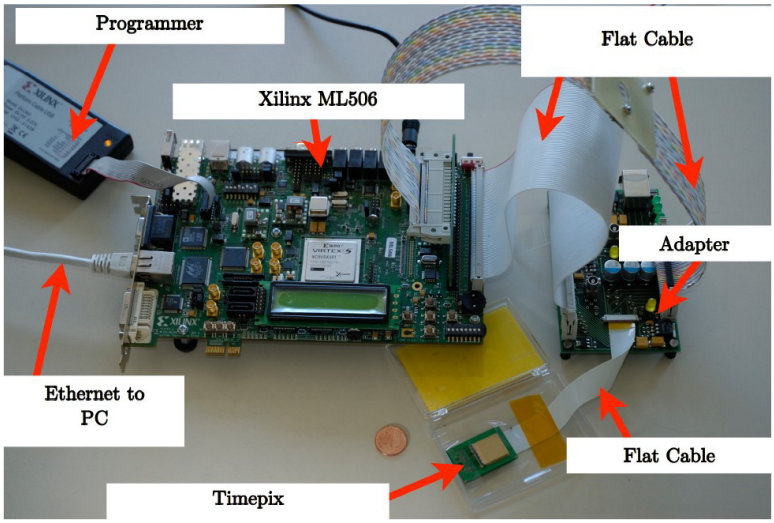



Figure 4.3: Timepix readout based on the Xilinx ML506 Evaluation boards developed by Michael Zamrowski, from [141].

connection is not possible. Therefore, an adapter board to another cable has to be put in place. As those cables were already in use with the MUROS, VHDCI was chosen. On the chip side, this results in the need of another board, called the Intermediate board, which connects to the cable. Additionally, there is another PCB which serves as a mount for the chip, called the chip carrier. All theses different boards, also shown in Figure 4.4, will be explained in the following sections. An additional benefit of the different boards is the distribution of components to assure the operation of the Timepix chip. In case of a failure or false design, not the complete hardware has to be exchanged, but only the part that does not work as desired. Also in case of damage during testing distinct components can more easily be removed. All these boards were designed in our group together with Dr. Jochen Kaminski who also did the PCB layout.

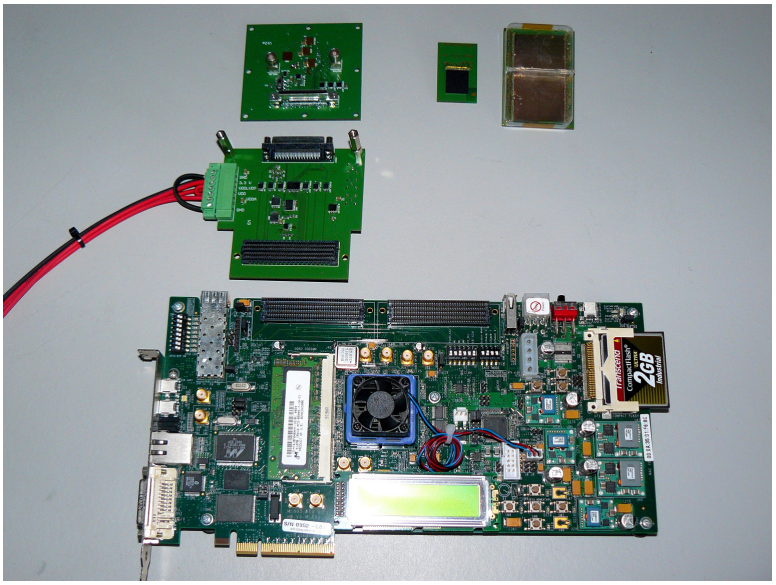
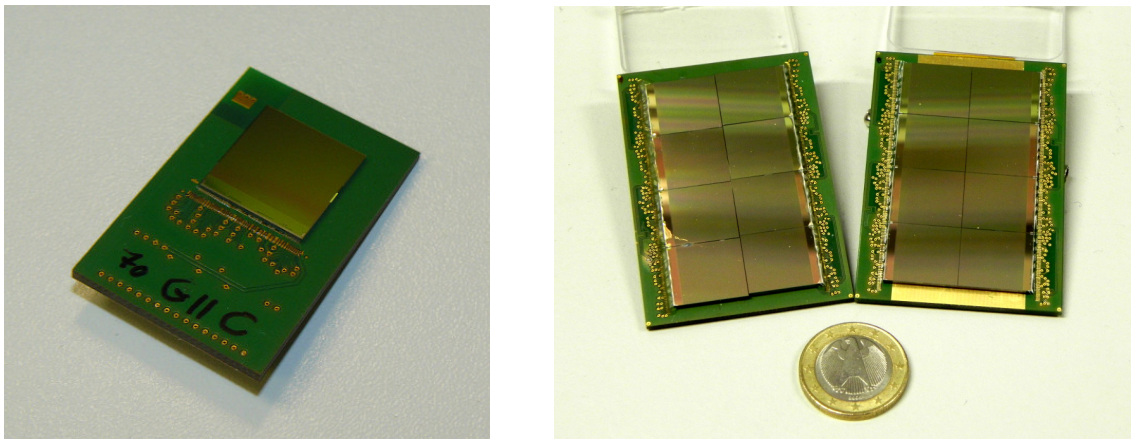


Figure 4.4: ML605-based Timepix readout system with all components excluding the VHDCI cable.

### 4.1.2 Chip carrier boards

In order to exchange Timepix chips, they are not directly glued on the board connected to the cable, which is the Intermediate board, but on a separate PCB called the chip carrier. There are two basic versions, one for a single Timepix chip (Figure 4.5a) and one for a chain of eight chips in a matrix of $2 \times 4$ chips, called octoboard (Figure 4.5b). On both versions, the chips are glued to the top side. Afterwards the electrical connection between the pads on the chip periphery, see Section 3.1.1 and the carrier is done by wire bonding. On the back side, there is a 32 pin (40 pins for the octoboard) connector to be plugged on the Intermediate board. Additionally, there are capacitors to buffer the supply voltages for the chips. InGrids can also be glued on the chip carriers. At the single chip carrier, there is a special pad for the high voltage connection for the grid. For the octoboard, a dedicated board has been designed for InGrids. On that board, each half of the eight InGrids (a matrix of $2 \times 2$) is connected to a pad for high voltage on either side of the board. On the rear side, two 4 pin connectors to the Intermediate board provide the high voltages. In Figure 4.5b, two octoboards for Timepix chips are shown. They are from different developments phases. The board on the left does not provide a large grounded area underneath the chips, which can be seen on the board on the right. This layer is connected through the PCB to the back side to transfer heat away from the sensitive surface of the chips towards the Intermediate board and out of the detector.



(a) Carrier for a signle Timepix chip.

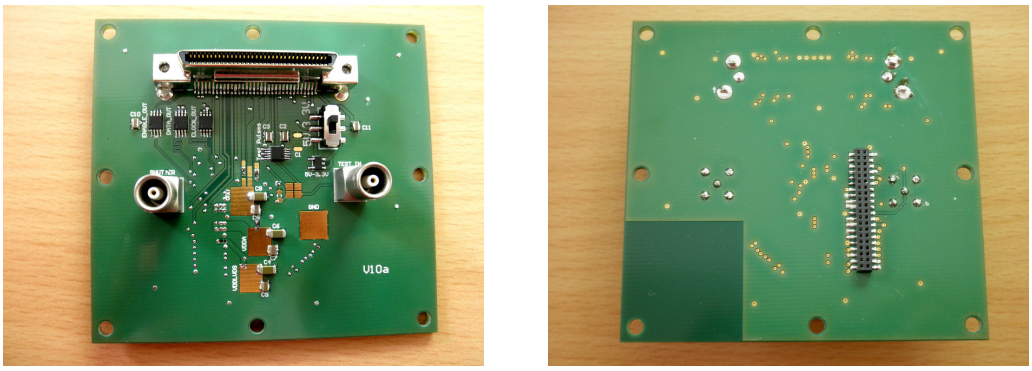
(b) Carrier for a chain of eight Timepix chips (octoboard).

Figure 4.5: Timepix chip carriers, not to scale.

### 4.1.3 Intermediate boards

Figure 4.6 shows the Intermediate board for the VHDCI cable, which is used in the Timepix readout system based on the ML605 board. The latest version is V10 with type `a` for single Timepix chips, Timepix octoboards and single InGrids and type `b` for InGrid octoboards with additional high voltage connectors on the back. The boards were designed such that they are compatible with the USB Interface, MUROS and SRS, which also have a VHDCI connector. The signals on the pins of the connector are the same, except for the power of the components on the Intermediate board, which need 3.3 V. The ML605 system and SRS can directly provide this voltage, while the USB Interface and MUROS provide 5 V. There is a switch on the Intermediate board, see Figure 4.6a, to enable a converter, in case the readout can only provide 5 V. There are two LEMO connectors, one to provide the shutter signal for the Timepix

chip from an external source and one for test pulses from an external source. Test pulses can also directly be generated on the Intermediate board by a multiplexer. This component is supplied by two reference voltage levels and a switch signal from the adapter board, see the next section. There are soldering pads to select the internal or external source for test pulses. For the 2.2 V supply voltages for the Timepix chip, there are two options, which again can be selected by soldering pads. In the first option, the adapter board, MUROS or USB Interface provides the power through the VHDCI cable, while in the second option, the power is directly provided through the Intermediate board. There are four large soldering pads on the top side, see Figure 4.6a to connect power cables. If the SRS-based readout is connected via a VHDCI cable, this power scheme is mandatory, as the SRS cannot provide the power for the chips. For the other systems, the powering is only sufficient to supply a single chip reliably, so for octoboards, also the second option has to be chosen. For more details how to configure the soldering pads, see [142]. The other components on the board are three LVDS drivers for the `DATA_OUT`, `CLOCK_OUT`, and `ENABLE_OUT` signals.




(a) Top side with VHDCI connector.

(b) Bottom side with 40 pin connector.

Figure 4.6: Intermediate board V10a with VHDCI connectors for MUROS, ML605 and SRS readout systems.

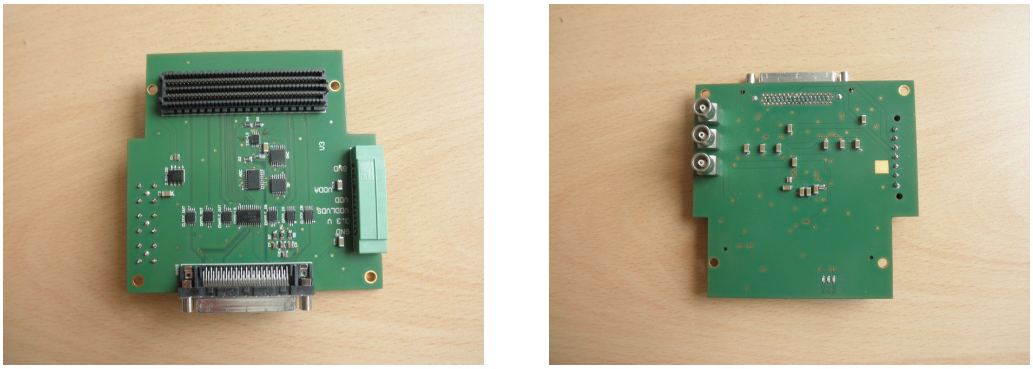
On the back side of the Intermediate board, see Figure 4.6b, a 40 pin connector provides the connection to the chip carrier. No other components are placed on this side to more easily connect to a detector. Single chip carriers, which only have a 32 pin connector, have to be put in a center position. For more details, see again [142].

### 4.1.4 Adapter boards

The latest version of the ML605 adapter board is V3, see Figure 4.7. Besides the FMC connector to the Xilinx board and the VHDCI connector, there is a seven pin Phoenix connector for the chip supply voltages and the 3.3 V for the Integrated Circuits (ICs) on this board and the Intermediate board. As the FPGA cannot generate or handle analogue signals, there is an eight-channel Analogue-Digital Converter (ADC), to analyse the `DAC_OUT` signals from octoboards or a single chip. A DAC generates the two voltages for the multiplexer on the Intermediate board for test pulsing and one voltage for `EXT_DAC`. These two components are controlled by the FPGA with a small Inter-Integrated Circuit (I2C)[1] network. The other components on the top side of the boards, see Figure 4.7a, are LVDS drivers, a CMOS level shifter and an operation amplifier for the DAC analogue voltages. The CMOS level shifter is necessary, as the FPGA can only provide 2.5 V CMOS signals, while the Timepix chip can only cope with 2.2 V.

[1] I2C is a serial data bus typically, used for inter-PCB communication between ICs. One data line (SDA) and one clock line (SCL) are used in a network with at least one master device controlling slave devices,each with its own address.

The LVDS drivers for the LVDS signals returning form the chip are implemented to protect the FPGA, the other three drivers are for the LVDS signals to the Timepix chip.



(a) Top side with VHDCI and FMC connector.

(b) Bottom side with LEMO connectors.

Figure 4.7: Adapter board for the Xilinx ML605 evaluation board via FMC connector.

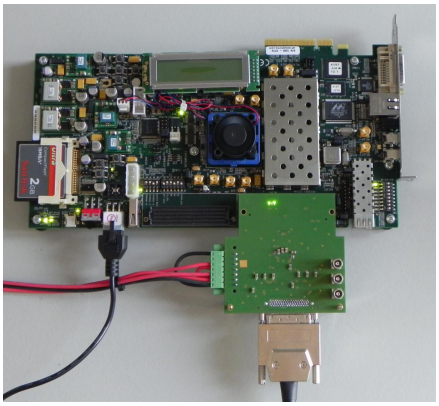
The back side of the board, see Figure 4.7b, holds three LEMO connectors for testing purposes. They provide the `M0`, `M1` and `SHUTTER` signal. There are also three LEDs to indicate a proper connection of the board and an operating FPGA firmware.

### 4.1.5 Application

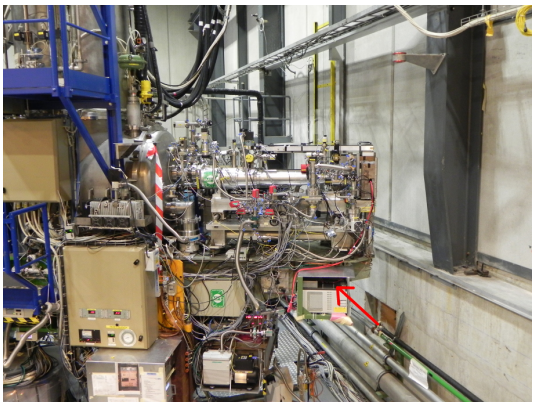
Figure 4.8a shows the ML605-based Timepix readout system in operation. Users, who already have the evaluation board or buy one, can build their own Timepix readout by adding the adapter board. If they have used the MUROS or USB Interface before, they can directly connect their detector with a VHDCI cable or use the Intermediate board presented in Section 4.1.3. For small scale systems up to eight Timepix chips or InGrids, the full functionality is provided by hardware, firmware and software. The system has proven a successful operation in our lab and was exported to the University of Siegen. Moreover, it is the standard readout of one of the four detectors of the CAST experiment at CERN, see Figure 4.8b. The detector was developed by our group [95] and commissioned at the experiment, were it now is fully implemented and continuously operated during the run periods.

## 4.2 SRS-based Timepix readout system

As explained in Section 3.5, the SRS by design aims at a simple implementation of new front-end chips into the hardware. Figure 4.9 shows the SRS design as proposed by the developers group. The hybrids or front-end chips and adapter board, or in the case of the depicted system digitiser card, are user specific. The whole chain from FEC to the computer is provided by the SRS. The user just has to design the carrier for the chip and the adapter card, which then is connected to the FEC by a PCI connector and of course his own FPGA code. As the system is not commercial, the knowledge is concentrated in the development group at CERN. At the time the FEC3 became available to our group, the FPGA firmware of the Xilinx evaluation board was transferred to that first version FEC during a three weeks research period at CERN to profit from the knowledge. Then, the main development for the SRS-based readout was conducted on a complete system with that FEC and its successor, the FEC6 in Bonn.



(a) System with adapter board and VHDCI cable in operation in the labority.



(b) Implementation in the CAST experiment, the arrow marks the position of the system.

Figure 4.8: ML605 base Timepix readout in operation.

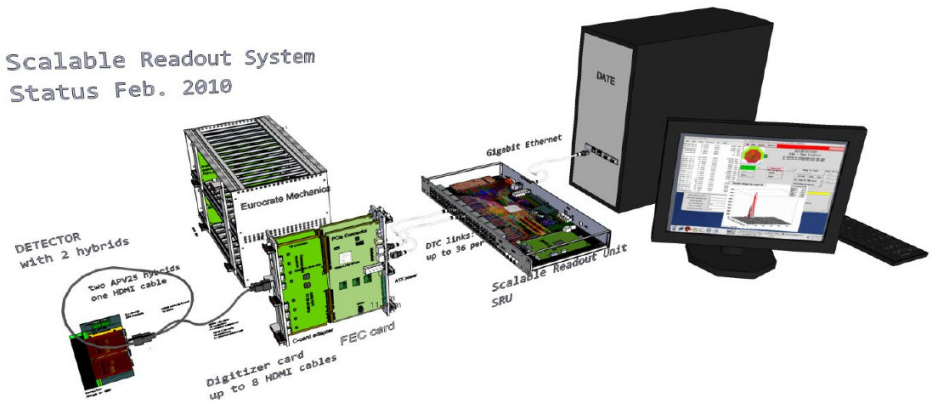



Figure 4.9: Schematic of the complete readout chain as designed by the SRS group, from [120]. From left to right: Front-end chip, Eurocrate, adapter card, FEC, SRU, computer.

### 4.2.1 Design choices

The design of the SRS-based Timepix readout is driven by the SRS design. The adapter card to the FEC first was a simple PCB to just route the chip signals to the FPGA by omitting the analogue signals like DAC_OUT or the test pulse voltages. In later development phases, this board became more complex. The latest versions will be presented below. For the cables between the adapter board and the chip, VHDCI was chosen for the first versions in order to reuse the existing Intermediate boards. As those cables can only be extended to 3 m, the design was changed later on to the HDMI standard with the demand to span about 25 m. Still, an SRS-based Timepix readout with VHDCI cables is available as final design, such that users can exchange the USB Interface, MUROS, or ML605-based system. Even though, the SRS-based readout aims to support many Timepix chips, the first setups were designed to read out at most one octoboard. Only the final version was extended to a large system, which by scalability achieved the goal. In Figure 4.10, an intermediate version of the system is shown, as it was used at a first test beam. By comparing to Figure 4.9 the similarity of the design is visible. Instead of the APV25 hybrid, a single Timepix chip on a carrier and Intermediate board serves as front-end. The adapter card to the FEC is smaller and an SRU not necessary for the small scale system. As it is possible for the ML605-based system, the chip power supply is applied to the Intermediate board. For the SRS-based Timepix readout, this method is mandatory and was kept for later designs, especially larger systems, as the FEC cannot provide the large amount of power needed by many Timepix chips. Also for the advanced design, the choice to use a chip carrier PCB, which is connected on an Intermediate board, was kept.

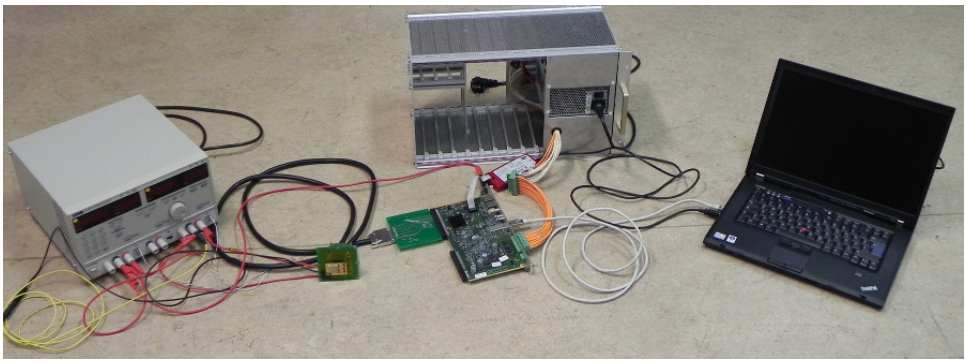
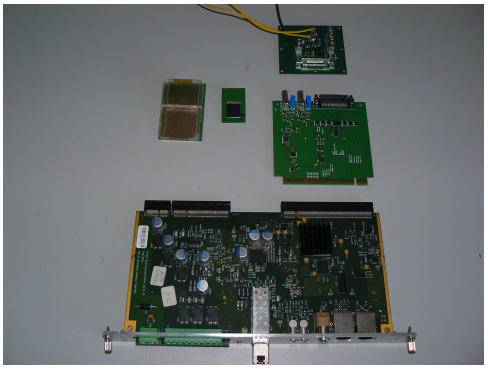


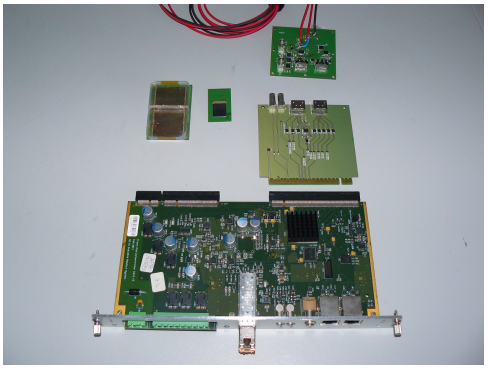
Figure 4.10: Complete Timepix SRS readout chain with single chip, external power supply, FEC and Eurocreate with power supply and computer.

### 4.2.2 Versions

As mentioned before, there are two versions of the SRS-based Timepix readout, one with HDMI cables and one with VHDCI cables. The goal of the VHDCI-based system was to be compatible with the ML650 system, USB Interface and MUROS, such that the same Intermediate boards can be used. The signals on the pins of the cable are given by the design of the other systems. The adapter board, in this design has to provide the same functionality as the adapter board of the ML650 system. Up to eight chips can be read out per FEC by this system depicted in Figure 4.11a. Contrarily to the VHDCI cable, an HDMI cable only has a few pins, see Section 4.2.5, but can span longer distances, if no CMOS or analogue signals are transmitted. So for the second version with the HDMI cables, the goal was to decrease the number of signals to transmit to a minimum and assure the reliability for longer cables. For that reason, most of the functionality has to be implemented on the Intermediate board close to the chip and not on the adapter card. The different PCBs are shown in Figure 4.11b.



(a) Components of the SRS-based Timepix readout with VHDCI cable.



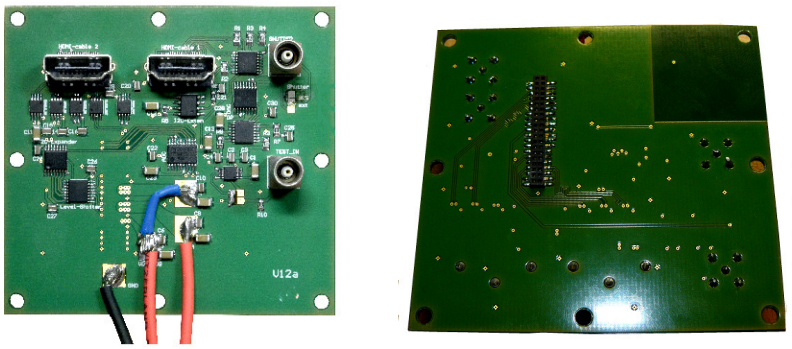
(b) Components of the SRS-based Timepix readout with HDMI cables.

Figure 4.11: Two versions of the SRS-based Timepix readout systems with all components despite the cables. The FEC3 is shown here.

### 4.2.3 Intermediate boards

The Intermediate board for the system with VHDCI is the same like the one explained in Section 4.1.3. For the system with HDMI, the Intermediate board is more complicated, as only a few signals are transmitted through the cables and more functionality had to be implemented on the board close to the chip. The latest version is V12 with type `a` for single chips and Timepix octoboards (see Figure 4.12) and type `b` for InGrid octoboards. As can be seen in Figure 4.12a, there are two HDMI connectors on one Intermediate board. One cable transmits all fast, differential signals to and from the Timepix chip, while the other one is responsible for the transmission of the slow control signals. For more details see Section 4.2.5. All signals through the first connector have LVDS drivers. As analogue or CMOS signals cannot be transmitted over distances longer than about 1 m, the signals needed by the chip are generated on the Intermediate board. For that reason, the I2C network spans not only the adapter board, but also reaches the Intermediate board. In order to propagate the I2C signal over longer distances, an I2C extender IC is placed on the Intermediate board as well as on the adapter board. The I2C network controls an eight channel ADC to read out the analogue `DAC_out` signals from the chips, a DAC to generate the two voltages for the test pulse multiplexer and one voltage for the `EXT_DAC` and an eight channel I2C expander. This device generates up to eight 2.5 V CMOS signals from I2C data packages. In this case, the `M0`, `M1`, `TRESET`, `ENABLE_TPULSE` and `POLARITY` slow control signals are generated by this IC and shifted to the 2.2 V level as desired by the chip by a CMOS level shifter. Another possibility to avoid the transmission of CMOS signals through the long cables would have been to convert them to differential LVDS and reconvert them on the Intermediate board. This option would have needed many pins on the cables, as per each CMOS signal, two LVDS pins would have been needed. This option was chosen for two signals only, the `SHUTTER` and the switching signal for the multiplexer. Those two need to be fast and require a defined timing. The disadvantage of the option with the I2C expander is that the signals generated by this device can only be changed by the I2C network, which operates at most at 400 kHz, while for the shutter, or the LVDS signal, a precision to a clock with about 100 MHz is required. For powering the Timepix chips on this Intermediate board, the HDMI cables cannot provide enough current. Therefore, the connection of an external power supply is mandatory for the Intermediate board V12. In Figure 4.12a, the soldering pads on the top side of the board are connected to power cables, where two power networks are interconnected. The back side of the board,

see Figure 4.12b, holds the same 40 pin connector as the other Intermediate board to connect single chip carriers or octoboards. In case of the V12b board, there are two additional four pin connectors for the high voltage for the InGrids.




(a) Top side with HDMI connectors.

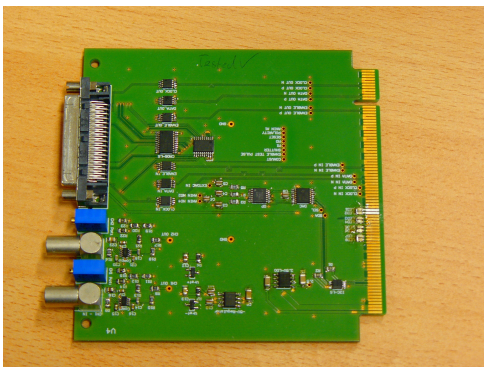
(b) Bottom side with 40 pin connector.

Figure 4.12: Intermediate board V12a with HDMI connectors for the SRS readout systems.

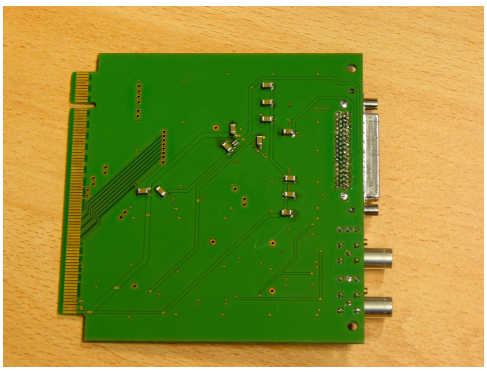
### 4.2.4 Adapter cards

The two different adapter cards to the SRS FEC are depicted in Figure 4.13 and Figure 4.14. As can be seen on the top side images, the VHDCI version holds more ICs, as it has to provide more functionality compared to the HDMI version. This is the case, as the HDMI version has most of the functionality implemented on the Intermediate board. An additional feature of the VHDCI adapter card are the two LEMO connectors. Each of them is connected to a discriminator, of which the thresholds can be regulated by potentiometers. So a user can connect for example scintillators, transmit the two signals from the discriminators to a coincidence logic in the FPGA and use it as trigger for the `SHUTTER` signal. The other ICs are similar to the ones on the ML605 adapter card: The ADC and DAC are controlled by I2C to generate and monitor analogue voltages. LVDS drivers buffer the differential signals, the CMOS control signals are level shifted from 2.5 V from the FPGA to 2.2 V for the Timepix chip and sent through the VHDCI cable, which therefore cannot be longer than a few meters, but has many pins. On the back side (Figure 4.13b), the lines for the powering of the ICs and the 3.3 V to the Intermediate board can be seen.

Contrarily, the HDMI version only sends few signals to the Intermediate board. There are the LVDS drivers and the I2C extender to drive the signals over a cable length of up to 25 m. Also some power for the ICs on the Intermediate board is provided. The lines can be seen on the back side in Figure 4.14b. There is a 3.3 V and a 2.5 V network, where the later voltage is generated by an Low-Dropout Regulator (LDO), the only IC on the back side. For the arrangement of the different signals on the HDMI cable connectors, see Section 4.2.5. The two LEMO connectors on the adapter card are directly connected to FPGA pins, they can be used for multiple purposes, for example for an external trigger signal. In the current configuration, both of them provide the `SHUTTER` signal. An external trigger can be connected to a LEMO connector on the front side of the FEC.

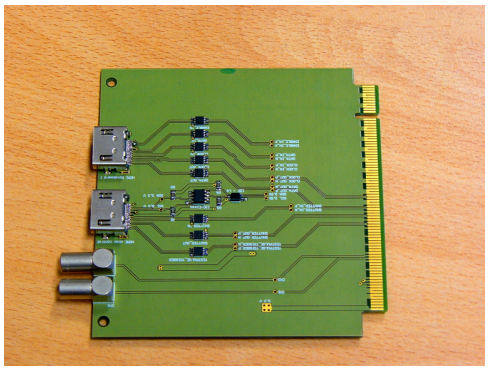


(a) Top side with VHDCI connector and ICs.

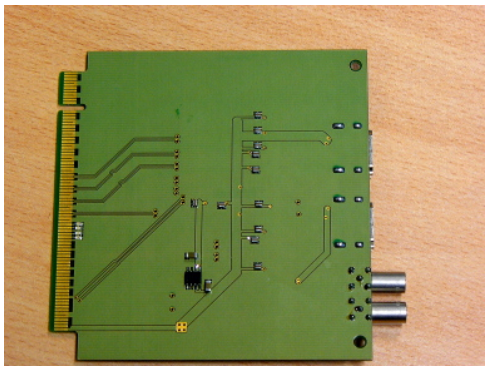


(b) Bottom side.

Figure 4.13: Adapter card for the SRS-based readout with VHDCI cable.



(a) Top side with HDMI connectors and ICs.



(b) Bottom side.

Figure 4.14: Adapter card for the SRS-based readout with HDMI cables.

### 4.2.5 HDMI cables

The design of the HDMI-based SRS Timepix readout aims to achieve a cable length of about 25 m between the system and the detector. For that purpose, a new scheme of signals transmitted through the cable had to be developed. The VHDCI cable, which was used before, provided many pins, but could only be short, as analogue and CMOS signals were transmitted. This scheme is prone to noise and to the decrease of the signal voltage level due to the resistance and capacitance of the cable. Before the introduction of a new scheme of signals through the cable, the signals which are needed by the chip in any case have to be emphasised. In Table 3.1 in Section 3.1.1, all in- and output signal of a Timepix chip were shown. Not all signals are necessarily needed to operate the chip, some are only necessary for special features. Table 4.1 shows the I/Os, which are necessary to operate the Timepix chip. The supply voltages are not included, as they are directly provided by the Intermediate board. Note, that the `POLARITY` and `P_S` signals can be tied to either high (2.2 V) or low (0 V) in general, depending on the detector design. The parallel readout mode of the Timepix chip is not compatible with the goal to achieve a long cable length, as it requires 32 CMOS signals. Hence, `P_S` is tied low directly on the chip carrier. In Section 3.1.4, we have seen that some signals require an exact timing, which needs to be as precise as the `FCLOCK` frequency. For that reason, those signals cannot be produced on the Intermediate board from the I2C network, but necessarily need to be transmitted though the cables. By design of the Timepix chip, those signals are provided and accepted as LVDS, which allows a noise free propagation over long distances. The signals are `ENABLE_IN`, `CLOCK_IN`, `DATA_IN`, `DATA_OUT` and `CLOCK_OUT`, each as `P` and `N` type, as LVDS is bipolar. The CMOS type `ENABLE_INC` is inappropriate and only used on the chip carrier between the chips in a chain. The `ENABLE_OUT` signals does not need to be sent back to the readout, as it is just needed by a Timepix chip to indicate the start of the data stream. The same holds for the `CLOCK_OUT` signals. However, if the readout has to sample the data from the chip encoded in the `DATA_OUT` signals, the clock signal is needed. Hence, in our design, there are five LVDS pairs, which necessarily have to be placed on wires inside the cable between readout and detector.

| Signal name | Type | Route | Description |
|---|---|---|---|
| ENABLE_INC | CMOS | Input | Mandatory, can be replaced by the ENABLE_IN LVDS signals. |
| PENABLE_IN<br>NENABLE_IN | LVDS | Input | Mandatory, can be replaced by the ENABLE_INC CMOS signal. |
| ENABLE_OUTC | CMOS | Output | Mandatory only inside a chain of chips, not to the readout, can be replaced by the ENABLE_OUT LVDS signals. |
| PENABLE_OUT<br>NENABLE_OUT | LVDS | Output | Mandatory only inside a chain of chips, can be replaced by the ENABLE_OUTC CMOS signal. |
| PFCLOCK_IN<br>NFCLOCK_IN | LVDS | Input | Mandatory. |
| PFCLOCK_OUT<br>NFCLOCK_OUT | LVDS | Output | Mandatory. |
| PDATA_IN<br>NDATA_IN | LVDS | Input | Mandatory. |
| PDATA_OUT<br>NDATA_OUT | LVDS | Output | Mandatory. |
| DOUT<0:31> | CMOS-HiZ | Output | Only for parallel readout. |
| RESET | CMOS | Input | Mandatory. |

| Signal name | Type | Route | Description |
|---|---|---|---|
| SHUTTER | CMOS | Input | Mandatory. |
| M0 | CMOS | Input | Mandatory.. |
| M1 | CMOS | Input | Mandatory. |
| P_S | CMOS | Input | High: Parallel Readout. Low: Serial Readout. |
| POLARITY | CMOS | Input | High: Pixel is set to collect positive charges (holes). Low: Pixel is set to collect negative charges (electrons). |
| ENABLE_-TPULSE | CMOS | Input | Mandatory. |
| | | | |
| EXTDAC_IN | Analogue | Input | Feature: External DAC input to set any of the 13 DACs. |
| TEST_IN | Analogue | Input | Mandatory for calibration. |
| DAC_OUT | Analogue | Output | Feature: Analogue buffered output to measure one of the 13 DACs voltages output. |

Table 4.1: Timepix in- and output signals, necessary for the operation.

The three analogue signals `EXTDAC_IN`, `TEST_IN` and `DAC_OUT` cannot be propagated through a long cable, because of the voltage drop. They are converted to digital signals on the HDMI Intermediate boards. It holds an ADC to read the analogue voltage from the chip and a DAC to generate the `EXTDAC_IN` and the two levels for the test pulse multiplexer connected to `TEST_IN`. Those ICs are controlled by I2C, which is an elegant solution, as it only needs two signal (data and clock) which can be connected to pins of the FPGA and the line can be extended to even hundreds of meters.
There is also the possibility to generate CMOS signals with a so called I2C expander IC. However, the change of the output signals of this device is limited by the I2C frequency. For the `M0`, `M1`, `POLARITY`, `RESET` and `ENABLE_TPULSE` signals, this is not critical, as they can be set to the desired value a long time before a Timepix operation starts, see Section 3.1.4. The `SHUTTER` signal needs the same exact timing as the LVDS signals mentioned before. As the `SHUTTER` signal is of CMOS type, it cannot be propagated through the cables. For that reason, it is sent out by the readout as an LVDS pair and converted to CMOS on the Intermediate board by an appropriate IC. The same holds for the signal that controls the switching of the multiplexer for the test pulses.
To summarise, for a proper operation of the Timepix chip over long distance cables, at least the following number of wires necessary: 14 LVDS lines and two I2C lines.

High definition multimedia interface (HDMI) is a standard for the transmission of audio and video, which was developed by a consortium of consumer electronic manufactures. The goal was to digitise the existing analogue video formats to achieve a copy-protected format. The signal transmission cables, which have also been developed and standardised within this campaign, provide features, which are also useful in the context of Timepix readout. The HDMI cable, a digital version of the analogue RGB video, consist of at least four shielded twisted pair cables, depending on the version. These cables are meant for the transmission of the red, green, blue and clock channel in HDMI as differential signals. In addition, there are other lines, which are meant for I2C, command and control signals and power. The cables come in different versions and connector types, but each with 19 pins, of which five are for the shielding. The connector types are named from A to E and have different shapes and sizes. The most commonly used one, which is also the only one to work reliably for cables longer than 5 m is type A. The different versions are labelled from 1.0 to 1.4 and recently 2.0. Partly, there are subcategories like 1.4a or even 1.3b1. In order to fulfil the HDMI requirements, cables have to pass tests like a measurement of

the eye diagram[2] intra-pair skew, inter-per skew, far end crosstalk, attenuation, differential impedance, isolation resistance, cable resistance, current capability and dielectric strength. Since HDMI 1.3, there is an additional classification, which is also interesting from the physics point of view: Category 1 cables, labelled as "Standard", have to fulfil less stringent limits and are tested at 74.5 MHz, while Category 2 cables ("High Speed") have harder requirements and are tested at 340 MHz. The values for the physics parameters are listed in Table 4.2. On the market, one will never find those parameters listed on the packing of a cable. Sometimes they are labelled "Standard" or "High Speed", but most of the time, the physics parameters are difficult to identify. On the internet, test reports of some special cables can be found (e.g. `http://www.comoss.com/ref/Test-Report/HDMI/HDMI-3M-test-report.pdf`) and there are commercial test systems available. A short summary of the HDMI history, versions, cable types and compliances can be found in [143]. Since HDMI 1.4, an additional twisted pair is available for the "HDMI with Ethernet" cable to connect devices with a data transfer rate of up to 100 Mbits/s.

| **Parameter** | **Category 1** | **Category 2** |
|---|---|---|
| Intra-pair skew | 151 ps | 112 ps |
| Inter-pair skew | 2.42 ns | 1.78 ns |
| Far end crosstalk | $< -20$ dB | $< -20$ dB |
| Attenuation | $< 8$ dB (100 MHz - 825 MHz)<br>$< 21$ dB (850 MHz - 2475 MHz)<br>$< 30$ dB (2475 MHz - 4125 MHz) | $< 5$ dB (100 MHz - 825 MHz)<br>linear with:<br>$< 12$ dB at 2475 MHz<br>$< 20$ dB at 4125 MHz<br>$< 50$ dB at 5100 MHz |
| Differential impedance cable area | $(100 \pm 10)\,\Omega$ | $(100 \pm 10)\,\Omega$ |
| Differential impedance connector and transition area | $(100 \pm 15)\,\Omega$ | $(100 \pm 15)\,\Omega$ |
| $(100 \pm 25)\,\Omega$ for not more than 250 ps allowed. | | |

Table 4.2: HDMI cable requirements.

In case of the Timepix readout with HDMI, the standard itself was not needed, just the cables were used because of their physical features. First of all, the commercial availability of a relatively cheap cable with five twisted pairs lead to the choice of this cable. Moreover, it has two lines desired for I2C, a power line, is designed for frequencies in the 100 MHz region (as needed by the Timepix chip), well shielded and provides features desired by a propagation of LVDS signals through the twisted pair lines as the intra-pair skew (difference of the propagation delay between the two cables of the pair) is only a small fraction of a 100 MHz clock period. A drawback, on the first glance, is the low number of only 19 pins. For that reason, a single HDMI cable is not enough to host all signals of one Timepix chip. When looking more into detail, it is an advantage to use two cables, in case the different signals are distributed in a smart way. Table 4.3 shows, how the signals of the Timepix readout have been shared between two HDMI cables. Cable one is called the `Data` cable, as it holds all LVDS signals of the Timepix chip, while cable two, the `Slow Control` cable, holds the I2C signals (SCL and SCA) and LVDS signals to be converted to CMOS on the intermediate board. Additionally there are voltages and ground lines.

[2] The eye diagram measurement is a method of telecommunication with an oscilloscope in order to measure several properties of data transmission. It is achieved by sampling the digital signal from the receiver repetitively by triggering on the system clock and overlaying the images on the screen. From the analysis of the overlying waveforms, the duty cycle, synchronisation with the system clock, noise, over- and undershoots and other properties can be extracted.

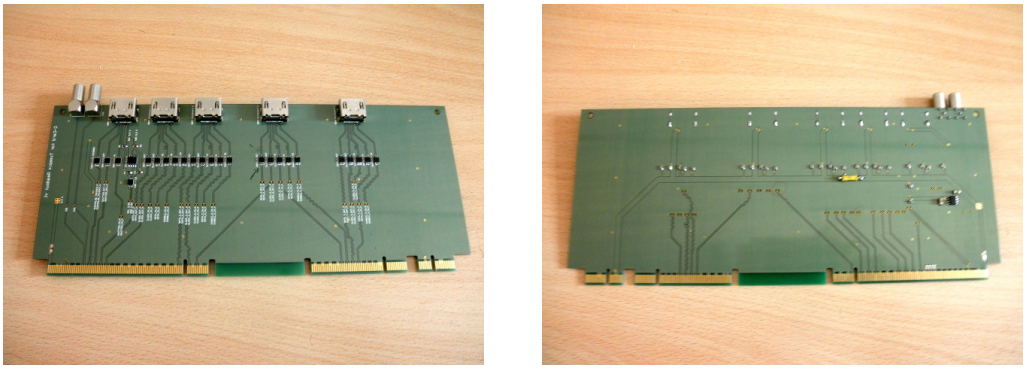
| Pin | Signal name from HDMI 1.4 with Ethernet standard | Timepix signal `Data` cable | Timepix signal `Slow Control` cable |
|---|---|---|---|
| 1 | TMDS Data2+ | DATA_OUT_P | Testpulse_trigger_P |
| 2 | TMDS Data2 shield | GND | GND |
| 3 | TMDS Data2- | DATA_OUT_N | Testpulse_trigger_N |
| 4 | TMDS Data1+ | CLOCK_OUT_N | SHUTTER_OUT_N |
| 5 | TMDS Data1 shield | GND | GND |
| 6 | TMDS Data1+ | CLOCK_OUT_P | SHUTTER_OUT_P |
| 7 | TMDS Data0+ | CLOCK_IN_N | SHUTTER_IN_N |
| 8 | TMDS Data0 shield | GND | GND |
| 9 | TMDS Data0- | CLOCK_IN_P | SHUTTER_IN_P |
| 10 | TMDS Clock+ | DATA_OUT_N | 3.3 V I2C |
| 11 | TMDS Clock shield | GND | GND |
| 12 | TMDS Clock- | DATA_IN_P | 3.3 V I2C |
| 13 | CEC | 3.3 V LVDS | GND |
| 14 | HEAC+ | ENABLE_IN_N | 2.5 V |
| 15 | SCL | GND | SCL |
| 16 | SDA | GND | SDA |
| 17 | HEAC shield | GND | GND |
| 18 | 5 V power | 3.3 V LVDS | GND |
| 19 | H EAC- | ENABLE_IN_P | 2.5 V |

Table 4.3: Pinout of the Timepix signals on the HDMI cables of the readout system.

As can be seen in Table 4.3, the `P` and `N` types are interchanged on the + and - pins of the HDMI twisted pairs for some LVDS signals. This is the case due to constraints on the Intermediate and adapter PCB layout to simplify the routing there. The signals hold the same name as on the Timepix pad. On the `Data` cable, the additional power of 3.3 V is evident. It is the supply voltage for the LVDS drivers on the Intermediate board. The reason, why this voltage is provided from the readout is electrical safety. The Timepix chip can only receive or send LVDS signals, when the readout is powered, otherwise the LVDS drivers are blocked. In case of an overload during mounting or handling, the drivers protect the chip. The same holds for the protection of the FPGA in the other direction. Also, the I2C ICs on the Intermediate boards are powered by the 3.3 V I2C net from the adapter board through the `Slow Control` cable, such that they are disabled, when the readout is off. The 2.5 V network supplies other ICs on the Intermediate board, for example the multiplexer, such that all of them are off, before the readout is powered. In case only one of the two cables is connected, only the components controlled by that cable are powered. From Table 4.3, it can also be seen that the `SHUTTER` signal (`SHUTTER_IN_P/N`) is differential. There also is a `SHUTTER_OUT_P/N` twisted pair to transmit the `SHUTTER` signal to the readout, in case an external shutter is connected to the Intermediate board. The `Testpulse_trigger_P/N` signal is the one for the test pulse multiplexer to switch between the two reference voltages. The sharing of signals between the two cables has been selected carefully to achieve that electronic safety feature. For larger systems, the separation of `Data` and `Slow Control` pays out again, as can be seen in Section 4.2.6. The appropriate cables for the setup are at least “High Speed” HDMI of version 1.4 or higher with Ethernet for the `Data` cable and at least “Standard” HDMI for the `Slow Control` cable.

### 4.2.6 System for many chips

To increase the number of chips, which can be read out with a single FEC, the adapter card was extended. As all chips connected shall be operated simultaneously, a single `Slow Control` HDMI connector is sufficient. Only the number of connectors for the `Data` cables was increased from one to four. This is the maximum achievable by the number of PCI connectors to the FEC. Hardware-wise, the PCB design for the data treatment could be copied, see Figure 4.15. The rest of the changes to handle more data was implemented in the FPGA firmware. With this design, 32 Timepix chips on a large Intermediate board can be operated in parallel with a single FEC. Such an Intermediate board was designed for the test beam with the 96-InGrid module, see Section 4.3.2. Using the scalability of the SRS, several FECs can be operated in parallel. They have to be connected by a Gigabit ethernet switch, each with its own IP, to the DAQ computer. By this design, an arbitrary number of chips can be read out.



(a) Top side with HDMI connectors and ICs.

(b) Bottom side.

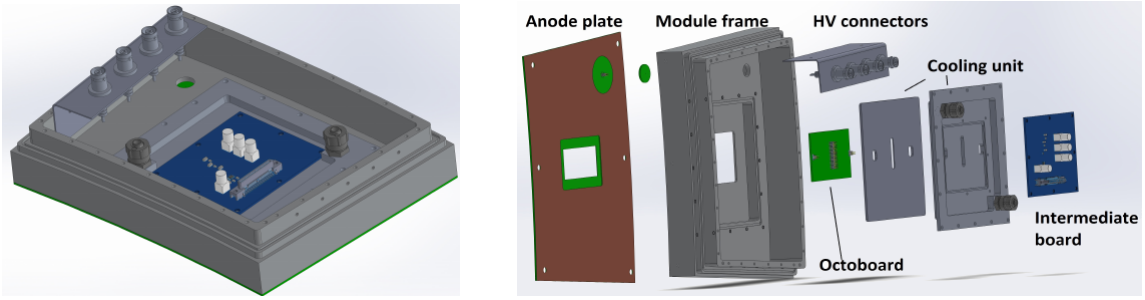
Figure 4.15: C type adapter card for the SRS-based readout with HDMI cables.

## 4.3 Pixel-TPC modules

Two module types for the LP TPC at DESY (see Section 3.8) were constructed to demonstrate the feasibility of a Pixel-TPC. As a first step a module for one octoboard and finally a module for up to 96 InGrids, of which several were produced. The design of the modules was carried out by Master and Bachelor students and their work will shortly be presented here.

### 4.3.1 8-InGrid module

This section summarises the work of Robert Menzen [144], who used the Computer-Aided Design (CAD) software `SolidWorks` to designed a module for the LP which can host one InGrid octoboard. Figure 4.16 shows the 3D model. In addition, a module for an octoboard of bare Timepix chips with GEM gas amplification was developed, which will not be discussed here. On the left side, in Figure 4.16b, an exploded view of the module can be seen with all the different components. On the very left, there is the Intermediate board, which is an earlier stage version of the VHDCI-based board. The module was read out by the intermediate version of the VHDCI-based SRS readout shown in Figure 4.10. As the Timepix chips produce about 1 W of heat each, a cooling system was also included in the module. The cooling pipes for water are embedded in the support structure for the octoboard. The




(a) Isometric view.

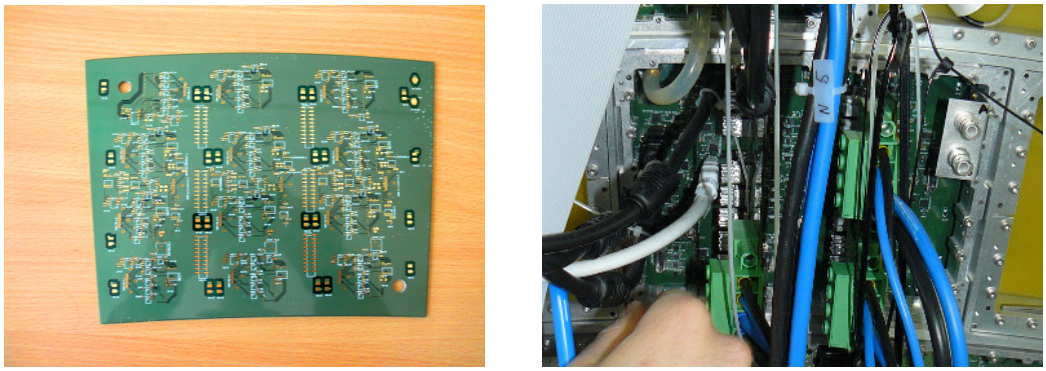
(b) Exploded view.

Figure 4.16: DAC drawings of the 8-InGrid module, from [144].

most massive part is the module frame, which fits the LP endplate. To achieve a uniform potential at the endplate, an anode plate with an opening for the InGrids finalises the design.
More details about how the module was used can be found in the test beam Chapter 7.

### 4.3.2 96-InGrid module

As a final step, the active area on the module was increased to the maximum which is achievable with InGrid octoboards. A module, which can host in total 12 octoboards was designed by Johann Tomtschak [145]. The choice to again use Octoboards justifies through the more simple exchangeability of broken chips. Many conclusions drawn from the production and usage of the first module were included in the design. A way to decrease field distortions from the different position of anode a grid was partly introduced. They followed suggestions from a detailed study [146]. A dedicated power supply was also designed [78]. To read out the 12 octoboards, the design of an Intermediate board was multiplied and optimised, such that four octoboards can be operated by a single `Slow Control` HDMI cable and one data cable per board. Such a combo is then read out by one FEC, as explained in Section 4.2.6. The complete Intermediate board can be seen in Figure 4.17a without the ICs and in Figure 4.17b with all ICs, cables and power supply. Appendix B shows some images of the module components and construction. See the test beam Chapter 8 for how the modules were used.



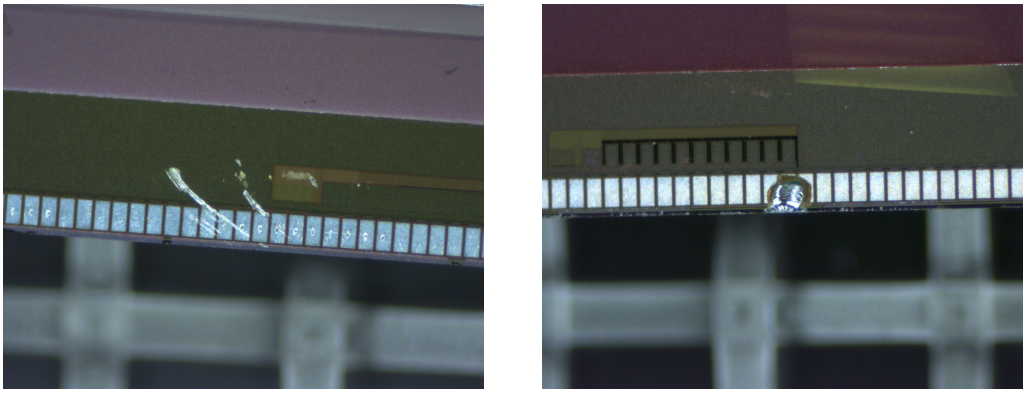
(a) Intermediate Board for twelve octoboards without ICs.

(b) Completely equipped and connected at the LP.

Figure 4.17: Intermediate board for 96 chips

### 4.3.3 Octoboard construction for the 2015 test beam

The biggest challenge during the preparation for final test beam was the construction of the octoboard modules mentioned in the previous section. In total 20 were needed (one completely equipped module with 12 boards and two partly equipped modules with 4 boards each). Additionally, three spare boards were produced. The InGrid chips were glued and wire bonded onto the carried boards by hand in the clean room in Bonn. As the chips are arranged in a chain, where the data is forwarded from chip to chip, a single defect chip prevents the complete board from working. Unfortunately, the fraction of chips, which did not work from the beginning was high. One reason were scratches or defects on the chip surface, which could lead to shorts between wire bonding pads. Two examples are shown in Figure 4.18, which show InGrids in a freshly opened gel pack as it was received from IZM. However, even chips without scratches on the surface showed shorts between bonding pads, which were not even placed side by side. For that reason, the chips were glued at the same time, but only one after the other was bonded and tested, before connecting the next chip of the chain. If a chip at the edge in the $2 \times 4$ matrix was found to be unusable, it was exchanged. For the chips at the edge this is easier than for the ones in the middle. If a middle chip was found to be unsusable, it was bypassed. In case more than two center chips were dead, they were removed by taking the risk to destroy neighbouring chips.



(a) Scratch on the bonding pads.

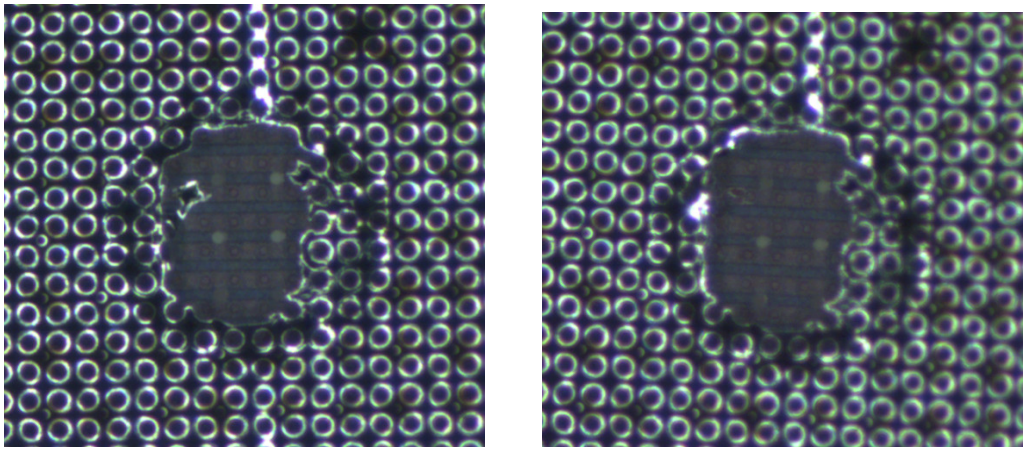
(b) Defect on the bonding pad side of the chip.

Figure 4.18: Defects on InGrids as they arrived from IZM.

Boards with only seven working chips were also accepted. Finally five octoboards with InGrids from the IZM-5 production and 18 boards from the IZM-6 production were built from a total of 231 InGrids. Only a single chip from the IZM-5 production did not work, while from the IZM-6 production, 38 chips had to be exchanged. Only two InGrids were destroyed due to mishandling. After all 23 boards were produced, they were tested with a high voltage of up to 340 V applied to the grid in an argon/isobutane 95/5 gas mixture. As the grid quality for the IZM-6 production was not the best one, some grids could not hold the voltage due to holes in the grid, where an aluminium shred touched the chip surface. Those defects were repaired by hand, which is a very delicate task. An example is shown in Figure 4.19, where in Figure 4.19a, the shred can be seen on the left side of the hole, while in Figure 4.19b, it has been removed. A difference in high voltage stability between chips with a flat grid and those with waves or even a loose grid at the corners could not be observed. In Appendix C, more details about the octoboards can be found.

The InGrids from the IZM-5 production could only withstand a voltage of about 300 V, while the IZM-6 grids could be tested until 340 V which is sufficient to achieve a gas amplification with a single electron

detection efficiency close to 100 %. The IZM-5 chips began to spark at the edges and outside the sensitive area. This could be due to the SU-8, which attracted water during an incorrect storage. The chips were put in a dry nitrogen atmosphere, which only slightly improved the performance. However, at the end of the test beam, they could be operated at the same voltage as the other InGrids. Such effects were also reported by other users of InGrids from the IZM-5 production [147].



(a) Grid hole with a shred touching the chip surface.

(b) Repaired hole in the grid of an InGrid.

Figure 4.19: Repair of a hole with a shred connecting chip and grid.

## 4.4 Data aquisition software

The computer program, with which the user can control and read out the Timepix chips via the readout system was also developed within these projects. It is based on a skeleton developed by Christian Kahra from the University of Mainz and called Timepix Operating Software (TOS) or often just DAQ software in this thesis. Written in C++, is is modular and can read out an arbitrary number of chips. The communication with the FECs is provided by an Ethernet socket based on UDP. As will be seen in Section 5.1, the firmware on the FEC FPGA only supports the basic functions of the Timepix chips. All more advanced procedures, which consist of sequences of this basic functions, are implemented in the software. A detailed description how to operate the software can be found in [142]. Describing the software in detail would clearly go beyond the scope of this thesis. Hence, only some of the features are listed here:

- Set the Timepix chips into reset state.
- Load, store and manipulate files which hold information about he DACs, matrix and threshold matrix of each chip.
- Set the DACs, matrix and threshold matrix in the chips.
- Optimise the THS value of each chip by a THS optimisation.
- Generate the threshold matrix by a threshold equalisation.

- Calibrate the chips concerning the measure of the time walk effect, the conversion of `TOT` counts to charge and `THL` DAC value to number of electrons. This can be done completely automated, as a multiplexer and DACs can generate test pulses of variable voltage controlled by the software.
- Check the travelling time of data and clock signal form the readout to the chips and back to avoid bit shifts in the returning data.
- Scan the voltage level of the Timepix DACs (DAC scan), by reading out the ADC.
- Automated data taking with several modes, shutter opening times and data formates.

Multi-threading is implemented in the software. In zero-suppressed readout mode, the theoretical readout rate of the Timepix chip or a chain of chips can be achieved, see Chapter 6. This does not decrease, if for example four octoboards are attached to one FEC. If several FECs are read out in parallel, each FEC is treated in a different thread. Therefore, to hold the maximum readout rate, it is desirable to have a computer with at least as many cores as FECs connected. The data is stored in `ASCI .txt` files in a folder for the run together with all settings. The software was designed to be controlled by command line. Recently, a graphical user interface and also a software to display the data online was designed [148].

CHAPTER 5

# FPGA firmware development

In Chapter 3, the hardware of FPGA boards was introduced. As explained, these devices have to be programmed with code, such that they operate as desired. In Chapter 3.1, the Timepix chip was explained. The aspects described there were introduced in order to understand, which functionalities of the readout system are needed to operate those chips. The function of the FPGA firmware is, to interface the computer running the control software to the Timepix ASIC. So it has to use a standard that can be connected to a computer on one side and provide all the signals the Timepix chip needs for a proper operation on the other side. The next sections explain the general design goals, followed by the choices made to achieve these requirements. Afterwards, the implementation in firmware code will briefly be explained in a more technical way.

## 5.1 Design goals

For the different FPGA boards, the design goals were mostly common. However, certain features were only implemented in a particular system due to the special requirements. There were five main subjects that drove the design:

- Reliability of the firmware
- Hardware requirements
- Readout speed
- Physics needs
- Full functionality of the ASIC

In the following, the details of these subjects will be explained. All these requirements are implemented in the code in different modules explained in the following sections.

**Reliability of the firmware** The steady operation of the firmware is a key component of the design. No operation shall lead to a hanging of the firmware. The data stream has to work in a way, such that the user can trust the information received. Bit shifts in the data have to be avoided. Each bit in the data stream to the ASIC has to be stored at its desired place in the registers. This especially applies to the bits in the FSR and the pixel matrix. Also the communication between the readout system and the PC has to work in a reliable way, such that no information is lost.

**Hardware requirements** The FPGA as an electronic device has to interact with other components provided by the boards in order to fulfil the wide range of demands. Different signal types have to be generated and transmitted via the adapter board to the Timepix chip. Analog signals, which cannot be processed or generated by the FPGA directly have to be treated by other components the FPGA has to communicate with. The same holds for the communication with the PC. For the different readout boards, also the hardware requirements of the different FPGAs have to be taken into account.

**Readout speed** Even though the Timepix chip itself is not designed for a fast and efficient transfer of information from the pixels to the readout, the firmware shall not additionally introduce speed limitations. It hence has to take the data format the chip provides into account to forward the information to the PC as fast as possible. But also the transmission of the data from the FPGA to the PC takes time and hence reduces the readout speed. So also the amount of data sent to the PC has to be minimised.

**Physics needs** The readout is especially designed for the application of the Timepix chip as anode in a gaseous detector. The system itself shall not spoil the capabilities of the ASIC. This in particular affects the timing resolution, which depends on the clock frequency the readout operates the chip at. Other constrains are the possible setup of a final system in a real experiment. In a TPC environment with a magnetic field, the powering of the readout board has to be placed far away from the detector or withstand the field. Also the data transmission to the PC has to span several meters to the counting room.

**Full functionality of the ASIC** All the features the Timepix chip provides shall be accessible with the firmware. First of all, the FPGA firmware has to provide all the signals the chip needs to execute its basic functions. Those are among others: Do a reset of the chip, set the FSR and get back the chip ID, set the matrix, read back the matrix, open or close the shutter, open the shutter for a defined time, read back `DAC_out` signals, set the `EXT_DAC` and generate test pulses. Moreover up to eight chips in a chain shall be handled. More complex functions, which consist of a sequence of the basic ones shall not be implemented in the firmware. The software at the PC shall be responsible to operate the FPGA, such that a sequence of simple operations is executed.

## 5.2 Basic design choices

Clearly, not all of the requirements can be fulfilled at the same time, some are even contradictory. High readout speed could primarily be achieved by a high clock frequency at the Timepix chip. This will however limit the reliability on the data quality. A reliable communication between PC and FPGA would be the Ethernet IP protocol, however this produces a lot of overhead and increases the amount of data to be transmitted. So compromises have to be found to achieve an optimal performance. Some very basic, mainly hardware related choices had to be made in order to start the firmware development. They are again sorted into the five categories mentioned above, but also overlap with the other goals.

**Reliability of the firmware** Standard gigabit Ethernet using the UDP (see Section 3.7.2) was chosen for data transmission between FPGA and PC. This way, the amount of transferred data is not as much as for IP. The reliability of the communication is partly assured as checksums are used and answer packets are sent back for acknowledgement. Completely lost packages however cannot be recovered. An example of such a packet is shown in Figure 3.18. It includes the Ethernet, IP and UDP headers, followed by the user data. Within the user data, an additional 18 byte long header, already proposed

in [141] is implemented. In this header, control parameters for the firmware are communicated, see Table 5.1. One of these parameters induces a complete reset of the firmware module that controls the Timepix chip. So even if a problem in the communication with the chip arises and the firmware hangs, the user can reset the system remotely and does not have to access the FPGA board that could be placed in a restricted area.

| Byte | Signal | Explanation |
|---|---|---|
| 1 | count_pc | Computer package counter. |
| 2 | count_xl | FPGA package counter. |
| 3<br>4 | length<br>length | Defines the number of bytes to be received or transmitted. |
| 5 | timepix_operation | Defines the operation to be performed. |
| 6 | freqency | Reserved for setting the FCLOCK frequency from software. |
| 7 | shutter_opening_time | Defines the time interval length the Timepix chip is active. |
| 8 | num_chips | Tells the FPGA the number of chips in the chain. |
| 9 | chip | Tells the FPGA the chip currently treated. |
| 10 | preload_plus | Delays the counters for data readout and shifts data. |
| 11 | option | Used in debug mode to switch between design option. |
| 12 | undefined | Not used. |
| 13 | undefined | Not used. |
| 14 | disable_chip | Select chips for not being processed. |
| 15 | i2c | Holds information for the I2C modules. |
| 16 | i2c | Holds information for the I2C modules. |
| 17 | i2c | Holds information for the I2C modules. |
| 18 | control_output | can be used for debug output. |

Table 5.1: 18 bytes Timepix control header. This header is added after the UDP protocol header and holds information to control the Timepix chip. More details can be found in [141].

The data returning from a single Timepix chip or octoboard is phase shifted with respect to the clock inside the FPGA due to the signal propagation time. In the case when the returning data signal edge is synchronous to the internal clock, small variations in the setup can lead to sampling errors for some parts of the data. To avoid this malfunction, the user has the possibility to shift the returning data in steps of 1/5 of the clock period. So in software, routines can be implemented that check the data quality. The user can then act and reverse the accidental bit shifts. A more advanced technique would be to use the clock returning from the chip to sample the data, but this has not been implemented as the other method works sufficiently well and such a method would need additional programming efforts, resources and testing.

**Hardware requirements** All the readout boards provide gigabit Ethernet connectivity. The Xilinx ISE environment has pre-defined firmware modules, so called cores, to support this link. The desired LVDS and CMOS signals can also be generated directly at the FPGA I/Os. All analogue signals have to be generated or analysed by external components on the adapter boards. It was decided to use the I2C standard to control these components. The shutter signal that triggers the data acquisition in the Timepix chip can be controlled directly from an external source via a LEMO plug on the Intermediate board. But as default, the firmware controls this shutter signal and takes the external source as a trigger.

For suitability in experiments, choices had to be made on the design of the readout. The computer and power supply have to be several meters away from the system for radiation protection and influences by strong magnetic fields. For reasons of costs, a dedicated board with the FPGA directly next to the ASICs could not be designed. Hence, available boards were used and the chips have to be connected to the boards via cables. As the best solution, HDMI was chosen (see Section 4.2.5), as those cables provide enough signal lines, a good shielding and are commercially available.
The requirements of the different FPGAs and readout boards did not allow to develop a firmware which is compatible to all systems. As far as possible, the same modules were used. But especially for the modules that have a close connection to the hardware, custom designs had to be developed. It was not possible to implement switches, which select between the different options, as in this case the complete logic for all options would have to be present inside the FPGA when it is programmed. Even a single design is already large and time critical. For the maintenance of the code, this is clearly a drawback that could not be avoided.

**Readout speed** Three different ways to treat the data from the chip to the FPGA are implemented in the firmware.
The most simple one that was already used in [141] is, to just pipeline all data from the chip via Ethernet and to the PC. From the FPGA side, this is the fastest way to forward the data. However for the Ethernet, this results in a large load, as even the data from pixels not hit is transmitted. Due to the limitation of data throughput, the readout rate is not at the maximum. Independent of the number of hits $N$, 917504 bits have to be transmitted.
The second method compresses the data from the chips and only transmits the real information to the PC. For every pixel hit in the chip, the x- and y-position in the matrix and the real pixel value is collected. The combined information of one pixel is called a hit. The method itself is called the hit-based zero suppression mode, as it reconstructs the value each pixel the Timepix chip has recorded from the data stream out of the ASIC and only forwards the non-zero information. That way, the load on the Ethernet is minimised in a typical physics case, where only few pixels received a signal. But the FPGA needs some time and large memory resources to treat the data. Due to the reduction of data to transmit, this speeds up the readout, if not too many pixels are hit. For one hit, 8 bits for the x-position, 8 bits for the y-position and 14 bit for the counter value have to be sent. There is an addition of 2 bits, as the internal FPGA memory cannot handle 30 bit, but only 32 bit words. For $N$ hits, these are $N \cdot 32$ bits.
The third method takes advantage of the time needed to read out the chip. It is designed for a continuous data taking. During run time, the FPGA continuously opens the shutter and reads out the chip. The data is stored in the FPGA and sent to the PC in the next readout cycle, such that the theoretically maximum readout speed can be reached. For zero suppression, a dedicated firmware module was developed, which is explained in the following. For the frequency the chip is operated at, 40 MHz has been chosen as the default option. This choice is influenced by the reliability. For some systems also the firmware itself limits this frequency, as the design is as large that timing constrains (see Section 3.4.4f.) do not allow higher frequencies. To increase the time resolution, a second clock can be transmitted to the chip, when the pixels are counting. That frequency was set to 80 MHz. Due to the limited memory resources in the FPGA, the maximum number of hits from one chip, which can be stored in the FPGA are 4096 hits per frame.
Another zero suppression algorithm that was also taken into consideration was the following: First, a binary matrix (black/white matrix) of $256 \times 256$ pixels is sent to the computer to indicate, which pixels were hit. Then in a defined order, the pixel values follow. The number of bits to transmit for $N$ hits in this case is $65536 + N \cdot 14$. This method is called black/white zero suppression. The information

about the black/white matrix is only complete after the pixel matrix of the chips was read out, which is a drawback of this method. The single hit values, in principle, could be sent beforehand.
In Figure 5.1, the number of bits in dependence of the number of hits is plotted. It can be seen that the first method, the non zero suppressed readout always gives the same number of bits, while for the other two methods, the hit-based zero suppression and the black/white zero suppression, the number of bits to send depends on the number of hits. For large occupancies higher 3640 hits per chip, the black/white method is superior to the zero suppressed mode. However, if no pixel is hit, there is a constant data flow of 65546 bits. In case of the typical applications of the Timepix and especially the InGrid, a low occupancy and many empty frames are expected. For that reason only the zero suppression method based on hits was implemented.

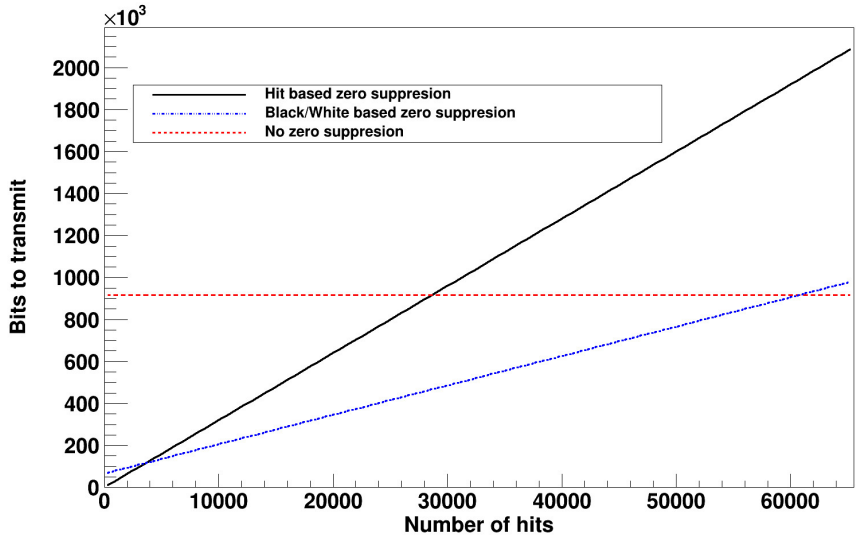



Figure 5.1: Comparison of the different readout modes. Number of bits to transmit in dependence of the number of hits per chip.

The readout speed itself largely depends on the zero suppression. As explained before, the hit-based zero suppression is already faster than just forwarding all data from the chip to the computer. The main driver for the readout speed is the time to readout the complete matrix (one frame) from the chip and this value is fixed for a given FCLOCK frequency. A frame consists of 917504 bits, which have to be packed to the data stream. As the data is sampled with FCLOCK, the same amount of clock cycles is needed, what defines the readout time. Secondly, the transmission time over Ethernet plays a role and here, zero suppression pays off. The third most time consuming process is the treatment and storage of data or hits in the computer. Figure 5.2 shows the readout time per frame for the non zero suppressed readout(4), the hit-based zero suppression(3) and the advanced hit-based zero suppression(1), which uses the readout time of the Timepix chip to send and save the hits meanwhile and hence achieves the maximum theoretical readout speed. For the advanced zero suppression at an intermediate stage, the data storage in the computer was multithreaded(2). The different time intervals for chip readout, sending and storage are also resolved in Figure 5.2.

**Physics needs** A clock frequency of 40 MHz limits the time resolution of the Timepix chip. To overcome this without increasing the frequency for readout and data treatment inside the FPGA, a second clock was produced that runs at 80 MHz by default. This clock is only applied to the chip, when

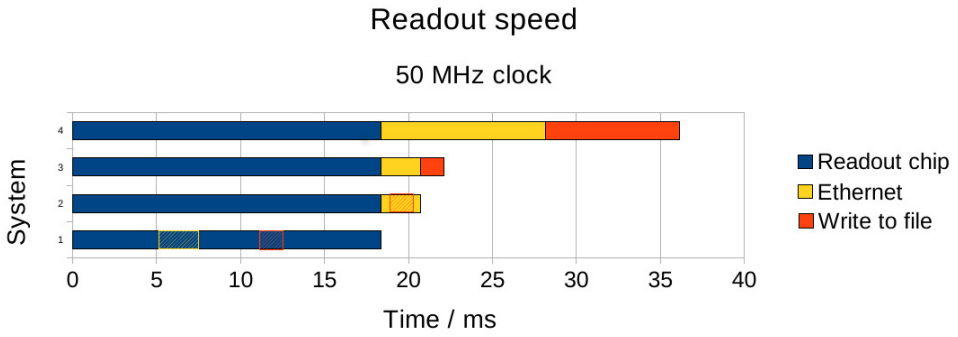



Figure 5.2: Comparison of the different readout times for a frame of a single Timepix chip at an FLCOCK frequency of 50 MHz with the most time consuming processes readout, Ethernet sending and file writing. 4: no zero suppression, 3: hit-based zero suppression, 2: intermediate stage of advanced zero suppression, 1: advanced zero suppression.

the shutter is open to improve the time resolution. Another physics aspect is the polarity of the charge sensitive part of the pixel logic. For gaseous detectors, electrons are collected and hence, the primary option in the design is a negative polarity.

**Full functionality of the ASIC** The Timepix chip provides two ways to read it out. As the FPGA is not directly next to the ASICs, the number of signal lines had to be reduced. For that reason, the serial readout was chosen, despite the parallel readout would improve the readout rate by a factor of 32. The functionality of the chip is reflected from the firmware side. Each of the basic operations is executed by a particular part of the firmware. In the firmware code, all logic for the Timepix operations is concentrated in one file. In this logic a command from the PC executes a sequence that puts all Timepix input signals in a state such that the desired operation is called. Together with the most important firmware logic, this one is explained in the following.

## 5.3 Firmware overview

In the theory part (Section 3.4), where the basics of FPGA programming have been explained, a simple counter logic was shown. There, the code consisted of only one file with one entity and one process in the entity. In principle, several entities can be initialised per file, which is not elegant. Mostly several processes with close connection are included in a file of code. The ports and signals offer to structure the code in a modular way. A file of code therefore will be called a module, which typically holds a single entity with ports and sometimes several processes. Figure 5.3 is a screenshot of the `Xilinx ISE environment`. It shows the hierarchy tree of the firmware for the SRS FEC6 for four octoboards, but the firmwares for the other systems have a similar structure. The different modules of the firmware can be seen in the figure. Each module corresponds to one file that also contains only one entity and its architecture. The name and location of this file is indicated at the end of the line. In the highest level, the project name is written, followed by the FPGA type. In the next level, there are six entries: one is the `fec6_timepix_top`, the others are test bench files for simulation starting with `tb_...`. The first one, also selected in the screenshot, is the top module of the firmware. This module has several submodules, which themselves have submodules and so on. Note that not all submodules are visible, as for some, the view was not expanded.
One special file not being explained is the constraints file `C_Card_HDMI.ucf`. As the name suggests, it

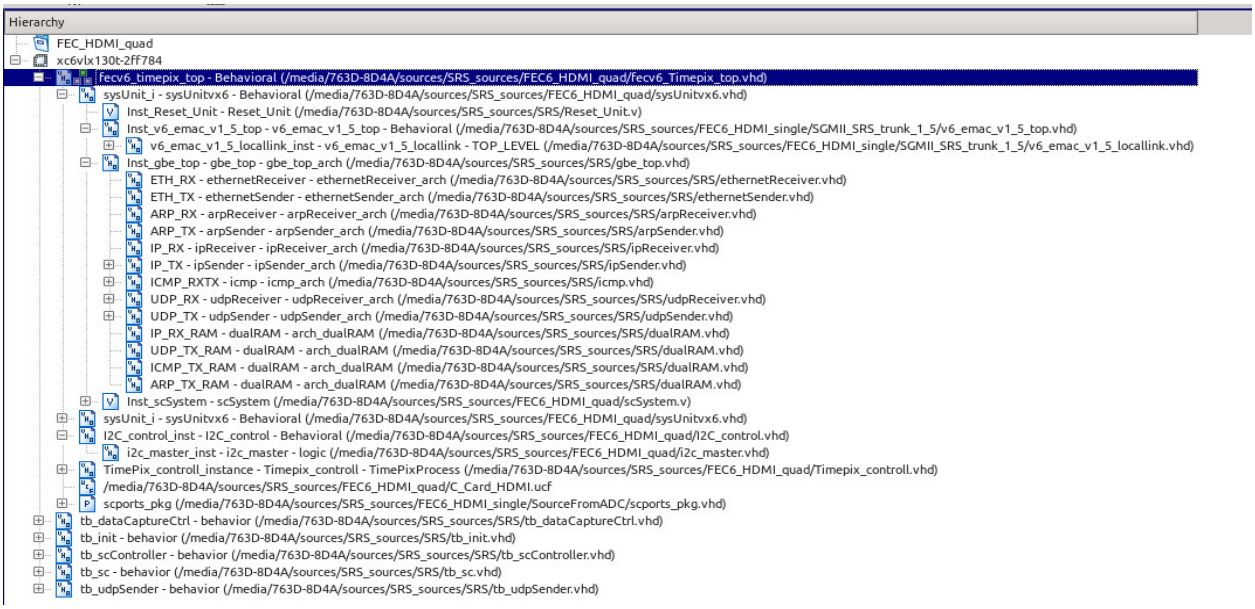



Figure 5.3: Firmware hierarchy of the SRS firmware for four octoboards.

holds information about the type C adapter card. In this file, all connections of the FPGA to the outside world are defined as for example on which PCI pin (where the type C adapter card is connected) of the FEC the clock signals to the Timepix chip is provided. Additionally the file specifies constrains for clock networks and the placement of certain logic components into the FPGA resources.

## 5.4 Firmware modules

In the following, some of the firmware modules are explained. The selection contains only the most important ones and at higher levels of the hierarchy. As the modules are interconnected, they have many signals, which are interchanged between them. Each module consists of one entity, which can be seen from the outside as black box with all the ports. For each module, the graphical display, as already used in Section 3.4 for the counter entity is shown in Appendix A. Only an overview of the operation performed in the architectural part of the entity is given. All the signals at the ports of the entity are explained in a table. Because of the large number of ports, those tables are also provided in Appendix A and the reader is advised to look them up there. However, most signals are self explaining by their name.

### 5.4.1 fec6_timepix_top

In Figure A.1 in the appendix, a graphical representation of the entity `fec6_timepix_top` is depicted. As shown in Section 3.4.1, the entity description contains all in- and output signals, while the behaviour or structure is defined in the architectural part of the code. All in- and output signals of the entity are explained in Table A.1.

**Architectural behaviour** The main task of this module is to combine the signals of the several subcomponents. As it is the top component of the firmware, the different subcomponents have completely different tasks. However, they are also interconnected through this module. `fec6_timepix_top` contains all connections to the real world as in- or outputs. It is for example the first place, the signals from

the chip or the on-board LEDs can be accessed. Therefore, there are the following processes performed in this module:

- Shifting of incoming data by multiples of 5 ns.
- Assignment of unused signal, e.g. `SELF_RSTN <= '0';`.
- Transformation of the bipolar LVDS signals to `std_logic` signals that can be handled in the FPGA or the other way around by using output or input buffers (OBUFDS/IBUFDS).
- Logic to let an LED blink to indicate that the system is in operation.

### 5.4.2 sysUnitvx6

In Figure A.2 and Table tab:sysU in the appendix, the entity `sysUnitvx6` is depicted together with an explanation of the signals in the table. The behaviour is explained in the following. This module is part of the SRS common code. It was modified and not all of its functionality was used.

**Architectural behaviour** The `sysUnitvx6` module is a key component of the SRS common code. As its name suggests, it is the module that provides the system functionalities. In the SRS design, it is connected to the readout modules through the top module by the signals starting with `ro` (ReadOut). Those are not used in the firmware designed for the Timepix chip, as the needs are different. Instead, the `sysUnitvx6` module was modified to provide a connection between the Timepix readout module and the system functionalities.
The only process this module contains is the clock generation. First, the `CLK200_P/CLK200_N` signals from the external oscillator is combined to an internal signal called `CLK200` running at 200 MHz by an IBUFGDS, a buffer for global signals, especially clocks. This is the fastest clock running inside the FPGA, which generates the slower clocks. It is, among others, used as the input signal of a Digital Clock Manager (DCM) [149] in `sysUnitvx6`. A DCM has been used, despite it is not the most advanced mode to multiply and divide clock signals. A PLL and a Mixed-Mode Clock Manager (MMCM) [150] have been tried as well. However, the timing of the design degraded, when these components were used or the Timepix clock at 40 MHz was not as stable as with the DCM. More precisely, a DCM_PS is used, as the option of phase shifting (PS) of the output clocks is used, when a FEC is in slave mode. This way, phase alignment between FECs is possible. Besides its feedback clock, the DCM produces a clock multiplied by 2 and divided by 5, which is the 80 MHz clock and a clock divided by 5, which is the 40 MHz. All output clocks are buffered in a BUFG before they are used any further. The 40 MHz clock is the largest network in the FPGA, as it drives the whole Timepix readout modules. From the 80 MHz clock, another 10 MHz clock is generated by a division by 8 in a BUFR.
Besides its own process, sysUnitvx6 has the following subcomponents:

- `Reset_Unit`: In this module, the general reset on start-up of the FPGA is generated, which is used in many other modules.
- `V6_emac_v1_5_top`: The top module of the Ethernet core is explained in the following.
- `gbe_top`: The top module of the SRS common code used to analyse the Ethernet packages is explained in the following.
- `scSystem`: This module and its subcomponents provide system parameters.

### 5.4.3 V6_emac_v1_5_top

**Architectural behaviour** `V6_emac_v1_5_top` is the top component of a core provided by `Xilinx`, the `Virtex-6 Embedded Tri-Mode Ethernet MAC Wrapper`. It takes care of the implementation of the gigabit Ethernet into the design. A documentation of this core, also including its subcomponents, of which only one is expanded in Figure 5.3, can be found in [151]. In this user guide, all in- and output signals and the behaviour are explained.
In the appendix in Figure A.3, a graphical representation of the entity `V6_emac_v1_5_top` is shown.

### 5.4.4 gbe_top

In Figure A.4, a graphical representation of the entity `gbe_top` is depicted. As shown in Section 3.4.1, the entity description contains all in- and output signals, while the behaviour or structure is defined in the architectural part of the code. All in- and output signals of the entity are explained in Table A.3.

**Architectural behaviour** This component is part of the common code provided by the SRS community. It is used to resolve the headers of the UDP layers and analyse the Ethernet packages. For each layer, it has a component for receiving and sending, respectively. This functionality is often used in the Timepix readout. For sending, the whole chain, starting from the construction of the different headers till the packing of data is managed from the `timepix_control` module. Therefore, the entity and its subcomponents needed to be extended. The input signals starting with `tx` and the `waitToSend` signal are used for this purpose. For receiving,the `gbe_top` module analyses the headers and, by the `NotOurFrame` signal, indicates if a Ethnernet package is meant for the particular FEC with its own IP and MAC address. The incoming data of the Ethernet package itself is directly picked up by the `header` subcomponent of `timepix_control`.

### 5.4.5 i2c_control

For this entity, the list of signals can be looked up inTable A.4 and the graphical representation of the entity `i2c_control` is depicetd in Figure A.5.

**Architectural behaviour** On the Intermediate board, which is connected to the Timepix chip carrier, several ICs are controlled with the I2C standard. For the communication, only two signals are necessary: the data signal `sda` and the clock signal `scl`. As explained in Section 4.2.3, an ADC, a DAC and an I2C expander are used. The `i2c_control` module is the interconnection between the `timepix_control` and the `i2c_master` modules. It contains the following processes:

- From the 10 MHz clock, the 100 kHz clock for the I2C standard is generated by a counter.
- A counter logic is used to let an LED blink, which indicates that the I2C clock is running.
- At start-up, a reset of the I2C interface is initiated and after reset the `reset_i2c_done` is set to logic 1.
- In a state machine that gets its condition from `timepix_control` depending on the I2C IC to be communicated with, the address of the component and the command is transformed into `i2c_addr` and `i2c_data_wr` for the `i2c_master` component. The sequences of I2C packages are generated as they are needed by the ICs to perform their operations. The ADC can be read out and the data of the incoming I2C pages is packed into the `ADC_result`, `ADC_ChId`

and ADC_alert signals. An important output signal of this module is op_finished, which indicates that the I2C command called has been executed. As the I2C clock runs only at 100 kHz, but the Timepix readout at 40 MHz, it takes comparably long to execute an I2C command.

### 5.4.6 i2c_master

**Architectural behaviour** The I2C interface is an open source code. i2c_master.vhd [152] from www.eewiki.net has been chosen. It respects the NXP UM10204 I2C-bus specification and leaves the user freedom for clock speed and a convenient way of connection to other modules. For single master systems, as the Timepix readout, this component is recommended by the FPGA programmer community at www.mikrocontroller.net. More information about the module can be found in [152].
For i2c_master, Figure A.6 and Table A.5 in the appendix are the references to look up the list of signals.

### 5.4.7 timepix_control

**Overview** timepix_control is the main component to control the Timepix ASIC. It generates the signals to operate the chip and manages the data read-out from the chip. Together with its subcomponents, it extracts the data from the incoming Ethernet packages, stores data for zero-suppression and controls the gbe_top module for data sending. The subcomponents are:

- Ethernet_header: The additional header for the Timepix operation, see Section 5.2, which does not follow the Ethernet standard, is read out and written. The data and parameters, for example timepix_operation or chip, are extracted and forwarded to timepix_control. The information from the I2C interface, which is the result of the ADC readout, is written into the defined position of the header.
- Serial: The Ethernet MAC provides bytes, the communication with the Timepix chip is bitwise. This component extracts the bits from the bytes by stopping the data stream from the output buffers of the Ethernet MAC as long as all eight bits are extracted from a byte.
- Deserial: For the opposite direction, this component packs the bits from the chip into bytes for the gbe_top module.
- Storage: For the zero-suppressed readout, a dedicated module has been designed. It contains a state machine to read out data from the chip and store it, to transmit the data and to read out and transmit the data of the last frame at the same time. More details are explained in the following. For the large Timepix readout, where each FEC controls up to four octoboards, this component is initiated four times, once for each octoboard. Remember that the FPGA is able to execute all logic in parallel.

For the detailed list of all I/O ports, the reader is referred to Table A.6. In the same appendix, also the graphical representation of the entity timepix_control is depicted in Figure A.7.

**Architectural behaviour** timepix_control mainly consists of a large state machine. The different states are called by the timepix_operation signal from the Ethernet_header module, which extracts this command from the Ethernet package. This command defines, which state is executed. Each state resembles a basic Timepix chip operation, see Section 3.1.3. The software hence can call the different operations directly.

The first process before the state machine in timepix_control is the initiation of counters called rx_counter, tx_counter, i2c_counter and counter. rx_counter, which counts the received bytes, is started by rx_ll_sof_n_0_i, the indicator for the start of an incoming Ethernet package. When rx_counter reached 31, the header information is present inside the FPGA. If notOurFrame indicates that the frame is meant for the specific FEC, tx_counter, i2c_counter and counter start counting. The later two are necessary for internal operation, while the first counter is used to count the bytes for transmission. The packing of an acknowledge signal starts as soon as the incoming package has been analysed. The sending of the return package, however, is delayed, by the waitToSend signal, until the called operation is finished.
In a second process, the output clock to the Timepix chip can be switched in a BUFGMUX between 40 MHz and 80 MHz, synchronisation of the output data, enable and clock signals is performed by ODDRs.
As mentioned before, the state machine with the different Timepix commands is the largest process in this module. It reflects the basic operations of the Timepix chip, as they are explained in the manual [67]. The timepix_operation command is an eight bit word represented by a hexadecimal number. Each number starts one of the following operations:

- "01" (Reset): The Timepix control signals M0, M1, ENABLE_TPULSE and in this state especially TRESET are set for a reset of the chip by changing the outputs of the I2C expander IC. When op_finished from the i2c_control module indicates the termination of the I2C operation, the correct assignment of the control signals at the chip is assured. Then, the Timepix clock is fed through the chip for a few cycles. Afterwards, the control signals are again changed by an I2C command, such that the chip is not in a reset state any longer. Additionally, the ENABLE_TPULSE signal for the Timepix chip is set to logic 0.

- "02" (open shutter manually): After the control signals are assigned as desired by the counting mode of the Timepix chip, the clock, enable and shutter signals are activated.

- "03" (close shutter manually): The control signals are kept in the counting mode and the clock, enable and shutter signals are deactivated. This is sufficient to stop the pixels from counting.

- "04" (start readout matrix): For the readout of the complete pixel matrix, first the control signals are assigned. Then, enable and clock start the data flow from the chip. Together with the deserial module, the data is packed into an Ethernet package. When the first package is full, the clock is stopped, which also stops the data flow from the chip. This command is always executed in a sequence with the two following ones.

- "05" (continue readout matrix): The software proceeds the readout and requests the next Ethernet package of data. The control signals do not need to be assigned again. Until the next Ethernet package is completed, the clock signal is continued to get the data from the chip. Depending on the number of chips connected in a chain, this command is repeated several times from the software until almost all data from the chip is sent to the computer.

- "06" (end readout matrix): The software has noticed that almost the complete data from the chip has been read out and only one last package is missing. It calls this command to receive the last data and disable the enable and clock signal at the end.

- `"07" (i2c reset)`: A special state in the `i2c_control` module is called that sets all I2C ICs in a reset state. The DACs are set to 0 V output voltage, the I2C expander output signals such that the Timpix chip does not perform any operation and the ADC is reset.
- `"08" (i2c expander)`: The outputs of the I2C expander IC can be programmed by the user manually. This command is mainly used to test the functionality of the device.
- `"09" (i2c DACs)`: The software transmits the DAC channel number and the binary value for the output voltage of the DAC channel. Then, the appropriate state is called in the `i2c_control` module to perform the operation.
- `"0a" (start set matrix)`: To set the pixel matrix, first the control signals are assigned. Then, the enable, clock and data signals are started. The data from the incoming Ethernet packages is serialised by the `serial` module. After the first Ethernet package has been decoded and forwarded to the chip, the clock is stopped as no new data is present. This command is always executed in a sequence with the two following ones.
- `"0b" (continue set matrix)`: As the control signals have already been assigned by the previous command, this operation directly starts the serialisation of data in the incoming Ethernet package to forward it, together with the clock, to the Timepix chip. This command is repeated by the software as often as needed to completely set the matrix of all chips in the chain. The software has to provide the correct order of the bits..
- `"0c" (end set matrix)`: When the software sends the last package of data, this command is called to terminate the matrix setting by deactivating the clock and enable signals after forwarding the last bits of information to the chip.
- `"0d" (set DACs write FSR)`: With this command, the DACs inside the Timepix chip are set by writing to the FSR. At the same time, the chip ID is read out from the chip. First, the control signals are set in the correct combination for writing to the FSR. Then, the incoming Ethernet data is serialised and sent to the chip together with the clock and an active enable signal. While the `serial` module is sending, the `deserial` module packs the data returning form the chip, which contains the chip ID, into bytes for the outgoing Ethernet package. To protect the internal DACs from further access, the control signals are set to a different mode at the end of execution.
- `"0e" (readout ADC)`: The incoming Ethernet package holds information about the channel of the ADC that has to be read out. This command calls the state for the ADC in the `i2c_control` module and picks up the data from the IC. The number of the channel read out, the binary information about the level and the alert signal are packed and sent back to the computer.
- `"0f" (test pulses)`: Caused by the `Testpulse_trigger` signal, the multiplexer on the Intermediate board switches between two voltages from the DACs. The user can specify the number of pulses in a range from one to 5000 and the frequency from 10 kHz to 500 kHz. This operation then switches the `Testpulse_trigger` signal from logic 0 to logic 1 as requested.
- `"10" (activate external test pulse)`: The `ENABLE_TPULSE` signal is set to logic 1, as needed by the Timepix chip to accept test pulses.
- `"11" (deactivate external test pulses)`: The `ENABLE_TPULSE` signal is set to logic 0. A reset also sets this signal to logic 0.

- "12" (set preload): In order to phase align the data returning from the chip with the clock inside the FPGA the user can specify a preload or offset value for each of the connected boards. The preload value is an eight bit word consisting of two parts: the highest three bits specify the phase shift. They can be set from decimal 0 to 4. For an increment of one, the data is shifted by 5 ns (one fifth of a 40 MHz clock cycle). The lower five bits can be set from decimal 0 to 31. This number is added to the counters that wait for the data returning from the chip. That way the signal travelling time through long cables from the FPGA to the Timepix chip and back can be compensated.

- "13" (open shutter for defined time): The shutter opening time shutter_opening_time is a 8 bit word in the additional header with the commands for the Timepix chip. It can take values from 0 to 255. After the outputs of the I2C expander IC have been set such that the Timepix chip is in counting mode, the shutter logic start. The shutter is opened for (46 · shutter_opening_time) clock cycles. The 46 has been chosen to access the full range of the pixel counters in the Timepix chip. The maximum number of clock cycles they can count to is 11810, and

$$46 \cdot 255 = 11730 \approx 11810. \tag{5.1}$$

  As the clock frequency is 40 MHz, the shutter can be opened for at most 293.25 µs with an increment of 1.15 µs with this operation. For reasons of a stable power supply during the shutter opening time, the shutter opens not directly after the control signals have been set. Changing these signals causes a larger power consumption of the Timepix chip and a voltage fluctuation. The shutter opens 15000 clock cycles, or 375 µs after the op_finished signal has been received from the i2c_control module.

  If ENABLE_TPULSE is activated, test pulses are sent to the chip as defined in the last test pulse command within the shutter opening time.

- "14" (open shutter for defined time, faster clock): The same logic as in the previous operation is executed, except that the output clock to the Timepix chip is set to 80 MHz. As inside the FPGA and shutter logic the 40 MHz clock is used, the maximum shutter opening time and increment stay the same. So in this operation it is possible that the pixel counters reach their maximum and stop counting, as the clock in the Timepix ASIC is 80 MHz.

- "15" (open shutter for defined time, 256 times longer shutter): The same operation as in "13", but with a shutter opening time of (46 · 256 · shutter_opening_time) clock cycles is performed. The maximum opening time increases to 75.072 ms and the increment to 294.4 µs.

- "16" (open shutter for defined time, 256·256 times longer shutter): For even longer shutter opening times up to 19.22 s with an increment of 75.37 ms this counting mode executes the same code with (46 · 256 · 256 · shutter_opening_time) clock cycles shutter opening time.

- "17" (open shutter with external trigger): Contrary to the operations "13" to "16", the shutter is only opened, when the external trigger signals is active. The counter logic waits exactly at the 15000th clock cycle after the op_finished signal for the ext_tigger signal going to logic 1 for the next time. If an external trigger is received, the shutter is opened for (46 · shutter_opening_time) clock cycles. This is the mode used for data taking at a TPC in a beam test, with the Timepix chip set to TOA mode. The external trigger stems from scintillators

outside the TPC and in the beam. Longer shutter opening times do not exist in this mode, as they are not needed in a TPC mode.

- `"18" (open shutter with external trigger, faster clock)`: To achieve a better timing resolution in the TPC mode, the 80 MHz can be used as sampling clock.
- `"19" (set I2C addresses)`: The user can set the I2C addresses that the firmware uses to communicate with the DAC, ADC and I2C expander on the Intermediate board.
- `"1a" (readout chip, store data in FPGA, zero suppressed output prepared)`: For the zero suppression of data from the Timepix chip, the readout of data from the chip and sending it to the computer has been separated. In this operation, the data is only read out from the chip and stored in the FPGA as hits, see section 5.4.8. First, the control signals are assigned for the transmission of data from the chip, then `readout_matrix_start` goes to logic 1 for a few clock cycles, which starts the treatment of data from the chip in the `storage` module responsible for the zero suppression. If several chips or boards are connected to one FEC, all associated `storage` modules start simultaneously. These modules give back `readout_matrix_stop`, which is logic 1 only during the time the complete Timepix data is requested by `storage` and activates the clock to the chip. After this operation has been performed, the data from the single chip(s) or octoboard(s) is stored in the block Random-Access Memory (RAM) of the `storage` module(s). In this operation the FPGA replies with two packages to the computer. The first one is the acknowledge for the command, while the second one indicates that the readout of the chip(s) or board(s) is complete.
- `"1b" (send data to computer)`: To send the zero suppressed data from the block RAM to the computer, this operation starts a state in the `storage` module that packs the hits in bytes for the Ethernet. The bytes are forwarded to the Ethernet MAC and sent to the computer when a package is complete at the end of this operation. Calling this operation once returns one package of data to the computer. Within the additional header, the software indicates the board and chip number of which the data shall be sent. The number of hits on that particular chip is also transmitted to the computer. From this number, the number of packages and bytes needed to collect all data from that chip is calculated and this operation is recalled as often as needed. Then, the computer can start to request the data of another chip.
- `"1c" (readout chip and send data of last frame)`: The fast readout of zero suppressed data in the `storage` module is controlled by this operation. It is a combination of operation `"1a"` and `"1b"`. The software can request hits from a certain chip that are already stored in block RAM, while the first request starts the readout of new data for the next frame that is stored in a different block RAM. An extra package is sent to the computer when the readout is finished.
- `"others" (nothing)`: In order not to have an undefined state, the `other` command has been set. In this state, nothing is done. All signals to the Timepix chip stay as they were at the end of the operation before.

### 5.4.8 storage

In Figure A.8, a graphical representation of the entity `storage` is depicted. As shown in Section 3.4.1, the entity description contains all in- and output signals, while the behaviour or structure is defined in the in architectural part of the code. All in- and output signals of the entity are explained in Table A.7.

**Architectural behaviour** The `storage` module is a state machine consisting of five states for zero suppressed data handling and a logic to start them. They are explained in the following. The zero suppressed readout is very memory consuming, as up to 4096 hits shall be recorded on each chip[1]. Each hit needs 8 bits for its x-position, 8 bits for its y-position and 14 bits for the pixel value, which adds up to 30 bits. The memory ports can only be specified to 32 bit words. For 4096 hits, this adds up to about 131 kbit of memory per chip. For the fast zero suppressed readout, the double amount of memory is necessary, as the data of the previous frame is still stored, while another frame is recorded. There are four subcomponents of which three are RAMs and one is a Read-only Memory (ROM):

- `TEST_RAM` is a generic single port RAM which is FPGA independent. It initialises a large array which is mapped into block RAM of the FPGA automatically. Due to its size, this memory is mapped into the `RAMB36E1` [153] resources of the FEC6 FPGA. For the 4096 hits on a single Timepix chip, four such block RAMs are needed. In each `storage` module, `TEST_RAM` is initialised eight times, once for each chip of an octoboard. If there are four `storage` modules, one for each board connected, this memory uses 128 of the 264 `RAMB36E1` RAMs or about 50% of the available resources. As there are also other components that use 23 of this type of block RAM 57% of the `RAMB36E1` resources are used.

- `blk_mem_gen_v7_3` is a specific single port RAM generated with the `Xilinx Core Generator` for the particular FPGA. This has been necessary to achieve the amount of memory needed for the fast zero suppressed readout. Within the `Core Generator` wizard, the memory was designed to use the smaller `RAMB18E1` [153] resources, as the `RAMB36E1` block RAM is already used by more than 50% . For a single chip, eight `RAMB18E1` are necessary to store 4096 hits. 12 are used by other components of the firmware. So in total, 268 of the 528 `RAMB18E1` block RAMs (about 50%) are used by the design.

- `row_store`: The counter information of one pixel is a 14 bit word. Due to the serial readout data structure of the Timepix chip, see Section 3.1.4, it takes 3329 bits until the complete information of the first pixel arrives at the readout. A generic dual port memory picks up this data and reconstructs the information of each individual pixel. It is programmed such that is has two address pointers: one for the input data and another one for the output data. So at the same time while data is written to the memory, data from a different address can be read out. Simultaneous read and write from the same address is forbidden. It takes some clock cycles until the output data is available to the outside of the memory. The `row_store` RAM has 256 positions, one for each pixel in a row. At each position, a 14 bit word can be stored, which is the same number of bits as the information inside a pixel. The reconstruction of the content of one pixel, say pixel number `p`, works the following way:
  - The address pointer rotates over the memory for the first time. When it arrives at position `p`, the highest bit of the counter in pixel `p` is also present in the stream from the Timepix chip. This value is written into a 14 bit vector at the highest position. So when the bit was a 1, the vector is `"10000000000000"`. This vector is then written into position `p` of `row_store`.
  - The address pointer rotates over the memory for the second time. By using the second address pointer before the other address pointer points to position `p`, the last value at position `p` is read out. This readout is timed such that when the old vector is present, in this case `"10000000000000"`, also the address pointer for writing points to `p` and the second highest

[1] A limitation had to be introduced because of the limited RAM resources in the FPGA. For higher number of hits per chip in a frame, the zero-suppression looses its benefits and the non zero-suppressed readout should be used.

bit of the counter in pixel p arrives from the chip. This bit is written at the second highest position of the old vector. In case it was a 1, the vector will be changed to "11000000000000" and written to row_store again at position p.

- This procedure is repeated until the second lowest bit from pixel p is stored and the output vector would be "11111111111110" if all bits from this pixel were 1. This vector is then used as address pointer for lfsrLookUpROM. The lowest bit of pixel p is not put into the vector, but directly to the lowest bit of this address pointer. The lfsrLookUpROM then checks, if that pixel counter value, which is a pseudo-random counter number, refers to a non zero real counter value. As has been shown in Section 3.1.2, the pixels do not return the true number of clock cycles they have counted, but an encoded value.

As this process is repeated independently for each row of the pixel matrix, the memory is rewritten each time and called row_store.

- lfsrLookUpROM converts the pseudo-random number value received from the pixels to the real value of counted clock cycles. It is a ROM that has the real value stored at the address with the pseudo-random number value. So when the firmware accesses the content at an address, which is given by the pseudo-random number received from a pixel, the output is the real value for that pixel. As the conversion list holds 16484 numbers, each 14 bits wide, this ROM already needs eight RAMB36E1. Most of the real values, however, are zero.

The first process in storage uses the clock returning from the Timepix chip to let an LED blink. This is currently the only process that uses the returning clock. As an extension of the firmware, the data sampling with the returning clock could be implemented here.
The state machine for the zero suppressed readout begins with the treatment of the start commands from the operations "1a", "1b" and "1c" of the timepix_control module. The case_Dout signal puts the machine into the different states.

- case_Dout = 0 is the reset state, where all counters are set to the initial value and the memories are disabled. If a start signal becomes true, the memory for writing is activated and the write address address_RAM and hit counter hit_counter are set to 0.

- case_Dout = 1 is the state to read out data from the chip and store it in the memory. It keeps the memories activated and starts the preload counter to compensate for delays of data. In the first part of the code, the data is stored in the memories. row_store is used to collect the information of each individual pixel. lfsrLookUpROM converts from the pseudo-random value to the real counter value. In a second part, counters are running that hold the information which bit from the chip is currently processed. The counters are chip_counter from 0 to the number of chips on the board, y_counter from 0 to 255 for the rows of the Timepix chip, b_counter from 13 to 0 for the pixel counter bits and x_counter from 255 to 0 for the pixels in one row. If the real value from lfsrLookUpROM is not zero, the values of the x_counter and y_counter are stored together with the real pixel value as a hit in the TEST_RAM or blk_mem_gen_v7_3. If there are more than 4096 hits on the chip, the memory starts overwriting the first hits. In this case, only the last 4096 hits are stored in the memory. At the end of the readout, case_Dout = 2 is called.

- case_Dout = 2 is a bridge state between readout and transmission. The memories are disabled. In a loop for all chips on the board, the hit counter value of the previous readout is written to the hit_counter_result signal that goes to the timepix_control module. When the first frame is transmitted, this value indicates how many packages the software has to request to collect the

complete dataset. To prepare the memory for the transmission, its address pointer is also set to the hit counter value.

- `case_Dout = 3` reads out data from the chip and transmits the data of the previous frame at the same time. The `useMemoryToWrite` signal switches between 0 and 1 after each readout. It indicates which memory block shall be written to. The other block is read out and the hits are transmitted. The code of the first part for data reception from the chip is similar to the one for `case_Dout = 1`. Then, the same code as in `case_Dout = 4` starts, but both parts run simultaneously. A control signal called `sending` stays 1 while the hits are transmitted. Only after this signal goes to 0, the receiving logic can finish and a new readout cycle can be started. `case_Dout = 2` is called between cycles to rewrite `hit_counter_result`.
- `case_Dout = 4` is responsible for the transmission of hits. Which part of the RAM shall be read out is indicated by the `chip` signal. The software request the data and another state machine starts packing all hits, each with 32 bits, into bytes for the Ethernet package. If a package is complete, the `timepix_control` module can stop and later proceed this operation.

### 5.4.9 ddr2_mem_control

At the time the development of the Timepix readout firmware was advanced on the FEC3, it was unclear which type of FPGA shall be implemented on the FEC6. The FPGA on FEC3, however, has very limited block RAM resources. Even though at that time, only a single octoboard was read out with one FEC, the resources were not sufficient to store the data of all eight chips for zero suppression. For that reason, a special memory controller has been designed to handle the external Double Data Rate Synchronous Dynamic Random Access Memory (DDR2 SDRAM) on the board. Using external DDR2 SDRAM requires a complex logic and an interface to the existing firmware. Additionally, it is not possible to read and write from that memory at the same time. Hence, the fast zero suppressed readout was not implemented on this FEC version. As data is only written to the memory for a very short time during the readout of the chip, see 5.4.8, this readout mode could have been implemented with some changes in the `storage` module. Luckily, the FPGA on the FEC6 came with large block RAM resources, such that the complicated implementation of a DDR memory could be omitted.
In Figure A.9, a graphical representation of the entity `ddr2_mem_control` is depicted. As shown in Section 3.4.1, the entity description contains all in- and output signals, while the behaviour or structure is defined in the architectural part of the code. All in- and output signals of the entity are explained in Table A.8.

**Architectural behaviour** The DDR2 SDRAM memory is only used for the FEC3. It consists of the `ddr2_mem_control` as a top module to interface to the `timepix_control` module without applying too many changes there. The `mig_v3_5` and two First In, First Outs (FIFOs) `FIFO_data_to_DDR2` and `FIFO_data_from_DDR2` are the subcomponents. The FIFOs buffer the input and output data from and to the DDR2 SDRAM running at 200 MHz and do the Clock Domain Crossing (CDC). `mig_v3_5` is the top module of the `Memory Interface Generator` from the `Xilinx Core Generator` that handles the I/O signals to the DDR2 SDRAM hardware. It is explained in detail in [154].
In the first process, the FIFOs are reset. When the reset signal becomes true, the main process to write to and read from the DDR2 SDRAM through the FIFOs can run by using the main Timepix readout clock which is typically 40 MHz. There are two main states, one for read and one for write that themselves consist of two states to access the addresses of the FIFOs. As it takes two clock cycles to write to `FIFO_data_to_DDR2` and this FIFO is read out from the DDR2 SDRAM side by 200 MHz,

the Timepix readout clock must not be faster than 100 MHz for a save operation of the DDR2 SDRAM memory because the `full` signal is not forwarded to `timepix_control` to stop the data flow. For the `FIFO_data_from_DDR2`, this is not critical, as an almost full signal `prog50_full_FIFOfromDDR2` has been programmed, which stops the DDR2 SDRAM memory from sending data with 200 MHz until the slower Timepix readout clock emptied some of the data in the FIFO.

CHAPTER 6

# Basic system verification

During the development of the readout system, the functionality of the Timepix chip was implemented step by step. First, the Ethernet communication between computer and FPGA was established and verified, for example by activating and deactivating an LED on the FPGA board from the computer software. Gradually, more and more complex operations were performed, of which some will be explained in this chapter. Only a single Timepix chip or an octoboard without gas amplification stage were sufficient for those tests.

## 6.1 Set matrix and FSR

To communicate with the Timepix chip, the control signals need to be correctly assigned and the data sent from the computer through the FPGA has to arrive at the chip in correct order and timing, such that for example the matrix or FSR is set correctly. A first hint that the communication between FPGA and Timepix chip is according to the specifications is, when the chips sends back its chip ID when the FSR is set. Figure 6.1 shows the first verification of this step. The image shows a screen shot of the `Chipscope` software, which is part of the `Xilinx` software environment. The tool is used to implement additional code in the FPGA together with the firmware code. The user can specify the signals in the final implementation in hardware he wants to monitor, like with an oscilloscope but inside the FPGA. In the figure shown, there are many signals under investigation, among others the slow control signals `M0`, `M1` and `TRESET`, the fast signals with data to the chip (`pixclk`, `timepix_data` and `timepix_enable`) and the fast signals with data from the chip (`data_in<0>`, `data_in<1>` and `data_in<2>`). The signal names are as in the firmware code. The signals are sampled by `pixclk`, which controls the timing of all signals to the chip. Each time bin in the time line at the top of the screen shot resembles one clock cycle. The user hence can inspect what happens inside the FPGA at every single clock cycle and for example compare to the code simulation or the logic in mind.
At about time bin 230, the control signals for setting the FSR are assigned and `timepix_enable` is going low. Then at about 430, many different operations are started. First the `serial` module at the very top of the image shows activity. It transforms the bytes with data for the FSR to bits, which are sent to the chip (`timepix_data`). At the same time, the `D2` signals goes high, which forwards the continuously active clock (`pixclk`) to the chip. Only delayed by the signal travelling time from the FPGA to the chip and back, the received signal show activity. The returning clock starts (`data_in<1>`) and at about time bin 670, a binary pattern is received at the data line from the chip ((`data_in<1>`),


Figure 6.1: `Chipscope` screen shot showing the timing of signals in the FPGA and the received chip ID.

which is the unique ID of the connected chip. The binary pattern is deserialised, packed into the Ethernet frame and sent to the computer, where it is encoded.
A more complex operation is the setting of the pixel matrix. It takes many more clock cycles and also needs data from several Ethernet frames. The matrix is read back, packed into Ethernet and was investigated at the computer to compare it to the matrix sent to the FPGA. That way, the correct setting was verified.

## 6.2 Readout rate

When the firmware development started, the readout speed was optimised by the implementation of zero suppression. At that time, the firmware was not as complex as in the final design and signal propagation in the FPGA was not an issue. Hence, also higher system clock speeds than the 40 MHz could be tested. The readout rate was evaluated by consecutively opening the shutter for a short time and reading out a single chip at different system clock frequencies. Figure 6.2 shows the results for the prototype system received from Mainz, the early version of the SRS-based zero suppressed readout and the final design at 40 MHz system clock frequency. As expected, the readout rate for the Mainz prototype is lower than for the system with zero suppression. The readout rate of the final design is close to the theoretical maximum $f_{max}$, which is proportional to the system clock frequency $f_{sys}$ and given by

$$f_{max} = f_{sys}/917504. \tag{6.1}$$

96.3 % of the theoretical maximum were achieved with a single chip (42.00 Hz readout rate) and 93.6 % with an octoboard (5.10 Hz readout rate). For the octoboard, the theoretical maximum rate is lower by a factor of eight due to the serial readout of the chips in chain.

## 6.3 Threshold equalisation

When the basic chip operations are functional, more complex routines can be done, for example the threshold equalisation. It is an algorithm in the DAQ software, which continuously calls basic operations to find optimal settings for the four threshold equalisation bits in every pixel. As has been explained in Section 3.1.2, first the value of the THS DAC needs to be optimised. Figure 6.3a shows a control plot

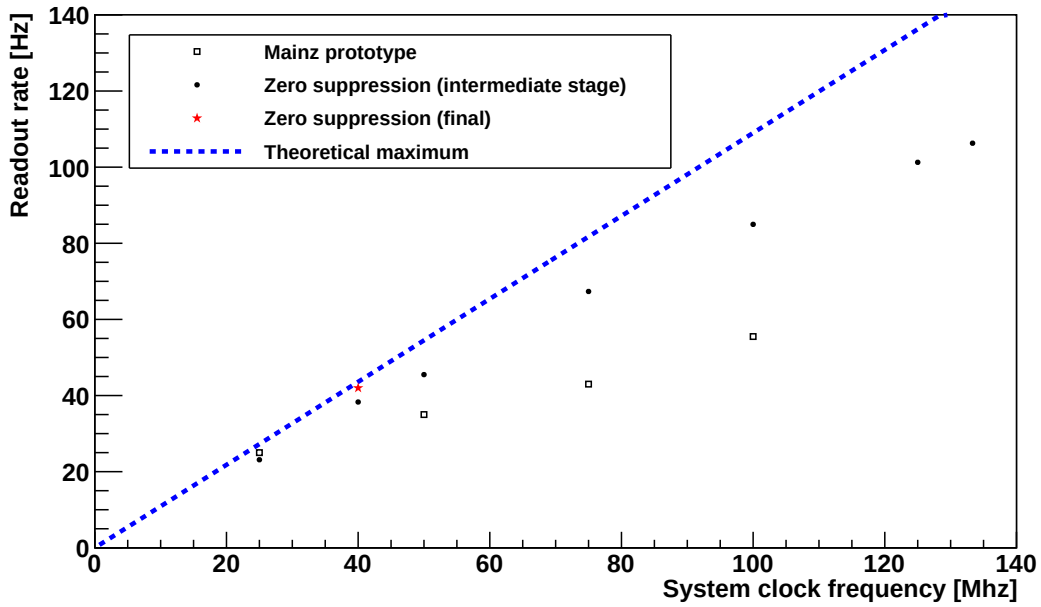
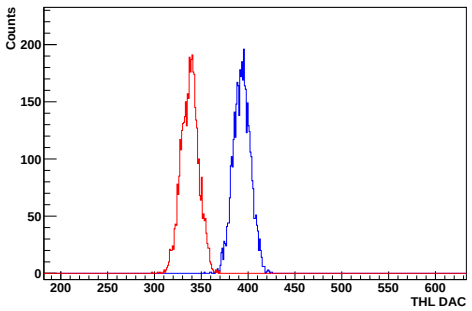
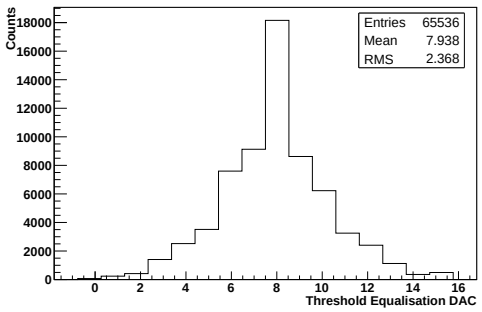



Figure 6.2: Readout speed in dependence of the system clock frequency at different design stages.

of the THS optimisation. It shows two distributions, of which the red one is taken with all threshold equalisation bits set to 0 and the blue one with all set to 1. From the distance of the two distributions, the optimal THS value can be derived. Only a few pixels were investigated, which is sufficient for an estimate of the THS value. More details about how this measurement is performed can for example be found in [75].




(a) Distributions from which the optimal THS value is extracted.




(b) Distribution of the threshold equalisation values for all pixels of a chip.

Figure 6.3: Control plots of the THS optimisation and threshold equalisation.

After the THS optimisation, the main threshold equalisation can be performed. When it is completed, a value for the threshold equalisation bits is assigned to every pixel in the matrix. As there are four bits for every pixel, the value can be between 0 and 15. Figure 6.3b shows the distribution of the values for all 65 536 pixels. As expected, it is centred around the value eight. The tails of the distribution stem from few pixels, which have a significantly different intrinsic threshold level.

The final result of the equalisation is shown in Figure 6.4. It shows again the red and blue distribution (the threshold levels of the not equalised pixels) and in addition in black, the distribution of the equalised pixels, which is significantly narrower. A Gaussian distribution has been fitted and its width indicates the quality of the chip, but also how exact the software and firmware performed the equalisation. Typically, the value is between 1.5 and 2.2 THL DAC units for measurements performed with the MUROS system. The value of 1.968 THL DAC units is therefore in range and all distributions show the expected shape, which confirms the correct behaviour of the SRS. The threshold equalisation was also performed with the MUROS with the same chip and no significant difference in the final threshold equalisation result was observed. In general, the performance of the newly developed readout systems was compared to the MUROS system. A few other examples are shown in the following. For the comparison shown here, the SRS with VHDCI cable was chosen, as with this system, the same cable and Intermediate board can be used as with the MUROS.

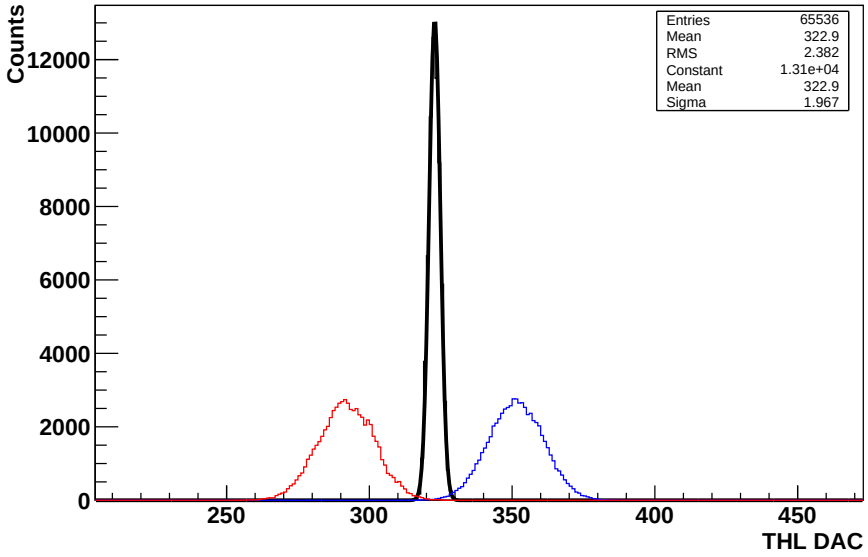



Figure 6.4: Result of the threshold equalisation. The distributions for the not equalised pixels is shown in blue and red. The black curve stems from the equalised pixels.

## 6.4 DAC scan

More and more features provided by the chip were implemented with a growth of the complexity of the firmware and hardware. One example shown here is the possibility to read back the analogue voltage level of the DACs set inside the Timepix chip (`DAC_OUT` signal). A so called DAC scan was performed where by software for each DAC, the value is changed from the minimum to the maximum. The voltage level is measured by the ADC controlled by the FPGA. By scanning each DAC over its complete range, a smooth rising (or falling, depending on how the logic is implemented) voltage is expected. However, there are some known issues for the Timepix chip for some of the DACs, which prevent the optimum behaviour. The result of the DAC scan is shown in Figure 6.5 for the MUROS and Figure 6.6 for the SRS. For both system, the curves are almost identical. One significant difference can be seen for the `BuffAnalogB` DAC, which for both systems does not show the expected behaviour. As this is known,

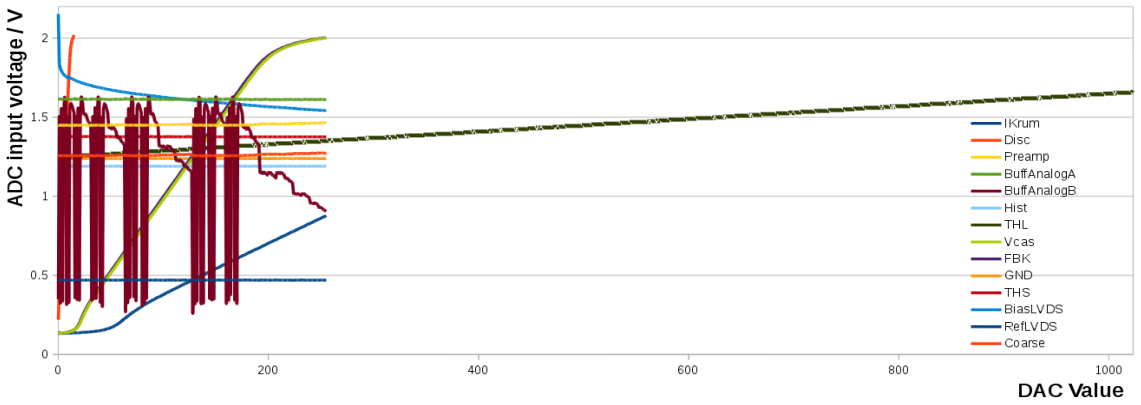



Figure 6.5: Result of a DAC scan taken with the MUROS.

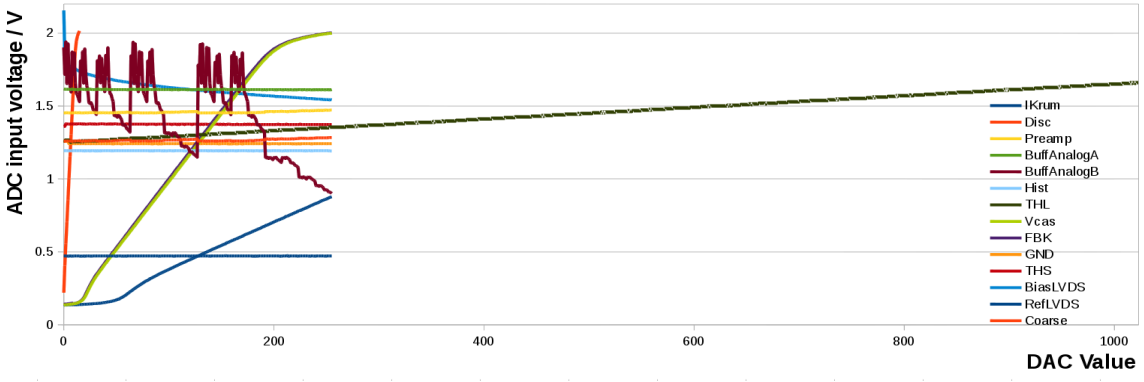



Figure 6.6: Result of a DAC scan taken with the SRS.

the different results for the two systems were not further investigated.
With the DAC scan measurements, the proper operation of the ADC on the self designed hardware was verified. Also the correct assignment of the bits to the FSR is proven.

## 6.5 Test pulses

Another component controlled by the FPGA is the DAC to generate the voltage levels for the `ExtDAC` signal and multiplexer for test pulses. A four channel DAC is used of which the output voltage of every channel can be set from software via the FPGA. Before the implementation, test pulses for calibration were provided by an external test pulse generator connected to the Intermediate board. For a calibration, the user had to set the correct amplitude at the pulser and then start the individual calibration step from software, change the voltage at the pulser and start the next step and so on. With test pulses from the multiplexer, an automated calibration completely controlled by the computer can be achieved. For a proper operation, it has to be assured that the test pulses from the multiplexer (internal pulser) with voltage levels from the DACs results in the same calibration as with the external pulser. In Figure 6.7, a TOT calibration curve is shown. It can be used to convert the TOT counter value recorded by a pixel into charge. For more details about how the calibration is done, see again [75]. The external pulser has been taken as a reference (solid line) and two different implementations of the internal test pulser are

shown, where both show the same result as with the external pulser. The errors on the measurements are smaller than the dots in the plot. The two methods differ only in the timing, the pulse is sent to the chip within the shutter window. For one method, it is applied directly after the shutter has been opened, for the other in the center of the shutter. As the shutter window is far longer than the pulse, it is not cut off by the end of the shutter. Only for pulses with a far higher amplitude than shown in the plot, the falling edge of the signal at the discriminators in the pixels would exceed the end of the shutter and a too short time over threshold would be measured especially when the pulse is applied in the center of the shutter. There were also other methods tried, for which a significant difference to the external pulser was found or the shape depended on the timing of the pulse within the shutter window, what is not expected. The two methods shown in the figure are unique in the fact that the signal applied is not a pulse, but only a falling edge within the shutter window. The rising edge is outside the window. As a falling edge induces a signal as for negative input charge, this is what is desired, see Section 3.1.5.

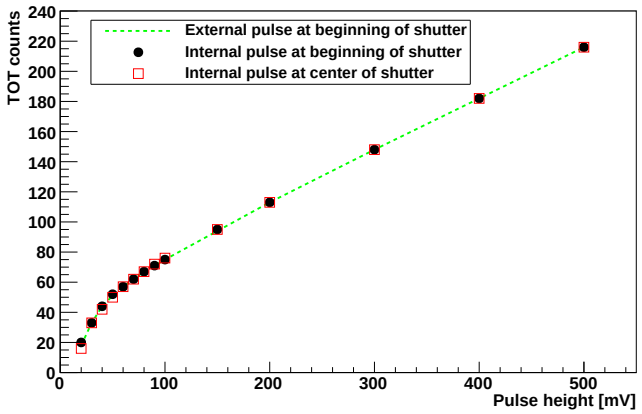



Figure 6.7: TOT calibration curve for comparison of the internal and external test pulses.

With this test, the functionality of the integrated test pulse circuit could be demonstrated. The implemented method was compared to the method previously used and resulted in the same TOT calibration. For the other calibrations, which rely on test pulses, the same was shown.

## 6.6 Calibration

With the generation of test pulses from software, automated calibration routines could be implemented. Those are the TOT calibration shown before, the time walk calibration and the S-curve measurement. The later is needed to convert the threshold level set (value of the global THL DAC in the FSR) to a number of electrons. The method is again explained in [75] and only results will be shown here. In brief, a defined number of test pulses (1000 here) is sent to the chip within the shutter window. The chip is set to Medipix mode to count the number of pulses. For one run in which the THL DAC is scanned, the voltage difference of the falling edge is constant. When the threshold is too high, the chip is not able to detect the pulses, while when the threshold is lowered, the chip at some point starts to record mainly noise. When the threshold is lowered further, the noise is not detected any more but only the pulses due to the specific implementation of the logic in the chip. Hence, the distribution of the number of recorded pulses with respect to the THL value is symmetric around the noise peak which resembles a threshold of zero electrons. The measurement is done for several voltage differences of the falling edge, resulting in different distributions, see Figure 6.8.

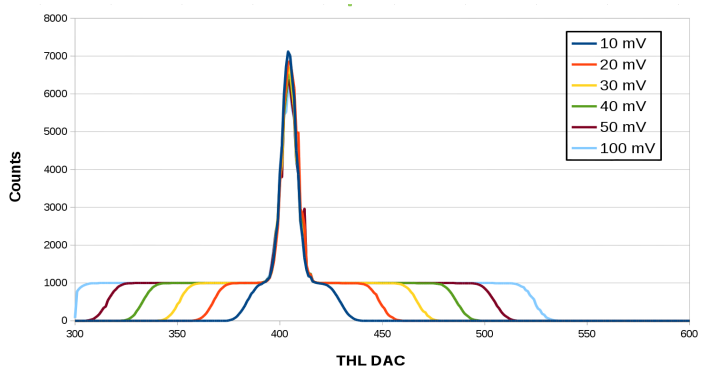
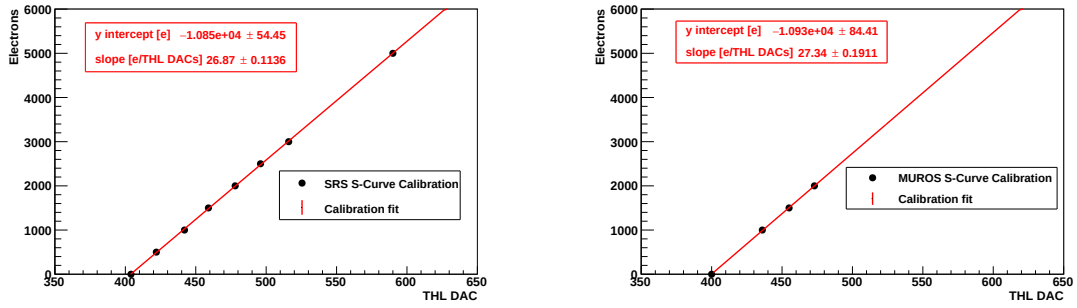



Figure 6.8: S-curve scan result as obtained with the SRS.

In each distribution, the point where only 50 % of the applied pulses are registered is of interest. At this THL value, the threshold level in electrons resembles the pulse height in electrons. The conversion of voltage difference to pulse height in electrons has been explained in Section 3.1.5. In Figure 6.9a, the 50 % THL value is plotted towards the pulse height in electrons for the SRS. With the curve, each THL value can be converted to electrons for a specific Timepix chip. A linear function has been fitted to the measurements and the slope and intercept are given in the figure. The interesting number are the (26.87 ± 0.11) e/THL DACs. It is comparable to the number of about 25 e/THL DACs given in the Timepix manual [67].
The same calibration has been performed with the MUROS for comparison and the result is shown in Figure 6.9b. Both, the slope and intercept of the fitted linear function are in agreement with the measurement by the SRS.




(a) Result from the SRS.

(b) Relult from the MUROS.

Figure 6.9: S-curve calibration to convert the THL DAC value to a number of electrons.

The measurements prove that also the calibration is reliably possible with the SRS-based readout. Similar measurements have also been performed with ML605-based system. In general and as a summary of this chapter, it was shown that both systems are operating as expected and perform similarly to the MUROS. The Timepix chip can be operated from software through the FPGA and also the analogue ICs controlled by the FPGA operate as desired. The systems can be used for data taking and measurements of physics properties of the whole detector including gas amplification structure, what will be expressed in the following chapters.

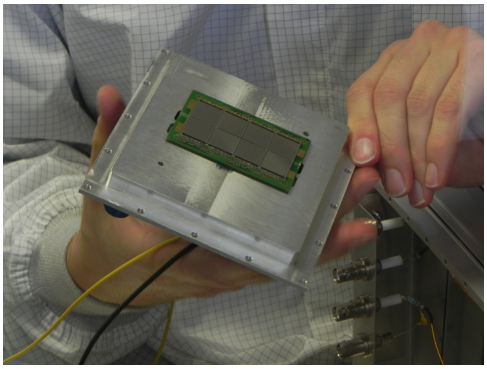
CHAPTER 7

# 2013 test beam with an 8-InGrid module

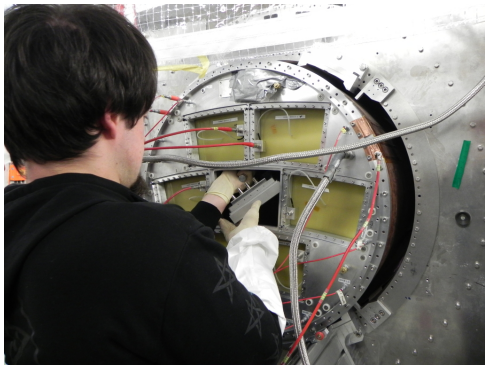
After the technical explanations in the previous chapters, the outcomes of the efforts will be presented in this and especially the following chapter.
As an intermediate step towards a large area Pixel-TPC, a test beam with a module of eight InGrids arranged on an octoboard was carried out at the LP (see Section 3.8) at the DESY II synchrotron in March/April 2013. The module explained in Section 4.3.1 was the second 8-InGrid detector ever tested. Before, a similar module based on a slightly different design was constructed and tested by colleagues from CEA Saclay [74]. Only a brief overview of the intermediate test beam will be given. For details, the reader is referred to [81] and [144].

## 7.1 Setup

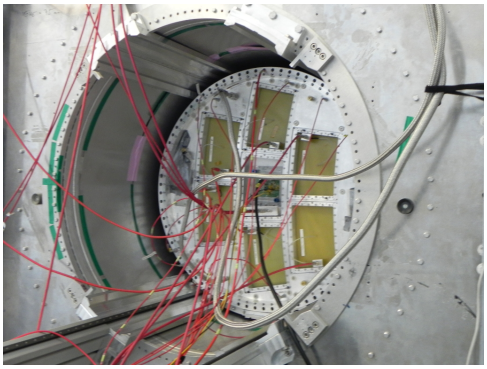
The module was assembled in the clean room (see Figure 7.1a) and tested in Bonn. All chips could be operated in the laboratory, where the power for the octoboards was provided by a standard power supply. However at the test beam, the power supply had to be placed about 10 m away from the 1 T magnet, in which the LP is embedded.
Due to the voltage drop along the cables, the voltages at the supply had to be set to 3.05 V for `VDD` and 3.30 V for `VDDA` to provide the desired 2.2 V at the chips. The constant currents drawn by the two voltages were 0.25 A and 1.66 A, respectively. In addition, especially the digital supply channel `VDD` requires significantly more power, when the pixels are counting. For that reason, the voltage had to be set to a higher value to assure a stable operation when the pixels are counting. Still, chip 8 was noisy in this setup and also disturbed the other chips. For a stable operation of the board, the threshold of the chip was set to a level where no noise, but also no signal was detected.
In Figure 7.1b, the mounting of the module at the LP can be seen. It was done by hand in the center of the endplate. Figure 7.1c shows the complete setup including the cables for high voltage (red) and read out (black). For most of the data taking runs, the TPC was positioned such that the electron beam was recorded by the lower chip row of chip 1-4. For the readout, an intermediate version of the VHDCI-based SRS with a FEC3 was used, see Section 4.2.2. The system was placed directly besides the magnet first, as can be seen in Figure 7.1d and connected by a long Gigabit Ethernet peer-to-peer connection to the computer in the counting room. The ATX power supply in the SRS crate was destroyed by the stray field of the magnet and had to be replaced. The FEC had to stay close to the endplate, as VHDCI cables can only span 3 m. Therefore, it was connected by power cables to the crate placed further away.



(a) Assembly of the module in the clean room.



(b) Mounting of the module to the LP endplate.



(c) LP endplate with 8-InGrid module and cables.

(d) SRS crate and FEC for the readout.

Figure 7.1: Impressions from the setup for the 8-InGrid test beam.

The LP was moved such that the electron beam from DESY II passes through the TPC volume and the primary ionisations can be registered by the octoboard.
The readout rate reached a maximum of 2.5 Hz and only the non zero-suppressed mode could be used at the time. For the trigger, the coincident signal of four scintillators in the beam was used. The shutter of the Timepix chips was opened by the readout with a delay which has been measured to 108 ns. About 640000 events have been recorded in about 100 runs with different settings. The parameters changed were:

- The voltage difference between grid and anode, as those were on a different height, with the aim to find a setup with minimal field distortions.
- The voltage at the grid to study different gas amplifications.
- The energy of the beam to measure different momenta.
- The position and angle of the beam to the endplate to study effects in dependence of the drift distance.

All measurements were carried out without magnetic field and with a field of 1 T and at drift fields of 130 V/cm and 230 V/cm. As the drift velocity of the primary electrons depends on the drift field, the expected arrival time for the maximum drift time in the chamber is different. The shutter opening time

was chosen to be 17.25 µs and 13.8 µs, respectively. The sampling frequency for the pixel counters was set to 40 MHz. As gas inside the TPC T2K was used.

In Figure 7.2, in image of the event display is shown. The event display is a graphical representation of the data taken within the shutter window. In this particular image, the pixels were set in the `TIME` mode, as for all measurements except the grid voltage scans. In `TIME` mode, the arrival time of charge is measured in each pixel and hence the z-position of the primary ionisation can be reconstructed, see Equation 2.10. The counter value of the pixels (see Section 3.1.2) and hence, the arrival time is encoded in the colour code the individual pixels are displayed in. Each pixel hit represents to the first order a single primary electron from the ionisation of the beam electron traversing the TPC volume. Those can better be seen in the enlarged part of the image. Because of diffusion along the drift path towards the readout at the endplate, the primary electrons have spread. The two axes in the display define the x- and y- direction, which are in the plane of the endplate along the chip edges. They range from 0 to 2×256 for y and 0 to 4×256 for x, where the binning is one pixel. This is because the chips are arranged on a 2×4 matrix. As can be seen, the beam has been adjusted such that the electrons end up on the lower chip row, on which all four chips are operational. A characteristic feature of this particular event is the region of high density electrons close to (x,y)=(200/200). It is mainly placed outside the line of primary electrons. Such a signature stems from $\delta$-electrons. Another feature are the areas of insensitivity along the line of electrons. They are exactly at the boundaries between the chips (multiples of 256 in x-direction). In

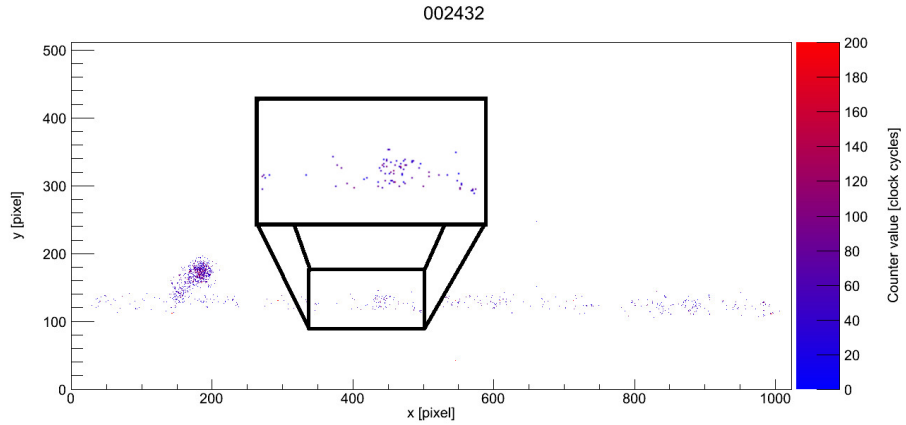



Figure 7.2: Event display image of an event from the 8-InGrid module with zoom on a track segment.

addition to the 8-InGrid module, also a module with an octoboard of eight bare Timepix chips with a triple GEM stack was tested with the same set of parameters. An example event display image is shown in Figure 7.3. The data of the GEM setup has so far not been analysed. As the amplification process in the GEM setup happens in different stages with transfer regions in between, single primary electrons cannot be identified any more at the readout. Instead large blobs of many secondary electrons can be seen. The chips in this setup have been programmed such that every second pixel is set in `TOA` mode, while the other half is set to `TOT` mode also named chequerboard pattern. Hence, the arrival time and the charge distribution in a blob can be measured, which is used to apply the center of gravity method to achieve a better spatial resolution. In the particular event displayed, a $\delta$-electron with higher energy is emitted from the track and curls in the magnetic field.

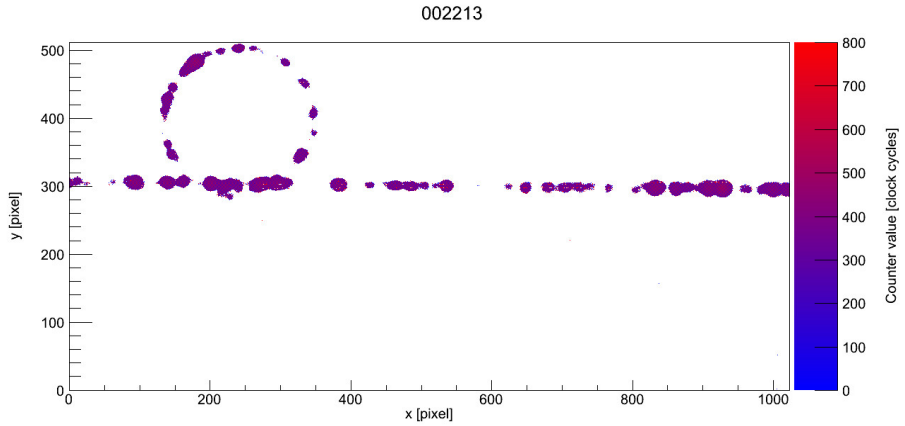



Figure 7.3: Event display image of an event from the eight Timepix module with triple GEM module.

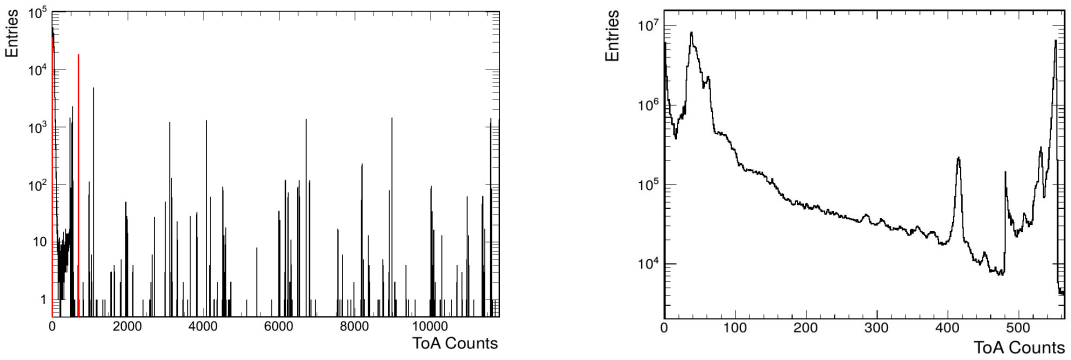
## 7.2 Analysis and results

An analysis of a small fraction of the data was carried out by Robert Menzen [144]. A short summary will be given in the following, while the details can be found in the master thesis. The analysis framework Modular Analysis And Reconstruction For The Linear Collider TPC (MarlinTPC) [155], a tool developed and used by research groups in the context of future linear colliders, was used. For that purpose, first the real positions of the chips on the octoboard were measured with a microscope. With this so called GEAR geometry, the ideal position of the pixels as displayed in the event display can be transformed into the real coordinate system. For the first analysis, a dataset of several measurements with the beam parallel to the endplate, but with different distances at a drift field of 230 V/cm and magnetic field was chosen. For comparison, a dataset with the same parameters but without magnetic field was also analysed.

### 7.2.1 Data quality

For several runs, the magnetic field led to disturbances in the power supply of the chip, which resulted in frames completely dominated by noise. Those frames were filtered by rejecting data files from a certain size upwards. The other data files then were converted into the Linear Collider Input/Output (LCIO) [156] format used by the framework.
To investigate the data quality, the spectrum of measured `TOA` counter values was evaluated. As the shutter was opened for 13.8 µs or 552 clock cycles, a maximum counter value of 553 cycles is expected (the shutter signal is asynchronous to the clock). In Figure 7.4a, the spectrum of all possible `TOA` counts is shown ranging from 0 to 11810, which is the maximum value a pixel can count. Figure 7.4b shows only the region of the spectrum where a signal is expected. In this plot, several peaks can be seen, of which the one around 400 `TOA` counts originates from the beam. The end of the shutter window can be seen as a sharp edge on the right end of the plot. The interesting features concerning data quality are the spikes in the region higher than the maximum counter value achievable within the shutter opening time. Those pixels counted longer than the shutter allows or their counted value was not read out correctly by the readout system. The first is possible for dead pixels which do not work as one would expect. However, the sheer number of pixels which counted more than 553 clock cycles is not compatible with the number of dead pixels. Also the origin of those high counts was shown to not correlate with the known positions of those pixels. It could be shown instead that the spikes stem from bit shifts in the

readout system, which have their origin in a shift of the clock to the data, such that certain data bits did not end up at the correct position when the counter value of a pixel was collected. This failure affects about 3.9 % of the data, of which half is due to pixels not hit, which have received a bit from a neighbouring pixel which was hit. For the data analysis, the high count hits were removed and only the physical meaningful data was used.




(a) TOA spectrum of a typical run from the 8-InGrid test beam, from [144].

(b) Zoom on the physically reasonalbe part of the TOA spectrum, from [144].

Figure 7.4: TOA spectra for data quality control of the 2013 test beam.

### 7.2.2 Data selection and track reconstruction

In each event, tracks were searched by using a Hough transformation [157], which can find straight line tracks. On the short length of only four chips, this approach is justifiable, as the bending in the magnetic field is low. Only a fraction of the recorded events was accepted for a further analysis. To select those, cuts were applied to reject events or tracks, which do not satisfy the following criteria:

- Number of tracks per event: Only events with a single track were selected to simplify the analysis.
- Number of hits per track: To reject incorrectly reconstructed tracks stemming from for example two very close tracks or only short segments, a track was only accepted with more than 200 and less than 1400 hits on about 5.6 cm length.
- Track geometry: Tracks at the edge or such which cross the area close to the chip boarder were not accepted, as those can loose some of their primary electrons and are mainly affected by field distortions at the chip borders. Hence, all accepted tracks are more or less parallel to the long board axis, which is defined as the x-axis.

By these cuts, about 50 % of the dataset was rejected. The number of tracks per event had the largest effect (30 %), while the effect of the hits per track cut was only little.

### 7.2.3 Preliminary analysis results

When a track was found, it was fitted with a linear regression method. Because of the orientation of the TPC during the selected runs, the tracks are parallel to the endplate. Thus, all studied parameters can be evaluated in dependence of the drift distance, which represents the z-position of the track.

First, the correlation between drift time and placement of the TPC in z-direction was investigated. The expected linear relation was confirmed. From a straight line fit, the drift time and the real anode position could be measured from the slope and the intercept of the fitted line, respectively. The measured drift time was in agreement with simulations and did not depend on the magnetic field, as expected.

The reconstructed track length is in agreement with the geometrical length of the octoboard, which is expected, as shorter tracks were removed in the data selection.

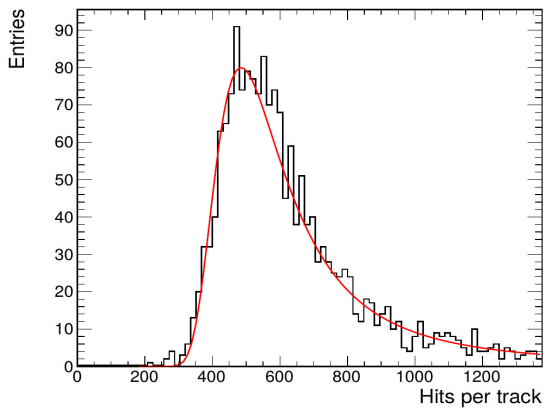
The number of hits per track length expected for T2K gas was calculated to be $\eta_P = 96.2\,\mathrm{cm}^{-1}$, see Table 2.1. This number is clearly only a mean value, as the ionisation is a statistical process. The distribution was measured for different z-positions (see Figure 7.5a as an example) and a mean value in good agreement was found with an expected dependence of the z-position: For tracks very close to the anode, the primary electrons cannot diffuse enough, such that several can end up in a single InGrid hole and only a single hit is recorded. For larger drift distances, the number of measured primary electrons decreases because of attachment of the primary electrons to gas contaminations.

For measuring the resolution of the detector, the residuals of the hits on the tracks are analysed. A residual is the shortest distance of a hit to the reconstructed track. For all hits on a track, the individual values form a distribution centred around zero only in xy-direction if the track is correctly reconstructed. In z-direction, the distribution is asymmetric because of the time walk effect, see Section 3.1.2. The Root Mean Square (RMS) width of the distributions is a measure for the diffusion and an agreement between measurement and calculation (Equation 2.15) was found. Figure 7.5b shows the mean values of the residuals in xy-direction for the different runs, in which the TPC was placed at different z-positions. The mean is shown in dependence of the x-position. One can see that the mean values form a certain shape, which emphasises the boarders between the chips. Moreover, this shape is independent of the z-position, as the data from the different runs give the same result. This indicated that the shape is induced close to the anode. In fact, other groups have seen similar effects at the board of modules. The s-shape, which can clearly be seen for the two central chips, originates from field distortions at the chip edges and so called $\vec{E} \times \vec{B}$ effects, which appear when the electric and magnetic field are no longer parallel. This effect clearly degrades the measured spatial resolution of the detector, as it broadens the total residual distribution. But, as the effect does not depend on the drift distance, it should be possible to correct for the shifts. The measured hit positions are no longer an exact projection of the primary electrons, but are displaced depending on their position on the xy-plane. Still, the displacement is a bijective function and by knowing the displacement, the exact projection could be recalculated. This was tried in the analysis, but needed further investigation.

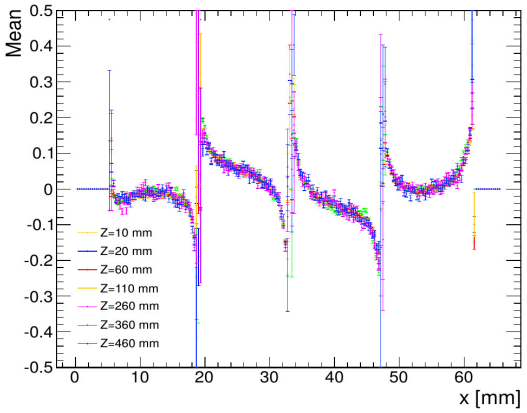
The RMS of the residual distribution gives access to the diffusion and resolution of the detector. The spatial single point resolutions $\sigma_{xy}$ can be obtained from the xy-residual distribution. For this distribution, however, all hits assigned to the track have an influence including the hit for which one wants to calculate the single point resolution. If $\sigma_N$ is the RMS of the residual distribution including the point under investigation and $\sigma_{N-1}$ is the RMS with rejecting that point, than it can be shown [158] that

$$\sigma_{geo,xy} = \sqrt{\sigma_N \sigma_{N-1}} \tag{7.1}$$

is the correct value for the single point resolution. For a perfect detector with ultimate intrinsic resolution, the single point resolution would only depend on the diffusion for different z-positions. The dashed line in Figure 7.6a represents this single electron diffusion. As a detector is not perfect, the measured $\sigma_{geo,xy}$ is expected to be worse and the better the detector, the closer the measured points approach the solid line, as can be seen in the figure. A measure for the intrinsic detector resolution is the extrapolation of the data point to zero drift, e.i. z=0. For a detector with a segmentation with pitch $d$ and uniform




(a) Number of hits per track (≈ 5.6 cm length) for a run at z≈ 160 mm fitted by a Landau distribuition, from [144].



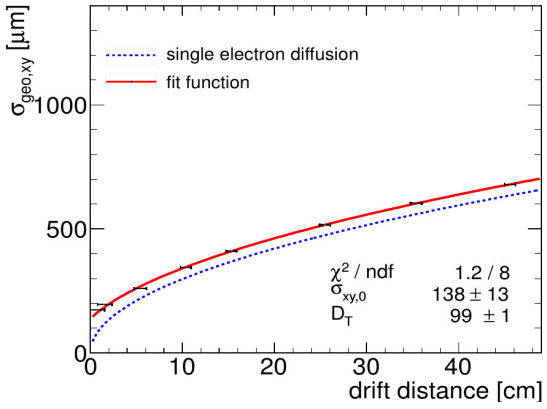

(b) Residual means for differenz z-positions with magnetic field, from [144].

Figure 7.5: Hits per track and field distortions as measured in the 2013 test beam.

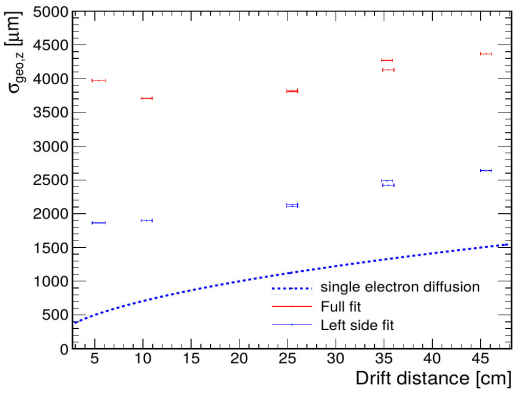
response on that segment, it can be shown that the intrinsic resolution is given by

$$\sigma_{0,xy} = \frac{d}{\sqrt{12}} \tag{7.2}$$

which for the pixel pitch of the Timepix chip would lead to an expectation of 15.9 µm. This value is the maximum which can be achieved when no center of gravity method can be applied, as is the case, if an electron activates a single pixel. Effects like field distortions decrease the resolution and $\sigma_{0,xy}$ will be larger. Additionally, the intrinsic resolution should be independent of the magnetic field. This could not be verified in the analysis, indicating that the field distortions have to be further investigated. The measured intrinsic resolution as shown in Figure 7.6a the fit parameter $\sigma_{0,xy}$ (Equation 7.1) is given by (138 ± 13) µm.




(a) Transverse resolution with magnetic field and field distortion correction, from [144].




(b) Logitudinal resolution with magnetic field and field distortion correction, from [144].

Figure 7.6: Transverse and longitudinal single point resolution as measured in the 2013 test beam.

The fit function for the xy-resolution $\sigma_{xy}$ in dependence of the $z$ position in the asymptotic region

(diffusion larger than readout segmentation) can be shown [159] to be given by

$$\sigma_{geo,xy}(z) = \sqrt{\left(\frac{A}{N_{eff}}\right)^2 + \left(\frac{D_T}{N_{eff}}\right)^2 \cdot z}, \tag{7.3}$$

where $D_T$ the transverse diffusion constant and $N_{eff}$ the number of effective electrons per measurement point. The factor $A$ is a constant for $z \to 0$. It represents the systematic error, which stems from the so called hodoscope effect. It occurs, when the drift length is very short, such that the diffusion is not high enough to spread the charge on several readout segments. The resolution then is in the order of the segmentation, which means that for very short drift distances

$$\sigma_{geo,xy}(z \to 0) = A = \sigma_{0,xy}. \tag{7.4}$$

For the InGrid, with single electron detection and resolution, $N_{eff}$ is equal to one, whereas for pads, which collect the signal from multiple primary electrons, $N_{eff}$ is larger, typically about 20-30 depending on the drift distance and pad size [160] [161]. This implies that for the InGrid, the fit formula for any $z$ is given by

$$\sigma_{geo,xy}(z) = \sqrt{\sigma_{0,xy}^2 + D_T^2 \cdot z}. \tag{7.5}$$

For rectangular readout cells, additional terms have to be taken into account, which decrease the spatial resolution and depend on the track angle.

The longitudinal resolution (in z- or drift direction) can be described similarly to Equation 7.5, by replacing the transverse diffusion constant $D_T$ by the longitudinal one ($D_L$) and the intrinsic spatial resolution $\sigma_{0,xy}$ by the intrinsic longitudinal resolution $\sigma_{0,z}$, which is given by the intrinsic timing resolution $\sigma_{0,t}$. They are related by the drift velocity:

$$\sigma_{0,z} = v_d \cdot \sigma_{0,t} \tag{7.6}$$

The timing resolution is given by the sampling frequency of the readout, with which the arrival time of charge is measured. In case of the Timepix chip, it is given by

$$\sigma_{0,t} = \sqrt{\frac{2T_c^2}{12}}, \tag{7.7}$$

where $T_c$ denotes the clock period the chip is operated at. The factor two is given by the fact that the error on the time measurement can be up to two clock cycles, as both the signal from the hit and the shutter are synchronised to an internal clock in every pixel [68]. In case of a frequency of 40 MHz and a drift field of 230 V cm$^{-1}$, the intrinsic longitudinal resolution is given by $\sigma_{0,z} = (755.2 \pm 0.5)\,\mu$m. This value is large compared to the effect of the drift, as can be seen in Figure 7.6b from the *Left side fit*, in which the measured values from a fit are constantly above the single electron diffusion by about $\sigma_{0,z}$. The *Full fit* is a fit to the measured residuals, which is additionally influenced by the time walk effect.

## 7.3 Conclusions for further developments

The test beam was successful and well received within the community [162]. The first preliminary results were published in [81]. However, the achievements were just an intermediate step towards the Pixel-TPC demonstrator. From the preliminary analysis results and the performance of the detector, many conclusions for the further development could be drawn.

### 7.3.1 Readout system

The SRS-based readout system performed very reliable. However, the ATX-Power supply of the crate did not withstand the stray field of PCMAG. The design with the short VHDCI cables between the module and the readout was just a temporary solution and longer cables are required, such that the readout system can be placed further away from the detector.
The bit shifts which were observed in the data were the main deficiency discovered in the readout and required some additional procedures to avoid those, see Section 5.2.
From the data analysis, it can be deduced that the longitudinal resolution is limited by the 40 MHz sampling frequency provided by the readout. The Timepix chip, however, is capable to be operated up to 100 MHz. As explained in Section 5.2, also this drawback was tackled.

### 7.3.2 Setup

In general, the module design was convincing. In particular the positioning of the anode plate closely surrounding the InGrids at a different height and at a different potential proved to minimise the field distortions at the octoboard edges. The choice to use an octoboard as basic unit simplified the handling. Still, field distortions are an issue, as can be seen from the analysis. They are the main reason for a spatial resolution worse than expected. The origin of the distortions are the gaps between the InGrids, where the potential is not well defined. This could also be shown in simulations and was studied in detail in [146]. A suggestion to avoid the field distortions are aluminium strips, which cover the gaps between the chips. Still, the installation of those strips is difficult, as it has to be done by hand without destroying the grid. Moreover, a conductive glue has to be used to fix the strips, which comes with the risk that the glue flows through the grid holes or down the isolation dikes at the chip edge and connects the grid to ground. Additionally, several grids are directly connected, which increases the capacity of the grid-anode structure. Sparks can be more severe in this case. However in the octoboard setup, four grids receive their high voltage from a single supply anyhow, so connecting those four grids by aluminium strips does not increase the capacity.
In the test beam, chip eight on the board could not be used because of the powering scheme with a laboratory power supply far away from the detector which resulted in a voltage drop due to the long cables. The ideal case could be a generation of the required 2.2 V close to the chips. It should provide a stable voltage level, even if the current drawn by the chips increases when the pixels start counting. Such a power supply was built and tested based on LDOs and buffer capacitors [78].
The cooling of the module was not used in the test beam, because the temperature could not be monitored anyhow and the large surface of the module provided enough cooling, such that it did not heat up significantly. The temperature monitoring still should be done, especially when the number of chips per module increases.

### 7.3.3 Physics needs

Originally, the InGrid module was not planned to be the first choice for the test beam. Its production was finished just in time to be taken to DESY . This test went unexpectedly well, so the whole test beam program was conducted with the GEM module as well as with the InGrid module. The data taken with the GEM module has not been analysed so far, as a similar test beam campaign has already been done [163]. For the future developments, only InGrid-based detectors were studied, mainly because of their single electron detection efficiency.
To study this type of detector more deeply, a larger area has to be equipped with InGrids in particular to record longer tracks. This requires a scale up of all detector components. For a demonstration of the

concept, a module with about 100 InGrids was foreseen.
On the analysis side, longer tracks will require more solid and faster algorithms especially for track finding. The standard Hough transformation in MarlinTPC is not designed to operate on such a high number of hits as is expected from a several tens of centimetre long track. New approaches were studied among others based on a partial track reconstruction on single chips, so called tracklets, which are then combined to a complete track [164].
The 2013 test beam itself was very successful, but the outcomes were not only what has been presented in the preliminary analysis. It also was a demonstration of the intermediate stage of the whole Pixel-TPC project and provided indications on what still needed to be done. The different tasks were the subject to master, bachelor and diploma projects, as mentioned above and also to the further development of the subjects described in this thesis. In the next chapter, the outcome of all the improvements will be explained.

CHAPTER 8

# 2015 test beam with the Pixel-TPC demonstrator

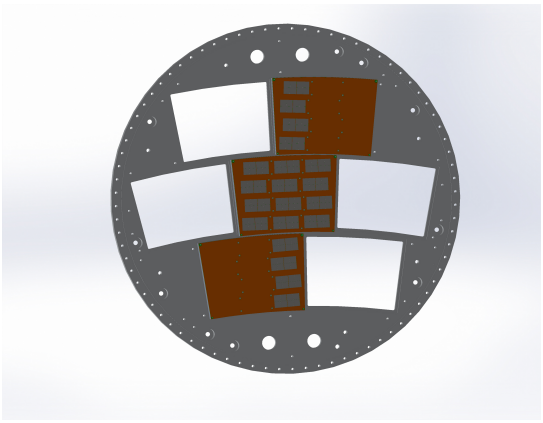
This chapter brings everything together. In March/April 2015, the test beam to demonstrate the Pixel-TPC was conducted at the LP at DESY. All components have been described in the previous chapters. These are the TPC prototype and its endplate in Section 3.8, the modules with in total 160 InGrids in Section 4.3.3, the SRS and its adaptation to read out this amount of Timepix chips in Section 4.2.6 with the complete firmware as explained in Chapter 5. In the first part, the setup for the test beam will explain how the different components were assembled. Then, results from a data analysis will be presented, followed by a conclusion of the test beam and suggestions for further developments.

## 8.1 Setup and experiences

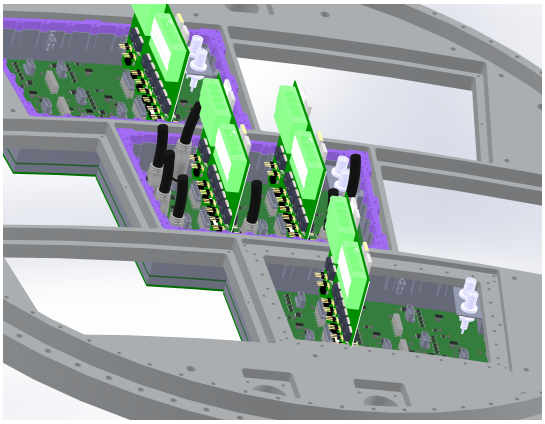
For the first time, all components were operated all together and simultaneously. Even if the individual parts have been tested separately in the laboratory, the interplay needed some fine tuning. In this section, the setup at the test beam area will be explained starting with the implementation of the modules at the LP in Section 8.1.1 followed by the conditions, cooling, high voltage and finally different run parameters in Section 8.1.5.

### 8.1.1 Module arrangement

The modules were arranged at the endplate, such that the maximum track length could be measured. Figure 8.1 shows a CAD drawing of the endplate from the in- and outside. In Figure 8.1a, the three modules with the InGrids on the octoboards as gray areas are shown, the brown area represents the anode. The outside view in Figure 8.1b shows the frame with the Intermediate board, low voltage boards and HDMI cables. Images of the setup are shown in Appendix B. The 20 octoboards were arranged such that the boards with the best and most operational chips (see Appendix C and Figure 8.2) were placed along the vertical axis in Figure 8.1a. For most of the runs, it was planned to shoot the beam such that those boards record signals. Unfortunately, seven chips on an octoboard in the center were not operational due to a short between the pin of the shutter signal and ground on the second chip in the chain. The particular wire bond had to be removed to operate at least the other octoboards nearby. Theoretically, this could have been corrected in firmware, which showed to be difficult and could not be performed during the test beam. From the total 160 InGrids, four chips were not connected due to shorts (marked black in Figure 8.2), seven chips showed no events due to electronic problems (red) and nine (including those on the malfunctioning central board) were noisy (blue) at the beginning of the test



(a) CAD drawing of the LP endplate with the three InGrid modules, view from inside.



(b) CAD drawing of the LP endplate with the three InGrid modules, view from outside.

Figure 8.1: CAD drawings of the LP endplate with the InGrid modules for the 2015 test beam.

beam. In some runs, additional chips were noisy, which could be resolved by a tuning of the threshold levels.

### 8.1.2 Setup conditions

The TPC was filled with T2K gas and flushed at a flow of 40 l/h. The temperature, pressure, water and oxygen contents of the gas were monitored permanently.
As in 2013, a coincidence signal from four scintillators at the beam entrance to the test beam area was used as trigger. The signal was duplicated and fed into the five FECs, each controlling and reading four InGrid octoboards via four data and one slow control HDMI cables of 15 m each. The time difference between the trigger signal and the shutter opening at the modules was measured to be 238 ns. All five FECs were connected to a switch via Gigabit Ethernet, from where a long cable was connected to the computer with the DAQ software in the counting room. In most of the runs, all pixels were set to TOA mode, to measure the arrival time of charge. The shutter was opened for 13.8 µs, with a sampling frequency of 40 MHz or 80 MHz. A THS optimisation and threshold equalisation were performed during the commissioning at the test beam. The threshold was set individually for each chip, first by an automated procedure in the DAQ software and then fine tuned by hand, such that each chip only had a few noisy pixels. The TOT calibration and the S-Curve measurement were performed after the test beam in the laboratory.

### 8.1.3 Cooling

Always four octobards were powered by one low voltage board [78]. They were cooled with water from the urban supply, of which the pressure was reduced from 4 bar to 1 bar at a flow of about 30 l/h. The water was distributed such that the central module received twice the amount of flux than the other two modules. No significant temperature difference between the entering and returning water could be observed.
In total 12 temperature sensors were placed on the three modules. At each module, one was placed at the Intermediate board in the center of the module. The temperature at that position was stable all the time at about 25 °C. The remaining sensors were place on low voltage power boards and there especially

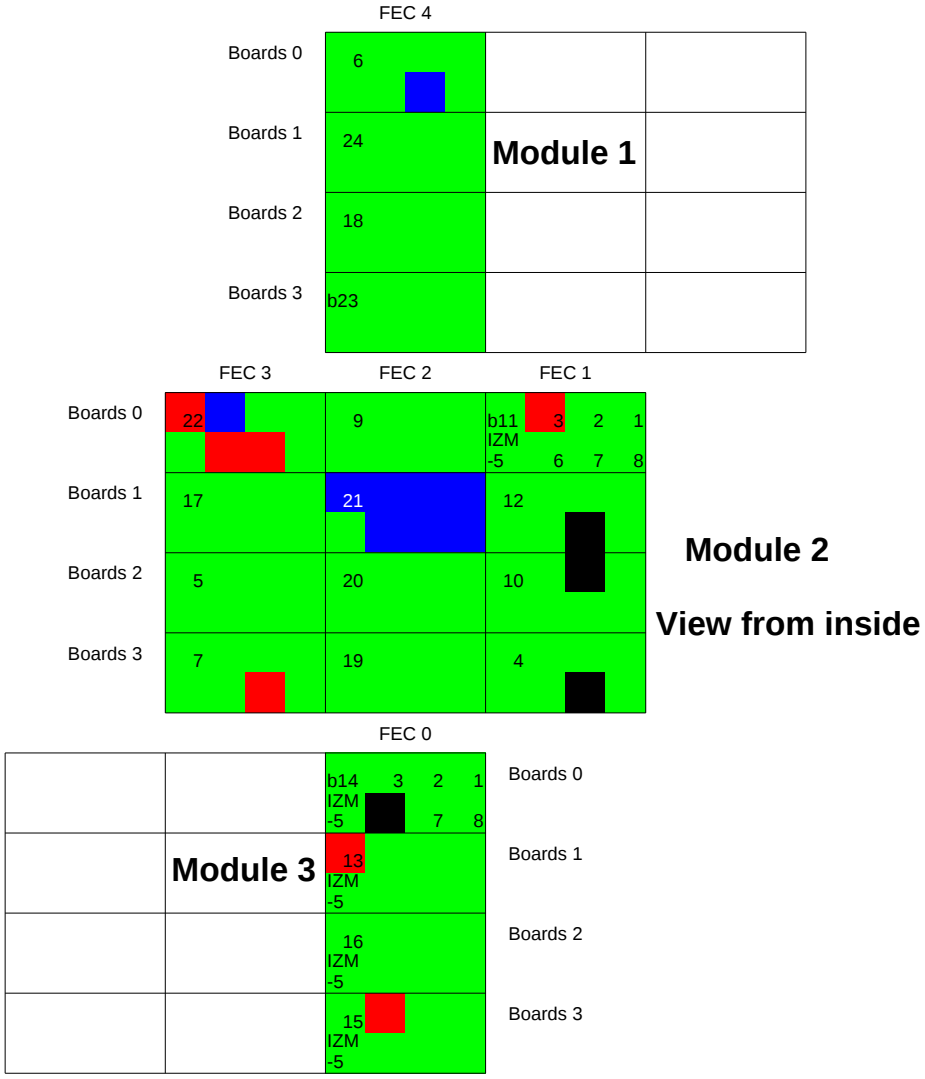



Figure 8.2: Arrangement of the octoboards on the modules, status before the test beam. The octoboards are labelled by their numbers as in Appendix C. On module 3, all boards are made of InGrids from the IZM-5 production. In total, two boards (b14, b11) are rotated, such that the chips are numbered opposite to the other boards. Chips marked in green were functional at the begin of the test beam, chips marked in black were not connected, chips in red did not show events and chips in blue were noisy. The boards and chips are shown as seen from inside of the TPC. The FEC numbers mark, which set of four octoboard was read out by which FEC.

at the LDOs, which supplied octoboards with a low resistance between ground and a supply voltage, see Appendix C. Here, a significant rise of temperature could be observed during data taking and especially when the system was awaiting a trigger, but the accelerator did not provide beam. In this state, the clock is already transmitted to all pixels and is permanently buffered and forwarded through the chip columns, which requires a lot of power. Still, the temperature did not rise to more than 100 °C for all LDOs apart from one component, which reached 130 °C. Such a high temperature is already at the edge of the specifications of the LDOs. In normal operation, the hottest components reached about 90 °C and none was destroyed. It has to be mentioned that another particular LDO was cooled by a connecting piece of the pipework of the water cooling circuit, which was covered with heat conductive paste and mechanically pressed onto the component. This LDO did already heat up to about 110 °C in laboratory tests, as it had to supply an octoboard with less than 1 Ω between ground and the chips supply voltage. The effect of this cooling was a reduction of temperature of about 30 K.

### 8.1.4 High voltage

The high voltage for the grids was provided by a single connector per module. The plug was connected to the Intermediate board by a wire and a 10 MΩ resistor in series. On the Intermediate board, the high voltage was distributed to the octoboards, where always a half board was connected to the main power line by again a 10 MΩ resistor. That way, a spark in one of the half octoboards cannot be as severe and a trip of a single board would not directly affect the other boards.
On two modules, the wire from the high voltage plug to the Intermediate board was broken at the begin of the test beam, but could be fixed. The high voltage was provided and controlled by a supply in the counting room. It was set such that a trip of the anode, module or field strip of the TPC would cause a ramp down of all voltages except the cathode voltage. In total, trips occurred very rarely. At the beginning of the test beam, the module with the IZM-5 boards was more likely to trip. This has already been seen in laboratory tests prior to the test beam. The voltage for that module had to be set to a 10 V lower voltage compared to the other modules. Also the central module showed higher currents on the high voltage than expected, but could be operated stable for most of the time. For a short period of the test beam serious issues occurred, when this module was constantly tripping. The problem could be traced down to a specific half octoboard, where the grid was connected to ground by only a few ohms. From outside the TPC, such a defect cannot be solved. The first idea for the reason was that a wire bond providing the high voltage for the InGrids could have fallen through the gap between the chips and touch the chip surface or the PCB. An exchange of the board was already planned, when suddenly the short disappeared and the module was even more stable in operation than before. Also the unexpected high current had disappeared. Later on, it was observed that the water content in the TPC had risen during the time of this issue. It is very likely that the heat conducting paste underneath the octoboards has welled up between the chips and even arrived at the grid, such that a conductive path was formed. After the paste had dried out, this path could have disappeared. During production, one octoboard became unusable due to this effect.
Sparks were observed only occasionally in normal operation, as the high voltage was set such that the detector was operated at a moderate gain of about 2000 to 4000. The anode was put to 370 V, while the InGrids were put to 340 V for module 1 (at the top in Figure 8.1b) and 330 V for module 3 with the IZM-5 octoboards and the central module 2 in the configuration for a drift field of 230 V/cm. The voltage difference between anode and grids was set such that the field distortions were minimised by using the experiences from the 2013 test beam. For a drift field of 130 V/cm, the anode voltage was lowered by 10 V to achieve a uniform drift field. Only at the very end of the test beam, the voltage was raised further and the gas gain was measured with the pixels set to TOT mode.

### 8.1.5 Different runs and parameters

190 runs with different parameters have been recorded with in total 1 527 363 frames. The runs are numbered from 28 to 215. One run number was accidentally assigned twice and a test run with number 5005 was also kept. Run 28 to 50 were used for the commissioning of the detector including some last changes in the SRS firmware and the fixes of the high voltage supply. From run 51 on, all systems were operational and the modules were completely powered, calibrated and the correct threshold levels were assigned.
The stage of the LP was moved to different positions with respect to the beam for the different runs. The extreme values of the engine encoder were:

- z-position (displacement along the TPC z-axis): −130 mm to 330 mm, which is the maximum allowed value by the control software. The beam hits the anode at about −135 mm. The highest distance of the beam to the endplate hence is about 465 mm, even if the TPC has a length of 567.6 mm.
- $\theta$ angle (rotation of the LP around the vertical axis): −40° to 15°, where at −40° the beam enters through the endplate.
- $\phi$ angle (rotation of the TPC in the magnet around the z-axis): −90° to 9°, where 4° is a rotation such that the beam optimally passes all three modules.
- h-position (lifting and lowering the LP): 0 mm to 65 mm, where 30 mm is a height such that the beam optimally passes all three modules.

Data was taken without a magnetic field and at 1 T, at sampling frequencies of 40 MHz and 80 MHz, with beam electron energies between 1 GeV and 6 GeV and also cosmic particles. At the end, the high voltage for the InGrids was scanned from 280 V to 350 V with the pixels also set to TOT mode in order to measure the gas gain. A typical run includes 10 000 frames and took about 40 min, depending on the readout rate. During night, also longer runs with up to about 85 000 frames were recorded when no shifters were present. The readout rate of the system achieved up to 5.2 Hz in untriggered mode, which is close to what is theoretically possible for the setup. The rate at which triggered data was taken, however, was lower and depended on the beam intensity. For 5 GeV, which was the standard setting, it was about 4.1 Hz, while for the highest intensity at 3 GeV, it went up to 4.8 Hz. All data was taken in zero-suppressed mode. A run with 10 000 frames resulted in about 4.8 GB of raw data (1.1 GB for compressed data), which is dominated by the noisy chips.
The physics program consisted of series of runs, in which only one parameter was changed, called a scan. Those were z-scans (change of the z-position of the LP), $\theta$-scans (rotation of the LP), $\phi$-scans (rotation of the TPC in the magnet), h-scans (change of the height of the LP) and p-scans (change of the beam electron energy). Some of those scans were performed with and some without magnetic fields and at different drift fields and sampling frequencies.
Apart from the few drawbacks mentioned, the test beam went smoothly and all systems worked reliably. Already during the test beam, first impressions were shown to the collaboration and an article for the linear collider newsline was prepared [165]. A few event display images are shown and explained in Appendix D.

## 8.2 Preliminary analysis

A first analysis of the 2015 test beam data is presented in this section. The goal is not to provide a complete analysis, but look at a few specific topics. The data quality will be investigated with similar

methods than for the 2013 test beam. Some chips died during the test beam. The number of operational chips in dependence of the runs will be shown together with possible reasons for the malfunction in Section 8.2.8. In this test beam, there were no completely noisy events, hence no cuts on the file size were applied. The cleaning of data is done in a more sophisticated way.
For the analysis of the test beam data, the MarlinTPC framework was used. In a first step, the raw data taken during the test beam as ASCI txt-files was converted to LCIO. The data type is than called `TrackerRawData`. In this step, the chips were also correctly arranged. This has been necessary, as for octoboards with only seven chips, the data is not associated to the correct geometric position. As the chips are all in a chain, the data of a board with e.g. chip 3 bridged is the same as the data of a board with chip 6 bridged from the view of the readout. Automatically, the not present chip will be displayed at the place of chip 8, as it is the last chip in the row. However, an additional feature was implemented in the DAQ, were the user can set the number of total missing chips on a board and their exact position. Then, the data is assigned to the correct chip. This also required an intervention in the FPGA firmware. During the test beam, one missing chip was not assigned and another one was assigned incorrectly by the operators. By looking at the event display with tracks passing the two relevant octoboards, the consequences of the shift could be seen, even during the test beam. Still, the incorrect assignment was kept until the end of the test beam, as it was clear that the effect needs to be corrected anyway.
The `TimePixXYReaderProcessor` of MarlinTPC was extended for reading the data of 160 Timepix chips into LCIO and now also includes the possibility to interchange data from chip to chip. The processor chain as implemented in the steering file for MarlinTPC is shown in Figure 8.3.

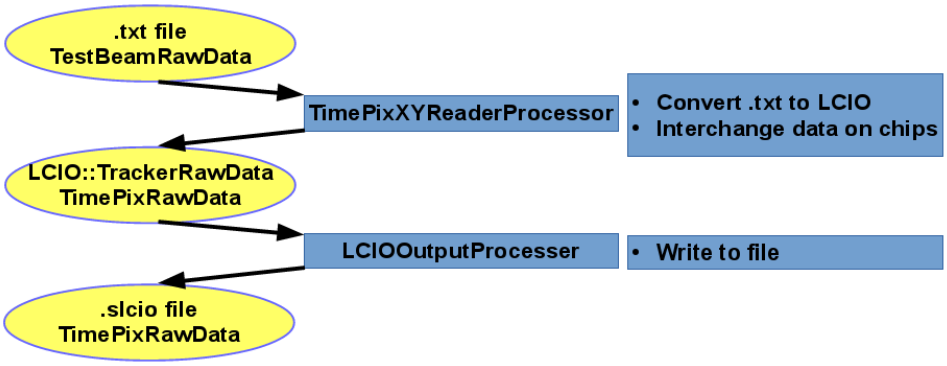



Figure 8.3: MarlinTPC processor chain to generate LCIO data from the test beam data.

In further analysis steps, MarlinTPC requires a mode map and a status map. The mode map is an LCIO file and holds information about the mode each individual pixel was programmed to. In case of most of the recorded data, all pixels were set in the TOA mode. Therefore, a uniform mode map with all pixels set to mode TOA could be generated by the `TimePixModeMapCreaterProcessor`. The processor chain, in this case a single one, is shown in Figure 8.4.

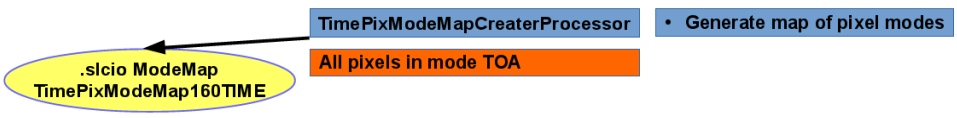



Figure 8.4: MarlinTPC processor chain to generate the mode map for the test beam data taken in TOA mode.

Similarly, the status map has been generated by the `TimePixMaskCreaterProcessor` as shown in

Figure 8.5. In this map, the status of each pixel is stored, which can be intact, dead or noisy. For the beginning, all pixels were set to intact.
With the data in the LCIO format and the two maps, more complex processors can be operated, as will be shown below. The first goal of the data treatment was to provide an adequate input to the `TimePixMaskCreaterProcessor`, such that a status map with all dead and noisy pixels can be generated. As from time to time different chips were noisy, chips died and dead columns have appeared, each run requires its own status map.

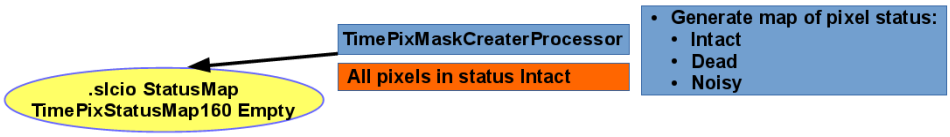



Figure 8.5: MarlinTPC processor chain to generate the status map with all pixels set to intact.

### 8.2.1 Data quality and cleaning

Although there were no completely noisy events, the data from the 2015 test beam includes far more noise of a different kind than the 2013 data. First, this is because the threshold for 160 chips could not be set as accurate by hand as for only eight chips. Then, the chips themselves were not all of the best quality, which means that there were several dead columns. And finally, there have been chips which were completely noisy. Clearly, this has an effect on the data quality. Dead pixels and completely noisy chips dominate the data and hence also the TOA spectrum. In Figure 8.11a, the raw TOA spectrum of a run is shown. It can be seen that there are many hits with a TOA counter value higher than possible. The highest possible value is close to 560 for the 40 MHz sampling frequency and a shutter opening time of 13.8 µs. It will be shown that those entries stem from dead and noisy pixels and are mainly not due to bit shifts in the readout.
An automated cleaning procedure has been developed based on the occupancy map of a run. In the occupancy plot, each pixel is displayed in a 2D map, with a value of how often the pixel was hit in the run. A so called hot pixel is hit in every frame, hence its value will be 100 % of the number of events. Noisy pixels also show up in the occupancy. Summing up all pixels in a histogram, the occupancy histogram, a large fraction of the noise can be separated from the physically meaningful data. A cut can be applied to reject noisy pixels. A pixel at the position were the beam passed the module also is hit from time to time. The cut value can be calculated by the following approximation:
From the ionisation in T2K gas, about 100 primary electrons are expected per 1 cm of track length. On this length, about the same number of pixels will give a signal (single electron detection). The area on which those electrons are distributed on the chip surface has a width, which is given by the diffusion and for all tracks of a run is dominated by the beam spread, which is at least 3.5 mm. So the 100 electrons are collected on an area of 3.5 $cm^2$ or about 12 000 pixels. The probability that a pixel is hit then is 0.83 %. So a pixel directly in the beam profile will be hit about $N = 83$ times in a run of 10 000 frames on average. Because of the high number of frames, the distribution can be assumed to be Gaussian with a width of $\sigma = \sqrt{N} = 9.1$ hits. Taking the three sigma range of the Gaussian into account, it is very unlikely that a pixel is hit more often than $N + 3\sigma = 110$ times in a run of 10 000 frames, which translates to about 1 % of the number of frames.
In the occupancy map or the occupancy spectrum, all pixels with a higher value can be assigned to be noisy or dead and a cut can be applied to identify those pixels. To be conservative, the cut value *OccCut* has been set to 2 %. Figure 8.6 shows the occupancy map for run 143, in which the beam was only

about 15 mm away from the anode. The run contains only 4043 frames, as it had to be stopped before the nominal end. Some pixels were activated in every frame. In the 2D plot, the colour code represents the number of frames each pixel has been hit. The scale was changed to a maximum of 80 (about 2 %) such that the beam profile becomes visible. All pixels marked in red were activated more than 80 times, which are primarily on specific chips, dead columns and noisy chips. The pixels in the beam profile are not red, only a few at the lower part of the plot are displayed in yellow. The same figure has been inspected with the minimum value set to 80 (not shown), in order to identify the pixels, which will be marked as noisy or dead. In this display, the beam profile cannot be identified.

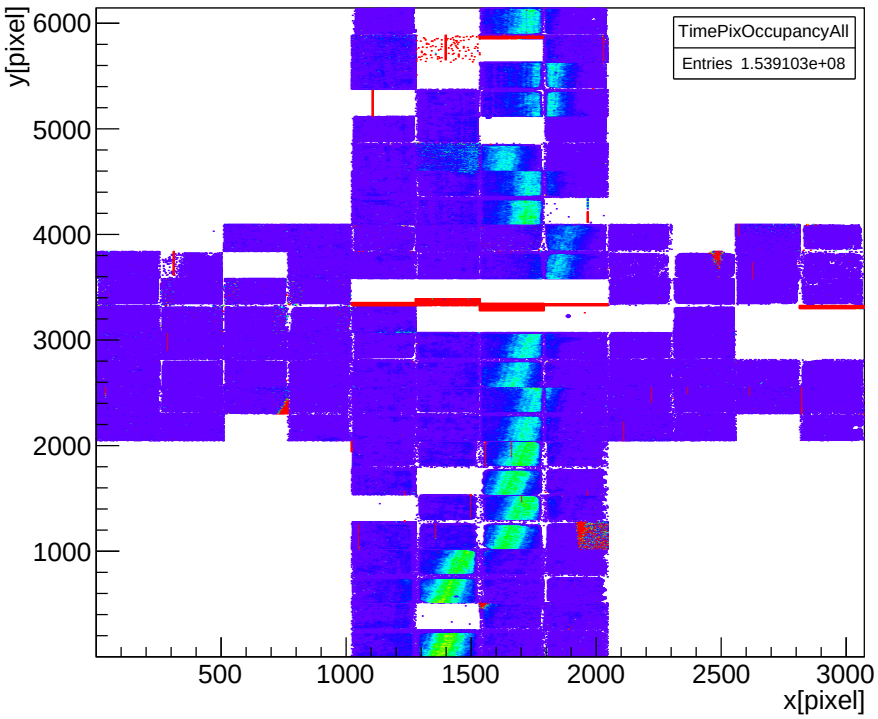
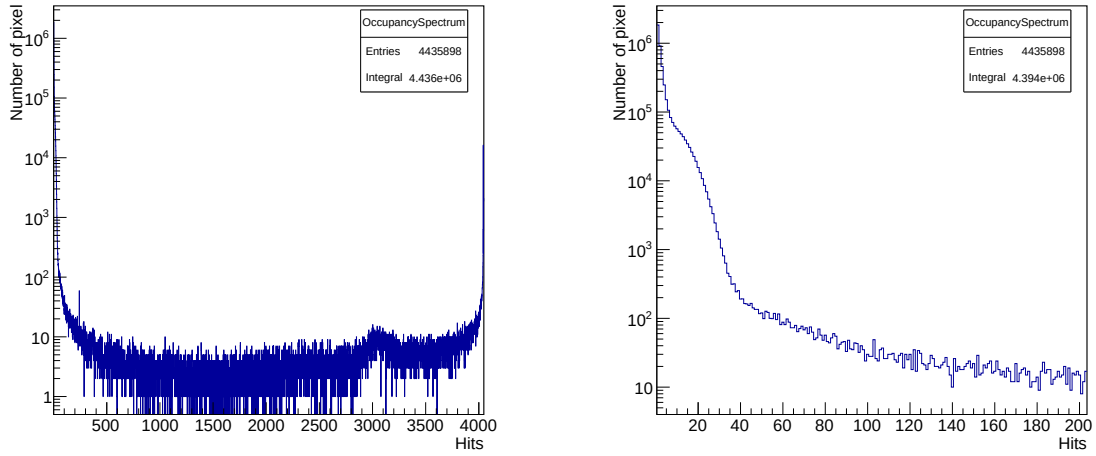



Figure 8.6: Occupancy plot of run 143 without cuts. The maximum number has been set from 4043 down to 80, such that the beam profile becomes visible. The shifts of the beam profile is due to the fact that the correct position of the chips has not been taken into account. The colour code represents the number of hits per pixel with red representing 80 hits.

The same data is displayed as a spectrum in Figure 8.7a with an enlarged view at the lower end in Figure 8.7b. Note the logarithmic scale on the y-axis, which represents the number of pixels per bin. The x-axis denotes the number of times the pixels in the particular bin were hit during the run. The prominent peak at the lower end of the spectrum up to about 40 hits (1 % as expected by the approximation) represents the pixels covered by the beam profile. The superelevation at very few hits stems from pixels outside the beam profile activated by scattered tracks. The occupancy cut for this run would mask all pixels with more than 80 hits.

The processor chain in MarlinTPC is shown in Figure 8.8. It starts with the `TimePixRemoveMaskedPixelProcessor`, which takes the LCIO file with the `TrackerRawData`, the mode map and the status map with all pixels set to intact. The processor sets all pixels in every event to zero, which are marked as




(a) Complete occupancy spectrum of run 143 without cuts.

(b) Lower end of the occupancy spectrum of run 143 without cuts.

Figure 8.7: occupancy spectrum of run 143 without cuts.

dead or noisy in the status map. As a status map with only intact pixels is fed into the processor, nothing is done in this first step. Next, the data is converted to `TrackerData`, which is required by the `TimePixOccupancyProcessor`. Apart from the occupancy and occupancy spectrum, the processor generates a log file, which contains the pixels which are rejected by the `OccCut`. In fact, not the complete list of pixels is given, but the processors identifies completely dead chips, columns and rows and isolated dead pixels. The value of dead or noisy pixels, until a row or column is marked as dead has been set to 85 pixels of 256 in a row or column and 3500 pixels for a complete chip. Additionally the chips which are completely empty are also noted in the log file.

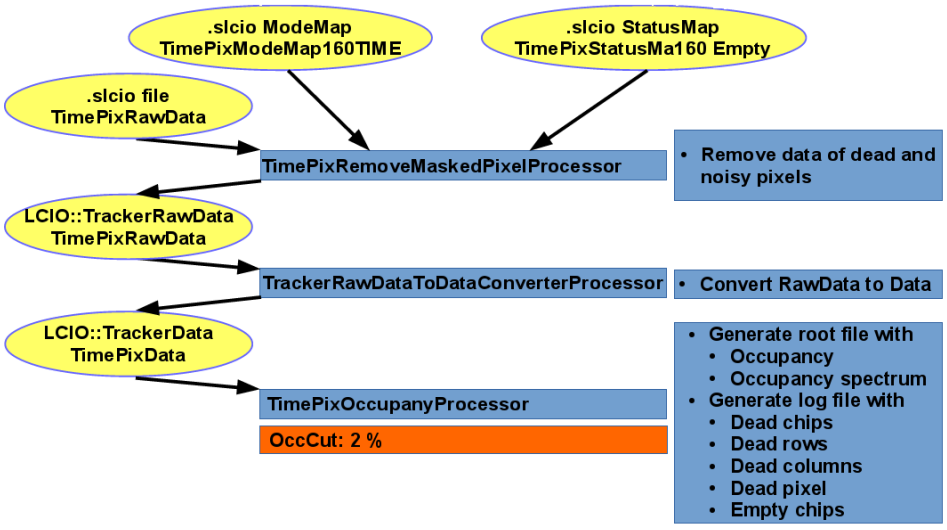



Figure 8.8: MarlinTPC processor chain to generate the occupancy plots and cuts for noisy and dead pixels.

To reject all data from dead or noisy chips, rows, columns and pixels, a new status map has to be

generated. This is again done by the TimePixMaskCreaterProcessor, which takes the information from the occupancy log file as input parameters, see Figure 8.9.

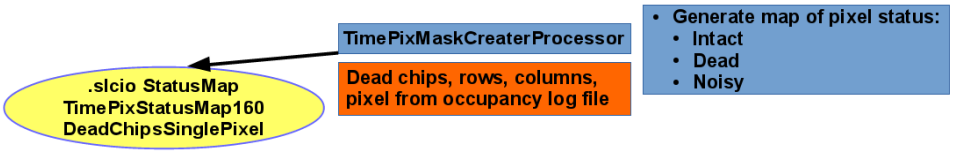



Figure 8.9: MarlinTPC processor chain to generate the status map with the dead rows, columns, chips and single pixel from the occupancy cut.

With the status map containing the information about the dead chips, rows, columns and individual pixels, the next step of data quality inspection can be started, which is the creation of the TOA spectrum with cleaned data. The flow chart can be seen in Figure 8.10. Again, the TimePixRemoveMaskedPixelProcessor is called first, but now uses the status map as generated before. After converting TrackerRawData to TrackerData, the PixelSpectrumProcessor is called, which generates the TOA spectrum.

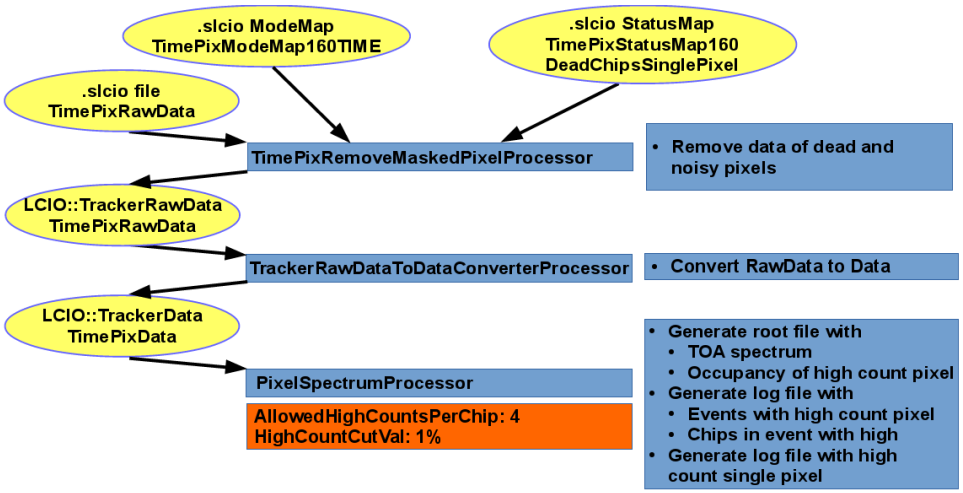
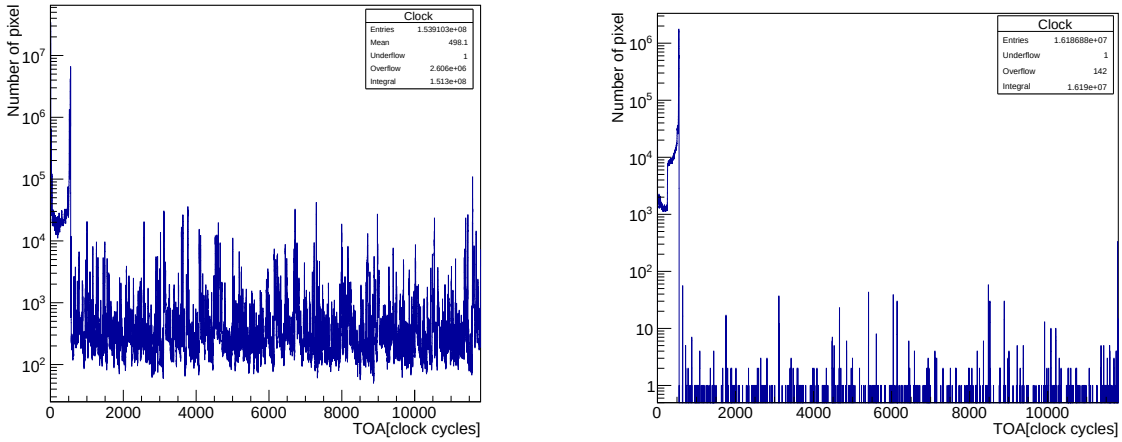



Figure 8.10: MarlinTPC processor chain to generate the TOA spectrum plot and cuts for high count pixels and events.

In Figure 8.11, the TOA spectra without (Figure 8.11a) and with (Figure 8.11b) OccCut can be seen. The number of entries has decreased by one order of magnitude and almost all entries in the overflow bin have disappeared. The overflow bin contains the counter value 11 810, which is the highest number a pixel can count to. This value is typically reached by dead pixels constantly in every frame. Still some high count values are left in the spectrum. For this particular run, there are 1197 hits left with a TOA value higher than 560 and 142 hits in the overflow after the OccCut. A closer inspection of those high count hits shows that 1074 hits have their origin in four frames and 58 hits stem from a single pixel. Remember that the occupancy cut just rejects pixels which were activated more than 80 times in this run. The conclusion is that there are still a few dead pixels, which are only activated rarely and that there are some single events, in which incorrect counter values occur. Two of the four frames mentioned above can be seen in Appendix D Figure D.8 and D.9. It can be seen that a single octoboard is affected by a malfunction, of which one can be explained by bit shifts of the data and the other one is possibly due to

corrupt Ethernet packages. To summarise, there are two effects, which result in high count pixels. First, there are still dead pixels, which are activated very rarely and second, there are single events, in which a few chips have many high count pixels generated by a malfunction of the readout or external effects. Therefore, a procedure has been developed in the `PixelSpectrumProcessor`, which first logs chips with more than a defined number of high count hits and the corresponding event number and second, logs individual pixels with high count hits, which are activated more than a defined number of times in a run. The maximum number of allowed high count hits per chip per event `AllowedHighCountsPerChip` has been set to 4 and the number of events, in which a particular pixel can have high count hits before it is marked `HighCountCutVal` has been set to 1 % of the number of events in the run. Hence, the log file contains a list of event numbers with the chips that had too many high count hits in the event and a list of pixels with too many high counts in the run. Again, a new status map has to be generated,




(a) Complete TOA spectrum of run 143 without cuts.

(b) Complete TOA spectrum of run 143 with occupancy cut.

Figure 8.11: Complete TOA spectra of run 143 at differenc cut levels.

in order to additionally reject the pixels with high counts. In Figure 8.12, the procedure is shown, which is again performed by the `TimePixMaskCreaterProcessor`. It generates the final status map for the run which includes the dead and noisy pixels. Therefore, it takes the two log files from the `TimePixOccupancyProcessor` and `PixelSpectrumProcessor`.

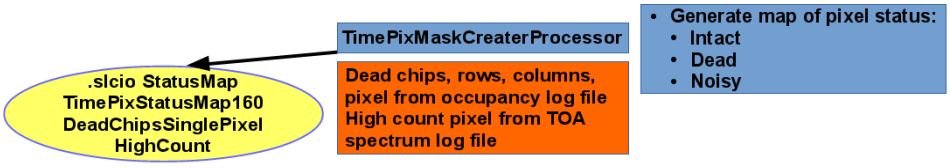



Figure 8.12: MarlinTPC processor chain to generate the status map with the dead rows, columns, chips and single pixels from the occupancy cut and the high count pixels from the TOA cut.

With this status map, the final data cleaning can be performed, which results in an LCIO file of cleaned data. The process flow can be seen in Figure 8.13. A new processor in this chain is the `TimePixThrowEventOrChipProcessor`, which has been written for the special purpose to reject complete events or single chips in an event. Therefore it takes the information in the log file of the

PixelSpectrumProcessor, in which events with too many high counts (AllowedHighCountsPerChip cut) on at least one chip were found. The user can select if only the data of that chip is rejected or the complete event. As the first case would bias the analysis, the rejection of complete events was selected. In the dataset of run 143, 13 of the 4043 events have been rejected. In total, after this step of data cleaning, 14 frames with at least 1 high count hit, but not more than 4 per chip were left, with in total 33 high count hits in the whole run. Those hits likely stem from defect pixels, which are rarely active.

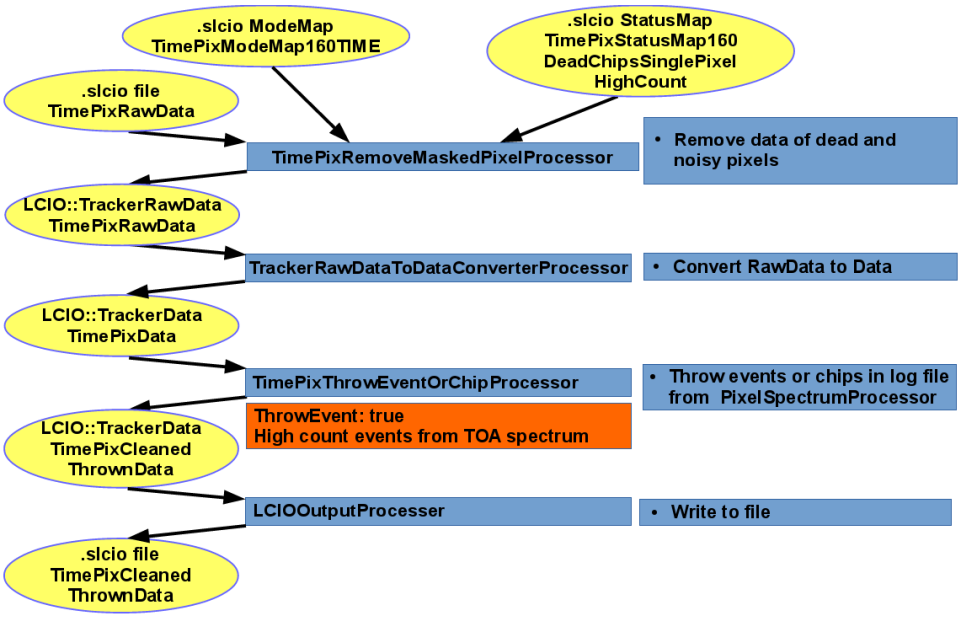



Figure 8.13: MarlinTPC processor chain to generate the cleaned data.

The effect of all the cuts has so far only been discussed for the high count hits, which are defined to have a TOA value larger than the theoretical maximum number given by the shutter opening time and the clock frequency. It could have been shown that almost all of those hits can be removed in the data cleaning and that they stem from malfunctioning pixels or bit shifts on single octoboard in very few events.

The effect on the physically meaningful data will be shown below by inspecting the lower part of the TOA spectrum. In Figure 8.14, it is shown for three different stages of data cleaning in an overlay plot. The solid line represents the data without any cuts. Its characteristics are a peak at very low TOA values (which stem from the defect octoboard in the center), a peak at exactly the number of clock cycles the shutter was open (≈560, from noisy pixels starting to count as soon as the shutter opens) with a sharp edge towards higher values, the peak from the beam very close to the sharp edge and several smaller peaks.

When the occupancy cut is applied (dashed line) another edge becomes visible at about 260 clock cycles. The following calculation will prove that it represents the position of the cathode. By taking the TPC length of 56.76 cm, the drift velocity of about 7.6 cm µs$^{-1}$ at the conditions of this run, the maximum drift time $t_{drift,max}$ in the TPC is given as

$$t_{drift,max} = 56.76\,\text{cm}/7.6\,\text{cm}\,\mu\text{s}^{-1} = 7.47\,\mu\text{s} \tag{8.1}$$

or about 299 clock cycles at 40 MHz. Subtracting this value from the end of the shutter at 560 clock

cycles gives about the 260 cycles. The signals within the time interval in between the two edges stem from interactions inside the chamber mostly at the time of the trigger. Particles, which enter the TPC later can still be registered. But their primary electrons arrive later at the readout, hence the number of TOA counts until the end of the shutter is lower. Noisy pixels can start counting any time within the shutter window. It can be seen that by the cut about 1000 entries are removed in every bin.
Finally the remaining data after the cleaning by occupancy and high count cut is shown as the red area. The high count cut only has a minor influence on the lower part of the spectrum.
In general, it can be seen that the peak with the data from the beam is not affected much by the cuts. In particular the peaks at very low clock cycles and exactly at the end of the shutter are significantly reduced. The several smaller peaks are also partly removed, while some are still existent. The most prominent ones differ by about 40 clock cycles or 1 µs, which is the circulation time of the single bunch in the DESY II synchrotron. So the peaks are due to off-trigger particles passing the TPC.

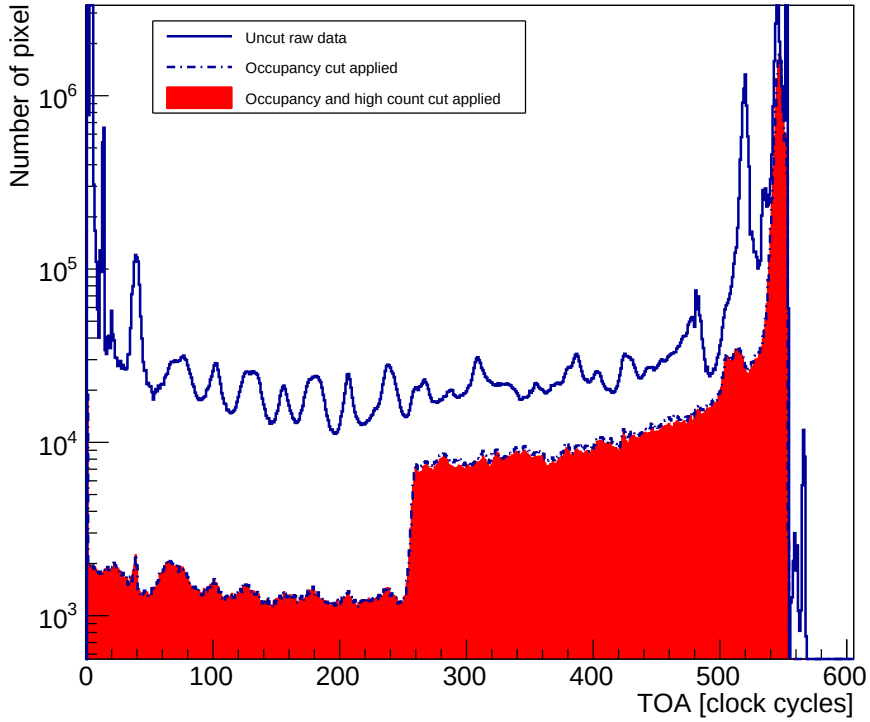



Figure 8.14: Lower end of the TOA spectra (physically meaningful data) at different cut level.

### 8.2.2 Drift velocity measurement

As can be seen in Figure 8.14, the TOA spectrum has two characteristic edges. The one on the right stems from the maximum amount a pixel can count within the shutter window ($N_{TOA,shutter}$), while the left side edge (at about 260 TOA counts) stems from the cathode ($N_{TOA,cath}$). However, it is not as prominent in all runs and can be smeared out by off-trigger events and higher order effects like time walk.
It has to be noted that the right edge in the TOA spectrum does not represent the anode, but the end

of the shutter window. The difference is given by the trigger delay ($d = 238\,\text{ns}$), which implies that ionised particles of triggered events have already drifted a certain distance when the pixels start counting. Therefore, the drift time is given by

$$t_d = d + t_{shutter} - N_{TOA}/f_{clock}, \tag{8.2}$$

where $t_{shutter}$ is the shutter opening time and $f_{clock}$ is the sampling clock applied when the shutter is open. $t_{shutter}$ can also be expressed by $N_{TOA,shutter}/f_{clock}$.
The drift velocity $v_d$ in the gas can be derived from the clock cycle difference between the two edges and the known TPC length $l_{TPC} = (567.6 \pm 1.0)\,\text{mm}$ [166]. For each run, it can be calculated by the drift time $t_{d,cath} = d + (N_{TOA,shutter} - N_{TOA,cath})/f_{clock}$:

$$v_{d,cath} = l_{TPC}/t_{d,cath} \tag{8.3}$$

Despite the fact that $N_{TOA,cath}$ cannot be derived accurately, a precision of 1-2 % for $v_{d,cath}$ can be obtained because of the long and well known drift distance.
The drift velocity can also be derived from a series of runs at different z-positions and the beam position in the TOA spectrum. A Gaussian distribution is fitted to the peak stemming from the beam and the mean value is taken as input for the calculation of the drift time. In Figure 8.15, this drift time is plotted against the corrected[1] stage position in z-direction. In addition, also the drift times for the cathode signal are shown. They are a hint to changes in conditions like temperature, pressure or contaminations during the scan.

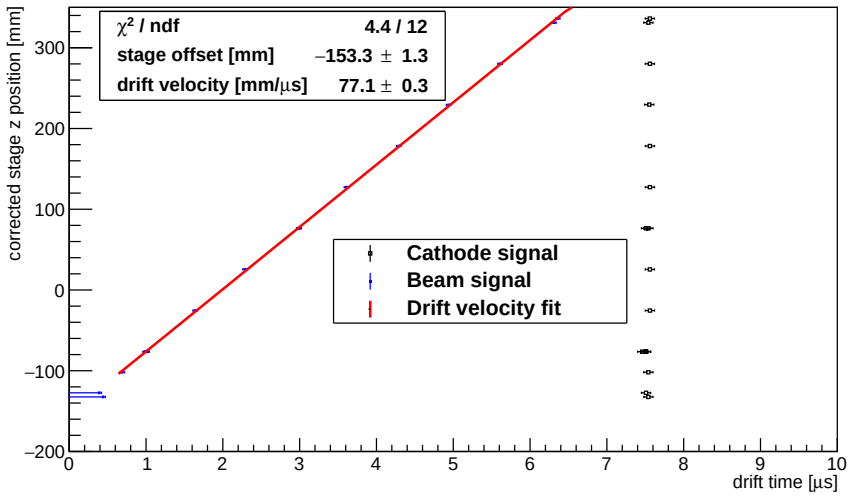



Figure 8.15: Drift velocity measurement of a z-scan with $B = 0\,\text{T}$ and $E_{drift} = 230\,\text{V cm}^{-1}$ (run 90-105).

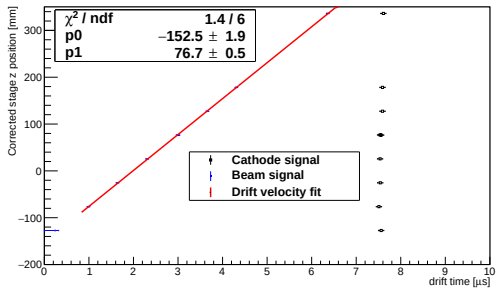
The expected linear relation is fitted by a line. The slope corresponds to the mean drift velocity $v_{d,meas}$ of the runs. From the intercept, the offset of the stage position to the anode position can be derived. In total, five z-scans with different field parameters have been analysed, see Figure 8.16. As the runs in a scan have been recorded within some hours, no significant changes in the conditions are to be expected. Table 8.1 summarises the results and compares them to Magboltz simulations. The measured stage

[1] After the test beam it was found out that when the stage is moved, the covered distance is 1.85 % larger than displayed at the control unit.

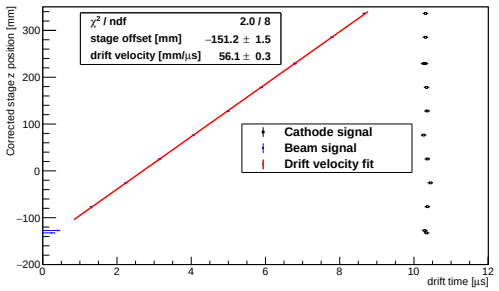
offsets are all consistent, as expected. The measured drift velocities $v_{d,meas}$ are in agreement with the simulations and do not depend on the magnetic field. The results from the measurement of the drift velocity $v_{d,cath}$ by the cathode position is given as a mean value for all runs of a scan $\bar{v}_{d,cath}$ in the table. The differences will be discussed in the following.

| Run | $B$ [T] | $E_{drift}$ [V/cm] | Stage offset [mm] | $v_{d,meas}$ [mm/µs] | $\bar{v}_{d,cath}$ [mm/µs] | $v_{d,sim}$ [mm/µs] |
|---|---|---|---|---|---|---|
| 51-59 | 0 | 230 | $-152.5 \pm 2.0$ | $76.7 \pm 0.6$ | $75.08 \pm 0.34$ | $76.50 \pm 0.02$ |
| 61-72 | 0 | 130 | $-151.2 \pm 1.6$ | $56.07 \pm 0.2$ | $54.80 \pm 0.09$ | $56.42 \pm 0.01$ |
| 76-89 | 1 | 230 | $-153.7 \pm 1.8$ | $76.9 \pm 0.5$ | $74.92 \pm 0.16$ | $76.39 \pm 0.01$ |
| 90-105 | 0 | 230 | $-153.3 \pm 1.3$ | $77.1 \pm 0.4$ | $75.3 \pm 0.09$ | $76.38 \pm 0.01$ |
| 121-135 | 1 | 130 | $-151.1 \pm 1.3$ | $52.49 \pm 0.2$ | $51.33 \pm 0.33$ | $53.23 \pm 0.01$ |

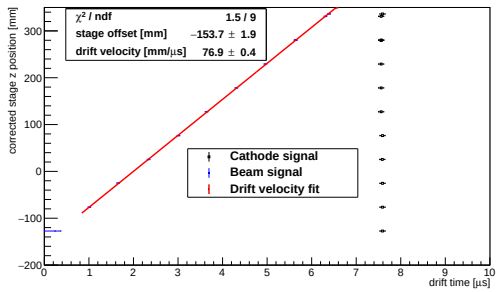
Table 8.1: Summary of the measured stage offset and drift velocities with comparison to Magboltz simulations.



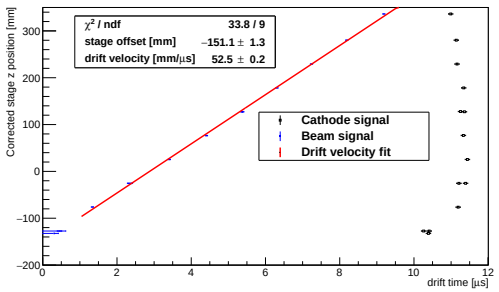

(a) Drift velocity measurement of a z-scan with $B = 0\,\mathrm{T}$ and $E_{drift} = 230\,\mathrm{V\,cm^{-1}}$ (run 51-59).




(b) Drift velocity measurement of a z-scan with $B = 0\,\mathrm{T}$ and $E_{drift} = 130\,\mathrm{V\,cm^{-1}}$ (run 61-72).




(c) Drift velocity measurement of a z-scan with $B = 1\,\mathrm{T}$ and $E_{drift} = 230\,\mathrm{V\,cm^{-1}}$ (run 76-89).




(d) Drift velocity measurement of a z-scan with $B = 1\,\mathrm{T}$ and $E_{drift} = 130\,\mathrm{V\,cm^{-1}}$ (run 121-135).

Figure 8.16: Further drift velocity measurements

An exception concerning the stable conditions is the z-scan from run 121 to run 135. Within this data taking period, the problem with the high voltage occurred and the water content had risen from the typical value of 58 ppm to 392 ppm at the maximum and 260 ppm at the end of the period. Table 8.2 shows the drift velocities as obtained from the cathode signal of individual runs and Magboltz simulations including the change of conditions. The general trend to lower drift velocities for higher water contaminations can be seen.

| Run | Water contamination [ppm] | $v_{d,cath}$[mm/µs] | $v_{d,sim}$[mm/µs] |
|---|---|---|---|
| 121 | 50 | 54.6 ± 0.6 | 55.84 ± 0.01 |
| 129 | 392 | 50.5 ± 0.5 | 51.03 ± 0.01 |
| 135 | 260 | 51.7 ± 0.5 | 52.82 ± 0.01 |

Table 8.2: Drift velocities $v_{d,cath}$ measured for different runs during a z-scan with $B = 1\,\mathrm{T}$ and $E_{drift} = 130\,\mathrm{V\,cm^{-1}}$ derived from the cathode signal. During the scan, the gas in the TPC was contaminated by water. The effect on the drift velocity is shown and compared to Magboltz simulations.

Figure 8.16d shows drift times measured for the tracks from the beam for that z-scan. Note the data points for the drift time of the cathode. They reflect the progression of the water contamination during the z-scan.

The drift velocities $v_{d,cath}$ measured from the cathode position are in average 1.2 % too small, see Table 8.1. This could stem from the method how the drift time is obtained. The central value of the fitted S-curve might not be the correct measure for the cathode position in the TOA spectrum.

In a simple simulation of a TOA spectrum, 1000 random Gaussian distributions in an interval from 300 to 550 clock cycles have been superimposed, see Figure 8.17. The width of the distribution was increasing towards the lower end of the spectrum to account for the diffusion. The lower edge of the spectrum has been fitted by an S-curve function as has been done for data. The S-curve center is significantly below the end of the interval. Hence, the difference between the two edges would be measured too large resulting in a too low drift velocity. However, the effect is on a level of only 0.1 % and cannot explain the the systematically too small drift velocities as obtained by the measurement of the cathode position. For a further investigation, the signals that contribute to the cathode signal have to be investigated. Possibly they do not directly stem from triggered particles, but are induced later and hence are measured with a lower TOA value.

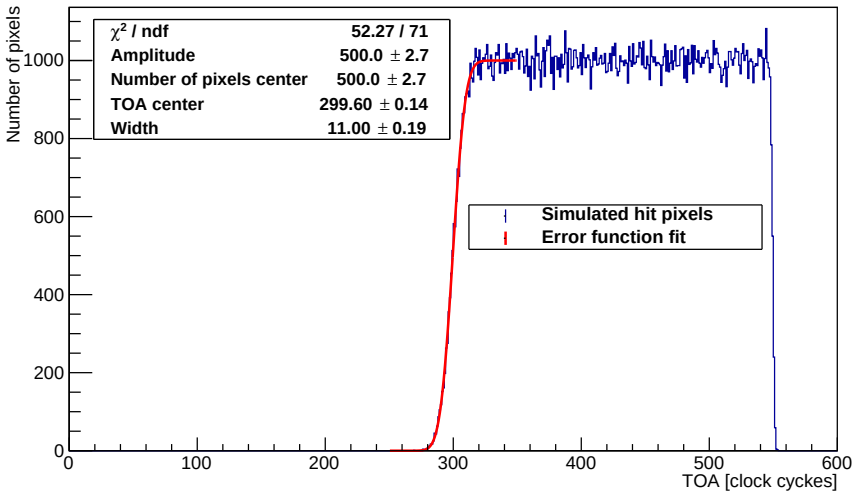



Figure 8.17: Simulated TOA spectrum. The distribution is a superimposition of 1000 random Gaussian distribution in an interval from 300 to 550 clock cycles. The lower edge of the spectrum is fitted by a s-curve function.

### 8.2.3 General remarks on track reconstruction

The cleaned data was processed further in order to reconstruct tracks, from which the physics parameters can be gained. In general, track reconstruction consists of two parts. First, track candidates are searched for by a track finding algorithm. This includes the separation of double tracks and the correct assignment of hits to the tracks. Hence, this part is the most critical and difficult one. The second step is the track fitting, where the assigned hits are fitted and a more accurate track is obtained. Optionally as a third step, the hits can be reassigned to the track in order to remove outliers or add hits, which are close to the more precisely fitted track.

There are already some processors with track finding and fitting algorithms implemented in the framework `MarlinTPC` which can cope with data from pixelised readout, see [164]. They can be divided in global approaches, where all hits are taken into account, and local approaches, where track segments, called tracklets, on a single chip or octoboards are reconstructed. Tracklets are then combined to a complete track. In this preliminary analysis, only global approaches have been used, as the processors for local approaches were not so well developed and did not perform reliably.

Most of the global track finders rely on a specific track model. The simplest one is the straight track model. It has the drawback that curved tracks cannot be found. For data taken without magnetic field where no curvature is expected, this still is a valid approach. A Hough transformation-based method was used and will be explained in the next section.

For curved tracks of high momentum particles, a straight line is still sufficient as a track candidate. The track fitter can still fit a curved track to the hits assigned by the finder. This has been tried, and, in combination with a reassignment of hits after fitting, led to satisfying results for a typically slightly curved track in the test beam data. However, tracks of scattered or lower momentum particles, curlers and delta electrons cannot be identified this way. Therefore, a concept for a new global track finder for curved tracks was implemented (see Appendix E). The results of the analysis of reconstructed curved tracks are shown in Section 8.2.6 and 8.2.7.

### 8.2.4 Straight track reconstruction

The processor chain to reconstruct straight tracks in runs without magnetic field is shown in Figure 8.18. First, the data is transformed from `TrackerData` to `TrackerHits` by the `InGridSimpleClusterFinder`. It requires the `GEAR` file, which holds the geometrical information of the TPC including the position of every pixel. This file has been generated based on microscope measurements of the modules [78]. The significant difference between the two formats is that `TrackerData` only holds the information of each pixel, while `TrackerHits` are physical hits according to the spatial position. These are three dimensional coordinates, of which x and y are given by the pixel position derived from the `GEAR` file. The z-position is calculated by Equation 2.10. The drift velocity is taken from a Magboltz simulation for the exact gas parameters, while the drift time $t_d$ is derived from the TOA counts as expressed in Equation 8.2.

For track finding, the `TimePixHoughTransformNormalProcessor` is used. As the name suggests, it finds tracks by a Hough transformation. It is performed in two dimensions and straight track candidates are only found in the xy plane. The hits are assigned on basis of their distance to the track. With the track candidate as seed, the `LinearRegressionProcessor` performs a three dimensional linear regression on the assigned hits. Afterwards, a reassignment of hits is done. By the `TimePixTrackEventDisplayProcessor`, the found tracks with their hits are displayed. An example of a typical track can be seen in Figure 8.19, where the track and hits are shown in the xy plane. Displays of the other two planes are shown in Figure 8.20.

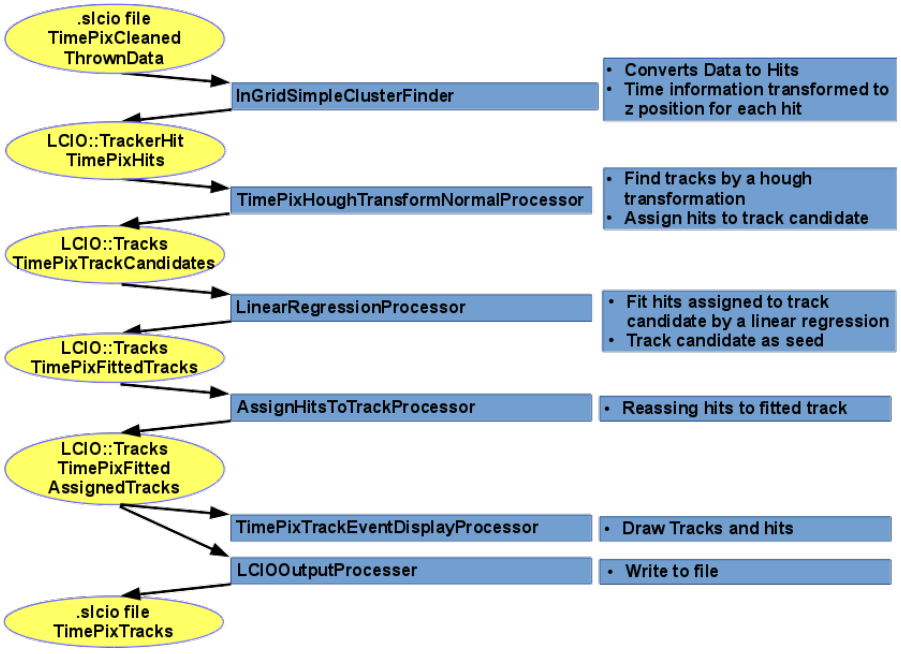
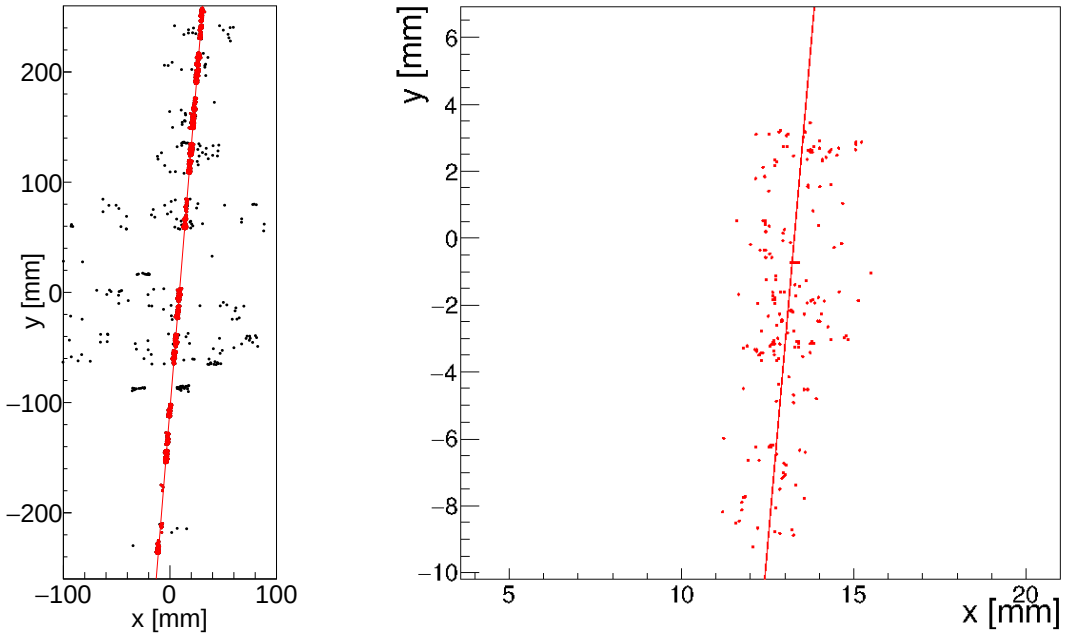


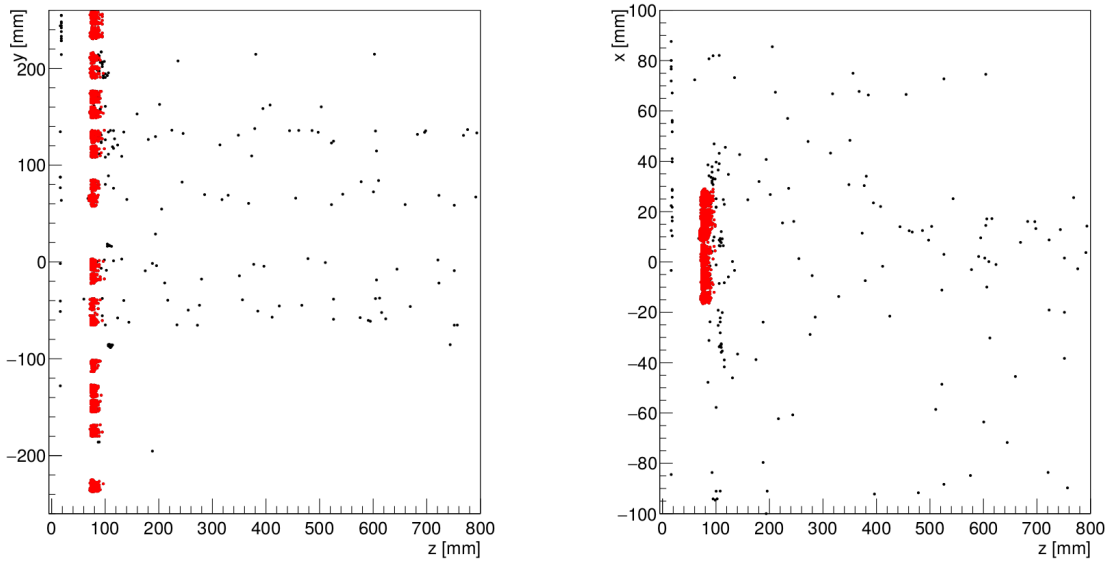

Figure 8.18: MarlinTPC processor chain to reconstruct straight tracks.




(a) Display with both axes to scale.

(b) Zoom on the reconstructed track with the assigned hits.

Figure 8.19: Display of a reconstructed straight track in the xy plane. The red line resembles the track and the red dots the assigned hits. The hits marked in black have not been assigned to the track.




(a) Display of assigned hits in the yz plane.

(b) Display of assigned hits in the xz plane.

Figure 8.20: Display of the hits assigned to a reconstructed straight track in the xz and yz plane.

### Field distortions and misalignment

With the found tracks and assigned hits, the properties of the detector can be explored. As for the 2013 test beam, first the residuals were analysed. Those are the distances of the assigned hits to the track. The distribution of the residuals reflects the diffusion and detector resolution. By definition, it should have a mean value of zero, if the linear regression is performed correctly. This requirement has to be fulfilled even for short intervals of the track. Therefore, the residuals are also analysed in small binned intervals in the direction of the track. Figure 8.21 shows the xy-residual distribution colour coded along the y direction. For the particular run shown, the beam was almost parallel to the y axis. The different chips are distinguishable and it can be seen that the residual distribution differs significantly along the y axis.

The mean value of the residual distribution in each interval is shown in Figure 8.22. In this plot, the y axis is displayed by the bin number.

As has been seen in the 2013 analysis, field distortions can be identified through this plot. However, especially the structure on the right side of the plot, which corresponds to the top module, cannot be due to field distortion. The mean values differ from zero with a linear increase from the center of the module. The same structure, but less prominent, can be seen for the chips of the lower module on the left side of the plot. Such a structure can only stem from systematic displacements of the hits on the modules. In fact, such an effect was expected to appear at that stage of the analysis.

### Alignment correction

The reason for the systematic displacements is that in fact the chip positions were accurately measured by the microscope on a single module [78], but the exact positioning of the modules with respect to each other could not be measured. Hence, the ideal position as in the CAD design was used. The

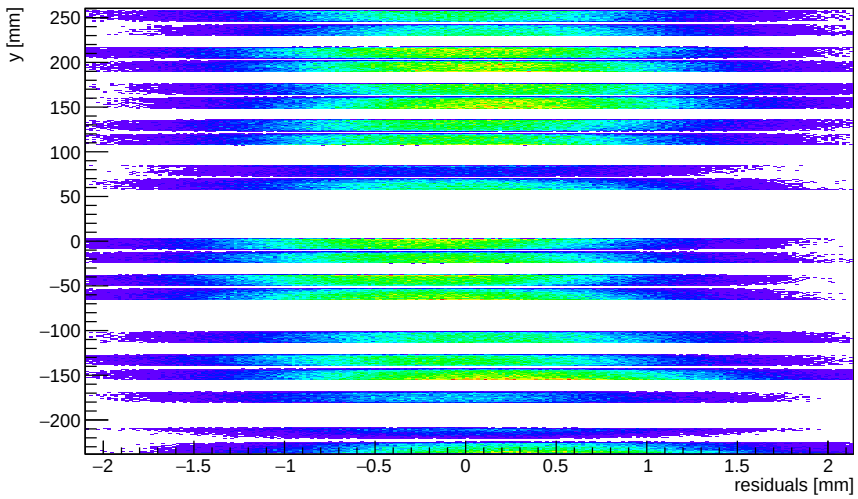



Figure 8.21: xy-residuals along the y axis without field distortions and alignment corrections. Run parameters: $B = 0\,\mathrm{T}$, $E_{drift} = 230\,\mathrm{V\,cm^{-1}}$, $z \approx 28\,\mathrm{mm}$.

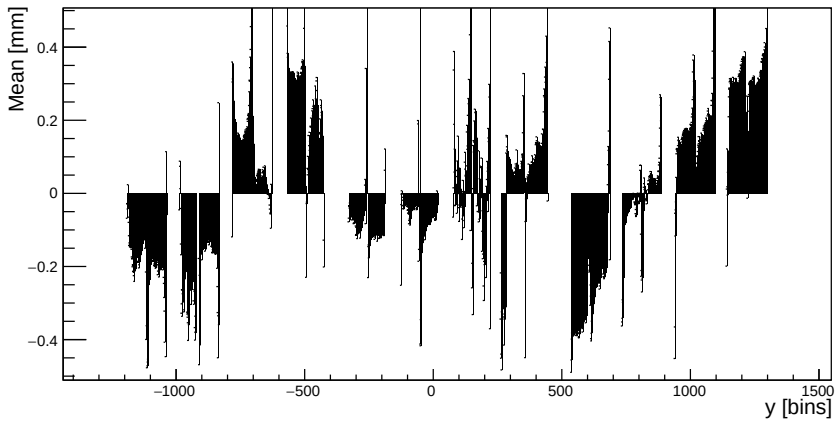



Figure 8.22: Mean value of the xy-residuals along the y axis without field distortions and alignment corrections. Run parameters: $B = 0\,\mathrm{T}$, $E_{drift} = 230\,\mathrm{V\,cm^{-1}}$, $z \approx 28\,\mathrm{mm}$.

GEAR geometry only holds an approximate estimate of the relative position of the modules. The correct alignment has to be performed by the analysis of straight tracks. A satisfying result can be obtained when both the top and bottom module are rotated by 0.008 rad or 0.92°. Clearly, the alignment needs to be studied in a more detailed analysis.
With a new GEAR file including the rotation of the modules, the track reconstruction was performed again. The mean residuals of the realigned modules are shown in Figure 8.23. The characteristic structure has disappeared. Still, the alignment is not perfect. For example in the right part of the plot, the mean residuals are systematically positive. A shift of the top module might lead to an improvement.

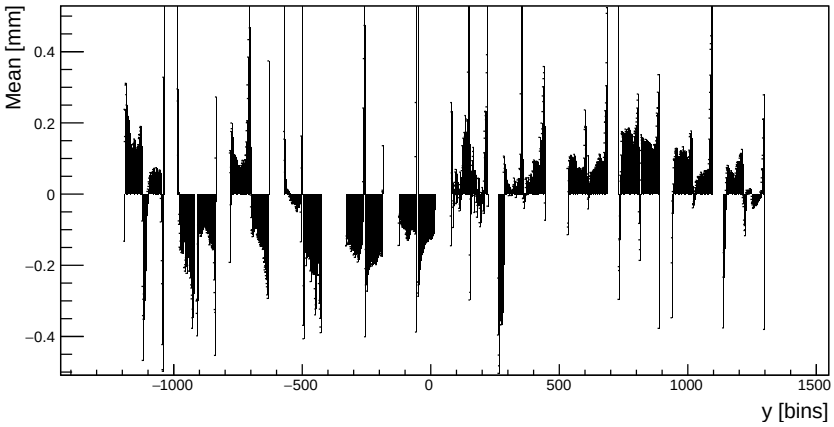



Figure 8.23: Mean value of the xy-residuals along the y axis without field distortions correction. The alignment of the modules has been modified. Run parameters: $B = 0\,\mathrm{T}$, $E_{drift} = 230\,\mathrm{V\,cm^{-1}}$, $z \approx 28\,\mathrm{mm}$.

#### Field distortion correction

From the results of the 2013 test beam it is obvious that the shift of the mean residual value also stems from field distortions. The effect of field distortions cannot be disentangled from the effect of misalignment very easily. As in the case of a detector without field distortions and a perfect alignment, the mean residual value would be zero in all binned intervals along the track, the mean residual offset can be used to correct for the field distortion. Also the still remaining misalignment will be corrected at least along the axis perpendicular to the beam. When this is done, the performance of the detector can be extrapolated to this ideal setup. To correct for the field distortions, an improved version of the correction algorithm used in the 2013 analysis was used [164]. A complete compensation of the mean deviations from zero cannot be expected, as the algorithm was designed for tracks along chips in a row. Figure 8.24 shows the mean residuals after the correction. The mean residual offset is reduced by a factor of two, but not completely compensated, so there is still some room for improvement.

### 8.2.5 Detector performance analysis with straight tracks

In a preliminary analysis, several detector properties were evaluated. Therefore, the reconstructed tracks were used as input for processors in `MarlinTPC` designed to generate displays of physics properties. Figure 8.25 shows the different processors. Form the large data set, a limited number of runs was selected for the analysis presented here.

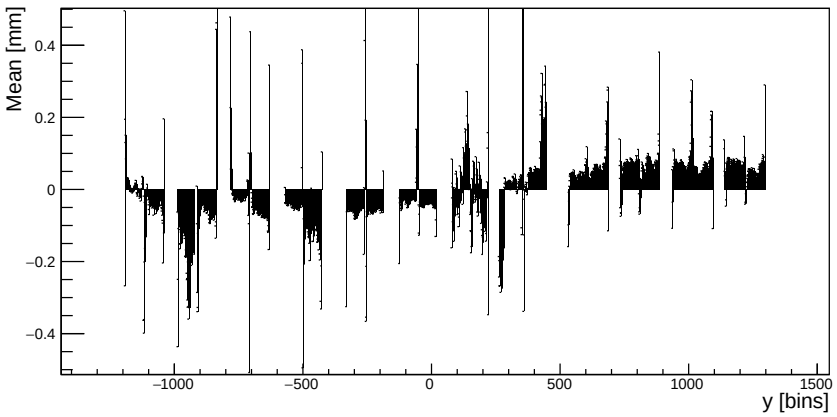



Figure 8.24: Mean value of the xy-residuals along the y axis with field distortions and alignment corrections. Run parameters: $B = 0\,\mathrm{T}$, $E_{drift} = 230\,\mathrm{V\,cm^{-1}}$, $z \approx 28\,\mathrm{mm}$.

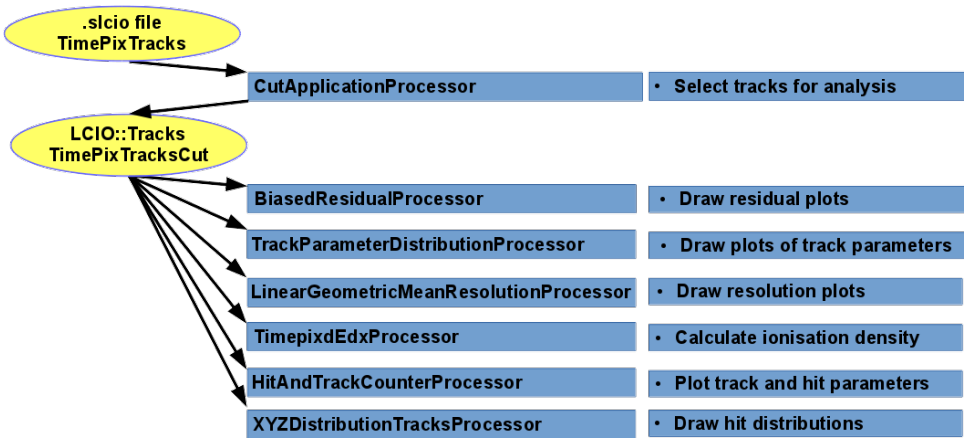



Figure 8.25: MarlinTPC processors in the analysis chain for tracks to evaluate the detector performance.

**Data selection** Z-Scans are particularly useful to study properties for different drift distances. The already aforementioned runs 90 to 105 without magnetic field, a drift field of 230 V/cm and clock frequency of 40 MHz were selected. Only events with one single track with at least 1200 hits were accepted for the analysis. By cuts on the track angle to the y-axis ($\phi$) and distance of the track to the origin ($D_0$), only tracks in the beam axis were selected. Table 8.3 shows the effect of the cuts for run 102. The finally accepted tracks are mainly selected by the single track per event cut, which rejects 65 % of the found tracks and is meant for a simplification of the analysis. The only cut applied afterwards that has a significant effect on the selected tracks is the $D_0$ cut. For that variable, stringent limits have been set to select only tracks in a narrow region of the beam to increase the effect of the field distortion corrections.

| Cut | none | + single tracks | + $\phi$ | + $D_0$ | + number of hits |
|---|---|---|---|---|---|
| Number of accepted tracks | 12401 | 4322 | 4224 | 3419 | 3418 |
| Accepted tracks [%] | 100 | 35 | 34 | 28 | 28 |

Table 8.3: Effects of the data selection cuts on the number of accepted tracks in run 102. The cut flow is from left to right. The "+" implies that the cut in the column was added to the previous ones.

**Track parameters** In the following figures, parameters of the reconstructed tracks are shown. As an example, run 102 was selected. For that run, the beam was about 75 mm away form the anode ($Z_0$ in Figure 8.26a). Each distribution is shown for the complete data set and for the tracks left after cuts. In the geometrical parameters of the track $\phi$ in Figure 8.26b, $D_0$ in Figure 8.26c and the inclination of the track towards the endplate plane $\lambda$ in Figure 8.26d, the peak from the beam can be seen.

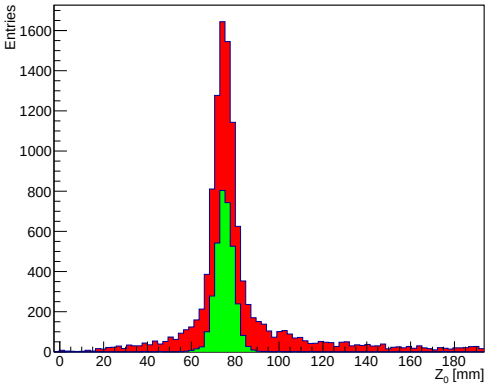
The number of tracks per event can be seen in Figure 8.27a, where after the cut all events with more than two tracks are assigned to the bin with zero tracks.

Comparing the number of hits per event in Figure 8.27b to the number of hits per track in Figure 8.27c, on can see that both distributions peak at about the same position and have a similar shape towards high hit numbers. From this one can deduce that most of the hits recorded belong to tracks and only little noise is left after data cleaning. It can also be seen that a typical track has about 3000 hits.

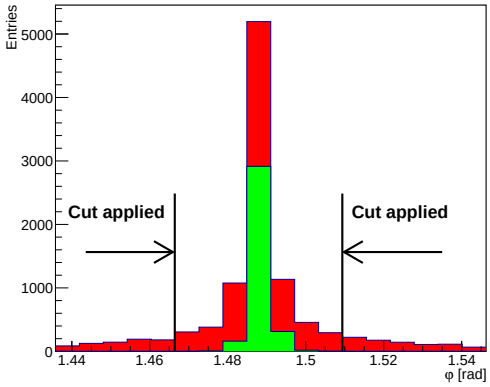
The track length distribution can be seen in Figure 8.27d. It peaks at the maximal track length recordable with the setup at 500 mm. This is expected as in run 102, the TPC was arranged such that the beam passes over all three modules.

From the number of hits on a track and the track length, the number of hits per track length can be calculated for each track. The distribution for all tracks is shown in Figure 8.28. However, the number needs to be corrected, as the gaps between the chips are included in the track length. The effective track length, which is covered with pixels where electrons can be registered is about 33.6 cm (24 chips, each with about 1.4 cm length). Taking the inactive chips along the beam axis into account, the effective track length reduces to 28.0 cm (20 active chips). In order to measure the ionisation along the track, this needs to be considered.

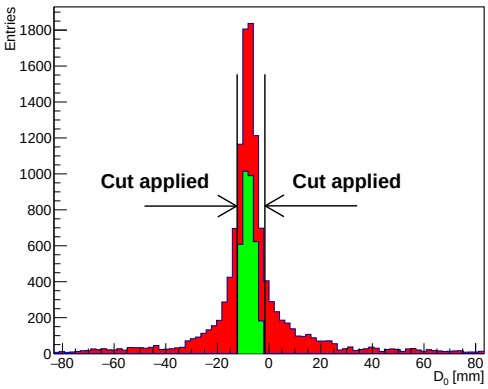
The effect of the cuts can be seen by comparing the track parameter distributions of the complete dataset depicted in red and the selected dataset in green. Short tracks with few hits and off from the main beam axis are rejected. After the cuts, only the longest possible tracks restricted to a defined area on the modules are left. Those have been selected as they have similar features and are suited for the analysis of physics and performance parameters.



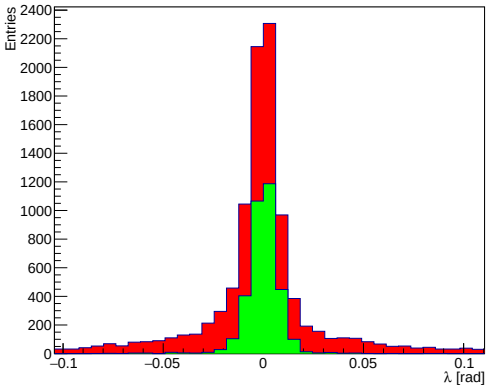

(a) Track distance to the endplate ($Z_0$) distribution.




(b) Track angle in the xy plane to the y plane ($\phi$) distribution.$\phi$ was used as cut variable.

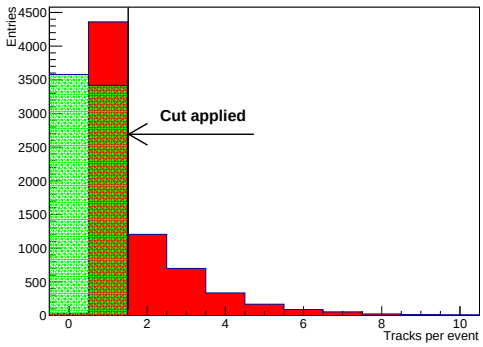



(c) Minumum distance of the track to the origin ($D_0$) distribution. $D_0$ was used as cut varialbe.

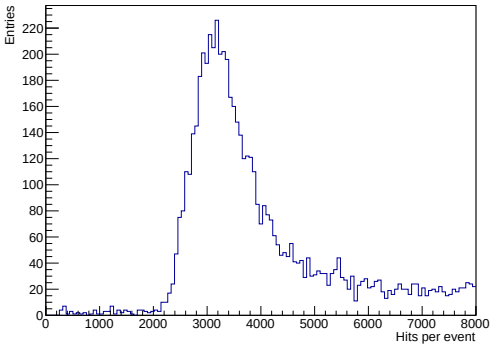



(d) Inclination ange of the track towards the endplate ($\lambda$) distribuiton.

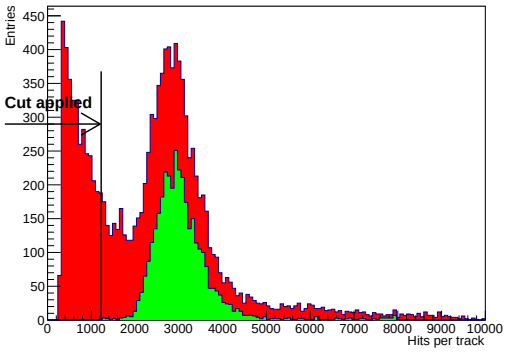
Figure 8.26: Geometrical track paramenters for the complete (red shaded) and cut (green shaded) dataset of run 102.



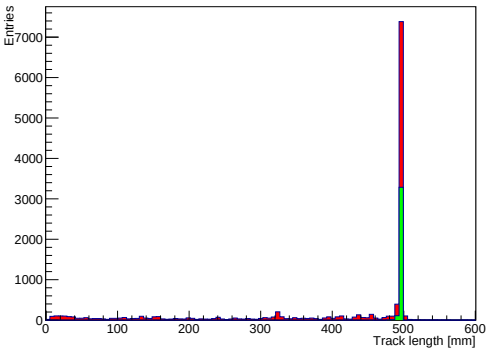

(a) Tracks per event distribution. The number of tracks per event was used as cut variable.




(b) Hits per event distribution for run 102. As this paramenter is based on events, the cuts have no influence.




(c) Hits per track distribution. Only tracks with more than 1200 hits were selected for the final analysis.




(d) Track length distribuiton. With the setup, the tracks can be 500 mm long at most and including the gaps between chips.

Figure 8.27: Track and hits paramenters for the complete (red shaded) and cut (green shaded) dataset of run 102.

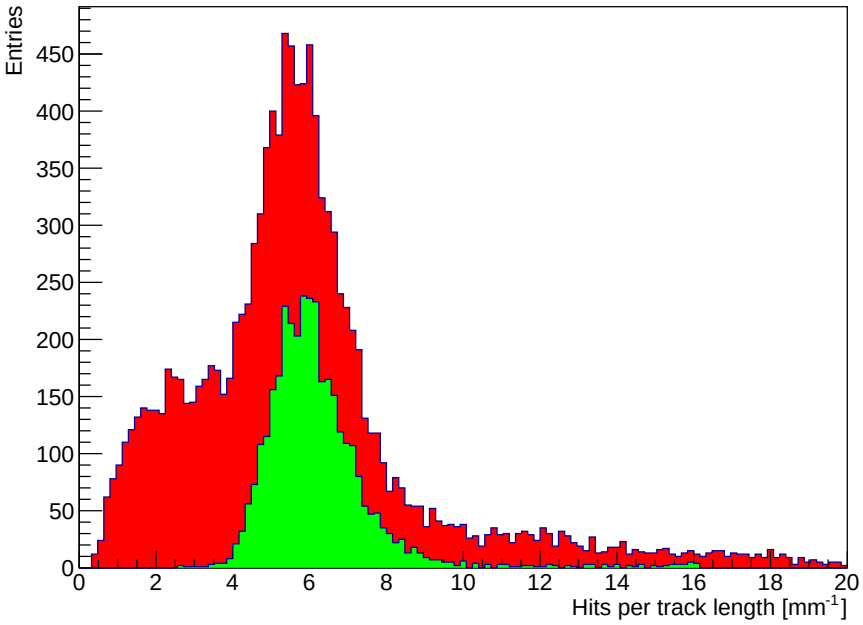
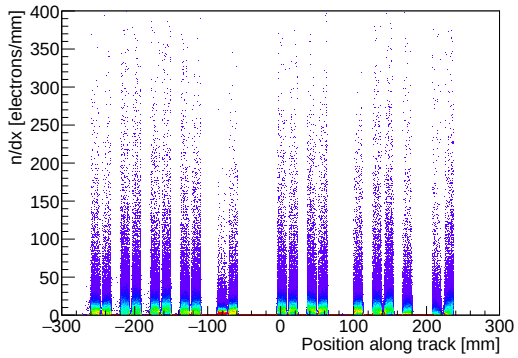


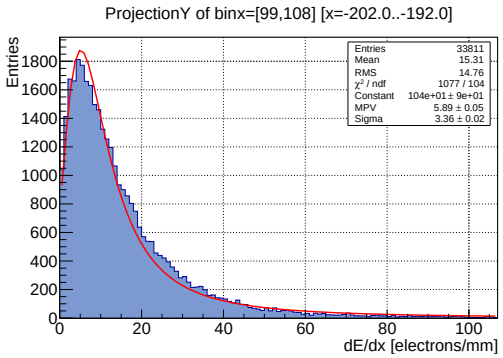

Figure 8.28: Hits per track length distribution for the complete (red shaded) and cut (green shaded) dataset of run 102. The track length also includes the gaps between chips.

**Energy loss** Because of the high single electron detection efficiency in case of sufficient diffusion provided by the InGrid, the energy loss $dE/dx$ of the primary particle can by measured by counting the number of hit pixels per track length. From Figure 8.28, a corrected mean value of about 107 electrons/cm is calculated, which is consistent with what is expected for T2K gas. However, this method only gives a total number of measured primary electrons on the complete track with a rough estimate of the effective track length. The resolution calculated for the mean and rms values of the distribution is (23.9 ± 0.7) % for the selected data. A fit to the peak[2] results in a resolution of (15.4 ± 0.7) % ($\sigma_{fit}/mean_{fit}$).
The energy loss was studied in more detail by looking into the individual contributions exemplary for run 102. Therefore, the number of hits were counted in intervals along the track. The interval length was set to 1 mm. Figure 8.29a shows the number of hits in the slices along the track. The different chips along the track can be identified. In Figure 8.29b, the projection of a 10 mm wide central chip region on the n/dx axis is shown. A Landau-like distribution can be observed as expected, see Section 2.4.1.
For each track, the number of hits in all intervals along the track were averaged to obtain a measure for the hit density. Figure 8.30a shown the result for a complete run. A resolution of (14.0 ± 0.3) % is obtained in the peak.
As the number of primary electrons per track length follows a Landau-like distribution, the average is dominated by the high energy deposits. To find an improved measure for the hit density, a truncated mean method similar to [167] was applied. For each track, only a subset of all intervals was used in the average. Different truncations were tried: rejecting a defined number of highest deposits, rejecting a defined percentage of highest deposits or rejecting a defined percentage of highest and lowest deposits.

[2] Besides the peak, there is a small contribution from not correctly reconstructed tracks with about the double amount of hits. Those stem from double tracks, which are that close that they were not separated.



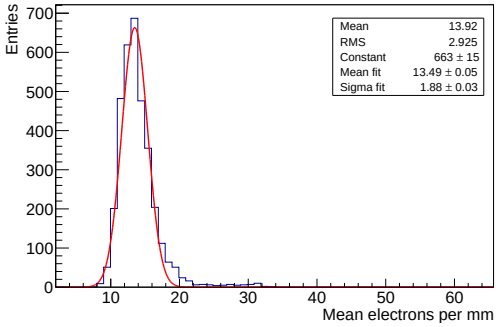

(a) Number of hits in slices along the track.



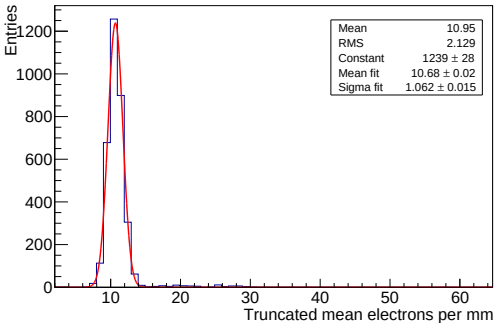

(b) Projection of Figure 8.29a on the n/dx axis for a 10 mm wide region in a chip center fitted by a Landau distribution.

Figure 8.29: Number of hits along the track in 1 mm slices along the track.

It was also tried to only accept intervals in the central region of the chips or truncate on basis of complete chips. The best result with a resolution of $(9.9 \pm 0.5)\,\%$ in the peak was obtained by rejecting the 5 % highest and 5 % lowest deposits in all intervals, see Figure 8.30b. However the results of most of the other methods were within a two sigma range.




(a) Mean number of hits in intervals of 1 mm along the track with a resolution of $(14.0 \pm 0.3)\,\%$ in the peak fitted by a Gaussian distribution.




(b) Truncated mean number of hits in intervals of 1 mm along the track with a resolution of $(9.9 \pm 0.5)\,\%$ in the peak fitted by a Gaussian distribution.

Figure 8.30: Energy loss distributions fitted by a Gaussian curve.

To compare the value with an expectation, the Photo-Absorption Ionisation (PAI) model used by Allision and Cobb [168] is taken into account. For pure argon they provide an approximation[3] for the expected resolution $R$ in % Full Width at Half Maximum (FWHM) of

$$R = 96 n^{-0.43} \, (xP)^{-0.32} \,, \tag{8.4}$$

where $n$ is the number of measurements along the track, $x$ is the interval length in cm and $P$ is the gas pressure in atm. As can be seen in Figure 8.31, the formula gives a good estimate for the expected $dE/dx$ resolution of experiments which differ significantly in all of the three parameters.

[3] In the original publication [168], the exponent for $n$ was −0.46. In recent publications [169], the value −0.43 derived in [170] is stated.

| det. | $n$ | $x$(cm) | $P$ | exp. | meas. |
|---|---|---|---|---|---|
| Belle | 52 | 1.5 | 1 atm | 6.6% | 5.1% ($\mu$) |
| CLEO2 | 51 | 1.4 | 1 atm | 6.4% | 5.7% ($\mu$) |
| Aleph | 344 | 0.36 | 1 atm | 4.6% | 4.5% ($e$) |
| TPC/PEP | 180 | 0.5 | 8.5 atm | 2.8% | 2.5% |
| OPAL | 159 | 0.5 | 4 atm | 3.0% | 3.1% ($\mu$) |
| MKII/SLC | 72 | 0.833 | 1 atm | 6.9% | 7.0% ($e$) |

Figure 8.31: $dE/dx$ resolution as measured for different experiments in comparison with the result obtained from Equation 8.4, from [169].

For the truncated mean method explained before, 280 slices of 1 mm (effective track length of 28 cm) have been taken into account and the expected $dE/dx$ resolution from Equation 8.4 is given by 7.57 % $\sigma/mean$[4] which can be compared to the measured value of (9.9 ± 0.5) %. Hence with the method presented, a resolution which differs by 31 % from the approximation by [168] can be reached. The algorithm can possibly be improved to find an even better measure for the energy loss. In [168], the intervals typically have a size of about a cm, so it is not clear if the approximation is still valid.
Note that in case complete chips are taken as basic interval of 1.4 cm and the number of slices is reduced to 20, a resolution of 10.12 % is obtained from the equation for the same effective length.

**Transverse and longitudinal spatial resolution** For the aforementioned z-scan, the residuals were investigated. As explained in Section 7.2.3, the detector resolution can be measured by comparing the measured residuals to the expected ones by diffusion only. Different measures for the resolution were evaluated, of which the results are shown in Figure 8.32:

- For the 3 sigma method (data points marked with black filled squares), the residual distribution of tracks fitted to all N hits is fitted in a range of 3 RMS around the mean value. From the fit, the sigma value $\sigma_N$ is taken as a measure for the width of the residual distribution. The obtained values are consistent with the single electron diffusion.

- The data points marked with green squares also take the residual distribution of tracks fitted to N-1 hits (see Section 7.2.3) into account. Also this distribution is fitted in a 3 RMS range around the mean value and the sigma value $\sigma_{N-1}$ is taken. As the final measure $\sigma_{N*N-1} = \sqrt{\sigma_N \sigma_{N-1}}$ is taken. It can be seen from Figure 8.32 that no difference to the previous method can be observed. This is expected as the difference between $\sigma_N$ and $\sigma_{N-1}$ is measured to be smaller than 0.2 % for tracks with 3000 hits.

- The N*(N-1) method does not use fits to the residual distributions, but just the RMS values. This method was also used in the 2013 analysis. It is shown as the data points marked with red filled triangles.

The data points measured by the last method were taken into account for the fit by the function given in Equation 7.5. From the fit, a single point resolution for zero drift distance $\sigma_{xy,0} = (0 \pm 276)$ µm (negative values are not physically meaningful) and a transverse diffusion constant $D_T$ of (327.5 ± 1.5) µm/ $\sqrt{\text{cm}}$ is obtained. The large error of the single point resolution is due to the lack of measurements close to the anode because of the trigger delay and the rising slope towards $z = 0$. The obtained transverse

[4] Assuming a Gaussian distribution, the FWHM value can be converted to $\sigma/mean$ through division by a factor 2.35.

diffusion constant is consistent with the value given by simulations for the conditions through the z-scan $D_{T,sim} = (324 \pm 12)\,\mu\text{m}/\sqrt{\text{cm}}$. Since the error on $\sigma_{xy,0}$ is large, no conclusion can be drawn from the fitted value. The shape of the fitted curve in comparison to the single electron diffusion hints on the resolution of the detector: All points are slightly above the optimum value given by diffusion. Hence, the resolution is completely dominated by diffusion, which is physically possible for a pixelated readout, as the intrinsic spatial resolution is $55\,\mu\text{m}/\sqrt{12} = 15.9\,\mu\text{m}$.

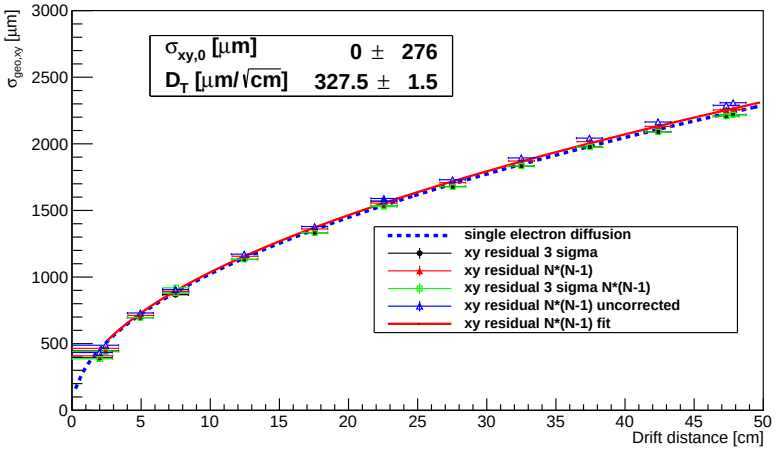



Figure 8.32: Transverse spatial resolution obtained by a z-scan with $B = 0\,\text{T}$ and $E_{drift} = 230\,\text{V/cm}$. The z-position for each run was deduced from the reconstructed tracks. For each run at a given z-position, the residuals were evaluated by different methods. For the fit of the results from the N*(N-1) method, the first two data points were not taken into account, as only an upper limit for the z-position can be deduced.

The points shown in blue in Figure 8.32 are obtained from the residuals without a correction for field distortions and are already close to the limit. For the measurement without magnetic field, the field distortions effects are smaller than expected when comparing to [144].

The result of the analysis of the longitudinal spatial resolution is shown in Figure 8.33. For each run, the residuals of the fitted track without the hit under investigation $\sigma_{N-1}$ have been taken. To minimise the effect of time walk, only the left side of the residual distribution has been fitted. As expected for a sampling frequency of 40 MHz, the longitudinal resolution is dominated by the resolution of the time measurement (about 750 µm, see Section 7.2.3) and possibly field distortions in z-direction and resembles what has been observed in the 2013 analysis. An interesting feature in both analyses is the rise towards very low drift distances. It is probably due to the hodoscope effect or the fact that by longitudinal diffusion, some electrons arrive before the shutter is open which at a first glance would narrow the left edge of the residual distribution. However in this case, the hits with large time walk have a stronger influence on the reconstructed z-position of the track. Thus, the residual distribution is widened also in the left edge.

The significant influence of the time resolution should be absorbed in $\sigma_{z,0}$ and hence a correct longitudinal diffusion constant is expected from a fit with the equivalent to Equation 7.5. However from the fit, the obtained value of $(280 \pm 4)\,\mu\text{m}/\sqrt{\text{cm}}$ is not in agreement with $(224 \pm 9)\,\mu\text{m}/\sqrt{\text{cm}}$ form simulation. Hence there could be an influence of other effects or the assumptions made to derive Equation 7.5 are not valid for a time resolution in the same order as the diffusion for large z-positions.

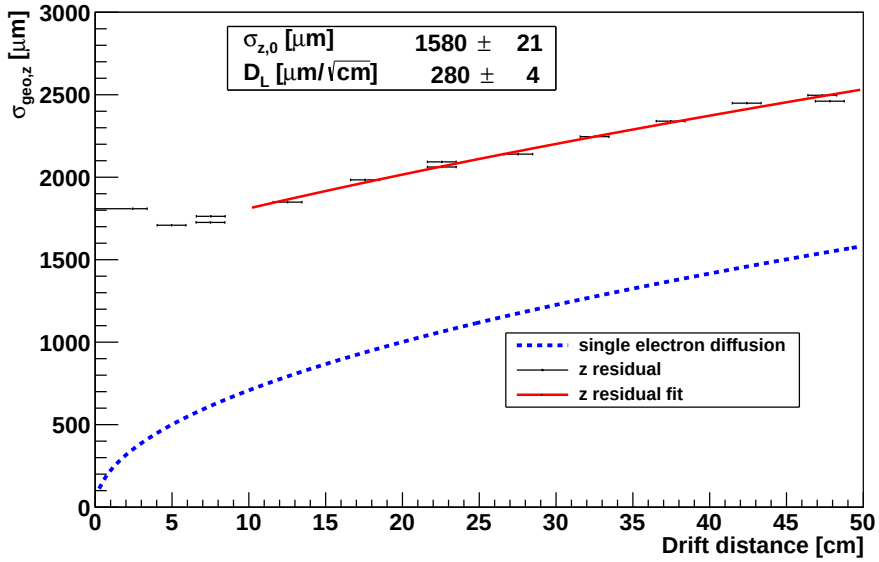



Figure 8.33: Longitudinal spatial resolution obtained by a z-scan with $B = 0\,\mathrm{T}$ and $E_{drift} = 230\,\mathrm{V/cm}$.The z-position for each run was deduced from the reconstructed tracks. For each run at a given z-position, the residuals were evaluated from the track with N-1 hits only. The effect of time walk is minimised as in [144]. For the fit, the first data points were not taken into account.

**Delta removal** If the region of high ionisation, caused by a delta electron, is assigned to a track, the high number of hits from that region have a significant influence on the track fitting. The identification and removal of delta electrons can improve the correct fitting of a track. The InGrid detector with its high granularity can resolve such high ionisation regions even when the delta has not completely left the track vicinity and the diffusion is not too large.

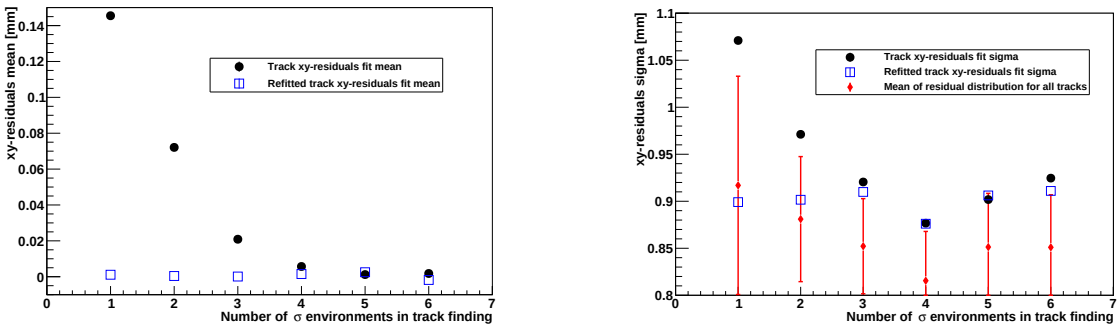
As a first very generic approach to remove hits that could possibly stem from delta electrons, the track finding and fitting was studied for different parameters that control the assignment of hits to the track. Those parameters define the allowed spread of assigned hits around the fitted track or track candidate in steps of sigmas expected from the diffusion.

To measure the effect, the xy-residual distribution was evaluated. As an example, again run 102 was used. For the z-position of 75 mm a width of one sigma is equivalent to 881 μm. As standard value, both the assignment and the track finding is done with a width of four sigma.

First, the effect of limiting the assignment of hits after the fitting was studied for widths of one, two, three, four, five and six sigma. The width for track finding was left at the standard value. As expected, the tails of the residual distribution are cut off but the fitted width is unchanged. Only in the case of an assignment of hits with a width of one sigma the fitted residual width decreases. The same results were obtained when the tracks were refitted after the assignment. Hence, this method is not suitable to improve the performance

As a second method, the assignment of hits by the track finder was studied for the different sigma widths. This has a direct impact on the track fitter, as it only uses the hits assigned by the track finder to fit the track. Decreasing the width for the assignment of hits also decreases the number of hits of the track. Possibly, an optimum sigma value can be found, where the hits of the ionisation by the primary particles are assigned to the track, but the ones from deltas are rejected. The reassignment after fitting was left at the standard value.

A first interesting observation, when increasing the sigma width from one to six is that the mean value of the residual distribution decreases and approaches zero, see the black points in Figure 8.34a. This might be due to the fact that when the number of hits per track decreases, the fit becomes less accurate and the reassigned hits differ from the track fitted to the central hits only. If the track is refitted after the reassignment, the residual mean value is constant and close to zero (blue points).
Next, the width of the residual distribution was evaluated by a Gaussian fit, of which the sigma is shown in Figure 8.34b as the black points. The errors on the fitted sigmas (0.2 µm) are too small to be displayed. As expected, the width decreases, when the fitted track becomes more accurate. However for a sigma larger than four, the width increases again. The resolution is at an optimum for an assignment of hits in the track finder of four sigma. For the refitted tracks (blue points), there is no decrease but also a minimum.
Now the question is, whether the minimum is significant. From the error bars given by the fit, the significance is given because of the high statistics in the residual distribution. But the fluctuations from run to run because of external influences can be by far larger. Therefore, the fluctuation of the residual width for the different tracks of a run was evaluated. From the distribution of track residual widths, a fluctuation and a mean value is given, which is also plotted in Figure 8.34b as the red dots with error bars resembling the fluctuations. Again, a minimum can be seen, which is not significant, as the fluctuations are large.




(a) Fitted mean value of the xy-residual distribution.

(b) Fitted sigma value of the xy-residual distribution.

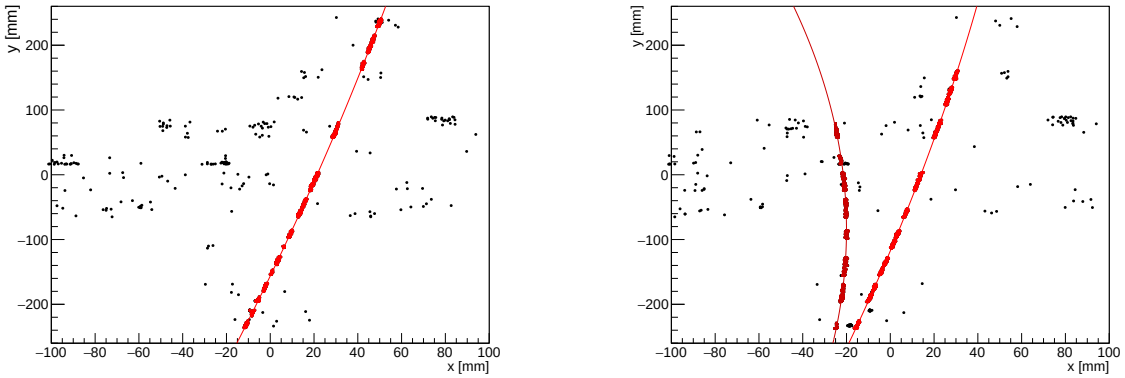
Figure 8.34: Track resolution for different hit assignment widths.

In general, the result can be a hint that there might be an optimum sigma value for the assignment of hits in track finding. By chance, it is the same number as the standard value.
Anyhow, with this very simple method, delta electrons cannot be identified and only the effect is minimised. More sophisticated methods are needed, which could be based for example on the number of hits in small intervals along the track as have been used for the energy loss measurement. Then the identified region of high hit density needs to be further investigated in order to decide if it should be excluded for track fitting.

### 8.2.6 Curved track reconstruction

The reconstruction of curved tracks is by far more demanding concerning computing power and the algorithm. In MarlinTPC there were two track finders suitable for finding curved tracks on pixel data. The Row Based Fast Hough Transformation Processor (FHT) [171] is written for pad-based readout with an interface to pixelised readout. This interface was coded explicitly for the single octoboard

module and cannot be extended to the more complex structure of staggered boards. The algorithm itself has a preferred track direction (perpendicular to the pad rows) and hence is not adequate for the analysis presented here.
The Timepix Windowed Randomized Hough Transform (WHT) can find short, straight track segments and combine them with the `CombineTracksProcessor` also to curved tracks [164]. However, it has problems for regions with a high density of hits and needs a large set of parameters optimised for the specific conditions.
So far, there was no need for a curved track finder, as the tracks on pixelised readout were at most 5.6 cm long, on which the curvature is not prominent. For the first time, the two aforementioned track finders were tested on data with longer tracks. The FHT was not able to find tracks of the pixelised readout with the general geometry. Only when the pixels were treated as pads (such that the interface to pixelised readout was bypassed), the tracks had the correct direction and the input parameters were fine tuned, the processor was able to provide track candidates. The WHT together with the combiner has severe issues to reconstruct long, almost straight tracks with gaps (of non functioning chips). It mainly reconstructed curlers and small track segments from a single long track event.
One possible option to find these long (and almost straight) tracks anyhow would be to use a Hough transformation to find a straight track approximating the curved one as a seed and then fit a curved track. This was tried and led to acceptable results. However, a single curved track was often reconstructed as several straight tracks.




(a) Single track event. The hits marked in red are assigned to the track.

(b) Double track event. The hits marked in red and dark red are assigned to the tracks, respectively.

Figure 8.35: Reconstructed curved tracks.

Therefore a new track finder based on a global approach, the `CircleFinder` (see Appendix E), was developed. In a preliminary state, it behaves better than the other methods and hence was used as the standard track finder for the analysis. An example of reconstructed tracks is shown in Figure 8.35. The reconstruction chain for curved tracks, including the helix track fitter, is shown in Figure 8.36. As for straight tracks, a reassignment of hits after the fit is performed.
An outlook for more adequate general track finding with a local approach will be given in the next chapter.
To briefly estimate the performance of the new track finder, it was compared to the Hough transformation-based method which performs acceptable on curved tracks. Therefore, 100 events were investigated by eye. The set was not preselected and contained empty, single track and multiple track events. Table 8.4

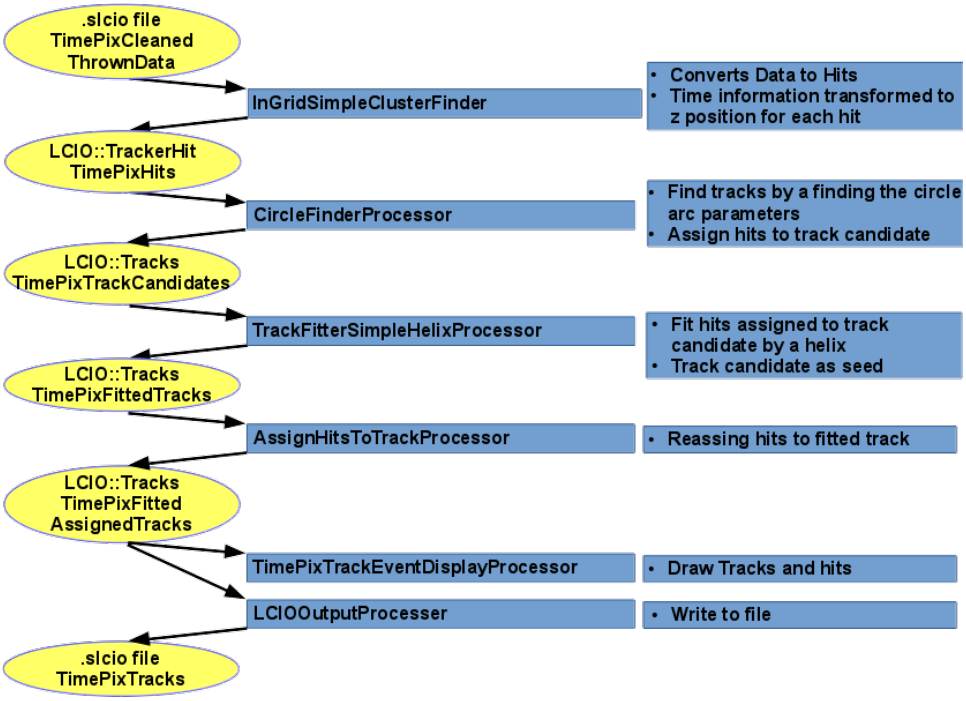



Figure 8.36: MarlinTPC processor chain to reconstruct curved tracks.

summarises the result of the track search in all 100 events. The “eye method” was taken as a reference. A track is marked as found, if the reconstructed track candidate has approximately all hits assigned as would have done by eye. A track is partially found, if a complete segment of the hits has not been assigned to the track. A multiple found track are several reconstructed tracks for a single track found by eye. A fake track is a track, which has been reconstructed, but does not resemble a track found by eye. Finally, a not found track is a track that has been found by eye but not by the reconstruction.

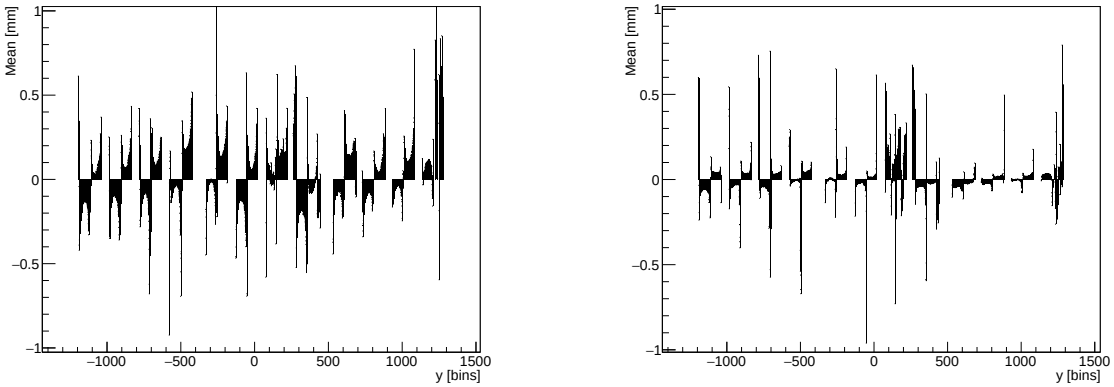
| Track finder method | Found | Partially found | Multiple found | Fake | Not found |
|---|---|---|---|---|---|
| Eye | 109 | 0 | 0 | 0 | 0 |
| `CircleFinder` | 73 | 0 | 1 | 5 | 36 |
| Hough transformation | 54 | 31 | 15 | 11 | 9 |

Table 8.4: Comparison of the performance in track finding of the `CircleFinder` and a Hough transformation in comparison to the human eye as reference.

As expected, the Hough transformation-based method frequently finds only track segments or reconstructs segments as several tracks. About 50 % of the tracks are found with about all hits correctly assigned. Less then 10 % of the tracks are not found. Especially in events with several tracks, fake tracks were reconstructed from segments of different real tracks or noise.

The `CircleFinder` either does not find a track (33 %) or finds the complete track with all hits (67 %). Especially almost straight, long tracks are found which are needed for the further analysis. For the not found tracks, many are due to the fact that the algorithm is in a preliminary state. For example in multiple track events, only the track with most of the hits is reconstructed. Tracks parallel to the x-axis are less likely to be found by the current implementation.

**Field distortions** The field distortion and the misalignment have also be corrected for the data with magnetic field. The uncorrected residual means along the y-axis are shown in Figure 8.37a for run 187. A characteristic u-shape with opposite sign on neighbouring chips can be identified. This shape is known to stem from $\vec{E} \times \vec{B}$ effects and has not been observed in data without magnetic field. The correction algorithm minimises the field distortions in total and also the $\vec{E} \times \vec{B}$ effects, see Figure 8.37b, but the remaining variations from zero are larger than without magnetic field.




(a) xy-residual mean values before correction. The shape of the deviations form zero within a chip indicates field distortions from $\vec{E} \times \vec{B}$ effects.

(b) xy-residual mean values after correction.

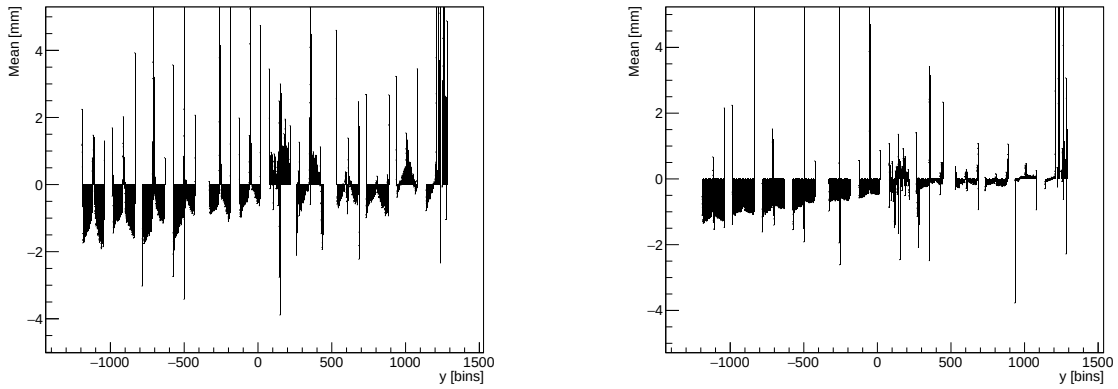
Figure 8.37: xy-residual means for run 187.

Because the longitudinal resolution did not improve as much as expected (see the next section) also the residual means in z-direction were investigated. For those, the mean value is not expected to be zero, as the z-residual distribution is asymmetric due to time walk. Still, the offset should be similar along the beam axis. Figure 8.38a shows the uncorrected z-residual means and a deviation even larger than for the xy-residual means can be seen. Again, a characteristic shape, this time of a triangle, can be identified. The origin is still unknown. Also the different z-position of the InGrids on the octoboard could show up in this plot. From the microscope measurements a maximum height difference of 600 µm has been reported [78].

In order to correct for the distortions, the xy-residual mean correction processor has been modified to correct the z-position of hits. The corrected mean values are shown in Figure 8.38b. The characteristic shape is minimised, but now a systematic global shape becomes visible: a linear increase of the mean values in dependence of the y-position.

Because of the large effect on the longitudinal resolution, a run without magnetic field was analysed again and a similar structure was found. Hence, the triangular shape is not due to $\vec{E} \times \vec{B}$ effects but field distortions. However, a distinctive global shape was not identified in the data without magnetic field.

The global shape can at a first glance only be the effect of an incorrect track fitting when the z-position is taken into account. The finding of no prominent global shape in the $B = 0\,\mathrm{T}$ data, where a different fitter was used, supports this argument. Also here, further investigations are necessary.




(a) z-residual mean values before correction. The shape of the deviations form zero within a chip indicates field distortions.

(b) z-residual mean values after correction.

Figure 8.38: z-residual means for run 187.

### 8.2.7 Detector performance analysis with curved tracks

For a limited number of runs, further detector properties were analysed, which can only be accessed from curved tracks or with magnetic field. The same analysis chain as for the straight tracks could be used.

**Transverse and longitudinal spatial resolution** Similarly to the same measurement for straight tracks, a z-scan (runs 178 to 190, $B = 1\,\mathrm{T}$, $E_{drift} = 230\,\mathrm{V/cm}$, sampling frequency 80 MHz) was selected to evaluate the residual distribution RMS for each run and to access the spatial resolution. The tracks for the analysis were selected by the same cuts as for straight tracks, just the values for the geometrical position had to be changed as the beam was placed at a different position and because of the bending of the tracks. This time, only a single method was used to evaluate the resolution.
Because of the magnetic field, distortions from $\vec{E} \times \vec{B}$ effects and the incomplete correction are expected to result in a spatial resolution not as close to the single electron diffusion as for the data without magnetic field. Figure 8.39 shows the transverse spatial resolution. The improvement in resolution from field distortion corrections is significant, as can be seen from the difference of the data points marked in blue to the ones marked in red. Still, the corrected values do not completely follow the single electron diffusion. The fit provides a reconstructed transverse diffusion constant $D_T$ of $(96.7 \pm 0.9)\,\mu\mathrm{m}/\sqrt{\mathrm{cm}}$ with is consistent with $D_{T,sim} = (96 \pm 5)\,\mu\mathrm{m}/\sqrt{\mathrm{cm}}$ from simulations. The single point resolution for zero drift distance from the fit $\sigma_{xy,0}$, which is still affected by the remaining field distortions, is $(121 \pm 23)\,\mu\mathrm{m}$.

The longitudinal spatial resolution is shown in Figure 8.40. There are three different sets of data points plotted. In red are the values obtained when the z-residual means were corrected. The same data set without corrections results in the data points marked in blue. In fact, the correction slightly increases the resolution. For comparison, the data points from the z-scan with 40 MHz and $B = 0\,\mathrm{T}$ are shown in black. Note that contrary to that z-scan, a sampling frequency of 80 MHz was used here. Therefore an improvement due to the doubled time resolution of about 380 µm is expected, see Equation 7.7. The improvements hold for both factors that contribute to the time resolution (factor 2 in the equation) as

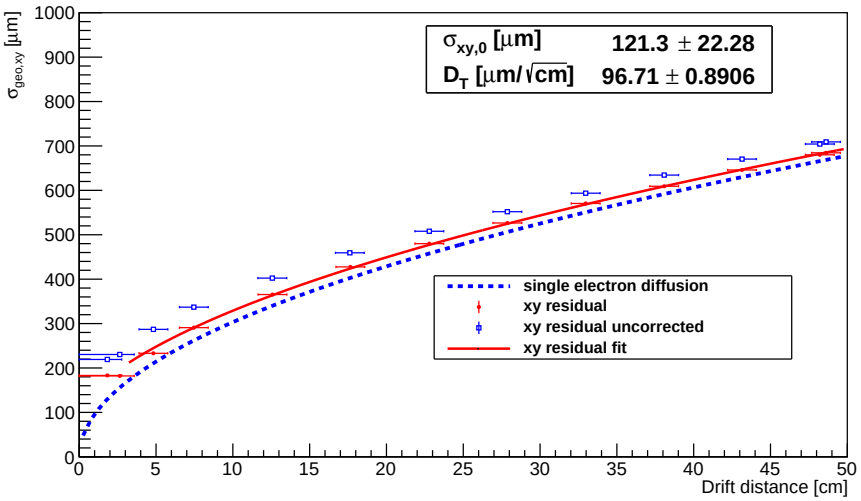



Figure 8.39: Transverse spatial resolution obtained by a z-scan with $B = 1\,\mathrm{T}$ and $E_{drift} = 230\,\mathrm{V/cm}$ and 80 MHz sampling frequency. The z-position for each run was deduced from the reconstructed tracks. For each run at a given z-position, the residuals were evaluated by the N*(N-1) method. For the fit, the first data points were not taken into account.

the reference clock in each pixel which is used to synchronise the hit and shutter signal has a higher frequency, see Section 3.1.2. It has to be mentioned that the external trigger signal from the scintillators which opens the shutter was still sampled with the 40 MHz. The uncertainty on the trigger signal only affects the global time measurement which results in a shift of all hits and hence the complete track. As there is no external reference tracking system, this effect cannot be detected.

As can be seen from the figure, the longitudinal resolution slightly increases but only for large drift distances. For short drift distances, the resolution stays about the same. As has been seen in the previous section where the global shape of the z-residual means has been shown, many effects on the longitudinal resolution have to be studied. Still, the corrected residual values have been fitted. The obtained diffusion constant is $D_L = (237 \pm 4)\,\mu\mathrm{m}/\sqrt{\mathrm{cm}}$, which differs from the simulated value $D_{L,sim} = (225 \pm 6)\,\mu\mathrm{m}/\sqrt{\mathrm{cm}}$. The single point resolution from the fit $\sigma_{z,0} = (1579 \pm 16)\,\mu\mathrm{m}$ is about the same as for the data without magnetic field.

**Momentum resolution** The radius $r$ or curvature $\Omega = 1/r$ of a track in a magnetic field $B$ is related to the momentum of the particle by Equation 2.4. The magnetic field was remeasured after the test beam by the DESY group and it was found out that for the settings used at the test beam, the field was not 1 T, but 1.022 T [172]. This corrected value is used for the momentum calculation. Beforehand, an $\Omega$ distribution is investigated in Figure 8.41a in this case for run 140, in which the particle energy of the beam was set to 1 GeV. A prominent peak for negative values can be identified with a tail towards higher negative curvatures. A negative curvature is associated to negatively charged particles as the electrons from the beam. Additionally, also positively curved tracks were recorded but their curvature is larger than the the one for the negatively charged particles. Positively curved tracks stem from positively charged particles, which are not provided by the accelerator. They hence must have been produced somewhere else. In fact this effect is known and expected, as the beam has to pass through the material of the magnet and the TPC wall and can undergo scattering and also pair production. This is also the

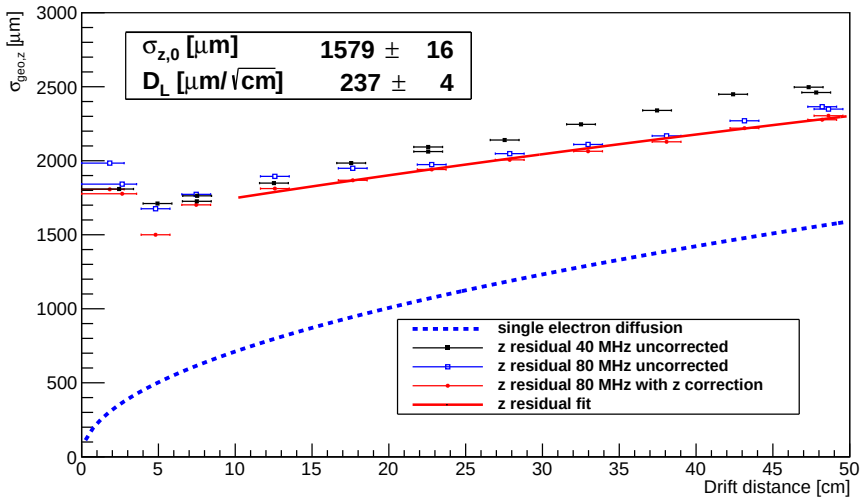


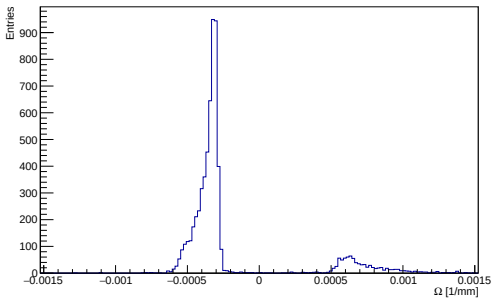

Figure 8.40: Longitudinal spatial resolution obtained by a z-scan with $B = 1\,\mathrm{T}$ and $E_{drift} = 230\,\mathrm{V/cm}$ and 80 MHz sampling frequency. The z-position for each run was deduced from the reconstructed tracks. For each run at a given z-position, the residuals were evaluated from the track with N-1 hits only. The effect of time walk is minimised as in [144]. For the fit, the first four data points were not taken into account, as only an upper limit for the z-position can be deduced. The results with z-residual mean corrections (red points) have been fitted. The uncorrected values are also shown (blue points). For comparison, the results (black points) from the 40 MHz $B = 0\,\mathrm{T}$ z-scan are also plotted.

reason for the tail of higher curved tracks, which have less energy. When some of the events were investigated by eye, it was often found that a positively curved track comes with a second negatively curved track in an event. A further, more detailed analysis of the positively charged particles could be interesting. In principle, also other particles can be produced when a beam electron interacts with the material.

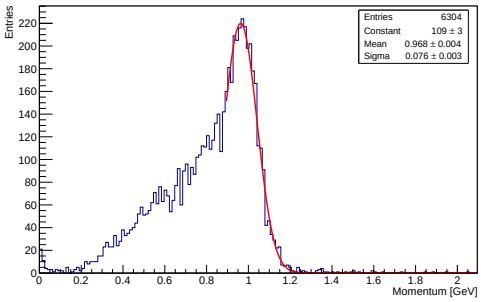
From the absolute curvature, the momentum of the particles is deduced and the distribution for the 1 GeV run is shown in Figure 8.41b. Again, a prominent peak can be seen at about the momentum expected. Also the tail from scattered particles at lower momenta reflects the expectation. In order to access the momentum resolution, the right edge of the peak was fitted by a Gaussian distribution. From the mean and sigma value, a momentum resolution of 8.07 % is obtained, which includes both the beam momentum spread and the intrinsic momentum resolution.

To compare the two contributions, the expected momentum resolution of the detector is calculated by the Gluckstern equation (2.24) and multiple scattering (Equation 2.28) from Section 2.4.2. As input, the following numbers are used:

- Single point resolution in run 140 at $z \approx 75\,\mathrm{mm}$: $\sigma_{xy} = 2.5 \times 10^{-4}\,\mathrm{m}$.
- Magnetic field: $B = 1\,\mathrm{T}$.
- Track length: $L = 0.5\,\mathrm{m}$.
- Number of hits: $N = 3000$.
- Radiation length in argon: $X_0 = 110\,\mathrm{m}$.




(a) Distribution of the parameter Ω describing the curvature of the track.




(b) Distribution of the measured momentum of the tracks. The right egde of the peak has been fitted by a Gaussian distribution to estimate the momentum resolution.

Figure 8.41: Results from a run where the beam has been set to provide 1 GeV particles.

This results in an intrinsic momentum resolution from the sagitta measurement (Gluckstern equation) $(\sigma_{p_t}/p_t)_{sag}$ of 0.16 % $\cdot p_t/GeV$ and an intrinsic momentum resolution from multiple scattering $(\sigma_{p_t}/p_t)_{MS}$ of 0.73 %. Multiple scattering dominates the resolution for momenta smaller than 5 GeV.
The beam momentum spread for 1 GeV was measured to be 6.36 % [173] [166], which is in the same order of magnitude to what has been measured and one order of magnitude larger than the calculated intrinsic momentum resolution. Because of the large beam momentum spread, the detector momentum resolution cannot be accessed with the test beam data.
A momentum distribution of run 187, where the beam particle energy was set to 5 GeV, is shown in Figure 8.42. The peak of the measured momentum at about 4.2 GeV does not resemble what is expected. A lower beam particle momentum can be excluded, as other groups obtained an approximately correct momentum measurement [166]. A 5 GeV particle on a circle radius of 16.7 m should be well found by the `CircleFinder` and especially be well fitted afterwards. The source for the too small reconstructed momentum has not been found in this preliminary analysis and needs further investigation. The remaining misalignment of the different modules can be a possible source for the effect. By the field distortion correction, the alignment is only corrected in direction perpendicular to the beam. A shift of the modules along the beam axis cannot be corrected that way and have an effect on the track curvature. However, the 15 % deviation form the expectation can not only be explained by an incorrect alignment on a scale of less than 1 mm. Possibly again, an incorrect track fitting could contribute to the measured effect.

**Pixel angular effect** For pads with a rectangular shape, the single point resolution depends on the track angle with respect to the direction of the long axis of the pad ($\phi$ angle). For pixels with a quadratic shape, this effect should not appear. This argument has been pointed out since the Pixel-TPC has been proposed but could not be proven so far, as no adequate data was available. In the test beam campaign, the TPC was rotated in the magnet. Hence, a $\phi$-scan was performed with runs at different rotation angles. This was done with magnetic field, which however would not have necessarily been the case for that kind of measurement. For all runs, the z-position was fixed, such that the beam was about 4 cm from the anode. The runs of that scan are 144 to 163. As the beam was at a different position in each run, no geometrical cuts were applied on the tracks used for the analysis. Only events with several tracks and tracks with less then 1200 hits were rejected. The same way as for the transverse resolution, the RMS value of the residual distribution can be taken to compare the resolution for different angles.

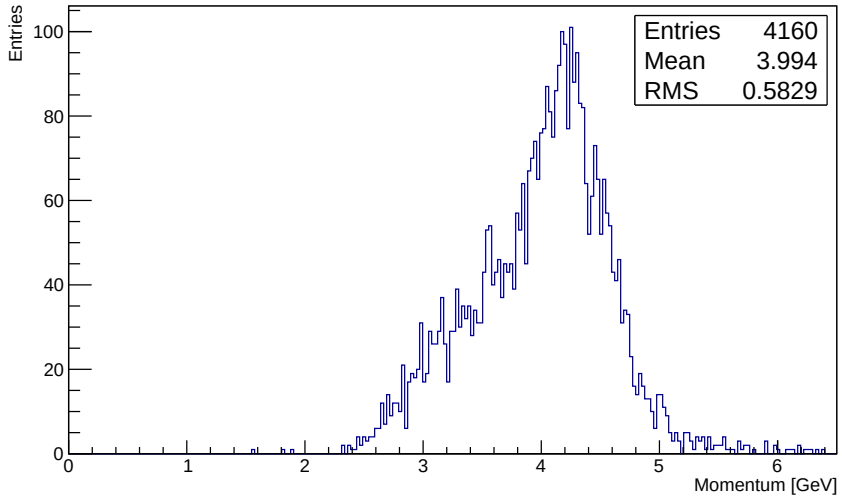



Figure 8.42: Distribution of the measured momentum of the tracks from a run where the beam has been set to provide 5 GeV particles.

For simplicity, the field distortion corrections were not applied (uncorrected residuals). The error of the residual distribution RMS value is dominated by the high statistics and does not account for the condition fluctuations between runs. Therefore, the uncorrected residual RMS value was evaluated for each track separately. For all tracks in a run, a distribution of values was obtained, from which the mean value is used to compare the resolution at different track angles, see Figure 8.43. The single electron diffusion for that z-distance is shown for comparison. As expected, the resolution does not depend on the $\phi$ angle as it can be described by a constant value within the error bars, which reflect the fluctuations.

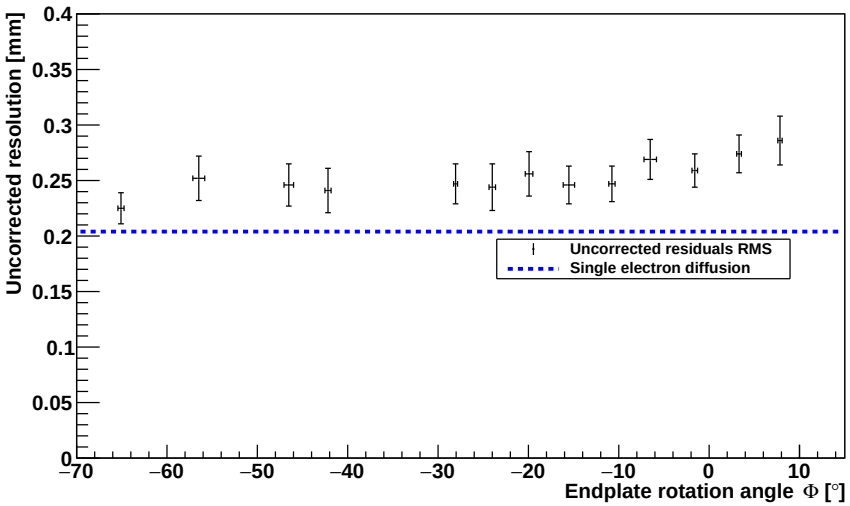
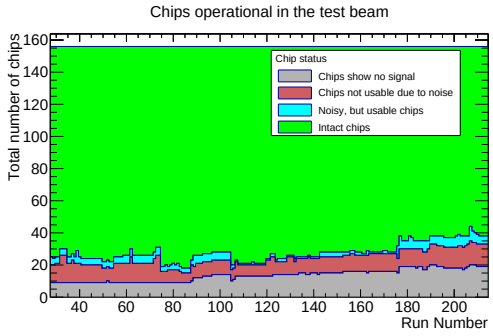


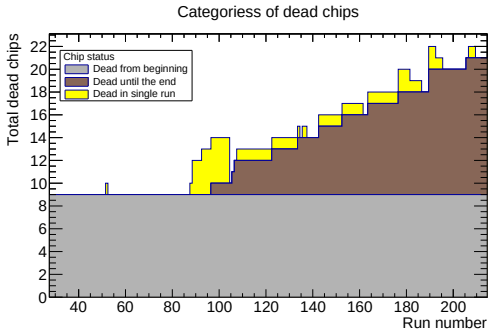

Figure 8.43: Single point resolution in dependence of the $\phi$ angle.

### 8.2.8 Dead chips

In Figure 8.2, the status of all chips before the test beam was shown. Some chips were noisy because the threshold could not be changed, others did not register events. During the test beam, the number of chips in that states increased. For each run, the number of chips in the different states is shown in Figure 8.44a. An additional state is also introduced: chips which are noisy, but can still be used to record data. It can be seen that the number of chips in the states fluctuates during the test beam. This is due to the fact that by tuning the threshold, some chips can change their status for example from noisy or not seeing a signal to intact.
Still in total, a decrease of intact chips towards the end of the test beam can be seen. This was further investigated and is shown in Figure 8.44b for the category of chips showing no signal. A similar plot has been produced for the chips that cannot be used due to noise (not shown, see [78]). The chips in each run, which could not be recovered by a threshold change are displayed. Those chips are labelled *Dead*. Sometimes, a chip that is thought to be dead in one run still showed a signal in later runs. Hence, a further differentiation in chips dead in all following runs (marked in brown) and dead only in single runs (yellow) was done.




(a) Chip status in dependence of the run number. The status of a single chip can change from run to run, from [78].




(b) Number of irrevocably dead chips in dependence of the run number, from [78].

Figure 8.44: Progression of the number of chips in different states during the test beam.

In total twelve chips died during the test beam. Additionally, the number of permanently not usable chips due to noise increased by six. The position of those chips is marked by an `x` in status map of all chips after the test beam in Figure 8.45. While on module 3 with the IZM-5 chips no chip changed its status, an accumulation of dead and noisy chips appeared on module 1. Especially the top two octoboards (6 and 24) are affected. On the central module, 4 chips changed the status of which 3 are on octoboard 12.
The large number of chips, which did not survive the test beam is concerning. However, the accumulation and the fact that no chip from the IZM-5 production died indicates to localised issues. Sparks, which are known to destroy gaseous detectors, are not favoured as reason for failure. First, they have not been observed during the test beam and second, in the last 15 runs with increased amplification voltage the number of dead or noisy chips has not risen significantly.
The reason for the malfunction of the octoboards on the top module and octoboard 12 on module 2 has not been found so far. The boards have not shown any conspicuous feature at the final testing during production (see Appendix C). The temperature of the power boards and the modules was monitored during the test beam. Also some specific LDOs temperatures were monitored. The temperature of module 1 shows no significant abnormalities. No correlation between excesses in the LDO temperature

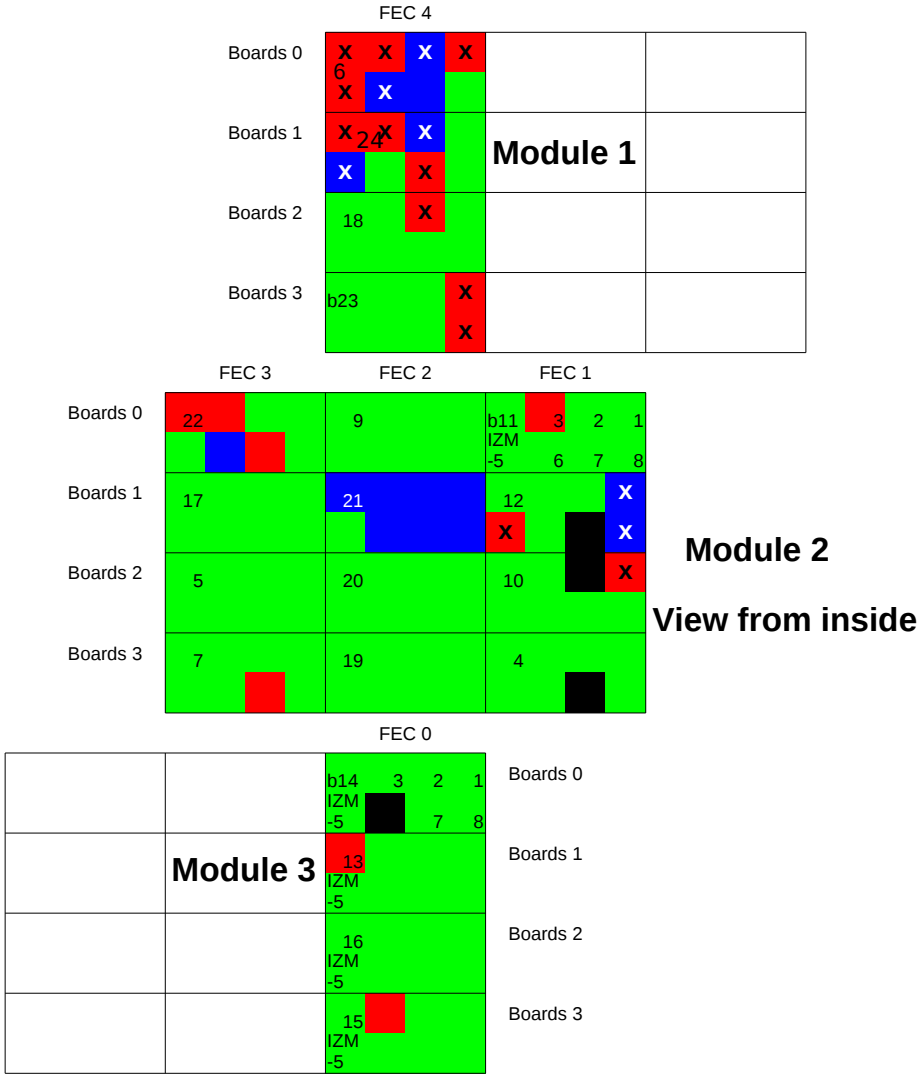



Figure 8.45: Arrangement of the octoboards on the modules, status after the test beam. The octoboards are labelled by their numbers as in Appendix C. On module 3, all boards are made of InGrids from the IZM-5 production. In total, two boards (b14, b11) are rotated, such that the chips are numbered opposite to the other boards. Chips marked in green were functional after the test beam, chips marked in black were not connected, chips in red did not show events and chips in blue were noisy. The chips labelled by an x were functional before the test beam. The boards and chips are shown as seen from inside of the TPC. The FEC numbers mark, which set of four octoboard was read out by which FEC.

and chips status change could be found. More details about the temperature measurements can be found in [78].
Finally, it has to be noted that the amplification structure of all InGrids stayed intact. The malfunction of the chips is only due to a failure of electronics in the Timepix chip.

## 8.3 Conclusions for further developments

The conclusions drawn from the 2013 test beam were an important input for later developments and the successful 2015 test beam. Still, the setup was not perfect and further improvements are necessary, especially in view of an even larger detector.
On the analysis side for the first time, tracks of a decent length from a Pixel-TPC were reconstructed and analysed. Therefore, the existing tools in MarlinTPC were used together with some processors specifically developed for this preliminary analysis. Those provide only limited capabilities so far. As the analysis was only preliminary, starting points for a more detailed and complete analysis are provided.

### 8.3.1 Module construction

The basic design idea for the InGrid modules of the 2013 test beam was used again for the final test beam. The octoboard as fundamental component has shown to be adequate. It was helpful, when one board on a side position had to be exchanged. The not functional board in the center could not be exchanged on short notice before the test beam, as no adequate spare was available and the access to the central position is difficult. The anode plate as guard at a higher position also seems to be a good option. The water cooling satisfied the needs. In a final design, another option should be chosen due to the danger of water leakage, bearing the risk to produce a short on the electronics or high voltage supply.
The powering scheme was a complete success. The chips could be operated much more reliably than during the 2013 test beam. Just the number of temperature sensors could be increased and integrated in the Intermediate board or a current monitoring should be introduced in order to detect short cuts, which could produce heat inside the TPC volume. Monitoring of the temperature at best on the Timepix surface or in the gas volume close to the active pixels could be used to correct for environmental influences on the gas properties.
The construction of the boards was already at the limit of what can be done by hand. The production of the 23 boards took about one month of clean room work. Due to the sensitive InGrid chips, concentration and careful handling was necessary at all times. An automation of some processes would be helpful, especially for the glueing of the chips to the octoboard PCB. As this was done by hand, the chips were rotated, shifted and also tilted in z-direction, which has a significant impact on the physics performance. Also the wire bonding could be automated if each chip is placed by a machine at an exactly defined position.
The short circuits inside many chips were the main issue during the production. Partially, they could be correlated to scratches on the surface, which were already present on the chips as the came form IZM. However, only the chips of the IZM-6 production were affected. Of those chips, several died during the test beam. Contrary, the IZM-5 chips did not show shorts during the production and also none was destroyed during the test beam. This hints to an issue during the IZM-6 production, which could be due to handling. Especially the observed scratches on the bonding pads support this argument.
A study to minimise field distortions was carried out after the 2013 test beam [146], and it was suggested to glue aluminium strips on the InGrids to cover the gaps between chips. There is a danger that conductive glue flows inside the grid holes or down the chip edges and produces a short circuit for the

high voltage. For that reason, the idea was abandoned for the 2015 test beam. In future studies, it will be interesting to see the improvements of this technique not only in laboratory test, but also in a test beam.
The high number of hits is an advantage of the Pixel-TPC. However with the current technology, wire bonds are facing the active area. To further increase the surface of a module covered by pixels, the Through-Silicon Via (TSV) technology should be applied.

### 8.3.2 Readout system

The readout system already performed well in the 2013 test beam. For the 2015 test beam it was further improved. This mainly refers to the bit shifts, which were removed almost completely. Further room for improvement has been detected, when the longitudinal resolution has been analysed. Despite the sampling frequency of the counters during the shutter opening time can be increased to 80 MHz, no significant increase in resolution was observed.
For a correct reconstruction of the z-position of a complete track, the sampling of the external trigger also needs to be fast to precisely control the opening and closing of the shutter. This only becomes relevant if the reconstructed track can be compared to the one measured by an external reference tracker.
The DAQ software could be further improved. For the large amount of chips, not every one can be controlled by the operator. Automated procedures are necessary in order to assure the correct operation of the chips during data taking. This includes the adjustment of the threshold in case a chip becomes noisy or does not register events to increase the number of operational chips per run.

### 8.3.3 Alignment and field distortions

The automated placement of chips has already been addressed before. With this method, the alignment of chips on a module could be improved. The alignment from module to module is a different issue. It has to be measured, when the modules are mounted to the endplate, possibly by a laser system. Another option, which can also be used in a complete analysis, is the calculation of the correct alignment form straight tracks by software. The Millipede [174] software package is suitable for that task.
The field distortions in the preliminary analysis have only been corrected along the axis perpendicular to the track. This is due to the implementation of the current correction algorithm. In a more sophisticated approach, a list not only of the mean residual values along the track would be needed, but a map for the total sensitive surface, which bijectively maps the measured position of a hit to the real position.

### 8.3.4 Track finding

As has been seen from the preliminary analysis, straight tracks are reconstructed reliably by the global approach of a Hough transformation. Because of the large number of hits, the computing time is larger than it would be for a pad-based detector. Instead of optimising that processor, a general track finder for pixelised data would be needed, which does not depend on the track model and uses a local approach. The way to go currently discussed is to reconstruct straight track segments on a single chip or octoboard by a Hough transformation. In principle, this can be done in parallel for all chips. Then in a second step, the tracklets found can be combined to a track candidate. This can be done by starting from the direction, where the tracks are best separated by the magnetic field and collecting the tracklets in a cone of expectation like in a Kalman fitter approach [175]. Another option would be to use the parameters of the reconstructed tracklets only. From those in a possibly purely analytical way, the ones belonging together can be calculated and finally form a track candidate. This method should be relatively fast concerning computing time.

On the track fitter side, less effort is needed as the same processors as for pad-based readout can be used. Because of the larger community, those processors are well developed. However, the helix fitter used herein needs to be investigated to assure that it correctly fits the tracks also in the xz and yz plane.

On a longer time scale, deltas should be identified and treated and the double track separation should be studied.

Also the improvement of the `CircleFinder` could be a very first approach.

### 8.3.5 Physics performance analysis

The $dE/dx$ resolution obtained from the measurement by a truncated mean method is 31 % larger than the expectation, what can possibly be improved. However, already the achieved value results in a satisfying energy loss resolution when extrapolated to the full ILD TPC. Therefore, the approximation in Equation 8.4 is used again. With the current module design, the effective track length would be about 1 m (1.5 m total track length) in the ILD. With the 1000 1 mm slices and the reduction factor of 31 %, an energy loss resolution of 5.7 % could be achieved, which almost meets the requirements for the detector. In case of a TPC endplate completely covered with pixels, the expected $dE/dx$ resolution from Equation 8.4 is 4.8 %. Hence, an improved module with increased active area would fulfil the specifications. The result should be confirmed also for other particle species to estimate the separation power.

It has been shown that the transverse spatial resolution given the field distortion effects are corrected is limited by diffusion only. Compared to results of a pad-based Micromegas in [176], the resolution is lower by a factor of about $\sqrt{22}$ over the complete z-range. However for the pad-based readout, the effective number of electrons contributing to a single measurement $N_{eff}$ is 21.6 ± 0.3, while for the pixelised readout, it is 1, which explains the difference.

As with the pixelised readout, the number of space points per track length is larger, an increase in momentum resolution is expected. The pad size of the Micromegas modules in [176] is $3 \times 7\,\mathrm{mm}^2$. Each module has 24 pad rows, hence the active length per module is 16.8 cm and the effective number of hits of a track parallel to the pad rows is $24 \cdot 22 = 616$.

For the current design of the pixelised module with eight chip rows, each chip with an active area of $14 \times 14\,\mathrm{mm}^2$, the active length is 11.2 cm. With the single electron detection efficiency, about 100 hits/cm are registered. The number of hits per track perpendicular to the chip rows is 1120, which is a factor of 1.8 larger than the effective number of hits on a pad-based module as expected. Using the Gluckstern equation (2.24) with the same transverse spatial resolution for both detectors, the momentum resolution of a pixelised module can be increased by a factor of $\sqrt{1.8} = 1.35$ or even 1.65 if the complete module would be covered with pixels.

The starting points for more detailed analyses have already been pointed out in the corresponding subsections. They mainly involve an improvement in track finding and fitting or on the detector side. The most important physics properties were at least briefly treated in the preliminary analysis. As a next step, also the double track resolution, at least for straight tracks could be analysed.

Therefore, the total number of hits per track can be used. As has been seen, there is a tail towards larger numbers, which stem from not correctly separated double tracks. However, track separation in the Hough space is not the optimal approach, especially for parallel and straight double tracks. Those cold be separated if one projects the hit positions on the axis perpendicular to the track (as done in the `CircleFinder` for curved tracks).

### 8.3.6 Timepix3

Intrinsically, the Timepix chip has some drawbacks for the application as readout of a TPC. Despite the analysis of the longitudinal resolution needs further improvement, it can already be seen that even in the case of the highest possible clock speed the chip can provide (about 150 MHz), the resolution is still significantly affected by the time resolution.
Additionally, the time walk effect decreases the resolution as it also influences the left edge of the y-residuals. The time walk cannot be corrected as the arrival time and signal height cannot be measured at the same time.
The readout rate of the Timepix chip is low, as always the complete matrix (917504 bit) has to be read out even if only the information of a single pixel (14 bit) needs to be accessed. This does not allow to use the chip in experiments requiring a high readout rate. As in the readout presented in this thesis, zero suppression has to be implemented at best in the readout system to minimise the network load, what consumes already a significant amount of FPGA resources.
Since 2014, the successor chip called Timepix3 [73] is available. The pixel matrix stayed the same with a pitch of 55 µm and a matrix of 256 × 256 pixels. The chip is produced in 130 nm CMOS technology and has three modes of acquisition. It can measure TOA only, TOA and TOT at the same time or do event counting and integrated TOT at the same time. Besides a frame-based readout, a data driven method is implemented. The data is already zero suppressed in the chip. For the TOA measurement, an additional clock of 640 MHz is used to count the exact arrival time with respect to the next edge of the slower clock. That way, a time resolution of 1.562 ns can be achieved. This is an improvement of a factor 5 compared to the maximum possible with the Timepix chip.
An InGrid has been produced from a small scale prototype of Timepix3, the Gossipo2 chip [177] with a pixel matrix of 16 × 16 pixels. The high frequency clock could be operated at 560 MHz and simultaneous TOT and TOA measurement was not available in the prototype. Implemented in a detector with a short drift gap of 1.3 cm it was used in a test beam at DESY, reporting significant improvements in resolution compared to the Timepix chip [178]. A $CO_2$ DME 50/50 gas mixture with low diffusion (about 25 µm/ $\sqrt{\text{cm}}$) and a drift velocity of 5.1 mm µs$^{-1}$ was used. Besides other interesting results, a position resolution $\sigma_{xy,0}$ of 10 µm and $\sigma_{z,0}$ of 27 µm (still influenced by timewalk) was measured.
Currently, the InGrid production for the Timepix3 is set up and laboratory test with the chip will soon be started, before this chip will also be applied in a Pixel-TPC.

CHAPTER 9

# Conclusion and outlook

As a feasibility study, the prototype TPC of the LCTPC collaboration has been equipped with a large area pixelised readout with in total 10.5 million channels. It served as a demonstrator for a novel type of particle physics detector, the Pixel-TPC. Therefore, a new readout system has been designed, pixelised endplate modules have been constructed and the complete setup was successfully operated in a test beam campaign. In a preliminary analysis of parts of the collected data, properties of the detector have been evaluated.

The TPC concept offers the capability of continuous tracking with many space points. As a gaseous detector, the material budget is low and the gas can be exchanged, which makes the TPC a candidate for high energy particle physics experiments at accelerators. Especially in view of the planned International Large Detector at the ILC, these features can be helpful for the particle flow concept.

New technology is needed to achieve the requirements for precision measurements of particle physics processes in case of TPC readout. Micro-pattern gaseous detectors as GEM and Micromegas are suitable for this task. For example, their gas amplification structure intrinsically provides a high granularity to fulfil the requirements on spatial resolution. To reflect this high granularity also from the readout side, the Pixel-TPC concept has been proposed more than ten years ago. It combines the micro-pattern gaseous detector with pixelised readout. The Timepix ASIC with $256 \times 256$ pixels, each of a size of $55 \times 55\ \mu m^2$, is currently used as charge collecting anode of a Micromegas like amplification structure, the InGrid.

By design, this type of detector offers a time of arrival measurement in every pixel, single electron detection efficiency, uniform gas gain and a high granularity resulting in an excellent spatial resolution. Every single pixel hit can be identified with the signal of an electron. A three dimensional space point of the primary ionisation in the TPC volume can be reconstructed from the pixel position and arrival time measurement.

However, a single unit of such a device only has a size of $2\,cm^2$. In order to equip the endplate of a TPC, many InGrids have to be placed side by side. Before the start of the project presented herein, one single board with an array of eight InGrids (octoboard) existed and was tested as readout of a TPC. A mass production of InGrids on wafer scale was set up to provide a sufficient number of chips for further developments. In order to control and read out the Timepix chip by a computer software operated by the user, a readout system is necessary as interface. The available systems at that time were able to handle no more than eight chips.

As a first step towards a large area pixelised gaseous detector, a new readout system was developed in the scope of this thesis. As a starting point, evaluation boards of the vendor `Xilinx` were used. Finally, the Timepix chip was implemented in the general purpose Scalable Readout System (SRS) to support an arbitrary number of chips. The evaluation board-based systems are in use in university laboratories and at the CAST experiment as readout for single chips.
An intermediate stage readout system was used at a test beam with a new octoboard version detector in 2013. Apart from powering problems, bit shifts in not more than 4 % of the data and minor other issues, the test beam was successful. A large data set was collected holding information about the performance of the detector. A preliminary data analysis was performed by Robert Menzen. On the maximum track length of only 5.6 cm, typically about 500 hits have been recorded per track. The drift velocities and gas gain for different parameter sets were reconstructed correctly. Also, the spatial resolution was studied and showed to be dominated by field distortions. The detector was well understood and already pointed out some of the capabilities of a pixelised TPC readout.
The experiences from the test beam triggered further studies on field distortion suppression, track reconstruction, powering and cooling.
For the final test beam in 2015, three modules for the endplate of the prototype TPC were built. Two were equipped with four octoboards and were arranged at an outer position of the endplate. The central module held twelve octoboards. They were read out by five Front-End Concentrator cards of the SRS controlled by a DAQ software, which was developed together with the Timepix readout system. The modules were water-cooled and equipped with dedicated power boards. From the 160 InGrids, 20 could not be used at the beginning of the test beam mainly due to short circuits inside the Timepix chips possibly stemming from incorrect handling. During the test beam, another 18 chips became unusable. The source of failure has so far not been found, but seems to be related to localised effects as all chips which became unusable were located close to each other. Additionally from the two production runs of InGrids used for the construction, only one showed these issues.
The readout system performed reliably and no systematic bit shift errors were found in the data. As the Timepix chips were not of such a good quality as for the 2013 test beam, a sophisticated data cleaning has been performed to extract the physical data from noise and defect pixels. The MarlinTPC framework was used for the preliminary analysis.
For the first time, tracks of a decent length from pixelised readout were reconstructed. A typical track with a maximum length of 50 cm (including insensitive areas and possibly unusable chips) has about 3000 hits. Both, straight tracks from runs without magnetic field and curved tracks were reconstructed. For the latter, a new track finding algorithm was developed which performs better than the already implemented ones. From the reconstructed tracks, performance parameters have been extracted of which some were predicted for a Pixel-TPC but could not have been provided so far due to the limited detector size.
The energy loss, which can be determined directly by counting the number of hit pixels per track length due to the single electron detection efficiency, was measured with a precision of $(9.9 \pm 0.5)$ % with a truncated mean method in an example run. Despite the value differs by 31 % from the expectation, it would be almost sufficient to achieve the requirements for the detector when extrapolated to a ILD Pixel-TPC already with the current module design. A beam with different particle species would be helpful to measure the separation power.
A transverse spatial resolution almost identical to the theoretical optimum was found in case of no magnetic field. With magnetic field, however, field distortions are still dominant.
For the longitudinal case, the spatial resolution is similar to what has been measured with the 2013 data in case of no magnetic field. As for the measurement with magnetic field a higher sampling frequency was used, an improvement of resolution was expected, but could not be observed. An inspection of the

field distortions in longitudinal direction uncovered a possible malfunction in track fitting, which needs further investigation.
Delta electrons can be identified by eye on the tracks and an exclusion of those for track finding would improve the resolution. In a first very simplified method, the effect of delta electrons was tried to be reduced by limiting the assignment of hits to the track to a restricted vicinity. An optimal parameter was found for the size of the vicinity, however, the result is not significant.
Investigating the momentum, tracks of positively charged particles were found, which do not originate from the primary beam. Those could be interesting for a further analysis. The momentum of beam particles was correctly reconstructed for 1 GeV particles. The measured momentum resolution resembles the beam momentum spread, which is one order of magnitude higher than the detector resolution expected from calculations. 5 GeV particles have been reconstructed with a too low momentum. In the preliminary analysis, the alignment of different modules has not been investigated in detail, which could be a reason besides an incorrect track fit.
For a pad-based readout, the transverse spatial resolution depends on the track angle with respect to the pad axes. For a pixelised readout, the situation is different as each grid hole is monitored by a pixel which are arranged in rows and columns with equal distance. Only for tracks with an angle of 45° to the chip axes, a minor effect is expected. The measured transverse spatial resolution for different track angles can be described by a constant in a range from 8° to −65°, hence, no angular dependence is observed for the Pixel-TPC.

At the end of the last chapter, a critical evaluation of the final setup and conclusions for further developments were presented. In addition and also to again emphasise those, it should be mentioned that with the large dataset further, more detailed analyses should be performed. Therefore, the capabilities of the reconstruction and analysis for pixelised data in MarlinTPC has to be extended. This holds in particular for the treatment of curved tracks. The high number of space points per track is challenging and requires to also take care of the computing time. Also, the field distortion correction and alignment need to be treated with more care.
Advantages towards a pad-based TPC readout were shown, with the constant single point resolution for different track angles being the most significant one. If the field distortions effects are further reduced, the momentum resolution would be increased by a factor of 1.35 due to the high number of space points compared to a pad-based readout. In case the gaps between chips are avoided, a factor of 1.65 is possible. For a study on double track resolution, algorithms which take advantage of the high granularity have to be developed.
To increase the acceptance of the Pixel-TPC, it has to be clarified why the 18 chips became unusable during the test beam. For a final detector, reliability plays an important role and a chip loss rate of that order of magnitude is not acceptable.
On the setup side at the large TPC prototype, an external tracking device would be helpful for a more detailed and precise evaluation of the detector properties.

For the future, the Timepix3 chip offers new possibilities for pixelised TPC readout, of which the better time resolution, simultaneous charge and time measurement and data driven readout are the most prominent ones. Further improvements and interesting results are to be expected from a Pixel-TPC with Timepix3. Therefore, a new readout system is required.
However, first the technical problems in InGrid production have to be solved especially concerning the handling and reliability of the devices. Another concern that did not show up in the test beam are shorts between a grid and the chip. As those would disturb the drift field of the whole chamber, a solution in case of such a failure has to be found. Either the chip (surface) has to withstand the high voltage, or the

field distortions have to be kept out of the drift region possibly by a gating device.
The feasibility of constructing and operating a Pixel-TPC has been shown and the preliminary results of the analysis proof most of the predicted advantages and are promising. For a Pixel-TPC at an ILD however, further research and development is required. As an option, the endplate could be only partly equipped with a pixelised readout. For a uniform field, the same amplification structure should then be used in the other regions as well.

# APPENDIX A

# FPGA firmware entity displays and port description

Additionally to Section 5.4, the graphical representation of the entities, which can be understood as black box with in and outgoing signals are displayed in this appendix. The logic, which is implemented inside the entity is explained in the main part of the thesis. Additionally, tables with all the port signals are provided with a short explanation for each signal.

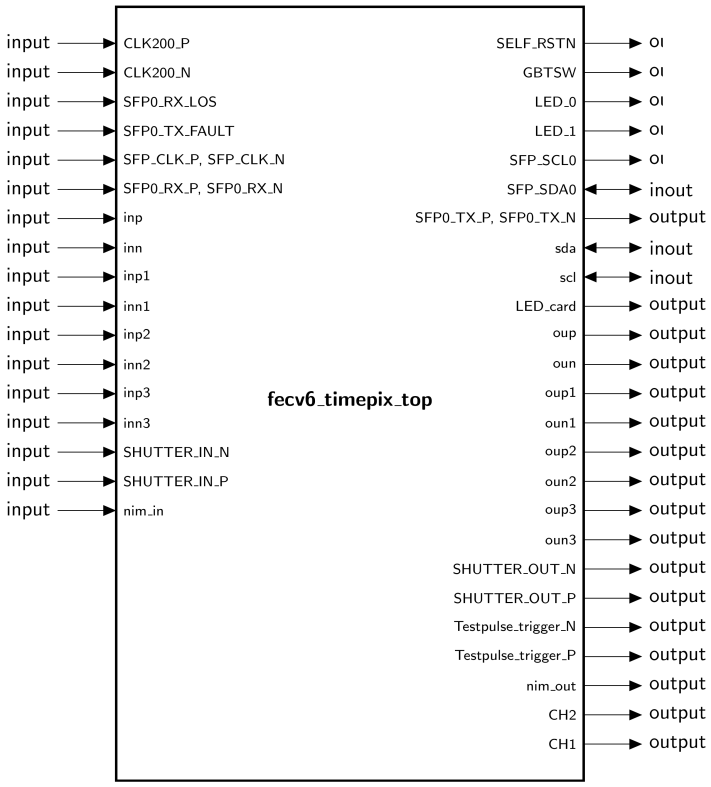



Figure A.1: Schematic view of the entity fec6_timepix_top, see Section 5.4.1.

| Signal name | Type | Route | Description |
|---|---|---|---|
| CLK200_P<br>CLK200_N | std_logic | Input | 200 MHz clock signal from the oscillator on the board. |
| SFP0_RX_LOS | std_logic | Input | LOS signal from SFP connecter on FEC6. |
| SFP0_TX_FAULT | std_logic | Input | FAULT signal from SFP connecter on FEC6. |
| SFP_CLK_P<br>SFP_CLK_N | std_logic | Input | Clock signal from SFP connecter on FEC6. |
| SFP0_RX_P<br>SFP0_RX_N | std_logic | Input | Data signal from SFP connecter on FEC6. |
| inp inn | std_logic_vector (2 downto 0) | Input | Vector of enable_out, clk_out and data_out from Timepix chip connected to HDMI port 1. |
| inp1 inn1 | std_logic_vector (2 downto 0) | Input | Vector of enable_out, clk_out and data_out from Timepix chip connected to HDMI port 2. |
| inp2 inn2 | std_logic_vector (2 downto 0) | Input | Vector of enable_out, clk_out and data_out from Timepix chip connected to HDMI port 3. |
| inp3 inn3 | std_logic_vector (2 downto 0) | Input | Vector of enable_out, clk_out and data_out from Timepix chip connected to HDMI port 4. |
| SHUTTER_IN_N<br>SHUTTER_IN_P | std_logic | Input | Signal connected to the Lemo plug on the intermediate board for the external shutter signal. |
| nim_in | std_logic | Input | Signal from nim_in Lemo connector on the FEC6 front panel. |
| SELF_RSTN | std_logic | Output | . Tied to ground. |
| GBTSW | std_logic | Output | Tied to ground. |
| LED_0 | std_logic | Output | Signal to LED_0 on FEC6 front panel. |
| LED_1 | std_logic | Output | Signal to LED_1 on FEC6 front panel. |
| SFP_SCL0 | std_logic | Output | I2C clock signal to SFP plug. Tied high. |
| SFP_SDA0 | std_logic | Output | I2C data signal to SFP plug. Tied high. |
| SFP0_TX_P<br>SFP0_TX_N | std_logic | Input | Data signal to SFP connecter on FEC6. |
| SDA | std_logic | Output | I2C data signal to adapter card. |
| SCL | std_logic | Output | I2C clock signal to adapter card. |
| LED_card | std_logic_vector (7 downto 0) | Output | Vector of signals to adapter card LEDs. |
| oup oun | std_logic_vector (2 downto 0) | Output | Vector of enable_in, clk_in and data_in from Timepix chip connected to HDMI port 1. |
| oup1 oun1 | std_logic_vector (2 downto 0) | Output | Vector of enable_in, clk_in and data_in from Timepix chip connected to HDMI port 2. |
| oup2 oun2 | std_logic_vector (2 downto 0) | Output | Vector of enable_in, clk_in and data_in from Timepix chip connected to HDMI port 3. |
| oup3 oun3 | std_logic_vector (2 downto 0) | Output | Vector of enable_in, clk_in and data_in from Timepix chip connected to HDMI port 4. |

Table A.1: fec6_timepix_top signals.

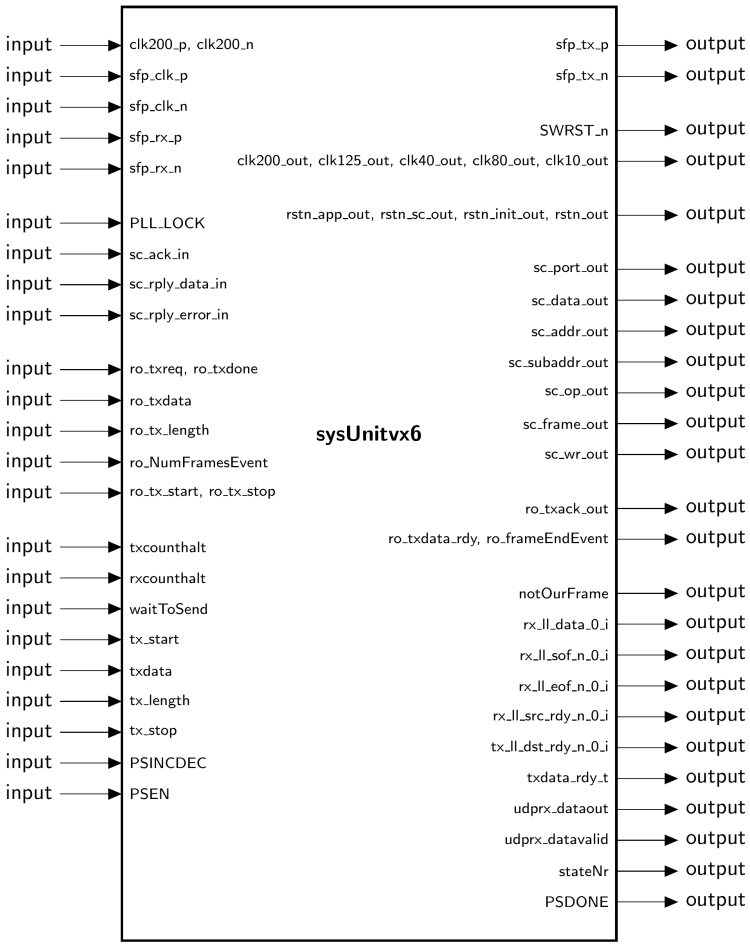



Figure A.2: Schematic view of the entity sysUnitvx6, see Section 5.4.2.

| Signal name | Type | Route | Description |
|---|---|---|---|
| clk200_p clk200_n | std_logic | Input | 200 MHz clock signal from top module. |
| sfp_clk_p sfp_clk_n | std_logic | Input | SFP clock signal from top module. |
| sfp_rx_p sfp_rx_n | std_logic | Input | SFP data signal from top module. |
| PLL_LOCK | std_logic | Input | External PLL lock signal from top module. |
| sc_ack_in | std_logic | Input | not used. |
| sc_rply_data_in | std_logic_vector (31 downto 0) | Input | not used. |
| sc_rply_error_in | std_logic_vector (31 downto 0) | Input | not used. |
| ro_txreq | std_logic | Input | not used. |
| ro_txdone | std_logic | Input | not used. |
| ro_txdata | std_logic_vector (7 downto 0) | Input | not used. |
| ro_tx_length | std_logic_vector (15 downto 0) | Input | not used. |
| ro_NumFrames-Event | std_logic_vector (6 downto 0) | Input | not used. |
| ro_tx_start | std_logic | Input | not used. |
| ro_tx_stop | std_logic | Input | not used. |
| txcounthalt | std_logic | Input | Halt signal for Ethernet package packing from timepix_controll module. |
| rxcounthalt | std_logic | Input | Halt signal for Ethernet package extracting from timepix_controll module. |
| waitToSend | std_logic | Input | Wait signal for Ethernet package sending from timepix_controll module. |
| tx_start | std_logic | Input | Start signal for data packing into Ethernet packages from timepix_controll module. |
| txdata | std_logic_vector (7 downto 0) | Input | Data from Timepix chip from timepix_controll module. |
| tx_length | std_logic_vector (15 downto 0) | Input | Desired length of data in Ethernet package. |
| tx_stop | std_logic | Input | Stop signal for data packing into Ethernet packages from timepix_controll module. |
| PSINCDEC | std_logic | Input | Phase shift increment/decrement signal from top module. |
| PSEN | std_logic | Input | Phase shift enable signal from top module. |
| sfp_tx_p sfp_tx_n | std_logic | Output | Ethernet MAC data output signals to top module. |
| SWRST_n | std_logic | Output | not used. |
| clk200_out | std_logic | Output | 200 MHz clock generated from oscillators to top module. |

| Signal name | Type | Route | Description |
|---|---|---|---|
| clk125_out | std_logic | Output | 125 MHz output clock from Ethernet MAC to top module. |
| clk40_out | std_logic | Output | 40 MHz clock generated from oscillators to top module for Timepix clock. |
| clk80_out | std_logic | Output | 80 MHz clock generated from oscillators to top module for Timepix clock. |
| clk10_out | std_logic | Output | 10 MHz clock generated from oscillators to top module for use in I2C modules. |
| rstn_app_out | std_logic | Output | not used. |
| rstn_sc_out | std_logic | Output | not used. |
| rstn_init_out | std_logic | Output | not used. |
| rstn_out | std_logic | Output | not used. |
| sc_port_out | std_logic_vector (15 downto 0) | Output | not used. |
| sc_data_out | std_logic_vector (31 downto 0) | Output | not used. |
| sc_addr_out | std_logic_vector (31 downto 0) | Output | not used. |
| sc_subaddr_out | std_logic_vector (31 downto 0) | Output | not used. |
| sc_op_out | std_logic | Output | not used. |
| sc_frame_out | std_logic | Output | not used. |
| sc_wr_out | std_logic | Output | not used. |
| ro_txack_out | std_logic | Output | not used. |
| ro_txdata_rdy | std_logic | Output | not used. |
| ro_frameEndEvent | std_logic | Output | not used. |
| notOurFrame | std_logic | Output | not used. |
| rx_ll_data_0_i | std_logic_vector (7 downto 0) | Output | Not our frame indicator from SRS Ethernet header analyser. |
| rx_ll_sof_n_0_i | std_logic | Output | Ethernet MAC receiver start of frame indicator. |
| rx_ll_eof_n_0_i | std_logic | Output | Ethernet MAC receiver end of frame indicator. |
| rx_ll_src_rdy_n-_0_i | std_logic | Output | Ethernet MAC receiver source ready indicator. |
| tx_ll_dst_rdy_n-_0_i | std_logic | Output | Ethernet MAC receiver destination ready indicator. |
| txdata_rdy_t | std_logic_vector (7 downto 0) | Output | not used. |
| udprx_dataout | std_logic_vector (7 downto 0) | Output | Data from SRS UDP packet analyser. |
| udprx_datavalid | std_logic | Output | Data valid indicator from SRS UDP packet analyser. |
| stateNr | std_logic | Output | State number (debug signal). |
| PSDONE | std_logic | Output | Phase shift done indicator for top module. |

Table A.2: sysUnitvx6 signals.

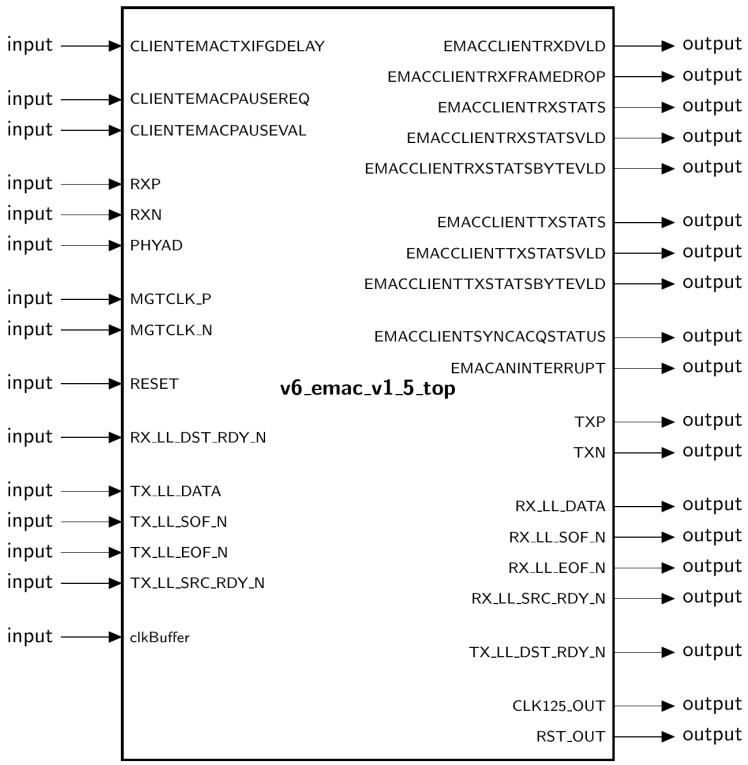



Figure A.3: Schematic view of the entity V6_emac_v1_5_top, see Section 5.4.3.

| Signal name | Type | Route | Description |
|---|---|---|---|
| clk | std_logic | Input | Timepix readout clock, typically 40 MHz. |
| rst | std_logic | Input | Reset signal from Ethernet MAC. |
| data_in | std_logic_vector (7 downto 0) | Input | Data from Ethernet MAC. |
| sof_in_n | std_logic | Input | Start of file signal from Ethernet MAC. |
| eof_in_n | std_logic | Input | End of file signal from Ethernet MAC. |
| src_rdy_in_n | std_logic | Input | Source ready signal from Ethernet MAC. |
| dst_rdy_in_n | std_logic | Input | Destination ready signal from Ethernet MAC. |
| fpga_mac | std_logic_vector (47 downto 0) | Input | FPGA MAC address from `scSystem`. |
| fpga_ip | std_logic_vector (31 downto 0) | Input | FPGA IP address from `scSystem`. |
| forceEthCanSend | std_logic | Input | Put to logic 1, enables sending. |
| txdata | std_logic_vector (7 downto 0) | Input | Data from `timepix_controll` module. |
| tx_length | std_logic_vector (15 downto 0) | Input | Length of Ethernet package to be sent from `timepix_controll` module. |
| tx_start | std_logic | Input | Starts sending from `timepix_controll` module. |
| tx_stop | std_logic | Input | Stops sending from `timepix_controll` module. |

| Signal name | Type | Route | Description |
|---|---|---|---|
| udptx_num-FramesEvent | std_logic_vector (6 downto 0) | Input | not used. |
| udptx_srcPort | std_logic_vector (15 downto 0) | Input | UDP source port from `scSystem`. |
| udptx_dstPort | std_logic_vector (15 downto 0) | Input | UDP destination port from `scSystem`. |
| udptx_sframeDly | std_logic_vector (15 downto 0) | Input | UDP frame delay from `scSystem`. |
| udptx_daqtotFrames | std_logic_vector (15 downto 0) | Input | DAQ total frames from `scSystem`. |
| udptx_dstIP | std_logic_vector (31 downto 0) | Input | Destination IP from `scSystem`. |
| udprx_portAckIn | std_logic | Input | Put to logic 1, enables receiver. |
| txcounthalt | std_logic | Input | Halt signal for packing Ethernet packages from `timepix_controll` module. |
| rxcounthalt | std_logic | Input | Halt signal for unpacking Ethernet packages from `timepix_controll` module. |
| waitToSend | std_logic | Input | Wait to send signal from `timepix_controll` module. |
| dst_rdy_out_n | std_logic | Output | Destination ready signal to Ethernet MAC. |
| data_out | std_logic_vector (7 downto 0) | Output | Data to Ethernet MAC. |
| sof_out_n | std_logic | Output | Start of file signal to Ethernet MAC. |
| eof_out_n | std_logic | Output | End of file signal to Ethernet MAC. |
| src_rdy_out_n | std_logic | Output | Source ready signal to Ethernet MAC. |
| tx_busy | std_logic | Output | not used. |
| txdata_rdy | std_logic | Output | not used. |
| frameEndEvent | std_logic | Output | not used. |
| udprx_srcIP | std_logic | Output | not used. |
| udprx_dstPortOut | std_logic | Output | not used. |
| udprx_checksum | std_logic | Output | not used. |
| udprx_dataout | std_logic_vector (7 downto 0) | Output | Data to `timepix_controll` module. |
| udprx_datavalid | std_logic | Output | Data valid signal to `timepix_controll` module. |
| notOurFrame | std_logic | Output | Not our frame signal to `timepix_controll` module. |
| statNr | std_logic | Output | Debug signal to top module. |

Table A.3: gbe_top signals.

| Signal name | Type | Route | Description |
|---|---|---|---|
| clk | std_logic | Input | Input clock of 10 MHz. |
| DAC_addr | std_logic_vector (8 downto 0 ) | Input | DAC address. |

| Signal name | Type | Route | Description |
|---|---|---|---|
| DAC_channel | std_logic_vector (1 downto 0) | Input | DAC channel to set. |
| DAC_level | std_logic_vector (11 downto 0) | Input | Binary DAC level value. |
| ADC_addr | std_logic_vector (6 downto 0) | Input | ADC address. |
| ADC_channel | std_logic_vector (2 downto 0) | Input | ADC to read out. |
| I2CExpander_addr | std_logic_vector (6 downto 0) | Input | I2C expander address. |
| I2Cexpander_data | std_logic_vector (7 downto 0) | Input | Binary I2C value. |
| I2C_operation_i | integer | Input | FPGA I2C state select from `timepix_controll` module. |
| LED6 | std_logic | Output | Signal to on board LED to indicate that I2C clock runs. |
| sda | std_logic | InOut | I2C `sda` signal. |
| scl | std_logic | InOut | I2C `scl` signal. |
| ADC_result | std_logic_vector (9 downto 0) | InOut | ADC readout result. |
| ADC_ChId | std_logic_vector (2 downto 0) | InOut | ADC channel number from readout. |
| ADC_alert | std_logic | InOut | Alert signal from ADC. |
| reset_i2c_done | std_logic | Output | I2C reset done. |
| op_finished | std_logic | InOut | Operation finished indicator for `timepix_controll` module. |

Table A.4: i2c_control signals.

| Signal name | Type | Route | Description |
|---|---|---|---|
| clk | std_logic | Input | Input clock of 10 MHz. |
| reset_n | std_logic | Input | Reset signal from `i2c_control`. |
| ena | std_logic | Input | Enable signal from `i2c_control`. |
| addr | std_logic_vector (6 downto 0) | Input | Address signal from `i2c_control`. |
| rw | std_logic | Input | ReadWrite signal from `i2c_control`. |
| data_wr | std_logic_vector (7 downto 0) | Input | Write data from `i2c_control`. |
| busy | std_logic | Output | Busy signal to `i2c_control`. |
| data_rd | std_logic_vector (7 downto 0) | Output | Read data to `i2c_control`. |
| sda | std_logic | InOut | I2C `sda` signal. |
| scl | std_logic | InOut | I2C `scl` signal. |

Table A.5: i2c_master signals.

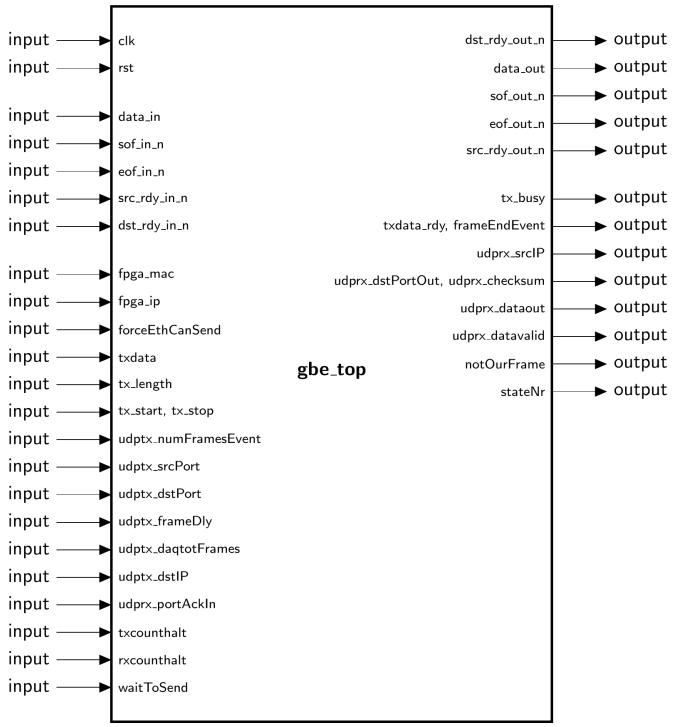



Figure A.4: Schematic view of the entity gbe_top, see Section 5.4.4.

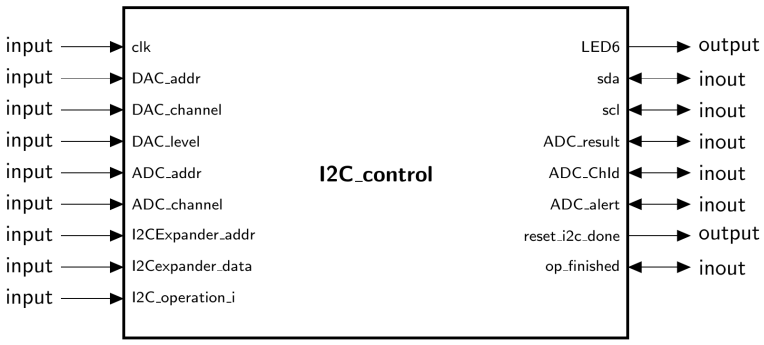



Figure A.5: Schematic view of the entity i2c_control, see Section 5.4.5.

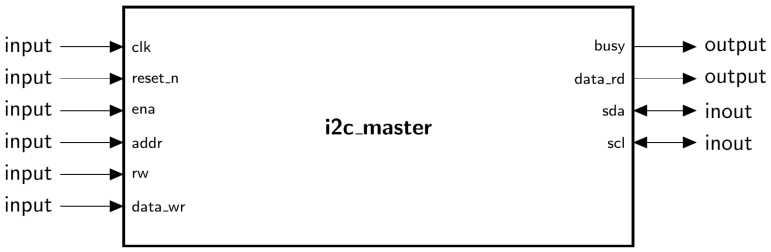



Figure A.6: Schematic view of the entity i2c_master, see Section 5.4.6.

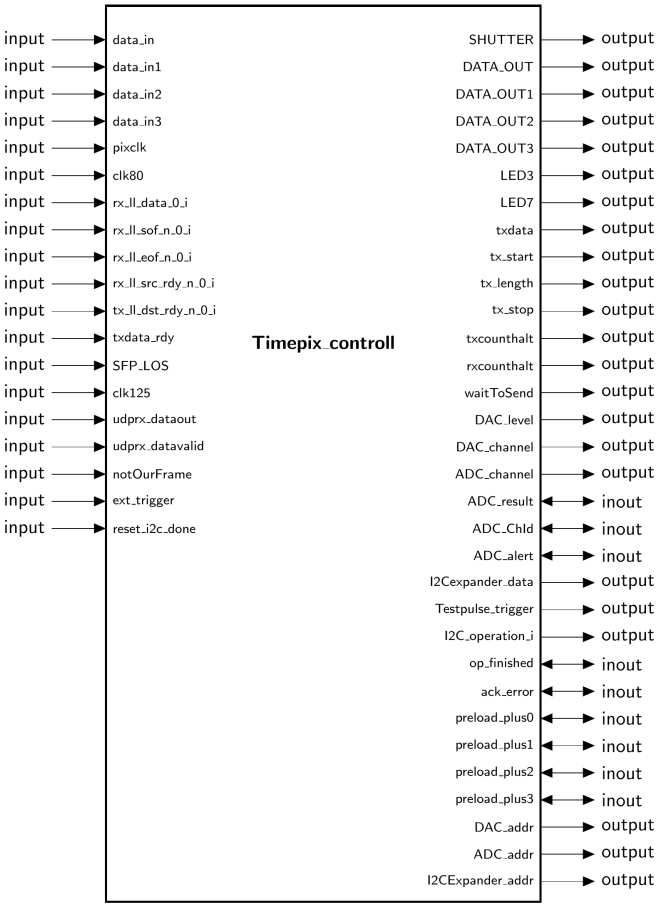



Figure A.7: Schematic view of the entity timepix_control, see Section 5.4.7.

| Signal name | Type | Route | Description |
|---|---|---|---|
| data_in | std_logic_vector (2 downto 0) | Input | Data, clock and enable signal from board 0. |
| data_in1 | std_logic_vector (2 downto 0) | Input | Data, clock and enable signal from board 1. |
| data_in2 | std_logic_vector (2 downto 0) | Input | Data, clock and enable signal from board 2. |
| data_in3 | std_logic_vector (2 downto 0) | Input | Data, clock and enable signal from board 3. |
| pixclk | std_logic | Input | Main Timepix readout clock. |
| clk80 | std_logic | Input | 80 MHz clock. |
| rx_ll_data_0_i | std_logic_vector (8 downto 0) | Input | Data from Ethernet MAC. |
| rx_ll_sof_n_0_i | std_logic | Input | Start of file signal from Ethernet MAC. |
| rx_ll_eof_n_0_i | std_logic | Input | End of file signal from Ethernet MAC. |
| rx_ll_src_rdy_n_0_i | std_logic | Input | Source ready signal from Ethernet MAC. |
| rx_ll_dst_rdy_n_0_i | std_logic | Input | Destination ready from Ethernet MAC. |

| Signal name | Type | Route | Description |
|---|---|---|---|
| txdata_rdy | std_logic | Input | Data ready signal from `gbe_top` module, not used. |
| SFP_LOS | std_logic | Input | not used. |
| clk125 | std_logic | Input | 80 MHz output clock from Ethernet MAC . |
| udprx_dataout | std_logic_vector (7 downto 0) | Input | Data from `gbe_top` module. |
| udprx_dataout | std_logic | Input | Data valid signal from `gbe_top` module. |
| notOurFrame | std_logic | Input | Not our frame indicator from `gbe_top` module. |
| ext_trigger | std_logic | Input | External trigger signal. |
| reset_i2c_done | std_logic | Input | Reset done signale from I2C interface. |
| SHUTTER | std_logic | Output | Shutter signal for Timepix chip. |
| DATA_OUT | std_logic_vector (2 downto 0) | Output | Data, clock and enable signal to board 0. |
| DATA_OUT1 | std_logic_vector (2 downto 0) | Output | Data, clock and enable signal to board 1. |
| DATA_OUT2 | std_logic_vector (2 downto 0) | Output | Data, clock and enable signal to board 2. |
| DATA_OUT3 | std_logic_vector (2 downto 0) | Output | Data, clock and enable signal to board 3. |
| LED3 | std_logic | Output | Signal to LED 3 on adapter board. |
| LED7 | std_logic | Output | Signal to LED 7 on adapter board. |
| txdata | std_logic_vector (7 downto 0) | Output | Data to `gbe_top` module. |
| tx_start | std_logic | Output | Start signal for packing of packages for `gbe_top` module. |
| tx_length | std_logic_vector (15 downto 0) | Output | Packet length signal to `gbe_top` module. |
| tx_stop | std_logic | Output | Stop signal for packing of packages for `gbe_top` module. |
| txcounthalt | std_logic | Output | Halt signal for packing of packages in `gbe_top` module. |
| rxcounthalt | std_logic | Output | Halt signal for unpacking of packages in `gbe_top` module. |
| waitToSend | std_logic | Output | Wait to send signal for `gbe_top` module. |
| DAC_level | std_logic_vector (11 downto 0) | Output | Binary level value for I2C DAC. |
| DAC_channel | std_logic_vector (1 downto 0) | Output | Channel of DAC to be set. |
| ADC_channel | std_logic_vector (2 downto 0) | Output | Channel of ADC to be read out. |
| ADC_result | std_logic_vector (9 downto 0) | InOut | Binary result of ADC readout to and from `i2c_control` module. |
| ADC_ChId | std_logic_vector (2 downto 0) | InOut | Chip ID of ADC readout to and from `i2c_control` module. |

| Signal name | Type | Route | Description |
|---|---|---|---|
| ADC_alert | std_logic | InOut | Alert signal of ADC readout to and from `i2c_control` module. |
| I2Cexpander_data | std_logic_vector (9 downto 0) | Output | Data to I2C expander. |
| Testpulse_trigger | std_logic | Output | Switch signal for multiplexer to generate test pulses. |
| I2C_operation_i | integer | Output | I2C state select to `i2c_control` module. |
| op_finished | std_logic | InOut | Operation finished signal to and from `i2c_control` module. |
| ack_error | std_logic | InOut | Acknowledge error to and from `i2c_control` module. |
| preload_plus0 | integer | InOut | Preload signal to shift data from board 0 in top module. |
| preload_plus1 | integer | InOut | Preload signal to shift data from board 1 in top module. |
| preload_plus2 | integer | InOut | Preload signal to shift data from board 2 in top module. |
| preload_plus3 | integer | InOut | Preload signal to shift data from board 3 in top module. |
| DAC_addr | std_logic_vector (8 downto 0) | Output | DAC address to `i2c_control` module. |
| ADC_addr | std_logic_vector (6 downto 0) | Output | ADC address to `i2c_control` module. |
| I2CExpander_addr | std_logic_vector (6 downto 0) | Output | I2C expander address to `i2c_control` module. |

Table A.6: timepix_control signals.

| Signal name | Type | Route | Description |
|---|---|---|---|
| outclk | std_logic | Input | Returning clock from Timepix chip. |
| pixclk | std_logic | Input | Main Timepix readout clock. |
| timepix_data_in_-storage | std_logic | Input | Data from Timepix chip. |
| deserial_enable_-storage | std_logic | Input | Enable signal for packing of bytes from `timepix_controll`. |
| readout_matrix_-start | std_logic | Input | Start signal to read out Timepix chip from operation `"1a"` in `timepix_controll`. |
| send_while_-reading_start | std_logic | Input | Start signal for fast zero suppressed mode from operation `"1c"` in `timepix_controll`. |
| send_while_-reading | std_logic | Input | Enable signal for packing of bytes in zero suppressed mode from `timepix_controll`. |
| reset_cases | std_logic | Input | Reset signal to go to `case_Dout = 0` from operation `"01"` in `timepix_controll`. |
| desired_lenght | integer | Input | Length of Ethernet package to be sent. |
| numchips | integer | Input | Number of chips on board. |

| Signal name | Type | Route | Description |
|---|---|---|---|
| chip | integer | Input | Chip to be processed. |
| preload_plus | integer | Input | Preload to shift correct for signal path. |
| disable_chip | std_logic_vector (7 downto 0) | Input | Disable chips such that no hits are saved. |
| board | integer | Input | Board to be processed. |
| is_board | integer | Input | Board the `storage` module was assigned to. |
| tx_ll_data_0_i_-storage | std_logic_vector (7 downto 0) | Output | Data bytes to `timepix_controll`. |
| deserial_hold_-storage | std_logic | Output | Halt signal for transmission to `timepix_controll`. |
| readout_matrix_-stop | std_logic | Output | Indicator that the readout of the Timepix chip is finished. |
| hit_counter_result | array | Output | Final number of hits on the chips after readout complete. |
| outclock_counter_-result | std_logic_vector (23 downto 0) | Output | Number of returning clock cycles received after readout complete. |
| LED7 | std_logic | Output | External clock LED blink signal to LED 7 on board. |
| case_dout_out | std_logic_vector (7 downto 0) | Output | `case_Dout` signal to `timepix_controll` for debug. |
| sendbitMatrix_-case_out | std_logic_vector (7 downto 0) | Output | `sendbitMatrix_case` signal to `timepix_controll` for debug. |
| useMemoryTo-Write_out | std_logic_vector (7 downto 0) | Output | Indicates, which memory block has been used to store the hits. |

Table A.7: storage signals.

| Signal name | Type | Route | Description |
|---|---|---|---|
| clk200 | std_logic | Input | 200 MHz system clock. |
| din | std_logic_vector (31 downto 0) | Input | Data from `storage` module. |
| wr_en | std_logic | Input | Write enable signal. |
| clk40 | std_logic | Input | Main Timepix readout clock. |
| readDDR2start-Address | std_logic_vector (30 downto 0) | Input | Start address to read out data from the DDR2 SDRAM. |
| readDDR2-NumberOfHits | integer | Input | Number of hits to be read out from the DDR2 SDRAM. |
| readDDR2 | std_logic | Input | DDR2 SDRAM is read out when this signal is 1. |
| addr_reset | std_logic | Input | Resets DDR2 SDRAM address to 0. |
| rd_en_fromDDR2 | std_logic | Input | Enable reading from DDR2 SDRAM. |
| ddr2_... | different | Output InOut | Signals to control DDR2 SDRAM hardware, see [154] |
| full | std_logic | Output | `FIFO_data_to_DDR2` signal, not used so far. |
| empty_FIFOfrom-DDR2_i | std_logic | Output | `FIFO_data_from_DDR2` empty signal to indicate that all data has been read out. |

| Signal name | Type | Route | Description |
|---|---|---|---|
| dout40 | std_logic_vector (31 downto 0) | Output | Data from DDR2 SDRAM. |
| ddr2_reset_done | std_logic | Output | DDR2 SDRAM reset done signal. |
| ddr_reading | std_logic | Output | Indicates that readout is ongoing. |
| wr_en_from-DDR2_out | std_logic | Output | Indicates that data is coming from DDR2 SDRAM. |

Table A.8: ddr2_mem_control signals.

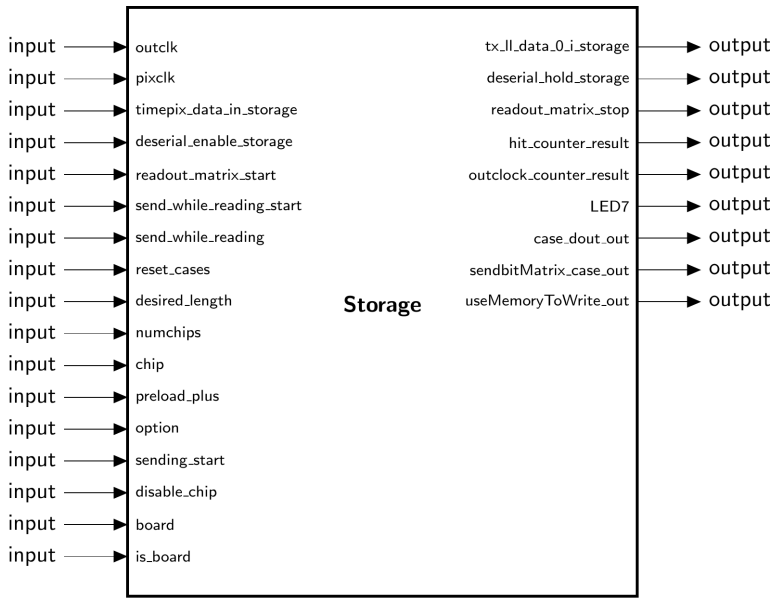



Figure A.8: Schematic view of the entity storage, see Section 5.4.8

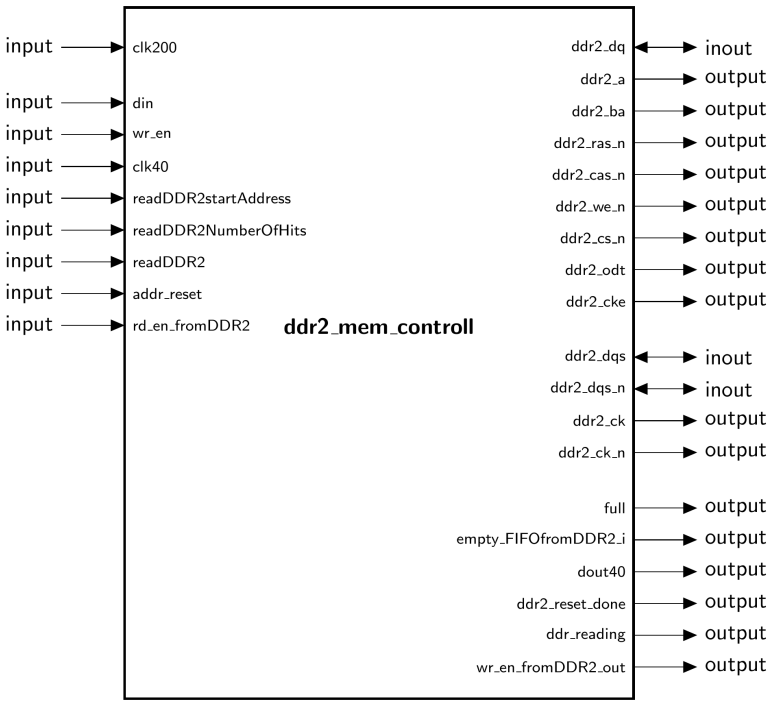
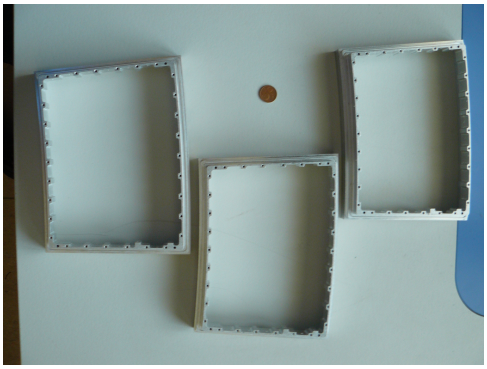



Figure A.9: Schematic view of the entity ddr2_mem_controll, see Section 5.4.9.

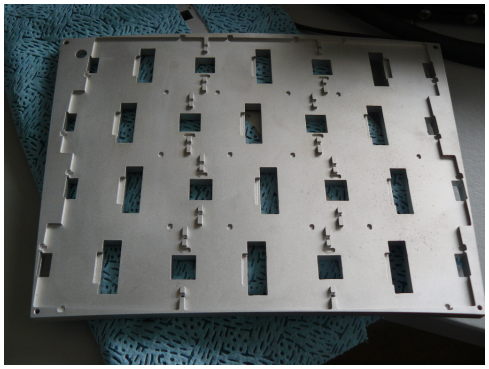
APPENDIX B

# Impressions from the 2015 test beam module construction and implementation

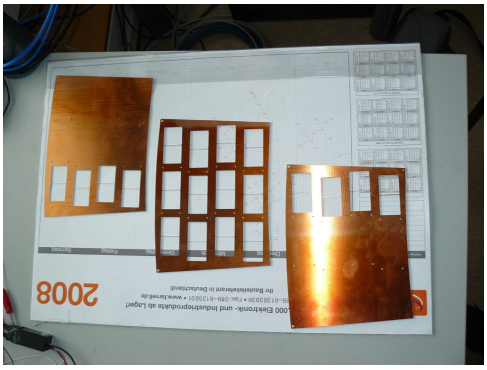
In this appendix, images from the construction of the three modules for the 2015 test beam at DESY are shown. Figure B.1 shows the different mechanical components, of which the module consists. Those are the frame which can be mounted to the endplate of the LP in Figure B.1a, the brackets with which the frames are fixed to the endplate to achieve gas tightness in Figure B.1e, the anode plates which assure a uniform drift field in the TPC volume and only have openings for the InGrids in Figure B.1d/B.1c and the power board which provides a stable 2.2 V supply voltage for the Timepix chips on the octoboards in Figure B.1f.
The next set of images shows the assembly of the octoboards in the clean room. In Figure B.2a, an octoboard under the wire bonding machine is shown while one of the chips is being bonded. A completely bonded board, together with the individual InGrids as they arrived in Bonn from IZM in a gel pack is shown in Figure B.2b. An example of a gap between two chips on an octoboard is shown in Figure B.2c. One can see the wire bonds between the chips which transfer the data though the chain and two bonds on each chip. In Figure B.2d, the 20 octoboards for the assembly of the modules are shown.
The set of Figures B.3 shows the part of the assembly of the modules in the clean room, in which the octobards are placed on the support structure. The procedure is shown for one of the two partly equipped modules in Figure B.3a and B.3b and for the completely equipped module in Figure B.3c to B.3f.



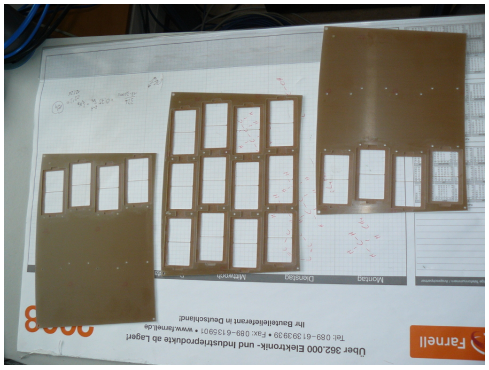
(a) Module fames for the LP.



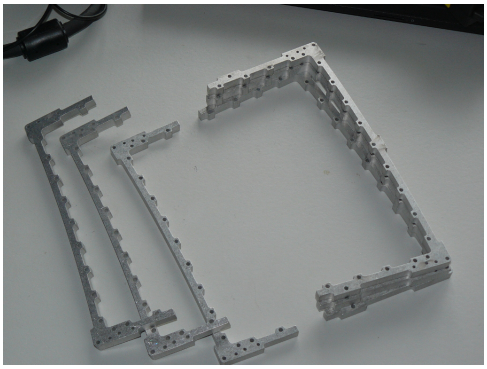
(b) Aluminium support structure for the octoboards including the cooling.



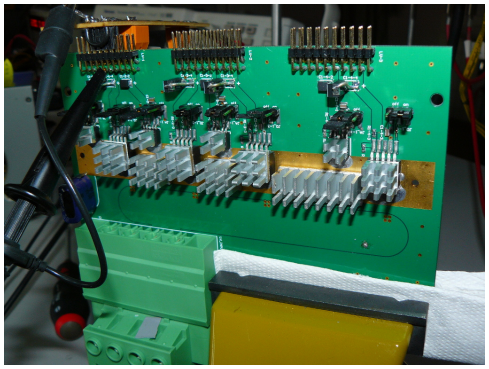
(c) Anode plates with opening for the octoboards, top side.



(d) Anode plates with opening for the octoboards, bottom side.

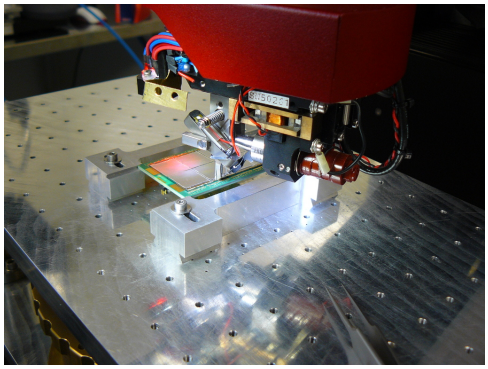


(e) Mounting brackets needed for the installation at the LP.

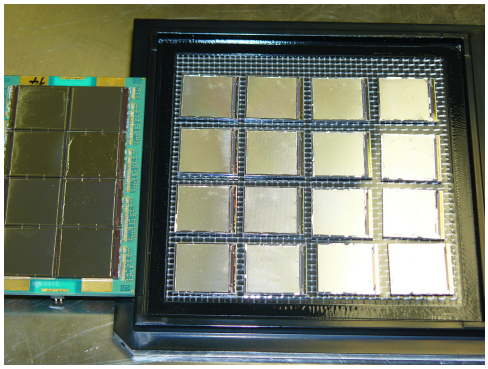


(f) Board for the power supply of four octoboards.

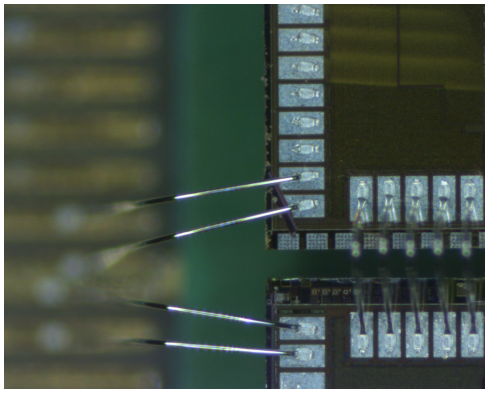
Figure B.1: Components for the module constructions.



(a) Wire bonding of a chip on an octoboad.



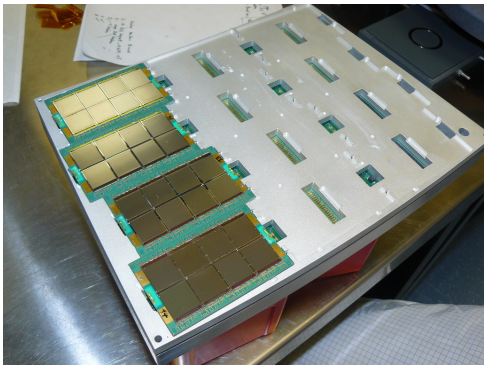
(b) Complete octoboard and single InGrids in a gel pack.



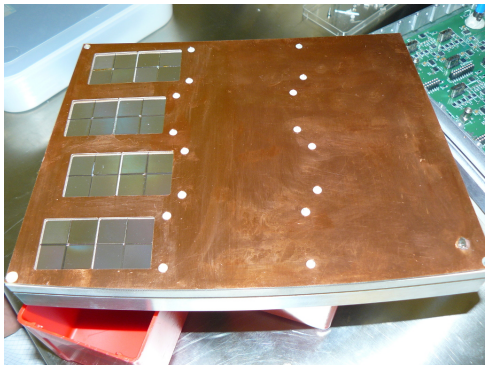
(c) Gap between two chips on an octoboard with connecting bonds.

(d) 20 octoboards in storage boxes waiting for the assembly.

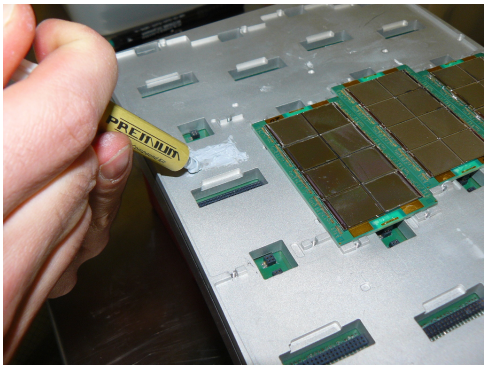
Figure B.2: Assembly of the octoboards in the clean room.



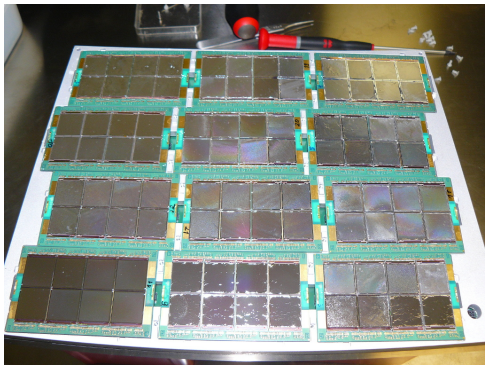
(a) Assembly of the first partly equipped module.



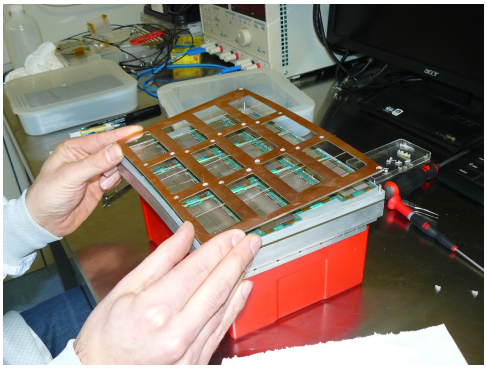
(b) Completely assebles first module.



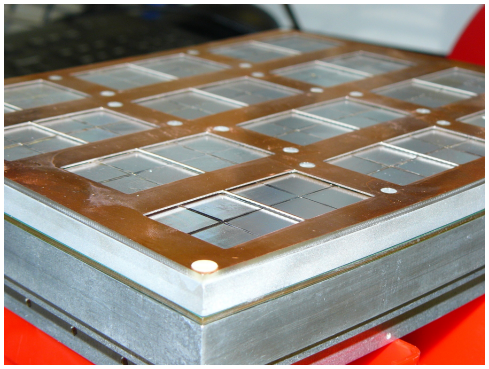
(c) Assembly of the complete equipped module. Deposition of heat conducting paste between the octoboards and the support structure.



(d) Completely equipped module with 96 InGrids arranged on 12 octoboards.



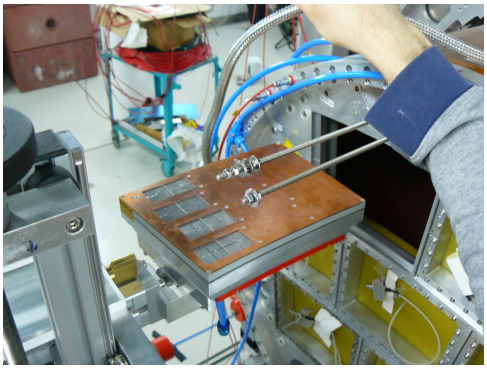
(e) Mounting of the anode plate on the completely equipped module.



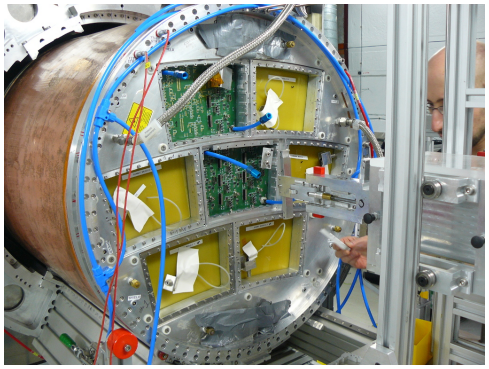
(f) Assebled module from the side showing the different layers frame, Intermediate board, support and anode.

Figure B.3: Module assembly.

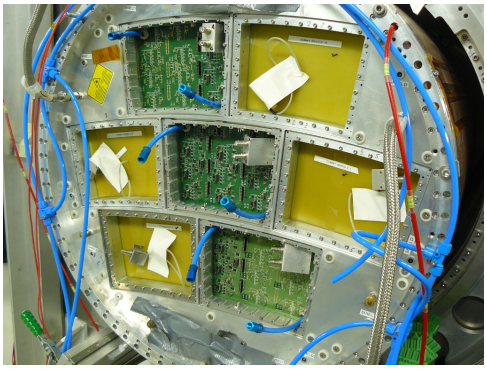
In Figure B.4, the installation of the modules at the LP at DESY is shown. The endplate was equipped with dummy modules, of which three were replaced with the InGrid modules, where the completely equipped module was placed in the center. Figure B.4a show the installation of the first module, which is a partly equipped one. A special mounting tool was used for the installation procedure. Figure B.4b shown the endplate, as the mounting of the central module was just finished and Figure B.4c the completely assembled endplate. The blue lines at the border of the endplate are the water cooling pipes, which were connected to the modules. In Figure B.4d, the modules are fully connected. The water pipes in blue, power lines in the blue/black bundles and data line in the white/black bundles can be seen. The cables for the temperature sensors are still missing in this image. Figure B.4e shows the five ATX power supplies, of which each supplies one power supply board shown in Figure B.1f. Finally, Figure B.4f shows the readout. It consists of two crates, of which one is only used to provide the power for half of the six SRS FECs. Five FECs6 were used to read out the 160 chips. They are interconnected by short network cable (white) for clock synchronisation.



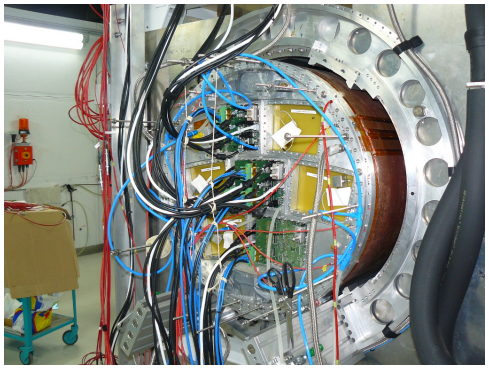
(a) Installation of the first, partly equipped module.



(b) LP endplate with two modules installed.

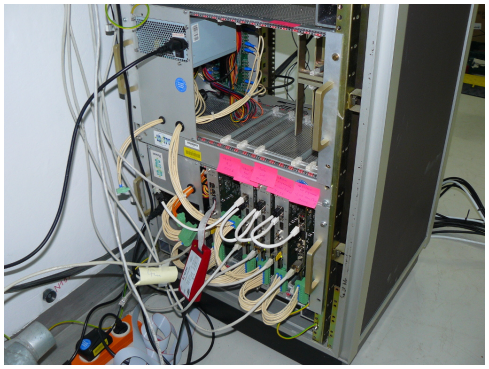


(c) LP endplate with all three modules installed.



(d) Setup with all cables mounted.

(e) Power supply units (standard ATX PC power supplies).



(f) SRS with five FEC6 for the readout of 160 chips.

Figure B.4: Assembly of the modules to the LP endplate at the test beam.

APPENDIX C

# InGrid Octoboards

For the two test beams presented in the thesis, in total 24 InGrid octoboards were produced. An InGrid octoboard is a chain of eight Timepix chips which have been post-processed to hold an InGrid, see Section 3.2. The chips are arranged in a matrix of $2 \times 4$ chips. In Table C.1, the quality of the individual boards and some properties are presented as measured after the production. The Timepix chips themselves were probed before the post processing and labelled by the letter `A` to F depending on the number of dead columns:

- A: no dead column
- B: one dead column
- C: two dead columns
- D: more than two dead columns
- E: bad DACs
- F: bad digital test

Chips of type `E` and `F` have not been delivered from IZM. Another value in the quality control during the production was the current a complete octoboard draws on the two supply voltages `VDD` and `VDDA` of 2.2 V. The expected values are about 0.2 A and 1.5 A, respectively. This is in particular interesting, as for the IZM-6 production, shorts circuits inside the Timepix chip or through scratches on the surface were the main reasons for a failure. Some boards showed a low resistance between one of the supply voltages and ground, which has been marked in the electronic test. The chips have been used, despite they draw a higher current. After the electronic test, the InGrid was put on high voltage in a gas mixture of argon/isobutane 95/5 and the current through the ideally isolating gap was measured. Finally, the status of the octoboard after the test beam is also indicated in the table.
The boards consist of InGrids from different production runs. Board V4/1 is made from IZM-3 InGrids of Timepix wafer 56. Because of the high number of InGrids needed for the 2015 test beam, IZM-5 and IZM-6 InGrids have been used. The boards V5/11, V5/13, V5/14, V5/15 and V5/16 are from the IZM-5 production on wafer 62. All other boards, except for V5/1 are made of InGrids from the IZM-6 production on wafer 68,69 and 74.

| No. | Chip types | Electronic test | LV Current [A] | HV current [nA] | Comment | Status after test beam |
|---|---|---|---|---|---|---|
| V4/1 | 8×A | ok | 0.54/1.50 | 0.78/1.80 @ 340 V | Used in 2013 test beam. Chip 8 had to be put to a high threshold because of powering problems. | All chips working. |
| V5/1 | | | | | Prototype board with bare Timepix chips used for bonding tests | Not working. |
| V5/2 | 4×D 4×A | all ok but chip 3 | 0.40/1.92 | 3.91/7.70 @ 340 V | Chip 3 sees no events. Used as spare at 2015 test beam. | Unknown. |
| V5/3 | 1×C 6×D 2×A | short on chip 7 ⇒ disconnected, chip 8 only 50 Ω to GND | 0.76/1.35 | 4.16/2.74 @ 340 V | Had to be exchanged before 2015 test beam. Heat conductive paste between chips produced short. | HV short after assembly. |
| V5/4 | 8×B | short on chip 3 ⇒ disconnected | 0.22/1.32 | 20.5/15.7 @ 340 V | Used in 2015 test beam. | 1 chip disconnected, 7 chips working. |
| V5/5 | 4×B 3×A 1×C | all ok | 0.10/1.62 | 3.06/1.32 @ 340 V | Used in 2015 test beam. | All chips working. |
| V5/6 | 8×B | chip 6 only 2.8 Ω to GND | 0.21/1.68 | 3.45/2.73 @ 340 V | Used on 2015 test beam. | 3 chips dead, 2 noisy, 3 working. |
| V5/7 | 7×B 1× A | all ok | 0.86/1.58 | 0.28/ 2.61 @ 340 V | Chip sees no events. Used in 2015 test beam. | 1 chip dead, 7 chips working. |
| V5/8 | 5×B 2× C 1×A | all ok | 0.26/1.63 | 23.6/24.7 @ 340 V | Used as spare in 2015 test beam. | Unknown. |
| V5/9 | 8×A | all ok | n.a./n.a. | 0.32/1.00 @ 340 V | Used in 2015 test beam. | All chips working. |

| No. | Chip types | Electronic test | LV current [A] | HV current [nA] | Comment | Status after test beam |
|---|---|---|---|---|---|---|
| V5/10 | 8×A | short on chip 6 ⇒ disconnected | 0.13/1.43 | 0.49/2.47 @ 340 V | Chip 5 sees no events. Used in 2015 test beam. | 1 chip disconnected, 1 chip dead, 6 chips working. |
| V5/11 | 8×B | all ok | n.a./n.a. | 0.09/0.33 @ 340 V | Chip 3 sees no events. Used in 2015 test beam. | 1 chip dead, 7 chips working. |
| V5/12 | 8×A | chip 3 LVDS output dead | 0.14/1.65 | 0.72/0.98 @ 340 V | Used in 2015 test beam. | 2 chips noisy, 1 disconnected, 1 dead, 4 chips working. |
| V5/13 | 7×A 1×A | all ok | 0.36/1.69 | 0.20/1.59 @ 300 V | Chip 4 always noisy, chip 8 sees no events. Used in 2015 test beam. | 1 chip dead, 7 chips working. |
| V5/14 | 3×D 2×A 2 ×D 1×B | short on chip 6 ⇒ disconnected | 0.21/1.39 | 0.32/1.88 @ 310 V | Used at 2015 test beam. | 1 chip disconnected, 7 chips working. |
| V5/15 | 8×A | all ok | 0.10/1.83 | 1.57/2.22 @ 300 V | Chip 7 sees no events. Used in 2015 test beam. | 1 chip dead, 7 chips working. |
| V5/16 | 8×A | all ok | 0.12/1.61 | 0.56/1.91 @ 310 V | Used in 2015 test beam. | All chips working. |
| V5/17 | 8×A | all ok | n.a./1.68 | 0.26/1.97 @ 340 V | Used in 2015 test beam. | All chips working. |
| V5/18 | 8×A | all ok | 0.23/1.44 | 0.60/ok. @ 340 V | Used in 2015 test beam. | 1 chip dead, 7 working. |
| V5/19 | 8×A | chip 6 only 1.5 Ω to GND | 1.16/1.57 | 0.69/2.33 @ 340 V | Used in 2015 test beam. | All chips working. |
| V5/20 | 8×A | all ok | 0.12/1.57 | 0.40/ok @ 340 V | Used in 2015 test beam. | All chips working. |
| V5/21 | 8×A | all ok | 0.10/1.44 | 0.60/ok @ 340 V | Used in 2015 test beam. | chip 1 working, short on chip 2 shutter, bond disconnected. Other chips not operational therefore. |
| V5/22 | 8×A | all ok | 0.10/1.47 | 0.50/2.20 @ 340 V | Chip 2 and 8 died in HV test, chip 3 and 7 only see noise. | 3 chips dead, 1 noisy, 4 working. |
| V5/23 | 8×A | chips 3 and 7 only 1.1 Ω to GND | 1.98/1.53 | 0.39/0.94 @ 340 V | Used in 2015 test beam. | 2 chips dead, 6 working. |

| No. | Chip types | Electronic test | LV current [A] | HV current [nA] | Comment | Status after test beam |
|---|---|---|---|---|---|---|
| V5/24 | 8×A | all ok | 0.11/1.22 | 0.39/ok @ 340 V | Used in 2015 test beam. | 4 chips dead, 3 noisy, 1 working. |

Table C.1: Timepix in- and output signals necessary for the operation.

APPENDIX D

# Event display images from the 2015 test beam

To monitor the behaviour of the detector, an online event display has been designed [148]. It displays the data just taken by the readout in a graphical way. The data file is interpreted and the individual hits are placed on the appropriate pixels on a chip at an octoboard. The counter value of the pixels is encoded in the colour code in the display being scaled from 0 (black) to 11810 (red). The colour gradient can be manipulated by hand by changing the maximum and minimum, such that a higher resolution in counter value by different colours can be achieved. As the display is just meant to look at the events online, it does not take the correct alignment of the different octoboards into account. Hence, straight tracks are not displayed as straight accumulations of hits on different boards.

A single octoboard can be selected by a double click in the overview part on the right part of the display. Then, the pixels of this octoboard are projected one-to-one to the screen pixels in the left part of the display. It is also possible to browse through an already completed run or to sum up the hits of a run in an occupancy image.

In Figure D.1-D.6, event display images from run 143 are shown. In this run, the beam was shot through the TPC parallel to the endplate, such that it passes all three modules. The moveable stage was set to z=−100 mm which means that the center of the beam profile was about 40 mm away from the anode. The beam energy was 6 GeV, the drift field 230 V/cm and the magnetic field 1 T.

Figure D.1 shows a typical event with a single track being registered on all three modules. In the right part of the display, the signals on all chips can be seen. Besides the signal from the track, there are two noisy chips, both on the central module, recognisable by the black and red bars at the upper chip edge (note that always the top row on an octoboard is rotated by 180°). There are some chips which are partially noisy in several columns as for example on the bottom module on the third lowest octoboard (which is also marked and shown in the enlarged view on the right) or the central module on the top right octoboard. Then, also single dead columns can be seen, which is most obvious on the enlarged octoboard on chip 1 (lower left), 2, 4 and 7 (top second to left). In the enlarged view, also the individual hits from the track can be seen. Every hit stems from a single primary electron, in case they have sufficiently diffused, which is probably not the case on chip 6. The colour code in the displays has been set such that the colour red indicates the maximum number of clock cycles, the chip can count during the shutter window. Electrons, which stem from ionisations close to the anode (were in the setup of this run the beam was focussed to) arrive the anode shortly after the shutter window was opened if one assumes that the displayed particle triggered the shutter. Hence, the pixels hit immediately start counting until the shutter closes. For that reason, the pixels hit by electrons from the primary ionisation of the beam

electron are displayed in red.
Figure D.2 is an image from the same run, but with several tracks, probably from an electron scattered in the TPC walls. On the bottom octoboards of the bottom module, a track with a completely different colour can be seen. This particle probably stems not from the triggered event and could be a second electron form the beam or, a cosmic particle or a particle from the same trigger, but at a different position further away from the endplate.
One feature of the Pixel-TPC is the high granularity, which allows to separate fine structures. This can be seen in Figure D.3 and D.4, where double tracks with a v-shape are shown. This means that they are clearly separated track in one part, but cannot be separated on another part. The question then is, how close they can be until it is impossible to identify two tracks. The octoboard at which this can be done by eye was selected for the detailed view. There, the center-to-center distance between the track signals is about 0.5 mm.
Another interesting feature resolvable by the Pixel-TPC is shown in Figure D.5, which shows a $\delta$-electron forming a small circle with a radius of about 3 mm in the magnetic field. Using Equation 2.4, the transverse momentum of the particle can be calculated to about 1 MeV.
A more ornate image is shown in Figure D.6, which reminds of famous bubble chamber images. It shows several tracks of particles curling through the entire TPC in the magnetic field. The track from the trigger particle can be seen on the bottom module. In these images, also the not operational chips on the central module can be seen, as those did not register a signal.
In Figure D.7, the image of a track from a different run is shown. In the setup for run 167, the LP was rotated and the beam was shot with an angle of $-34°$ with respect to the endplate through the TPC. The displayed colour of the pixels hit hence changes from red at the bottom to blue at the top. Here, the colour range was set such that the track is displayed with the maximum gradient. Again, hits displayed in red stem from ionisations close to the endplate, whereas those in displayed in blue had to drift a longer distance through the TPC and hence arrived the endplate at a later time in the shutter window. The hit pixels hence counted a lower number of clock cycles until the end of the shutter window. The larger distance to the endplate of the blue part of the track can also be seen from the width of the distribution of hits. In the blue part, the track is wider, because those electrons have diffused along their drift.
Finally, Figure D.8 and D.9 show frames with corrupted data on some octoboards.

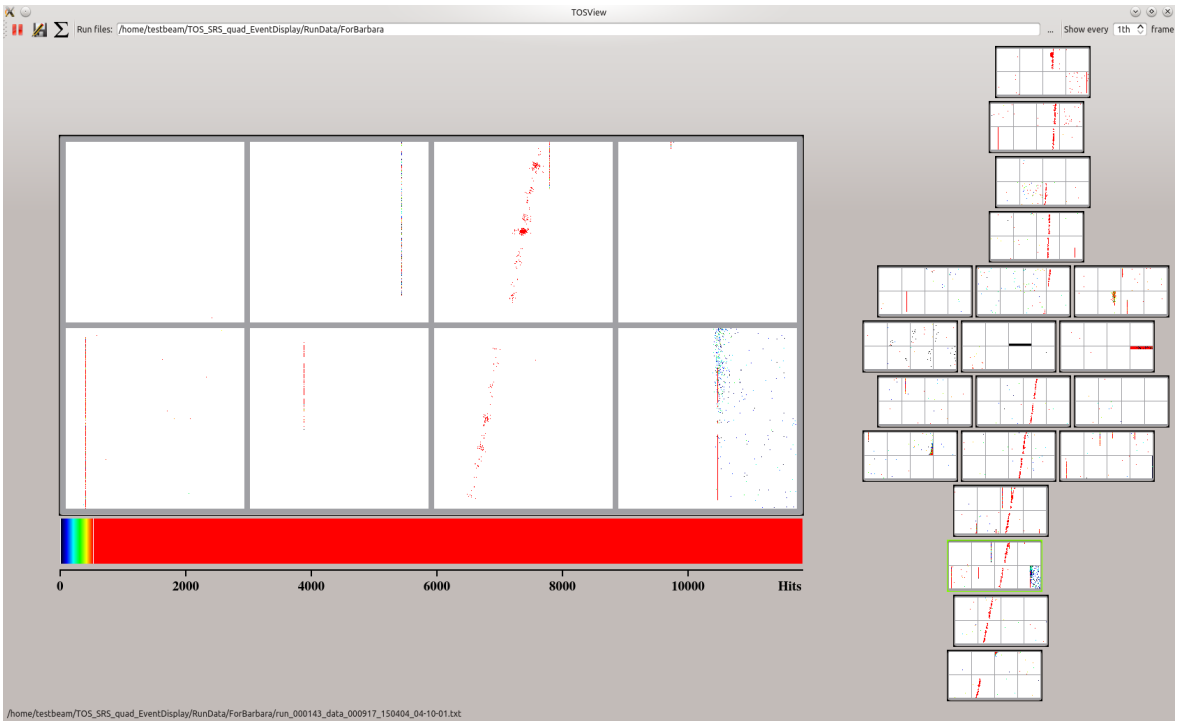



Figure D.1: Event display image of a typical event from the 2015 test beam. Besides the single track, noisy pixels, dead columns and completely noisy chips can be seen.

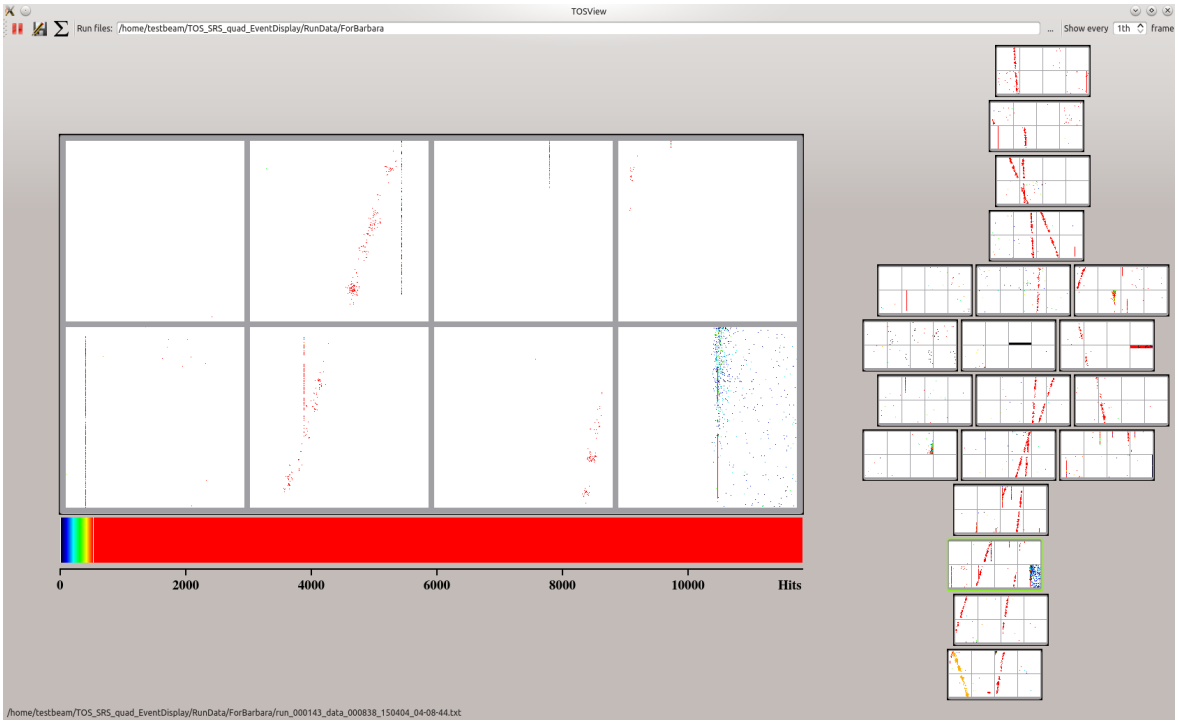



Figure D.2: Event display image of an event from the 2015 test beam with several tracks, of which for the one on the bottom octoboard, the arrival time of the individual hits are significantly different than for the other tracks.

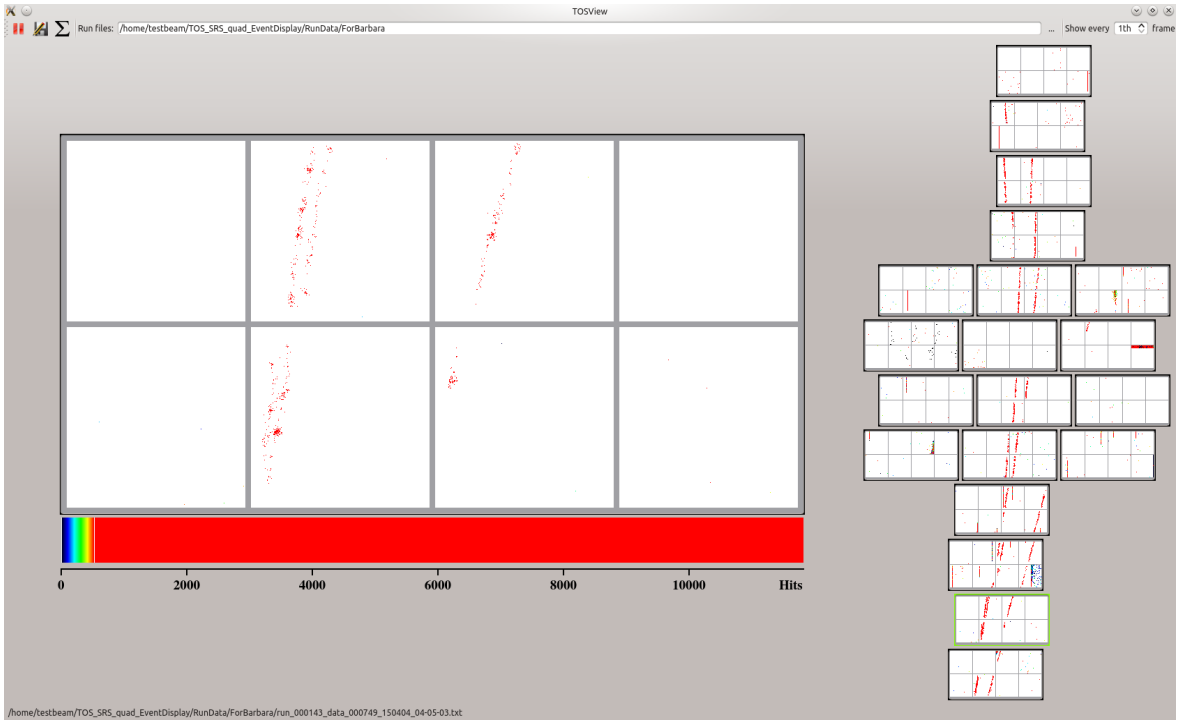



Figure D.3: Event display image of an event from the 2015 test beam with a double track and an additional track. The octoboard, at which the tracks can still be separated by eye was selected. The distance between the tracks is about 0.5 mm there.

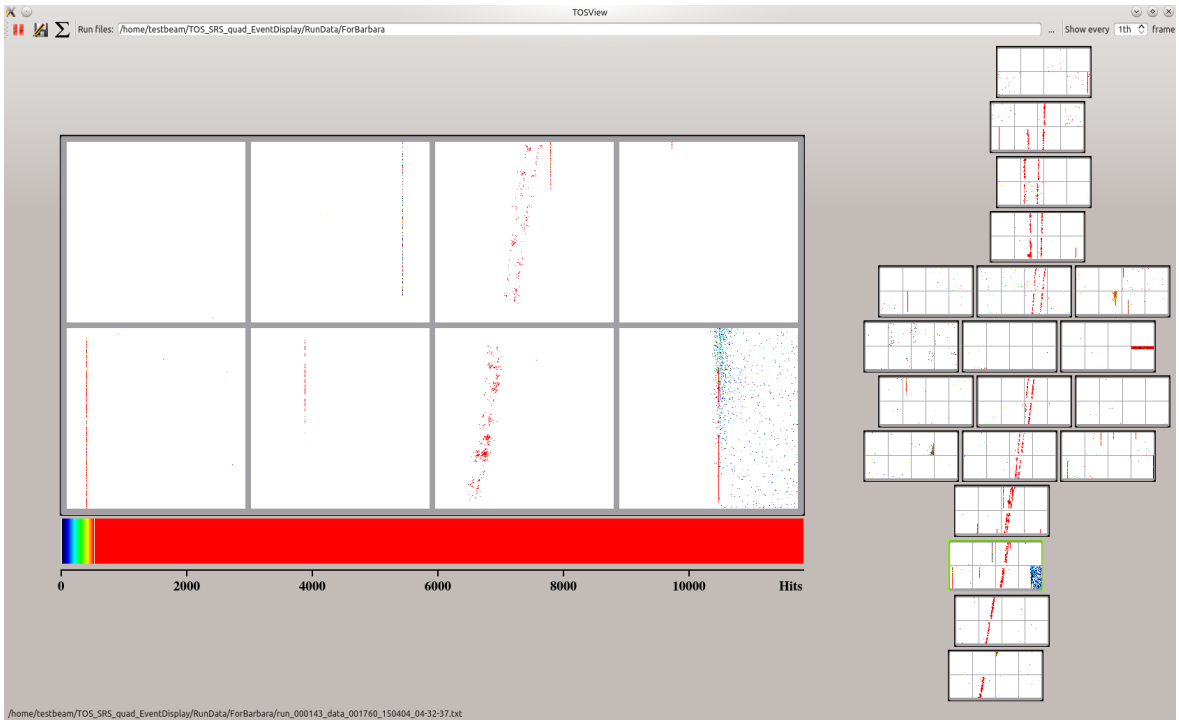



Figure D.4: Event display image of an event from the 2015 test beam with a double track. The octoboard, at which the tracks can still be separated by eye was selected. The distance between the tracks is about 0.5 mm there.

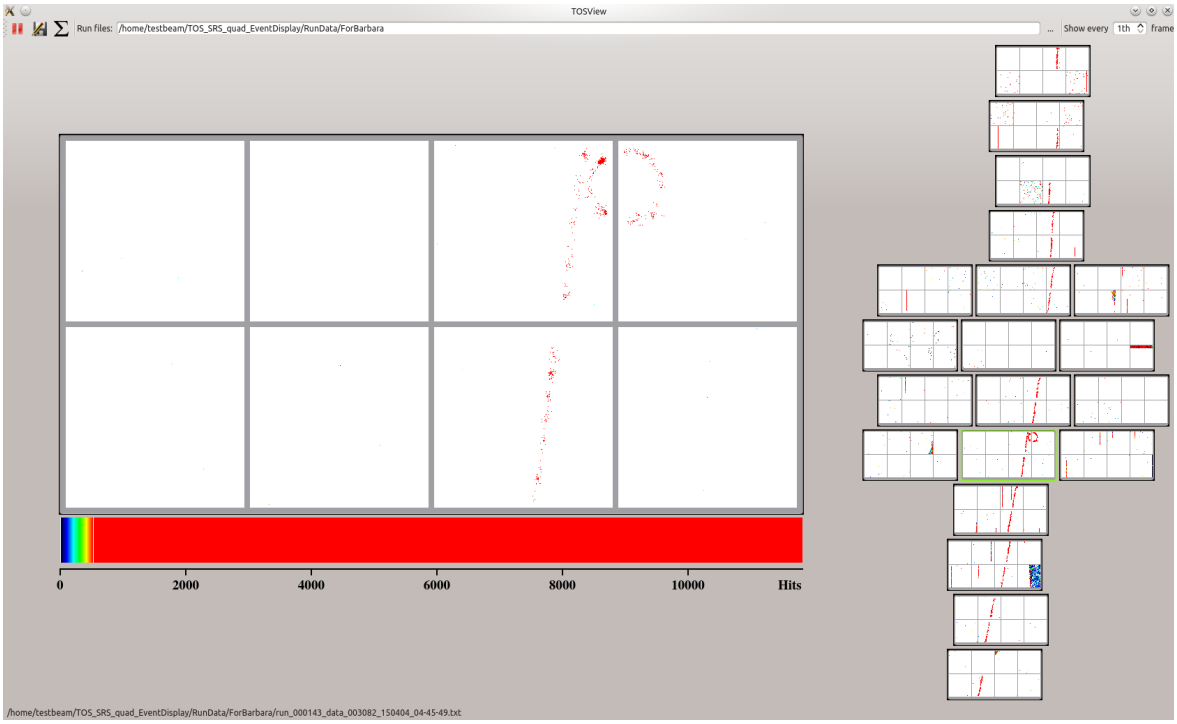



Figure D.5: Event display image of an event from the 2015 test beam with a single track releasing a delta electron. From the radius of the delta electron, which is about 3 mm, it can be deduced that the particle had an energy of about 1 MeV.

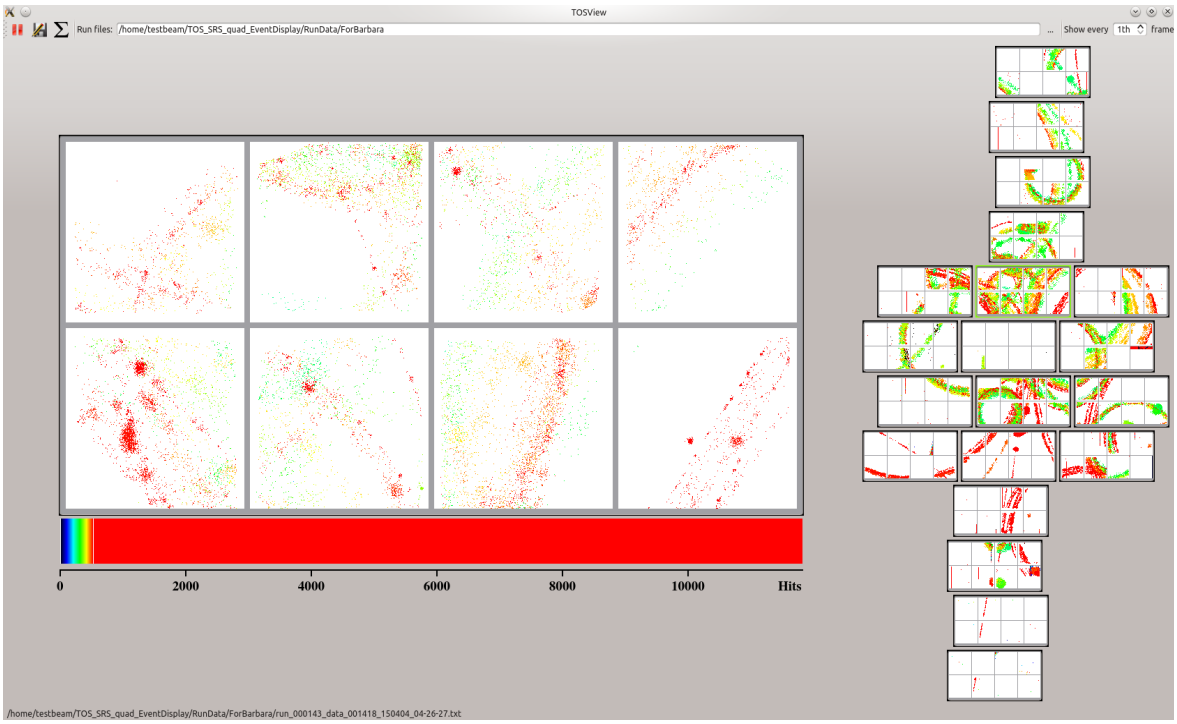



Figure D.6: Event display image of an event from the 2015 test beam with many low energetic particles curling in the TPC.

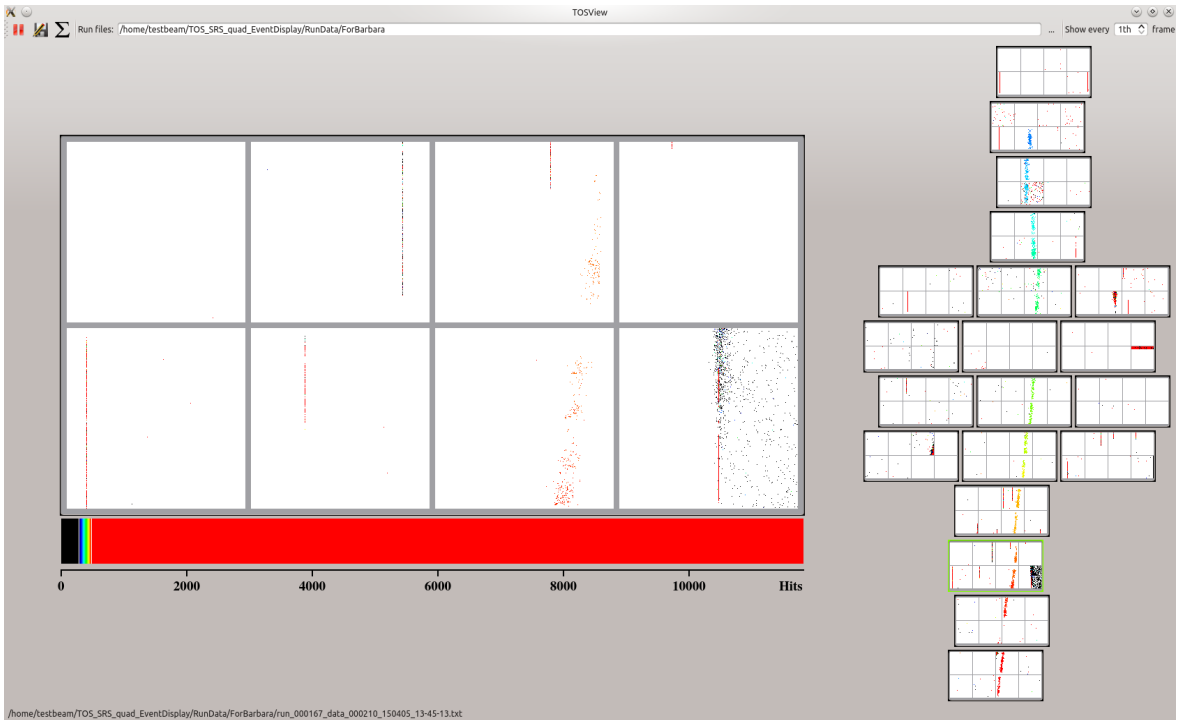



Figure D.7: Event display image of an event from the 2015 test beam showing a single track. From the different colours of the hits, it can be deduced that the track has an angle towards the endplate, as the hits were registered at different arrival times.

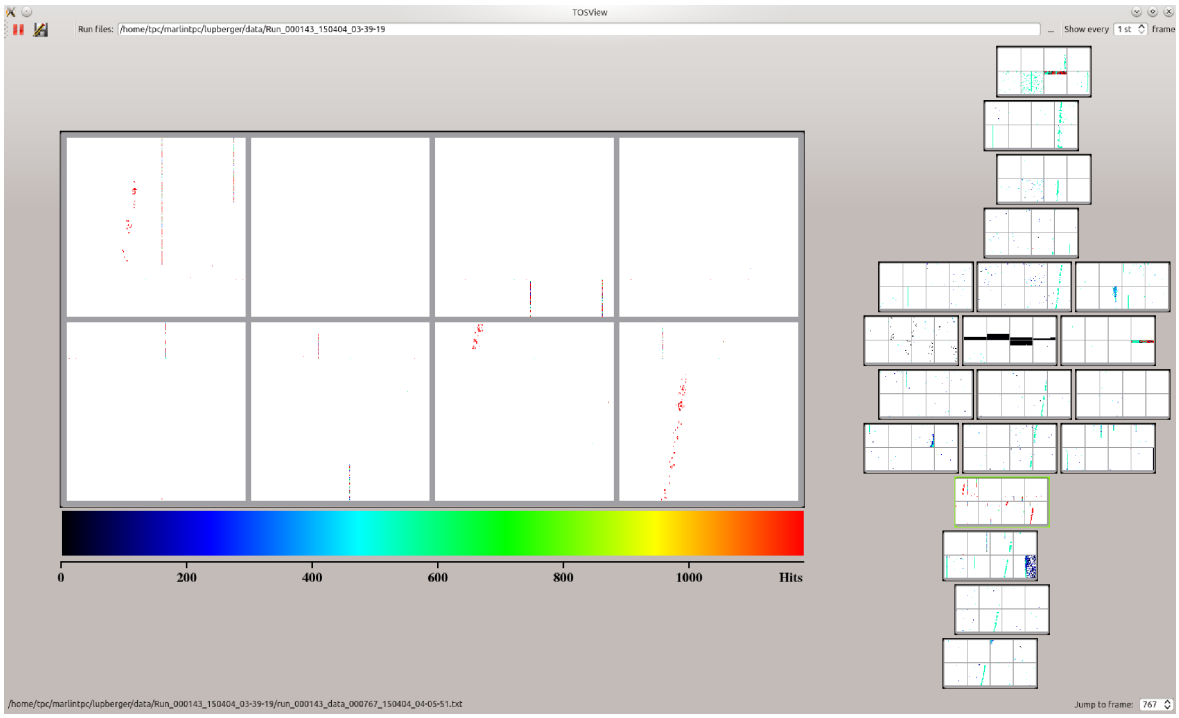



Figure D.8: Event display image of an event from the 2015 test beam with corrupted data on an octoboard.

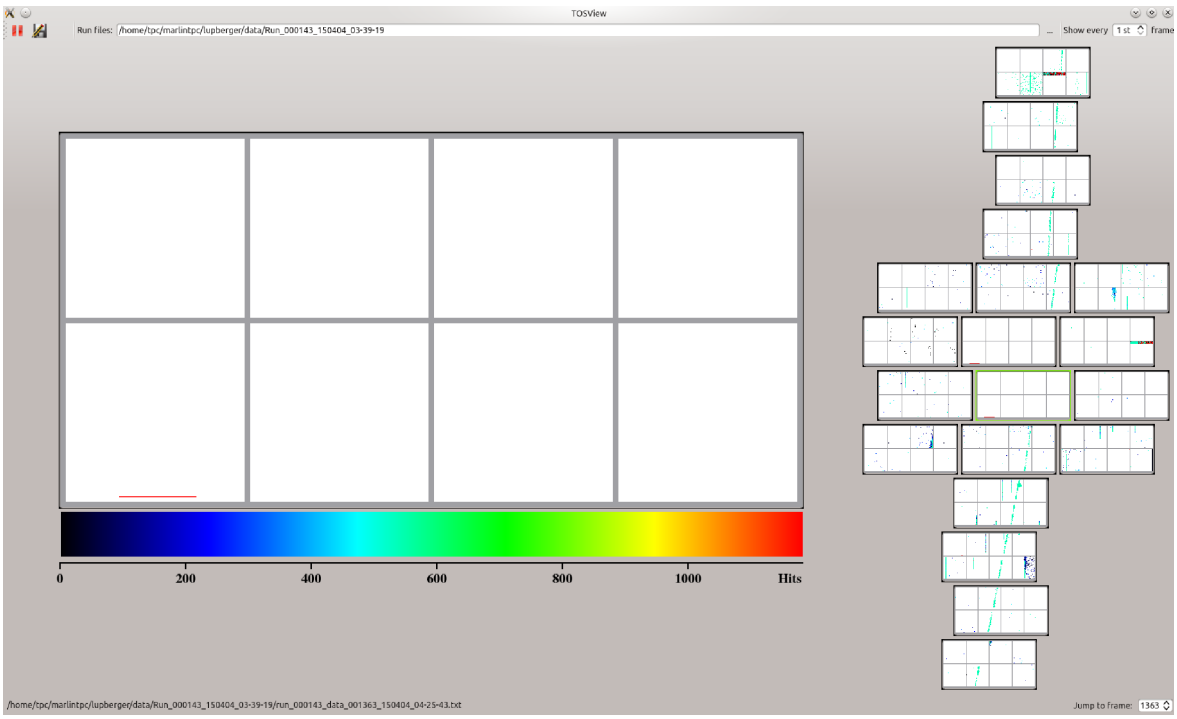



Figure D.9: Event display image of an event from the 2015 test beam with corrupted data on two octoboards.

APPENDIX E

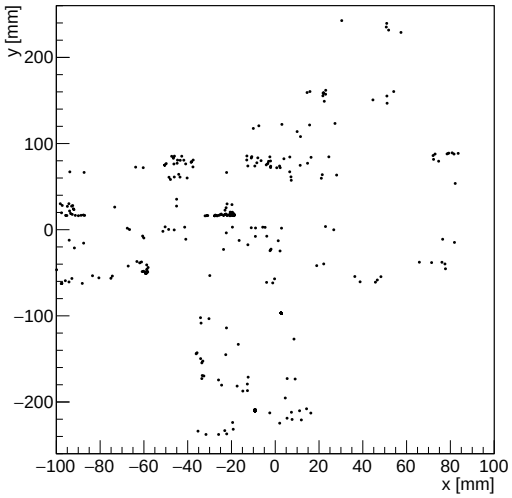
# The circle finder: A track finder for curved tracks

In this appendix, the track finding algorithm developed for the analysis of curved tracks is explained. The method uses a global approach, which means that all hits in the event are treated together. It has to be noted that the algorithm is in a preliminary state and not completely developed. Therefore, there are many aspects which can be optimised or extended.

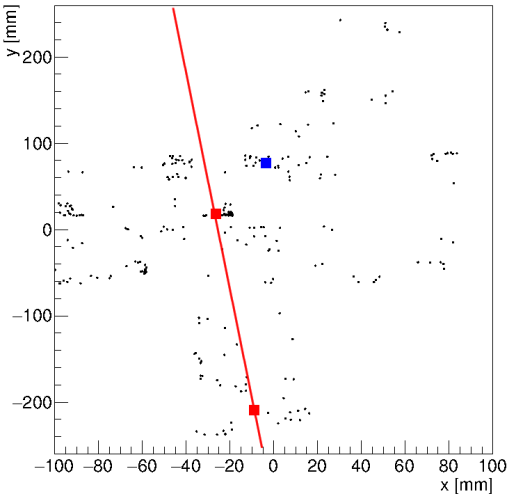
## E.1 Algorithm at a glance

The basic idea of the `CircleFinder` is that the hits of a track passing through the magnetic field are distributed on a circle arc in the xy-plane. Because of that assumption, the algorithm favours a curved track model and is not designed to find straight tracks. It only searches for tracks by using the xy plane. The z-position of a hit is not taken into account so far.
As a starting point, two hits in the event are randomly selected and the line between them is calculated. Figure E.1a shows an event with only noise. In Figure E.1b, the first step has been performed. Next, a third hit is randomly selected. If this third point is close to the line between the first two hits, the algorithm proceeds. This is very unlikely the case for an event with only noise. For a track as in Figure E.2, there are many hits close to a line between two other hits. If the condition is fulfilled, an orthogonal line is calculated such that it crosses the line between the two hits.
This is shown in Figure E.2b. The two hits marked in red were randomly selected and the red line was calculated. Then the hit marked in blue was randomly selected and fulfilled the condition, such that the orthogonal line in blue was calculated. This procedure is repeated for a defined number of times that should possibly depend on the number of hits in the event. For the time being it is repeated 10 000 times.

If the event contains a curved track, the orthogonal lines theoretically intersect in the center of the circle. Finding the circle (3 degrees of freedom) has been transformed to finding the circle center (2 degrees of freedom). The circle radius can then simply be found by the distance of the hits to the center.
First, almost straight, long tracks shall be found. As the tracks can have a moderate curvature, the parameter space where the circle center can be found is large. Therefore, the circle center finding is the most difficult part of the algorithm.
Second, the parameters of all orthogonal line are analysed. In the endplate coordinate system, each line

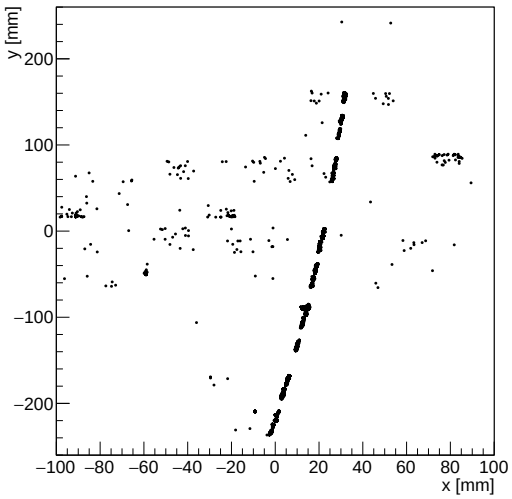



(a) Example of an empty event.

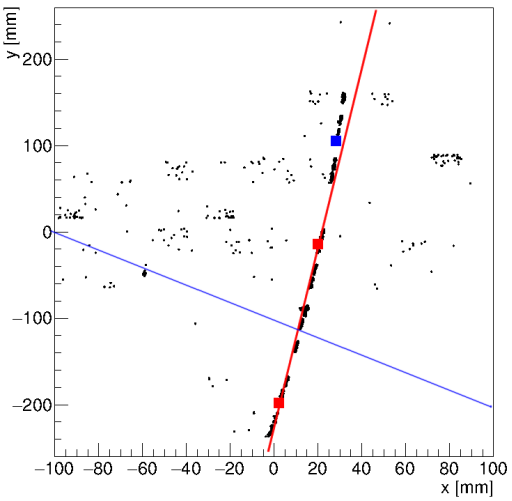



(b) Starting point of the circle finder. The displayed line would be rejected, as the third hit marked in blue is to fare away.

Figure E.1: Event with only noise.




(a) Example of an event with a track




(b) Starting point of the circle finder. The displayed line would not be rejected, as the third hit marked in blue is close enough. The blue line orthogonal to the red one and through the center between the hits marked in red is calculated.

Figure E.2: Event with a track to reconstruct.

is parametrised by the angle to the y-axis phi and the minimum distance to the origin $D_0$. In Figure E.3, the distribution of the phi angles is shown and a prominent peak can be seen. Such a peak is expected, as the orthogonal lines from an almost straight, long track on the circle arc recorded by the module almost point to the same direction. The phi value at the maximum ($phi_{max}$) is extracted from the distribution. The same is done for $D_0$. With $D_{0,max}$ and $phi_{max}$, a main orthogonal line can be constructed. Then, the complete space is rotated by $-phi_{max}$ and shifted by $-D_{0,max}$, such that the main orthogonal line is the x-axis.[1]

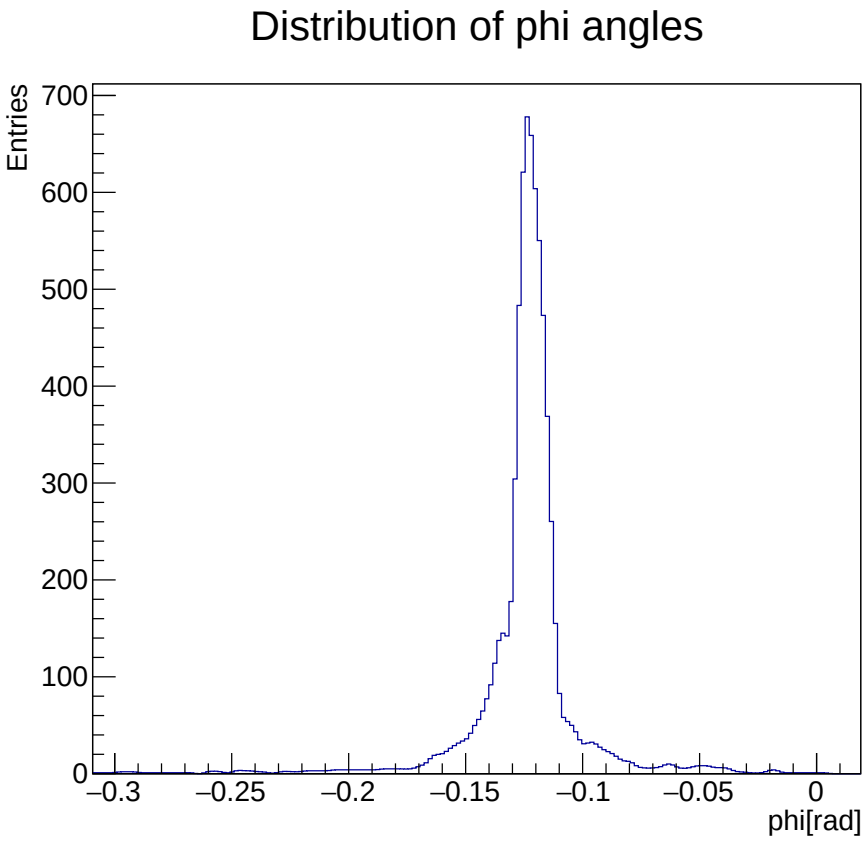
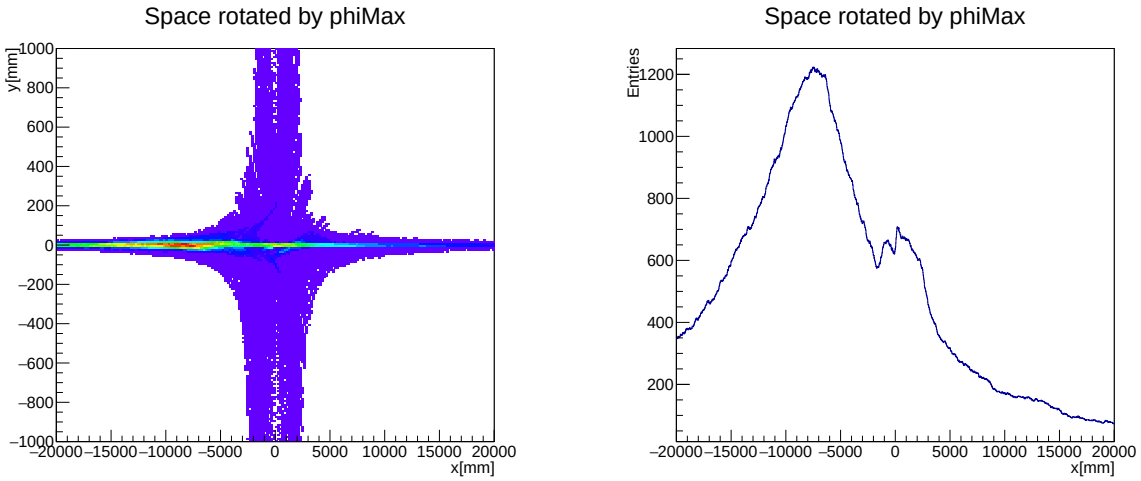



Figure E.3: Distribution of orthogonal lines phi angles.

For each rotated orthogonal line, the intersect with the main rotated orthogonal line (the x-axis) is calculated and the line is drawn in a 2D histogram called rotated space (see Figure E.4a) in a defined interval around that intersect. This is only done because the drawing of all lines is the most time consuming part of the algorithm and therefore, they cannot be drawn in the complete space, which in the current state of the algorithm ranges form $x_{min} = -20\,\text{m}$ to $x_{max} = 20\,\text{m}$. In the rotated space, the maximum needs to be found. Again because of the large space, finding this maximum cannot be done by going through all bins. Instead, an interval around the x-axis is projected on the x-axis. That way, the search problem is transferred from 2D to 1D. That is also the reason, why the space has been rotated.
Now, the maximum of the 1D projection shown in Figure E.4b can be extracted. This value is the position of the rotated circle center. Rotating it back by $phi_{max}$ gives the coordinates of the circle center

[1] At this point an improvement can be implemented, if depending on the value of $phi_{max}$, the space is rotated such the main orthogonal line becomes either the x- or the y-axis. In the current implementation with the x-axis, tracks along the y-direction are preferred by the finder.




(a) Space with the intercetions of the orthogonal lines rotated by phi$_{max}$.

(b) Projection of the rotated space on the x-axis. A few bins around the x-axis are projected, in case phi$_{max}$ has not been deduced accurately. The peak in the distribution stems from the accumulation of intersecting othogonal lines at the circle center.

Figure E.4: Event with a track to reconstruct.

$x_{max}$ and $y_{max}$, from which the distance to the module center is calculated. This value is needed to define another 1D plot, in which the distance of each hit to the circle center is plotted. If the circle center has been correctly found, all hits of a track should have the same distance, which is only smeared out by diffusion.

This distribution is plotted (see Figure E.5a) and fitted at the maximum value[2] by a Gaussian curve and the sigma and mean value mean$_{fit}$ are extracted. Note that the 1D plot with the hit distance to the circle center is the best way to distinguish two parallel tracks which cannot be separated already in the phi plot.

For the assignment of hits to the track, the distribution is used again. All hits in a defined sigma range around $textmean_{fit}$ are assigned to the track.

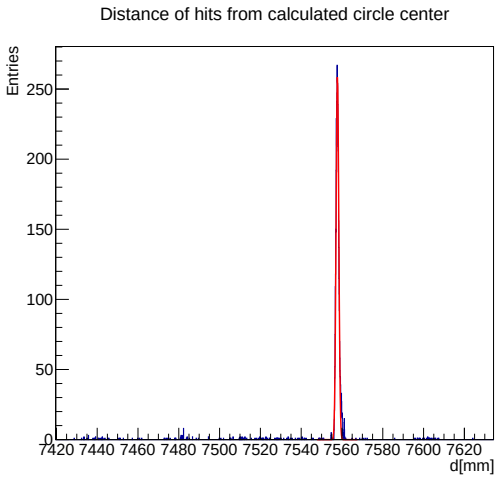
This makes the finder robust, as even if the circle center has not been accurately found, which widens the hit distance distribution, the hits are correctly assigned. In a later step of the reconstruction, the track fitter than can find the correct track parameters.

Now, the track candidate can be constructed. The $\phi$ angle of the track is given by phi$_{max} + \pi/2$, the track D$_0$ by the distance of the circle center minus $textmean_{fit}$ and the track curvature $\Omega$ by $-1/textmean_{fit}$.

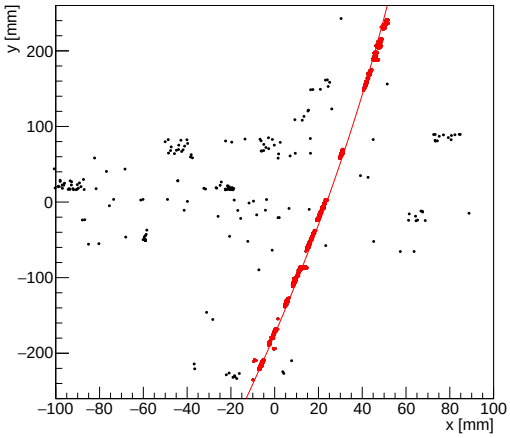
Figure E.5b shows the final reconstructed track candidate as red line and the assigned hits marked in red.

The assigned hits are removed from the event and the search starts again if a sufficient number of hits is left.

[2] There could be several distributions from different tracks and only one is selected that way.




(a) Distance of hits to calculated circle center. A Gaussion distribution is fitted to the highest peak. The hits within a defined range around the fit mean are assigned to the track.




(b) Example of a track reconstructed by the circle finder. The red line desribes the track candidate calculated from the track parameters, the hits marked in red are assigned to the track.

Figure E.5: Assignment of hits to the track.

## E.2 Features in mind during the design

As the name suggests, the algorithm finds circles. Particles of low momentum are curling in the TPC on circular trajectories and should give a sharp maximum in the space of orthogonal line intersections. Their circle center will be very close to the accumulation of hits. Hence, such curlers are objects which can be found by the algorithm if the focus is put on them.
Double track separation is an important task of the track finder. In principle, the `CircleFinder` is designed to separate tracks already at the very beginning when the maximum in the phi distribution is selected. Explicitly, not the mean, but the maximum was chosen in case there are several peaks. Only if the different tracks are parallel to each other, this will not work. In this case, the separation will be done in the 1D plot of the hit distance.

## E.3 Limitation

In the current status, the algorithm is designed to preferably find long, almost straight tracks as needed for the preliminary analysis. Therefore, it only searches for the maximum in the projection plot at radii larger than ±2 m. If the maximum is inside this interval, it tells the user that there might be tracks with smaller radii or curlers but does not search them. Instead, it looks for second maxima outside the interval.
For curlers and low momentum tracks, it might be better to search for the maximum of orthogonal line intersection in the now limited 2D space.
As can be deduced from the explanation of the algorithm, the circle center finding is the most critical part. If the position is incorrect, the hits might still be correctly assigned in single track events. For events with several tracks however, the algorithm looses its power. Therefore, a more robust method to find the circle center would be helpful. However, the computing time does no have to increase

significantly.

## E.4 Computing time

The run time of the algorithm has been compared to the Normal Hough Transformation processor and needs about the double amount of time per event. This is acceptable as it finds curved tracks, which needs one further dimension. The most time consuming part is the filling of the space by drawing orthogonal lines which is already limited to a small interval where the circle center is expected. There might be still some parts of the code which can be optimised concerning computation time.

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# Acronyms

**ADC** Analogue-Digital Converter. 63, 67, 68, 71, 78, 87, 88, 90, 92, 100, 101, 172, 175, 176

**ALICE** A Large Ion Collider Experiment. 6, 17, 22

**ARP** Address Resolution Protocol. 54

**ASIC** Application Specific Integrated Circuit. 25, 35, 37, 38, 41, 44, 79, 80, 82, 84, 88, 91, 161

**ATCA** Advanced Telecommunications Computing Architecture. 51

**ATLAS** A Toroidal LHC Apparatus. 5, 42

**CAD** Computer-Aided Design. 74, 115, 116, 133, 223

**CAST** CERN Axion Solar Telescope. 42, 59, 64, 65, 162

**CDC** Clock Domain Crossing. 95

**CERN** European Organization For Nuclear Research. 5–7, 25, 26, 38, 59, 64

**CLB** Configurable Logic Block. 43, 51

**CLIC** Compact Linear Collider. 7

**CMOS** Complementary Metal-Oxide-Semiconductor. 25, 34, 63, 66–68, 70–72, 159

**CMS** Compact Muon Solenoid. 5

**CTPR** Column Test Pulse Register. 29, 32–34

**DAC** Digital-Analogue Converter. 27–29, 32–34, 63, 67, 68, 71, 75, 77, 78, 87, 90, 92, 98, 100–103, 171, 172, 175, 176, 187, 222, 227

**DAQ** Data Acquisition. 34, 51, 53, 57, 74, 77, 98, 116, 120, 157, 162, 171

**DATE** ALICE Data Acquisition And Test Environment. 51

**DC** Direct Current. 28

**DCM** Digital Clock Manager. 86

**DDR** Double Data Rate. 52, 95

**DDR2 SDRAM** Double Data Rate Synchronous Dynamic Random Access Memory. 95, 96, 177, 178

**DESY** Deutsches Elektronen-Synchrotron. 38, 54, 56, 74, 105, 106, 113, 115, 127, 150, 159, 181, 185, 222

**DOD** Department Of Defence. 53

**DSL** Digital Subscriber Line. 53

**EEPROM** Electrically Erasable Programmable Read-Only Memory. 44, 52

**ENC** Equivalent Noise Charge. 29, 34

**EWSB** Electroweak Symmetry Breaking. 7

**FDL** Fast Discriminator Logic. 28

**FEC** Front-End Concentrator. 51–53, 59, 64–68, 74, 75, 77, 78, 84–89, 92, 93, 95, 105, 106, 116, 117, 155, 166, 185, 186, 222

**FF** Flip-Flop. 43, 44, 48

**FHT** Row Based Fast Hough Transformation Processor. 145, 146

**FIFO** First In, First Out. 95, 96

**FMC** FPGA Mezzanine Card. 52, 60, 63, 64, 222

**FPGA** Field Programmable Gate Array. 25, 43, 44, 47, 49–53, 58–60, 63, 64, 66, 68, 71, 73, 74, 77, 79–86, 88, 89, 91–93, 95, 97, 98, 100, 101, 103, 120, 159, 170, 172, 221, 222

**FSR** Fast Shift Register. 26, 29, 31–33, 79, 80, 90, 97, 101, 102

**FWHM** Full Width at Half Maximum. 141, 142

**GEM** Gas Electron Multiplier. 17, 23, 26, 37, 38, 74, 107, 108, 113, 161, 221, 223

**GOSSIP** Gas On Slimmed Silicon Pixel. 38, 42

**HDL** Hardware Description Language. 44, 47, 48

**HDMI** High Definition Multimedia Interface. 51, 59, 66–75, 82, 115, 116, 166, 222, 227

**I/O** Input/Output. 26, 32, 43, 44, 52, 70, 81, 88, 95, 227

**I2C** Inter-Integrated Circuit. 63, 67, 68, 70–73, 81, 87–92, 166, 169, 172, 175, 176

**IC** Integrated Circuit. 63, 67–69, 71, 73–75, 87, 89–91, 103

**ILC** International Linear Collider. 3, 4, 7–9, 22, 161, 221

**ILD** International Large Detector. 10, 11, 13, 14, 20–22, 54, 56, 158, 162, 164, 221, 222

**IP** Internet Protocol. 53–55, 74, 80, 170, 171, 222

**ISO** International Organisation For Standardisation. 53

**LCIO** Linear Collider Input/Output. 108, 120–122, 125, 223

**LCTPC** Linear Collider TPC. 38, 54, 161

**LDO** Low-Dropout Regulator. 68, 113, 118, 154

**LED** Light Emitting Diode. 52, 64, 86, 87, 94, 97, 166, 172, 175, 177

**LEP** Large Electron-Positron Collider. 5–7

**LHC** Large Hadron Collider. 3–7, 22, 51

**LHCb** Large Hadron Collider Beauty. 5

**LP** Large Prototype. 38, 54, 56, 74, 75, 105, 106, 115, 116, 119, 181, 182, 185, 186, 192, 222–224

**LSB** Least Significant Bit. 33

**LUT** Lookup Table. 31, 43, 44, 48, 49, 51

**LVDS** Low Voltage Differential Signalling. 27, 28, 32, 58, 63, 64, 67, 68, 70–73, 189

**MAC** Media Access Controller. 53, 54, 88, 92, 168–171, 174, 175

**MarlinTPC** Modular Analysis And Reconstruction For The Linear Collider TPC. 108, 114, 120–126, 132, 136, 145, 147, 156, 162, 163, 223, 224

**MAXIPIX** Multichip Area X-Ray Detector Based On A Photon-Counting Pixel Array. 58

**MCP** Micro-Channel Plate Detector. 58

**Micromegas** Micro-Mesh Gaseous Structure. 17, 23–26, 35–38, 158, 161, 221

**MIP** Minimum Ionising Particle. 12, 42

**MMCM** Mixed-Mode Clock Manager. 86

**MPGD** Micro-Pattern Gaseous Detector. 17, 36, 37, 54

**MSB** Most Significant Bit. 33

**MUROS** Medipix Universal Read-Out System. 57–59, 61–64, 66, 222

**MWPC** Multi-Wire Proportional Chamber. 11, 17, 36

**OSI** Open Systems Interconnection. 53

**OTA** Operational Transconductance Amplifier. 28

**PAI** Photo-Absorption Ionisation. 141

**PCB** Printed circuit Board. 60–63, 66, 73, 74, 118, 156

**PCI** Peripheral Component Interconnect. 51, 64, 74, 85

**PLL** Phase Locked Loop. 44, 86, 168

**PMOS** p-Channel Metal-Oxide Semiconductor. 28

**PRIAM** Parallel Readout Image Acquisition For Medipix. 58

**RAM** Random-Access Memory. 92, 93, 95

**RMS** Root Mean Square. 110, 142, 149, 152, 153

**ROM** Read-only Memory. 93, 94

**RTL** Register Transfer Level. 46, 49, 221

**SEM** Scanning Electron Microscope. 23, 35, 36, 40, 41, 221

**SFP** Small Form-Factor Pluggable. 51, 166, 168

**SiD** Silicon Detector. 10, 22

**SNR** Signal-To-Noise Ratio. 28

**SRS** Scalable Readout System. 25, 43, 51, 52, 58–60, 62–70, 74, 84–87, 98, 100, 101, 103, 105, 106, 113, 115, 119, 162, 169, 185, 186, 222

**SRU** Scalable Readout Unit. 51, 65, 66

**TCP** Transmission Control Protocol. 53

**TOA** Time Of Arrival. 30, 31, 34, 91, 116, 120, 121, 124–128, 130, 131, 159, 223

**TOS** Timepix Operating Software. 77

**TOT** Time Over Threshold. 30, 31, 34, 101, 102, 116, 118, 119, 159

**TPC** Time Projection Chamber. 4, 10, 11, 13–22, 25, 26, 30, 37, 41, 42, 54, 56, 57, 74, 80, 91, 92, 105–107, 109, 110, 115–119, 126–128, 130, 131, 137, 150, 152, 155–159, 161–164, 181, 191, 192, 195, 203, 221, 222, 224

**TSL** Timepix Synchronisation Logic. 27, 29

**TSV** Through-Silicon Via. 157

**UDP** User Datagram Protocol. 53, 55, 77, 80, 81, 87, 169, 171, 222

**USB** Universal Serial Bus. 53, 57–59, 62–64, 66, 222

**VHDCI** Very-High-Density Cable Interconnect. 57–59, 61–70, 74, 100, 105, 113, 222

**VHDL** Very High Speed Integrated Circuit Hardware Description Language. 44, 45, 47

**WHT** Timepix Windowed Randomized Hough Transform. 146

**WIMP** Weakly Interacting Massive Particles. 42

**XFEL** X-Ray Free-Electron Laser. 7

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