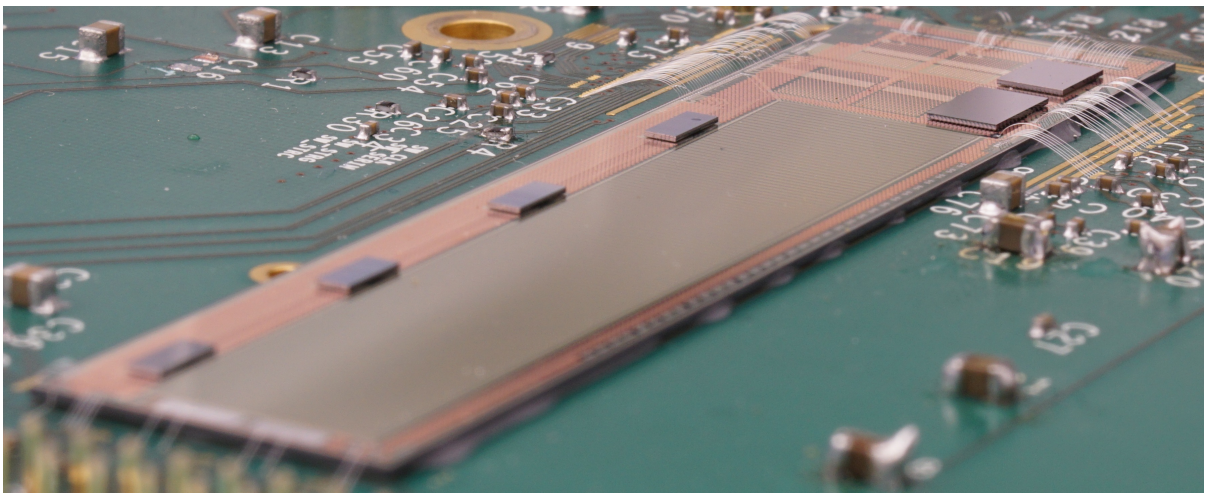
Development of Pixel Modules for the Belle II Detector



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Contents

Table of Acronyms

DEPFET **DE**pleted **P**-channel **F**ield **E**ffect **T**ransistor

DCD **D**rain **C**urrent **D**igitizer

DCD-RO **DCD** **R**ead**O**ut

DHP **D**ata **H**andling **P**rocessor

DHE **D**ata **H**andling **E**ngine

DHH **D**ata **H**andling **H**ybrid

DHC **D**ata **H**andling **C**oncentrator

PXD **P**i**X**el **D**etector

SVD **S**ilicon **V**ertex **D**etector

VXD **V**erte**X** **D**etector

FPGA **F**ield **P**rogramable **G**ate **A**rray

ROI **R**egion **O**f **I**nterest

ASIC **A**pplication **S**pecific **I**ntegrated **C**ircuit

ADC **A**nalog to **D**igital **C**onverter

DAC **D**igital to **A**nalog **C**onverter

SM **S**tandard **M**odel

ONSEN **ON**line **SE**lector **N**ode

DATCON **DAT**a **CON**centrator

HLT **H**igh **L**evel **T**rigger

MPV **M**ost **P**robable **V**alue

MIP **M**inimum **I**onizing **P**article

TLU **T**rigger **L**ogic **U**nit

CHAPTER 1

Introduction

"What are things made of?" is a question which was already asked by ancient Greek philosophers. The first philosophers to suggest the idea of an undividable building block of matter were Leucippus and his successor Democritus, who coined the term "atomos" (indivisible) for those building blocks [1]. However, in absence of conclusive experiments, this theory was opposed by most philosophers. In the early 19th century, an atomic theory was described, based on observations like the law of definite proportions and the law of multiple proportions. Since then knowledge about the most fundamental building blocks of the universe has been greatly expanded, cumulating in the currently accepted **S**tandard **M**odel (SM) of particle physics. This model contains all known fundamental particles (three families of quarks and leptons), the interactions between them due to the strong force, the weak force and the electromagnetic force, as well as the force carriers. In 2012 the Higgs Boson was discovered at ATLAS and CMS, two detectors located at the LHC accelerator at CERN, experimentally verifying the Higgs Mechanism which is required by other measurement results [2]. However, the SM can't be correct as it is, since there are several unexplained phenomena:

- The SM describes three fundamental forces acting on particles. Gravity is not included.
- Astronomy shows, that there has to be more than the visible matter to support the universe. This is known from the rotational speed of galaxies, which should drop off far from the center of the galaxy, but does not. Estimates of matter in a galaxy based on emitted light and based on the rotational speed yield different results. This and other observations can be explained by dark matter and dark energy. Current theories suggest, that dark matter makes up 27% of the energy in the universe and that 68% of the universe is made up by dark energy. Therefore, only 5% of the universe is built from matter and energy described by the SM [3].
- Neutrinos in the SM need to be massless, however observed neutrino oscillation requires a non-zero neutrino mass >0 [4]
- The observable universe is made mostly out of matter. There is no explanation in the SM to explain the matter-antimatter asymmetry; it predicts that almost the same amount of matter and antimatter should have been created.

Despite of all these weaknesses, the SM describes all (currently) observed effects in particle physics. Further tests of the SM are needed to check its validity range and to find deviations from the known SM. These deviations, so called physics beyond the SM, will hint towards new theories, increasing our knowledge about the universe. One possibility to test for physics beyond the SM is the precision approach, where precision measurements search for deviations from the SM due to higher order effects.

Some of these precision measurements can be performed in the so called “B factory”, a collider which produces B mesons to study their decay spectrum and rare processes within it. B factories are asymmetric energy e^+/e^- colliders running at center of mass energy of 10.58GeV, which is the energy of the Y(4S) resonance, mainly producing $B/\bar{B}$ meson pairs. Historically, the two experiments that establish the CKM model of quark mixing, (measuring V_{ub} and V_{cb}) and were the first to show direct CP violation (outside the kaon system) have been Belle at the KEKB collider and BaBar at PEP-II collider [5]. Many further measurements were possible due to the rich decay spectrum of B mesons [6].

In 2010 the Belle detector stopped its successful 10 year operation for an upgrade. Discovery of physics beyond the SM is possible using rare decays in the B meson system and precision measurements SM parameters. This needs an order of magnitude more data, which cannot be recorded in a reasonable time with existing machines.

Therefore, the KEKB collider is upgraded to the "SuperB factory" SuperKEKB, which started test operation at the beginning of 2016 and will go into physics operation around 2018. It is an asymmetric e^+/e^- collider running at the center of mass energy of the Y(4S) resonance. Delivering 4 GeV/7 GeV e^+/e^- at beam currents of 3.6 A/2.6 A respectively, it will achieve an unprecedented instantaneous luminosity of $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}$, about 40 times higher than the current world record set by KEKB. The increase in luminosity is achieved by squeezing down beams to $\sigma_1 y = 48\,\mathrm{nm}$, $\sigma_2 y = 63\,\mathrm{nm}$ at the interaction point [7]. The increased luminosity translates in both higher event rates and higher background rates.

To cope with these requirements, the Belle detector is upgraded to Belle II. For each particle in an event, the detector has to measure its momentum, charge, type, energy and the position of its vertex. This requires the first layer to have a resolution in the order of a few µm and to be as close as possible to the interaction point, which in a high luminosity environment implies both high track density and substantial background occupancy. Thus, the first layers of Belle II need to have a high number of readout channels, a high readout speed and need to withstand a high amount of ionizing radiation. Since particles at Belle II typically have low momentum, multiple scattering has to be minimized using thinned detectors with a minimal material budget. These challenging requirements can be met by a DEPFET silicon pixel detector.

A **DE**pleted **P**-channel **F**ield **E**ffect **T**ransistor (DEPFET) detector is a pixelated detector which integrates detection and amplification directly into each pixel [8]. For Belle II, large all silicon modules will be produced with a thickness of only 75 µm in the sensitive area. The modules do not need further support or cooling inside the acceptance region since the main readout electronic of the DEPFET detector is placed outside of the acceptance region. [9] Ionizing particles passing the detector modulate the drain current of the pixel transistors which is digitized by the DCD ASIC for each pixel. Since the amount of data produced by this ASIC is too high to be transported off-module, data is reduced using a second DHP ASIC for on module zero suppression [9].

The integration and optimization of such a system was the main task of this thesis. Much emphasis was put on characterization of the DCD, as it is one of the most performance critical building blocks of the detector. With an optimized DCD, measurements on matrices are performed.

In this thesis, examples of measurements performed at previous B factories and possible measurements at future SuperB factories are introduced and the requirements for a B factory are elaborated. The next chapter gives an overview over the SuperKEKB accelerator and the Belle II experiment which is currently built in Japan. The fourth chapter introduces the DEPFET technology and the pixel modules for the Belle II pixel detector. The next chapter gives an in-depth look into two of the **A**pplication **S**pecific **I**ntegrated **C**ircuits (ASICs) used to read out the DEPFET sensor in Belle II. It further goes into details about the prototype test systems used to investigate these and gives a short overview about the work done as part of this thesis. Chapter six discusses measurements on the DCD, its optimization and investigations on

radiation hardness and temperature stability. It further presents measurements performed to find issues with data communication between DCD and DHP. In the next chapter, the optimized DCD settings are used to optimize the first full scale Belle II prototype and to run it during beam test. In chapter eight, results of the first large DEPFET matrix are shown which are read out using Belle II back end electronic. Optimal operation parameters were determined using both high resolution laser measurements as well as in pixel resolved beam test measurements. Also, in this chapter, the pedestal compensation algorithm is introduced and an investigation of the needed dynamic range of the DCD and the strength of its (**D**igital to **A**nalog **C**onverters) DACs is performed.

CHAPTER 2

Physics Motivation

2.1 The Standard Model

Nature shows the existence of four fundamental forces: Gravitation, which acts on mass and (described by Einstein's famous formula $E = mc^2$) energy, the electromagnetic force acts on electric charge, the weak force which acts on flavor and the strong force which acts on a color charge. The electromagnetic and weak force can be unified to the electroweak force.

The SM of elementary particles describes the known particles and their electromagnetic, strong and weak interactions. Gravitation is not described by the SM. Since gravitation acts on all particles it is omitted when describing which forces act on which particle.

All particles have a property called spin. Particles with half integer spin (1/2) are called fermions and make up all matter, particles with whole number spin (0,1) are called bosons. Bosons can be separated in force carriers with spin 1 and the spin 0 Higgs boson.

2.1.1 Fermions

The SM describes 12 fermions and their antiparticles which make up all matter. Like shown in figure 2.1, six quark flavors exist: Down (d), up (u) , strange (s), charm (c), bottom (b) and top (t) . Quarks have mass, carry color charge, electric charge and flavor, thus they interact via the strong, electromagnetic and weak forces. They are ordered in two types: up type quarks (u, c, t) with an electric charge of $2/3\,e$ and down type quarks (d, s, b) with an electric charge of $-1/3\,e$. Three generations of quarks exist, each generation is heavier than the previous, thus only generation 1 is stable and the third generation b-quark is instable. Antiquarks have opposite charge and flavor quantum numbers. Each quark carries a color, either red, green or blue. Antiquarks carry anti-colors (anti-red, anti-green, anti-blue). Particles created from quarks (baryons, which are made of 3 quarks, mesons which are made from 2 quarks) need to have neutral color, either having one of each color or a color - anti-color pair. The other 6 fermions are leptons, forming 3 generations: electronic leptons (electrons e^-, electron neutrinos ν_e), muonic leptons (muons μ^-, muon neutrinos, ν_μ) and tauonic leptons (taus τ^-, tau neutrinos, ν_μ). Leptons have no color charge, so the strong force does not affect them. e, μ^- and τ^- have electronic charge and flavor, thus they interact via electromagnetic and weak force. Neutrinos have no charge and only interact via weak force. All leptons have mass, though neutrinos should be massless according to the SM. Experimentally, neutrino oscillations can be observed [4], which require neutrinos to have a mass > 0. Currently, only upper limits of the neutrino mass are known.

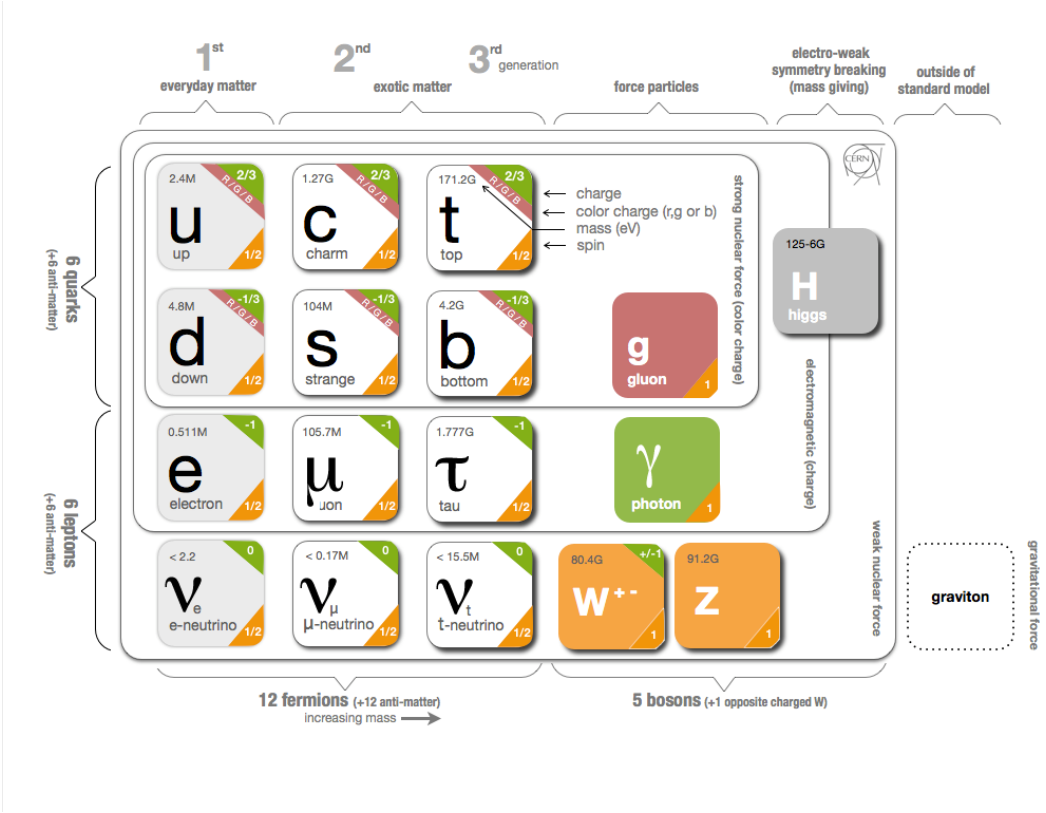


Figure 2.1: Info graphic of the SM particles. From [10]

2.1.2 Bosons

Spin 1 (gauge/vector) bosons act as force carriers in the SM. The neutral photon mediates electromagnetic force. The $W^{\pm}$ and Z boson mediate the weak force. They are massive, both $W^{\pm}$ carry charge and thus couple to the electromagnetic interaction. The strong force is mediated by gluons. Gluons are massless[1], electromagnetic neutral and carry color charge, thus they couple to the strong interaction.

In 2012 the scalar (spin 0) Higgs Boson was discovered at CERN. It is a result of the Higgs mechanism which breaks symmetry between electromagnetic and weak force and gives mass to leptons, quarks and the $W^{\pm}$, Z and Higgs Boson [2].

2.1.3 Symmetries of the Standard Model

The SM is a renormalizable local gauge invariant quantum field theory. It's symmetry group is SU(2) x U(1) x SU(3), where SU(2) x U(1) correspond to the symmetry group of the electroweak force. The SU(2) is the generator of 3 bosons mediating the weak force, U(1) is the generator of the photon mediating the electromagnetic force. SU(3) in the SM corresponds to the strong force described by **Q**uantum **C**hromo **D**ynamics (QCD) and results in 8 gluons.

The SM is CPT symmetric [12]. This means that a physical process which is charge reversed (i.e. particles are replaced by their antiparticles, C), has all momenta and spins reversed (Time reversal, T)

[1] The standard model predicts a gluon mass of $m_g = 0$, current measurements show an upper limit of the gluon mass of $m_g < O(1\,\text{MeV}$ [11]

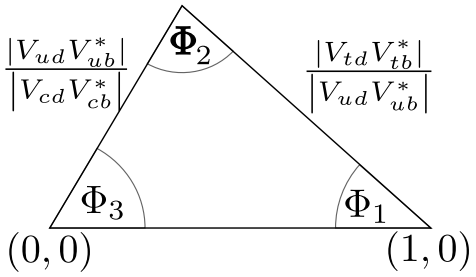


Figure 2.2: CKM unitary triangle: Two sides and three angles of this triangle can be determined by measurements, over constraining it. This allows to test the CKM formalism.

and has its position mirrored at an arbitrary plane (Parity transformation, P) will follow the same physical rules. Parity is a symmetry for both strong and electromagnetic interactions but is violated in weak interactions, which was shown in the Wu experiment (1957) [13].

CP violation was first measured in the Kaon system [14]. CP violation describes that weak interactions of particles can differ from the interactions of their antimatter particles. This is an important point to describe the imbalance between matter and anti-matter in the observed universe. As with Parity, CP is a symmetry for the electromagnetic and strong interactions[2] but is violated for weak interactions. Kobayashi and Maskawa proposed in 1973, that CP violation could be explained if (at least) three quark generations exist [17]. Thus, CP violation was predicting a third generation of quarks, 4 years before the bottom quark was experimentally discovered (1977) [18] and 22 years before the top quark was found [19]

2.1.4 CKM Matrix and Unitary Triangle

Flavor changes by the weak interactions are represented by the unitary Cabibbo-Kobayashi-Maskawa matrix:

$$\begin{bmatrix} d' \\ s' \\ b' \end{bmatrix} = \begin{bmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{bmatrix} \begin{bmatrix} d \\ s \\ b \end{bmatrix} \tag{2.1}$$

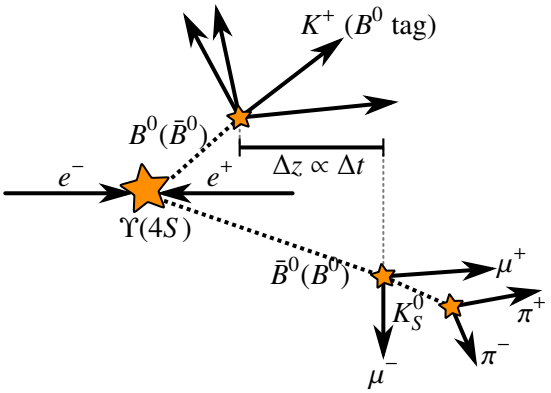
where $|V_{ij}|^2$ is the transition probability of quark i to quark j. The CKM matrix can be represented as 3 rotation matrices U_{12}, U_{13}, U_{23} and one complex phase matrix U_δ which generates CP violation:

$$\begin{aligned} U_{12} &= \begin{bmatrix} c_{12} & s_{12} & 0 \\ -s_{12} & c_{12} & 0 \\ 0 & 0 & 1 \end{bmatrix}; \quad U_{13} = \begin{bmatrix} c_{13} & 0 & s_{13} \\ 0 & 1 & 0 \\ -s_{13} & 0 & c_{13} \end{bmatrix}; \\ U_{23} &= \begin{bmatrix} 1 & 0 & 0 \\ 0 & c_{23} & s_{23} \\ 0 & -s_{23} & c_{23} \end{bmatrix}; \quad U_\delta = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & e^{-i\delta} \end{bmatrix}. \end{aligned} \tag{2.2}$$

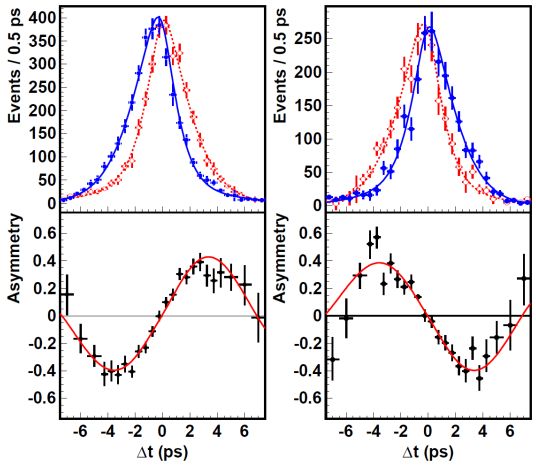
Here, c_{ij} and s_{ij} are $\cos\phi_{ij}$ and $\sin\phi_{ij}$, with mixing angle ϕ_{ij} between quark generation i and j and a complex phase δ. Using this representation, the CKM matrix can be written as

$$V_{CKM} = U_{23}U_\delta^\dagger U_{13}U_\delta U_{12} \tag{2.3}$$

[2] The SM allows, but doesn't require CP symmetry in the strong interactions. Strong CP violation has not been observed, other parameters of the SM suggest that it is strongly suppressed [15, 16]



(a) Example for a CP violating process: A $\Upsilon(4S)$ is created by ane^+e^- collision. It is decaying into a $B^0\bar{B}^0$ pair. Measuring a K^+ allows to tag one of the mesons as B^0, thus the flavor of the second meson is known. Here the second meson decays into a CP eigenstate. Since the $\Upsilon(4S)$ was created with a boost, the lifetime of the B mesons translates into a displacement of the secondary vertex, which allows the measurement of lifetime differences.



(b) Belle result for $\sin 2\Phi_1$: The *top* plots show the number of reconstructed events with good tag quality after subtraction of background for B^0 (red) and $\bar{B}^0$ (blue). The *bottom* plots show the asymmetry[a] of both distributions. The *left* plots corresponds to CP-odd modes, including the one described int the text. The *right* plots show the result for CP-even modes $B^0 \to J/\psi K^0_L$ and $\bar{B}^0 \to J/\psi K^0_L$ [5]

[a] The asymmetry is defined as ${}^{N_+-N_-}/_{N_++N_-}$ where $N_+(N_-)$ is the signal at each bin for $q = +1(-1)$

Figure 2.3: Measurement of CP asymmetry between $B^0 \to J/\psi K^0_S$ and $\bar{B}^0 \to J/\psi K^0_S$

Since the matrix is unitary, six independent equations can be written: $\sum_k V_{ik}V^*_{jk} = 0$ for all $i, j \in \{u, c, t\}, i \neq j$ and $\sum_k V_{ki}V^*_{kj} = 0$ for all $i, j \in \{d, s, b\}, i \neq j$. Each of this 6 equations represents a triangle in the complex plane. 4 of the triangles have large differences between largest and smallest element (i.e. longest and shortest side), thus at least one angle would be close to 0, amplifying measurement uncertainties and making it hard to over constrain the triangle.

B physics is a subset of flavor physics which studies weak interactions of b quarks. For this, $V_{ud}V^*_{ub} + V_{cd}V^*_{cb} + V_{td}V^*_{tb} = 0$ is chosen, since its sides are of similar length[3] and all terms contain the coupling to a b quark. The triangle is normalized to the side $V_{cd}V^*_{cb}$, called "the" unitary triangle (of b physics) and shown in figure 2.2. The triangle is fully characterized by two sides (with the third of length 1). It also can be characterized by its angles which are defined as

$$\Phi_1 \equiv \arg \frac{-V_{cd}V^*_{cb}}{V_{td}V^*_{tb}} \quad \Phi_2 \equiv \arg \frac{-V_{td}V^*_{tb}}{V_{ud}V^*_{ub}} \quad \Phi_3 \equiv \arg \frac{-V_{ud}V^*_{ub}}{V_{cd}V^*_{cb}}. \tag{2.4}$$

Thus the unitary triangle is over constraint and measurements of its angles and sides can hint to tensions of the CKM matrix and thus to physics beyond the SM.

2.2 Main Historical Achievements of B factories

B factories are specialized accelerators running at the center of mass energy of the $\Upsilon(4S)$ (10.58 GeV). The $\Upsilon(4S)$ mass is just above the production threshold of a $B\bar{B}$ meson pair. B mesons have a wide decay spectrum, including many rare decays which couple to off-diagonal elements of the CKM matrix, thus allowing measurements of CKM constants. The two major B factories were the PEP-II collider using the BaBar detector which was taking data form 1999 to 2008 and the KEKB collider using the Belle detector for data taking from 1999 to 2010. One of their many results was a measurement of the $\sin 2\Phi_1$. This is (in part) achieved by measuring the CP asymmetry between $B^0 \to J/\psi K_S^0$ and $\bar{B}^0 \to J/\psi K_S^0$ which is shown in figure 2.3(a): The $B\bar{B}$ pair produced by the $\Upsilon(4S)$ is a P-wave entangled state. If the earlier decaying meson decays into a flavor specific eigenstate, the flavor of the second meson can be determined to be the opposite. This is called "flavor-tagging". Propagating in time, the second meson's quark content can oscillate from an unmixed into a mixed state. If the particle decays into a CP eigenstate, mixed and unmixed phase interfere constructive for B^0 and destructive for $\bar{B}^0$. If the flavor-tagging process happens after the second meson decayed, the interference of mixed and unmixed phase is inversed. In this case the interference is destructive for B^0 and constructive for $\bar{B}^0$. This result is shown in figure 2.3(b), where a time dependent asymmetry between B^0 and $\bar{B}^0$ can be observed. The x axis shows the time difference $\Delta t = t_2 - t_1$, where t_1 is time when the flavor tagged B decays and t_2 is the time when the second B decays into the CP eigenstate. This directly shows the presence of CP violation outside the kaon system. To measure this and similar processes, B factories needed to fulfill several requirements:

- Δt is too short to be measured directly. It can be measured by using asymmetric beam energies, resulting in a boosted reference frame. Thus, Δt is translated into a decay vertex difference $\Delta z = \beta\gamma c\Delta t$, where $\beta\gamma$ is the boost of the reference frame and c is the speed of light. Since Δz is small (100 µm), a high vertex resolution is required.

- Several decays involved in this (and other) measurement have a small branching fraction, so a large $B\bar{B}$ sample is required. High luminosity is needed to achieve large enough statistics in a reasonable time.

With the given data from B factories, it could be shown that the CKM model fits within the SM. The experimental confirmation of the Cabibbo-Kobayashi-Maskawa mechanism was one part which lead to the Nobel prize for Kobayashi and Maskawa in 2008.

2.3 Limits of the Standard Model

The SM is extremely successful in describing interactions between particles at small scales but has some unsolved issues:

- Gravitation is not described by the SM.

- General relativity seems not to be compatible with the SM.

- Dark energy and dark matter make up 95 percent of the observable universe but are not described by the SM [3].

[3] Using the Wolfenstein representation it can be shown that the other triangle ($V_{ud}V_{td}^* + V_{us}V_{ts}^* + V_{ub}V_{tb}^* = 0$) results in identical equations up to terms of $(\sin\phi_{12})^5$

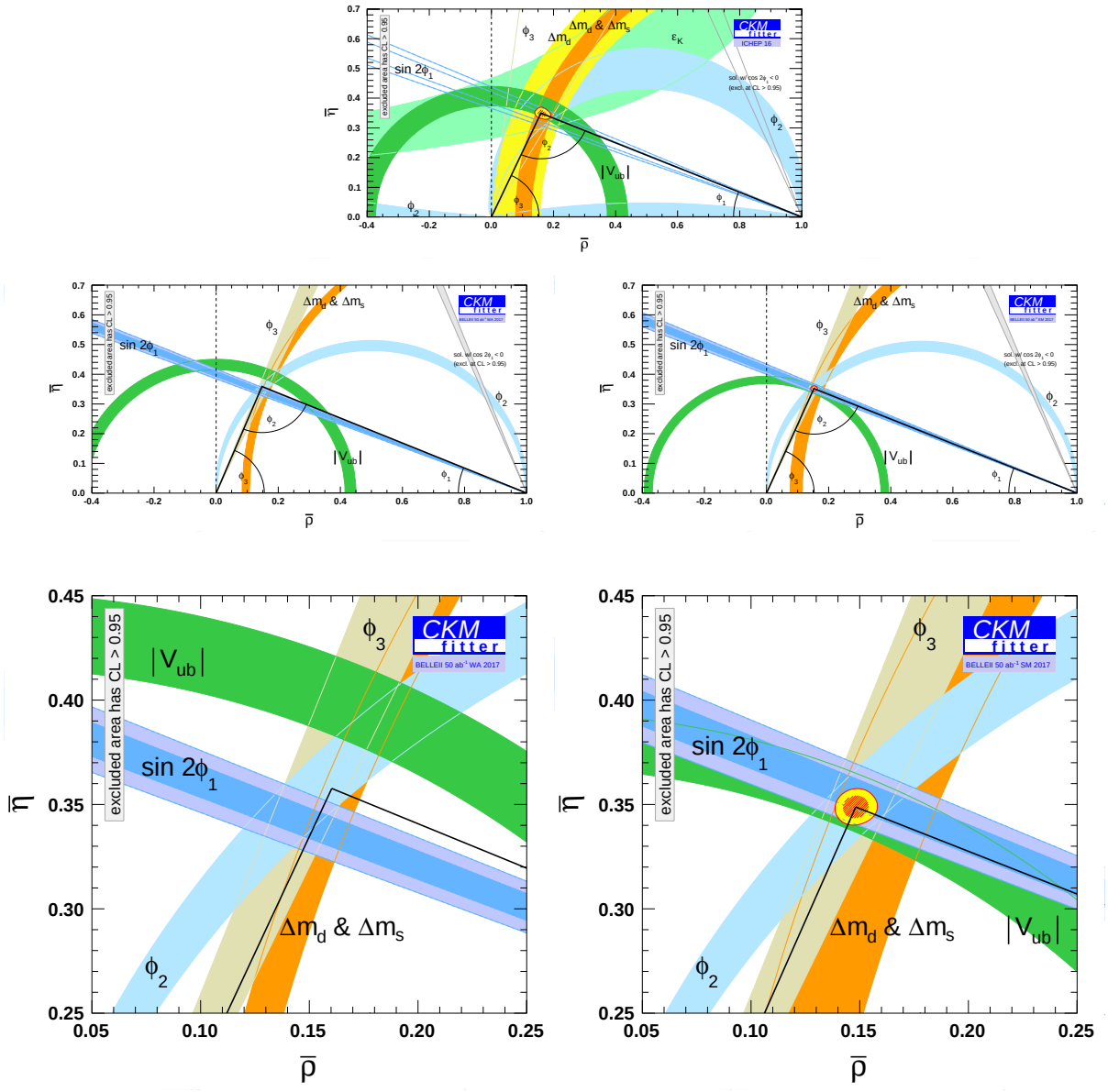


Figure 2.4: Measurements of the CKM parameters: The point of the Unitarity Triangle where Φ_2 is located can be parametrized by two variables, $\bar{\rho}, \bar{\nu}$. Together with (0,0) and (1,0) $(\bar{\rho}, \bar{\nu})$ completely describes the triangle. Different measurements (colored bands) exclude parts of the parameter space. *top*: Currently, all measurements agree within their uncertainty, resulting in an overlap and values for $\bar{\rho}, \bar{\nu}$ shown by the red-yellow area. *right*: Projection for $50\,\mathrm{ab}^{-1}$ assuming SM compatible central values. *left*: Projection for $50\,\mathrm{ab}^{-1}$ assuming the current world average of the individual measurements, with reduced uncertainties. This would result in a disagreement with the SM. *left and right*: Projections only show measurements, where Belle II is expected to result in comparable or higher precision than other measurements. The bottom plots are zoomed in versions of the above. From [20].

- The observed matter/antimatter asymmetry is many orders of magnitude larger than can be explained with CP violation.

To answer these questions, measurements are needed to test the SM parameters and hint towards physics beyond it. Tests can be done using three different approaches: The cosmic approach measures spectra and rates of cosmic particles and searches for dark matter and dark energy, with experiments like Super-Kamiokande or IceCube. The high energy approach tries to find deviations from SM predictions at highest possible energies. This is done at CERN using proton-proton collisions at of 14 TeV. At these high energies, new particles can be produced directly, as seen in the Higgs discovery. The third way is the precision measurements of known interactions to observe higher order effects which might deviate from the SM expectations. The Belle II experiment described in this thesis is an example for a precision measurement.

2.4 Possible Measurements at SuperB factories

The unitary triangle is constrained by several measurements. This is shown on the figure 2.4 *top*, where confidence bands of several measurements are shown for the unitary triangle. The current results are all in agreement with the standard model, though there are some tensions, like a 3σ difference between inclusive[4] and exclusive[5] $|V_{ub}|$ measurements [21, 22]. Using higher statistics from a SuperB factory (and better systematics) the confidence bands will get smaller. Two scenarios are shown:

- Using the current world averages of individual measurements (2016) would result in figure 2.4 *left*. With this precision, currently invisible disagreements between measurements are significant and hint towards physics beyond the SM.
- Using SM compatible values would result in figure 2.4 *right*.

More detailed information on this topic can be found in [20]. A possible deviation from SM prediction is observed in $R(D)$, $R(D^*)$, with

$$R(D^{(*)}) = \frac{\mathcal{B}(\bar{B} \to D^{(*)}\tau\bar{\nu}_\tau)}{\mathcal{B}(\bar{B} \to D^{(*)}\ell\bar{\nu}_\ell)}, \ell = e, \mu,$$

which is the ratio of branching fractions of $\bar{B}$ to $D^{(*)}$ with a tau in the final state vs a electron or muon in the final state. Figure 2.5 shows combined measurement results with a 4σ difference between SM predictions and the current world average. Higher statistics would reduce the statistical uncertainty of the measured values for $R(D)$ and $R(D^*)$, possibly showing a disagreement and hinting towards physics beyond the standard model.

Apart from CKM measurements, the rich decay spectrum of B mesons makes the measurement of several rare decays possible, which can be used for further precision measurements in the SM. One example for these kinds of measurements is the branching ratio measurement $\mathcal{B}(B \to \tau\nu)$. In the SM this decay is mediated by a W^+. Certain SM extensions would allow other particles, for example a hypothetical charged Higgs Boson, to modify the branching ratio, thus a precise measurement of the branching fraction has a high sensitivity for new physics [24]. For this decay, only a single charged track

[4] An inclusive measurement determines a CKM matrix parameter by measuring the differential branching fraction over all decays containing the quark level transition mediated by the parameter

[5] An exclusive measurement determines a CKM matrix parameter by measuring the branching fraction of an specific decay

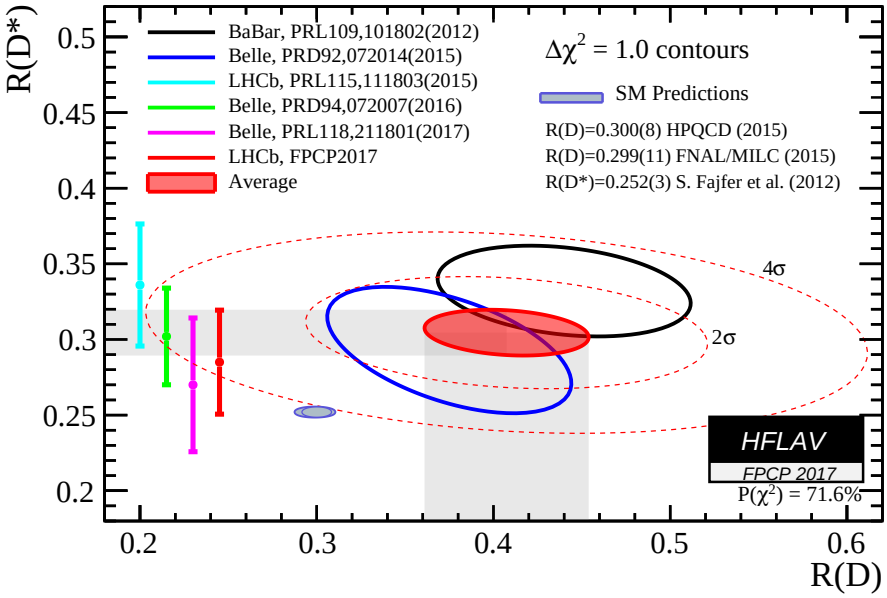


Figure 2.5: Measurements and theoretical prediction for $R(D)$, $R(D^*)$, from [23]

and missing energy from the neutrino are expected. Reconstructing these events requires a large coverage detector with a clean background, like a SuperB factory.

In addition to a significantly larger data set, a SuperB factory will feature an improved detector which will decrease systematic uncertainties due to better particle identification and better vertex separation, which will further reduce measurement uncertainties.

Further informations on possible measurements can be found in [20].

CHAPTER 3

A new SuperB Factory

The measurements described in the previous chapter need an order of magnitude larger data set. To acquire this amount of data in a reasonable time, a new collider is needed providing higher luminosity. This collider, SuperKEKB, will be described in the following chapter, the Belle II detector needed for recording the data is described in chapter 3.2.

3.1 SuperKEKB

The SuperKEKB collider is a so called SuperB factory, a collider specifically tailored to produce B-Mesons. It will run at 10.58 GeV, the center of mass energy of the $\Upsilon(4S)$, which decays almost exclusively into $B^0\bar{B}^0$ and B^+B^-, colliding e^+/e^- of 4 GeV and 7 GeV. Due to the asymmetric energies, the Y(4S) and its decay product will be boosted with $\beta = \frac{7\,\text{GeV}-4\,\text{GeV}}{10.58\,\text{GeV}} \approx 0.28$. This boost translates lifetime into distance from the primary vertex and allows the measurement of lifetime differences between both B mesons by spatially resolving their decay vertices's. SuperKEKB targets an instantaneous luminosity of $8 \times 10^{35}\ /\text{cm}^2/\ \text{sec}$, 40 times higher than the world record set by KEKB. The luminosity $\mathcal{L}$ of two colliding beams with Gaussian profiles is [25]

$$\mathcal{L} = \frac{N_1 N_2 f}{2\pi \sqrt{\sigma_{1x}^2 + \sigma_{2x}^2}\sqrt{\sigma_{1y}^2 + \sigma_{2y}^2}},$$

where N_1, N_2 are the particles per bunch of both beams, f is the bunch crossing frequency and σ_{1x}, σ_{1y}, σ_{2x}, σ_{2y} are the widths of the beam profile. An increase of luminosity can be achieved by increasing the beam current $N_{1/2}f$ or by decreasing the width of the beam. SuperKEKB will achieve the luminosity increase using twice higher beam currents and applying a nano-beam scheme where the beam is focused to a smaller area at the interaction point. During its lifetime it will produce an integrated luminosity of $50\,\text{ab}^{-1}$, almost a factor 50 higher than the $1.041\,\text{ab}^{-1}$ recorded by its predecessor [26]. Main differences to KEKB are

- New RF cavities and RF supplies which allow the usage of higher beam currents
- New final focusing magnets which can squeeze down the beam to $\sigma_y = 48\,\text{nm}/63\,\text{nm}$ and $\sigma_x = 10\,\mu\text{m}/10\,\mu\text{m}$ instead of $\sigma_y = 940\,\text{nm}/940\,\text{nm}$ and $\sigma_x = 147\,\mu\text{m}/170\,\mu\text{m}$ achieved at KEKB. This so called nano-beam scheme is the main source of the luminosity increase[7].

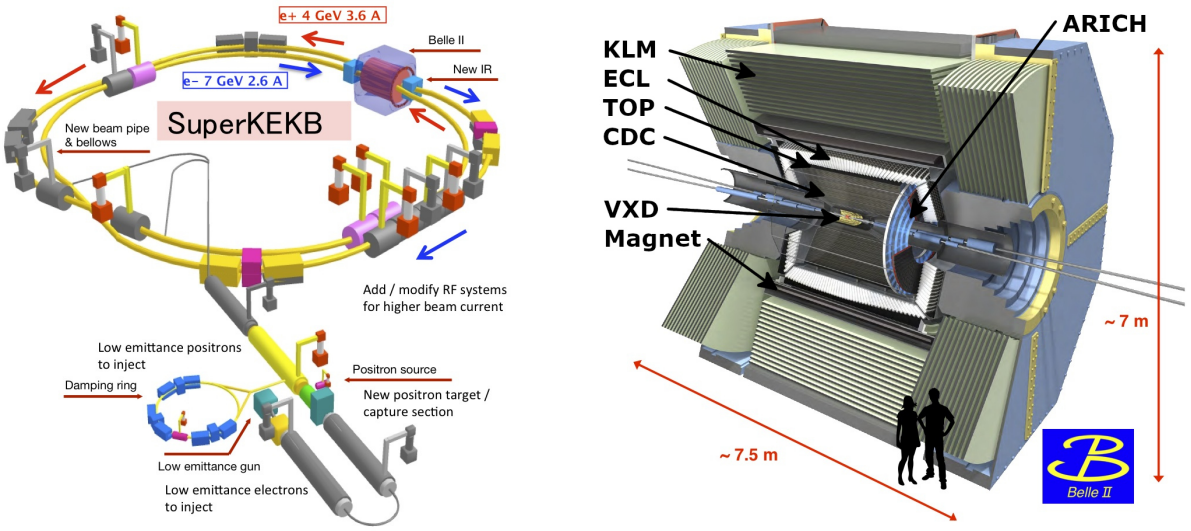


Figure 3.1: *Left:* Schematic of the SuperKEKB Accelerator. *right:* Schematic of the Belle II detector. The DEPFET Pixel detector is displayed in red in the center of the detector.

- A new beam pipe closer to the interaction point, which allows the first detector at lower radii, improving vertex resolution
- A boost reduced from $\beta = 0.425$ to $\beta \approx 0.28$ which requires an improved vertex resolution. The boost was reduced to decrease the expected background; one main background at SuperKEKB, synchrotron radiation, scales with $(\frac{E}{m})^4$, another background, Touschek scattering[1], with $\frac{N}{E^3\sigma}$, with beam width σ and the number of beam particles N [27]. Thus beams with less energy asymmetry will produce less background.

These changes will result in higher event and background rates. To cope with the new requirements an upgraded detector, called Belle II, is needed.

3.2 Belle II

Belle II will be a hermetic, onion like detector with an acceptance region of 17° to 150° in θ. Its purpose is to measure type, charge, energy and origin of particles produced in the interactions taking place in its center. The detector follows a typical design: The inner part of Belle II is within a magnetic field to bend the trajectories of the charged particles. The inner detectors (VCD and CDC) measure the track of the charged particles, providing the particles momentum, its charge[2] and an estimate of its origin, which is described by the impact parameter. Going further outside, the next detector layer (TOP and ARICH) performs particle identification. This is achieved by measuring the Cherenkov angle and combining this measurement with with energy and impulse measurements from other layers. The next detector layer is the electromagnetic calorimeter (ECL) which provides an energy measurement for the particle. All

[1] Touschek scattering describes beam loss due to intra-bunch coulomb scattering. Collisions between particles in the same bunch can result in a large enough transversal energy for one particle to be kicked out of the bunch, which then will be lost due to collisions with the beam pipe or beam collimators

[2] To be precise: the sign of the charge

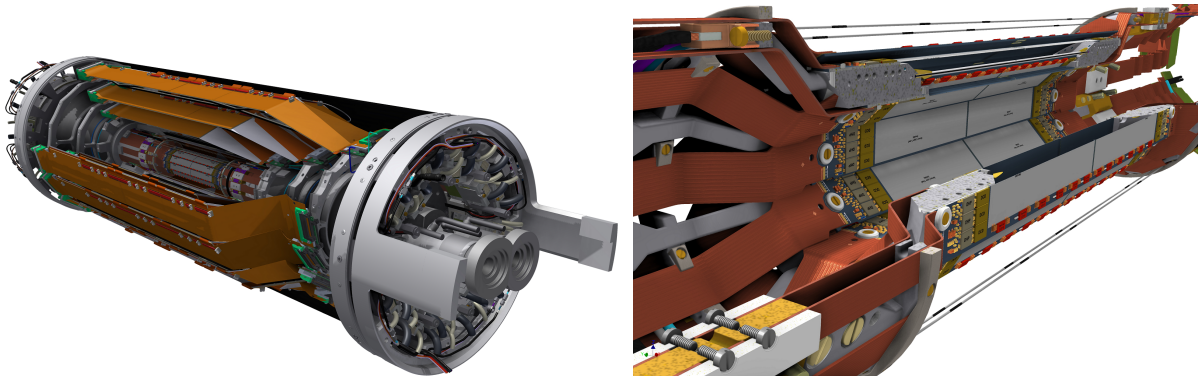


Figure 3.2: *Left:* CAD drawing of the VXD. 3 layer of SVD with slanted parts in the forward direction are visible, the innermost SVD layer is hidden behind the others. The PXD is visible in the center. *right:* CAD Drawing of the PXD. It consists of two layers, mounted back to back. Pictures from the Belle II Collaboration

previous systems are within a superconducting solenoid magnet, producing a field of 1.5 T. The last detector layer is the K_L and Muon System (KLM), which identifies both K_L and muons.

The impact parameter resolution of a detector is a measure of its capabilities to distinguish vertices. For a two layer detector with radii of r_1, r_2, point resolutions of σ_1, σ_2, the particle momentum p, the thickness x of the first layer in units of the radiation length X_0, the impact parameter resolution is [34]

$$\sigma_{d_0} \approx \sqrt{\frac{r_2^2\sigma_1^2 + r_1^2\sigma_2^2}{(r_2 - r_1)^2}} \oplus \frac{r}{p \sin^{\frac{3}{2}} \theta} 13.6\,\text{MeV} \sqrt{\frac{x}{X_0}}, \tag{3.1}$$

which is the convolution of two terms. The first term depends on the detector geometry and is the high momentum limit for the impact parameter resolution. Highest resolution is achieved, if the innermost layer is as close to the beampipe as possible. Since the collider will have a high luminosity and the number of particles is proportional to the inverse squared radius, the innermost detector layers need both high granularity and fast readout.

The second term of 3.1 depends on the energy of the particle and the material budget of the innermost detector layer and the beam pipe. It models measurement errors due to multiple scattering and limits the impact parameter resolution at low particle momenta. Belle II will measure B meson decays, the momentum distribution of the expected particles is mainly below 1 GeV c^{-1}. To achieve a good vertex resolution, the material used by the tracking detector has to me minimized.

The innermost detector in Belle II will be the **V**erte**X** **D**etector (VXD) which consists of 6 layers of silicon sensors. The innermost two layers are the **PiX**el **D**etector (PXD) which consist of thinned, all silicon DEPFET pixel modules. With radii of 1.4 cm and 2.2 cm it will be closest to the interaction point, face the highest particle flux and will have to cope with the highest radiation damage. It will feature 8 million pixel with a size between $50 \times 55\,\mu\text{m}^2$ and $50 \times 85\,\mu\text{m}^2$. Being thinned down to 75 µm, it will achieve an ultra low material budget of $0.2\,\%X_0$ per layer [28]. The Pixel detector will be described in more detail in chapter 4.

The next 4 layers form the **S**ilicon **V**ertex **D**etector (SVD), which is made of double-sided strip detectors. The P and the N side have strips along the z and $r - \phi$ direction which are read out by the APV25 ASIC [29]. Using an origami layout[3], all ASICs are on one side of the sensor which allows

[3] A way to connect strips from the backside of the sensor to ASICs mounted on the front side, which requires folding the flexible PCB around the sensor edge and over wire bonds

easier cooling [30] and a low material budget of 0.7 $\%X_0$. It features a strip pitch of 50–75 µm in $r-\phi$[4], 160–240 µm in z and a shaping time of 50 ns. Its fast data acquisition allows online tracking to extrapolate Regions Of Interest (ROI) on the PXD to reduce data by storing only pixel data from these ROIs. [31]

The next detector is the **C**entral **D**rift **C**hamber (CDC). It is a wire chamber filled with a low Z helium ethane gas mixture, spanning radii between 168 mm and 1 111 mm. It consists of 56,576 wires in 56 layers, providing momentum information for charged particles and dE/dx measurements for particle identification [32]. Compared to Belle, the new CDC offers a larger tracking volume, more layers and smaller azimuthal cell size close to interaction point, which allows to cope with the higher track density expected at Belle II.

Particle identification is performed using the Cherenkov effect: Particles passing through matter faster than the speed of light in the matter emit photons in a specific angle of $\cos\phi_C = \frac{1}{\beta n}$ with the particles speed $\beta = \frac{v}{c}$ and the refractive index of the medium n. Measuring the Cherenkov angle allows the determination of β, together with the impulse measured in the inner detectors, the particles mass (and thus its type) are estimated.

Particle identification in the barrel region is done by the **T**ime **O**f **P**ropagation detector (TOP). It consists of quartz bars with a high surface reflectivity and is read out at one end using segmented Micro Channel Photo Multiplier Tubes with a time resolution of less than 50 ps. With the intersection point and angle known (from CDC), the time of arrival of light can be used to calculate the Cherenkov angle. ([33] and [9], chapter 7)

In the forward end cap region, particle identification is done by the **A**erogel **R**ing **I**maging **CH**erenkov detector (ARICH). Particles traverse two layers of an aerogel radiator with different optical indices. Both produce Cherenkov rings which traverse an expansion region. The length of this region is chosen so that rings of both aerogels overlap at the readout plane, where they are measured by position sensitive Hybrid Avalanche Photo Diodes. From this, the Cherenkov angle can be computed. ([9], chapter 8)

The particle energy is measured in the **E**lectromagnetic **C**a**L**orimeter (ECL). It consists of CsI(TI) scintillator crystals, which are being read out by photomultiplier tubes. Due to the long radiation length of the material of 16.1 X_0, charged particles[5] create showers in the material and deposit all their energy which then is measured. The new ECL reuses crystals used at Belle, but features a new readout scheme (waveform sampling), which will allow it to cope with the higher particle rate at Belle II. ([9], chapter 9)

The outermost detector is the $\mathbf{K_L}$ and **M**uon system (KLM). It identifies muons which escape the detector and measures K_L, neutral particles which can be long-living enough to reach the KLM. The KLM in the barrel region reuses some Resistive Plate Chambers from Belle, but replaces the innermost two layers with scintillating strips which are read out by silicon photo multipliers. The KLM layers are interleaved with iron plates of the magnets return yoke. In the end cap region, only scintillating strips are used. The changes with respect to Belle are expected to reduce the efficiency loss when neutron background is present. ([9], chapter 10)

[4] Strip pitch in $r-\phi$ means that the strips are measuring the $r-\phi$ coordinate, while this strip has its long side in z direction

[5] with the exception of muons

CHAPTER 4

The DEPFET Pixel Detector

The PXD features two layers of all silicon, thinned DEPFET pixel detectors at radii of 1.4 cm and 2.2 cm respectively. At these radii, the PXD needs to cope with an occupancy of 0.4 hits $\mu m^{-2}\, s^{-1}$, ionizing radiation of 2 Mrad/year and a neutron flux of 2×10^{12} 1 MeVn_{eq} /yr, while providing a vertex resolution of 15 µm. A good impact point resolution for low momentum particles requires an ultra low material budget of 0.2 $\%X_0$ per layer - a mayor effort only achieved by thinning the active area, a readout scheme placing most of the readout outside of the acceptance region and using a self-supporting structure without any active cooling in the acceptance area. For Belle II, the inner layer will consist of eight, the outer layer of twelve ladders. Both ladder types are 15.4 mm wide, 2×67.975 mm (inner) / 2×84.975 mm (outer) long and consist of two modules glued together. Each module contains an active area with pixels realized in the DEPFET technology which is described in 4.1. The readout scheme of the pixels is described in 4.2. The layout and features of the modules will then be described in 4.3. At the end of this chapter, the back end electronics and services needed for PXD operation will be described.

4.1 The DEPFET Technology

A DEPFET (**DE**pleted **P**-channel **F**ield **E**ffect **T**ransistor) is a modified P-FET (**P**-channel **F**ield **E**ffect **T**ransistor). A P-FET is a four terminal device (source, drain, gate, bulk) where a current between source and drain can be controlled using the gate potential. The substrate of the transistor needs to be at least as positive as source or drain, so the bulk terminal needs to be connected to a positive voltage[1]. If the Gate-Source Voltage (V_{GS}) is smaller than the threshold voltage (V_{th}) of the P-FET, a channel can be formed between Source and Drain so that the device is conducting. There are two operation regions, depending on the Drain-Source Voltage (V_{DS}), V_{GS} and V_{th} which are shown in figure 4.1.

Using the oxide sheet capacitance C_{ox}, the width W and length L of the transistor gate and the charge carrier mobility μ_p, the drain current I_D flowing through the transistor can be calculated:

- $V_{DS} > (V_{GS} - V_{th})$: In the linear region, I_D is linear to V_{GS}:

$$I_D = -\mu_p C_{ox} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right).$$

  In first order the P-FET behaves like a resistor whose resistivity can be changed by V_{GS}.

[1] On most FETs, bulk is connected to source, so they appear as three terminal device and feature a parasitic diode.

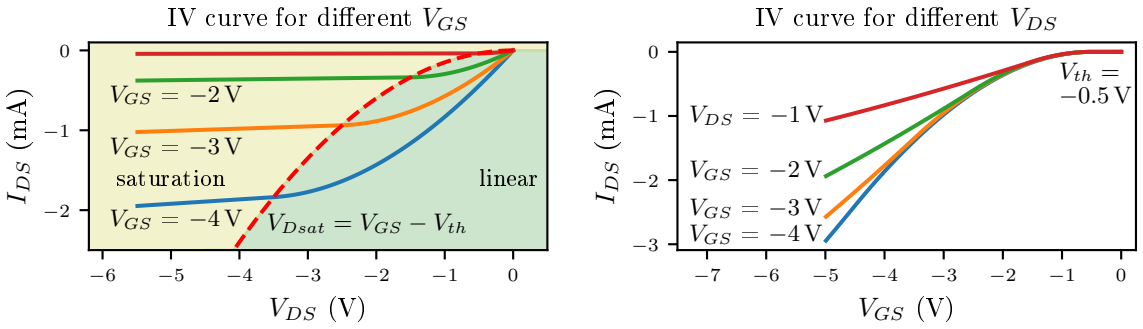


Figure 4.1: IV curve of a FET for different V_{DS} and V_{GS}

- $V_{DS} \leq (V_{GS} - V_{th})$: In the saturation region, I_D is almost independent of V_{DS}:

$$I_D = -\frac{\mu_p C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2 (1 + \lambda (V_{Dsat} - V_{DS})).$$

In first order the P-FET behaves like a voltage controlled current source with the gain

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = -\mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{th})(1 + \lambda (V_{Dsat} - V_{DS})).$$

The $\lambda(V_{Dsat} - V_{DS})$ term is due to an effect called channel length modulation with $V_{Dsat} = V_{GS} - V_{th}$, which models the influence of the drain voltage on the channel near the drain implant.

4.1.1 Charge Collection and Internal Amplification

A DEPFET is a P-FET on a fully depleted n-doped substrate. As depicted in figure 4.2 it features an additional n implementation directly beneath the channel, the so called internal gate. The internal gate is a potential minimum for electrons and thus attracts charge. A charge q_s in the internal gate induces a mirror charge αq_s in the channel ($\alpha < 1$ due to stray capacitance), which modulates the gate potential by $\Delta V = \frac{\alpha q}{C} = \frac{\alpha q_s}{C_{ox} WL}$. The DEPFET is operated in saturation region; the drain current through the transistor gets modified to

$$I_D = -\frac{W}{2L}\mu_p C_{ox}\left(V_{GS} + \frac{\alpha q_s}{C_{ox} WL} - V_{th}\right)^2 (1 + \lambda (V_{Dsat} - V_{DS})) \tag{4.1}$$

Defining the internal charge amplification $g_q = \frac{\partial I_D}{\partial q_s}$ yields

$$\begin{aligned} g_q = \frac{\partial I_D}{\partial q_s} &= -\frac{\alpha \mu_p}{L^2}\left(V_{GS} + \frac{\alpha q_s}{C_{ox} WL} - V_{th}\right)(1 + \lambda (V_{Dsat} - V_{DS})) \\ &= -\alpha \sqrt{2\frac{I_D \mu}{L^3 W C_{ox}}(1 + \lambda (V_{Dsat} - V_{DS}))} \\ g_q &= \alpha \frac{g_m}{WLC_{ox}} = \alpha \frac{g_m}{C}, \end{aligned} \tag{4.2}$$

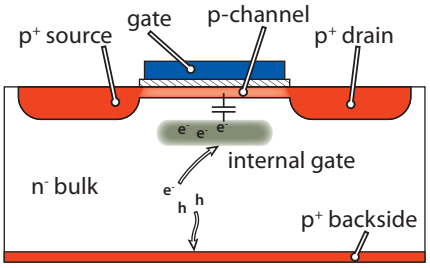


Figure 4.2: Sketch of a DEPFET pixel cell, cut along the transistor channel. Current from a P-FET is modulated by charge in the internal gate. Picture from [34].

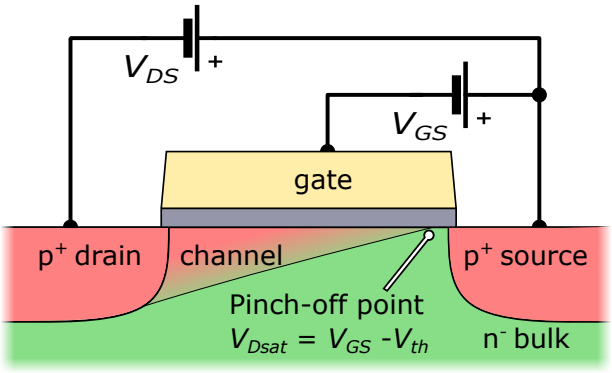


Figure 4.3: Sketch of a pFET channel with pinch off. In saturation, $V_{DS} \leq V_{GS} - V_{th}$ results in part of the channel not being formed. This is called pinch off. Thus, the voltage drop over the channel is limited to $V_{Dsat} = V_{GS} - V_{th}$.

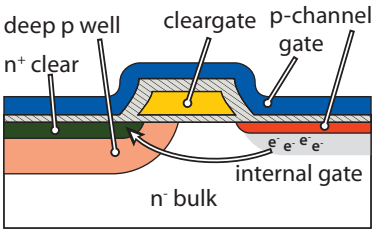


Figure 4.4: Sketch of a DEPFET pixel cell, cut perpendicular to the transistor channel. Charge can be removed from the internal gate applying a high potential to a nearby clear contact. During normal operation, the clear contact is shielded from the sensor by a deep p well, so that the internal gate is the implantation most attractive to electrons. Picture from [34].

where C is the capacity of the gate. This allows the measurement of charge stored in the internal gate by measuring the drain current. The above equations are a simplified model of the DEPFET. $V_{GS} - V_{th}$ changes the current in a saturated MOSFET quadratically. This is due to two linear effects: The charge density in the channel is linear to $V_{GS} - V_{th}$. The pinch off point, like shown in figure 4.3 limits the voltage drop over the channel to $V_{Dsat} = V_{GS} - V_{th}$, resulting in the above formula for I_D. The internal gate of the DEPFET is small and located in the middle of the channel. It has a very limited influence on the pinch off point of the channel. Thus, a change in charge is expected to result in a linear change of I_D. For this thesis, the equation 4.2 is a good estimation, as changes expected from $\frac{\alpha q_m}{C_{ox} WL}$ are small enough that the quadratic contribution in the above equation are smaller than 2 % even for the largest used signals.

The readout of a DEPFET is a non destructive process; charge in the internal gate stays there after readout. Since charge is constantly created both by ionizing radiation and by leakage current, the internal gate would run full after some time, making the sensor insensitive ([35], Chapter 6.5). To avoid this, the DEPFET is cleared repeatedly. This is done by an additional clear contact on which a high positive voltage is applied. Since the clear contact itself is a $n+$ contact, it would attract electrons like the internal gate, leading to signal loss. To prevent this, the clear contact sits in a deep p-well. During integration phase of the DEPFET, the clear voltage is lowered, so that all charge can reach the internal gate. For clearing, a high voltage pulse is applied and charge is removed by a punch through mechanism. The internal gate and the clear contact are the source and drain of a parasitic nMOS transistor with the deep

p-well as the bulk. Punch through is an extreme case of channel length modulation where the depletion layer around the source and drain merge into a single depletion region- This allows charge to be removed from the internal gate through the deep *p*-well into the clear contact. The voltage needed for this can be reduced by controlling the surface potential of the parasitic nMOS transistor. This is achieved by a cleargate structure between the clear implantation and the internal gate like shown in figure 4.4. Both the *clear low* and the *cleargate* potential have to be carefully adjusted, which was one part of this thesis. In previous DEPFET sensors, different *cleargate* mechanisms have been implemented, including actively switched *cleargate* potentials and dedicated structures for capacitive coupling the *cleargate* to the clear voltage and using a constant *cleargate* potential. DEPFETs for Belle II use a *cleargate* which capacitively couples to the clear voltage. This is achieved by parasitic capacitive coupling without dedicated structures, which limits the coupling strength between *cleargate* and clear. With dedicated structures, the coupling between *cleargate* and clear potential is about 50 %, with parasitic coupling it is about 30 % [36]. This is sufficient since in the linear transistor layout used for Belle II, the internal gate is small and has large clear implantations on both sides, yielding good intrinsic clear properties[2].

In this thesis, two different sensors were used; a small sensor with parasitic capacitive coupling and a large sensor with dedicated coupling structures.

4.1.2 Sensor Depletion

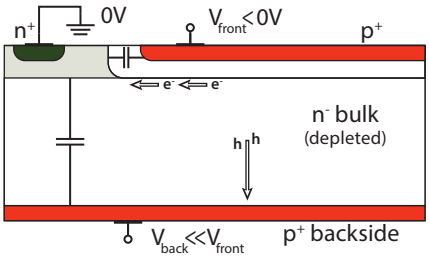


Figure 4.5: Principle of sidewards depletion. The sensor volume is depleted from a negative contact on top and bottom side. Using V_{front} and V_{back}, the depth of the potential minimum can be set. Electron-hole pairs created in the sensor bulk will be separated by the electric field. Holes will drift to the backside implantation (or the frontside implantation). Electrons will drift to the potential minimum and from there to the side contact. Picture from [34], modified.

The silicon substrate of the sensor is depleted using sidewards depletion. A negative potential is applied from both front side implantation (potential V_{front}) and backside implantation (potential V_{back}) and a positive potential V_{Bulk} is applied from an implantation at the side of the silicon as depicted in figure 4.5. The silicon substrate is depleted from both sides and when being fully depleted, a potential minimum is formed. Electron-hole pairs produced in the volume will get separated, holes will drift towards the backside/frontside implantation, while electrons produced in the substrate will drift towards the potential minimum and then diffuse along the minimum until they get close to the bulk contact. The depth of the potential minimum can be chosen by varying V_{front} and V_{back}.

The DEPFET has different *p+* implantations on the front side, which are connected to different voltages, so the depth of the potential minimum is different depending on the position within the pixel. Front side depletion voltages in the DEPFET are *source*, *drain* and *drift*, the backside is depleted by the *depletion* implantation. Though the DEFPET features a bulk contact, during normal operation charge will travel to the internal gate. The internal gate is cleared repeatedly using a high positive voltage, leaving it with a higher (more positive) potential than the external gate, which needs to be active during this process. When switched to its "off" state, the external gate is more positive than the *source* potential, pulling the capacitively coupled internal gate with it and leaving the internal gate several volts above *source*. During the integration phase, the internal gate will be the most positive point in the pixel and

[2] Circular DEPFET transistors are typically used for spectroscopy applications, where both speed and position resolution are of less importance. In these detectors, the gate forms a ring with the clear contact at one point.

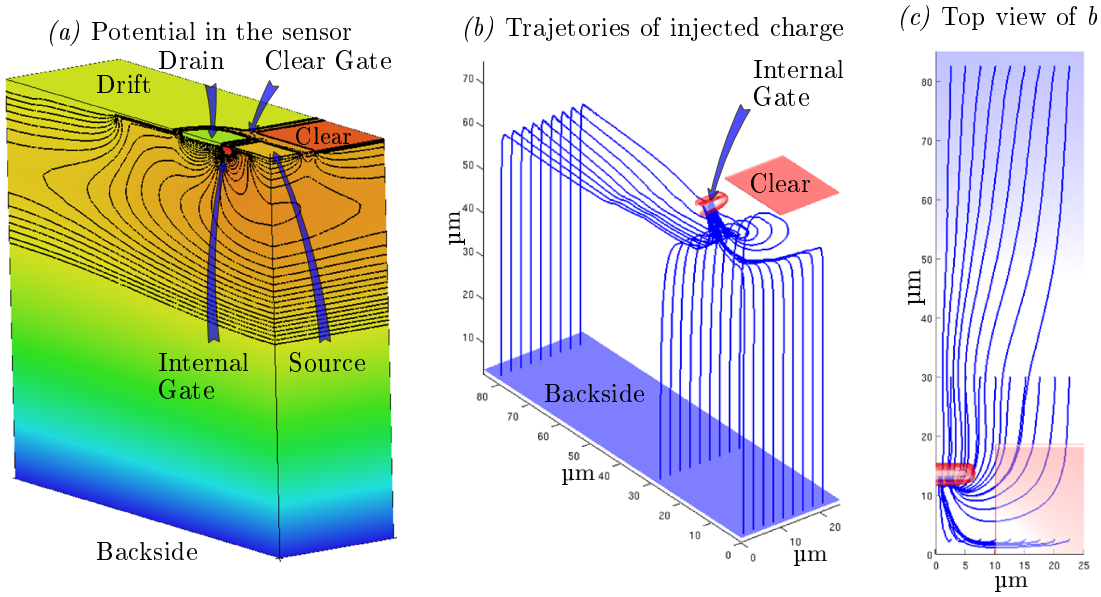


Figure 4.6: *(a)* 3D simulation of potential in the DEPFET for a 75 µm thick sensor. Pixels have a symmetry axis perpendicular to the gate, in this direction half a pixel is shown. *(b)* and *(c)* Charge transport in a DEPFET for different for different injection positions. From [36], calculated with WIAS-Oskar3.

collect charge. If the system is not repeatedly cleared, the internal gate will run full and charge will be lost, typically through the parasitic diode between internal gate and source [36].

Figure 4.6 *(a)* shows the potential in the DEPFET during charge collection. The sensor volume is cut perpendicular to the gate and along the pixel borders, the potential is shown both by color and equipotential lines. Figure *(b)* and *(c)* show the simulated trajectories of electrons which were injected at different positions on the backside. This was performed for final Belle 2 pixel layouts. Charge first drifts towards a layer approximately 10 µm below the sensor surface, then it drifts laterally towards the internal gate, albeit not always on a direct path. Charge can drift below the $n+$ clear implant since the clear implant is shielded by a deep p-well. Directly below the internal gate, charge drifts horizontal again into the internal gate.

4.1.3 Pixel Readout

The equivalent circuit of a DEPFET transistor is shown in figure 4.7. It is a five terminal device, three for readout, two for clear. The charge in the internal gate can be determined by measuring the voltage of the source follower configuration or by measuring the drain current directly.

- In the source follower configuration, which is shown in the middle of figure 4.7, a known (constant) current is forced through the DEPFET and V_{DS} is measured. This has the advantage that threshold voltage differences between DEPFETs change the voltage linearly. The settling time of this operation strongly depends on the load capacitance C_L of the source line. Using the small signal model of a source follower, the rise time t_r can be calculated as [37]:

$$t_r = \frac{2.2}{g_m}\left(C_L(1 + \frac{C_{GS}}{C_{GD}}) + C_{GS}\right) \tag{4.3}$$

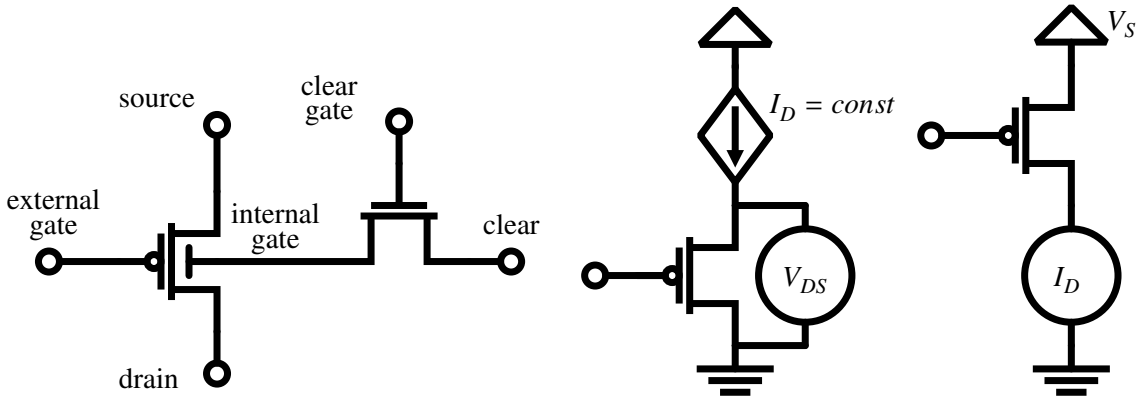


Figure 4.7: *Left*: Equivalent circuit of a single DEPFET transistor. *Middle*: Source follower readout of a transistor. *Right*: Drain current readout of a transistor.

with Gate Drain capacitance C_{GD} and Gate Source capacitance C_{GS}. For a realistic matrix setup this can reach several microseconds, which is at least an order of magnitude too slow for a high speed pixel detector needed for Belle II, where 100 ns have to be achieved.

- The drain based readout directly measures I_D while the source is connected to a constant voltage and the drain voltage is held constant by a readout ASIC, so that the line stays at a constant potential and the line capacity can be (ideally) neglected for readout speed. This is shown on the right of figure 4.7, A disadvantage of this readout is the quadratic dependence of I_D on the threshold voltage. Ionizing radiation changes V_{th} of MOS structures. Thus, threshold voltage inhomogeneities due to production spread and irradiation will result in large I_D inhomogeneities and measures to cope with this have to be used.

For Belle II, drain based readout is chosen. The current of a DEPFET can be sampled using correlated double sampling and single sampling.

- Correlated double sampling samples the current, then clears the pixel and then samples the baseline (pedestal) current of the pixel. Both currents are subtracted and the residual current is measured. Advantages of this scheme are rejection of 1/f noise and rejection of pedestal current. The ADC just needs to cope with the signal itself. Disadvantages are the higher noise (the noise of first sample is added to the total noise) and longer processing time: The signal needs twice the settling and sampling time.

- When single sampling, the ADC digitizes the complete current (including the pedestal) directly. The pedestal needs to be known a priori and is subtracted later. Advantages are the shorter time needed for readout, the lower noise in the input current. Disadvantages are that the range of the ADC needs to cope with pedestals and signal at the same time, so either the ADC needs a wider dynamic range (yielding higher noise on the measured current if ADC noise is constant in ADC codes and each ADC code is wider) or has a reduced headroom for signal.

To achieve the readout speed required for Belle II, single sampling was chosen. Pedestal currents are subtracted both using a constant current for all pixels and a small pixel by pixel offset. The remaining pedestal current is digitized together with the signal and is subtracted in digital domain. If most pixels in a readout are not hit, noise on the supply lines can be rejected using pixels without hits and calculating

common mode noise from them. For the DEPFET pixel detector in Belle II this is possible since the ladder with highest occupancy is expected to have an occupancy of (1.28 ± 0.30) % at design luminosity [38].

4.2 Sensor Readout

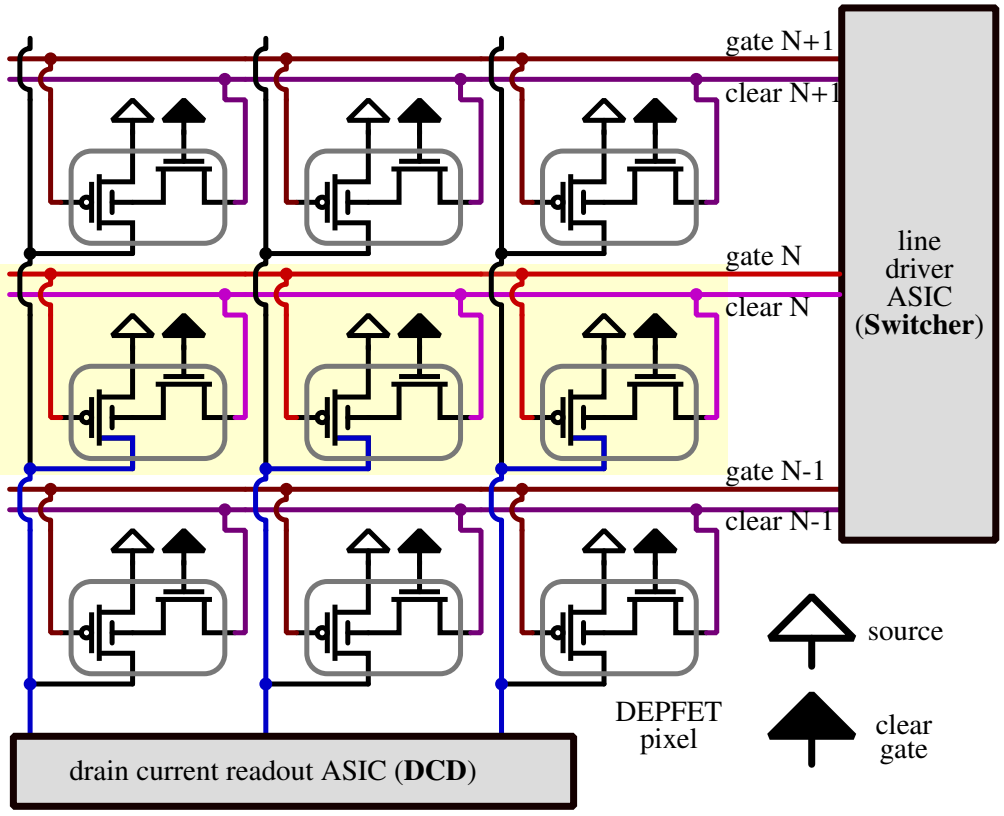


Figure 4.8: Schematic of a DEPFET Matrix. All *source* and *cleargate* are connected for all pixels on the matrix. The clear and gate lines of each row are connected together and to a line driver (SWITCHER) ASIC. The drain lines of pixel in each column are connected together. The highlighted row is active. Only active DEPFETs are conducting, so that the gate-line, drain line pair uniquely identifies the pixel.

A DEPFET sensor is a matrix of DEPFET pixels connected as shown in figure 4.8. The source contacts of all pixels are connected to a common source contact. The gate and the clear contacts of pixels in one row are connected together to form a gate line and a clear line. The drains of the pixels in the same column are connected together to a drain line. A constant source voltage is applied to the DEPFET matrix, which can be steered using the gate and clear lines. Each drain line is connected to an ASIC with a constant input potential which can digitize the received current. Each pixel can now be identified by a unique pair of gate line and drain line. For readout, an individual gate line is switched to the "gate-low" potential, so that its transistors are in an "on" state and the other transistors are kept in the "off" state, with a "gate-high" potential applied. All clear lines are on the "clear low" potential and the pixels are in readout mode. After the drain current is settled, it is measured and compared to the known pedestal current of the DEPFET pixel. Next, all pixels within a row are reset by applying a "clear high" potential

for a short time ($\approx$ 20 ns) to the clear line of the gate line in the “on” state. This effectively removes all charge from the internal gate of the DEPFET pixels, resetting them. A measurement of the clear efficiency can be found in figure 7.3 on page 81. After this, the gate line is switched into an "off" state and the readout for the next row is started.

This continuous readout is called rolling shutter readout. The integration time of each readout has the same length but a different start point. If a particle hits the matrix at time T, all rows between the time T and $T + \Delta t$ need to be stored, where Δt is the frame time. One drawback of the DEPFET technology used is the inefficiency in time. If a particle passes through a row while the row is cleared, the particle cannot be detected. For Belle the frame time is 20 µs while the clear time is 20 ns, so the effect is in the order of 0.1 %. There are other DEPFET like detectors which do not suffer from this, but are bigger and more complex to steer [39].

The readout of the matrix is done by two ASICs. A line-driver (the Switcher, described in section 5.1) which steers the clear-lines and gate-lines and a current digitizer, which measures the drain currents (the DCD, described in 5.2). Knowing the sequence of current measurements on each drain line and the time when which gate was switched on, the Source Drain currents of all pixels can be reconstructed.

In order to achieve high readout speed, 4 rows are read out in parallel. This is realized by connecting all gate and clear contacts of 4 rows to one line and connecting every 4th pixel of each column to one drain line. This 4-fold readout needs four times more drain readout channels but is 4 times faster.

4.3 Module Layout

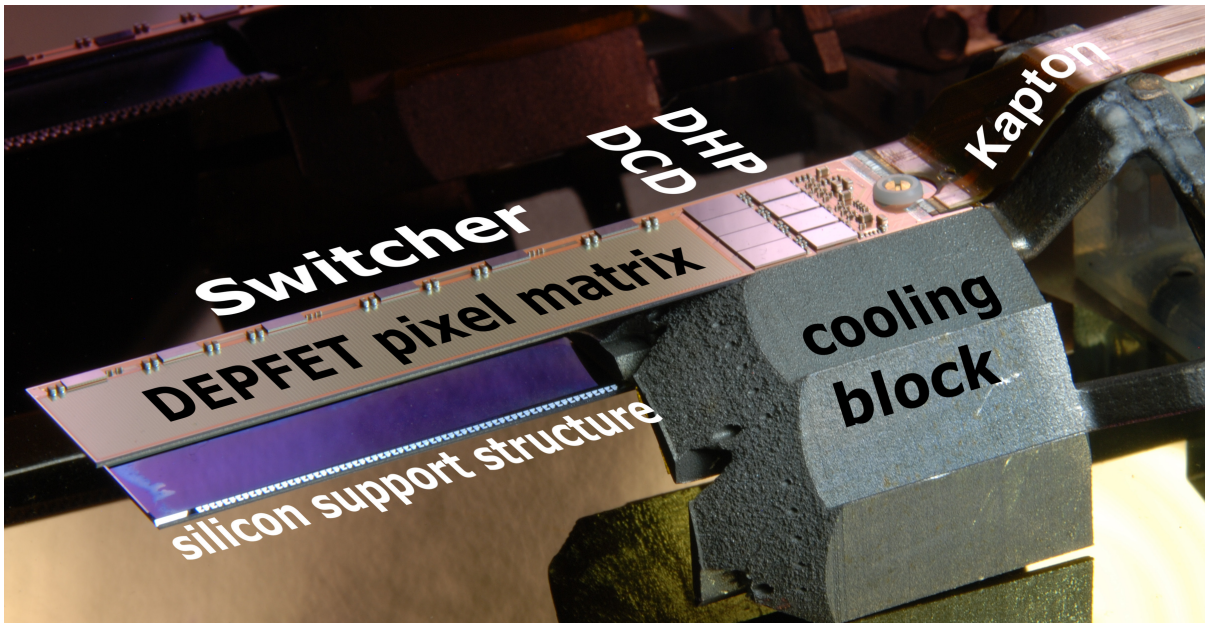


Figure 4.9: Two PXD9 modules on mounted on a cooling block (SCB). On the upper module, The sensor, ASICs and passive components are visible. On the lower module the thinned backside of the sensor and the structured etching of the balcony can be seen.

A Belle II DEPFET Module is an all-silicon structure containing an active pixel sensor and the readout electronics for this. A photo of two modules can be found in figure 4.9 showing front and backside. A module mainly consists of three parts:

- A matrix of 768 columns and 250 rows of DEPFET pixels organized in $768/4 = 192$ gate-lines and $250 \times 4 = 1000$ drain-lines. For the pixel size, the matrix is segmented in two parts: The 512×250 pixel in forward and backward direction have a size of $50 \times 60\,\mu m^2$ on the inner layer and $50 \times 85\,\mu m^2$ on the outer layer. The 256×250 pixels in the central region are smaller: They have a size of $50 \times 55\,\mu m^2$ on the inner layer and $50 \times 75\,\mu m^2$ on the outer layer. For steering voltages the matrix is segmented in three parts of 256×250 pixels, which have their own *cleargate* and *gate-on* potential. This allows to mitigate inhomogeneous radiation damage along the column direction if needed.

- The balcony, which features 6 line driver ASICs called Switcher which are bump bonded to the module. Each Switcher steers 32 gate- and clear-lines of the matrix. Each of the three segments of the matrix is steered by two switchers. Additional capacitors are placed close to the Switcher ASICs for voltage stability. Due to space constrains on the balcony, some pads for these are placed on top of the thinned DEPFET matrix. Chapter 5.1 describes the Switcher in greater detail.

- An end of module which contains bump bonded readout ASICs. Two types of ASICs are needed, each pair of ASICs reads out a quarter of the pixel area: The Drain Current Digitizer (**D**rain **C**urrent **D**igitizer (DCD)) features 256 inputs for drain lines which are held at constant potential and digitize incoming currents with an 8 bit ADC at the frequency of ≈ 9.53 MSample/s. The output data rate of one DCD is $\approx 20\,\mathrm{Gbit\,s^{-1}}$ – too much to be transmitted off module. A second ASIC, the Data Handling Processor (DHP), reduces data from the DCD by zero suppression: The signal is compared against the known pedestal current and only transmitted if the value of a signal is above threshold and requested by a trigger. Doing this, a data reduction of 20 can be achieved. The DHP sends the data out over a $1.52\,\mathrm{Gbit\,s^{-1}}$ link, steers the DCD and acts as a slow control master. One DHP additionally steers the Switcher ASICs on the balcony. The detailed description of the DCD is given in 5.2, the description of the DHP can is given in 5.3. The four DCDs can subtract different currents before digitizing the current from the DEPFET pixels. This allows to mitigate inhomogeneous radiation damage along the row direction and compensate for pedestal spread due to production variation.

A single Kapton flexible PCB, carrying lines for 24 voltages and 11+1 differential data lines[3], connects the module to the backend electronics. Lines carrying high power are connected using reflow soldering to the end of stave, other voltages and signals are wirebonded to landing pads in a 2 layer wirebond process. The depletion voltage needed at the backside is supplied by a punch-through implantation below the drain line fanout at the sensor edge. Around 100 passive components are soldered to the end of stave, mainly decoupling capacitors. Each module will be connected to a cooling block using one screw on the end of stave.

A DEPFET module is partially thinned and needs both frontside and backside implantations. This is achieved by first processing the backside of the sensor wafer, then wafer bonding it to a handle wafer. The sensor wafer is then thinned to the required thickness and its frontside is processed. Anisotropic wet etching allows to a structured thinning of the backside. The complete active area is thinned to 75 um, using the SiOx interface of the wafer bonding process as an etch stop. The balcony has grooves etched into it, which allows a lower material budget while being ridged enough to be self-supporting[4]. The end of module outside the acceptance region is not thinned. It hosts the readout ASICs which dissipate

[3] 5 Data lines for slow control, one clock line, one control line to the module, 4 high speed data lines from the module. The +1 is an analog test sent over one differential line.

[4] The silicon used for the handle wafer has a (110) orientation. Using potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH), structured thinning of the handle wafer can be achived with wall angle of 53°.

most power and is connected to an actively cooled cooling block (SCB). They are actively cooled by the cooling block. The active area of the sensor uses below 1W since only one gate is switched on simultaneously. The Switchers use below 0.5 W. Due to the low power dissipation in the acceptance region, no additional active cooling apart from forced convection is required.

A ladder for the PXD is made of two modules (forward and backward[5]) glued together at $z = 0$. Additional grooves for ceramics allow a stiff connection. Since the Switchers need to be at the same side after gluing, forward and backward modules need the Switcher balcony at different sides. For the two layers of the pixel detector, four different module types are needed: IB, IF, OB, OF (I=inner layer, O=outer layer, B=backward, F=forward).

4.4 Services and Back End Electronic

The pixel detector needs outside services to work. These are cooling, power and control signals.

Cooling The detector is cooled by a cooling block at the end of stave and a laminar flow of cold nitrogen along the sensor. The cooling block works using a closed two-phase CO_2 loop. Liquid CO_2 is produced at a pressure near its evaporation point. Heat is removed by evaporating of CO_2 into a gas phase. This allows for constant temperatures along cooling lines if enough liquid CO_2 is circulated. In Belle II, **PiX**el **D**etector (PXD) and SVD will use liquid CO_2 from the IBBelle cooling plant, a design already used at CERN for the **I**nsertable **B**-**L**ayer (IBL) of the ATLAS experiment [40].

Power Each module of the PXD is connected to a patch panel using a Kapton flexible PCB. The patch panel carries all signals and voltages required for detector operation and has decoupling capacitors mounted. On the patch panel, data and power lines split. Power is routed using Glenair Micro-D-Sub cables to a custom made power supply, which provides the 24 voltages needed for detector operation and has remote sensing capabilities[6] for all ASIC supply channels, *gate-on*, *gate-off*, *clear high* and *clear low*. It is remote controlled over TCP and connects to the Belle II slow control. In the experiment the power supply will be in a crate; for lab usage cooling and main power have to be provided. [41, 42]

Control Signals Data is routed from the patch panel to the module controlling backend electronic, the **D**ata **H**andling **H**ybrid (DHH). The DHH consists of two **F**ield **P**rogramable **G**ate **A**rray (FPGA) boards, one **D**ata **H**andling **E**ngine (DHE) for each PXD module, and one **D**ata **H**andling **C**oncentrator (DHC) for each 5 DHEs. The DHE is a module controller. It sends clock and control signals to the PXD Module, receives high speed data from it and acts as slow control master. Data from the modules is mapped from chip coordinates to module coordinates and is clustered to reduce its size. Using Trigger information from the DHC, the DHE builds events and transmits them to the DHC using an optical high speed link. The DHC bundles data from five DHEs and distributes clock and control signals to them. At this stage, the pixel data is still too much to be saved and is reduced by using **R**egion **O**f **I**nterest (ROI) selection in the **ON**line **SE**lector **N**ode (ONSEN). It receives clustered data from the DHC and only saves data which is at least in one ROI. The achievable data reduction factor depends on the background but is planned to be in the order of 10 [43]. The ROIs are produced by two systems: The **DAT**a **CON**centrator (DATCON), a system doing 4 layer tracking on FPGAs using **S**ilicon **V**ertex **D**etector (SVD) data and the HLT, a

[5] Forward modules are in boost direction, $z > 0$ in detector coordinates, backward modules are in $z < 0$.

[6] Due to long high resistivity lines, the voltage at the power supply and the voltage at the load can differ several volt in the system. Sense lines counteract this by measuring voltage (almost) without using current. The power supply regulates the sense voltage, thus counteracting voltage loss on the power lines.

server farm for online tracking on SVD and CDC data. Particles with low momentum will not reach all layers of the SVD and cannot create ROIs. For Belle II, especially pions with an energy in the range of a few ten MeV are interesting. They will be saved using neural networks in the DHEs, where their cluster shape and their created charge are analyzed. They are then marked and will be kept even if they are outside of the ROIs. Data selected by the ONSEN will be sent to the event builder. A more complete description of the DAQ chain can be found in [44] (ONSEN), [45] (DATCON) and [46] (**H**igh **L**evel **T**rigger (HLT)). An overview can be found in [9].

CHAPTER 5

Development Process for Large Scale Pixel Modules

The Belle II pixel detector is a complex system. Three ASICs need to work together to read out the DEPFET matrix.

During the development process, single ASICs were characterized using specialized test setups before several ASICs were used together. This process allowed concentrating on single system aspects, limiting the complexity of the development process.

The components used for the test performed during this thesis are described in chapters 5.1.1-5.3. This includes the ASICs (DCD, DHP, SWITCHER) and the testboards (Hybrid 4, Hybrid 5, Hybrid 6). An overview of software needed for steering and reading out the system is described in chapter 5.4, with an emphasis on software developed during this thesis.

Development steps performed during this thesis are:

- Readout and steering of standalone DCD (Development described in [47]). Tests (and some changes) of Software and Firmware were performed as part of this thesis.
- Steering of standalone Switcher [48]
- Characterization of standalone DCD (Chapter 6)
- The readout and steering of a single DHP02 as well as its characterization (mainly in [49]). The development of the DHP02 DAQ software and its integration into the existing DAQ system was preformed as part of the thesis.
- Steering a single SWITCHER using a DHP02 and Switcher1.8G, verifying the interface between both ASICs, finding the correct timings and settings for an optimal Switcher sequence and checking the different operation modes of the Switcher. This was performed using a Hybrid 5 PCB without matrix. Instead of the matrix, a small PCB was present where several channels were wirebonded to and could be probed using an oscilloscope.
- Steering a DCD by the DHP. Here, the settings for the communication and timing between both ASICs were optimized so that DCD is in sync with the **D**ata **H**andling **P**rocessor (DHP) and data transmission from and to the DCD works as expected. This was done for DCDBv2, DCDBv3pipeline, DHP02 and DHPT1.0 at different clock speeds.

- Creating mapping tables between DHP memory location and position in input/output data streams for ADC data/offset DAC settings. Implementing these in software and implementing mapping between the position assumed by the DHP and the real pixel position on large and small PXD6 matrices.

- Reading out a small matrix by DCD and DHP, with a Switcher controlled by the DHP. The matrix was characterized and its operation voltages were optimized using measurements with a laser system (chapter 7).

- Reading out a large matrix with multiple DCDs, DHPs and Switchers and optimizing its operation voltages (chapter 8).

5.1 Component Description

During the thesis, multiple components were used which are described in this chapter. These contain the ASICs, measurement boards and the readout systems. During the thesis, mainly two **A**nalog to **D**igital **C**onverter (ADC) ASICs were used, the DCDBv2 and the DCDBv3pipeline. The DCDBv2 was characterized in depth and irradiated, while the DCDBv3pipeline was used for later measurements on data link performance. Both ASICs were developed at the University of Heidelberg and are described in more detail in chapter 5.2. The ASICs for steering and data reduction (DHP02 and DHPT1.0) were developed in Bonn, the DHP02 was mainly characterized in Bonn [49], parts of the characterization were done in the scope of this thesis. Both versions are described in chapter 5.3. The SwitcherB1.8 ASIC is the row controller of the DEPFET module. It was developed in the University of Heidelberg. It has to ramp up and down the gates of the 4 rows of pixels attached to its output and apply the clear pulse to all the pixels connected to that line, with an estimated capacitive load of 150 pF [50]. The ASIC needs 7 voltages: The four steering voltages the ASIC should apply to the DEPFETs (*Clear High/Low*, *Gate High/Low*), the voltage for the digital logic of the Switcher (SW_{VDD}, 1.8V above SW_{GND}), a voltage for the Switcher substrate which needs to be the lowest one applied to the Switcher[1] (SW_{sub}) and a reference voltage for the level shifters used to switch the high voltage signals (SW_{Vref}, 1.8V above SW_{sub}). It features 32 output channels, each with a clear and gate line, and is controlled over four steering signals: ClearStrobe, GateStrobe, SerIn, Clock. Internally, the Switcher consists of a 32 bit shift register with each bit being the enable for one output channel. The enable signal is fed by SerIn and Clock, the output of the last bit in the shift register is routed to a SerOut pad, so that multiple Switchers can be daisy chained. Rows on a disabled output have a constant high potential on the gate line and a constant low clear potential so that the DEPFETs connected to them are integrating charge while the transistor itself is switched off. The gate line is switched on (*gate-on* voltage applied) on the rising edge of the GateStrobe signal. Simultaneous, the last active gate line is switched off (*gate-off* voltage applied). If the Clock signal is low this happens immediately, else when the Clock signal gets low. If the ClearStrobe is applied, the clear lines of all currently enabled Switcher outputs apply the *clear high* voltage as long as the ClearStrobe is held high. Using this, multiple Switcher sequences are possible, like reading only parts of the matrix, not activating certain gate/clear lines, switching between active gates with and without an overlapping time, where both are switched on.

There have been multiple Switchers with additional features, but they can be treated as similar ASICs in the scope of this thesis – except for one feature: The first implementation of the Switcher can ramp a

[1] This is a voltage needed on most CMOS ASIC, but in typical applications, it can be guaranteed that the ground voltage is the lowest voltage used. Due to irradiation damage on the matrix, this is not the case for the Switcher ASIC

voltage of 25 V[2] with respect to SW_{GND}, while typical matrices need a voltage between 16V and 19V with respect to matrix GND for fast clear times. Since matrix GND (*source* voltage) is at +7 V, clear performance with this Switcher was limited and the ASIC had to run out of its specifications. Newer versions can ramp an amplitude up to 25 V, where the lower level can be up to 25 V above SW_{GND}.

5.1.1 Measurement Boards

ASICs and matrices were tested using custom PCBs. ASICs on bump bond adapters are glued to them and are then electrically connected by wirebonds. These Hybrid PCBs offer a variety of test points, power and data adapters. Three different boards were used:

5.1.1.1 Hybrid 4

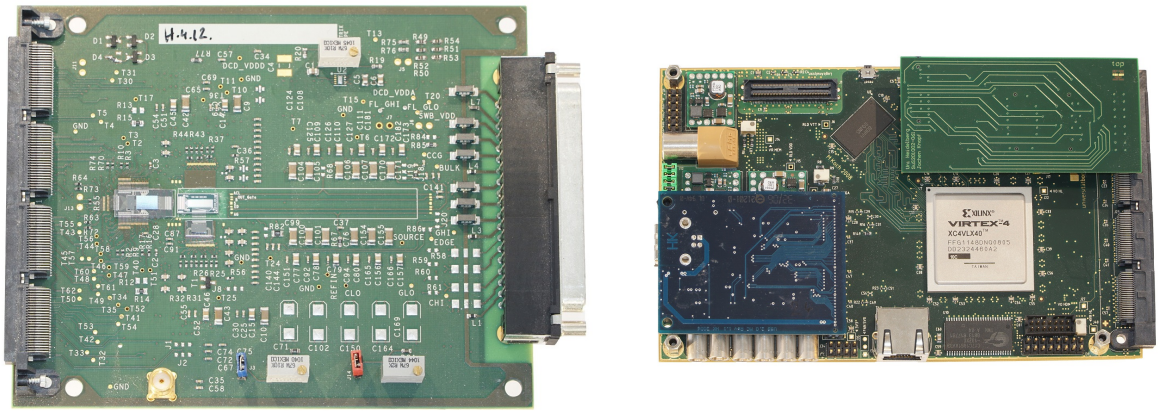


Figure 5.1: *Left:* Picture of Hybrid 4. *Right:* Picture of the Virtex 4 readout system used to read out Hybrid 4

Figure 5.1 shows a Hybrid 4[3] PCB which features a DCD with a **DCD R**ead**O**ut (DCD-RO)[4] directly connecting to the V4 FPGA readout system developed in Bonn [34]. It is used to operate a small (32×64 pixel) PXD6 matrix, which is wirebonded to the DCD and a single Switcher. The DCD and Switcher are mounted on bump bond adapters, which are glued to the PCB. Power and signals lines are connected to the PCB using wirebonds. A hole below the matrix allows backside illumination with a laser and reduces material particles have to transverse in a beam test. Power is supplied over a 25 pin D-Sub cable. An external current source can be connected to inject test currents into the DCD. The PCB is connected over a 200 pin Samtec QTS-100 connector to the V4 readout board. The Switcher in this system is steered by the FPGA. The area below the DCD wire bond adapter has no copper planes or vias, so heat produced by the DCD dissipates slowly and the DCD can reach rather high temperatures.

[2] The specifications mention a maximum voltage of 20 V, but higher voltages were tested without damaging the Switcher

[3] More precise: Hybrid 4.1. Hybrid 4.0 was used to test the DCD with a matrix of the previous generation which uses two Switchers for clear and gate. It was not used for measurements shown in this thesis.

[4] The data output of the DCD is a low voltage single ended signal, designed to transmit data over a centimeter distance. To read this out, the DCD-RO ASIC translates this into a differential signal. Therefore it sits on the same bump bond adapter. Due to space constraints (bump bond pads, chip size, wire bond pads, connector size and pins on the FPGA), signals are multiplexed 2:1, so only half of the DCD can be read out simultaneously. It was used as a placeholder when the DHP was still in its design phase.

5.1.1.2 Hybrid 5 – Full Scale System Demonstrator with Small DEPFET Matrix

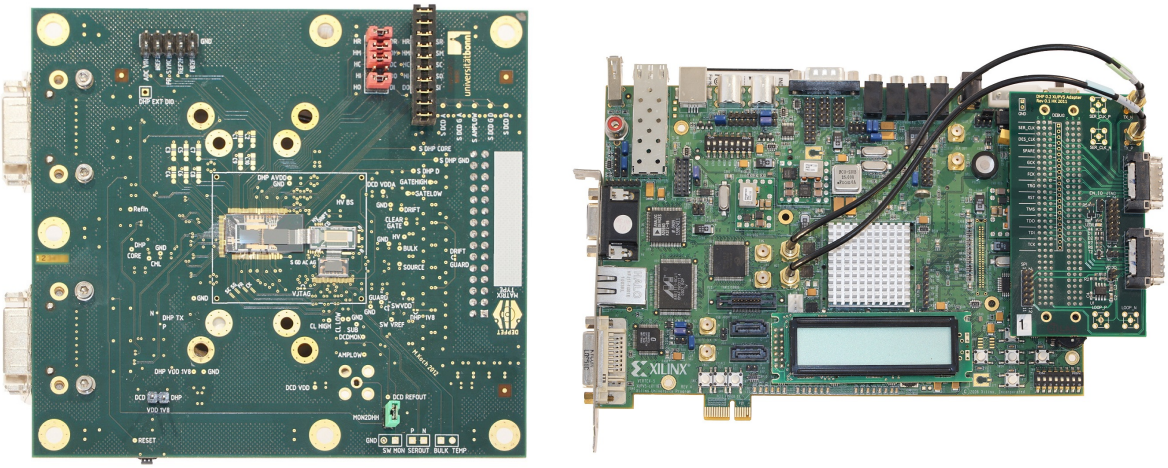


Figure 5.2: *Left:* Picture of Hybrid 5. *Right:* Picture of the DHH emulator used to read out Hybrid 5. The adapter board developed in Bonn can be seen on the right side of the FPGA board.

Hybrid 5 is a full scale demonstrator for the final PXD Module. It contains a small (32×64 pixel) matrix, steered by a Switcher, a DCD to digitize the DEPFET currents and a DHP to do zero suppression and to control both DCD and Switcher. DCD and DHP share a bump bond adapter, the Switcher is mounted on a second one. Both bump bond adapters and the matrix are glued to the PCB and are wirebonded. Below the Matrix a hole in the PCB allows for backside illumination and reduces material (and therefore multiple scattering) during beam tests. On this PCB, the DHP acts as JTAG Master. To select which ASICs are in the JTAG chain (e.g. for boards with only a DCD mounted but no Switcher) headers are available. This also allows configuring DCD and/or Switcher using external (commercial) JTAG tools. A test current can be injected into the DCD over a SMA connector. Power is supplied over a 30 pin Samtec IPL1-115 connector. The system is connected to the readout (DHH emulator or a DHH) using two InfiniBand connectors[5]. The area below DCD and DHP has copper planes and many thermal vias, on the backside of the ASIC a water cooled block can be mounted.

5.1.1.3 Hybrid 6 – Large PXD6 Matrix

The Hybrid 6 PCB is a test system for a large PXD6 matrix. ASICs used for readout are directly mounted on the periphery of the matrix, which is then glued to the Hybrid 6 board. All matrices have 192 columns (3 DCD/DHP pairs) and 480 or 640 rows (4 or 5 Switchers). During design of the matrix, the DHP design was not finalized and the usage of DCD-RO ASICs was planned. The Switcher control and JTAG signals were routed off the matrix to wirebond pads. When the DHP footprint was finalized it was possible to change the metallization of the end of the matrix, but no connection for Switcher JTAG and control signals from the DHP was implemented. Thus, different to Hybrid 5, the Switcher ASICs still need to be controlled by the FPGA. The new control signals needed two additional InfiniBand connectors, the connectors used in Hybrid 5 stay with the same functionality. Since JTAG signals for the Switcher are single ended, 1.8 V logic, which is problematic to transmit over long cables, Hybrid 6 features a

[5] At time of design, this was assumed to be the final setup used in Belle. With a newer generation of the DHP, several high speed control signals could be bundled together in a single line using Manchester codes (a way to encode signals by transitions instead of voltage levels) and one of the InfiniBand connectors could be replaced by an RJ45 cable.

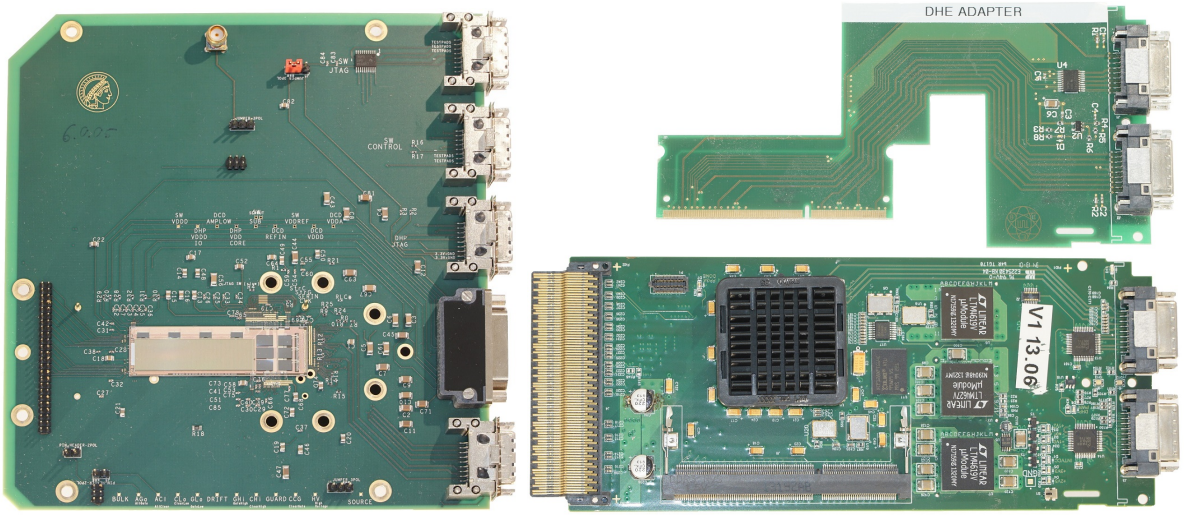


Figure 5.3: *Left:* Picture of Hybrid 6. *Right:* Picture of the DHE and the adapter board used to read out Hybrid 6

LVDS/Single ended level shifter, so that the signal is transmitted differential over the cable. Due to a poor choice of this component, the single ended signals use 3.3 V which lead to the destruction of the matrix with the most Belle II like pixel geometry available[6]. For one other matrix, the level shifter was undervolted to 2.2 V, which the Switcher input pads can survive and the Switcher supply voltage was raised to 1.9 V. On the last module each single ended line was connected over a resistor so that too high voltages would not be able to force a current into the Switcher which could harm the input pads. Hybrid 6 uses a 51 pin Glenair Micro-D-Sub connector, which is the same type of connector and cable foreseen for the final Belle PXD modules. On the backside, a large water cooled block can be mounted.

5.1.2 Readout Systems

During this thesis several readout systems were used, one for standalone DCD measurements, a second one for first measurements with the DHP (DHHemulator). The third readout system used was the final Belle II backend electronic (DHE). These readout systems and their differences are described in the following sections.

5.1.2.1 Virtex 4 Readout System

Hybrid 4 is read out using the Virtex 4 readout system shown in figure 5.1. It is a FPGA board developed in Bonn [34], using a firmware developed at the University of Heidelberg [47]. The board communicates with the PC over USB 2.0, has trigger inputs for **T**rigger **L**ogic **U**nit (TLU) communication and connects to Hybrid 4 using a 200 pin connector, directly reading DCD data. Different firmware versions were available for raw and zero suppressed data readout of the matrix and readout of data from a single ADC of the DCD. In this thesis, the system was mainly used for characterization of ADC data.

5.1.2.2 DHH Emulator

The DHH emulator is a readout system for the DHP and was used to readout Hybrid 5. It is shown in figure 5.2 and consists of a commercial Virtex 5 development board (XUPV5-LX110T), for which an

[6] The input pads of the Switcher were made for 1.8 V. Under constant load, the overvoltage protection failed

adapter board was developed. Data is transmitted to the PC using Gigabit Ethernet with the UDP protocol. The DHP was used with half of its data rate (800 Mbit s^{-1} instead of 1.6 Gbit s^{-1}) to keep the input data below the output bandwidth, so that a complex buffering logic could be avoided. Data from the DHP is directly packed and sent over UDP, all event building has to be done by the receiving PC. This allows continuous data acquisition. Slow control and measurements (ADC transfer curves) are steered using a Microblaze softcore implementation, which leads to a rather low data rate in the slow control. The DHH emulator features a TLU receiver for triggering. Due to the slow transmission of the trigger number (only available after the event has arrived), data has to be reordered on the PC. In this thesis, it was mainly used for readout of Hybrid 5.

5.1.2.3 DHE

The DHE is a part of the **D**ata **H**andling **H**ybrid (DHH), the first system of the PXD back end electronic in Belle II and is used as a readout system for lab use. It is a FPGA card following the **A**dvanced **M**ezzanine **C**ard (AMC) standard. It features 2 InfiniBand connectors to connect a PXD module, a SODIMM slot for memory or addon cards and a backplane connector. A precision current source (0 to 200 µA, 3 nA steps) is available to characterize DCDs connected to it. During Belle II operation it will be located in an **A**dvanced **T**elecommunications **C**omputing **A**rchitecture (ATCA) shelf and transmit data over backplane to the DHC using a 6.5 Gbit s^{-1} link running a custom-made UCF protocol [51]. The DHC bundles data from 5 DHEs and sends it out for further processing. For lab usage, a single DHE card data can be mounted on a carrier board which supplies the DHE with power and connects it to **S**mall **F**orm-factor **P**luggable (SFP+) connectors, where data (Ethernet, using UDP), slow control (Ethernet, using IPBUS) and a TLU connection are present. The DHE does event building on the FPGA and discards all (empty) packets of the DHP. Events are sent over UDP to the PC, where the frames of the event need to be put together. It acts as JTAG master using a hardware implementation and creates the clock, trigger and synchronization signals for the system.

For Belle II, memory in the SODIMM slot will be used for storing data from the DHE, for Hybrid 5 operation this was not needed since only a single DHP/DCD pair is connected. For Hybrid 6 the SODIMM slot is used for an adapter card delivering the Switcher control and JTAG signals to the DEPFET. Both DHE and the adapter card are shown in figure 5.3 (*right*). In this thesis, the DHE was mainly used for measurements with Hybrid 6.

5.2 Drain Current Digitizer for Belle

The Drain Current Digitizer (DCD) is used to digitize the drain current from the DEPFET pixels. It consists of 256 analog channels with a readout speed of 9.6 MSample/s and a digital block with eight outputs, each 8-bit wide working at a speed of 305 MHz (at Belle II) and eight 2-bit inputs for pedestal-compression data, working at the same speed. Each analog channel consists of two cyclic current Analog Digital Converters (ADCs) working interleaved for higher sampling rates, a Trans-Impedance Amplifier (TIA) as input stage as well as static subtraction current sources and dynamic current sources for pedestal compression. It was produced in UMC 180 nm technology and has a size of $4\,240 \times 4\,969\,\mu m^2$. It uses two high speed control inputs, a 305 MHz clock and a synchronization signal every 128 clock cycles (every 4 samples). Its settings are accessed over JTAG.

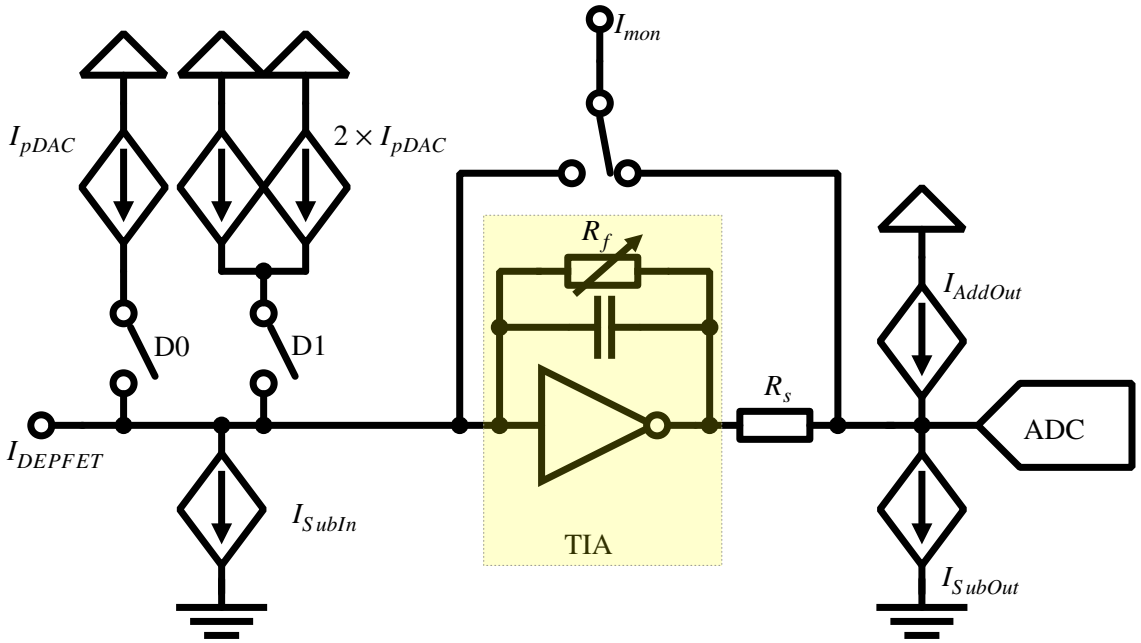


Figure 5.4: Block diagram of a single DCD channel. D0 and D1 are the control bits for the 2-bit current sources, which can be dynamically switched. The input node is stabilized by an TIA, the resulting current is sampled by an ADC.

5.2.1 Trans-Impedance Amplifier

Current from a DEPFET needs to be fed into a constant potential to minimize effects from the drain line capacitance and thus to have low settling times needed for the readout speed. In all versions of the DCD, this is achieved by a **T**rans-**I**mpedance **A**mplifier (TIA). The TIA is show in figure 5.4. It features a switchable feedback resistor R_f in the return path which allows to change the amplification. Capacities in the TIA and in the return path can be added to adjust the TIA bandwidth, allowing to cope with different drain line capacitance. The ADC is connected to the TIA outpup by the resistor R_s, so a voltage change of the TIA output will result in a current change for the ADC. Assuming a constant ADC input voltage, the current change is $\Delta I_{ADC} = {}^{R_f}/_{R_s} \times \Delta I_{TIA} = 1 \times \Delta I_{TIA}, \ldots, 4 \times \Delta I_{TIA}$. If only a small dynamic range is needed, the current can be amplified.

5.2.2 Pedestals Subtraction and Compression

Digitizing the DEPFET current directly is not ideal, since the expected signal is just a $\approx 3\,\%$ modulation on top of a large pedestal current[7]. Due to threshold and gain variations, pedestals may vary from pixel to pixel but have a large common part. The common part is subtracted by the SubIn current sources in front of the data TIA input. Pixel to pixel variations of the pedestal currents can be equalized using dynamic switched current sources. These are 2-bit current sources which are controlled via the DHP and add current to the input node. Data for them are shifted in over eight 2-bit channels running at 305 MHz. The current sources are active all the time and either source into the channel or into a (bypass) resistor. This is done so that the current source always has the same working conditions and thus settles

[7] Assuming $g_q = 500\,\mathrm{pA}\,e^{-1}$, $6\,000\,e$ signal, $100\,\mu\mathrm{A}$ pedestals)

fast. The 2-bit DAC is built out of 3 current sources like shown in 5.4. Depending on the data word (D1,D0), $0 - 3 \times I_{pDAC}$ are added to the current from the DEPFET. I_{pDAC}, the LSB current of the 2-bit DACs can be selected using a 7-bit DAC (pDAC). The algorithm used to find optimal offset DAC values is described in 8.2. In the DCDBv2 both SubIn and pDAC are very large. SubIn has a maximum range of around 320 µA, pDAC has a design value of 120 µA, the maximum range of the dynamic pedestal current sources is $3 \cdot I_{pDAC}$=360 µA. Those values are much higher than needed: SubIn needs to subtract the common drain current which is expected to be around I_D = 360 µA. pDAC sets the LSB strength of 2-bit current sources, which can reduce the pedestal distribution by a factor of 4. Assuming the pedestal distribution covers 4 times the ADC range 4×30 µA before compression, pDAC needs to be set to the dynamic range of the ADC (30 µA). Wider pedestal distributions can not be compressed without loosing pixel, thus larger pDAC values are not needed. Also, all 7-bit DACs in the DCDBv2 have a wrongly scaled lowest bit, which is twice as high as it should, effectively reducing the DACs to 6-bit resolution. Thus the granularity of the DACs is quite low and optimal DAC settings can be far from optimal values. These issues have been resolved in further DCD iterations.

5.2.3 Current ADCs

The ADC in the DCD digitizes currents, by comparing them with a reference current. A simple form of the used algorithm would look like this:

- Compare the current to a reference current (the threshold for the bit).
- If it is bigger than the reference current, the reference current is subtracted and the MSB of the digital word is set, else the current stays as it is and the MSB is zero.
- The remaining current is multiplied by two
- The above steps are repeated n times, until the design accuracy is achieved.

This algorithm has the disadvantage that the threshold for comparison needs to be the same at all places where the comparison occurs. To get better error redundancy (error = threshold variation) an algorithm with two comparisons is used, producing ADC codes in redundant binary representation. General properties of this algorithm are discussed in the next section. The specific implementations are introduced on page 39 (cyclic ADC) and 40 (pipeline ADC).

In a noise-free system this algorithm could yield an arbitrary accuracy. Real implementations add noise in each step and multiply existing noise together with the signal, limiting the maximum number of steps with meaningful output.

Redundant binary representation Typically, digital values are given as $(d_{n-1}, \ldots, d_0)$, $d_i \in \{0, 1\}$ and represent the number $x = \sum_{i=0}^{n-1} 2^i \times d_i$, so the numbers $[0, (2^n) - 1]$ can be represented with an unique representation. Negative numbers can be represented for example by the two's complement. In the redundant binary representation one allows $d_i \in \{-1, 0, 1\}$ to represent $x = \sum_{i=0}^{n-1} 2^i \times d_i$, so all numbers between $[-2^n + 1, 2^n - 1]$ can be represented. Many numbers have multiple representations, for example in a five bit system the number 13 can be represented as $(1, 0, 0, -1, -1)$, $(0, 1, 1, 1, -1)$, $(0, 1, 1, 0, 1)$, $(1, -1, 1, 1, -1)$ and $(1, -1, 1, 0, -1)$. Converting binary representation into standard binary codes is achieved by a 2-state state machine as introduced in [52]. To store a redundant binary representation number with N digits a $N + 1$ digit binary number is needed[8].

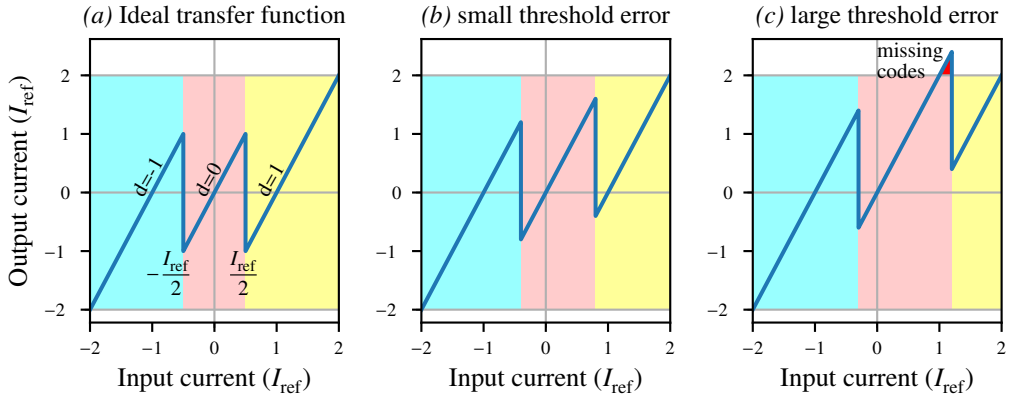


Figure 5.5: Transfer curve of a single ADC step. Each step produces one value $d_i \in \{-1, 0, 1\}$. *(a)* shows an ideal stage. *(b)* Small comparator threshold shifts can do not influence the digitization. *(c)* Large threshold shifts will result in missing codes, an digitization error described in 6.1.6

ADC digitization Scheme The ADC in the DCD digitizes a current in the following way: Using n steps and an initial current $I_{init} = I_{n-1}$

- I_{n-1} is compared both against a threshold of $-\frac{I_{\text{ref}}}{2}$ and $\frac{I_{\text{ref}}}{2}$. If it is smaller than $-\frac{I_{\text{ref}}}{2}$, a $d_{n-1} = -1$ is stored and a current of I_{ref} is added. If I_{n-1} is larger than $\frac{I_{\text{ref}}}{2}$, a current of I_{ref} is subtracted and $d_{n-1} = 1$ is stored. In the case $-\frac{I_{\text{ref}}}{2} < I_{n-1} < \frac{I_{\text{ref}}}{2}$, the current remains and $d_{n-1} = 0$ is stored.
- The remaining current $I_{n-1} + d_{n-1} \cdot I_{\text{ref}}$ is multiplied by two
- The above steps are repeated for $I_{n-2} = 2 \cdot (I_{n-1} + d_{n-1} \cdot I_{\text{ref}})$ until n steps are done.

For a current I_{n-1} in the range $[-2I_{\text{ref}}, -2I_{\text{ref}}]$ the output I_{n-2} is in the same range. Current outside that range will stay outside the range. The transfer function of this operation is shown in figure 5.5 *(a)*. One property of the algorithm is that wrong decisions in a step can be corrected in the next step. For example if the real value would be 60 but the step $n = 6$ would decide for high (value of 64), the following steps could still add -4 to the value, achieving a correct result. Therefore, the threshold of the high/low comparators is not needed to be exact. If the comparator thresholds are within $[0, I_{\text{ref}}]/[-I_{\text{ref}}, 0]$, each step will stay in the required input range and the result will be correct. To maximize the allowed threshold dispersion, a default threshold of $\pm\frac{I_{\text{ref}}}{2}$ is chosen. This is shown in the transfer function with a small threshold shift in 5.5 *(b)* and a too large threshold shift in 5.5 *(c)*.

For currents in the input range, the algorithm returns

$$I_{init} = I_{n-1} = d_{n-1} \cdot I_{\text{ref}} + \frac{I_{n-2}}{2} = \sum_{i=0}^{n-1} \left(d_i \cdot \frac{2^i \cdot I_{\text{ref}}}{2^{n-1}} \right) + \delta I,$$

with $\delta I < \frac{I_{\text{ref}}}{2^{n-1}}$. The data from each step is the currents redundant binary representation.

Implementation Details The algorithm described above was implemented as a cyclic version and a pipeline version. Both versions consist of multiple ADC stages; one is shown in figure 5.6. An ADC

[8] The code -2^N available in the $N + 1$ digit binary number will be unused

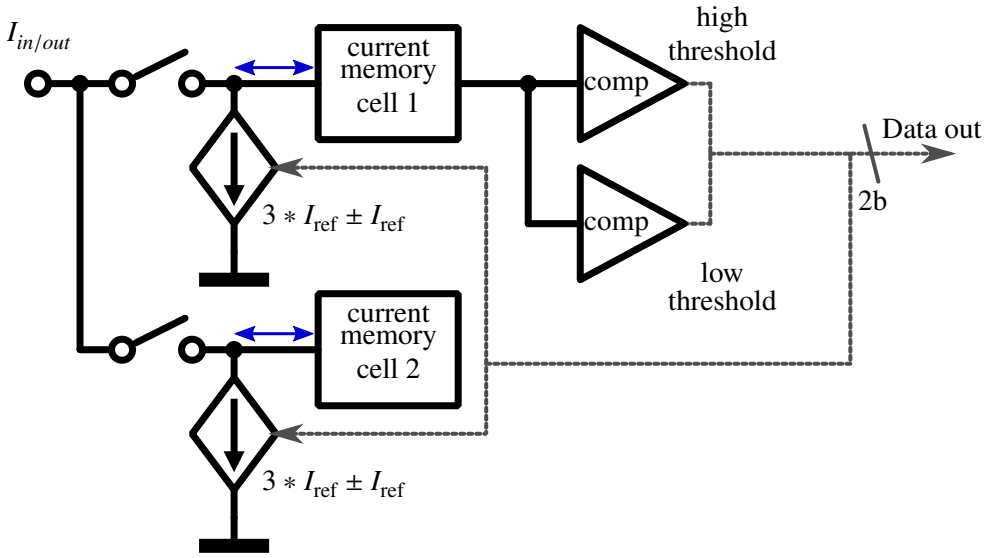


Figure 5.6: Schematic of single ADC stage: Current is saved in both memory cells. The current from memory cell 1 is compared against two thresholds. Depending on the result, (dashed data line) the current subtraction cells are switched high or low. Then, both switches are closed and the resulting current is read.

stage consists of two current memory cells. Each current memory cell has switchable addition and subtraction current sources. One of the memory cells is connected to two comparators which steer the switchable current sources.

During the digitization process, the input currents $I_{1\,\mathrm{in}}$ and $I_{2\,\mathrm{in}}$ are stored in current memory cells one and two. Then the current memory cells are switched to a hold state. The comparators connected to current memory cell one decide, if the current is above the higher threshold, between the thresholds or below the lower threshold. The current memory cells are switched to output their current and depending on the comparators the switchable current sources in both memory cells are switched to add $I_{1\,\mathrm{add}}/I_{2\,\mathrm{add}}$ or subtract $I_{1\,\mathrm{sub}}/I_{2\,\mathrm{sub}}$ to these currents. Since both current cells are on, the effective output current is

$$I_{out} = I_{1\,\mathrm{in}} + I_{2\,\mathrm{in}} + \begin{cases} I_{1\,\mathrm{add}} + I_{2\,\mathrm{add}} \\ 0 \\ -I_{1\,\mathrm{sub}} - I_{2\,\mathrm{sub}} \end{cases}, \tag{5.1}$$

depending on the comparator decision. Assuming $\left|I_{1\,\mathrm{add}}\right| = \left|I_{2\,\mathrm{add}}\right| = \left|I_{1\,\mathrm{sub}}\right| = \left|I_{2\,\mathrm{sub}}\right| = I_{\mathrm{ref}}$ and $I_{1\,\mathrm{in}} = I_{2\,\mathrm{in}} = I_{\mathrm{in}}$, this results in $I_{\mathrm{out}} = 2 \cdot (I_{\mathrm{in}} + d_i \cdot I_{\mathrm{ref}})$ for the next step.

The current memory cells used in the DCD are only able to sink current, while the algorithm needs both positive and negative currents. This is realized by current sources in the current memory cell, which add an offset of $3 \cdot I_{\mathrm{ref}}$ to the input current. This way, a negative current can be stored. The two comparators get a copy of the current stored in one of the current memory cells where it is compared against $2.5 \cdot I_{\mathrm{ref}}$ ($3.5 \cdot I_{\mathrm{ref}}$). If the current is below (above) $2.5 \cdot I_{\mathrm{ref}}$ ($3.5 \cdot I_{\mathrm{ref}}$), current is added (subtracted) in the memory cells by increasing (decreasing) the offset to $4 \cdot I_{\mathrm{ref}}$ ($2 \cdot I_{\mathrm{ref}}$). The comparator decision is stored as ADC output of this stage. Since the TIA inverts current, larger matrix currents result in more current flowing out of the ADC. Thus, a comparator decision below $2.5 \cdot I_{\mathrm{ref}}$ results in an output code of $d_i = 1$.

In the DCDs these reference currents are provided by the DACs Source_1 in the current memory cell and

Source_2 in the comparator. Both I_{Source_1} and I_{Source_2} provide a current of $0.5 \cdot I_{\text{ref}}$, thus the comparators contain 5 (low) and 7 (high) Source_2 current sources. The current memory cell contains 8 Source_1 current sources which are switchable, so that, depending on the comparator settings, 4, 6 or 8 are active.

If current sources are not set optimal, several errors can occur:

- An offset I_{offset} is added or subtracted during each step, i.e. $I_{n-2} = 2 \cdot (I_{n-1} + d_{n-1} I_{\text{ref}} + I_{offset})$, the input range is shifted by $2^n - 1/2^{n-1} \approx 2I_{offset}$ as shown in [34]. The DCD features strong subtraction current sources in front of the ADC which will dominate range errors.

- Due to the used algorithm, threshold shifts in the comparators do not change performance. Thus, the ADC works as long as the low comparator has a current between $[2.5 \cdot I_{\text{ref}}, 3 \cdot I_{\text{ref}}]$ and the high comparator has a current between $[3 \cdot I_{\text{ref}}, 3.5 \cdot I_{\text{ref}}]$.

- Changes in I_{add} and I_{sub} can have different effects:
  - Common changes where $\left|I_{add}\right| = \left|I_{sub}\right|$ change the gain of the ADC, since this effectively changes the dynamical part of I_{ref} in the current memory cell. As long as the comparators can cope with the changed effective I_{ref}, the ADC response is linear, else the response is similar to large threshold shifts.
  - Differential changes between I_{add} and I_{sub} produce discontinuities in the ADC curve, the largest at $\pm I_{\text{ref}}/2$. Assuming an error only in the first ADC digitization cycle this can be explained like the following: Between $\pm I_{\text{ref}}/2$ the first digitization cycle does not add or subtract current, thus it works correct. For input currents I_{n-1} below $-I_{\text{ref}}/2$, the first stage adds a current I_{add}. The digitization algorithm assumes this current would be I_{ref}. The following stages now digitize the current

    $$I_{n-2} = 2 \cdot (I_{n-1} + I_{add}) \equiv I_{n-2} = 2 \cdot (I_{n-1} + (I_{add} - I_{\text{ref}}) + I_{\text{ref}})$$

    instead of $I_{n-2} = 2 \cdot (I_{n-1} + I_{\text{ref}})$, producing a jump of $I_{add} - I_{\text{ref}}$. The input range of the ADC is $4 \times I_{\text{ref}}$. To have less than an 1 LSB jump due to this effect, $\left|I_{add} - I_{\text{ref}}\right| < {}^4/_{256} I_{\text{ref}}$ must hold true, same for I_{sub}.

- Different I_{ref} in both current memory cells are effectively the same as common changes to I_{add} and I_{sub} in one current memory cell, with the same effects.

Cyclic ADC Implementation (DCDBv2) The ADC in the DCDBv2 is built as a cyclic ADC from two of the above explained ADC stages. The first stage samples the current from the TIA in its first memory cell and then into the second memory cell, compares the current to the threshold and then puts out the current of $I_{\text{out}} = 2 \cdot (I_{\text{in}} + d_i \cdot I_{\text{ref}})$. This current now is sampled by both memory cells in the second stage. After processing, the second stage puts out the current into the first stage again. This cyclic process continues 4 times (8 stages) until a 9-bit accuracy is achieved. Each stage needs 8 clock cycles (of 320 MHz), the total process needs 64 clock cycles. This leads to a sampling frequency of 5 MSamples /s. Two ADCs work interleaved to achieve the row frequency needed for Belle

First sample	Mean input current	Output code
$I_{1\,\text{in}} < \frac{I_{\text{ref}}}{2}$	$\frac{I_{1\,\text{in}}+I_{2\,\text{in}}}{2} >= I_{\text{ref}}$	63 (too low)
$I_{1\,\text{in}} > -\frac{I_{\text{ref}}}{2}$	$\frac{I_{1\,\text{in}}+I_{2\,\text{in}}}{2} <= -I_{\text{ref}}$	-63 (too high)
$I_{1\,\text{in}} > \frac{I_{\text{ref}}}{2}$	$\frac{I_{1\,\text{in}}+I_{2\,\text{in}}}{2} <= 0$	1 (too high)
$I_{1\,\text{in}} < -\frac{I_{\text{ref}}}{2}$	$\frac{I_{1\,\text{in}}+I_{2\,\text{in}}}{2} >= 0$	-1 (too low)

Table 5.1: Possible sampling errors for the first stage of DCDBv2. $I_{1\,\text{in}}$ and $I_{2\,\text{in}}$ are sampled 12.5 ns apart so changes can happen. If the comparator threshold differs from $\pm\frac{I_{\text{ref}}}{2}$, some errors are more likely than others

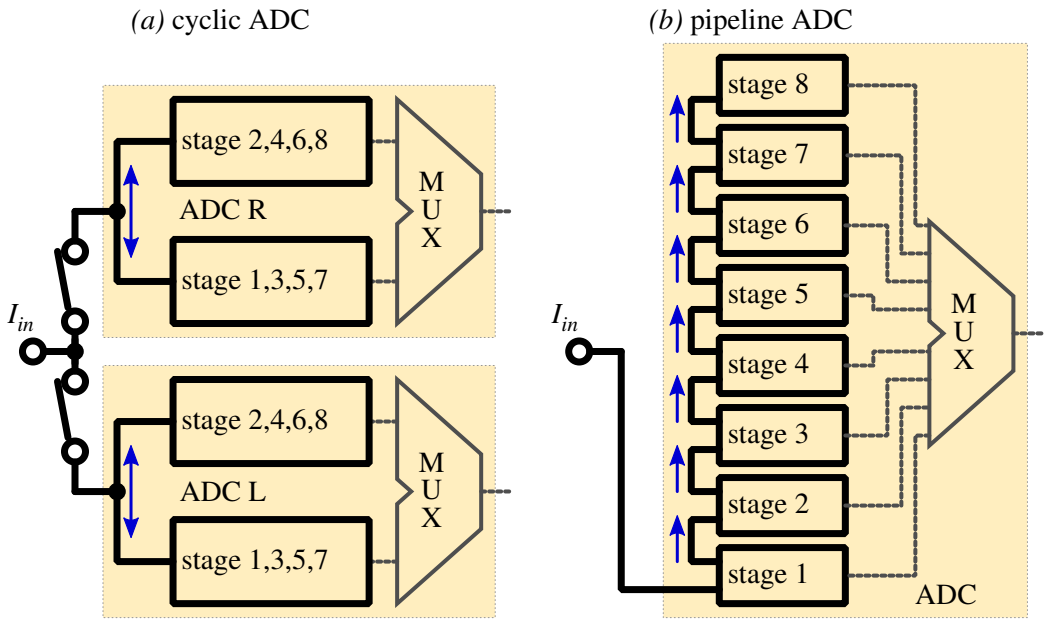


Figure 5.7: Schematics of current mode ADCs. Arrows indicate the way the current is copied. *(a)* In a cyclic ADC, the current is digitized in two stages working interleaved. To achieve the required sampling speed, two ADCs are used per channel. *(b)* A pipeline ADC consist of 8 stages, where either all even or odd stages work at the same time.

II. In this ASIC, the current from the TIA is sampled twice, each in a window of 12.5 ns. During these 25 ns the current needs to be constant, since the algorithm assumes $I_{1\,\mathrm{in}} = I_{2\,\mathrm{in}}$. If this is not the case, artifacts can appear if the error in the first step is too large to be corrected by the redundant binary algorithm. These are listed in table 5.1. Assuming perfect comparator thresholds, artifacts can only appear if $I_{1\,\mathrm{in}}$ and $I_{2\,\mathrm{in}}$ differ at least I_{ref}. Shifted comparator thresholds reduce the needed difference for these errors [53].

Pipeline ADC Implementation (DCDBv3pipeline) This ADC version uses 8 pipelined ADC stages. Each stage with an odd number samples the current from the previous (even numbered) stage into both of its current memory cells, then does the operation and sends out $I_{\mathrm{out}} = 2 \cdot (I_{\mathrm{in}} + d_i \cdot I_{\mathrm{ref}})$ to the next (even numbered) stage. Then the even numbered stages do their operation. After two operation cycles, the pipeline ADC is ready for the next input current. Using one ADC per DCD channel running at half the frequency of the two cyclic ADC, the pipeline ADC can achieve the required 10 MSamples /s while delivering lower noise. Having twice as much stages as both cyclic ADCs together, it needs more area. The first stage of the pipeline differs from the other stages: Its two current memory cells are combined to one with twice the current capacity. Since the multiplication of the first stage misses, the dynamic range of the pipeline ADC is twice the one of the cyclic ADC. The DCDBv3pipeline compensates this by having the option for a smaller resistor between TIA and ADC (15 kΩ instead of 30 kΩ), multiplying the current by 2 before the ADC[54].

5.2.4 Digital Part

The digital part of the DCD converts the ADC output from redundant binary representation into two's complement binary representation. An 8 stage ADC produces a 9-bit output. For convenience the LSB will be dropped since it is mainly noise. The resulting 8-bit output codes of the 256 is split into eight groups of 32 channels. Data from these are multiplexed and transmitted over one of the eight 8-bit output links. Data for dynamic pedestal offsets is received and demultiplexed in the digital part. Another task of the digital part is creating timing signals for the ADC from the external clock and the synchro-reset signal. The DCD features a JTAG interface for configuration and testing. A boundary chain register allows to simulate test inputs and to sample DCD output. One main configuration register and 3 channel register chains allow configuration of the DCD. The main configuration register contains 25 global 7-bit DACs and 36 global control switches[9]. The channel registers contain the switches to 3 channel individual settings.

5.2.5 Known Issues on DCDBv2

The main version of the DCD used in this thesis is the DCDBv2. It has several limitations:

- The 7-bit DACs have a bad scaled and inverted last bit. They effectively behave like 6 bit DACs. On most DACs this is no problem, but on some sensitive DAC settings (SubIn, pDAC) the optimal value could not be chosen.

- The subtraction current sink SubIn of the DCD is very strong compared with the dynamic range and much stronger than needed. Finding a good point for a pedestal distribution (all pedestals in the dynamic range, but as low as possible) was not always possible. This problem got worse due to the problem with the 7-bit DAC LSB.

- The dynamic 2-bit offset DACs are too strong (about 120 µA for the LSB when pDAC is set to its maximum). Due to this, there was typically only one good DAC setting for a given pedestal setting. The maximum current needed is the dynamic range of the channel input (see chapter 8). This problem got worse due to the problem with the 7-bit DAC LSB.

- The clock input has no buffer to amplify the received signal. Instead the external clock is distributed in the DCDBv2, increases the capacity on the fastest signal. When connected to a clock with a weak driver (like the one in the DHP02) the maximum operation speed is limited. Using DCDBv2 and DHP02 together, a speed of only 260 to 270 MHz was achievable. To be on the safe side, DCDBv2 and DHP02 were run at 250 MHz instead of the target speed of 305 MHz. The standalone DCD system did not have these problems.

- The reference current is not temperature stable. It is built using a diode and a resistor. Simulations showed a stability of $(0.14 \pm 0.05)\,\%\,^{\circ}\mathrm{C}^{-1}$. This is most critical for SubIn, because the large 100 µA DEPFET current has to be subtracted and to stay constant on the level of 1 LSB $\approx 80\,\mathrm{nA}$[10]. This effect was found during measurements presented in chapter 6.4.

[9] Numbers for DCDBv2

[10] This feature was not seen on DCDBv1, since SubIn was much weaker. All measurements were done with SubIn at high settings, where the current sources where in saturation.

5.2.6 Known Issues on DCDBv3pipeline

The DCDBv3pipeline was only used for part of the thesis, so no mayor investigation of its properties was performed. However, a few things were noticed:

- Like in DCDBv2, the 2-bit offset DACs are too strong. This was changed in following DCD versions due to results presented in this thesis.
- The pipeline ADC showed "missing codes", areas of several consecutive codes which do not appear in output data. These appear for some channels, mostly at code ±63 and look like errors due to strong threshold shifts in the comparator. Adjustments of settings and voltages reduce the occurrence, but limit the operation window of the DCDBv3pipeline.
- The DCDBv3pipeline supports very high gain options which are not usable for DEPFET operation, while providing no low gain option. Following versions removed the high gain setting if favor of a lower gain setting.
- The testpattern available in the DCD to test its digital communication is rather weak. It was improved in one of the following ASIC versions.

5.3 Data Handling Processor

A single DCD creates $8 \frac{\text{bit}}{\text{word}} \times 8 \frac{\text{link}}{\text{DCD}} \times 1 \frac{\text{word}}{\text{Hz link}} \times 305\,\text{MHz} = 19.5 \frac{\text{Gbit}}{\text{DCD}}$ of ADC data. To steer the 2-bit offsets it requires $2 \frac{\text{bit}}{\text{word}} \times 8 \frac{\text{link}}{\text{DCD}} \times 1 \frac{\text{word}}{\text{Hz link}} \times 305\,\text{MHz} = 4.9 \frac{\text{Gbit}}{\text{DCD}}$ of input data. Each DEPFET module has 4 DCDs, the total DEPFET detector has 160 DCDs, requiring ≈ 0.74 Tbit of input data and producing ≈ 3 Tbit of output data. It is not possible to transmit this amount of data to and off module within the geometrical and power requirements given by Belle II.

To cope with this amount of data, a second ASIC, the Data Handling Processor (DHP) is located at the end of stave, directly next to the DCD. Its task is to reduce the data from the DCD, provide the clock, the synchro-reset signal and the needed offset data to the DCD. One of the DHPs on a module steers the Switchers. Reduced data are bundled and sent over a single high speed link per DHP. Data reduction is achieved by zero suppression. Digitized currents from the DCD are compared against their known pedestals. If the measured current is above the pedestal plus a configurable threshold, the signal will be stored. All other data is discarded. To allow a low threshold operation, common mode noise of the system is reduced by common mode correction before the zero suppression. Further data reduction is achieved by triggered readout. The PXD has a frame rate of 50 kHz, while the expected trigger rate in Belle II is 30 kHz.

The known pedestals and the offset DAC data for the DCD are stored in memories. These memories can be programmed by JTAG. To guarantee data integrity against **S**ingle **E**vent **U**psets (SEU)[11], data is stored with Hamming encoding. Parameters for timing, operation modes and DAC settings are stored in two registers using JTAG. The registers are protected against SEU using triple redundancy. Further registers can be accessed over JTAG for the on-chip temperature sensor and for error detection[12]. A more detailed description of the DHP and its registers can be found in [49] and [55]. The processing chain of the DHP is shown in figure 5.8:

[11] An SEU is a flipping data bit (e.g. bit due to ionizing radiation).

[12] SEU protection and readout of the error counters is only available on the "production version" DHPT, not on the "full size demonstrator" DHP02. The DHPT uses a newer production technology, allowing additional features. SEU studies on the technology used can be found in [49].

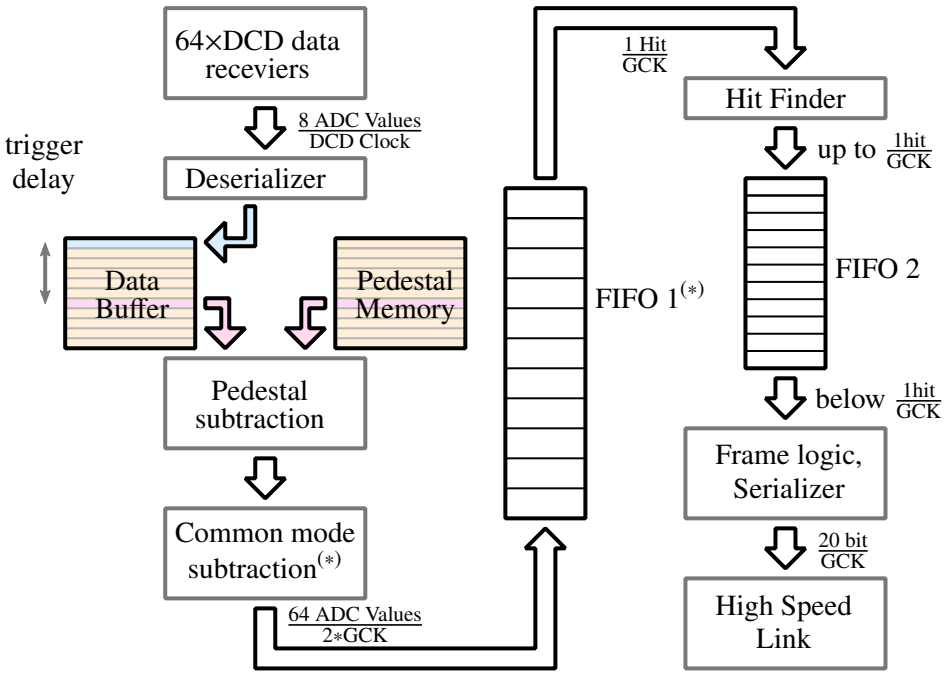


Figure 5.8: Schematic of DHP processing chain. Data arriving from the DCD is processed at a constant rate up to the hit finder. The time needed by the hit finder depends on the number of hits in each row, so FIFO1 is needed to buffer data.
(*): On DHP02 the whole row is stored in a single 64-byte wide FIFO1. On DHPT1.X FIFO1 consists of one FIFO for each of the 64 columns and the common mode subtraction block pushes data into the FIFOs only if there was a hit for this column, better utilizing the buffer capacity.

- Data from the DCD are stored in a dual port memory. This allows reading data from up to one frame before the trigger signal.

- Pedestals are subtracted and the common mode is calculated using a two pass algorithm described in [49]:

  - Pedestal values ($\text{ped}_{1\ldots N}$) are subtracted from the measured ADC values ($\text{ADC}_{1\ldots N}$). To handle only unsigned values, a constant value is added. $\text{data}_1 = \text{ADC} - \text{ped} + \text{const}$.

  - A coarse common mode (CM_1) is calculated over all N pixel in the gate $CM_1 = \frac{\sum_{k=0}^{N} \text{data}_{1\,k}}{N}$. This common mode may be biased by pixels with signal on top of the expected pedestal. This bias can be reduced using a second pass common mode calculation.

  - Pixels which show a signal are masked:

$$\text{data}_{2\,k} = \begin{cases} \text{data}_{1\,k} & \text{if } \text{data}_{1\,k} < \text{threshold} + CM_1 \\ CM_1 & \text{else} \end{cases} \tag{5.2}$$

  - The second pass common mode (CM_2) is calculated: $CM_2 = \frac{\sum_{k=0}^{N} \text{data}_{2\,k}}{N}$.

- Pixels are zero suppressed:

$$\mathrm{ZS}_{in\,k} = \begin{cases} \mathrm{ADC}_k - \mathrm{ped}_k - CM_2 & \text{if } \mathrm{ADC}_k - \mathrm{ped}_k - CM_2 < \text{threshold} \\ 0 & \text{else} \end{cases} \tag{5.3}$$

  After zero suppression, this data is written to FIFO1

- Hits are serialized in the Hit finder: $\mathrm{ZS}_{in\,k}$ words are taken from FIFO1 and all values above 0 are written in correct order as "hit"-words to FIFO2, containing column and amplitude. If data are from the next row, a "row"-word is added to FIFO2 before containing row and common mode of the following hit-words. The common mode is the same for all rows in a gate. Since the "hit"-word only uses 15 bit and the "row"-word would need 17 bit, the LSB of row information is transmitted within the "hit"-word, resulting in 16 bit wide words for both and less "row"-words in the data stream.

- Data words from FIFO2 are sent over a high speed link to the backend electronic. This link runs at 1.525 Gbit and follows the aurora standard. Due to 8-bit/10-bit coding, the effective data rate is 1.22 Gbit.

5.3.1 DHP02

The DHP02 is the main ASIC used during this thesis. When referring to the DHP without specifying, the DHP02 is meant. It is a full size demonstrator produced in an IBM 90 nm technology. Due to area constrains, FIFO sizes are limited to depth of 16 for FIFO1 and depth of 512 for FIFO2. DHP02 uses different modes for programming memory, sending memory content as raw data (further denoted as memory dumps), zero suppressed data acquisition and testing. When running, data is received and stored; the core only computes ZS data only when triggered. Switchers are steered using a sequencer which generates pulses for the Switcher signals with selectable phases. The timing of clock and synchronization signal for the DCD can be adjusted using a delay element. The DHP02 is connected to the back end using a clock line, two synchronization lines for frame synchronization and triggering, high speed data and slow control using JTAG.

Being the first full size DHP, the DHP02 has some limitations:

1. Due to a bug, the clock out signal of the DHP02 is weak, because the output stage for the clock signal is bypassed and the internal clock signal is directly used. Together with the missing input buffer on the DCD side, this leads to a limit of 260 MHz for the DCD operation.

2. The internal logic needs a matrix length of 32 gates (one Switcher) to operate or the steering sequence is scrambled. This is no problem for Hybrid 6 or final modules but Hybrid 5 only uses 16 gates ($1/2$ Switcher).

3. The delay elements for the DCD signals are not linear

4. Common mode calculation assume 256 Pixel connected to the DCD, so the common mode is divided by $N = 256$. Having less pixel connected (like 128 in Hybrid 5 or 250 in the final modules) underestimates the common mode.

5. The DHP02 PLL is very voltage sensitive. When switching between acquisition state and the idle state the current consumption changes, possibly breaking the link due to voltage drops. This can be mitigated by (a) carefully adjusting the voltage, (b) good connection between power supply and

DHP02, including decoupling capacitors close to the DHP and (c) checking after every switching if the channel is up. Since the current also changes when triggering, an effect like this can happen during data taking if the PLL voltage is close to the limit. For optimized setting, the link is very stable during data taking.

6. The offset DAC data sent to the DCD is only updated in normal acquisition mode. No raw data pedestals can be taken using offset DACs.

7. Every time the DHP02 changes its state, some part of the offset DAC memory gets overwritten by data from a different address. This creates either insensitive or noisy pixel in one gate.

8. Output of offset DAC data stops directly when receiving the JTAG command, while data taking continues to the end of the frame.

9. Changing from acquisition state to memory dump state produces a frame with zero suppressed header and raw data, requiring to go into idle state first, increasing the possibility to lose the link.

The issues 5 – 9 were found in the scope of this thesis. Due to the issues with the current generation and the request for additional features, a new version was developed.

5.3.2 DHPT1.0

The DHPT1.0 is the first ASIC used in high energy physics produced in a 65 nm technology. It is a close to final prototype for Belle II. With smaller feature size (65 nm vs 90 nm on DHP02), more memory and more complex logic could be implemented while having same size, similar power consumption and compatible footprint:

- The internal FIFOs could be increased in size. FIFO1 increased from depth of 16 to 256, FIFO2 is increased to from 512 to 4096 words. In addition, the layout of FIFO1 changed: In the DHP02, FIFO1 stored complete rows, regardless how many hits a row had. In the DHPT, FIFO1 consists of 64 FIFOs, one per sensor column. Only hits are stored in the individual FIFOs, making it possible to store more than 256 rows in FIFO1 without data loss (unless 256 consecutive hits are present in the column).

- Two pedestal memories are available. Both are laid out as dual port memory so they can be written during operation. This allows updated pedestals to be loaded into one memory while the other pedestals memory is used for data acquisition. When finished, a JTAG register is used to switch between both memories.

- The DHPT1.0 logic operates continuously, no states are used. Triggering the system does not change current consumption.

- The DHPT1.0 has memory for arbitrary Switcher control sequences instead of a sequencer. A second Switcher control sequence memory is present. The Switcher control signal can be used to toggle alternative matrix operations on special rows.

- The trigger line uses Manchester encoding to transmit multiple signals (fsync, trigger, Switcher control, memory dump trigger) over a single line. This includes the control for full memory dumps which was previously state based and therefore very slow.

- The clock output buffer is stronger and a differential clock output is available so that DCD operation at the target frequency is possible.
- Linear delay elements are present at all signals from and to DCD and Switcher, except for slow control.
- The number of pixels in each gate can be reduced by masking drain lines. The division in the common mode calculation only takes into account pixels which are connected.

The new DHPT1.0 improves all issues seen in the previous version and increases the maximum possible sensor occupancy which can be read out with no data loss. It needs less interface lines to the back end while providing additional working modes . Some issues remained which were fixed in subsequent chip versions but had to be dealt with in the test system used in this thesis.

- The serializer in the high speed link has a timing problem resulting in scrambled data. Using a higher supply voltage of 1.54 V instead of the nominal 1.2 V mitigates this but is outside of the specification, potentially reducing the lifetime of the DHPT1.0[13]
- If the high speed link uses clock compensation, parts of the data in $\frac{1}{16}$th of the memory could be shifted by one gate. Depending on the high speed link data rate, this could happen ≈ 0.1 % (normal data rate) or ≈ 50 % (half data rate) of the cases.
- When switching into the alternative Switcher sequence, the first 32 bit of the sequence are repeated twice
- The data receivers for DCD data have strong electrostatic discharge protection. This results in a large capacitance of the receiver and too slow signal rise times. This was found out during measurements presented in 6.6. In addition, the signals duty cycle is distorted due to hysteresis in the data receivers which amplify the asymmetric signal rise times of the DCD. Another source of duty cycle distortion are asymmetric delay elements after the receiver. To get error free communication between DHPT1.0 and DCDBv3, the delay values had to be manually changed and the DCD digital supply voltages needed to be increased. In addition, the V_{ref} reference potential provided by the DCD had to be adjusted using a potentiometer. More on DCD and DHP communication can be found in 6.6.

A more in depth list can be found in [56].

5.4 Software

To perform measurements on different devices, readout and steering software is needed. For automated switching of bias voltages, a power supply software supporting different devices and (potentially) hardware interfaces was developed.

5.4.1 Slow Control

Slow control software is needed to configure the ASICs on the Hybrid boards and set the working modes of the FPGA readout boards. For each of the systems used had its own control software. For ADC measurements using Hybrid 5, an combined slow control and data acquisition "DCDtestapp" was used,

[13] No DHPT1.0 broke down during the thesis

mainly developed in [47] and modified for faster and more automatized tests in the scope of this thesis. For Hybrid 5, the "DHP Config GUI" developed in [49] was used. Hybrid 6 was controlled by a DHE and a prototype of the final Belle II slow control system was used. It is based on **E**xperimental **P**hysics and **I**ndustrial **C**ontrol System (EPICS)[14] and consists on severs which allow access to the slow control settings over network and which publish slow control data. Using EPICs, measurement software can configure the system and perform calibrations and measurements. In the scope of this thesis, multiple python based measurement programs were written. Manual configuration of slow control variables is possible using command line tools or GUIs built in **C**ontrol **S**ystem **S**tudio (CSS)[15].

5.4.2 Data Acquisition

During this thesis the BonnDAQ readout software receiving data from the DHHemulator, an ONSEN prototype[16], the DHE and the DHC and was developed. It receives device data over Gigabit Ethernet, features saving data to disc, spying on live data for online monitoring and receiving a complete copy for integration in the EUDAQ framework[17] during beam tests. Since several different readout systems needed to be developed, care was taken to make code reusable. This lead to a multi threaded design using different threads with different tasks.

1. A device thread is receiving data from the connected readout systems, creating full device events and checking data integrity. The implementation differs for each readout system.
   - The DHHemulator sends raw DHP frames using UDP with an trigger number appended. Main challenges for the device thread were receiving up to 625000 (mainly empty) data packages and event building. For small events (<500 byte), the trigger number was updated in frames transmitted after the data frames belonging to the event. For big events this could sometimes change. In addition, some operation modes do not change the trigger number, so artificial trigger numbers had to be created and events had to be separated without using the trigger number.
   - DHE and DHC send single detector events using multiple UDP packages. A DHE event consists of a start of DHE message, at least one data message and an end of DHE message. Each message is transmitted using one or multiple UDP packages. A DHC event consists of a DHC start of event message, followed by one or multiple DHE events and a DHC end of event message. The device thread ensures data integrity by checking for sane message sequences, correct checksums and matching DHE/DHC event meta data. Since UDP is not reliable, packet drops need to be handled. Message sizes are only implicitly transmitted by the UDP packet size. To be able to read multiple messages from a stream, messages need to be embedded in a data structure which allows reading from files. For this, the format used by the ONSEN prototype is used. All data structures are discribed in Appendix D. The device thread can (optionally) insert dummy frames to keep synchronization with outside systems in case of lost or damaged messages.
   - The ONSEN prototype sends DHE messages with headers over a TCP stream. The device thread needs to find initial synchronization and then separate between events after the correct

[14] `http://www.aps.anl.gov/epics/`

[15] `http://controlsystemstudio.org/`

[16] The ONSEN device thread was mainly developed by the working group of Prof. Dr. Wolfgang Kühn, University of Giessen, integrating this thread was done as part of this thesis,[57]

[17] The EUDAQ framework is used for data taking of Mimosa telescopes at beam test facilities, `https://github.com/eudaq/eudaq`

DHE/DHC messages arrived.

2. An event builder thread combines multiple devices into one data stream. This thread was mainly written by S. Furletov [58]. Since the DHE and DHC combine data streams in hardware and lab setups only use a single device, support for this was dropped in the DHE and DHC version of the readout software.

3. A data distribution thread allows user to get a copy of received data. This is important for online data quality monitoring and for integration in the EUDET telescope. This thread creates a server where clients subscribe to. The software supports three kinds of subscriptions: The user can subscribe for a single event, for a continuous stream of events or for a exclusive continuous stream of events. Subscribing to single events is rather slow but ensures that the event received by the subscriber is always a recent one. The difference between the exclusive and non-exclusive stream of events is that the software will create back pressure if an exclusive subscriber can not keep up, but silently skip events for an non-exclusive subscriber which can not keep up.[18].

4. A file writer thread stores data to disc. It supports explicit file names, can name files by run number, keeps track of current run numbers and split files beyond a certain size. Files can be compressed using the BLOSC 1.0 format[19]. Depending on the arriving data rate, data is compressed with either ZLIB (slow, good compression) or LZ4 (fast, weaker compression). Depending on the input data, this results in compression rations between 2 and 10[20]. File compression and explicit file naming is only available on BonnDAQ for DHC and DHE.

5. A control thread allows interaction with the software sending commands using TCP. The DHE and DHC version also allows querying statistics and error counters.

For ONSEN and DHHemulator, the threads were started in separate processes and communicating using sockets (and shared memory)[21]. For DHE and DHC, an easier to use single process solution was developed. Features existing in the previous framework were rewritten in C++11 and unified in a single executable.

Data can be accessed using a C++ class and a python plugin. The python plugin consists of Cython code wrapping and accessing the C++ code so that the python implementation is fast and always consistent with the C++ code. For files and live data, users can select whether they want to read data from a specific or from all DHEs and if they want to read data from a single or all DCD/DHP pairs. Files can be read using a filter accessing zero suppressed, raw or all data data. Multiple subscriptions to a single data server are possible. This was tested with up to 10 simultaneous connections[22].

A description of the data format used by the BonnDAQ readout software can be found in Appendix D.

[18] Currently there is no possibility for BonnDAQ to create back pressure on DHE and DHC. The backpressure is only applied to the device thread so that its buffers are used and the user notices the back pressure

[19] `https://github.com/Blosc/c-blosc`

[20] Examples for good compression: Recording single ADC transfer curves: 10x compression. Zero suppressed source data: 2.3x compression. Reading DCD test pattern: 100x-300x compression. Reading pedestals using ZS data: 3.8x compression (almost reducing the complete overhead). Reading pedestals using memory dumps: 1.3x compression.

[21] This software was initially developed by S. and J. Furletov. It features an event builder but no complex file naming, no file compression and no statistics and error counter. During this thesis, the receiving and controlling part for ONSEN and DHHemulator was developed and implemented in the existing architecture

[22] The theoretical maximum depends on the number of file descriptors allowed by the system and the amount of available memory, since each connection creates a buffer.

5.4.3 Data Quality Monitoring

For usage in beam tests, a simple **D**ata **Q**uality **M**onitor (DQM) was developed within the scope of this thesis. The DQM connects over network to BonnDAQ and receives a subset of the events. It clusters data and can mask noisy pixel. The data is used to create hitmaps and several histograms: The cluster signal spectrum, the seed signal spectrum and histograms containing the common mode, a number of firing pixel, the cluster size and a histogram showing the number of pixel against their occupancy.

The near instant availability of DQM data has proven extremely useful during beam test and for lab measurements.

5.4.4 Power Supply Control Software

A software was written to remotely control power supplies needed for DEPFET operation. Up to 9 power supplies are needed to power one test system, with convenient access not always possible. The current implementation allows usage of 3 different power supply types (TTi QL355TP in Version I and II, Hameg HMP4040, TOELLNER TOE8842-32 and TOELLNER TOE8842-130), which are connected to the PC via USB[23] or serial port. Each channel can be named and controlled by connecting the power supply to a command server using TCP. Using this, automatic startup sequences for Hybrid 4 modules were realized. The applied and measured voltage, applied and measured current as well as the device status is read by the software and can be logged to text files. Examples for this are shown in chapter 6.3 and 6.4.

The custom-made Belle II PXD power supplies were used to power Hybrid 6. These power supplies are built for usage in a rack. For lab usage, they need a primary power supply; similar is true for the DHE and some breakout boards. Controlling and switching these in remote lab setups is performed using this software.

Hybrid 4 and Hybrid 5 were powered by TTi QL355TP power supplies. The same was done for Hybrid 6 before the custom power supply was available. This required up to 9 dual channel power supplies to be steered by the software.

[23] The devices used feature an internal USB to serial port converter

CHAPTER 6

DCD Measurements

The DCD is the first ASIC in the readout chain of a Belle II PXD module. Its main task is to digitize the drain current of the DEPFET. For this purpose it contains 256 ADCs whose performance is essential for the overall detector performance. Several **D**igital to **A**nalog **C**onverters (DACs) and two operation voltages influence the performance of the ADC and need to be optimized to achieve best performance. ADC discretization errors and quality criteria which are used for an optimization are discussed in chapter 6.1. The measurement setup is introduced in chapter 6.2.

Since the Belle II pixel detector will be operated in a high radiation environment, the radiation hardness of the DCD needs to be sufficient. This was tested in an irradiation campaign in Karlsruhe using X-rays with an endpoint energy of 60 keV. The results of these measurements are presented in chapter 6.3. At Belle II the pixel modules will be mounted on a cooling block which will be cooled to $-25\,^{\circ}$C , so the temperature of the DCD is expected to be around $30\,^{\circ}$C. During lab usage, the DCD is mounted on a PCB at room temperature and can heat up to $55\,^{\circ}$C - $70\,^{\circ}$C, depending on settings and convection possibilities around the DCD (open setup, closed aluminum box, plastic cap over the DCD). The optimizations and tests are performed at room temperature if not stated otherwise. Chapter 6.4 presents measurements performed to check for performance deterioration at different operation temperatures. All these measurements were performed on a standalone DCDBv2 and are summarized in chapter 6.5.

Using the DCDBv3pipeline, the communication with the DHP[1] was checked and rise times of signals between DCD and DHP were investigated. These measurements are summarized in chapter 6.6

6.1 ADC Discretization Errors and Optimization Parameters

An ideal linear ADC can be characterized by the following properties:

- The number of discrete output values, typically given as the number of bits in the output code.
- The current increase needed to increase the output code by one. This is called the LSB width.
- The offset, which is the input current producing the ADC code 0.

The DCD features 8-bit ADCs[2] and switchable input subtraction current sources, so it has a switchable

[1] DHPT1.0

[2] Internally, it features an 8.997-bit ADC, where the last bit is dropped, so that the effective number of bits is 7.994. The missing 0.003 / 0.006 bit result from the fact that the ADC can put out only 511 / 255 of 512 / 256 values. The conversion can not have the result -256 / -128.

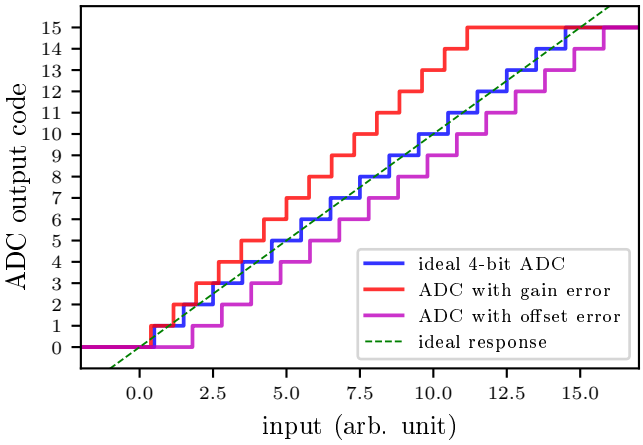


Figure 6.1: Transfer curves of a 4-bit ADC with gain and offset errors.
Blue: Result of an ideal 4-bit ADC
Red: Result of an ADC with gain error.
Magenta: Result of an ADC with offset error.

offset. The LSB width can be changed directly using DAC settings for the ADC and can be switched indirectly by using different gain settings for the TIA in front of the ADC.

6.1.1 Quantization Errors

The transfer curve of an ideal 4-bit ADC is shown in figure 6.1. Due to quantization, the reconstructed signal deviates up to $\pm 1/2$ LSB from the original signal. This leads to a quantization noise of

$$1/\sqrt{12}\,\text{LSB} \cong 0.289\,\text{LSB}.$$

6.1.2 Gain Errors

Figure 6.1 shows an ADC curve with a gain error. Gain errors are typically defined as deviations from a specified gain. Since the gain in the DCD can be set, the gain error of the ADCs in the DCD is defined as deviation from the mean gain. The dynamic range available for pedestals is typically limited by the ADC with the highest gain while the detection efficiency is limited by the ADC with the lowest gain.

6.1.3 Offset Errors

Similar to gain errors, offset errors are typically measured from the specified offset. This is shown in figure 6.1, where the dashed line denotes the expected response and the magenta line has a constant offset from the expected response. In the DCD the offset is switchable, so offset errors are deviations from the mean offset. The main reason for the offset errors is the spread of the input subtraction current sources (SubIn) and not the ADC. When subtracting larger currents with SubIn, the channel to channel spread of SubIn becomes wider. When reading out a DEPFET matrix, this adds to the pedestal distribution width. Therefore the offset is measured as the current at which the DCD measures the code zero. The offset error is then defined as the deviation from the mean offset from all measured curves.

6.1.4 Range Errors

An ADC with range errors will not put out all possible ADC codes, reducing its effective number of bits and its effective dynamic range. This is shown in figure 6.2. When reading out a DEPFET matrix, a smaller dynamic range can lead to the effect that some pixels have a pedestal current outside the dynamic range.

Hits in those pixels have a lower chance of being detected[3]. Signals of pixels with high pedestal values are limited to $\mathrm{ADC}_{\text{code max}} - \mathrm{ped}_{\text{code}}$. This lead to "dead" pixel if $\mathrm{ADC}_{\text{code max}} - \mathrm{ped} <$ DHP threshold or a loss in position resolution on multi pixel clusters.

6.1.5 Integrated Nonlinearity

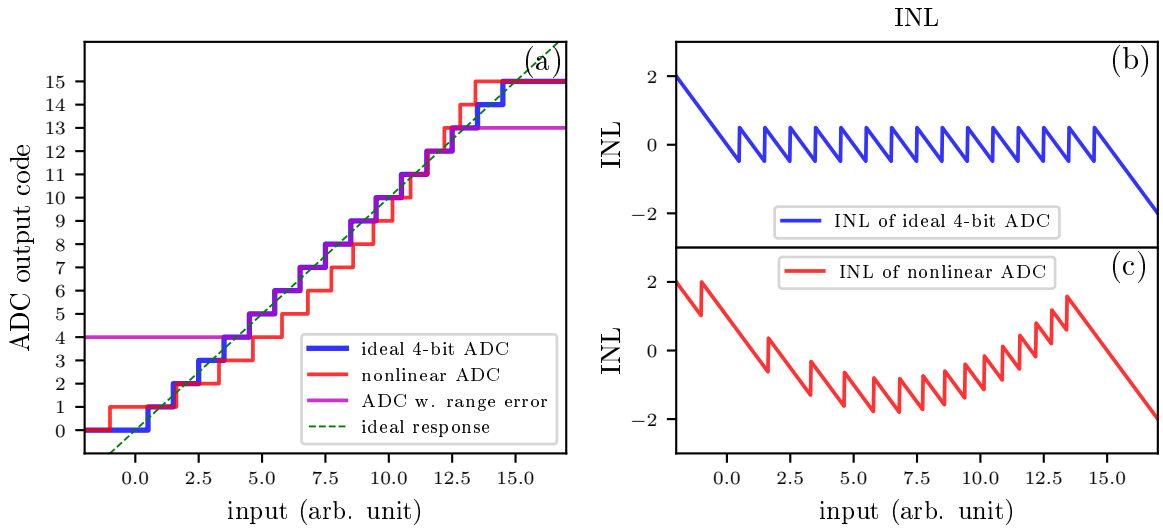


Figure 6.2: *(a)* Transfer curves for ideal and non-ideal 4-bit ADCs. The highest and lowest ADC code are the overflow/underflow bin. A transfer curve with limited range has different overflow/underflow bins. *(b)* INL is determined ignoring overflow and underflow bins. The INL of an ideal ADC is 0.5 LSB *(c)* INL for a nonlinear ADC curve without local defects.

The **I**ntegrated **N**on**L**inearity (INL) is a measure of the nonlinearity for the ADC transfer curve. It is defined as the maximum of the absolute deviation from the expected ideal response. Since gain and offset of the ADC are not fixed, the expected ideal response is estimated by a linear function:

$$y = a + bx \text{ with } b = \frac{\sum_{i=0}^{n}(x_i - \bar{x})(y_i - \bar{y})}{\sum_{i=0}^{n}(x_i - \bar{x})^2},\ a = \bar{y} - b\bar{x} \tag{6.1}$$

Some ADCs show nonlinear effects close to the lower end of their dynamic range. These would dominate the calculated INL, making it insensitive to other effects. To avoid this, the linear fit and INL determination is only performed on the inner part of the transfer function. Figure 6.2 *(a)* shows the transfer curve for both an ideal and nonlinear ADC. The INL curve for the ideal ADC is shown in *(b)*. Ignoring first and last ADC code, the INL is 0.5, which is the limit due to quantization. Transfer functions with nonlinearity create larger INL as shown in *(c)*. Large INL can also be created through local defects. These are explained in 6.1.6. When taking only one ADC measurement per input value, ADC noise will add to the INL. When taking multiple ADC measurements, noise can smear out the transition between ADC codes. Using the mean of the received ADC codes can seemingly improve the INL-value below the theoretical minimum. Using the median of the received codes will prevent this.

[3] If a pedestal is above the maximum ADC signal it is lost. Pedestals below the minimal ADC code may still be detected if they have a signal which is strong enough to get into the dynamic range.

During ADC measurements performed in this thesis, INL never got close to the theoretical minimum, therefore the mean could be used.

Bad linearity can make the signal s pedestal dependent since subtracting pedestal a from measured value $b = a + s$ assumes for the signal $I(s) = I(b) - I(a) \propto b - a$. If the absolute value of b is known[4], this can be mitigated by offline correction. Doing this would require significant computing resources, so a good linearity is preferred.

6.1.6 Differential Nonlinearity

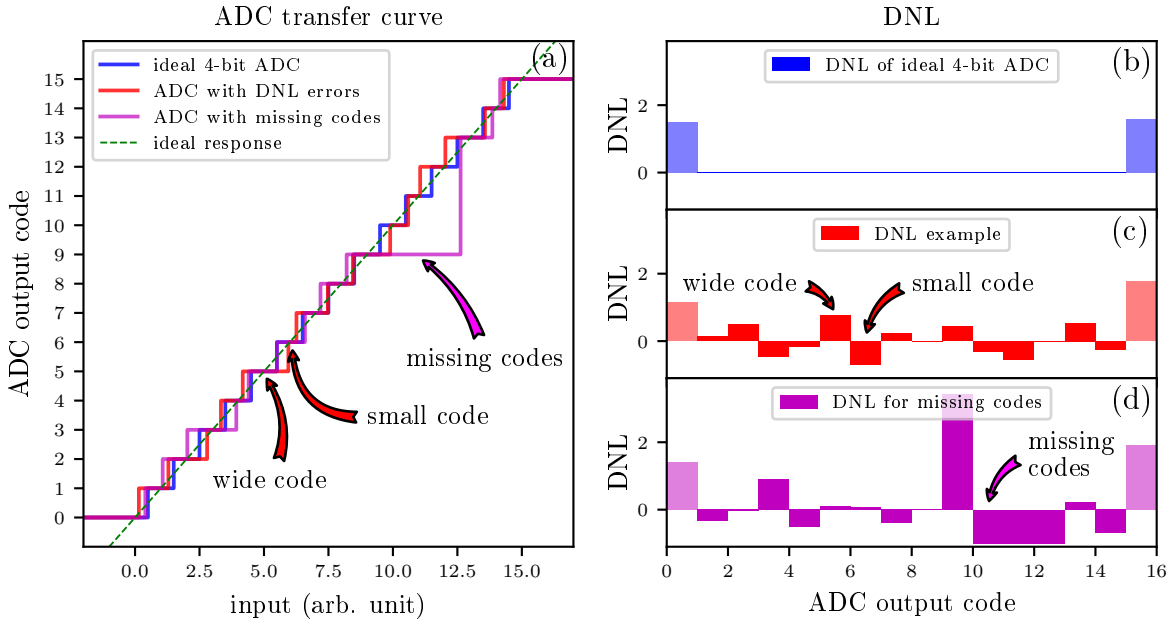


Figure 6.3: *(a)* Transfer curves for 4-bit ADCs with DNL errors. The highest and lowest ADC code are the overflow/underflow bin. *(b)* DNL is determined ignoring overflow and underflow bins. The INL of an ideal ADC is 0 LSB. *(c)* DNL for a nonlinear ADC curve without local defects. *(d)* DNL for a nonlinear ADC curve with a missing code.

Differential nonlinearity is another measure of ADC performance. Instead of focusing on the total deviation between expected and real transfer curve, DNL measures how much the width of each step deviates from the expected step width. It is defined as

$$DNL_i = \frac{\text{width of step i}}{\text{expected step width}} - 1.$$

Since the first and last ADC code are overflow bins, DNL is determined ignoring these codes. The minimal DNL is -1 (width of 0), on an ideal ADC, all codes have the DNL of 0. When characterizing an ADC, either the $max(|DNL_i|)$ or $min(DNL_i), max(DNL_i)$ is given. The DNL distribution of three ADC curves are shown in figure 6.3 *(b-d)*. Figure 6.3 *(b)* shows the DNL of an ideal ADC; *(c)* shows the DNL of an non ideal ADC curve. When using non optimal bias settings, the ADCs in the DCD show missing

[4] The absolute value of b can be reconstructed by the known pedestal a, the signal s and the amount of digitally corrected common mode noise in the DHP c as $b = a + s + c$. The common mode value is present in the data stream from the DHP but is currently planned to be discarded at DHE level

codes. In a DNL measurement this will show up as a high DNL entry next to several entries close to -1, as shown in *(d)* . During matrix readout, missing codes will show as noisy or insensitive pixel. Missing codes are easy to spot in DNL while in an INL measurement they can be masked by high nonlinearity.

Determining the width of individual ADC codes requires multiple current steps within each ADC code with high statistics, increasing the measurement duration and requiring low noise.

A faster measurement can be performed using a DNL histogram method. Using a varying input signal for the ADC, ADC codes are measured and a histogram of the measured ADC codes is calculated. Wider ADC codes will be measured more often than small ADC codes. Comparing the abundance N_i of each ADC code with the expected occupancy $\frac{1}{k}\sum_{i=1}^{k} N_i$, DNL can be calculated as

$$\mathrm{DNL}_i = \frac{\text{measured occupancy}_i}{\text{expected occupancy}} - 1.$$

Fast measurements typically use a sine wave as input [59]. Since the DCD measures current inputs and no dynamic current source (sine/ramp) was available, a current was ramped step by step and at each step a measurement was performed. The noise of both the ADC and the current source effectively smear out the input signal[5]. If the step size is smaller than the noise, this results in a homogeneous input signal distribution. In this case, the expected count of each ADC code is the mean of the ADC counts in all bins used for DNL calculation[6], so the DNL can be calculated as [60]

$$\mathrm{DNL}_i = \frac{N_i}{\frac{1}{k}\sum_{i=1}^{k} N_i} - 1. \tag{6.2}$$

6.1.7 INL from DNL

The INL of an individual ADC code can be calculated as the sum of all previous DNL values:

$$\mathrm{INL}_i = \sum_{j=0}^{i-1} \mathrm{DNL}_j. \tag{6.3}$$

This definition of INL is not directly comparable to the one described in chapter 6.1.5, since the expected gain for both is calculated differently: The INL of the first bin is 0 by this definition. Inserting equation 6.2 in 6.3 shows that the INL value of the last bin is also 0. Therefore, the INL value from DNL behaves like an INL where the expected function is the straight line defined by the first ADC bin as startpoint and the last ADC bin as endpoint. In comparison, the direct INL described in chapter 6.1.5 has a fit function as expected function. Both functions can be compared after removing the excess offset and slope from the INL from DNL function. The result of this is shown in figure 6.4, where *(a)* shows the measured transfer curve, *(b)* shows the DNL extracted from the data and *(c)* shows the resulting INL from both fit and DNL. As expected, both methods yield the same result, which confirms that the measured DNL values are correct.

[5] The main noise contribution of the DCD is the first current memory cell.

[6] Both overflow bins need to be discarded. In addition, Bins on the edge of the dynamic range were discarded because nonlinearities in these areas are not important for the DCD performance. In DCDBv2, the linearity at the upper edge of the dynamic range is good, the low edge will not be used since all pixels need to be within the dynamic range even with common mode noise

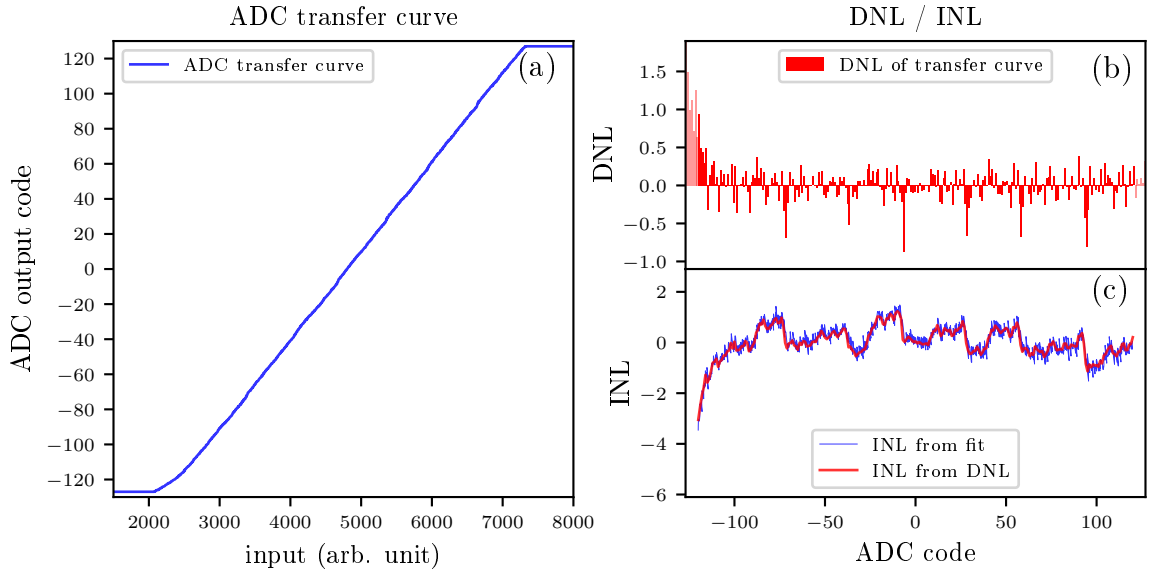


Figure 6.4: *(a)* Example transfer curve of DCDB3pipeline at good settings. *(b)* DNL of the transfer curve ignoring data outside of −120 to 120 LSB. *(c)* INL acquired with a fit (blue) and INL calculated from DNL (red). The fit method yields finer resolution but needs a known input current, captures noise and is influenced by the quantization noise. Both measurements yield comparable results

6.1.8 χ^2 as Quality Criterion

Using INL as an optimization criteria has certain drawbacks as INL only gives the information about how large the maximum deviation is and not how often large deviations occur. For DCDBv2, INL is typically dominated by the deviations at the lower end of the ADC transfer curve. A measure more robust against this is a modified χ^2:

$$\chi^2 = \frac{1}{n-2}\sum_{i=0}^{n}(y_i - a - bx_i)^2 \frac{1}{1\,\mathrm{LSB}^2} \tag{6.4}$$

$$\chi^2 = \frac{1}{n-2}\sum_{i=0}^{n}\left(y_i - \left(\bar{y} - \frac{\sum_{i=0}^{n}(x_i-\bar{x})(y_i-\bar{y})}{\sum_{i=0}^{n}(x_i-\bar{x})^2}\bar{x}\right) - \frac{\sum_{i=0}^{n}(x_i-\bar{x})(y_i-\bar{y})}{\sum_{i=0}^{n}(x_i-\bar{x})^2}x_i\right)^2 \frac{1}{1\,\mathrm{LSB}^2}. \tag{6.5}$$

The second line implicitly performs a linear regression to the data. This measure does differ from the normal χ^2 as it sets the measurement uncertainty implicitly to 1 LSB, resulting in the sum of squared differences at each point. Thus, χ^2 is a dimensionless measure how well the assumption of a straight line with a standard deviation of 1 LSB fits to the measured data. Small χ^2 values suggest that a standard deviation of 1 LSB overestimates the nonlinearity, large χ^2 hint to an underestimated standard deviation and thus a higher nonlinearity.

Squared differences between measured and expected values were chosen, because some large deviations from the expected curve are considered much more harmful than many small deviations.

6.1.9 ADC Noise

The ADC noise is a measure of how strong the correlation between a given input current and the measured ADC code is. It is measured as the standard deviation of the ADC codes at a given output code and is called "code"-noise for distinction during this paragraph. Typically, a low "code"-noise is preferable, but extremely low values close to zero can indicate problems. During detector operation the given output code needs to be translated into a current, so the ADC has a "current"-noise. For an ideal ADC this is $\sigma = \frac{\text{LSB width}}{\sqrt{12}}$, real ADCs have a higher "current"-noise, even if the "code"-noise at some input currents is 0. One problematic example of a low "code"-noise are missing/long codes. The currents in the range of the long code typically have a very low "code"-noise but the wide code has a large "current" noise. The current measurements close to the missing codes will show a high "code" noise, since the ADC will put out codes from below and above the missing ones. So both the high noise and low "code" noise values can indicate problems[7]. In this thesis noise refers to "code" noise when talking about ADCs.

6.2 Experimental Setup

Measurements on the DCD were performed with a Hybrid 4 and the Virtex 4 readout system. The DCD is mounted on a Hybrid4 PCB which is read out by the V4 FPGA board[34]. Current can be injected into the DCD before and after the TIA using a special input pad. The ADC in which current is injected can be selected using the configuration register of the DCD. The current for the measurement is supplied by a Keithly SMU 2400 and is selectable in the nA range. An additional filter[8] was used to remove noise from the regulation loop of the current source, which is in the kHz range and would result in artifacts in the data [61]. Transfer curves are recorded in a range between 4 and 26 µA with a step size of 50–80 nA. The data is recorded with an improved version of the DCDBTestApp[47], operation voltages were steered with the power supply software written within this thesis. For data analysis, a MATLAB framework was developed.

6.3 Radiation Tolerance of DCDBv2

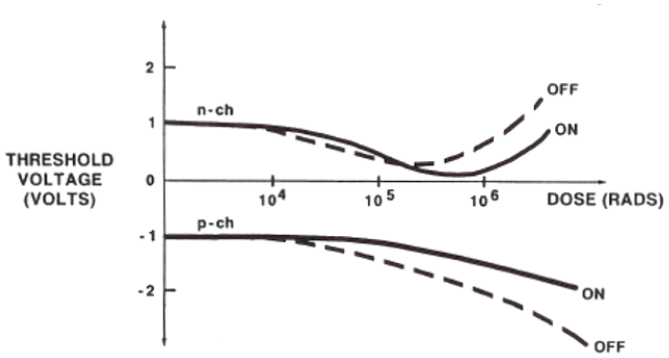


Figure 6.5: Representative plot of threshold voltage as function of radiation dose for pMOS and nMOS transistors. From [62].

[7] High "code" noise can also indicate strong nonlinearities. While a "code" noise of 0 can be achieved by a low noise ADC for an input in the middle of its bins, the 512 ADCs in the DCDs are optimized for low area and will show code noise for any input current, except in long codes and the overflow bins.

[8] RCR Filter, with a time constant of 10 msec

Radiation damage originates from ionizing and non ionizing energy loss processes. During the operation of the Belle II experiment, the main radiation damage for the PXD will be produced by ionizing radiation. Damage due to non ionizing energy loss is expected low enough to be ignored for ASICs [38], due to the fact that e^+, e^- beams are used. Ionizing radiation passing the device creates electron hole pairs. Part of the electron hole pairs will be created in the silicon oxide (SiO_2). The part that does not recombine is called electron hole pair yield. Electrons have a high mobility in SiO_2, so they can leave the oxide while holes can be trapped in the SiO_2. In addition, radiation forms interface states at the SiO_2/Si interface which can trap charge carriers. Both effects lead to a net charge-up of the oxide. The charges change the gate potential in the transistor channel, resulting in a threshold voltage shift. Thin oxides have higher sheet capacitances, thus the threshold voltage shift for the same trapped charge is smaller. Since charge transport, electron hole pair yield and trapping processes depend on the applied bias voltage, the devices need to be irradiated while being biased like in the final experiment [62]. This can be seen in figure 6.5, where the threshold voltage shift is shown for pMOS and nMOS devices biased on and off during irradiation. The behavior of pMOS and nMOS transistors is quite different. In pMOS transistors holes are charge carriers. Thus, trapped charge carriers have the same charge as trapped holes in the oxide and shift the threshold voltage in the same direction. In nMOS transistors, charge carriers are electrons and thus have the opposite charge of trapped holes. Since holes are trapped quickly compared to the formation of interface states, an nMOS transistor typically[9] first shows a negative threshold voltage shift and a positive voltage shift at higher doses. This results in a critical dose window. For the DCD this critical dose window is in the range of a few 10 kGy where the performance can degrade. Radiation damage from ionizing radiation anneals over time. The rate of annealing has a strong temperature dependence, where warmer devices anneal much faster.

The PXD is expected to experience a dose of 18 kGy yr^{-1}, which will result in a total ionizing dose of 200 kGy[10]. To ensure proper operation, all detector components need to work up to this dose. Thus, several components were irradiated and then tested.

- A radiation test of a matrix prototype was published in [63] and [64]. Having not the final oxide and nitride thickness and not the final layout, the result of this prototype is expected to be worse than for the final modules.
- Parts of the DHP were irradiated and its memory cells were checked against SEU errors in [49], its analog parts were irradiated in [65] up to 1 MGy.
- The switcher was irradiated to a dose to 245 kGy [48].
- The prototype DCDBv2 was irradiated as a part of this thesis up to 200 kGy.

6.3.1 Irradiation Measurement Setup

The DCD was irradiated at KIT using X-rays with an endpoint energy of 60 keV. It allows focused irradiation, an area with the diameter of ≈ 1 cm[11] was irradiated to have a good homogeneity across the DCD. To ensure the operation of the DCD during its complete lifetime, it was irradiated in multiple steps

[9] Depending on the device and enviromental factors, one of the two effects in an nMOS transistor can be dominant, so that it shows a purely positive or purely negative threshold voltage shift.

[10] This neglects the ramping of luminosity over time. While radiation is luminosity depended, it also depends on tuning of the machine, which probably will improve over time.

[11] The distance to the radiation source (and therefore the diameter) is one way to change the dose rate. Thus the diameter was close to 1 cm, but changed for different steps

to ensure measurements with critical threshold voltage shifts for nMOS transistors. For each step, the following procedure was performed:

- The DCD was irradiated to the given dose. During irradiation, the DCD was running and its current consumption was monitored (see figure 6.11).
- After irradiation the hybrid board was unplugged and put into an oven for annealing. The DCD was annealed for 100 minutes at a temperature of 80 °C. During annealing, the DCD was not powered.
- After annealing the DCD was placed inside the X-ray machine again and characterized like described below. The X-ray machine was switched off during the characterization.

6.3.1.1 Optimization parameters

The bias voltages *RefIn* and *AmpLow* and the DAC settings Source_1 and Source_2 have a strong influence on the DCDBv2's performance.

AmpLow is the ground connection for the TIA and is used as low potential for several amplifiers in the ADC. It influences the dynamic range and the gain of those amplifiers.

RefIn is the reference potential used in the ADC. It is used as reference potential for the transconductors in the ADC. Both comparator and memory cell are reset to the *RefIn* potential after each step. The current going into the ADC is defined by the potential difference between the TIA and the ADC which defaults to *RefIn*. A too low *RefIn* potential will reduce the dynamic range of the ADC since current memory cell has not enough headroom between ground and *RefIn* to store the voltage corresponding to the current. Similarly, A too high *RefIn* may limit the current the TIA can source into the TIA since the potential needed to do this is above the dynamic range of the TIA. The amplifiers in the comparator and current memory cell depend on both *RefIn* and *AmpLow*, so the difference of those voltages is important.

Source_1 and **Source_2** define the reference current I_{ref} described in chapter 5.2.3, Source_1 being the ADCs reference current which is used in the current memory cells, Source_2 being the reference current which is used in the comparator. Both should be adjusted to the same current and are expected to strongly depend on each other.

During each characterization, a 2D scan was performed on both voltages, another 2D scan was performed on both DAC settings. During each 2D scan the other parameters were set to the pre-irradiation standard for comparability. Voltage values given are with respect to Analog GND, all voltages are sensed.

The performance of the DCD was determined by injecting an external current into a single ADC, varying it and recording the ADC response. This results in a transfer curve like shown in figure 6.4 *(a)*. From this data, quantities like gain, χ^2, INL, maximum noise and minimum noise were calculated for the ADC and setting.

6.3.2 Pre-irradiation Measurement

Figure 6.6 shows the result of a voltage scan, results from one ADC is shown in each column. Figure 6.6 *(a)*, *(b)* are gain and offset of the ADC curve. Their value is not an optimization criteria. Figure 6.6 *(c)* and *(d)* show INL and χ^2. Their value is the main performance criteria for ADC operation. Both result in very similar results with optimal (small) values at the same voltage settings. Figure 6.6 *(e)* and *(f)* show maximum noise and dynamic range of the ADC. Good setting should have full dynamic range of 255, high maximum noise is an indicator of missing codes and indicates settings which should not be

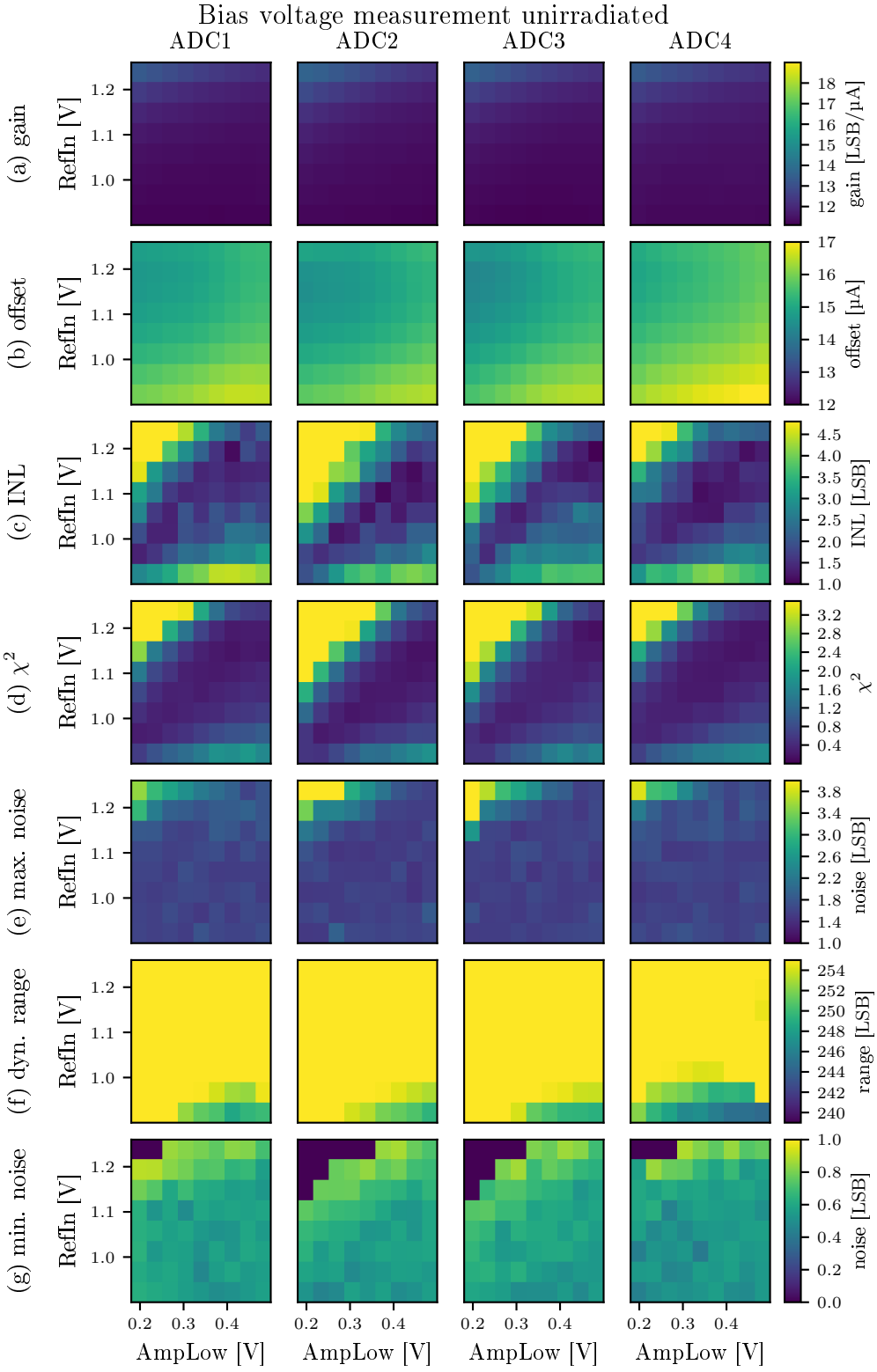


Figure 6.6: *RefIn/AmpLow* measurement results before irradiation using ADC values between −110 to 110 LSB for the linear fit and calculation of INL and χ^2. *(a)* and *(b)*: Gain of the transfer curve and current corresponding to ADC code 0. *(c)* and *(d)* INL and χ^2 are quality criteria using the maximum deviation and normed sum of squared deviations from straight line fit. *(e)* High maximum noise appears on discontinuities in transfer curve. *(f)* The dynamic range can be reduced by non optimal settings. *(g)* Low minimum noise appears at missing codes in transfer curve.

used. These plots show issues if *RefIn* is chosen too high (noise) or low (dynamic range). Figure 6.6 *(g)* shows the minimum noise within the measurement range. The low values at high *RefIn* and low *AmpLow* voltages is due to missing codes.

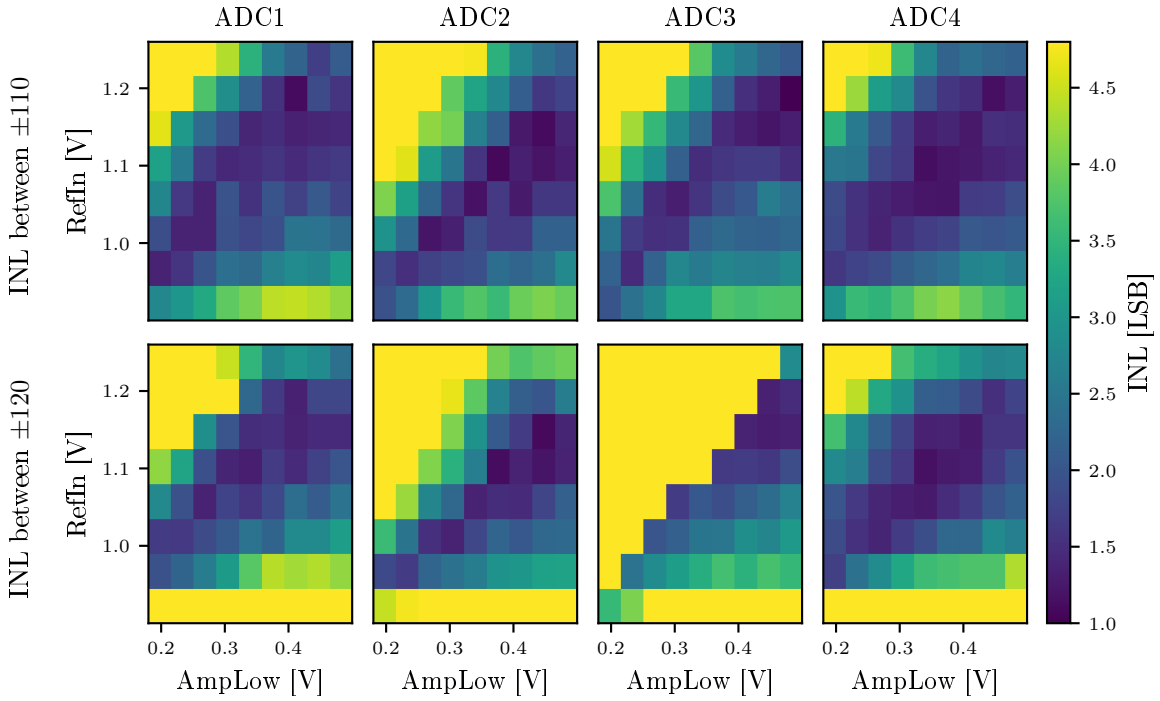


Figure 6.7: *RefIn*/*AmpLow* measurement results before irradiation. The *top* plots show the INL calculated for each ADC using values between −110 LSB and 110 LSB. The *bottom* plots show the INL calculated for each ADC using values between −120 LSB and 120 LSB. The optimal point found for each ADC is similar. Using wider cuts, INL increases due to non-linearities at low ADC values, especially for ADC 3. For further analyses, ADC values between −110 LSB and 110 LSB were used.

Figure 6.7 shows the INL for all ADCs which behave quite similar. The top four plots show the INL which was calculated using all values between -110 and +110, the bottom four plots show the INL for all values between -120 and + 120. Depending on the voltages, some ADCs show nonlinearities at the edge of the dynamic range. In 6.7, this is the case for ADC 3, which shows a very different result for the ±120 range than for the ±110 range.

These nonlinearities typically appear at the lower edge on the dynamic range, similar to the effects seen in 6.4 *(a)*, but more pronounced. Using a larger range for the calculation of INL and χ^2 increases the sensitivity for nonlinearities at the edge of the dynamic range. During detector operation, all pixels should have a pedestal value larger than the minimal ADC value to be distinguishable from pixel outside the dynamic range. Thus, almost no pixel should have very low ADC values. This limits the effect nonlinearities at the lower end of the dynamic range have on detector performance, hence the cut of −110 to 110 LSB (which includes 86 % of all ADC values) was chosen as a cut for the rest of the analyses. All measurement results for all four ADCs at all radiation levels can be found in appendix A. Several bias voltages can be found where all ADCs show a good operation with low INL, low χ^2, full range and no indication of missing codes, leaving a good operation window.

Expected values for a good ADC **Gain**: The ADC gain determines its dynamic range and resolution. It can be changed by different feedback resistors to increase two-, three- or fourfold. In addition it can be modified by different $\text{Source}_1/\text{Source}_2$ settings. The DCD was designed to feature a gain of $16\,\text{LSB}\,\mu\text{A}^{-1}$, but to cope with the pedestal distribution of a DEPFET matrix, a lower gain is needed. The settings used during all measurements were optimized for about $11\,\text{LSB}\,\mu\text{A}^{-1}$ on an nonirradiated DCD. Higher gain reduces the dynamic range (in μA), leaving less room for the pedestal distribution. Lower gain reduces the current resolution and decreases the signal measured from the DEPFET. Good gain values are 10 to $14\,\text{LSB}\,\mu\text{A}^{-1}$, which result in a dynamic range of 18.3 to 25.6 μA and a MIP MPV signal of 16 to 22 LSB, assuming $g_q = 400\,\text{pA}\,e^{-1}$.

Offset: The offset value is the current which corresponds to ADC value 0. Since it can be changed with internal settings, only the offset distribution width on the DCD is relevant, which should be smaller than a few μA. This was the case for all measurements.

Maximum noise: The measured noise is the convolution of the ADC noise and the noise of the current source. Localized effects like nonlinearities can amplify the noise at certain ADC values. The maximum noise measured at any input current should be as low as possible, with everything below 2.5 LSB being a good result.

Minimum noise: In the measured area between −110 to 110 LSB, the minimum noise should not be below 0.3 LSB, since very low values indicate long ADC codes which typically have a missing code in their vicinity.

Dynamic range: A good ADC should use its complete range; thus, the dynamic range should be 255 LSB.

INL and χ^2: INL should be below 2 LSB and χ^2 should be below 0.8 LSB to ensure good ADC linearity. A local nonlinear effect of 2 LSB increases the particle detection threshold by that amount, decreasing the sensor efficiency. INL is more strict than χ^2, so it serves as the main quality criterion. This can be done, since every time χ^2, gain, or noise flag an ADC transfer curve as problematic, INL does the same. INL does not reliably detect a slightly decreased dynamic rage, thus a crosscheck with this is necessary.

6.3.3 Measurements during Irradiation

The DCD was irradiated in steps to a total dose of 5 kGy, 10 kGy, 20 kGy, 35 kGy, 60 kGy, 100 kGy, and 200 kGy. The INL of the characterized ADCs for all irradiation steps are shown in figure 6.8, the dose increases from top to bottom. At 5 kGy the optimal point and performance are unchanged compared to the nonirradiated case, while the performance at high *AmpLow* voltages and low *RefIn* voltages increases. This effect continues at 10 kGy where most of the measured voltage combinations result in a good performance. One reason for this can be found in the Source_1 measurement. The strength of Source_1 changes due to radiation, which is visible in the gain of the ADC. As a result, the new $\text{Source}_1/\text{Source}_2$ working point allows more voltage combinations with good performance.

At a dose of 20 kGy unexpected effects appear. The analog part of the DCD cannot be switched off anymore using the JTAG configuration. The current consumption of the digital part is at $I_{VDDD} = 460\,\text{mA}$ instead of $I_{VDDD} = 260\,\text{mA}$ before the irradiation and the current consumption on the digital part starts to change depending on the bias voltages. The ADCs show a bad performance which is mainly due to a bad $\text{Source}_1/\text{Source}_2$ setting shown in figure 6.9. Since the characterization runs automatically using pre-irradiation settings as default, the bias voltage measurements use a far from optimal setting. Still the best DAC setting shows a reasonable performance even without voltage optimization. At higher doses, the default DAC setting gets closer to a good one and the performance seen in the voltage scans improves. At the same time, the current consumption of the digital part reduces. Starting with 60 kGy, the DCD

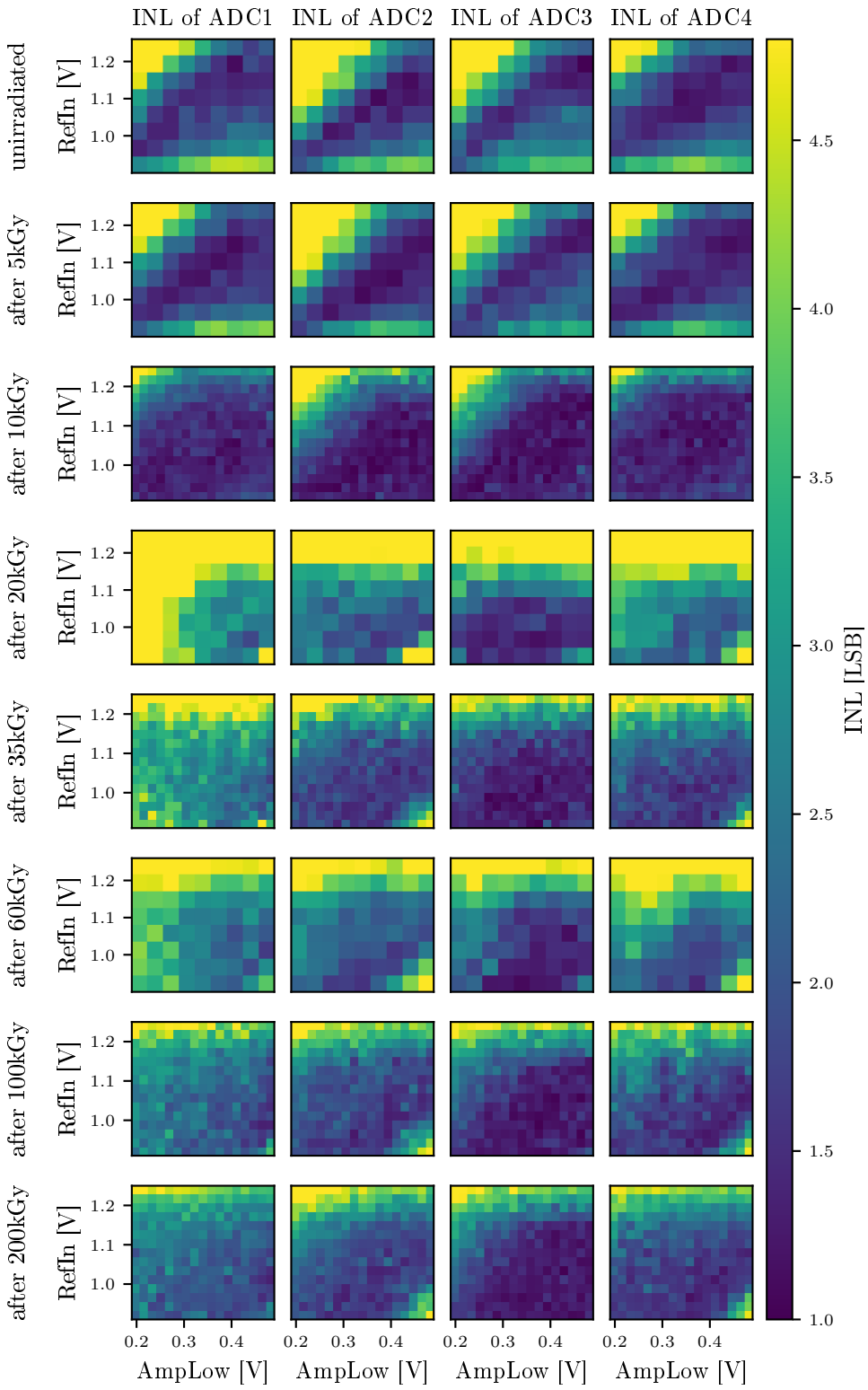


Figure 6.8: Summary of *RefIn*/*AmpLow* measurement results during irradiation campaign showing INL. Each row corresponds to one irradiation step, each column corresponds to a single ADC.

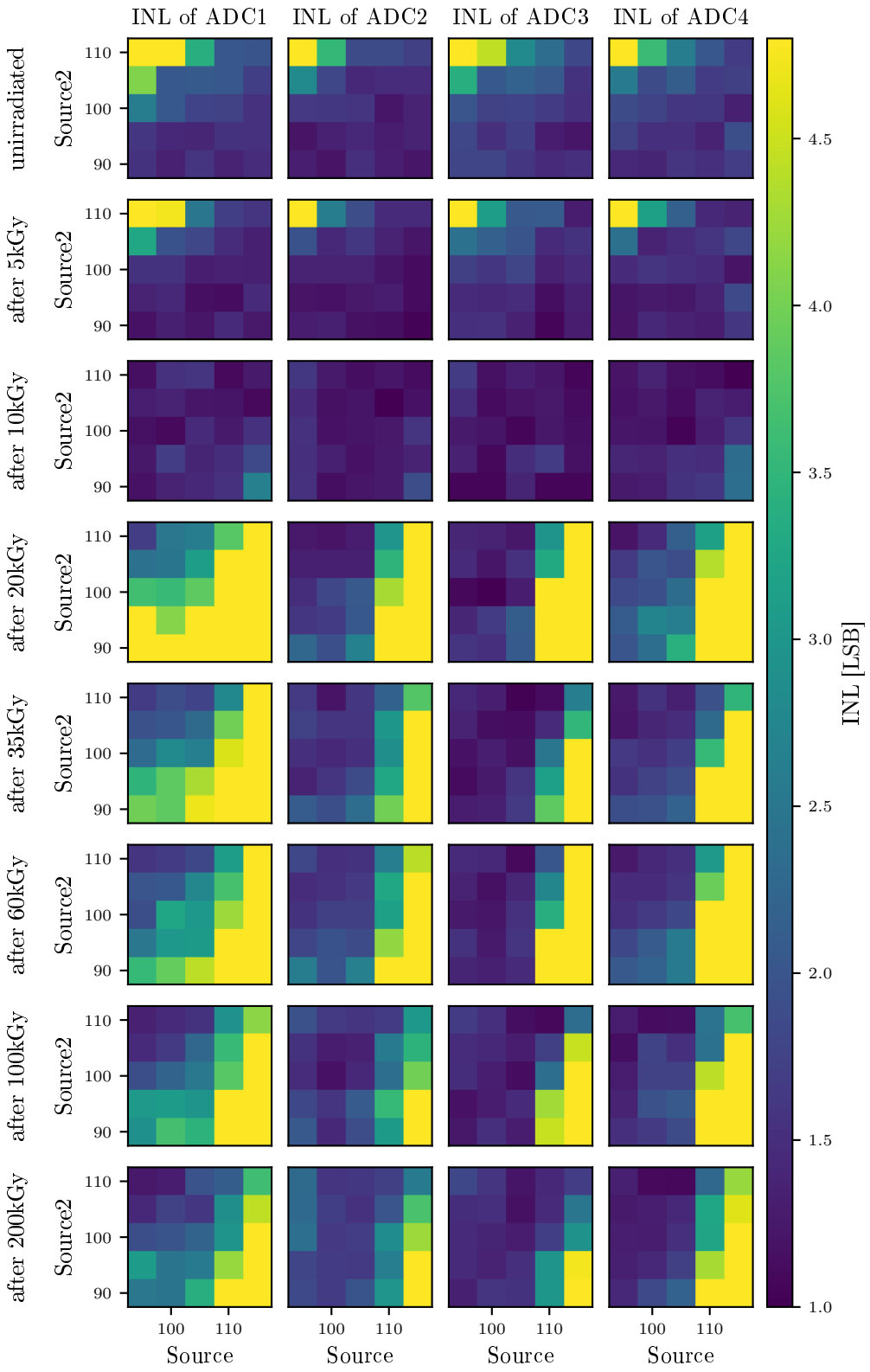


Figure 6.9: Summary of $Source_1$/$Source_2$ measurement results during irradiation campaign showing INL. Each row corresponds to one irradiation step, each column corresponds to a single ADC.

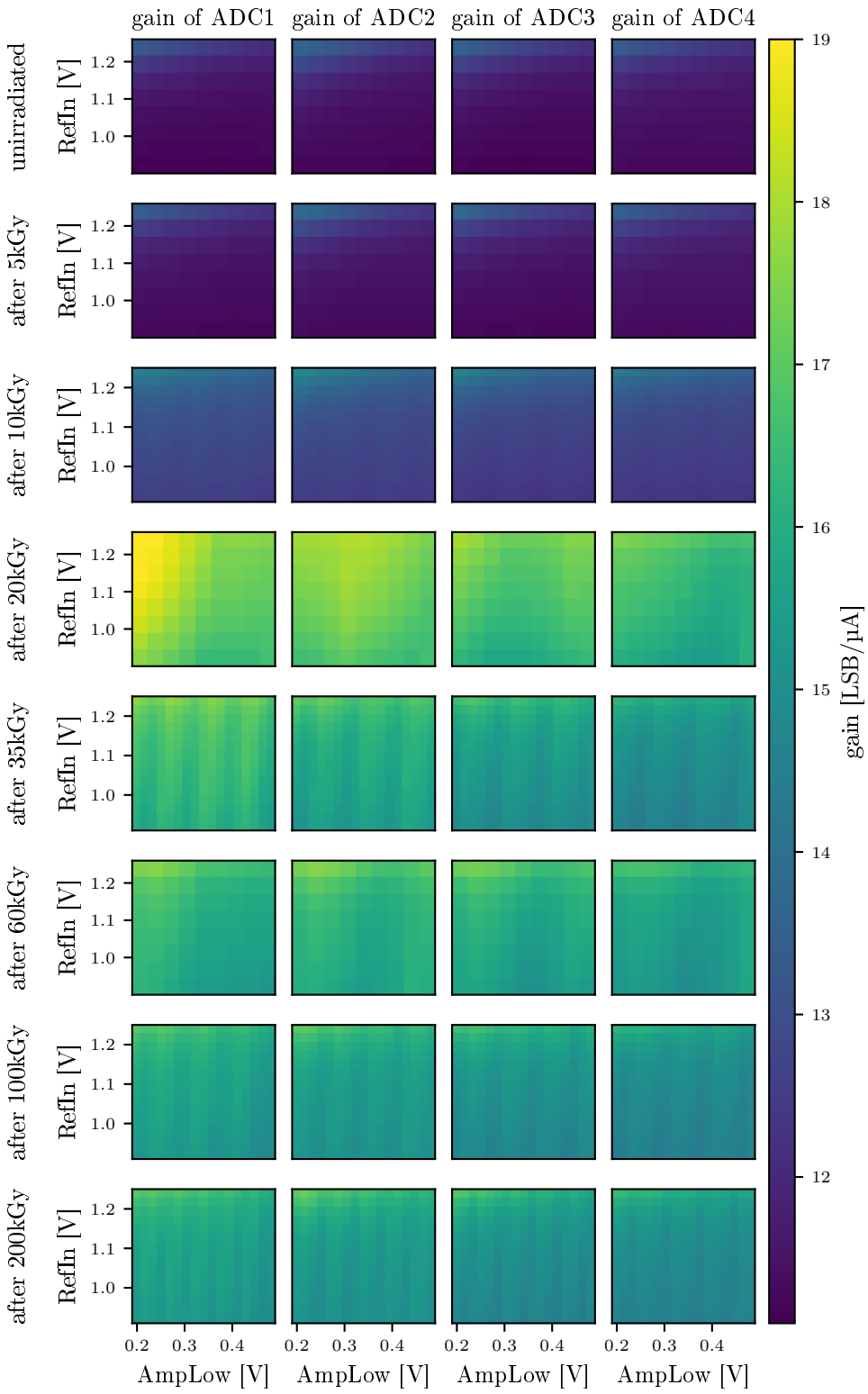


Figure 6.10: Summary of *RefIn*/*AmpLow* measurement results during irradiation campaign showing ADC gain. Each row corresponds to one irradiation step, each column corresponds to a single ADC.

reacts again to the on/off configuration.

Several measurements show a wave pattern in the gain measurement like shown in figure 6.10. It shows up in longer measurements (10 kGy, 35 kGy, and 100 kGy) and has a higher frequency in the measurement at 200 kGy. These wave patterns are an artefact of temperature fluctuations in the room[12]

6.3.4 Power Consumption during Irradiation

During the irradiation, the applied voltages and the current consumption of the system were recorded. The voltages are shown in figure 6.11 *top* and are constant except for some exceptions: *AmpLow* and *RefIn* are changing their values during the voltage scans. The DCD digital supply voltage (VDDD) ran into current limit several times. The current consumption of the ASIC is shown in figure 6.11 *bottom*. During characterization before irradiation, the DCDs digital current consumtion stays constant during scans over bias voltages and DAC settings. It only changes after each scan cycle when the DCD is switched in a different mode. The current consumption also stays constant before and after the scan. After the first irradiation the digital current is increased from 260 mA to 360 mA and slowly starts to decrease. This is more apparent after the second irradiation step where a longer characterization was done over night. A second increase can be seen after the 20 kGy irradiation step (320 mA to 480 mA), a third (very small one) can be seen after the 65 kGy step. After each of these steps the current seems to do an exponential decay over time. Starting with the 20 kGy irradiation, the digital current consumption starts to change when *AmpLow* and *RefIn* voltages are varied. This is unexpected, since analog and digital part of the chip should have separate power domains. The analog currents stay roughly the same during the irradiation. The *AmpLow* current and the VDDA current decrease a bit with increased dose, while the *RefIn* current gets a bit larger. These effects can be explained with a change in bias currents.

6.4 Temperature Dependence after Irradiation

In Belle II, the DCD will be operated at 30 °C, while all optimizations were performed at room temperature, without cooling, so the DCD was considerably warmer. To ensure good operation across a large temperature range, the system performance was checked at different temperatures. For this, the system was mounted in a climate chamber. Different ambient temperatures ranging between 30 °C and −30 °C were set while checking the relative humidity to be below 80 %. Due to humidity, lower temperatures could not be reached, while higher temperatures are no realistic scenario for detector operation. The chip temperature could not be measured directly because the climate chamber was too small to mount an infrared camera. Measurements at room temperature showed the ASIC temperature to be 35 to 50 °C above the ambient temperature, depending on the usage of a protective plastic cap (high temperature) and the airflow. The fan of the climate chamber produced a rather strong airflow, the ASIC was covered with a plastic cap with holes to allow some airflow. Due to this, the temperature is estimated to be (40 ± 5) °C above ambient, which translates the ambient temperature range to a chip temperature range of

[12] Measurements at different voltages were performed first for the lowest *AmpLow*/*RefIn* voltage pair, ramping *RefIn* and then *AmpLow*. This translates the frequency in the pattern into a time dependent effect with a frequency of 45 measurements for the characterization after 200 kGy. During the irradiations after 10 kGy, 35 kGy and 100 kGy the frequency of the pattern is lower, approximately 65-70 measurements. The difference between those measurements is the number of steps per ADC curve, which was higher during the characterization after 200 kGy, so that each measurement took longer. In both cases the effect has a time scale of 20-25 minutes. On an idle system, fluctuations in power consumption can be seen in a similar frequency (visible on VDDD in figure 6.11 *bottom left* at 2 days, 11 hours), which is in the timescale of a climate system regulation. Using a small climate chamber with a well-regulated temperature (like in chapter 6.4), an effect like this cannot be seen.

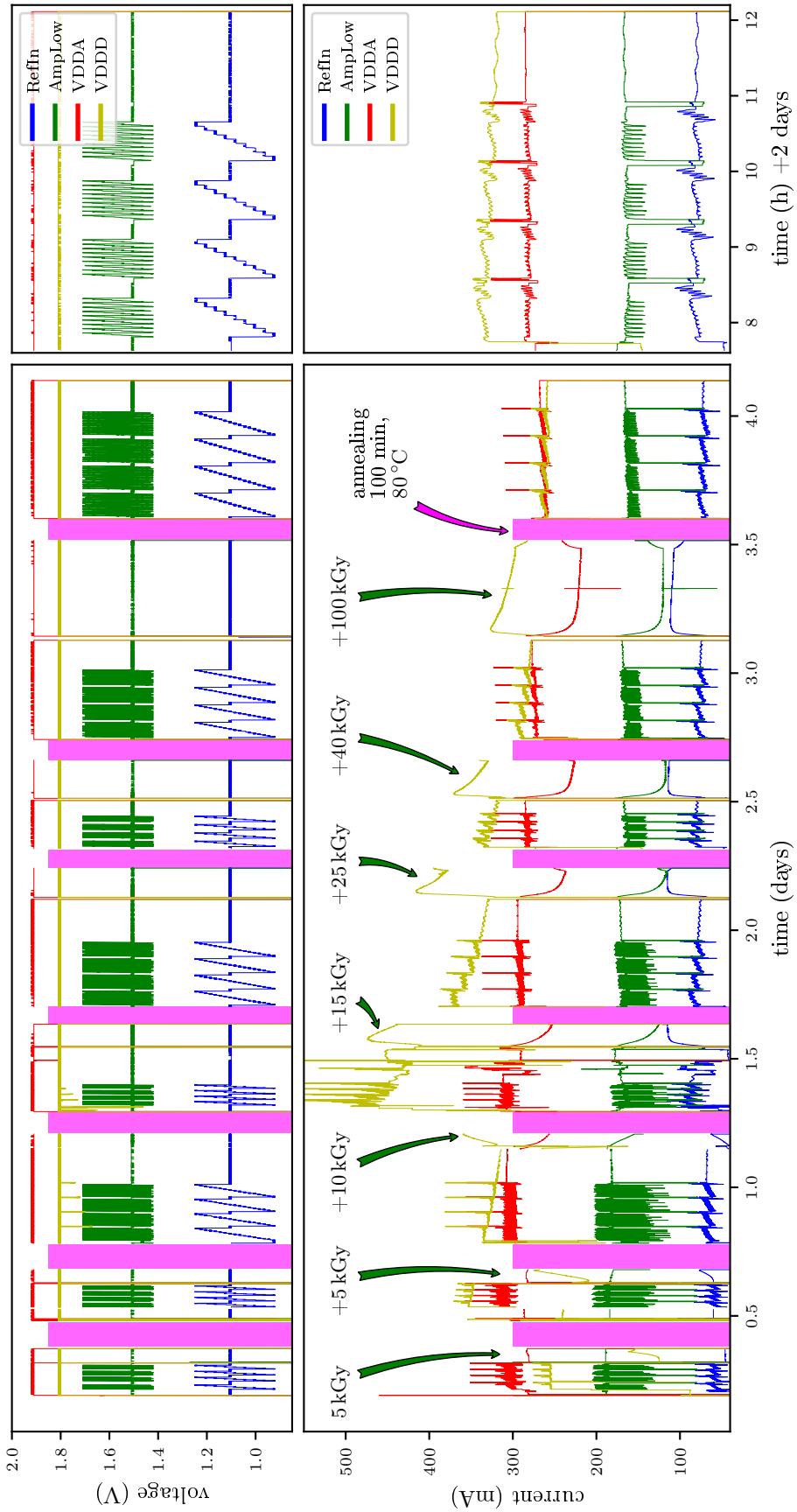


Figure 6.11: DCD voltages *(top)* and current consumption *(bottom)* during irradiation. Purple Boxes show annealing steps where the system was not connected. *(right)*: Zoom onto measurement performed after 6 kGy. During characterizations, *RefIn* and *AmpLow* are changed, resulting in varying current consumption. Four blocks are visible; one for each measured DCD channel. Different block length in the *left* plot is due to differences in voltage step size during scans and different current step size in the transfer curve. After the scan, the digital supply current keeps fluctuating on a time scale of ≈ 20 min.

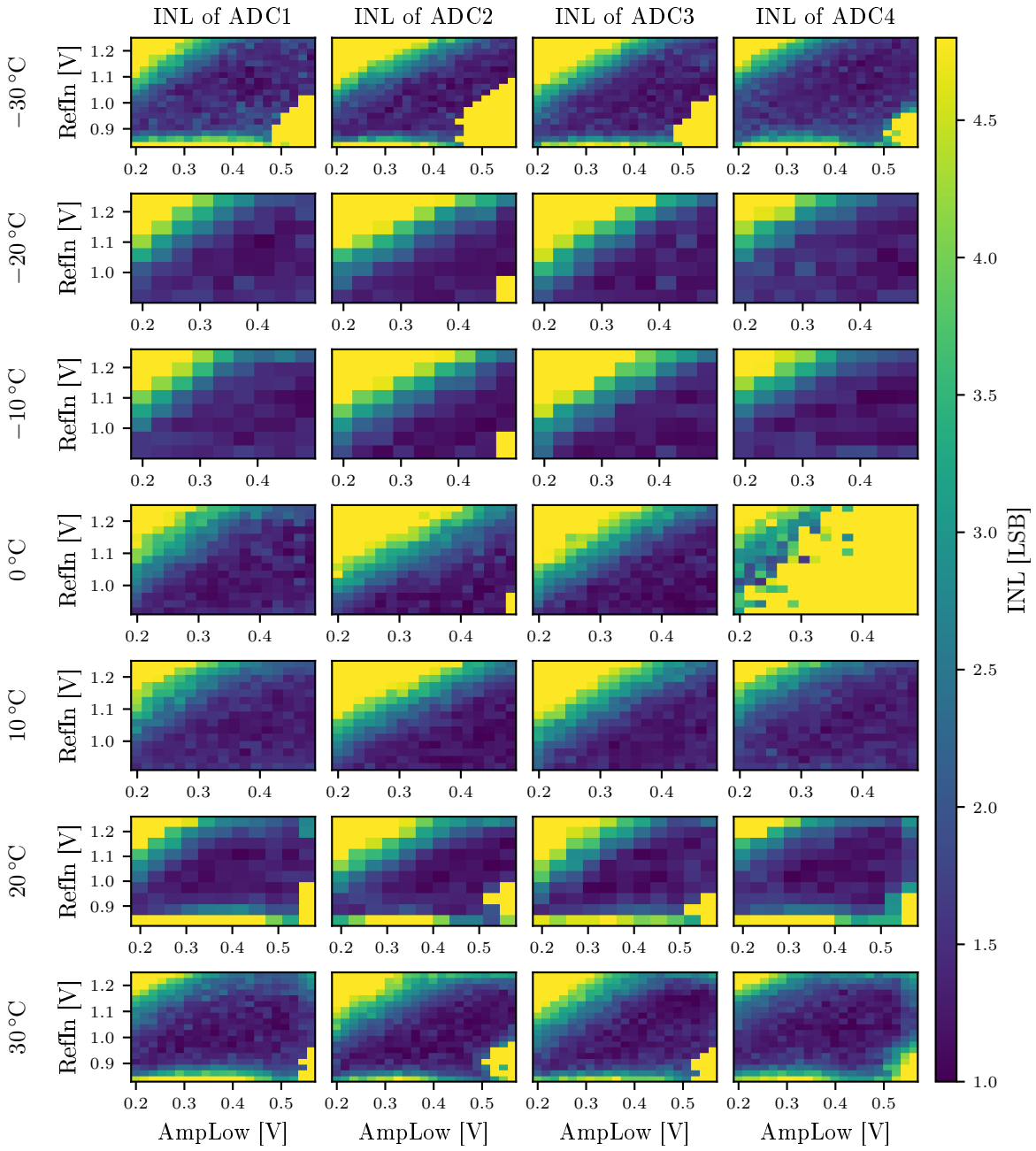


Figure 6.12: Summary of *RefIn*/*AmpLow* measurement results at different temperatures showing INL. Each row corresponds to one temperature, each column corresponds to a single ADC. The operation window is in first order independent of the temperature and a good operation region can be found for all temperatures. Note that −30 °C, 20 °C and 30 °C use different ranges for bias voltages.

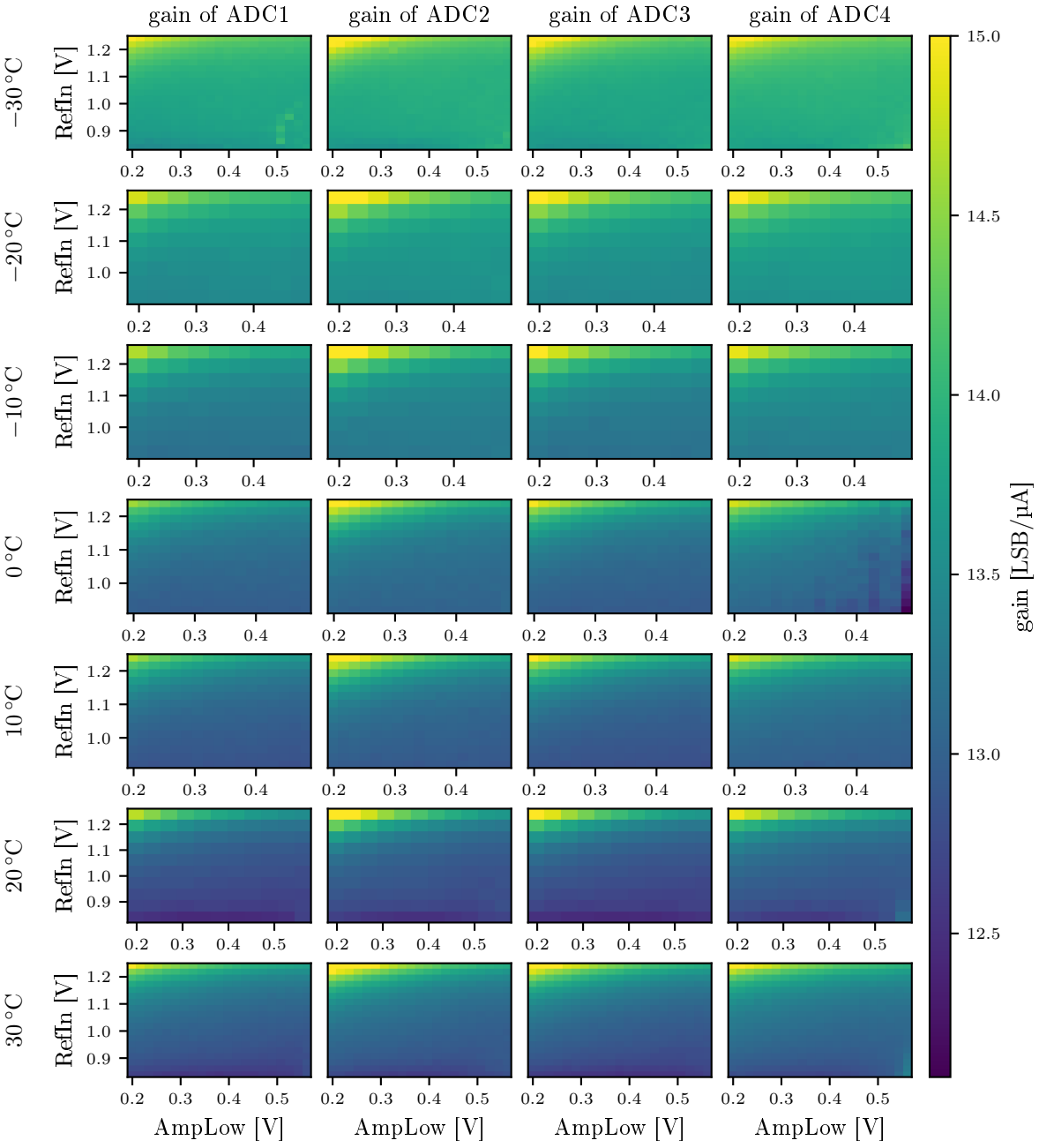


Figure 6.13: Summary of *RefIn*/*AmpLow* measurement results at different temperatures showing ADC gain. Each row corresponds to one temperature, each column corresponds to a single ADC. The observed gain is highest for the coldest setting. This is due to the not temperature stable current reference, which reduces the currents Source_1 and Source_2, which determines the LSB width.

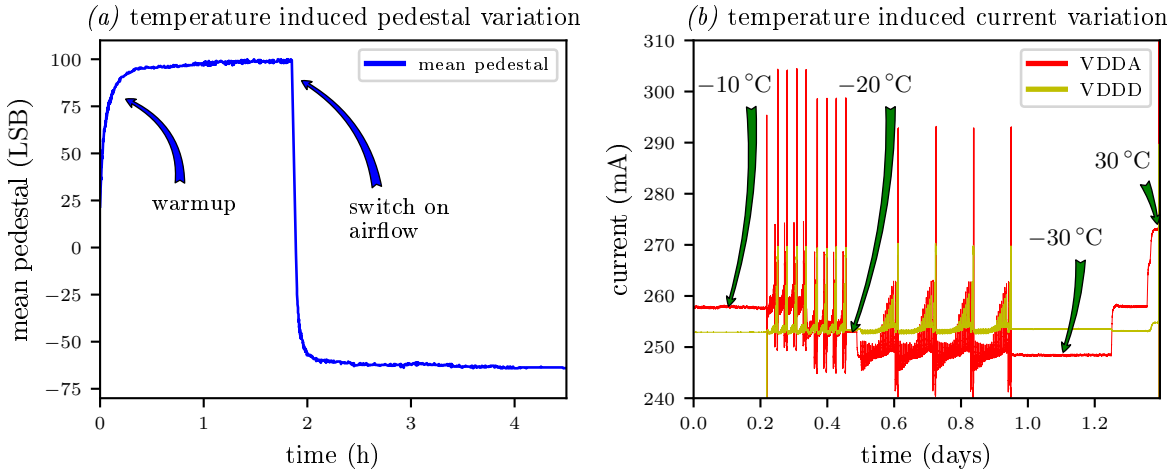


Figure 6.14: *(a)*: Mean pedestal measured by the DCD during warm up of the system and airflow change. Hybrid 4 has low thermal conductivity so warming the system takes hours until pedestals are completely stable. This measurement was performed on a different Hybrid than used in the irradiation campaign.
(b): Current consumption of digital and analog current during temperature scan with irradiated Hybrid. Switching the temperature results in a modified analog supply current.

approximately 10 to 70 °C with measurement steps every 10 °C. At each temperature, the characterization procedure used during the irradiation was performed. The result is shown in figure 6.12. The performance at different temperatures is similar in terms of noise, dynamic range, INL and χ^2, while gain and offset vary like shown in figure 6.13. The gain is dependent on the on $\text{Source}_1/\text{Source}_2$ setting, the offset is dependent on SubIn. All DACs in the DCD vary with temperature since the reference current of the DCD is not temperature stable. The consequence of a non-stable reference current is shown in figure 6.14 *(a)*, which shows the mean pedestal variation when changing the airflow over the DCD. SubIn subtracts typically 100 µA, while an LSB of the ADC is around 0.08 µA. So the stability needs to be better than 0.08 % to limit deviations to 1 LSB $^\circ\text{C}^{-1}$.

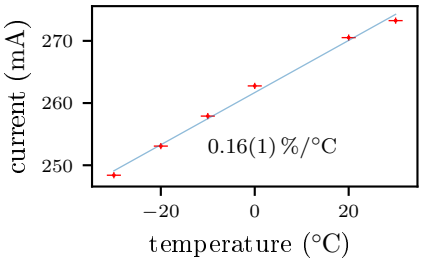


Figure 6.15: Analog current consumption of DCD at different climate chamber temperatures.

Differences in the temperature can also be seen in the recorded power consumption during the temperature measurements. At different temperatures the analog power consumption of the DCD changes. This is shown in figure 6.14 *(b)*. Clear differences between the power consumption can be seen. The current is measured at each temperature and shown in figure 6.15. In first order, the reference current should change linearly with the temperature. The measured data shows small deviations from linear behavior. Ignoring these yields a (0.16 ± 0.01) %/°C current change for the whole analog part. This is in reasonable agreement with simulations, which expect (0.140 ± 0.005) %/°C current change in the reference current [66]. To achieve a pedestal stability better than 1 LSB thus requires a temperature stability of better than 0.5 °C. While this is possible in detector operation with sufficient cooling, newer DCD versions feature a better reference current source with a maximum variation below 0.005 %/°C.

The first measurements were started 4 days after irradiation. During this time the system was at room temperature. Both the current consumption and the performance of the system changed over

this time. The analog current went from (267.0 ± 0.5) mA down to (265.0 ± 0.5) mA, the digital part went from (259.0 ± 0.5) mA down to (253.0 ± 0.5) mA. During the temperature scans, the current consumption on the digital part was almost independent of the the bias voltages again[13]. The performance is comparable with the performance after the 10 kGy irradiation while the current consumption is close to the consumption after 200 kGy. The change in the performance between the last irradiation and the first characterization in the climate chamber is probably due to incomplete annealing during the 100 minutes at 80 °C, as the DCD recovered while being unpowered for 4 days. Setting and setup differences can be excluded, as the setup was thoroughly replicated: The same power supplies were used for the same voltages, the same software and settings were used, just the location was different.

6.5 Summary of Obtained with DCDBv2

A successful DCD irradiation program was performed. At all radiation levels, a working point with reasonable performance can be found in the measurements of $\text{Source}_1/\text{Source}_2$. Due to the fixed DAC values for $\text{Source}_1/\text{Source}_2$, the performance during the bias voltages measurement is not optimal. The irradiation effects were enhanced due to temperature effects: The irradiated DCD used considerably more current, which changes its temperature and reference currents. The observed effects could be improved by optimized DAC settings.

The DCD was annealed at 80 °C for 100 min without biasing of the transistors. After that, it still showed performance changes over time, visible by gain fluctuations and variations in the current consumption. Further, the first ADC to be characterized after each setting shows considerably worse performance with doses at and above 20 kGy. Unirradiated and during all temperature measurements it showed comparable results to the other ADCs. Unirradiated, the DCD can reach temperatures of up to 70 °C; with the higher current consumption due to irradiation it is expected to be warmer than this. Thus, the temperature produced by the DCD is high enough to continue annealing, which might be the explanation of the performance variations after measurements.

After four days of annealing at room temperature, the irradiated DCD was successfully operated in a temperature range between −30 °C and 30 °C ambient temperature, corresponding to approximately 10 to 70 °C. Thermal simulations showed an expected DCD temperature on Belle II modules of 30 °C, which is well in this region [67]. At this time, the performance of the irradiated device was comparable to a nonirradiated device.

The main problems observed were

- The failure of the configuration bits in the DCD. As a result, several transistors in the DCD were changed from linear geometry to a more radiation hard circular geometry for the next chip generation

- The temperature sensibility of the DCD. A short term work around was the development of a PCB with better thermal properties and mounting space for a cooling block, as long term solution the next chip generation featured temperature stable reference current sources.

These issues were fixed in future ASIC generations, a repetition of the irradiation to validate the fixes has not yet happened.

[13] After irradiation, small changes were visible. After the irradiation, current was read out using a resolution of 0.1 mA, during irradiation the current was measured with only 1 mA, so it is possible that small changes were not visible during irradiation

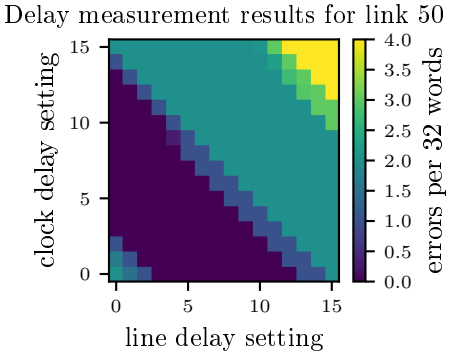


Figure 6.16: Measurement result for one of 64 data lines. The color code is the number of errors per readout cycle in dependence of the clock delay and the local delay. The test pattern of this bit produces two errors when off by one clock cycle. The small bands with one error are due to duty cycle distortion: Time constants for rising edges are smaller than for falling edges.

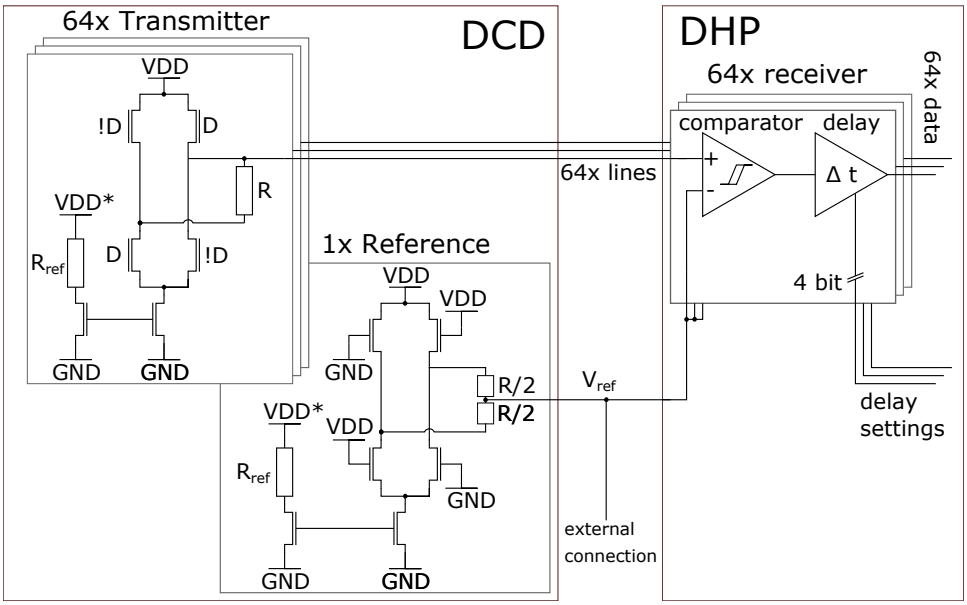


Figure 6.17: Sketch of communication between DCD and DHP. *(*)* The reference current source for the transmitter is connected to *DCD DVDD* in DCDBv3pipeline and to *DCD AVDD* in its successors to reduce noise on the transfer lines.

6.6 Link Parameters between DCDBv3pipeline and DHPT1.0

The DCD and the DHP communicate over 82 high speed lines and 5 lines for JTAG. To guarantee a good communication the DHP features independently configurable delay elements on all 82 lines. The DCD can be switched into a special debug mode where it puts out a known test pattern. An optimization procedure was developed comparing the measured pattern against the received pattern: First, the number of errors in the received pattern is measured for each data line, clock delay setting[14] and data delay setting. The result of the measurement for one line is shown in figure 6.16. The violet area corresponds to parameters for the clock delay and line delay where no errors were observed. The azure blue area (1 error) shows a transition region where the communication does not work. The turquoise area (2 errors) receives the pattern correctly – just shifted by one whole word. The clock delay setting is a global setting, while line delays can be chosen individually for each line. Next, for each data line the size of the

[14] The DCD needs two fast control signals; clock and synchronization, which is sampled by the clock signal. Shifting clock by one cycle, the DCD would see the same control input. Thus, when delaying clock the synchronization is delayed too.

operation window is determined. It is defined as the number of consecutive good (i.e. error free) data delay settings. If more than one sequence of consecutive good settings is found, the longest one is taken. This is repeated for every clock delay setting and data line. Using the information from all data lines, the quality of each clock delay setting is calculated. The quality of each clock delay setting is defined as the performance of the worst data line at this clock delay setting. Finally, the optimal settings are determined, by first selecting the clock delay with the highest quality, i.e. where the worst (smallest) data delay operation window was best (largest). At this clock delay setting, data delays are selected so that they are in the middle of the determined "good" operation window.

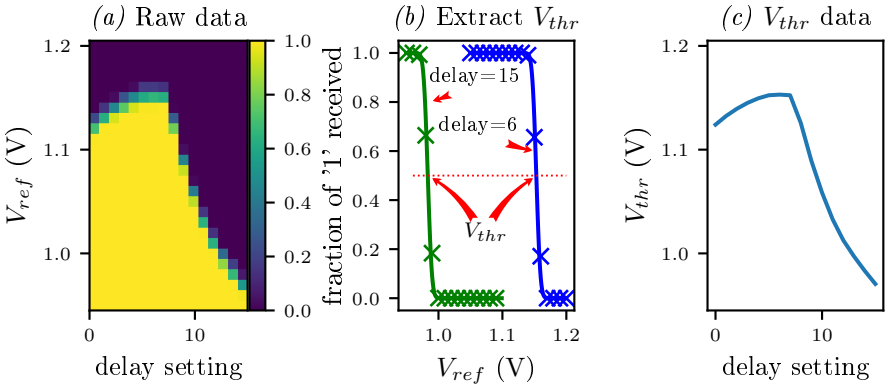


Figure 6.18: Visualization of data analysis process used to reconstruct the DCD waveform. *(a)*: For each of the 32 readings of each transmission line, data is recorded. The X axis shows the delay setting used, the Y axis shows the voltage used to overwrite DCD V_{ref}. For each column of this plot, the threshold value is determined by fitting an error function as shown in *(b)*. Repeating this step for all data results in figure *(c)*.

Even if the test pattern is received error free, bit errors could be observed in the communication between the DCDBv3pipeline and the DHPT1.0. This is due to transmission problems between DCD and the DHPT1.0, which are not found by the DCDs weak test pattern[15]. Several weak points in the communication were found. The DCD has lower driver strengths for falling signals, so low voltage intervals are shorter than high voltage intervals – which on an alternating pattern is known as duty cycle distortion. The data input on the DHPT1.0 have a built-in hysteresis which translates the different rise/fall times into duty cycle distortion, making the driver strength mismatch worse. The delay elements in the DHPT1.0 show an asymmetry in rise and fall times - further increasing the duty cycle distortion. Together, these effects can cause low signals to not be recognized correctly. They are not found by the test pattern, since it does not feature a strong test for this. In the test pattern, 7 lines go from high to low at the same time. Crosstalk due to capacitive coupling between the transmission lines helps in this case. To investigate the communication between the ASICs, the voltage waveform on the transmission line is needed. A direct measurement of the waveform is not possible due to line size and spacing in the µm range. Further, the capacity of the probe would disturb the signal, since even high end probes have a capacity of a few pF. Using the delay elements, the DHP can be used as a sampling oscilloscope with a time resolution used as a 1 bit and a time resolution of one delay value ((0.282 ± 0.020) ns at 1.54 V*DHP Core*, measured on a different DHP[16]). Using the reference potential, a voltage value can be extracted.

The communication between DCD and DHP is shown in figure 6.17. The DCD features 64+1

[15] The test pattern sends the words 0, -127, 0, followed by 29 times the word 127, thus most bits change together.

[16] Linear interpolation of measured values (0.290 ± 0.015) ns at 1.5 V*DHP Core* and (0.270 ± 0.015) ns at 1.6 V*DHP Core*. Data from [68].

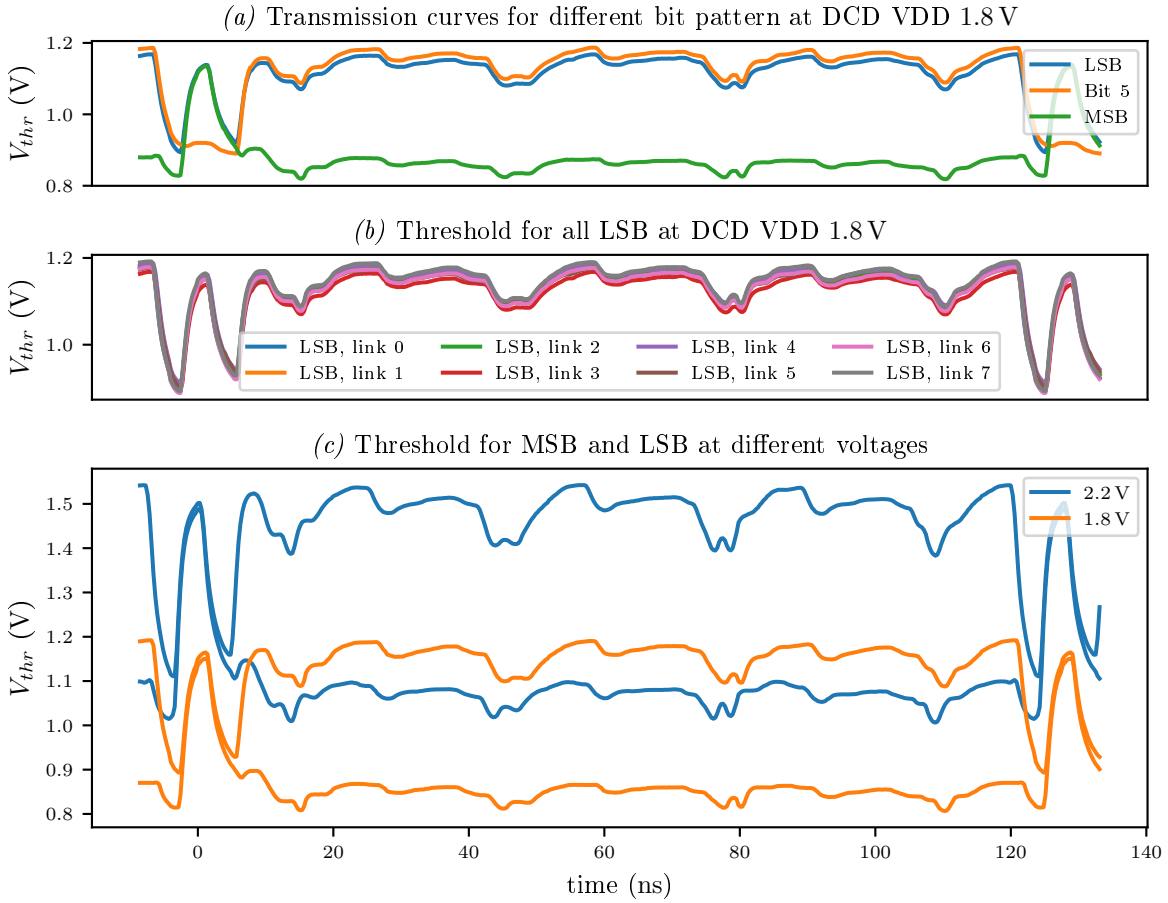


Figure 6.19: *(a)* shows the result for three bits on one link against time. The MSB (Bit 7) is only high for one clock cycle, The LSB (Bit 0) has two low and two high transitions. Bit 1 - 6 have the same test pattern. *(b)* shows the LSB signals for different links. From this measurement the channel to channel difference can be calculated to be $\sigma = 10\,\text{mV}$. *(c)* shows the MSB and LSB signal for different *DCD DVDD* voltages. A higher voltage increases both high and low level. The overall amplitude only increases slightly.

differential drivers, 64 for data and one for a reference voltage V_{ref}. The data drivers have their negative node connected to GND, while the positive terminal connects to the output pin. V_{ref} is produced by a voltage divider between the logical high and low value and puts out a logical 0.5. On DHP side a differential receiver is used with the data line connected to the positive terminal and V_{ref} connected to the negative terminal. On Hybrid 5, an external connection allows overwriting the V_{ref} potential used by the DHP. Measuring the signal while changing the reference allows reconstructing the original waveform, which is shown in figure 6.18. The digital test pattern repeats each 32 bits transmitted over a line. The data recorded for one link transmitting one bit is shown in figure 6.18 *(a)*, where the x axis shows the delay value which was set and the y axis shows the applied V_{ref}. Due to noise on the reference line and the signal line the high to low transition is smeared out. This allows neglecting the hysteresis of the DHP. The fraction of the signal being sampled high follows an error function, as shown in figure 6.18 *(b)*, where data from *(a)* is shown for two different delay values. Using a curve fit, the threshold voltage V_{thr} and width of the error function is determined. Using V_{thr} as a voltage measurement during transmission of one data words results in figure 6.18 *(c)*. This analysis is performed for all 32 words of

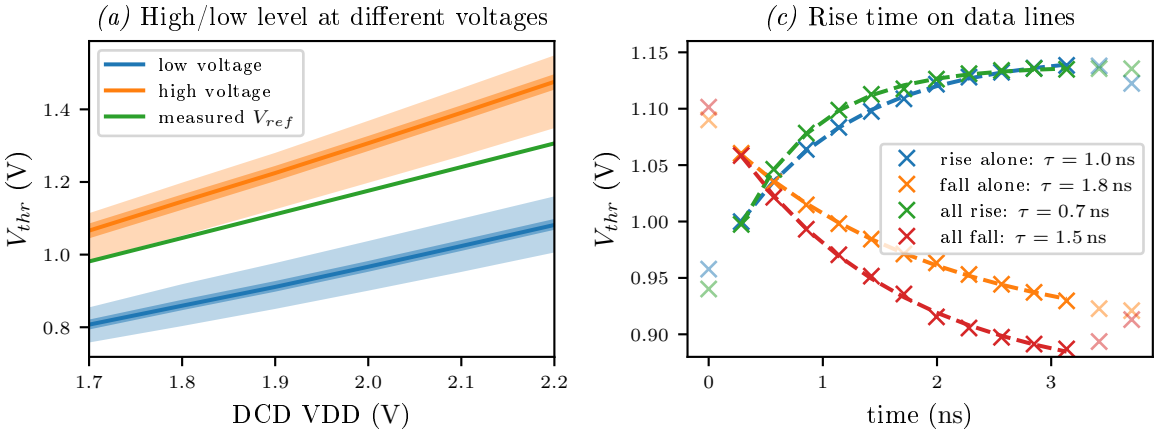


Figure 6.20: *(a)* shows the *DCD DVDD* dependence of the driver signal. The dark band represents the channel to channel variation of the mean signal; the bright band shows the minimum and maximum voltage within the signal. The green line shows the reference voltage V_{ref} sent by the DCD. *(b)* shows the transition of low/high values with and without cross talk. Solid markers show points used for the curve fit.

all 64 lines. A delay element is expected to delay the signal by (355 ± 20) ps[17][68], which was measured on a different setup. A delay setting of 14 would correspond to (3.95 ± 0.30) ns, which is one clock cycle at a DCD clock of 250 MHz. This was checked by recording all 16 delay setting and comparing a delay of 14 against a shift of one clock cycle, which is a very good match. Thus, the complete waveform can be pieced together using data from all samples on the line, resulting in a picture as shown in figure 6.19. *(a)* shows the waveform for 3 lines transmitting different bitpatterns. *(b)* shows the overlay of all LSBs transmitting their signal. As can be seen from this plot, different lines have a different offset. During the time when the outputs of all bits are constant (16 ns - 80 ns, half of a transmission cycle), the high and low level can be calculated to be (1 150 ± 10) mV and (860 ± 10) mV where the uncertainty represents the channel to channel differences due to production spread of the DCD driver. Figure 6.19 *(b)* shows the waveform at different *DCD DVDD* for the LSB and MSB of the transmission. Larger voltages result in higher low and high levels and a larger amplitude. This is summarized in 6.20 *(a)* for different voltages of *DCD DVDD*. The dark band around the lines represents the channel to channel variation; the light band includes the variation of the signals itself, like the dip around 45 µs in figure 6.19 *(b)* . The green line in 6.20 *(a)* displays the mean V_{ref} given by the DCD[18]. For each 100 mV increase in *DCD DVDD*, the high level rises by (81 ± 2) mV and the low level rises by (54 ± 2) mV, increasing the amplitude by (27 ± 2) mV. At the same time, the variations get larger, possibly counteracting part of the amplitude gain.

From the measurement curves, the signal rise time can be extracted as shown in figure 6.20 *(b)*. One can see, that transitions from low to high have a much shorter rise time. This is due to the output driver of the DCD which has an asymmetric driving strength. In addition, crosstalk can be seen. Two rise times are shown: *"Rise alone"* is from the LSB at a time where only the LSB and the MSB have a transition. These two lines are far apart on the bump bond adapter and their neighboring lines are at a constant potential during the transition. *"All rise"* is from bit 1 at a point where all but the MSB have a low to high

[17] at 1.2V DHP VDD

[18] It is measured by adjusting the external V_{ref}. If no current is needed, external and internal V_{ref} are expected to have the same mean value. Oscilloscope measurements of DCD V_{ref} show that it is not constant but shows four drops in every readout cycle, very similar to the drops visible in 6.19.

transition, so both neighboring lines of bit 1 show the same voltage increase. This effectively reduces the capacitance seen by the line and reduces the rise time. The same can be seen for falling signals. For real data, a transition on a line where the neighbors perform the opposite transition will be even slower. The observed rise/fall time of up to (1.8 ± 2.0) ns is too high for reliable operation at nominal frequencies. Signals do not settle completely, so a high to low transmission after a long high period are critical, especially for data which is transmitted during the regular fluctuations in the signal. These fluctuations appear with a regular 40 MHz period – one of the frequencies used in the ASIC. These fluctuations are also visible on the power line when using an oscilloscope[19]. Another issue is the asymmetric signal strength. Due to the hysteresis in the receiver of DHPT1.0, the asymmetry of the signal (and thus the duty cycle distortion) increases. In addition, the delay elements of the DHPT1.0 are not symmetric and add further to the duty cycle distortion, reducing the width of a low level. Thus, finding a good delay setting gets hard.

The main reason for the slow rise and fall is a higher capacitance on the line and at the DHPT1.0 input. As a result of this measurement, the next iteration of the DHPT was produced without hysteresis and with reduced **E**lectro **S**tatic **D**ischarge (ESD) protection, reducing the parasitic input capacitance from 3 pF to 1 pF [69]. Further, the delay elements are improved to be symmetric. On DCD side, the output driver current was increased from 1.2 mA to 1.33 mA, with an additional high current option of 1.84 mA. The reference current for the output driver was changed, so it is determined by *DCD AVDD*, which is more stable than *DCD DVDD*. To make future measurements easier, an improved test pattern was proposed which was implemented in the production version of the DCD for Belle II [70].

[19] Though Hybrid 5 has better voltage filtering and larger supporting capacitors, the fluctuations are expected to decrease on large DEPFET modules since the supporting capacitors are closer to the ASICs and connected with a lower impedance line

CHAPTER 7

Measurements on Hybrid 5

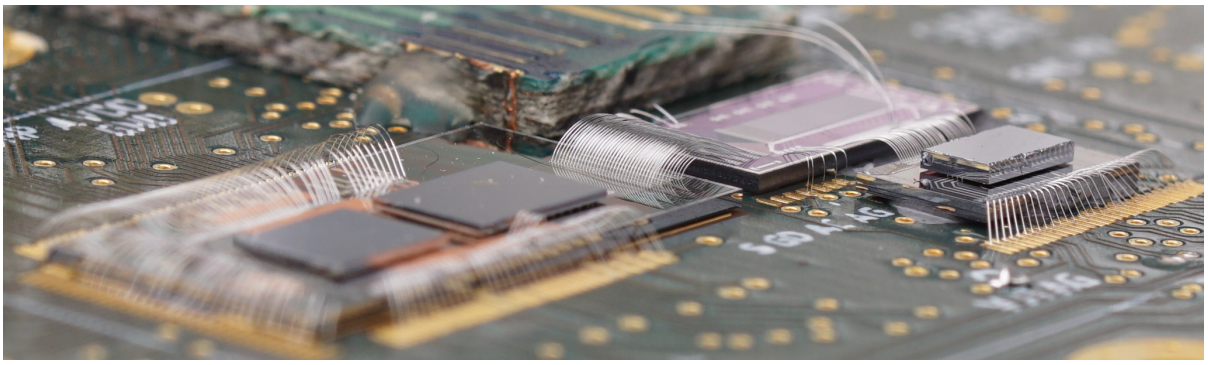


Figure 7.1: Picture of Hybrid 5. DCD and DHP are mounted together on one bump bond adapter, the Switcher is mounted on a second bump bond adapter. The bump bond adapter and the matrix are connected together and to the PCB using wire bonds. Long wire bonds connect some Switcher outputs to external test pads.

In this chapter, the performance of a small DEPFET matrix is analyzed using a laser setup and a source. This was done using the first full scale system demonstrator produced for the PXD; the first DEPFET matrix to be read out by a DHP. The characterization was done to prepare the system for the first beam test where a DHP was used to read zero suppressed DEPFET data [57]. Figure 7.1 shows a picture of such a system.

A particle (or laser pulse) interacting with the sensor will create charge which modulates the current; the current will be digitized and results in a higher ADC code than the expected pedestal code (ped). The excess of the ADC code above the pedestal and common mode (CM) is called a firing pixel, its signal is $\mathrm{ADC}_i - \mathrm{ped}_i - \mathrm{CM}_2$. On Hybrid 5 pedestal subtraction and common mode correction is done in hardware by the DHP. Only firing pixels with a value above a certain threshold will be sent to the backend electronic, values below the threshold will be discarded as noise as shown in formula 5.3. Charge deposited in the matrix can span multiple pixels; it creates so called clusters. The cluster signal is defined as the sum of all signals within the cluster. The cluster seed is defined as the pixel showing the highest signal. For Belle II type matrices, mostly one or two pixel clusters are expected, since thin sensors with large pixels are used.

The optimal working point of the matrix was determined using the laser setup sketched in figure 7.2. In the laser setup, the DUT is mounted on a 2D motor table which is movable in steps of 0.5 µm, while a laser is illuminating the backside of the sensor with a spot size smaller than 3 µm [71]. For laser measurements, laser pulses are injected in the sensor and the response is measured. This measurement is

repeated while changing operation voltages of the matrix. An analysis of the data allows determination of an optimal working point. Depending on the measurement, two measurement strategies were used:

- The laser is injected at the same position for every voltage setting.
- The DUT is moved below the laser and measurements on a 2D grid of positions are performed for each measurement. At each position, laser pulses are injected into the matrix and the response is measured.

The measurement results of this are presented in chapter 7.1.

For the source measurement, the pulse height histogram was recorded while illuminating the system with a gamma source. Using several sources with varying gamma energies in the range from 8.05 keV to 59.95 keV and comparing the response for each source, an energy calibration of the system was performed, which is described in chapter 7.2.

Issues with Hybrid 5 The DHP02's limitations described in 5.3.1 need some workarounds. The DHP02 has a weak clock output and the DCD has no clock input buffer so the maximum frequency for the clock is limited to 250 MHz. An optimization of the synchronization delay elements for the clock and synchronization signal by [49] showed no working setting when using clock speeds above 160 MHz so this frequency was used[1]. The PLL in the DHP02 was designed for frequencies around 300 MHz, so it is unable to lock to such low frequencies. Thus, the DHP02 needs the core clock transmitted in addition to the GCK, requiring an additional differential line. The matrix used in Hybrid 5 (F07: ARR_128x16_ST_SD_SCG_Z075_TS, explanation of the abbreviations can be found in footnote 1 on page 89) has 16 gates and 128 drains with a standard Belle II like layout with a 6 µm long (low gain) transistor gate and $50 \times 75\,\mu m^2$ pixel pitch. The DHP02 assumes 256 connected drains when calculating common mode correction. With only half the drains corrected and the other channels out of the DCDs dynamic range, common mode noise will be underestimated, increasing the noise, smearing the signal and requiring a higher threshold in the DCD. Since the DHP02 could not work with a 16 gate matrix, a switcher sequence for 32 gates was used. Since nothing is connected to the Switcher channels for gate 17-32, the matrix is completely switched off during that time, while the DCD tries to subtract $\approx 100\,\mu A$ of pedestal current. Thus, the DCD gets out of its working point. When the current is switched on again, the DCD needs ≈ 400 ns to recover. Thus, 2 of 16 gates are lost for data taking. The varying load on the matrix lines may degrade performance. Despite these issues, a reasonable performance could be achieved.

7.1 Determination of Optimal Working Point using Laser Measurements

The DEPFET matrix uses multiple voltages to form the field geometry in the sensor bulk which is needed to achieve good charge collection. As a result, multiple voltage settings influence the detector performance and need to be optimized. The following potentials are used within a DEPFET Matrix:

- Source, drain and gate potential are the potentials applied to the DEPFET transistor. The *source* potential is the reference potential for the matrix; all voltages are given with respect to the *source* potential. The drain potential is given implicitly by the input node of the DCD. Both drain and

[1] After the beam test, better delay settings were found, which is shown in 8.1, but at the time 160 MHz was the highest possible frequency.

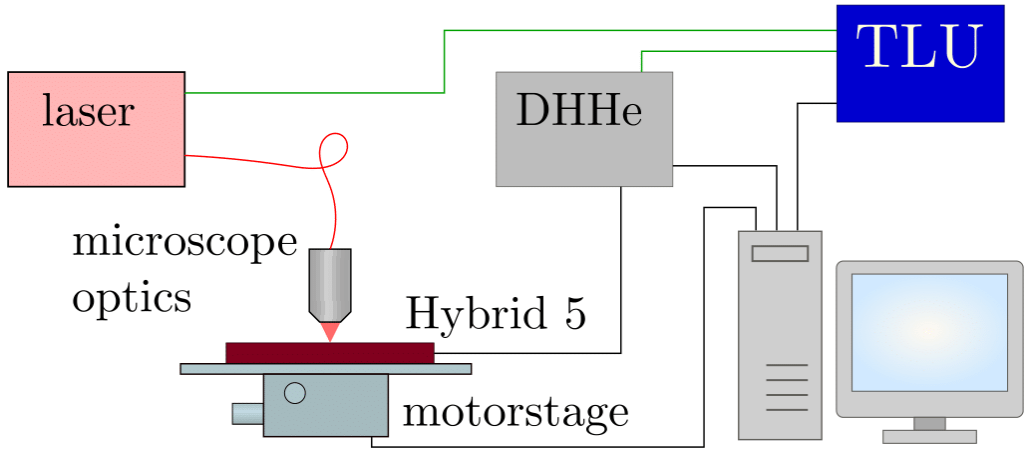


Figure 7.2: Sketch of the setup used for laser measurements on Hybrid 5. The DUT (Hybrid 5) is mounted on a motor table and is read out by a DHHe. The laser pulse and the readout are synchronized using a Trigger Logic Unit (TLU) [72]. TLU, DHHe and motor table are controlled by a PC which records data from the DUT.

source are $p+$ implantations so they are coupled to the sensor bulk by a diode. The source-drain voltage needs to be high enough for the FET to be in the saturation region. The default potential of *source* is 7 V above system ground (GNDA). The gate of the FET needs two potentials: one applied during readout and clear, one applied during charge collection. The *gate-on* potential applied during readout and clear needs to be low, so that the DEPFET starts conducting, but high enough for the DEPFET to stay in its saturation region. It mainly influences the current flowing through the DEPFET and needs to be adjusted to yield the expected current. A lower *gate-on* potential results in higher drain currents, a higher internal amplification and a wider spread of the drain currents. It is typically between -1.5 V and -4.5 V[2] and has no large influence on charge collection in the matrix. The potential applied during charge collection needs to be high enough to switch the transistor into a non-conducting state even if the internal gate is full of electrons.[3] It is called *gate-off* potential and has a typical value of 3 V (wrt. *source*). The difference between *gate-on* and *gate-off* influences the potential of the internal gate: While clearing the matrix, the readout gate potential is applied. During this process, charge is removed from the internal gate by the clear contact and the potential of the internal gate is set to a potential determined by the capacitive voltage divider built from the sensor potentials and their coupling to the internal gate. The strongest capacitive coupling is between the internal and external gate, thus during the clear pulse the internal gate is in first order set to a potential determined by the capacitive voltage divider between those two, which is above the *gate-on* potential. When switching the gate potential from *gate-on* ($V_{g,on}$) to *gate-off* ($V_{g,off}$), the internal gate changes its potential V_{ig} by $\Delta V_{ig} = {}^{C_{coupl}}/_{C_{total}} \times \left(V_{g,off} - V_{g,on}\right)$, where C_{coupl} is the coupling capacity between the internal and the external gate and C_{total} is the total capacity between the internal gate and the sensor. The internal gate is a local maximum attracting electrons, so the resulting V_{ig} needs to be sufficiently positive.

- The *bulk* potential needs to be high sufficiently for the transistor diodes at the bulk/source and bulk/drain interface to be biased in reverse direction. The standard value for *bulk* is 10 V.

[2] It depends on the gate width of the matrix, the threshold voltage (radiation dependent), pedestal spread, dynamic range of the DCD etc.

[3] Additional requirement: *Gate-on* and *gate-off* need to be 3 V apart for the switcher to work

- Like gate, the clear contact has two potentials; *clear high* is applied for active clearing while *clear low* is applied during charge collection and readout. The *clear high* potential needs to be high enough to completely clear the internal gate. The minimum value needed is influenced by the length of the clear pulse and the *cleargate* potential. Higher clear voltages do not degrade the sensor operation, their rise and fall times make the clear pulse a bit longer. On the systems used the maximum *clear high* is limited by the switcher, which supports only 25 V between its ground potential and the maximum voltage. This results in a maximum clear potential of 18 V above *source*. The *clear low* potential has a strong influence on charge collection. If it is chosen too high the clear contact stays attractive during readout which leads to charge loss. A too negative *clear low* potential can cause electrons to be injected from the clear contact into the internal gate, creating additional charge. This effect is called back injection. It fills the internal gate with electrons, reducing the attraction for electrons and increasing noise. Both effects, especially back injection, are influenced by the *cleargate* potential. Due to space constrains, the *clear low* potential is called *clear* in some plots.

- The *cleargate* separates the clear implantation from the internal gate, its potential influences the coupling between both. At the same time it acts as a spacer between the transistor and the drift region of the pixel, between the transistor and the clear implantation and between the clear implantation and drift region. On the border between clear implantation and FET it lays directly between source and drain implantation. A too negative *cleargate* potential can form a parasitic channel between source and drain, resulting in all transistors turning on in parallel. At high *cleargate* voltages the shielding between clear implantation and internal gate gets weak and back injection can occur at higher clear low potential. In addition, a too high *cleargate* potential can trap electrons beneath the clear gate, resulting in a much longer charge collection time which results in charge loss. For brevity, the *cleargate* potential is called *CCG* in most plots.

- The *depletion* potential is the main potential for depletion of the sensor. Too positive *depletion* potentials result in a not fully depleted sensor, too negative potential result in the minimum potential valley being too close to the surface, where charge can get stuck at the border between *drift* and *cleargate* or can be attracted by the clear contact.

- The *drift* potential is applied in the outside regions of the pixel. The *depletion* field transports charge vertically to a layer beneath the sensor surface. Far from the internal gate the *drift* potential helps to form a voltage gradient towards the internal gate so that charge is collected via drift. A too positive *drift* potential will result in charge loss in the pixel drift regions due to charge which will not arrive in time and due to charge which gets trapped at the border between drift region and the transistor region which is shielded by the clear gate. The trapping depends on the minimum potential layer of the sidewards depletion. Therefore both the *cleargate* voltage and the *depletion* voltage will influence the optimal *drift* potential. A too negative potential can result in lost charge at the pixel borders between columns.

An optimization of the sensor potentials can be broken down into several small steps. The *gate-off*, *bulk* and *source* potential have a low influence on detector performances; they were set to values known from design. The *gate-on* potential sets the DEPFET pedestal current. A constant current can be subtracted from all DEPFET pedestal currents by the SubIn in the DCD. The resulting pedestal current distribution could be further reduced by using the dynamic 2 bit offset DACs as described in 8.2, but on a small, non-irradiated sensor this feature is not needed for good performance. *Gate-on* and SubIn need to be chosen so that the residual current of all DEPFET transistors is in the dynamic range of the DCD with

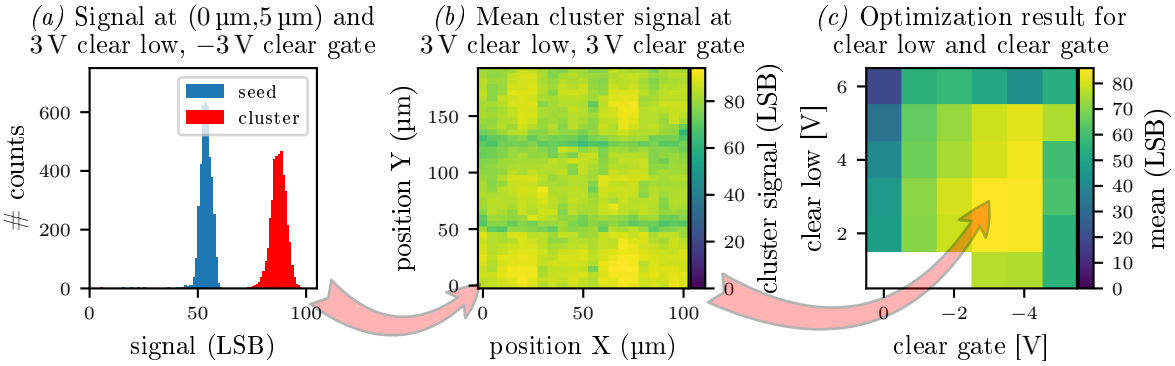


Figure 7.4: Example of a laser measurement on Hybrid 5 and illustration of the analysis procedure. *(a)* At each laser position, the signal is recorded and signal histograms are filled. *(b)* The cluster signal is measured for each laser position and filled into a signal map. On an optimized sensor, this plot is expected to be flat. *(c)* shows the mean of the cluster signal map for different voltages.

enough headroom for signal. On Hybrid 5 the pedestal current distribution is small so that the *gate-on* potential can be chosen to result in 100 µA mean pedestal current, the common part is subtracted by SubIn. Other settings can influence the current so slight adjustments can be necessary. Optimizing *gate-on*/SubIn is the first step before any other optimization and is typically done by hand.

The *clear high* voltage mainly influences the charge removal from the internal gate. The minimum required *clear high* voltage strongly depends on the *cleargate* potential. Each 1 V increase in *cleargate* allows about 3 V lower *clear high* voltage. On the PXD6 matrices used in this thesis, the operation window for *cleargate* with good charge collection is small, therefore clear is optimized as single parameter. For optimization different *clear high* voltages are used. At every voltage the signal given by the matrix is measured, while injecting a laser pulse into the matrix every frame. An incomplete clear causes charge to remain in the internal gate, increasing the measured signal a frame later. At sufficiently large *clear high* voltages the signal is minimal and constant with higher clear voltages. For this measurement, the injection position is not relevant, since the effect of clear on the internal gate is measured. A measurement result is shown in figure 7.3. The Hybrid 5 board used for this measurement is equipped with a Switcher1.8. In this Switcher generation the maximum clear voltage is limited to 20 V above GND. Therefore the *clear high* voltage was chosen as maximum voltage the switcher supports.

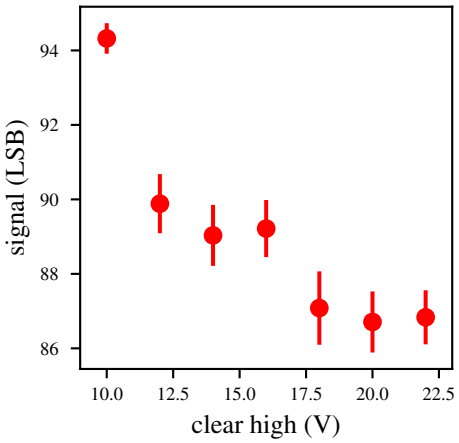


Figure 7.3: Measurement of clear efficiency at different *clear high* voltages. Laser pulses are constantly injected into the matrix; incomplete clear will increase the measured signal.

The remaining four potentials (*depletion*, *drift*, *cleargate* and *clear low*) are optimized in two successive 2D parameter scans. For optimization, charge collection at different potential pairs is measured using a laser scan. The *depletion* and *drift* potential are important for charge transportation towards the internal gate, *cleargate* and *clear low* are important for charge collection in the internal gate. Thus, *depletion* and *drift* are optimized first.

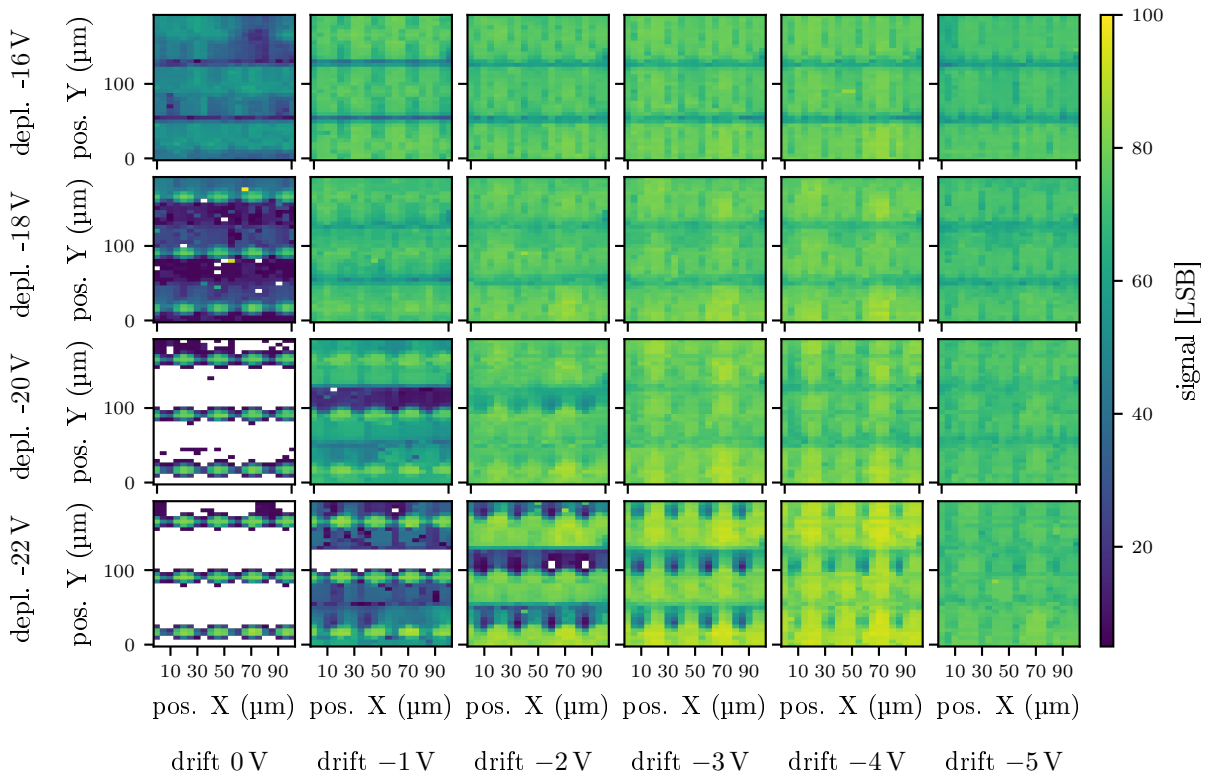


Figure 7.5: Laser measurement result for Hybrid 5. Each subplot is a laser measurement taken at different voltages for *drift* and *depletion* and shows the cluster signal against the injection position. From this data, results in 7.6 can be calculated.

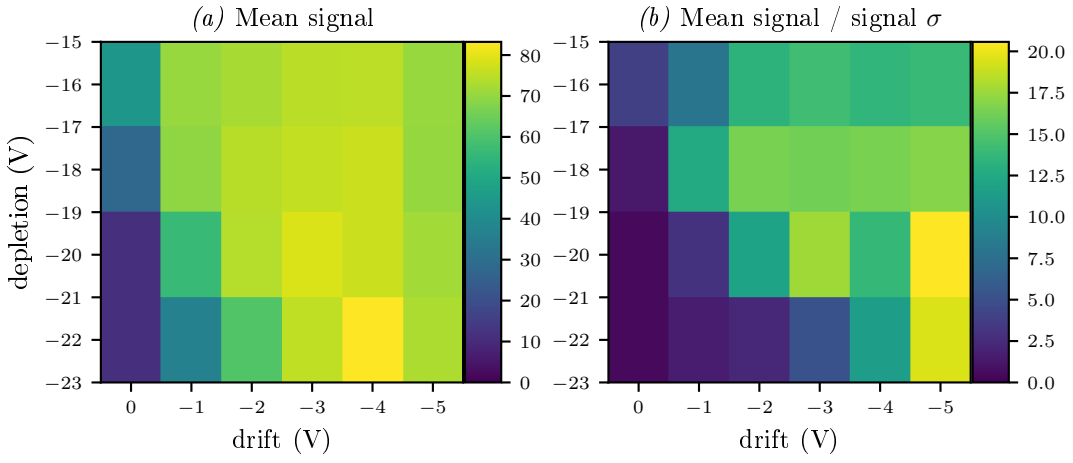


Figure 7.6: Result for *drift/depletion*. Each point corresponds to a laser measurement. *(a)* shows the mean of the cluster signal over all laser positions as function of the bias voltages. *(b)* uses the mean calculated for the other plot and divides it by the standard deviation of the cluster signals over all laser position. An optimal point should have a high signal and a reasonable signal over width.

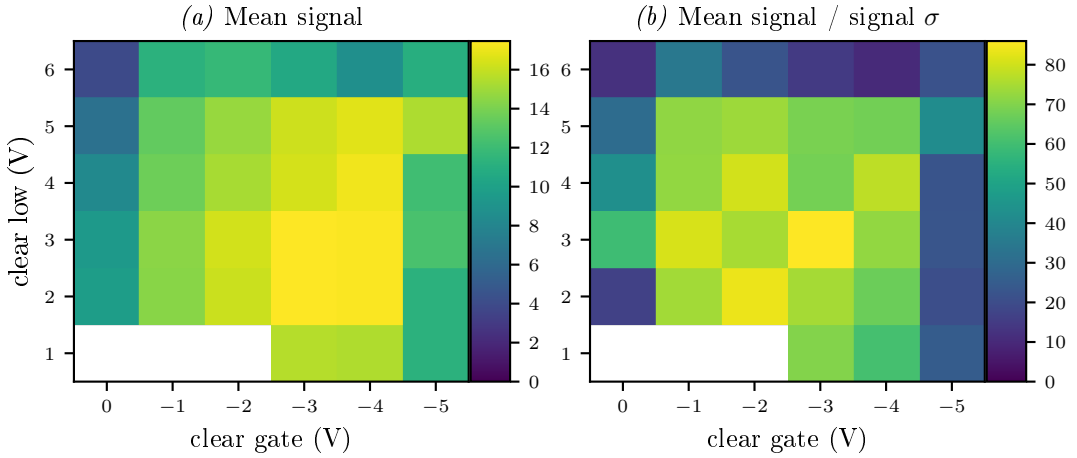


Figure 7.7: Result for *clear low*/*cleargate*. Each point corresponds to a laser measurement. *(a)* shows the mean of the cluster signal over all laser positions as function of the bias voltages. *(b)* uses the mean calculated for the other plot and divides it by the standard deviation of the cluster signals over all laser position. An optimal point should have a high signal and a reasonable signal over width.

Since the charge collection in the DEPFET can have position dependent effects, a 2D grid of laser positions was measured for each voltage combination. From the position dependent matrix response, different performance numbers can be extracted:

- The mean of the cluster signal distribution, which should be homogeneous for well chosen bias voltages.
- The mean of the seed signal distribution which will be similar to the cluster signal near the pixel center and much smaller at the pixel border.
- The cluster size distribution.
- The width of the above distributions.

Figure 7.4 *(a)* shows the recorded histogram for a single laser position. The charge collection measurement for each bias voltage setting is performed on an area of $210 \times 390\,\mu m^2$ with measurements every $10\,\mu m$ in both directions for a total of 819 laser positions per voltage setting. The results at a single voltage are shown in figure 7.4 *(b)*, where the mean cluster signal determined at each position is shown. From each of these measurements, a single number, in this case the mean of the mean cluster signals, is extracted and used for a final plot, which is shown in 7.4 *(c)*.

Figure 7.5 shows the result of one voltage measurement. Each small plot is the result of a laser measurement at different bias voltages for *depletion* and *drift*. The seed signal can be found in B.1. The same procedure was repeated for *cleargate* and *clear low*. Their raw data can be found in B.2 and B.3.

Using this information the mean signal and the charge collection uniformity can be determined for each voltage setting. This is done by calculating the mean and standard deviation of the cluster signal at all 819 laser measurement points. This mean is used as the mean charge from the sensor at this voltage setting, while the standard deviation is used as a measure of the charge collection homogeneity. These two numbers were determined for all potential pairs in the measurement, resulting in the plots 7.6 for *depletion*/*drift* and 7.7 for *cleargate*/*clear low*. *(a)* shows the mean of the cluster signal over all laser

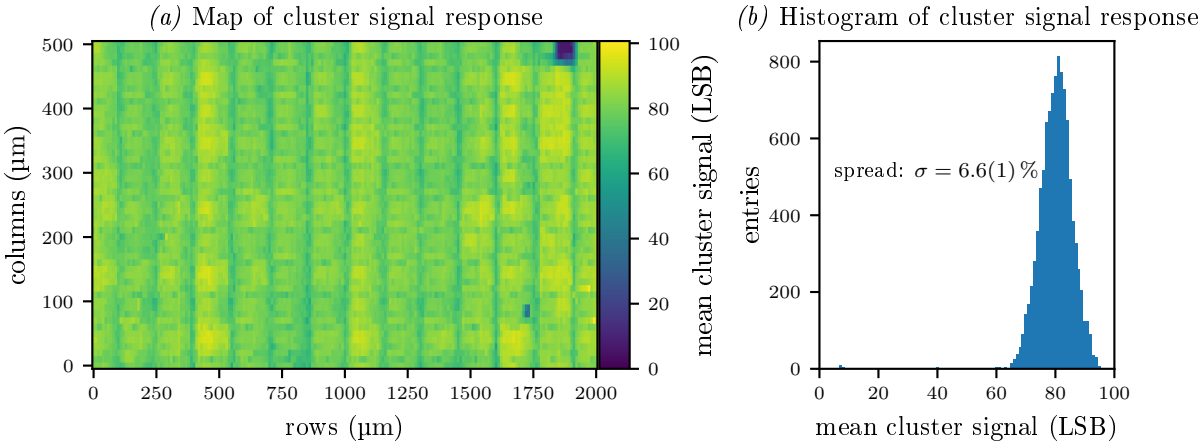


Figure 7.8: Result of large area laser scan over 13.3 % of the matrix. *(a)* shows the laser response as function of the laser position, *(b)* shows a histogram of the laser repsonse.

positions as a function of the bias voltages, *(b)* uses the mean calculated for the other plot and divides it by the standard deviation of the cluster signals over all laser position. An optimal point should have a high signal and a reasonable signal over width. Some positions yield a good mean signal and width but are not usable due to other effects. These are mentioned in the description.

From 7.6 the optimal potentials for *depletion*/*drift* are determined to be *depletion* = −19 V and *drift* = −3 V, far away from bad settings at −22 V and −16 V. A setting with *drift* = −5 V looks promising, but measurements form another test system with a similar matrix (Hybrid 4.1.00) showed issues starting with *drift* voltages below *drift* = −5 V. To be on the safe side, a conservative bias voltage for *drift* was chosen. Using *depletion* = −18 V and *drift* = −3 V, a *cleargate* vs *clear low* measurement was performed, resulting in optimal potentials of *clear low* = 3 V and *cleargate* = −2 V taken from 7.7. During the *depletion*/*drift* measurement, *cleargate* and *clear low* were already at the optimal voltages, so that a further iteration was not needed. The starting voltages for *cleargate* and *clear low* were determined to be optimal using 3D charge transport simulations by the sensor designer and were verified in this measurement.

To confirm the performance at the chosen voltages, a final measurement was performed over a large area of $2\,010 \times 510\,\mu m^2$, with a step size of 10 µm. The 2D cluster signal map is shown in figure 7.8 *(a)*, figure *(b)* shows a histogram of the cluster signal response. One blind pixel is visible on the top right. Measuring a much larger area was not possible due to backside metallization. The measured signal spread is 6.6 % at an injected signal of ≈ 80 LSB, which corresponds to 4× **M**inimum **I**onizing **P**article (MIP) signal, slightly larger than the signal expected from slow pions.

7.2 Energy Calibration using Gamma Sources

For energy calibration the DEPFET matrix was irradiated with gamma sources using the optimal voltages determined with the laser measurements. Ionizing radiation produces electron hole pairs in silicon proportional to the radiation energy; creating a known amount of electron hole pairs and measuring the signal seen by the DCD allows the determination of the internal amplification g_q when the gain of the DCD is known. Using the conversion factor in silicon ($A_{conv} = (3.65 \pm 0.02)\,\mathrm{eV}\,e^{-1}$) [73] and the ADC

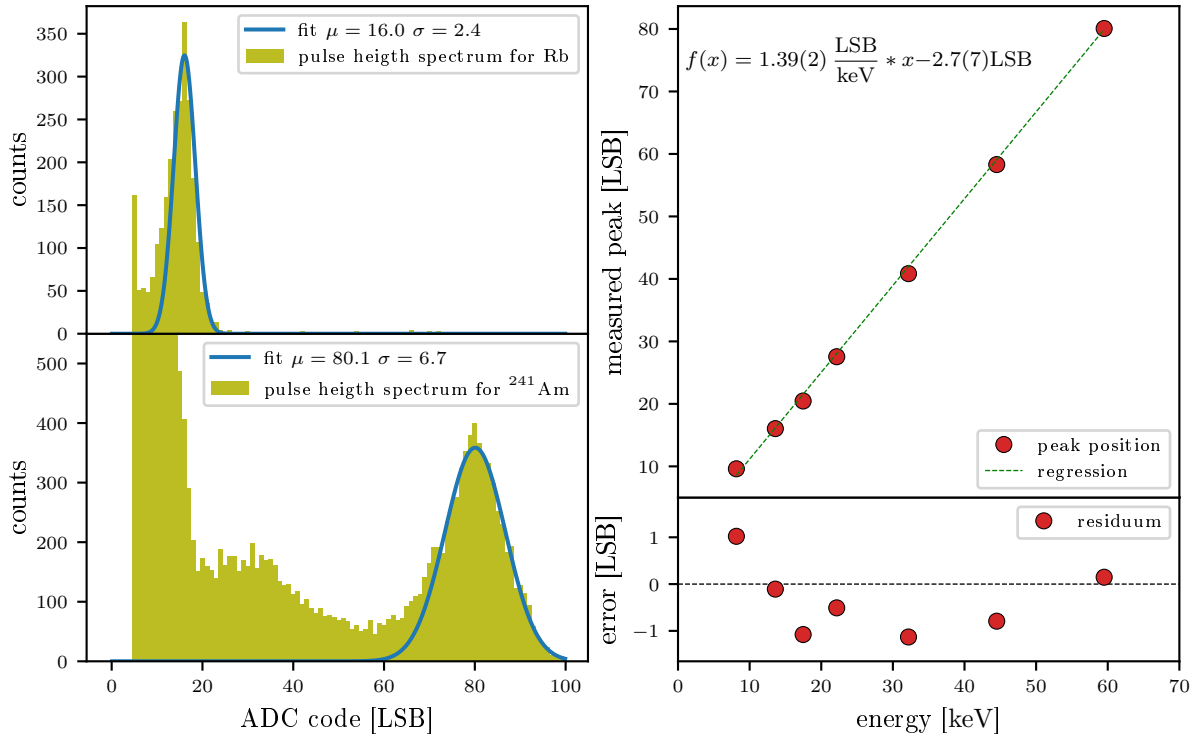


Figure 7.9: Energy calibration of Hybrid 5. *(a)* shows the pulse height spectrum of a variable x-ray source with a Rubidium and the fit to the $K\alpha$ line at $E_{K\alpha} = 13.39\,\text{keV}$. *(b)* shows the pulse height spectrum of a ^{241}Am source with an energy of $E_\gamma = 59.54\,\text{keV}$. *(c)* shows the linear dependency between photon energy and measured peak position. *(d)* shows the residua from the expectation values from the fit.

gain b one gets

$$\text{ADC}_i = I_{sig} * b = q * g_q * b = \frac{E_\gamma}{A_{conv}} * g_q * b \tag{7.1}$$

$$g_q = \frac{\text{ADC}_i * A_{conv}}{E_\gamma * b} \tag{7.2}$$

For a source measurement, the matrix is irradiated by a source while being read out. The pulse height spectrum of the measured clusters is calculated and a gauss function is fitted to the distribution as shown in figure 7.9, where *(a)* shows the pulse height spectrum of a variable x-ray source with a Rubidium target. The peak in the spectrum is the Kα line at $E_\gamma = 13.39\,\text{keV}$. *(b)* shows the spectrum for ^{241}Am with an energy of $E_\gamma = 59.54\,\text{keV}$. The cut at low counts is due to the threshold of 5 LSB applied in the DHP. In total, spectra from 7 different sources were measured, they are listed together with the used energy in B.1 and are shown in B.4. Comparing the known energy with the measured peak position results in the energy calibration shown in 7.9 (c). Using linear regression, the dependency of energy and measured peak position is determined as

$$f(x) = (1.392 \pm 0.010)\,\frac{\text{LSB}}{\text{keV}} * x - (2.8 \pm 0.7)\,\text{LSB}. \tag{7.3}$$

Using $\frac{\mathrm{ADC}_i}{E_\gamma} = (1.392 \pm 0.010)\,\frac{\mathrm{LSB}}{\mathrm{keV}}$, the ADC gain $b = (11.21 \pm 0.06)\,\mathrm{LSB}\,\mu\mathrm{A}^{-1}$ which was measured for this DCD similar to the measurements shown in chapter 6, g_q can be determined to be

$$g_q = (457 \pm 5)\,\frac{\mathrm{pA}}{e}.$$

The constant term of the regression is (2.7 ± 0.7) LSB, significantly different from 0 LSB. A reason for this could be the way pedestals are taken. During the pedestal acquisition, the DHP02 uses considerably less power than in normal operation, possibly changing the temperature of the DCD, which results in different subtraction currents. Common mode changes of all pixel can be corrected by the DHP02, but on Hybrid 5 only half of the channels are connected. Changes in the subtraction current sources are seen by the connected channels while the other channels are out of the dynamic range and do not see the change. Thus only half of the effect is corrected in the DHP02. An indicator that this is the case can be found when considering the common mode values sent by the DHP02, which mainly sends the codes 46-47 while a common mode of 0 should give the code 48. The mean common mode is at 46.5, 1.5 LSB too small, so the offset in current is expected to be -3 LSB with only 1.5 LSB corrected, which explains a part of the (2.8 ± 0.7) LSB shift.

The energy resolution (ΔE/E) of the system is shown in figure 7.10. It is 14 % at the **M**ost **P**robable **V**alue (MPV) of a MIP. The energy resolution number was obtained using raw ADC values without gain equalization on ADC channel or pixel level and could be degraded due to the known issues with the DHP02: The first gates were masked, since they were partially out of dynamic range during source scans due to DHP02 issues.

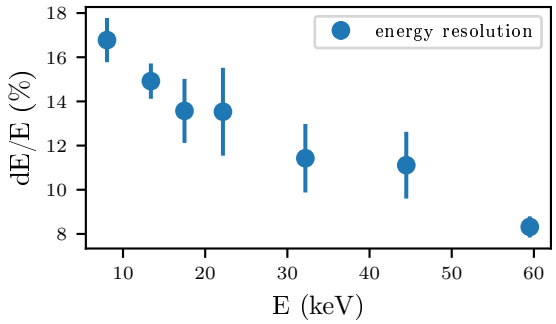


Figure 7.10: Energy resolution at different energies determined on a Hybrid 5 module.

7.3 Hybrid 5 Measurement Results

In this chapter, an optimization using laser measurements was shown, yielding optimal matrix voltages of

$$\mathit{depletion} = -19\,\mathrm{V},\ \mathit{drift} = -3\,\mathrm{V},\ \mathit{clear\ low} = 3\,\mathrm{V} \text{ and } \mathit{cleargate} = -2\,\mathrm{V}.$$

Using these voltages an energy calibration was performed using 7 different sources and yielding an internal amplification of

$$g_q = (455 \pm 5)\,\frac{\mathrm{pA}}{e},$$

which is in agreement with the expected amplification. A possible reason for the fit line having an offset not compatible with 0 LSB was found in the way pedestals are taken. Systems with newer ASICs don't show this behavior [74]. The deviation between expected and measured peak positions is less than

1.2 LSB with an standard deviation of (0.71 ± 0.10) LSB. The energy resolution is 14 % at the MPV of a MIP, using raw data without calibration constants. For Belle II operation, energy resolution is not important, since it does not contribute to detection efficiency and the tracking resolution does only weakly depend on the energy resolution[4].

After the characterization[5], the module was the first module with a DHP to be used in a beam test [57].

[4] The resolution is limited by the large center of the pixel, where only single pixel clusters will be detected

[5] The software development needed to perform this measurement and to analyze laser scans and source scans semi-automatically was part of this thesis. Repeating the measurements at different bias voltages was done by C. Hönig as part of his Bachelor thesis [75]. The results shown in this thesis were obtained by reanalysing the data.

CHAPTER 8

Measurements on Hybrid 6

The first large DEPFET matrices were examined using a system called Hybrid 6. Due to metalization issues, the matrix production with Belle II prototypes produced by HLL Munich yielded only three non-broken matrices with the matrix types I06 (ARR_768x160_ST_SD_SCG_Z075), J00 (ARR_768x120_-CC_PC_Z075) and I00 (ARR_768x120_CC_ED_SCG_Z100)[1] The I06 matrix and J00 matrix were assembled first with all Switchers and all DCDs and DHPs. Due to production problems, one Switcher of the I06 matrix was not usable and the attempted rework destroyed the module. The J00 module was used during the beam test in January 2014. Since the J00 module was only produced in late December 2013, no optimization could be performed prior to the beam test. Due to the lack of a suitable power supply, only one DCD analog part could be used at a time[2]. Data from this beam test is available, but it is strongly degraded due to bit errors in the transmission between DCD and DHP. The pedestal distribution read by the DCD is much wider than its dynamic range. It shows a strong gradient along the row, a gradient along the columns and large in-gate variations, so large parts of the matrix were not sensitive to particles. No JTAG read back of the Switcher configuration was possible, due to a differential/single ended converter with a wrong voltage rating of 3.3V while the Switcher works at 1.8V. With some careful

[1] Matrix properties:

- **ARR_768x120**: Pixel Array, in this case with 768 drain lines and 120 gates.
- **ST**: Standard clear gate (parasitic capacitive coupling to clear).
- **CC**: Clear gate with dedicated capacitive coupling structures.
- **SCG**: Surrounding clear gate (clear gate surrounds the transistor and separates it from the pixel drift region)
- **SD**: Standard drift field (An implantation in the drift region where a potential can be used to increase the drift field towards the DEPFET).
- **ED**: Enhanced drift field (A drift implantation with an additional deep implantation at the far end of the drift field).
- **PC**: Poly cover (A gate structure above the drift region where a potential can be used to increase the drift field towards the DEPFET).
- **Z075**: Pixel pitch in row direction in µm, in this case 75 µm. The pixel pitch in column direction is 50 µm for all matrices.
- **TS**: 6 µm gate length, low g_q. **T1**: 5 µm gate length, medium g_q. **T2**: 4 µm gate length, high g_q.

[2] The bench power supplies used have limited sense capabilities. They require the force voltage to not be higher than 1V (TTI) [76] or 2V (HAMEG)[77] above the sense voltage. Due to long, high resistivity supply lines, three active (analog on) DCDs need a higher difference between force and sense voltage and two active DCDs were at the limit. During the beam test, the high speed link with two of the three DHPs worked when only one ASIC pair (DCD and DHP) was used, but with two or more ASIC pairs being used, no link could be established. Later this problem could be fixed.

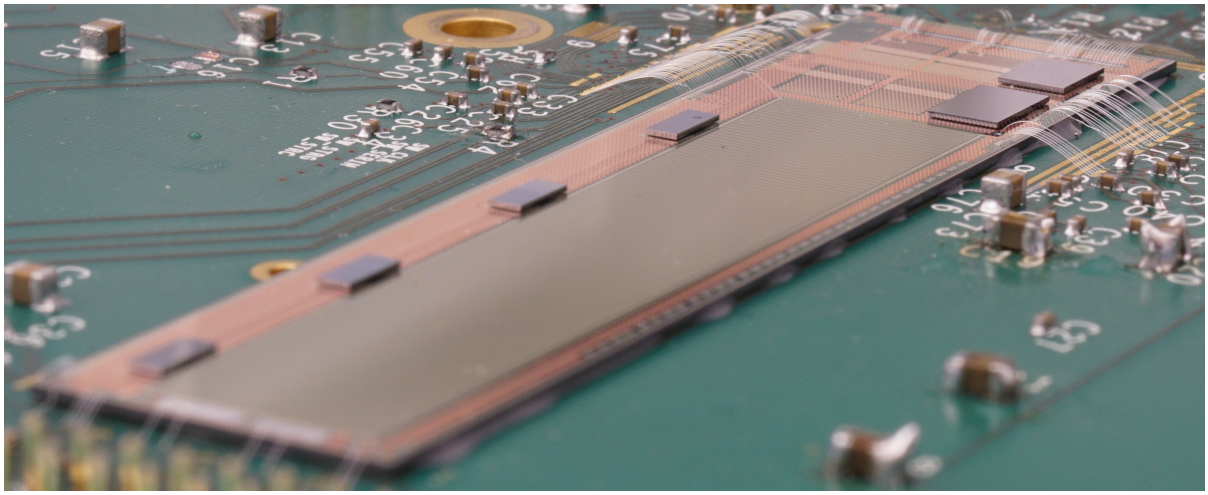


Figure 8.1: Picture of Hybrid 6. DCD, DHP and Switchers are directly mounted on the silicon support of the DEPFET matrix. Wire bonds connect the matrix to the PCB.

optimization (undervolting of the converter) writing was possible without damaging the Switcher, but a reset could only be applied with switching the converter on and off.

After the beam test, the third matrix (I00) was assembled with all Switchers but only one DCD/DHP pair[3]. A fix for the Switcher JTAG communication was applied, so that both reading and writing was possible, but the other problems remained.

This chapter describes the optimizations and measurements done on the Hybrid 6 system, specifically the Hybrid with matrix I00, unless otherwise mentioned. This module is shown in figure 8.1. Chapter 8.1 describes the optimization of the delay elements to achieve a stable readout.

The pedestal distribution width is larger than the dynamic range of the DCD. To read out all pixel, the pedestal compression functionality in the DCD needs to be used. For this, an optimization algorithm was developed and tested with simulations. This is laid out in chapter 8.2, together with conclusions drawn for further improvements of the DCD. Chapter 8.4 describes matrix parameter measurements performed with a laser setup. During a beam test campaign, several of the measurements were repeated using 4 GeV electrons at DESY. In chapter 8.5, these measurements are presented and compared to those from the laser setup.

Further optimizations, like determination of coarse delay settings, DHE/DHP trigger delay settings and high speed link optimizations, were performed in the scope of this thesis to ensure reliable and correct data taking. Due to their technical and often rather simple but tedious nature, they will not be further elaborated on. Their main result is a working, usable system.

As explained in chapter 5.2.5, the system could only run at 250 MHz. Since both laser and beam measurements were focusing on sensor performance, the speed was further reduced. While ASICs were run at 250 MHz, each gate of the matrix was sampled twice before the next gate was switched on, resulting in an effective gate readout time of 256 ns. The first sample showed some artifacts and was discarded; the second sample was used for the analysis of the sensor performance. The results of this analysis are presented in chapter 8.3.

Both modules were operated at a *gate-on* voltage of −4.3 V, which is considerably more negative than

[3] Some drain lines for the other DCDs are shorted to source. If connected to a DCD, the voltage on these drain lines would destroy the ASIC. Repairing this by removing individual DCD bump bonds would only be possible with a high risk, so it was omitted.

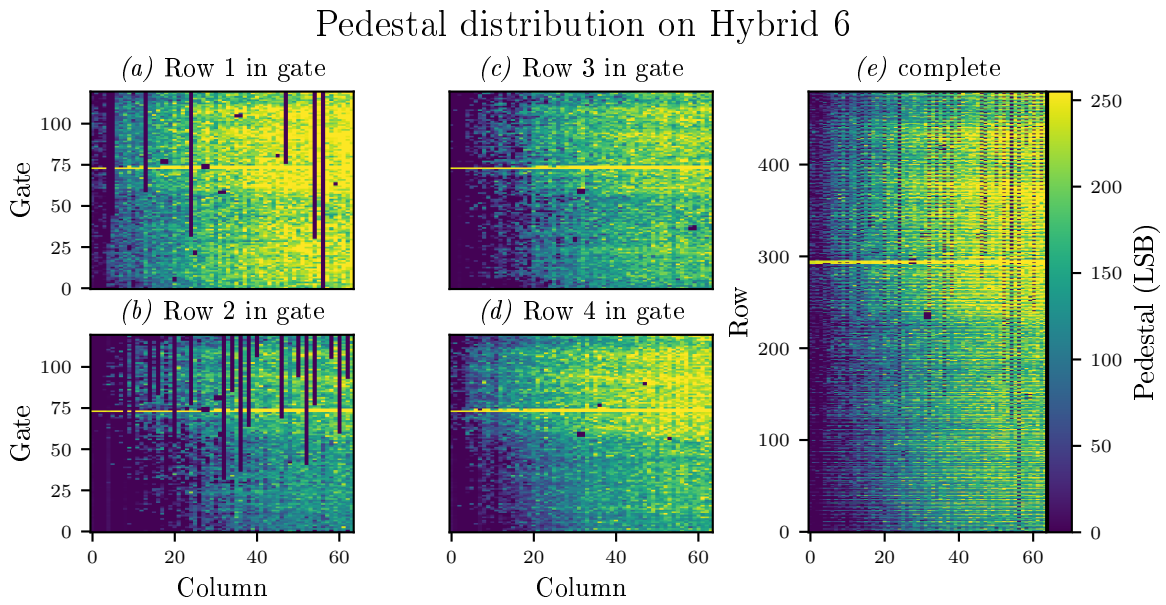


Figure 8.2: Pedestal distribution of matrix J00. *(a)-(d)* show the pedestal distribution of one DCD separated by which row in the gate the pedestal is. The individual rows show similar gradiends but their absolute value is different, with row 1 having the lowest pedestal and row 2 having the highest. The dark lines are broken drain lines. On both large PXD6 modules they appear only in row 1 and 2 in the gate, with many more appearing in row 1. *(e)* shows the pedestal map of all 3 DCDs. The pedestal gradients correspond with the direction of the analog power supply.

expected. Measuring the *source* current at the power supply, the mean drain current I_D was estimated to be $(65 \pm 10)\,\mu\text{A}$. With DEPFETs switched off, the *source* current was not zero since the source line is the ground line for several voltages. Thus, the measurement has a large systematic uncertainty. I_D is expected to be around $100\,\mu\text{A}$ for *gate-on* of $-2.5\,\text{V}$, and higher for more negative *gate-on* voltages, but both modules needed considerably more negative voltages. The voltages were checked to be correct on the PCB, using test points as close to the wirebonds as possible. Possible reasons for this could be a bad power connection between the matrix and the PCB or be related to transistor properties on the matrix. What points to the latter is the strong variation of the DEPFET pedestal currents which are very inhomogeneous with a strong structure repeating each gate, even at these low currents. Thus, both modules were used at a lower I_D; a fact which results in a lower g_q.

The pedestal distribution of all three DCDs of module J00 are shown in figure 8.2 *(e)*. It contains two effects worth to note:

- The four sub-rows in each gate show large differences in pedestals, while the same sub-row in each gate is similar. The four plots in figure 8.2 *(a)-(d)* illustrate this. Every plot contains the same sub-row from each gate read by DCD 1 (the rows 1, 5, 9,... are in one plot, the rows 2, 6, 10,... are in a different plot and so on). Separating rows like this leaves the system without a row-like structure. Thus, row 2 in gate N is more similar to row 2 in gate $N \pm 1$ than it is to its direct neighbor rows.

- The strong gradients along the rows in figure 8.2 *(e)* are most probably due to bad powering on the PXD6 module. ASIC pair 1 shows falling pedestal values going from low to high column indices,

ASIC pair 3 shows increasing pedestals when going from low to high column indices. ASIC pair 2 shows a gradient similar to ASIC pair 1 but less pronounced. Further, the DCDs of ASIC pairs 1 and 3 show columns with reduced dynamic range. This can be explained by a voltage drop along the DCDs and its supply lines. Each DCD has individual power lines. DCD 1 and DCD 3 are each powered from one side with the power connector on opposite sides, the analog part of DCD 2 is powered from the same side as DCD 1, its digital part is powered like DCD 3. These issues are fixed for final modules[4].

The remaining gradient along the columns is most likely due to an inhomogeneity introduced during wafer processing. It is different for both sensors, which supports this hypothesis. The plots 8.2 *(a)-(d)* show one drain line per column. In these plots, broken drain lines are dark strips. These only appear in row 1 and 2 in each gate and row 1 shows this defect much more frequent. Further, drain lines in row 1 are only broken in they belong to an even column, while row 2 has broken drain lines both in even and odd columns. Each row in one gate has a slightly different connection and layout of its corresponding drain line. The effects observed during the production of PXD6 sensors have led to an optimization of the production, by performing multiple metalization tests, process parameters optimizations and changes in critical areas of the pixel layout. Together, these changes will minimize metalization issues for final Belle II pixel modules [78].

8.1 Delay Optimization

The DCD/DHP communication is influenced by three parameters. The first parameter is the DCDs digital supply voltage, which directly influences the bias current for the transmitter. A higher bias current results in a larger difference between the high and low level, which should increase the data integrity. The second parameter is the delays used between the internal DHP clock which steers data sampling and the clock signal provided for the DCD. The last parameter is the delay between the internal DHP synchronization signal and the row sync signal provided to the DCD.

Initial settings for the delay elements were provided for a clock speed of 160 MHz, but they did not work properly at higher clock speeds ([49], page 73).

Changing each of the initial parameters independently decreases the data integrity – so a 2D measurement over the two delay settings was performed. The DCD has a built-in test pattern for these purposes, but the test pattern is rather weak: Some lines do not change their signals, the other lines repeat their output very often. Receiving the correct test pattern does not guarantee to have a good communication, so the data from the raw matrix readout was used. With the pedestal spread being wider than the DCD input range, all possible data words (-127 to $+127$) from the DCD are expected to be seen. Further, the word -128 should not appear as the ADCs in the DCD cannot produce that output code.

With this, three quality criteria can be specified:

- Due to the large pedestal spread on the matrix, the frequency how often each pedestal value is measured should have a similar order of magnitude. When communication is bad, some bits are stuck, so that some words are expected to be measured much more frequently or much more rarely. To quantify this, the standard deviation of the logarithm of pedestal value appearance is calculated. If words appear similarly often (same/similar order of magnitude), the logarithms of their appearances are similar and the standard deviation of these numbers is small. For this

[4] On Hybrid 6, DCDs are powered over wirebonds and 0.5 µm thick aluminum traces. Final modules will distribute power over 1 µm thick copper and 0.5 µm thick aluminum traces. In addition, power distribution in the DCD has been improved.

measurement, the over/underflow bins and their neighbors need to be neglected[5]. The result should be neither too low nor too high.

- The value -128 can only appear due to bit errors, thus the number of occurrences of this word is a measure of the transmission quality. Good settings should not show this value.
- When the communication is impaired due to a bad row synchronization delay, the DCD will put out values one clock cycle later and every pixel gets the value of its neighbor. If this effect is stable, it can be mitigated by shifting the syncrhonization signals by one clock cycle in digital domain. If the row synchronization signal has a bad phase, this effect is not stable and will impair the system performance. Each pixel may jump between its own data and data of its neighbor or the DCD will work with reduced performance as it gets the synchronization signal not every 128 clock cycles but sometimes after 127 or 129 clock cycles. This effect can be detected by comparing multiple readouts pixel by pixel. With good timing the signal should be similar in each frame. To quantify this effect, all pixels which change by more than 12 between two frames were marked as bad readouts and were counted. Changing the row synchronization signal changes the sampling point with respect to the Switcher sequence. Thus, small changes in the pedestal distribution are expected when varying the row synchronization. Not usable (bad) readouts can further occur due to bit errors.

Both delay parameters have 32 settings. As shown in [55], the delay elements are not linear, they have a large jump between settings 15 and 16. At this point, a jump between the measured values can be observed. Both delays work in the same direction, so the diagonal structures in the measurement are expected. For each of the setting combinations, 20 raw memory dumps were recorded and the number of bad readouts, the number of forbidden values (-128) and the logarithmic homogeneity of the pedestal histogram were determined for every pair of delay measurement, resulting in figure 8.3 *(a)* - *(c)*. A result of a pedestal distribution with good delay setting is shown in figure 8.3 *(a)*, a distribution with bad settings is shown in 8.3 *(e)*. For a clock speed of 250 MHz, the new values used are clock delay 6 and sync delay 9, resulting in an error-free communication.

8.2 Pedestal Compression

The DCD features dynamically switchable 2-bit DACs to reduce pedestal spread by adding a current to the pedestals. The data needed for the 2-bit DACs are streamed from the DHP, the LSB width of the 2-bit DAC can be set by the pDAC setting in the DCD. An example of this process is sketched in figure 8.4. This chapter describes previous work and its limits. Then, a new algorithm is proposed to overcome these limits. The algorithm is characterized using a simulated matrix and DCD; finally its performance on real data is shown using a Hybrid 6.

8.2.1 Previous Algorithm

A first algorithm was proposed and measured with DCDBv1 in [47]. This algorithm assumes a Gaussian pedestal distribution and tries to reduce the width σ of the distribution. Therefore the initial pedestal distribution is measured and the μ_0 and σ_0 of the distribution is determined by fitting a normal distribution and extracting the fit parameters. Pedestals between $\mu_0 \pm 2k\sigma_0$ are considered and the distribution is split

[5] Over/Underflow bins hold all values not in range. In this configuration, some DCD channels do not reach the maximum/minimum bin, so all bins above +120 and below -115 LSB are ignored for this measurement.

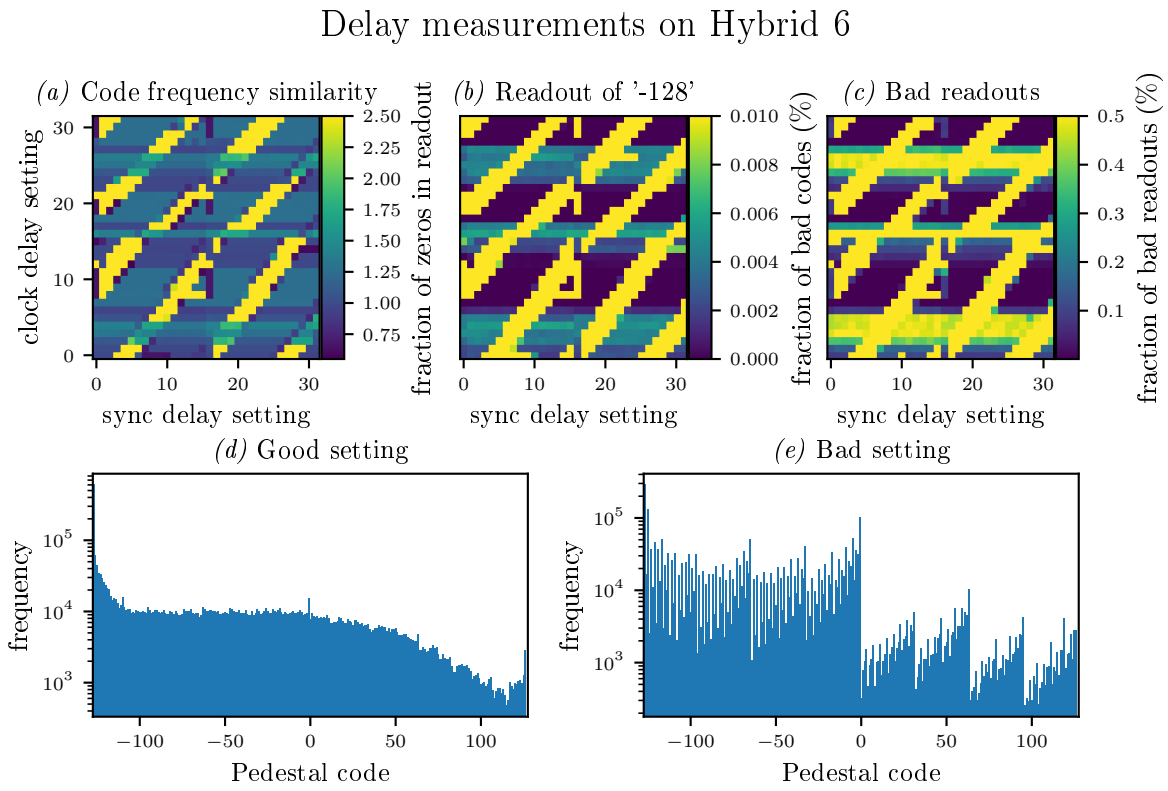


Figure 8.3: Delay measurement results for Hybrid 6. *(a)-(c)* show different quality criteria. *(b)* and *(c)* should be at zero for good settings, while *(a)* should not change in the area of a good setting and is useful to determine the optimal area. The setting choosen should be in the middle of a good area. *(d)* shows a good result. Many pixels are below the acceptance region, thus the peak at the lower border. *(e)* shows a result which is bad due to bit errors and shows multiple pattern spaced by 2^n codes.

in 4 bins: Bin 3 contains pixels with pedestal below $\mu_0 - k\sigma_0$, Bin 2 pixels between $\mu_0 - k\sigma_0$ and μ_0, Bin 1 pixels between μ_0 and $\mu_0 + k\sigma_0$, Bin 0 contains all pixels above $\mu_0 + k\sigma_0$ and is the bin all pixels should be in after offset correction. If pedestals from Bins 1-3 are shifted into Bin 0 by applying offset DACs, the resulting mean of the distribution is at $\mu_{\text{result}} = \mu_0 + 1.5k\sigma_0$. With this algorithm, different values for k result in different final pedestal width σ_{result}. Simulation in [47] showed a value of $k \approx 1$ is best to reduce the distribution width. The expected width is $\sigma_{\text{result}} = 0.34{\sigma_0}^6$. A practical implementation of this is achieved taking calibration data for all offset settings at different pDAC settings. For each pDAC setting, the offset is chosen so that the distance between the pedestal value and the target mean $\mu_0 + 1.5k\sigma_0$ is minimized. With the known optimal DAC settings the width of the virtual pedestal distribution at this pDAC value is determined. This is repeated for all pDAC settings and the pDAC setting where the standard deviation of the pedestal distribution is minimal is selected as optimal result. An experiment with $k = 1.5$ ($\pm 3\sigma_0$) was performed and resulted in a reduction of the pedestal distribution width to $0.55\sigma_0$, higher than the expected width of $0.44\sigma_0$ for this k.

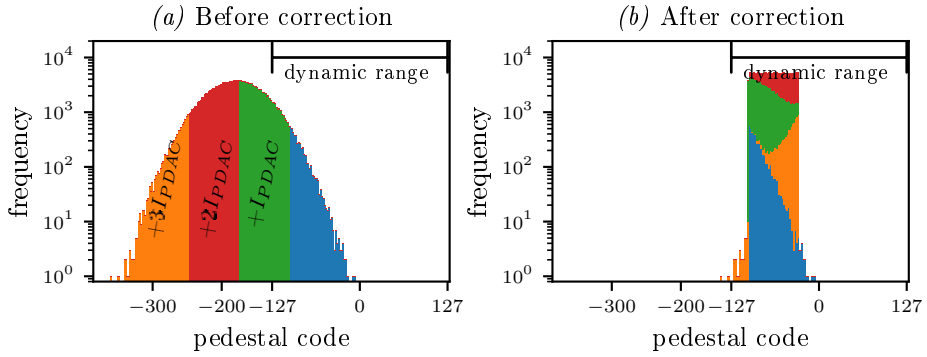


Figure 8.4: Explanation of pedestal compression algorithm showing pedestal distribution before and after optimization. Most of the pedestals are outside of the DCDs dynamic range before the optimization. Using the Offset DAC settings, a current of 0, I_{pDAC}, $2I_{\text{pDAC}}$ or $3I_{\text{pDAC}}$ is added to some pixels which results in a reduced pedestal spread. These plots show an ideal case where all information is known a priori (i.e. also pedestal values outside the range of the DCD), all DACs are linear and no crosstalk happens.

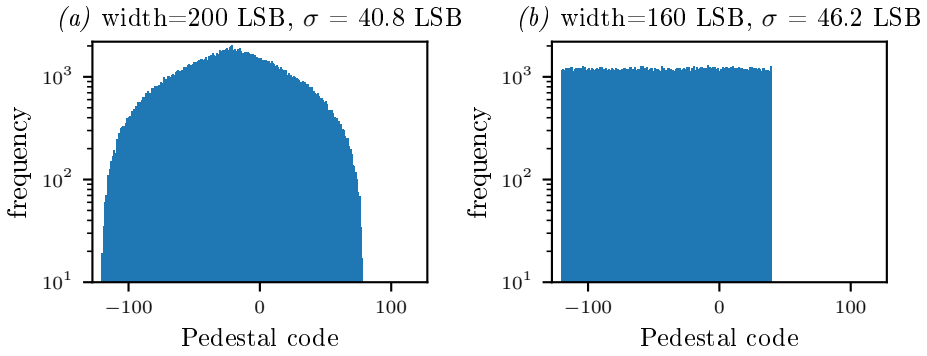


Figure 8.5: Two pedestal distributions with different widths and σ. The old algorithm would chose *(a)*, while *(b)* offers more headroom for signal.

8.2.2 Limits of Previous Algorithm

The previous algorithm has some limitations, which encouraged the development of an improved algorithm:

1. The algorithm assumes a gaussian pedestal distribution, while matrices can have an arbitrary distribution.

2. The algorithm needs a known distribution, so most of the pedestal distribution needs to be within the dynamic range of the DCD. Offset DACs are used to compress wide pedestal distributions which may be wider than the dynamic range. Since the Offset DACs can only add current, the DCD needs to be configured so it has the uppermost quarter of the pedestal distribution in its dynamic range so that the resulting distribution can have the maximum headroom for signal. This is illustrated in figure 8.4. Thus, up to $\frac{3}{4}$ of the pedestal distributions width is unknown, typically containing the center of the distribution where most pedestal values are.

[6] assuming arbitrary adjustable offset strength

3. The algorithm is not stable and can yield unusable results: If the distribution and thus the target mean is too high or too low, a given solution can be to use a very high/low I_{pDAC} current so that almost all pixels end up in the overflow bins; resulting in an extremely small distribution width but an almost completely blind detector.

4. The σ of the pedestal distribution is a non-ideal optimization parameter. Figure 8.5 shows two distributions where the distribution with smaller σ is worse than the other distribution, which offers superior signal headroom.

5. Broken pixels (e.g. disconnected drain lines) are not taken into account; ADCs with limited dynamic range (e.g. ADCs with a minimum code larger than -127) may be seen as in range while being out of range. Therefore an optimization might yield insensitive out of range pixels which are not noticeable on the final pedestal distribution.

The first two issues can be addressed by changes to the algorithm; issues 3 and 4 are addressed by changes in the algorithm's quality determination function. Issue 5 needs changes in both algorithm and quality determination function.

8.2.3 Improved Pedestal Subtraction Algorithm

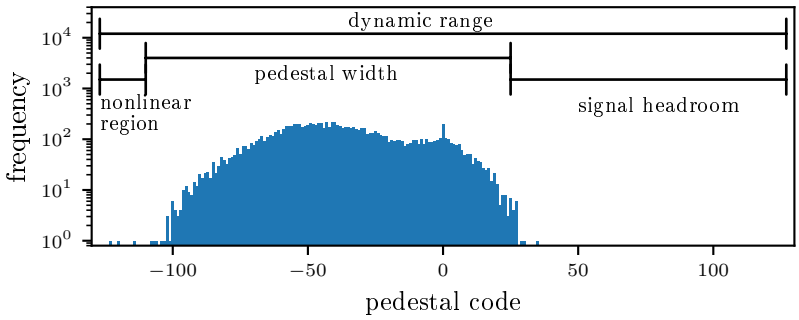


Figure 8.6: Illustration of dynamic range, pedestal width, signal headroom and nonlinear region. Task of the Offset DAC algorithm is to maximize the signal headroom

For detector operation, the maximum number of pixels in the detector should work. To achieve that, as many pixels as possible should

1. be in the dynamic range of the DCD

2. have a large enough headroom for signal.

As laid out in chapter 4, the signal needs to be large enough to cope with the signal generated by slow pions. A larger headroom is nice but will not increase the physics performance of the detector which is given by its position resolution, efficiency and capability to detect slow pions. Thus, the algorithm shown does not try to make the typical pixel better, but tries to make "bad" performing pixels as good as possible[7]. The headroom is most critical to pixels with a high pedestal after correction, so the headroom

[7] Optimizing broken pixels and extreme outliers may severely degrade performance, so a few pixels are cut out from the optimization. The cut percentage is one of the variables used to tweak the algorithm

of these pixels will be maximized. Figure 8.6 shows the relation between dynamic range, signal headroom and pedestal width.

Since the position of a pixel within the dynamic range of the DCD can be changed using SubIn and the *gate-on* voltage applied during readout, the pedestal distribution can be moved up or down after the optimization. Thus, the headroom is maximal if the pedestal distribution width is minimal. The lowest ADC values of the DCD are typically nonlinear. Thus, the lowest ADC value should be above some minimum ADC value. Respecting the previous points, pDAC and the 2-bit offset DACs need to be optimized. This is achieved by the following algorithm:

1. Determine if the pixel is in the dynamic range:
   a) The pedestal values for all pixels is determined
   b) A small current is added (in the order of an ADC LSB) using $\mathrm{Sub_{Out}}$ on the DCD.
   c) 1a and 1b are repeated several times for $\mathrm{Sub_{Out}}$ values between 0 and 20. Pixel within the dynamic range will show an increase in pedestal; pixel outside the dynamic range will show no increase[8].
   d) From this data, a minimum pedestal map is calculated: Pixels within the dynamic range are assigned a minimum pedestal of -127 since they will always stay above the lower border of the dynamic range. Pixels outside the dynamic range are assigned a minimum pedestal of their current value plus 5 LSB to avoid the nonlinear ADC range.
2. A similar map could be produced for high thresholds, but up to now, no optimized DCD had any problems with limited range or nonlinearities at the upper border of its dynamic range. Therefore a constant threshold is assumed.
3. Calibration data is taken analog to the previous algorithm: All pixel use the same 2-bit DAC setting and for each combination of pDAC and 2-bit DAC setting, raw frames are recorded as calibration.
4. A bad pixel list is determined. A pixel is regarded bad if it is not below the high threshold from step 2 when adding no current (pDAC setting 0)[9] or if it never is above the minimum pedestal threshold determined in step 1. Bad pixels given by the user are added to the list (i.e. known broken pixel or ADCs, unconnected drain lines etc.).
5. Using the calibration data, the offset calibration is performed. Since no distribution is known, the target value for the mean is not known a priori. Thus, several target mean values are tried and later the best one is chosen, fixing issue 1 and 2. For each pDAC setting and possible target mean value:
   a) The optimal offset DAC values are determined. From the four 2-bit DAC settings, the one is chosen which is closest to the target mean, ignoring DAC values which have a pedestal below the minimum pedestal determined in step 1 or above the high threshold set in step 2. Already in this step, the algorithm tries to avoid pixels out of the dynamic range. Pixels which are never above the minimum pedestal will be set to DAC value 3, pixels which are never below the high threshold will be set to DAC value 0, so that the pixels are as close to the dynamic

[8] Pixels 'just' outside the dynamic range can be identified by comparing the slope of the first few measurement points with the slope of the last few measurement points. Pixels so close to the dynamic range that they change their value already on the first step and therefore cannot be noticed by this mechanism are implicitly in the dynamic range: During detector operation $\mathrm{Sub_{Out}}$ is set to 2 by default so that some current is added to all pixels, pushing those pixels into dynamic range.

[9] ADCs receiving way too much current show strange effects where they at some values put out ADC codes below their maximum code —- so a "never show below high threshold" condition could lead to bad pixels not being recognized

range as possible. If a pixel only has DAC settings resulting in too high and too low pedestal values, a too low pedestal value is chosen[10].

b) The quality of this setting is determined using the 2-bit DAC settings determined above to create a virtual pedestal distribution from the calibration data. The quality of the distribution is given as a number, where lower numbers indicate better quality. For quality determination, pixels marked as bad in step 4 are ignored. The quality is then determined by the number of pixels above the dynamic range or below their pedestal value from the minimum pedestal map, the width of the distribution and the highest pedestal appearing in the distribution. The largest penalty is applied for pixels above the high threshold; a slightly lower penalty is applied for pixels below the minimum pedestal value. The width of the distribution is applied as a considerably smaller penalty so that the algorithm first tries to find setting with all pixels in the dynamic range before trying to reduce width. A very small penalty is applied for the highest pedestal in the pedestal distribution. It acts as a tie breaker if several settings have the same amount of bad pixels and similar distribution width. In this case the setting with the lowest high pedestal should be taken. The idea behind this is that while this can be achieved by other settings, changing these may also slightly degrade performance too[11]. The values for the high and low pedestal of the distribution are taken from the quantiles of the distribution, so that outliers like non-found broken pixels can be ignored. The default quantiles used are the 0.1 % and the 99.9 % quantile. While the quality of the distribution is determined without bad pixel, all pixels are optimized. A false flagged bad pixels still will get an optimal offset DAC setting.

c) After determining the quality of each setting, the mean and pDAC value resulting in the best overall setting are selected.

The above algorithm removes all issues discussed before. Since no distribution is used, issue 1 and 2 are solved. The price for this is a longer calculation time, but since it is below 20 seconds for each DCD/DHP pair in a large Belle II modules on a single core, this poses no real restriction. Issue 3 is resolved by a better selection process and a quality determination which is aware of bad pixels. Issue 4 is effectively solved by a better quality determination; issue 5 is solved by measuring and determining the dynamical range and taking this into account during 2-bit DAC selection and quality determination. The performance of the algorithm was investigated using a simulated DCD and matrix. The simulation assumes ideal, noise free ADCs and a constant pedestal distribution, so measurement results need to simulate only for one frame[12]. Like in the real DCD, a constant current is subtracted from the input and the currents given by the switchable current source are added. The switchable current sources are steered by the setting for pDAC, the constant current is steered by the setting for SubIn. The system simulates channel to channel differences in the constant current sources and in the three current sources the 2-bit DAC consists of. The pDAC and SubIn settings itself are simulated to be ideal and are much finer than in the real system. The simulation of the TIA contains two crosstalk sources:

- The intra-symbol crosstalk which depends on the current of the other channels during this digitization. This can be used to simulate voltage drops.
- The inter-symbol crosstalk which depends on the current the channel has digitized one gate earlier. This can be used to check for hysteresis effects.

[10] Pixels below the minimum pedestal may be blind, pixels above the high threshold *will* be blind
[11] Due to variations in the DCD current sources and variations in g_m of the DEPFET
[12] Inter symbol crosstalk needs a few extra gates prior to the first gate to be simulated

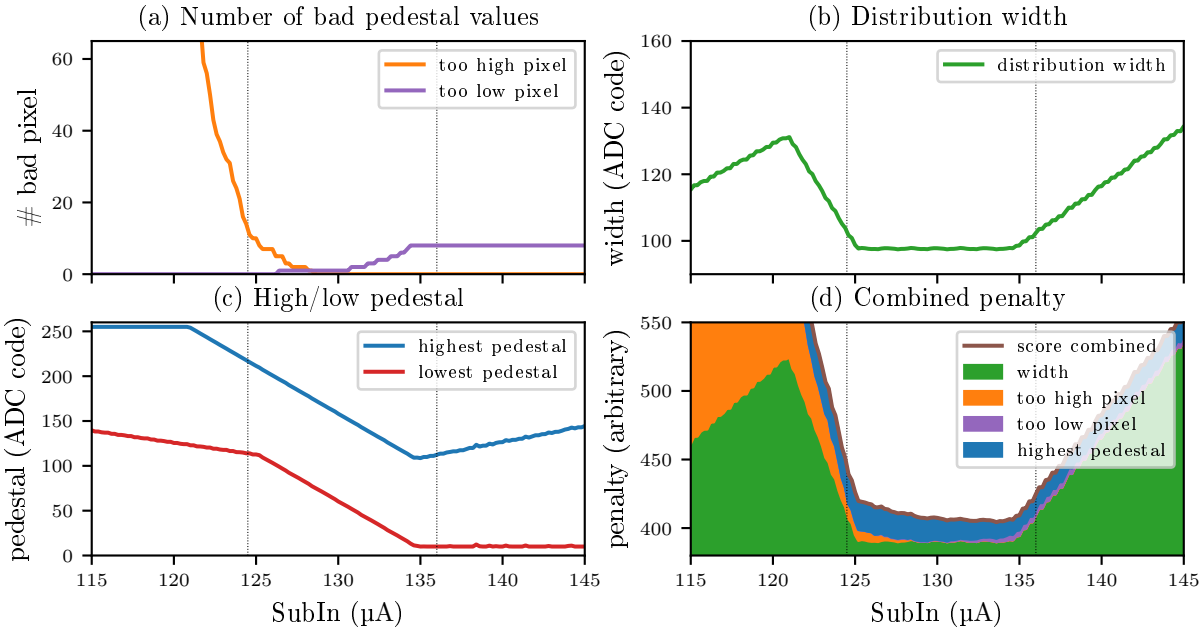


Figure 8.7: Example for resulting quality when changing SubIn. *(a)* shows the number of pixels outside the allowed range, *(b)* shows the pedestal distribution width and *(c)* shows the 99.9 % and 0.1 % quantile of the pedestal distribution. *(d)* shows the resulting scoring, where lowest is best. For the quality, *(a)* is more important than *(b)*. Only the 99.9 % quantile from *(c)* is used. It is least important for optimization.

Using the simulation, the offset DAC algorithm was tested and characterized by different pedestal distributions. The width of a pedestal distribution can result from different effects:

- Variations of the (measured) current in column direction can be caused by the matrix and by voltage drops along the DCD and its supply lines, as seen on Hybrid 6.
- Variations in row direction are mainly caused by the matrix. Voltage drops along the *gate-on* supply line could result in a gradient, but since the power consumption in this line is rather low and the effects seen on matrices are not linear, this effect is expected not to be large.
- Variations which repeat every four rows. This can result from the layout of the sensor, where some rows show a higher pedestals than others[13] or from the DCD which has different offset errors in each channel.
- Random pixel to pixel variations, due to production variations.

The pedestal compression algorithm needs to be able to cope with all these effects, thus 16 different pedestal distributions were created. Each pedestal distribution uses a different mixture of the effects above, their contributions are listed in B.2. Using these pedestal distributions, simulated data taking

[13] On new PXD9 DEPFET matrices even and odd rows have a different connection to the source voltage, which can change the pedestal current. On PXD6 matrices a similar effect can be seen which has a different reason. Ion implantation is performed under an angle of 7° with respect to the surface normal. Depending on the geometry, some ions can reach below masks on their border. On PXD9 this effect was reduces using "quad implantations", 4 implantation steps, where after each step the waver is rotated by 90°. [36]

was performed while changing single parameters of the simulated DCD. Using this data, the pedestal compression algorithm was used. Since all pixels on the matrix are good, no bad pixel map was used. The minimum good pedestal was fixed to -117 (10 above the minimum ADC code) instead of performing a range scan. The maximum good value was set to 82 (45 LSB[14]) below the maximum ADC code. If not stated otherwise, the optimization was performed with the 0.1 % and 99.9 % quantile, so 0.2 % of the pixels are regarded as outliers. The ADCs are set to a dynamic range of 24 µA.

8.2.3.1 Effect of SubIn

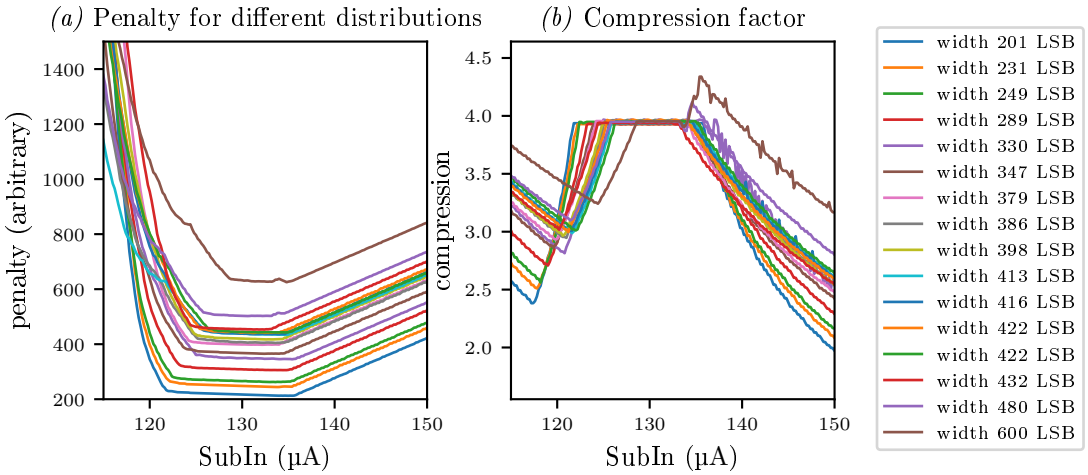


Figure 8.8: *(a)* Result for multiple pedestal distributions. The distribution width is determined by the 99.9 % and 0.1 % quantile before the compression. In the valley, the penalty is dominated by the width of the distribution. *(b)* shows the compression factor, which almost reaches the theoretical maximum of 4. For the two widest distributions there is a spike above 4, where both loose some pixels but therefor decrease their width, since pixel out of range show the ADC code of the under/overflow bin. Depending on the weights chosen for the optimization, this behavior could be changed. The chosen weights work well at reasonable distribution widths.

The simulation was performed for different SubIn currents. For each SubIn setting, a virtual offset measurement and an offset optimization were performed. Figure 8.7 shows the quality criteria for a single pedestal distribution. Below the right dashed line, many pixels are above the high threshold, so the result is bad. Between the dashed lines, almost all pixels are in the good area, resulting in a constant width. The score is only changed by the position of the 99.9 % quantile. Above the left dashed line, too much current is subtracted. Since the number of pixels in the dynamic range is more important, the algorithm sacrifices distribution width to keep all pixels in the dynamic range. Figure 8.8 *(a)* shows the total quality results for multiple distributions. All results have an optimal valley, where they yield similar results over several SubIn settings. In the valley all setting yield a similar performance where only the high edge of the distribution changes. This valley gets smaller for wide pedestal distributions. While an arbitrarily fine switchable SubIn would be ideal, even a SubIn with coarse steps of several µA will allow a good solution.

The compression ratio can be calculated as the width of the uncompressed distribution divided by the width of the compressed distribution. This is shown in figure 8.8 *(b)*. In each case, the width is calculated

[14] This corresponds to approximately twice the expected MPV of a MIP

by the 99.9 % and 0.1 % quantile. In their optimal plateau, all distributions show a compression close to 4, which is the theoretical maximum. This measurement shows that the algorithm works as expected.

8.2.3.2 Effect of pDAC LSB Width

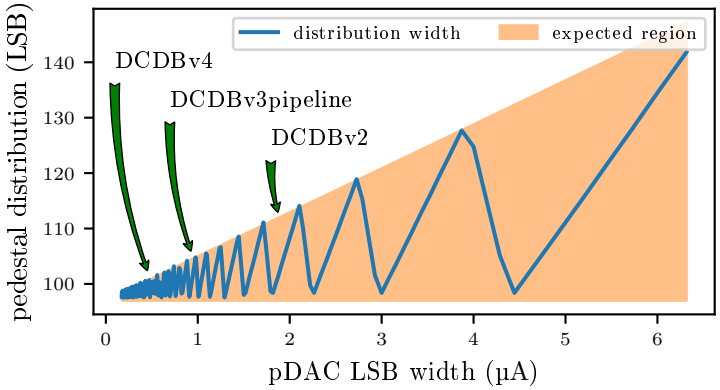


Figure 8.9: Simulation results for different pDAC granularities. The expected region only determined by the pedestal width. 0.1 to 99.9 % percentile) before compression and $I_{\text{pDAC LSB}}$. The optimization algorithm returns values which are slightly higher than expected, since it takes the number of bad pixels into account and sacrifices width to reduce this number. As a reference, the estimated (effective) pDAC LSB of diffferent DCD versions is given.

Using different pDAC granularity $I_{\text{pDAC LSB}}$ the algorithm was investigated. Depending on the specific maximum (I_{max}) / minimum (I_{min}) pedestal current in the distribution and the distribution width $\Delta I_{tot} = I_{max} - I_{min}$, a pDAC LSB width of $4nI_{\text{pDAC LSB}} = \Delta I_{tot}$ with $n \in \mathbb{N}$ result in good compression, other values result in worse pedestal compression. The optimal subtraction setting for a pedestal distribution of distribution width ΔI_{tot} = is $I_{\text{pDAC}} = {}^{\Delta I_{tot}}/_{4}$. After compression the pedestals will be between $I_{max} - ({}^{\Delta I_{tot}}/_{4})$ and I_{max}

- If I_{pDAC} is larger than optimal ($I_{\text{pDAC}} = {}^{\Delta I_{tot}}/_{4} + \Delta I$), the resulting distribution width is between $I_{max} - ({}^{\Delta I_{tot}}/_{4} + \Delta I)$ and I_{max}. The current of $3I_{\text{pDAC}}$ is added less often than in an optimal case and the distribution is ΔI wider than optimal

- If I_{pDAC} is smaller than optimal ($I_{\text{pDAC}} = {}^{I_{tot}}/_{4} - \Delta I$), not all pedestal can be compressed. For current between I_{min} and $I_{min} + 4\Delta I$, the current can't be added into the desired range of $I_{max} - ({}^{\Delta I_{tot}}/_{4} - \Delta I)$ and I_{max}, because no offset setting is strong enough. While the desired range is ΔI smaller than in the optimal case, it is enlarged by $4 * \Delta I$ due to the not handled pedestals, resulting in a distribution which is $3\Delta I$ wider than optimal.

For a given ΔI_{tot} and $I_{\text{pDAC LSB}}$, the algorithm can choose between using $I_{\text{pDAC }small}$ and $I_{\text{pDAC }large}$, with

$$I_{\text{pDAC }small} = n_{\text{pDAC}} * I_{\text{pDAC LSB}} \leq {}^{\Delta I_{tot}}/_{4} \leq (n_{\text{pDAC}} + 1) * I_{\text{pDAC LSB}} = I_{\text{pDAC }large}.$$

Assuming the optimal subtraction current to be $n_{\text{pDAC}} * I_{\text{pDAC LSB}} + \Delta I$ with $\Delta I \leq I_{\text{pDAC LSB}}$, the resulting distribution width when using $I_{\text{pDAC }small}$ is ${}^{\Delta I_{tot}}/_{4} + 3\Delta I$. Using $I_{\text{pDAC }large}$ results in ${}^{\Delta I_{tot}}/_{4} + (I_{\text{pDAC LSB}} - \Delta I)$. In the worst case, this results in a pedestal distribution that is ${}^{3}/_{4} I_{\text{pDAC LSB}}$ wider than optimal. The theoretical prediction and the simulation result is shown in 8.9, where the resulting width is plotted

against the $I_{\text{pDAC LSB}}$. Since the pedestal distribution is not known before, this worst case can happen during detector operation. The DCDBv2 used in this thesis effectively utilizes a 6 bit DAC with a range of 120 µA for the LSB, resulting in $I_{\text{pDAC LSB}} \approx 2\,\mu\text{A}$; the DCDBv3pipeline has a similar current range and a 7 bit DAC. Using input from these simulations, the next generation has an improved pDAC range of 60 µA, resulting in a $I_{\text{pDAC LSB}} \approx 0.5\,\mu\text{A}$. This will reduce the additional width due to pDAC granularity from ≈ 18 LSB to ≈ 5 LSB.

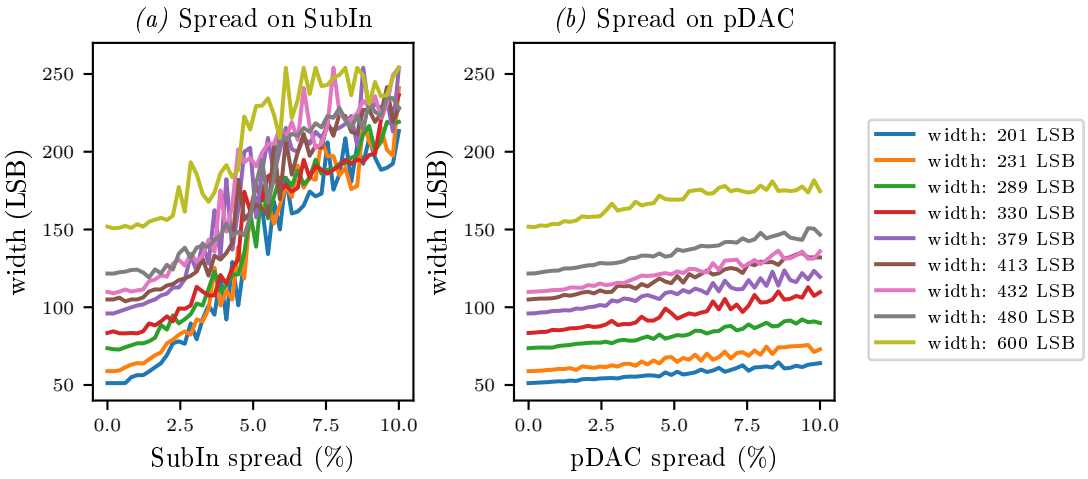


Figure 8.10: *(a)* Effect on the spread of SubIn on the effective pedestal width. *(b)* Effect on spread of pDAC on the effective pedestal width. The variations in each line of both plots are due to the simulation. For each simulation a new random spread is used for each SubIn.

8.2.3.3 Effect of Non-Ideal Current Cells

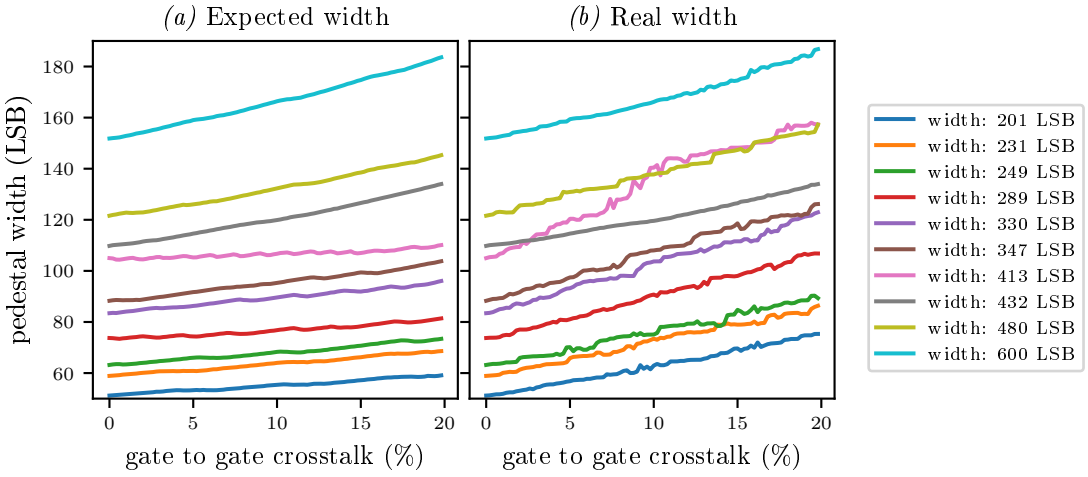


Figure 8.11: Simulation results for different gate to gate crosstalk coupling constants. Here the width expected by the pedestal compression algorithm (shown in *(a)*) differ from the real width (shown in *(a)*)

For these measurements, the input subtraction current sources and the current sources in the 2-bit

DACs are assumed to have channel to channel variations. These variations are implemented by drawing the DAC strength randomly from a normal distribution with the mean value at the expected strength and a σ of a percentage of the expected strength. Variation in the subtraction current sources should just increase the pedestal width, a result which is shown in figure 8.10 *(a)*. Since SubIn is very strong, even small variations have a large influence on the achieved pedestal width after optimization. This is an effect especially important for small pedestal distributions, since the pedestal compression algorithm needs to compress the pedestal distribution folded with the SubIn spread. For small pedestal distributions the width contribution from the SubIn spread gets dominant earlier. This can be seen on the plot: The shown pedestal distributions have different widths, but their width gets closer as the SubIn spread increases. The effect of the pDAC spread is shown in 8.10 *(b)*. It is smaller, since the pDAC current cells are less strong. In addition, each 2-bit DAC consists of 3 pDAC current sources, where the relative spread is expected to be lower than on a single current source. Since the algorithm does not rely on any linearity, it continues to work but results in wider distributions. For the DCDs, DAC spreads in the order of a percent are expected [79], which will not significantly decrease performance.

8.2.3.4 Effects of Gate to Gate Crosstalk

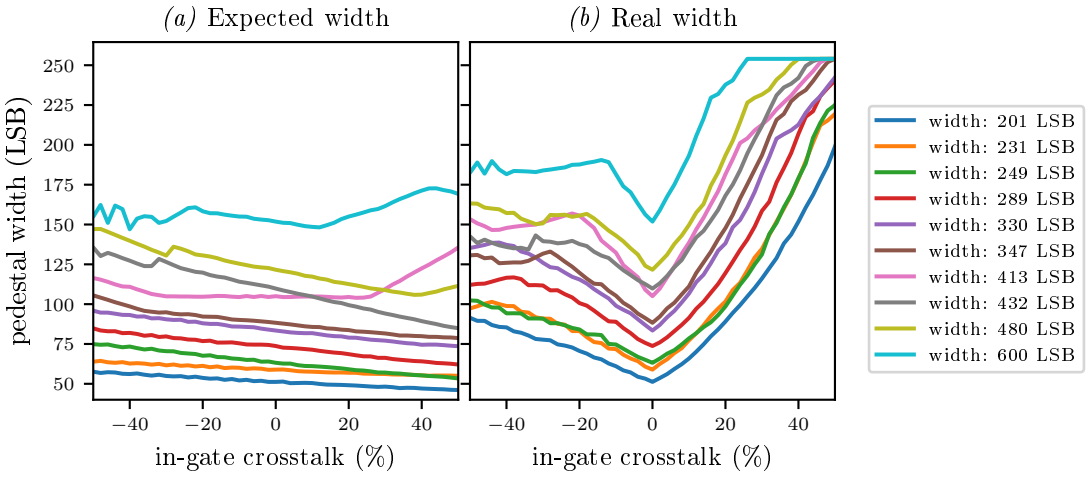


Figure 8.12: Simulation results for different in-gate crosstalk coupling constants. Here the width expected by the pedestal compression algorithm (shown in *(a)*) differs from the real width (shown in *(a)*).

The TIA in the DCD has a limited bandwidth, thus measurements could be influenced by current which was sampled previously. This effect is modeled by changing the ADC input current $I_{ADC\ in}$ to

$$I_{ADC\ in} = I_{Pedestal} - I_{\text{SubIn}} + d_{offset} \times I_{\text{pDAC}}$$

to

$$I_{ADC\ in} = I_{Pedestal} - I_{\text{SubIn}} + d_{offset} \times I_{\text{pDAC}} + c \times I_{ADC\ prev}, \tag{8.1}$$

with the pedestal current $I_{Pedestal}$, the global subtraction current I_{SubIn}, the offset correction current I_{pDAC}, the 2-bit DAC setting d_{offset} and the ADC current from the previous sampling $I_{ADC\ prev}$ which is modulated by a coupling constant c. If the offset correction uses the same current $d_{offset} \times I_{\text{pDAC}}$ at every sampling point, it just seems that I_{pDAC} and I_{SubIn} are stronger by a factor $1 + c$, while sampling a stronger pedestal current of $I_{Pedestal} + c \times I_{Pedestal\ prev}$, possibly making the measured pedestal distribution

wider. This is the case when taking calibration data for the offset measurement. During normal operation, consecutive pixels on the same drain line can have different 2-bit DAC settings, thus the ADC sees a current which differs from the expected by $\Delta I_{ADC\ in} = c \times \Delta d_{offset} \times I_{\mathrm{pDAC}}$, where $\Delta d_{offset} = d_{offset\ prev} - d_{offset}$. This degrades performance: When calculating the expected pedestal distribution, the algorithm uses data which is different from the real pedestal distribution. To determine the quality of the pedestal distribution, a measured pedestal distribution has to be used instead of the expected distribution. This is shown in figure 8.11, where *(a)* shows the width from the pedestal distribution expected by the offset algorithm. The expected distribution gets wider since in the calibration data the ADC input current is replaced by $I_{Pedestal} - I_{\mathrm{SubIn}} + d_{offset} \times I_{\mathrm{pDAC}} + c \times I_{ADC\ prev}$. This effect is smallest, if pedestals are purely random. If the pedestals on a matrix show a gradient along rows or columns, there is a positive correlation between $I_{Pedestal} - I_{\mathrm{SubIn}} + d_{offset} \times I_{\mathrm{pDAC}}$ and $I_{ADC\ prev}$, increasing the width. This can be seen in the plot: The curve with pedestal width 413 LSB is purely random and shows the smallest increase in width when looking at the expected width.

Figure 8.11 *(b)* shows the real width determined by the simulation. Here the width for some pedestal distributions increases more strongly than for others, depending on the distribution width of $\Delta I_{ADC\ in} = c \times \Delta d_{offset} \times I_{\mathrm{pDAC}}$.

For the tested pedestal distributions, this effect resulted in an 1.2 to 2.8 LSB increased distribution width per percent crosstalk. Effects from this could be mitigated by taking more calibration data. Instead of taking calibration data for each pDAC settings and each 2-bit DAC setting, pixels would need calibration data for each pDAC setting , each 2-bit DAC setting the pixel could have and each 2-bit DAC setting of the previous pixel on this drain line. From this, one could estimate $\Delta I_{ADC\ in}$ and use this to achieve better estimated pedestals. This would require 4 times the calibration data and considerably more computing power. Since on real devices the algorithm works well, this was not done.

8.2.3.5 Effects of In-Gate Crosstalk

The ADC response of a single channel could be influenced by current flowing into other ADC channels. This was simulated by modifying

$$I_{ADC\ in} = I_{Pedestal} - I_{\mathrm{SubIn}} + d_{offset} \times I_{\mathrm{pDAC}}$$

to

$$I_{ADC\ in} = I_{Pedestal} - I_{\mathrm{SubIn}} + d_{offset} \times I_{\mathrm{pDAC}} - c \times I_{ADC\ mean}$$

with the coupling constant c, the mean current flowing into all ADCs[15] $I_{ADC\ mean}$ and the other symbols defined as in formula 8.1. Here the coupling constant can be positive and negative. A coupling constant of $c = 1$ would subtract all common variations of the current, effectively negating effects from SubIn. Pedestal distributions which have a fluctuating mean pedestal for different rows could benefit from positive c constants since it partially negates the gradient. During calibration data taking, the effect of pDAC on the sensor will be over/underestimated by $c \times I_{\mathrm{pDAC}}$ and wrong calibration constants will be chosen. This is shown in figure 8.12. The estimated width in *(a)* gets better for most pedestal distribution for larger c since their initially measured width gets smaller, at least up to a point. Exception to this is again the distribution with width 413 LSB, since it has almost no variation in the mean pedestal in row direction. The real width shown in figure 8.12 *(b)* shows, that both under and overestimating the offsets results in a performance degradation. The measured width increases by 1.4 to 3 LSB per percent

[15] To avoid circular dependencies, the mean current is calculated only using $I_{Pedestal} - I_{\mathrm{SubIn}} + d_{offset} \times I_{\mathrm{pDAC}}$, the idea being that this effect acts like a current flowing into the ADC but is no real current.

crosstalk, with wider distributions getting a worse increase. Chapter 8.2.5 presents observations which could be explained by in-gate crosstalk. However, they only appear in extreme cases, where many drain lines are unconnected. For normal operation, real devices show no indication of an effect like this being present, though no in-depth measurement campaign has been performed to exclude it.

8.2.4 Results on Hybrid 6

All Hybrid 6 matrices show very wide pedestal distributions and need pedestal compression to have all pixel in the dynamic range. The pedestal of matrix I00 without pedestal compensation is shown in figure 8.13 *(a)*. Pedestal compression only can add current, thus most pixels would be below the dynamic range. In figure *(a)*, less current was subtracted from all pixels, so more pedestals are in the dynamic range and the width of the pedestals distribution is visible. After compression, the algorithm expects the distribution shown as map in *(b)* and as histogram in *(d)*. The measured result is shown in figure *(c)* and as histogram in *(e)*, and is very close to the expected value. The difference between both distributions is shown in *(f)* and has the mean of -1 LSB with a standard variation of 7.5 LSB. The pedestal distribution shown here has some headroom in both directions and was chosen like this to allow variation of matrix bias voltages which increase and decrease the pedestal. For Belle II detector operation, a higher SubIn setting could be used to shift pedestals towards lower ADC codes and increase headroom for signal. Using a higher SubIn setting during optimization would decrease the length of the distribution tail towards high pedestal codes, but increase the width of the distribution center.

8.2.5 Results on Other Devices

On both Hybrid 5 and final detector modules, some DCD channels are not connected to the matrix. On Hybrid 5, half of the channels are not connected to the matrix and thus out of their dynamic range. It was observed that sourcing current in these channels changes the response of the connected channels. During calibration data taking, the unconnected channels get the same 2-bit DAC setting as the other channels; during operation, the algorithm sets them to the maximum DAC value per default. This difference leads to an underestimation of pedestal current when using low DAC settings, thus resulting in pixels with low DAC settings being overcompensated and resulting in a too high corrected pedestal. Setting unconnected pixels to a 2-bit DAC setting of 0 results in an undercompensation of pixels with a high DAC setting. This effect can be mitigated by excluding unconnected channels from calibration data taking: At each step during calibration data taking, unconnected channels use the same 2-bit DAC setting (for example 0). After optimization unconnected channels are set to this setting. Using this, the resulting pedestal distribution width after optimization can be decreased.

Final detector modules only have a small fraction of channels not connected; so on these modules the effects are expected to be less pronounced than on Hybrid 5, but for optimal performance, the same strategy should be used.

8.3 Optimization of Switcher Sequences

The matrix used on Hybrid 6 has 7.5 times the number of gates and longer drain lines compared to small test matrices. Thus, the drain line capacity increased significantly, which has influences on the settling times of the drain currents. To optimize the time when the DCD samples its input current, a sampling point curve is recorded. This measurement is performed by varying the phase between Switcher operation and the sampling point of the DCD, to find a sampling point which has a settled current and is close to the clear pulse, since data arriving between the sampling and the clear pulse in the currently read gate is lost.

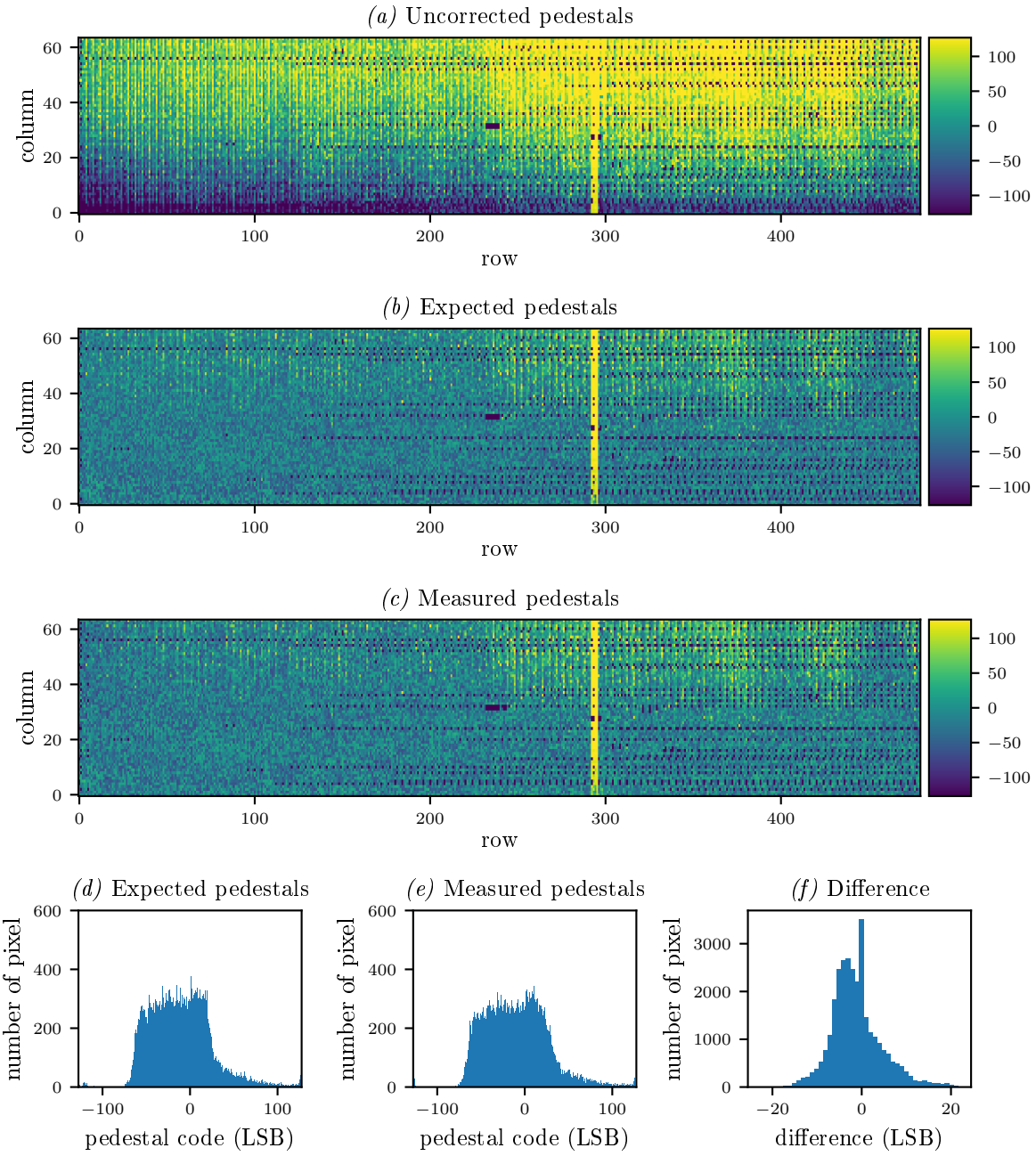


Figure 8.13: *(a)* Before correction, the pedestal distribution spans the complete dynamic range. *(b)* and *(d)*: The pedestal distribution estimated by the algorithm. *(c)* and *(e)*: The measured pedestal distribution after compression. *(f)*: The difference between expected and measured pedestal code.

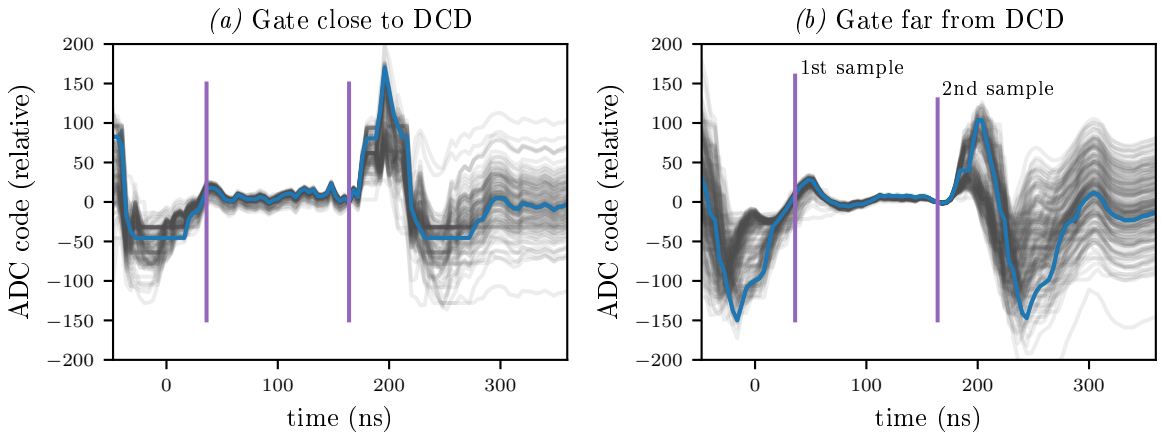


Figure 8.14: ADC signal versus sampling point. The sampling point is switched by changeing the phase of the Switcher signals with respect to the DCD sampling point. The ADC signal of a single drain line is highlighted, the 255 other drain lines are shown semi-transparent. All curves are normalized to have the value 0 at the second sample point. Two sample points are shown as vertical lines. During the first sample point the current is not settled, resulting in bad ADC codes. Several artifacts can be seen: The flat part at the valley is due to the signal being out of the dynamic range of the DCD. The flat regions of the spike are due to the DCD issues shown in table 5.1. Figure *(a)* shows the result for gate 10, close to the DCD. Figure *(b)* shows the result for gate 110, close to the end of the matrix.

In this measurement, some artifacts are expected since DCDBv2 samples twice. On dynamic signals, like a sampling point curve, both samples can have different values and artifacts listed in table 5.1 can appear. The result is shown in figure 8.14. After switching on a gate, the current settles until it reaches a plateau between 60 ns and 160 ns. When raising the clear line from *clear low* to *clear high*, current is capacitively injected into the drain line resulting in a high spike, which is seen starting at 190 ns. The valley around 240 ns is due to two effects: When clear is at a high voltage, the channel is influenced by the positive clear potential, decreasing the source drain current of the DEPFET. At the end of the clear process, the clear line is switched from *clear high* to *clear low*, creating a negative current spike on the drain lines. After the clear process, the next gate is activated and the current settles to a new value. The figure shows a sequence with 256 ns gate cycles, both for gates *(a)* close and *(b)* far from the DCD. The sequence is twice as long as normal. A normal sequence would need the clear pulse earlier when the drain current isn't completely settled. Since the system could not be used with a slower clock speed, each gate was sampled twice, discarding the first sample. This mitigated the issues shown in figure 8.15 *(a)* which shows the pedestals calculated at the first sample point. Here the pedestal codes -1 and 63 are measured more often than expected while codes slightly above -1 are measured less often. This is not stable, so many pixels in the sensor will be noisy, show a too low or high signal or will show less efficiency due to problems with the readout. These issues are not present at sample point 2 shown in 8.15 *(b)*. To determine sensor performance, only the second sample was used. Successors of the DCDBv2 will not have this problem since they sample input current only once.

8.4 Laser Measurements

For measurements using a laser, the laser system described in chapter 7.4 (page 81) was used. Using the water cooled block on the backside of the Hybrid 6 PCB, long measurements at stable temperatures

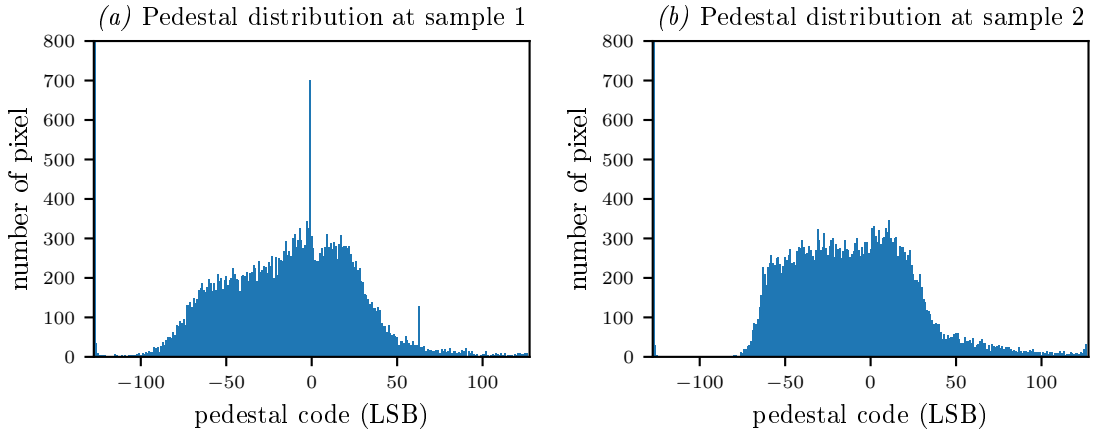


Figure 8.15: Pedestal distribution separated by sample point. *(a)* shows the first sample where pedestals are not settled. The spikes for pedestal codes -1 and 63 are due to the not settled signal. *(b)* The pedestal distribution for the second sample point is smaller and at has a higher mean value. It does not show spikes.

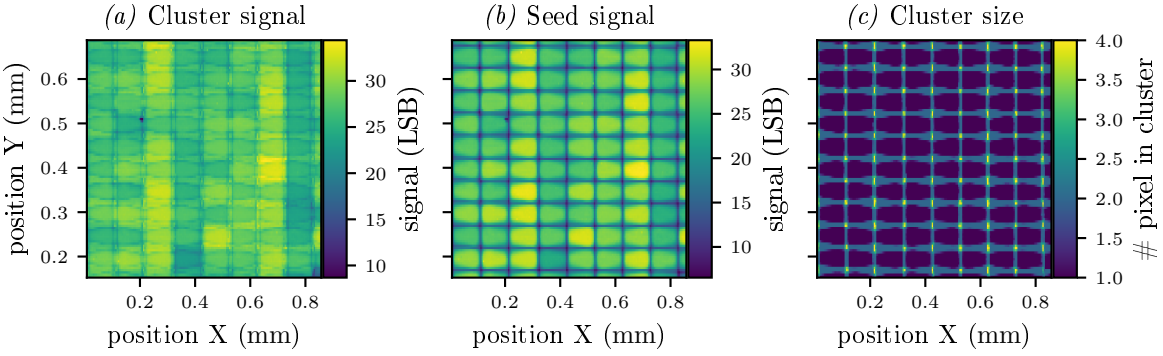


Figure 8.16: Laser measurement on Hybrid 6. Figure *(a)* shows the cluster signal, *(b)* shows the seed signal and *(c)* shows the cluster size depending on the laser position. The x axis is shown along the matrix row direction, the y axis is shown along the matrix column direction

could be taken. Similar to measurements performed on small matrices, laser pulses were injected into the matrix, producing electron-hole pairs. For each laser measurement shown in this chapter, the laser was moved to a total of 18190 positions laid out on a grid of 170×107 positions with a spacing of 5 µm in both directions, resulting in a total measurement area of $850 \times 535\,\mu m^2$. With a pixel size of $100 \times 50\,\mu m^2$, the area scanned was chosen so that 8 rows (2 gates) and 10 columns were fully covered. At each position, laser pulses were injected into the matrix and the sensor response was recorded 800 times[16]. To minimize environment effects during each 8:45h long measurement, the hybrid board was cooled using $(17.0 \pm 0.1)\,^{\circ}C$ warm water flowing through a large copper cooling block mounted on the backside of the Hybrid PCB. The measurements were performed in a $\approx 1\,m^3$ large aluminium box inside a climate controlled room with an air temperature of $(20 \pm 2)\,^{\circ}C$. Different to the measurements on small matrices, many low intensity pulses were used since the laser was not synchronized to the readout system. In addition, the injected signal was reduced to be around 1.5×MIP MPV to better reflect a typical particle.

[16] Recording data only took a fraction of the total measurement time, most time was used to wait for the motor table to reach its target position and to handle communication errors with the DHE

With lower signal, the readout threshold is more important. This can be seen on figure 8.16 *(a)*, where the mean deposited cluster charge is shown against the laser position. The seed signal is shown in figure 8.16 *(b)*. From the seed signal one can determine the pixel border, which can also be observed from the cluster size 8.16 *(c)*. Close to the pixel borders the reconstructed cluster signal is lower than expected since the shared part is smaller than the threshold and thus lost.

8.4.1 Measurements at Different Bias Voltages

Similar to measurements performed on Hybrid 5, the optimization is done in two main steps: First *drift* and *depletion* voltages are optimized, then the *capacitively coupled clear gate* and *clear low* voltages are optimized using optimal settings for the *depletion* and *drift* voltages. For each bias voltage setting, a laser measurement is performed. *clear high* was not optimized; the Switcher mounted on the large matrix has a nominal tolerance of 20 V between SW_{GND} and its highest potential, which results in maximum 13 V for *clear high* (which is referenced to *source*). From small pixel matrices and simulations this is known to be lower than optimal. For data taking, a voltage of 17 V was used which is above official specifications for the Switcher. In addition, the clear pulse length was increased by 4 ns to 20 ns, which should ensure a better clear of the internal gate.

Figure 8.17 shows the resulting cluster charge of these laser measurements for *drift* and *depletion*. Measurements were performed moving the laser along the row direction (which is referred to as X), taking data at each point. When one row of measurements was taken, the laser was moved in column direction (which is referred to as Y), and the next row was measured. In most measurements, a low signal is visible at X$\approx$ 0.2 mm, Y$\approx$ 0.51 mm. This is due to a dust particle on the backside of the matrix, which blocks part of the light.

Multiple measurements had to be repeated since the DHE firmware was prone to crashes[17]. Two data points with partially broken data were not replaced, both can be seen in figure 8.17. For *drift* = -7 V and *depletion* = -18 V, the data taking crashed due to issues with the firmware. The incomplete row and the missing row were excluded from all analysis. Since the measurement was almost done, it was not repeated. For *drift* = -5 V and *depletion* = -16 V, the DHE trigger stopped working correctly. Instead of recording 800 events for each measurement point, the DHE triggered mainly 0-2 times per measurement point and sometimes up to 100 times. Thus, lots of measurement points do not contain data. At positions where data was recorded, it agrees with expectation. Since the DHE apparently continued working and all files were correctly created, this error was not detected in time and the measurement was not repeated.

Similar to measurements performed on Hybrid 5, the quality of the detector response is quantified by two numbers, the mean signal which should be maximized and the width of the signal distribution, which should be minimal. A large signal width hints to a non homogeneous response, either due to nonworking pixel or due to charge loss in areas within a pixel. In addition, the mean cluster size can give information on the amount of charge sharing happening in the sensor. From this data, a summary plot for *drift* and *depletion* can be created which is shown in figure 8.18. The first row shows results for a 2D scan over both potentials; using the data which is shown in figure 8.17. This measurement shows a wide voltage range with good settings; excluding settings with *drift* = -1 V, all values are usable; though only settings with *depletion* = -18 V or *depletion* = -20 V are optimal. The mean cluster size for the good settings is around 1.4 - 1.5 pixels. A significantly smaller cluster size would hint towards charge being lost in the sensor; a significantly larger cluster size indicates missing charge separation. This can be seen for the setting *depletion* = -18 V, *drift* = -1 V in figure 8.17. The small, dot-like structures are areas where single pixel clusters are seen, but laser hits in the drift region always create two pixel cluster, in this case

[17] Recoverable errors happened every few minutes due to the trigger implementation. In addition, some non-recoverable errors happened every few day, which needed a cold start of the system.

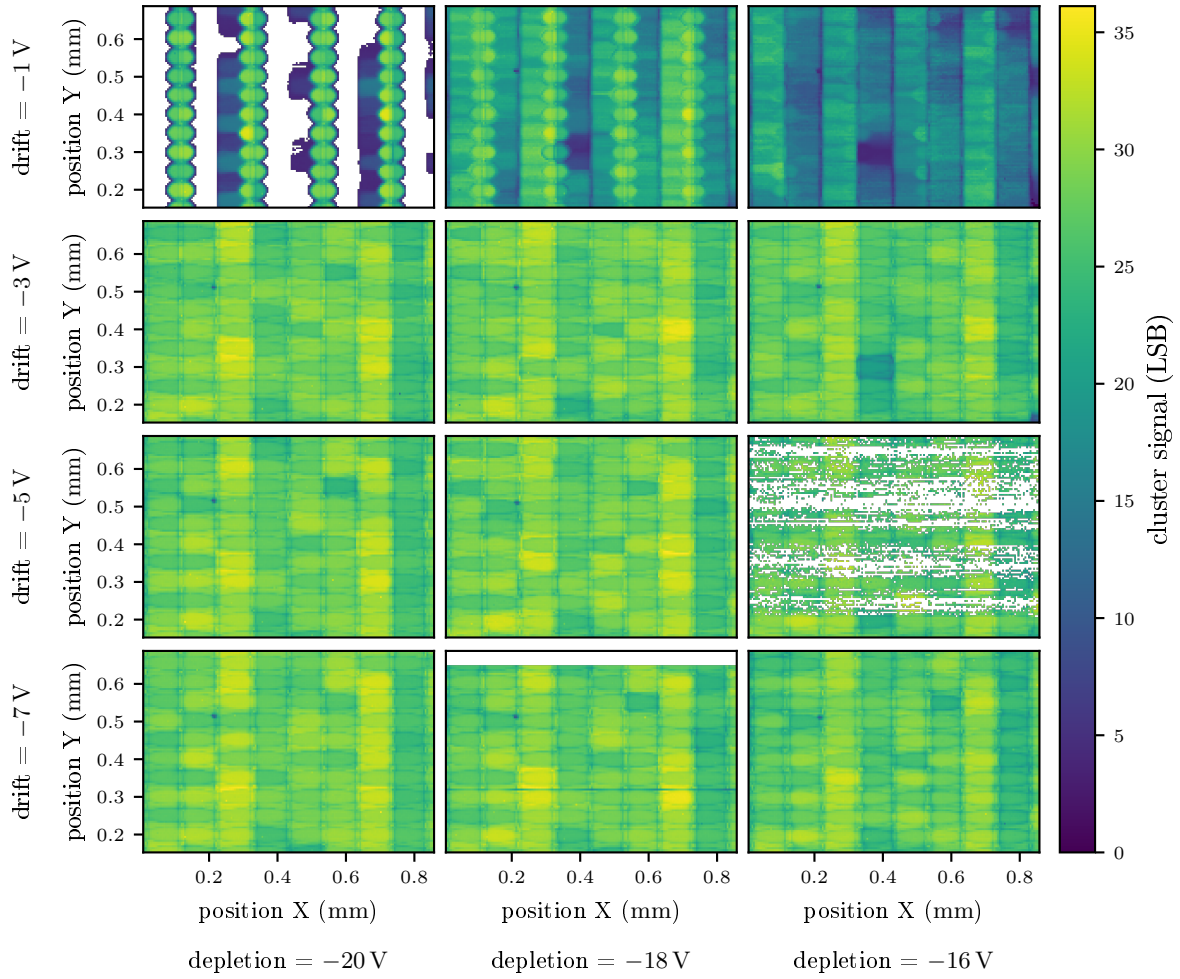


Figure 8.17: Cluster signal for different *drift* and *depletion* potentials settings at default *capacitively coupled clear gate* and *clear low* potentials.

reducing sensor resolution. For this setting, the large clusters appear because the drift fields are weak at the interface between the drift area and the surrounding clear gate structure, leading to long collection times and due to diffusion to charge sharing. For some pixels, most charge is still collected, while others show a significant decrease in measured charge.

The second and third row of figure 8.18 show 1D measurements, where one of the bias voltages was fixed while the other was varied. Varying *depletion* in the second row shows expected behavior. A *depletion* potential between −18 V and −20 V volt is best to get the highest possible signal with a good homogeneity. More positive *depletion* potentials lead more charge sharing. This can be used to slightly improve the sensor resolution while reducing the overall signal. More negative *depletion* lead to areas with charge loss within the sensor.

As seen from the last row of figure 8.18, all values for $drift \leq -3\,\mathrm{V}$ show a similar performance, $drift = -3\,\mathrm{V}$ shows the largest cluster size of the good settings and is used as optimal value.

The measurement results for *capacitively coupled clear gate* and *clear low* can be seen in figure 8.19, the summarized data is shown in figure 8.20. The operation window of *capacitively coupled clear gate* is between −2 V and −2.5 V, the operation window of *clear low* is between 3 V and 4 V. Several effects

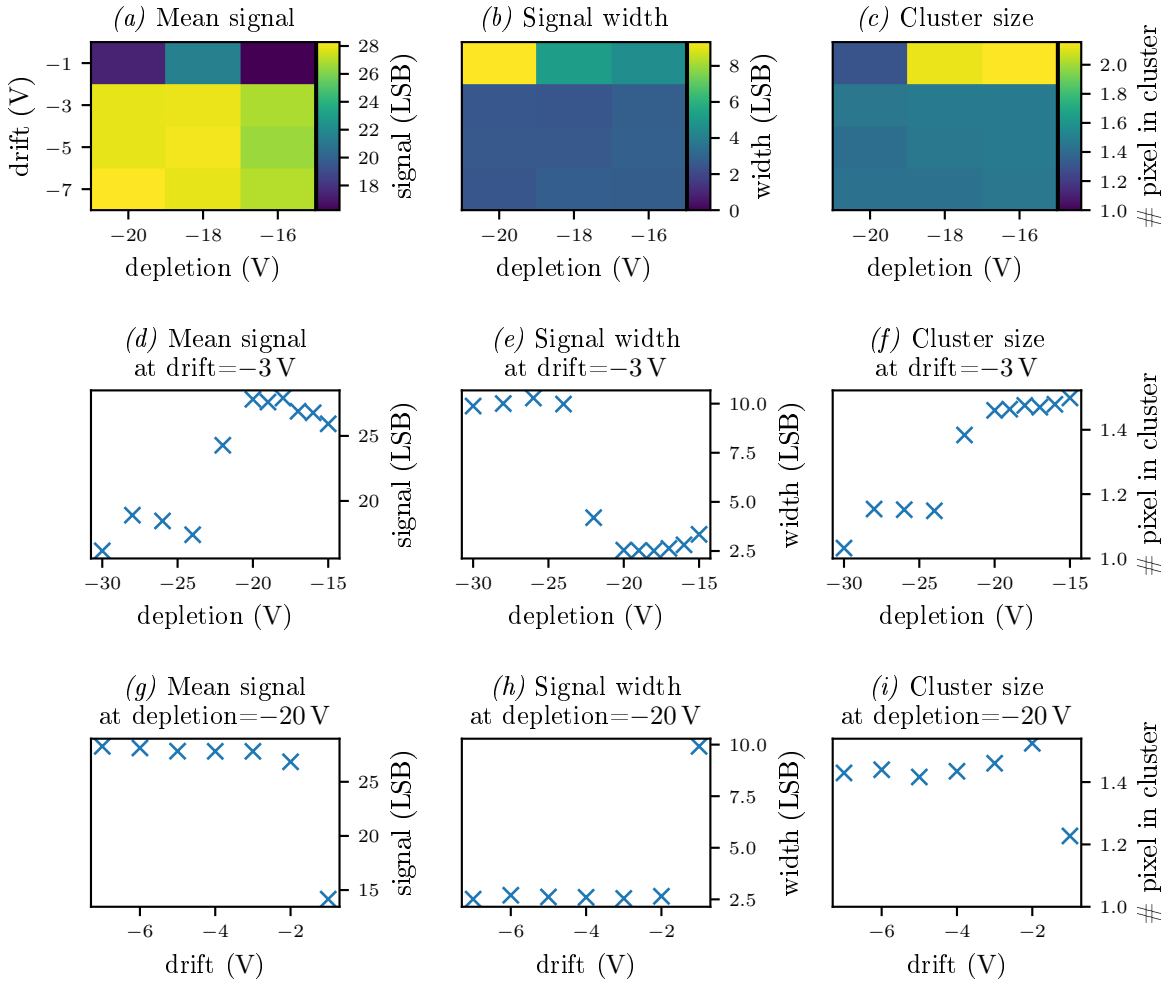


Figure 8.18: Summary of measurements for *drift* and *depletion* potentials. The first row shows results for the 2D scan varying both potentials. The second row shows the dependence on *depletion* at default *drift* potential; the last row shows the dependence on *drift* at default *depletion* potential.

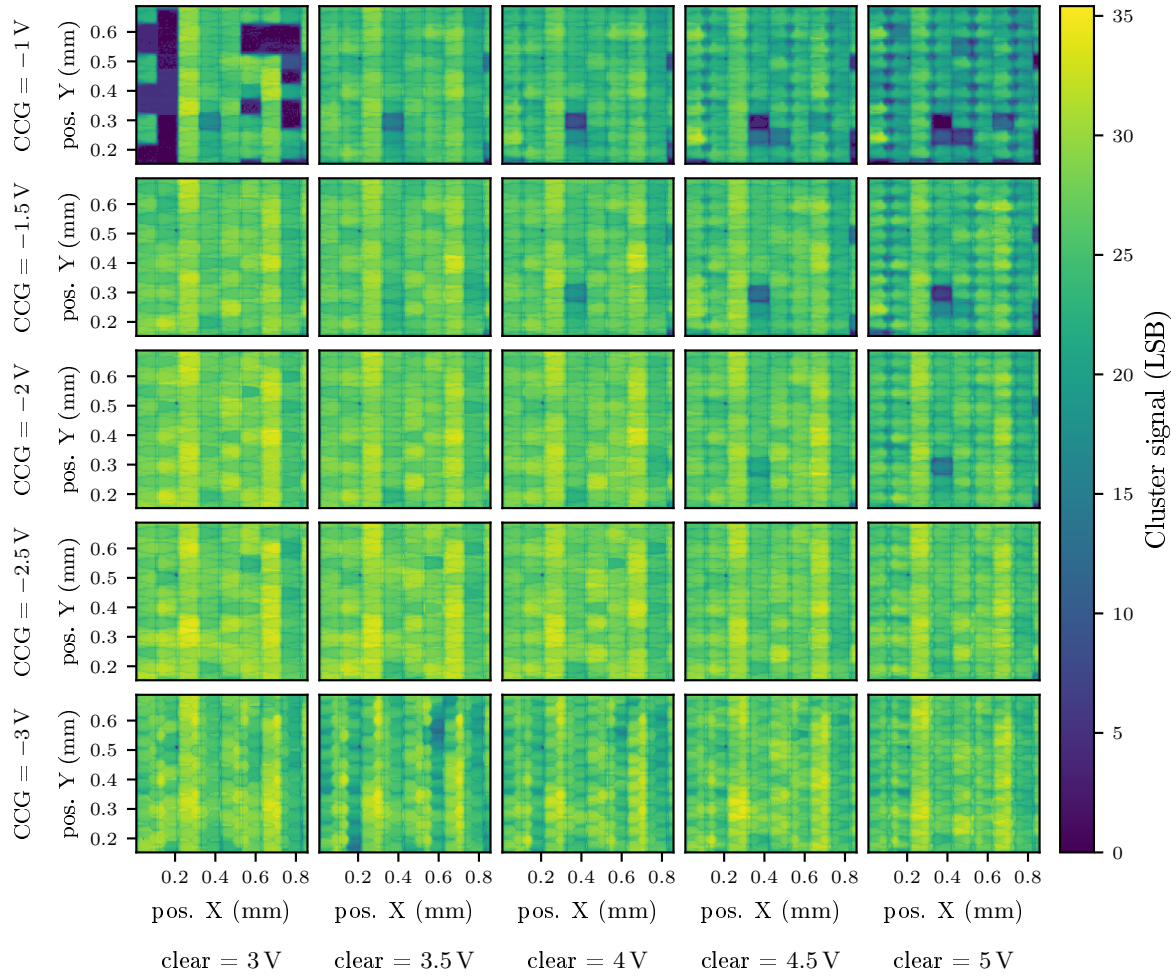


Figure 8.19: Cluster signal for different *capacitively coupled clear gate* and *clear low* potentials settings at default *drift* and *depletion* potentials.

can be seen:

- A too positive *clear low* potential will make the clear implant attractive for electrons, resulting in charge loss. This can be best seen at *clear low* = 5 V and *capacitively coupled clear gate* = −1 V. In this measurement, charge loss occurs near the pixel center where the clear implant is located.
- Measurements with a too positive *capacitively coupled clear gate* potential show less overall signal. This could be explained due to charge loss from the internal gate into the clear contact. A more positive *capacitively coupled clear gate* potential reduces the voltage barrier between internal gate and clear contact.
- Both effects above have a dependence on the respective other voltage.
- Measurements with a too negative *capacitively coupled clear gate* potential show a strange behavior in the drift region, where mostly multi-pixel cluster and less charge are detected. This is an effect of the surrounding clear gate layout used, as it does not change the charge collection near the DEPFET but charge injected in the the drift region.

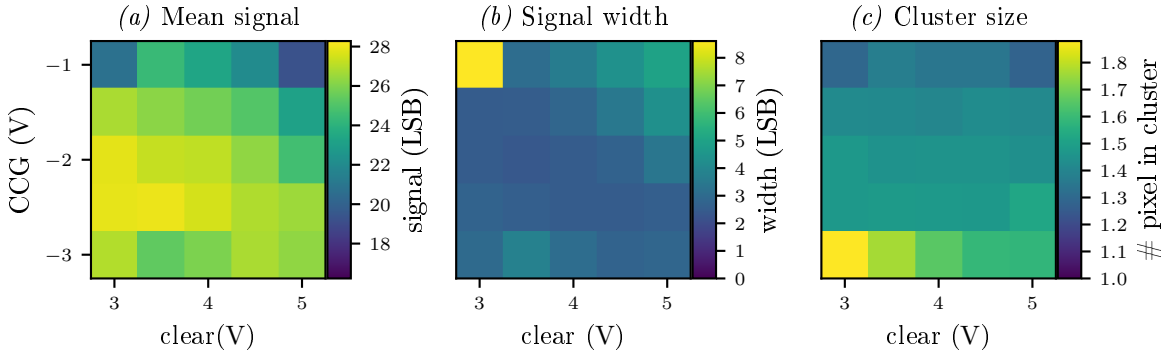


Figure 8.20: Summary of laser measurements for *capacitively coupled clear gate* and *clear low* potentials.

The optimal values used in further measurements are *capacitively coupled clear gate* $= -2\,\mathrm{V}$ and *clear low* $= 3\,\mathrm{V}$.

8.4.2 Large Area Measurement at Standard Voltages

As a final measurement with the laser, an exhaustive measurement over the working part of the matrix was performed. For this measurement, large steps of $11 \times 22\,\mu\mathrm{m}^2$ were used to speed up the measurement. One mayor issue for this measurement is the distance between matrix and microscope optic, which is not constant when moving the hybrid using the motor table. This has several reasons

- The thinned down sensor is bent due to gravity acting on the sensor and due to different thermal expansion coefficients between silicon and metallization, which both resulting in mechanical stress and a deformed sensor plane.
- The motor table is not perfectly parallel to the focus plane.
- The PCB is not mounted perfectly parallel in the mounting mechanic.
- The matrix is glued to the Hybrid PCB with a rather thick layer of silicon glue with low shear moment, to reduce additional mechanical stress on the module due to thermal expansion mismatch between silicon and the PCB material. This glue is applied by hand so it has no uniform thickness, resulting in an angle between PCB and the module.

Since the laser system is not automatically movable in this direction, the measurement was performed in several steps and on each step a manual focusing was performed. The focus was chosen so that the sensor surface was slightly out of focus at the beginning of each measurement step, then went in focus during the step and then went slightly out of focus again. In total, an area of $3.14 \times 19.8\,\mathrm{mm}^2$ was measured in a time of 129 hours[18], resulting in over a quarter million different measurement positions. Every 3 hours (5720 laser positions), new pedestals were taken. In this time the laser was positioned outside of the active area. The result of this is shown in figure 8.21.

Figure *(a)* shows the cluster signal. A gradient along the columns (X) is visible, similar to the uncorrected pedestal. Pixel at high x values show considerably less signal. Further, the signal in each gate has the same substructure which could be observed in the pedestals: Two rows have a medium signal, one row has a higher signal and one a lower. Most areas show a quite homogeneous in-pixel

[18] 129 hours of active measurement time. Including refocusing the measurement took 25 hours longer

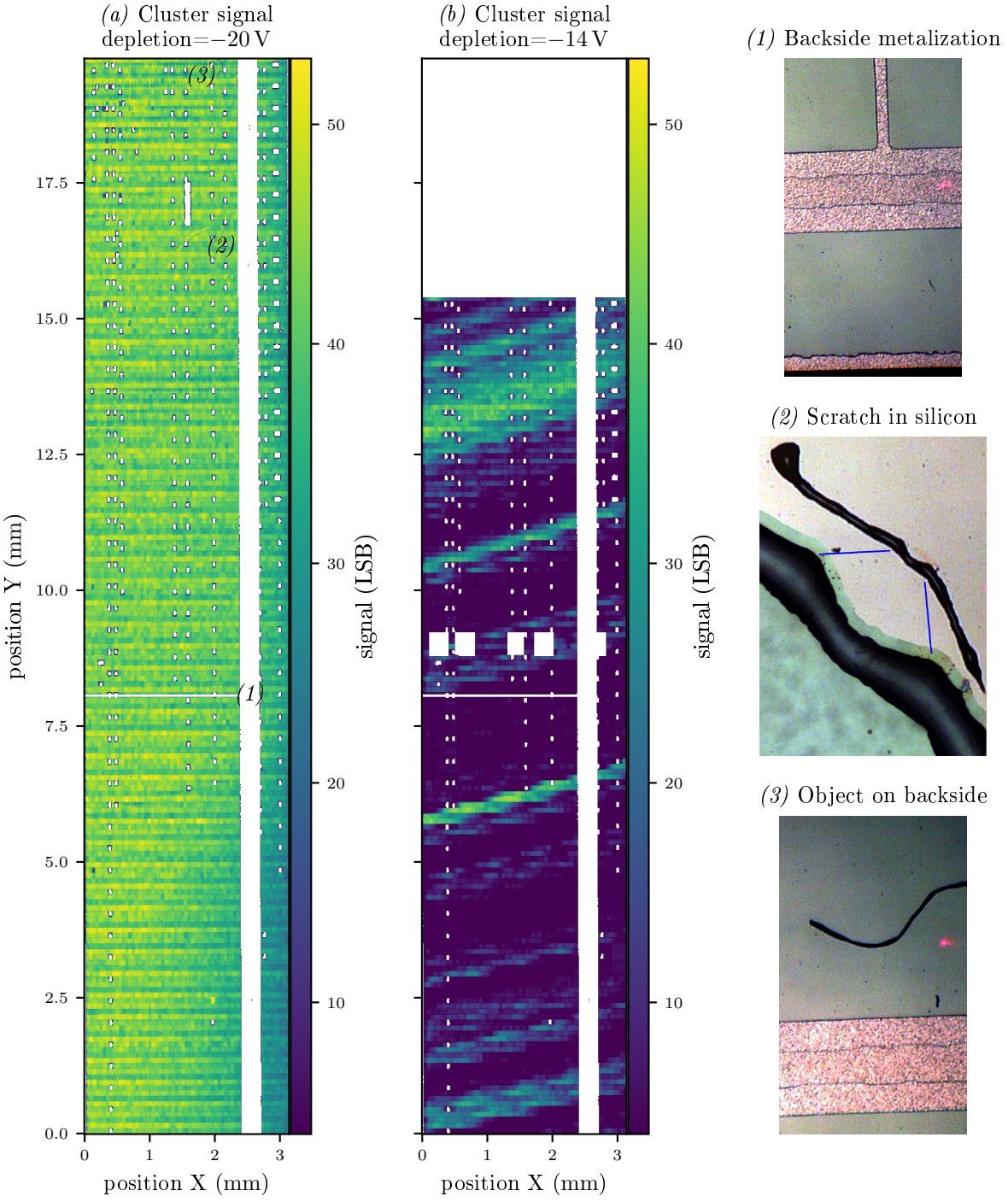


Figure 8.21: Large area laser measurement over 41 % of the area on Hybrid 6 using default potentials. Figure *(a)* shows the cluster signal for *depletion* =−20 V, *(b)* shows the cluster signal for *depletion* =−14 V which is too positive for most pixel. Here, no data was taken for Y>15.4 mm. *(1)* - *(3)* are pictures from the backside of the matrix at positions shown in *(a)*. Note that photos from the matrix are rotated 90° with respect to the data.

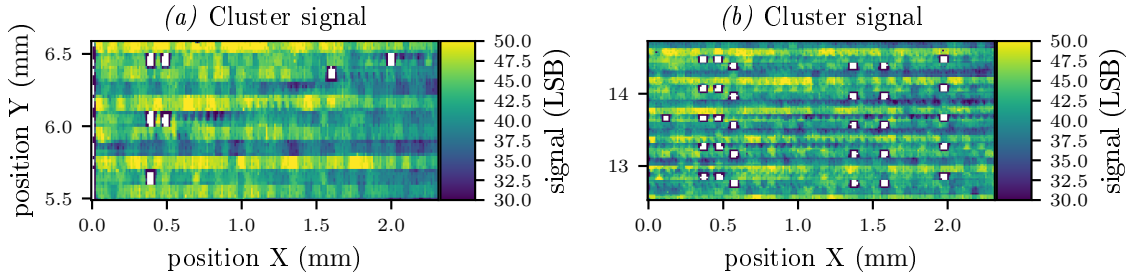


Figure 8.22: Zoom into large area laser scan at *depletion* =−20 V, showing less homogeneous stripes.

signal, but there are areas where the response is less homogeneous, for example (X=1, Y=6.25) or (Y=13 to Y=14) or Y=19.5. Two of those are enlarged in 8.22. These inhomogeneous regions do not follow gates or drains, but are lines over the sensor with an angle. This measurement was performed with a *depletion* potential of −20 V, close on the edge of the operation window. Some areas of the large matrix have a different operation window for the *depletion* potential and start to become inhomogeneous at this voltage. A further hint to this can be seen in 8.21 *(b)*, which shows the cluster response for was seen on a large area scan with very positive *depletion* voltage of −14 V, where again lines like this were visible. The inhomogeneities at −20 V coincide with the areas which show a good response already at −14 V. An effect like this, albeit more pronounced, was observed on large and small final Belle II DEPFET matrices (PXD9), which show ring segments on the sensor. These have different operation windows for the *depletion* potential.

On figure *(a)*, several understood artifacts can be seen:

- Figure 8.21 *(1)*: The large vertical line and the horizontal line are part of the backside metalization and block light.
- Figure 8.21 *(2)*: A scratch on the backside which shows a higher signal. The laser used has a wavelength of 680 nm resulting in an absorption length of ≈ 4.5 µm [80]. The scratch removed insensitive surface material, like the backside passivation, thus less light is lost at the surface area.
- Figure 8.21 *(3)*: Defects which show less signal are due to surface features or particles on the surface which block part of the lights

8.5 Beam Test Measurements

Laser measurements easily allow position resolved studies of the charge collection efficiency, but the final performance needs to be optimal for charged particles. Both create electron/hole pairs in the silicon bulk. The difference between both is, that a laser pulse with a wavelength of 680 nm, as used in the laser measurements, has an absorption depth of ≈ 4.5 µm producing electron/hole pairs only at the sensor surface. Charged particles produce electron/hole pairs along their path through the sensor material. Thus, results from both measurement types can differ. Effects which reduce charge collection from the backside of the sensor will be pronounced in laser measurements, since these effects influence all the charge created. Effects happening on the front side or in the silicon bulk may not be visible in laser measurements, since this charge can use different paths towards the internal gate and can encounter different charge loss mechanisms or be more susceptible to some charge loss mechanisms.

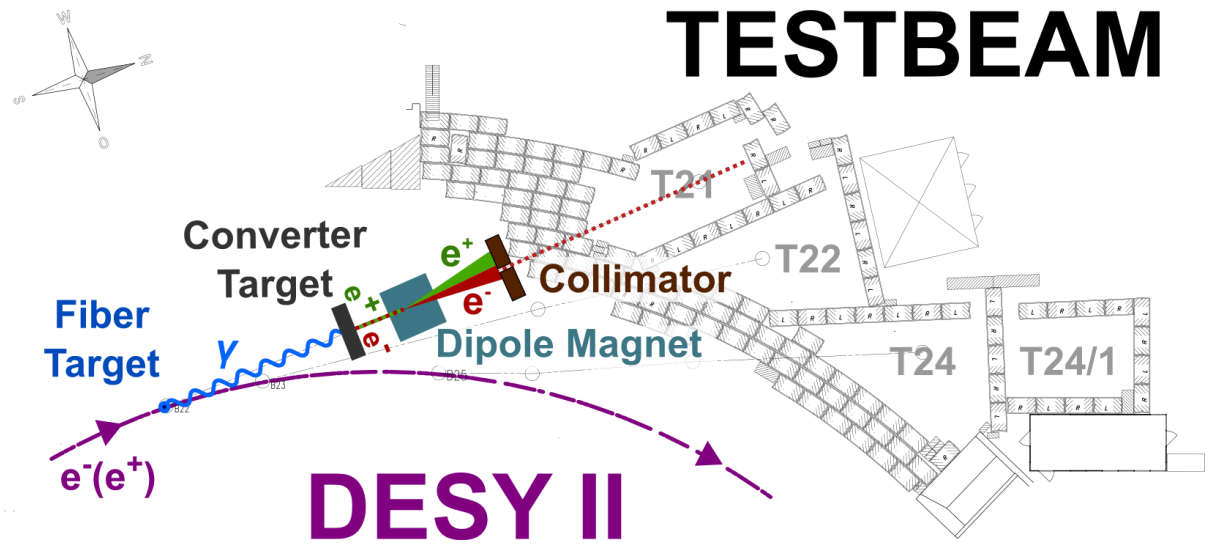


Figure 8.23: Schematic Layout of the beam test area at DESY. Primary electrons/positrons create Bremsstrahlung in a carbon fiber target. Resulting photons create electron positron pairs in a metal conversion target. Varying the field of the dipole magnet, the type and energy can be selected. Other particles are filtered by the collimator. From [81].

DEPFET Pixel detectors will be used for vertexing in Belle II. Vertexing performance depends on several factors, some of them were given in formula 3.1 for a two layer detector.

- Position resolution of the both sensors σ_1 and σ_1.
- The distance between sensor and interaction point. A first layer close to the interaction point is desirable for the lowest possible vertex resolution.
- The sensor thickness in units of radiation length. For low momentum particles, multiple scattering dominates the vertex resolution. Using the telescope setup at the beam test it could also be measured directly [82].
- Hit efficiency: If the sensor does not detect a particle, the extrapolation to the vertex suffers, since the sensor only contributes to the uncertainty due to multiple scattering.
- Number of broken pixels: Particles intersecting broken pixels might either be lost, reducing the hit efficiency or may be wrongly reconstructed, reducing the position resolution.

The hit efficiency and the position resolution can be measured in a beam test. Together with results from a voltage optimization, they will be discussed in this part. Beam tests can further be used to cross-check and validate simulations of charge collection in the DEPFET. This was performed in [83].

8.5.1 Measurement Setup

Beam test measurements were performed at the Beam test facility at DESY. Bremsstrahlung is created by Carbon fibers in the (up to) 7 GeV beam of the e^- synchrotron DESY II. The resulting photons are used to create e^+e^- pairs in a selectable metal conversion target. A magnetic field separates e^+ and e^- by charge and momentum, so that only particles of a certain charge and in a small momentum range can pass through the following collimator. Varying the magnetic field, users can select the particle

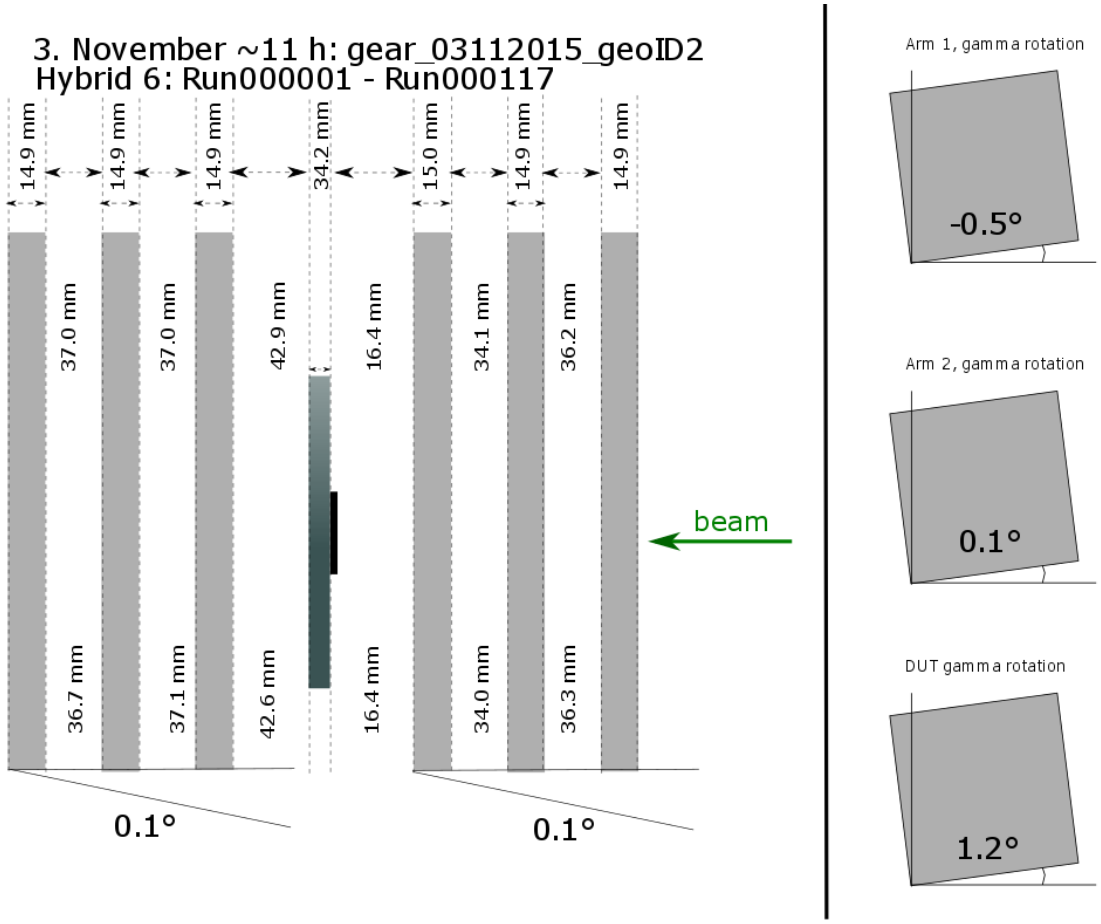


Figure 8.24: Sketch of the measurement setup geometry. The setup consists of two telescope arms with three planes each and the DEPFET sensor in the middle. The measured distances were used for most of the runs and result in a telescope pointing resolution of $(4.7 \pm 0.5)\,\mu\text{m}$ in u and v at the DUT plane.

type and the particle momentum between 1 to 6 GeV c^{-1} with a momentum resolution of 5 % [81]. A schematic of the beam area can be seen in figure 8.23 . The **D**evice **U**nder **T**est (DUT) is mounted on a motor stage which can adjust the position of the DUT in a plane perpendicular to the beam and rotate the DUT along one axis. The DUT is mounted so that columns are counting down and rows left to right (viewed from beam direction). Charged particles passing through the DUT are tracked using the EUDET telescope. The telescope consists of six layers of MIMOSA26 sensors, three before and after the DUT, with spacings given in 8.24. A MIMOSA26 sensor is a $1.06 \times 2.12\,\text{cm}^2$ binary readout CMOS pixel sensor featuring $576 \times 1\,152$ pixels with a size of $18.4 \times 18.4\,\mu\text{m}^2$, a thickness of 50 µm and an integration time of 115.2 µs per frame. Using hit information of the telescope, the expected hit position on the DUT can be interpolated to $(4.7 \pm 0.5)\,\mu\text{m}$ (see 8.5.5), using the geometry shown in figure 8.24, a DUT thickness of 50 µm silicon and a beam energy of 4 GeV.

Readout of all systems is triggered by a **T**rigger **L**ogic **U**nit (TLU)[19] which gets input signals of multiple channels, typically connected to scintillators. The setup used for these measurements used one large scintillator in front of the telescope and one **F**ront **E**nd (FE)-I4 trigger plane, a planar hybrid pixel sensor connected to an FE-I4 readout ASIC, which is mounted behind the telescope. The FE-I4

[19] A description can be found at `https://twiki.cern.ch/twiki/bin/view/MIMOSATelescope/TLU`

is the readout chip of the **I**nner **B**arrel **L**ayer (IBL) of the ATLAS experiment at CERN, featuring 336×80 pixels with $50 \times 250\,\mu m^2$ size. Each of its 26880 channels consists of a charge sensitive amplifier with constant current feedback and a comparator with tunable threshold. Charge injected in the amplifier changes the output voltage. If the output voltage is above threshold, the time above threshold is registered. Due to the constant current feedback, time above threshold is approximately linear to the injected charge [84]. Each channel can be connected to the "hit-or" line, which will signal if any of the selected pixels is high. This signal is routed off chip and can be used as input for the TLU. Thus the trigger plane can be used like a scintillator with configurable size so only particles passing through a region of interest trigger a readout of all detector planes [85].

Data is recorded using EUDAQ[20], in the scope of this thesis, the EUDAQ producer [86] needed to save DEPFET data was updated to support data from a DHE and the new DAQ.

With this setup, data were taken in November 2015. Over the course of 3.5 days, 23 different settings were measured, resulting in an data set of 164 GB, containing 180 million events, 200 million DUT hits and over 1 billion reconstructed tracks.

8.5.2 Track Reconstruction

For further analysis, tracks needed to be reconstructed and the most probable hit position on the DUT needs to be determined. This was done using the TBSW framework[21]. It is a software framework built on top of MARLIN[22], LCIO[23] and EUDAQ. MARLIN is used to split the reconstruction into several steps, LCIO is used for data persistency of reconstruction objects between steps and EUDAQ is used decode the input format. The TBSW framework covers all steps of the analysis from data preparation, clustering, track finding/fitting, sensor alignment and DUT analysis.

For analysis of sensor performance, a collection of events, consisting of a sensor signal and the corresponding estimated intersect location of the particle, is needed for each performed experiment. These were determined from measurements using TBSW.

This section contains a coarse description of tasks performed by the TBSW framework, a more detailed version can be found in [83].

Data unpacking The input data format needs to be unpacked and detector data needs to be converted into a common data format for all sensors. For the MIMOSA26 sensors, code from the EUDAQ framework is used. Unpacking of data recorded by a DHE and DHP was developed in the scope of this thesis. The unpacker in TBSW uses a slightly modified version of this code.

Data Preparation Some pixels on a sensor show signals when not being hit, creating noise hits. Pixels which show this too often (i.e. a fraction above 10^{-3} hits per frame) are called 'hot' pixels and are masked for further processing. The resulting data is clustered and the most probable hit position on the sensor plane is determined[24].

Coordinate System Each sensor is a planar layer with coordinate u along readout columns, v along readout rows and w along the sensor normal, so that (u, v, w) is a right handed coordinate system with the

[20] "a generic multi-platform data acquisition framework" `https://github.com/eudaq/eudaq`

[21] Created mainly by B. Schwenker, found on `https://bitbucket.org/BenjaminSchwenker/tbsw/`

[22] **M**odular **A**nalysis & **R**econstruction for the **LIN**ear collider `http://ilcsoft.desy.de/marlin`

[23] **L**inear & **C**ollider **I/O** `http://lcio.desy.de/`

[24] For a single pixel hit, the pixel center is used. Multi pixel hits with binary readout use center of gravity; non-binary readout pixels can improve the resolution using η-correction or similar techniques, like shown in [87]

origin in the center of the sensor (half width, half height, half depth of the sensor volume). Particle tracks are stored in telescope space (x, y, z) with z parallel to the beam and y pointing upwards. Rotations of each plane with respect to the telescope space are described as α counter clockwise around u, β counter clockwise around v,γ counter clockwise around w. Thus, hit positions on sensor plane k can be translated into the telescope space using six alignment parameters $(x_k, y_k, z_k, \alpha_k, \beta_k, \gamma_k)$. Sensors are numbered along the beam line, starting at k=0.

Track Reconstruction Track reconstruction estimates the trajectory of a particle from the hit position in the telescope space. This is achieved by translating sensor hit positions into telescope space, finding track candidates and then performing a track fit using a Kalman filter which models multiple scattering. The intersect of track and DUT can be translated back into sensor coordinates and results in an estimate of the intersect location. The uncertainty of the intersect is estimated by the square root of the diagonal elements of the covariance matrix given by the Kalman filter. It is called telescope resolution and depends on the sensor resolution of each plane, the multiple scattering of each plane (which is in turn dependent on particle energy and radiation length of the used sensor) and the geometry of the telescope. Two different geometries were used, shown in figure 8.24 and C.1. They result in resolutions of $(4.7 \pm 0.5)\,\mu\text{m}$ and $(3.9 \pm 0.4)\,\mu\text{m}$ at a particle energy of 4 GeV.

The distance between the cluster position measured by the sensor and the intersection point with the DUT determined by the track is called residual. The residual distribution depends on the DUT resolution, the telescope resolution and errors due to misalignment of the telescope. A well aligned setup has negligible alignment errors and since the DUT cluster is not used in tracking, errors on track intersect and DUT position are statistically independent. The width of the residual distribution σ_{res} is the folding of telescope pointing resolution (σ_{tel}) and DUT (σ_{DUT}) resolution:

$$\sigma_{res} = \sqrt{\sigma_{tel}^2 + \sigma_{DUT}^2}.$$

The beam at DESY is collimated with a small beam spot and tracks almost parallel to the beam. If the DUT is not tilted (i.e. its normal vector and the beam are parallel), correlations between u and v residuals are small and $\sigma_{DUT,u}$, $\sigma_{DUT,v}$ can be calculated independently from each other.

Alignment A correct alignment is needed for meaningful track residuals. Coarse initial alignment parameters can be determined from manual measurements with accuracies of 5 mm for x, y, z and 20 mrad for α, β, γ[25], but the alignment parameters need to be known with accuracies below 1 µm for Δx and Δy and below 10×10^{-4} rad for $\Delta\gamma$. The z parameter is less important if the beam divergence is small like at the DESY beam test facility, α and β are less important if they are smaller than 1°. Determining alignment parameters $(x_k, y_k, z_k, \alpha_k, \beta_k, \gamma_k)$ is done once per measurement. A measurement consists of multiple events (> 10000), each event has i_k hits on sensor k with position u_{i_k}, v_{i_k}, the w_i coordinate is 0 for all hits since a hit is assumed to happen at half depth of the sensor.

Using the collimated beam model, alignment parameters are determined using a three step process:

1. Using initial alignment parameters, x correlation histograms are produced for each pair k, l of sensors. Each event has i_k, i_j hits in sensors k, l. From each hit on plane k, a track is created which intersects plane k at the hit position and is parallel to the beam axis. The intersection coordinates of the track with the other sensor planes are used as expected hit positions. The $x_{(k,l)}$ correlation

[25] Errors are rather large since they consist of measurement errors of the casing position, different mounting position of the module PCB in the casing and different glued positions of the sensor on the module PCB

histogram gets filled with $\tilde{x}_{i_k} - x_{i_l}$ for all pairs i_k, i_j of hits in sensors k, l. Here, $\tilde{x}_{i_k}$ is the expected hit position on on sensor l, extrapolated from sensor k, and x_{i_l} is the measured hit position of the hit on sensor l. This is repeated for all events. The resulting histogram contains a small correlation region from hits belonging to the same track and a flat combinatorial background from hits belonging to different tracks. A truncated weighted average using only bins above $f *$ maximum of histogram typically with $f = 0.5$ results in a first estimate for $x_k - x_l$. Analog, $y_(k, l)$ correlation histograms are created and an $y_k - y_l$ estimate is calculated. For the first plane, absolute alignment parameters are set to $x_0 = 0\,\text{mm}$, $y_0 = 0\,\text{mm}$.
If all telescope planes are close together, the beam is collimated and only thin DUTs with low multiple scattering contribution are used, good correlations should be observable between the first plane and all other planes. This was the case during the DESY beam test. Hence, only correlation plots between the first plane and each following plane were needed for alignment.

2. Using alignment parameters from the previous step, track based alignment is performed using a Kalman filter with annealing [88]. No cut on the track quality is made, so the track sample can contain tracks with noise hits or wrongly paired hits. For this first pass of track based alignment, only x_k, y_k and γ_k are optimized, other parameters are fixed.

3. With updated alignment parameters, a second track based alignment step is performed. In this step, cuts on track quality are performed to get a track sample as clean as possible. Like in step two, a Kalman filter with annealing is used, this time for all parameters except for the z component of the first and last telescope layer[26]

Intersect Finding With final alignment parameters, a track finding and track fitting step is performed excluding clusters on the DUT. Using this data, the intersection of the reconstructed tracks with the DUT plane is calculated.

As a last step in TBSW, tracks and hits in each event are matched. A cluster and track are matched, if the distance between the reconstructed track intersect and the cluster are minimal and do not exceed the search radius of 0.5 mm. All clusters and tracks are saved together in a ROOT[27] file. This file is used for further analysis outside of TBSW.

8.5.3 In Pixel Measurements at Different Bias Voltages

The MIMOSA26 sensors in the EUDET Telescope have a resolution of 3.5 µm. Depending on geometry, beam energy and material of the DUT (including mechanics), the pointing resolution of the telescope can be between 3 µm and 5 µm, much smaller than the DUT pixel size. Thus, studies about charge collection and cluster size are possible with in-pixel resolution. This can be achieved by segmenting the area of a pixel into multiple bins.

The energy loss of a charged particle follows a Landau distribution, thus $O(100)$ particles are needed in each bin to determine mean signal height with a reasonable statistical uncertainty. With bins of $5 \times 5\,\mu\text{m}^2$, each pixel on the DEPFET matrix would be separated into 200 bins, which would need about 20000 tracks through each pixel to get a good accuracy. With particle rates achieved at DESY of about 1 to

[26] Stretching, a linear scaling of all z_k components, leaves residuals invariant but can be avoided if the total length of the telescope setup is fixed.

[27] ROOT Data Analysis Framework, `https://root.cern.ch/`

1.5 kHz, acquiring this amount of data is not possible within a reasonable time[28]. Higher statistic is achieved by mapping the whole sensor onto a so called "super pixel". A super pixel is an $m \times n$ pixel area, onto which all pixels are mapped. This is achieved by dividing the sensor into $m \times n$ pixel chunks. Each track passing a chunk at position u_c, v_c relative to the origin of the chunk is handled as a track passing the super pixel at coordinate u_c, v_c . This requires a translational symmetry of the pixel matrix which is given for the sensor mounted on Hybrid 6. The PXD6 sensor used on Hybrid 6 is shown in figure 8.25. It features pixels which are organized in a 2×2 quad-pixel layout, so pixels in even and odd rows have a row wise mirrored geometry and pixel with even and odd column have a column mirrored geometry. Gate and clear line are shared by a gate, thus quad pixel layouts in row 1 and row 2 have a different (almost row wise mirrored) metalization compared to quad pixel layouts in row 3 and row 4 in the gate. As a result the minimum size of the super pixel should be 4 rows and two columns. Smaller super pixels are possible when mirroring data from even/odd rows and columns but could not capture layout induced differences in the pixel response.

Figure 8.26 shows a sample measurement: Each plot shows the bins of the 4×4 super pixel. Figure 8.26 *(a)* shows the seed signal received with respect to the hit position of the track. At pixel borders the seed signal is lower due to charge sharing. Figure 8.26 *(b)* shows the cluster signal which in an ideal sensor would be constant over the whole sensor. Here pixels in a row show very similar performance but the signal varies between rows. The pixel centers show a high signal, in the center of the charge sharing region the signal has a similar signal. Between these is a small border with lower signal, similar to effects seen in the laser scans in figure 8.16 *(a)*: Some particles deposit charge in the second pixel which is too small to be detected and thus the reconstructed mean charge is lower. Charge is only lost, if it is smaller than the threshold. The shared charge q_{sh} is $q_{sh} = q_t * f(u, v)$, with the total charge q_t and a position dependent sharing ratio $f(u, v)$. During the laser scan, both position and injected charge were constant. In the beam test, the total charge is drawn from a landau distribution and the position is variable and only known with an error. Thus the effect is smeared out and less visible compared to the laser. The mean received charge drops significantly for areas where 3 or 4 pixel clusters are expected. The MPV

[28] An area of around 64×150 pixels was investigated. For this area, about 200 Million DUT hits would be needed. This is the amount which was taken during the whole time available at DESY for all settings (assuming, none of the DUT hits were due to noise and all hits had a track). With an estimated event rate of 1000 good hits per second, a measurement like this would take about 50 hours.

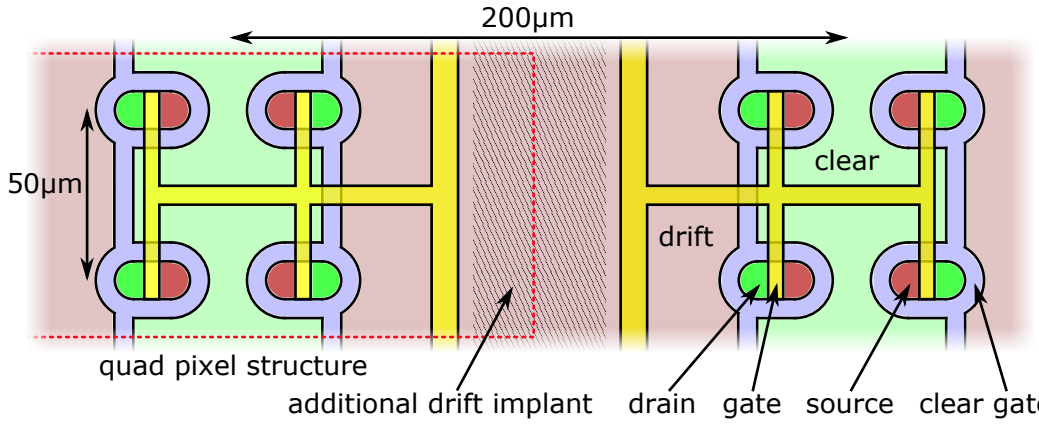


Figure 8.25: Simplified layout of the DEPFET sensor used on Hybrid 6 (not to scale). Two columns and one gate with four rows are shown. Drain lines, source lines, clear lines and structures for capacitive coupling of *cleargate* to the *clear* potential are not shown for in this layout for clarity.

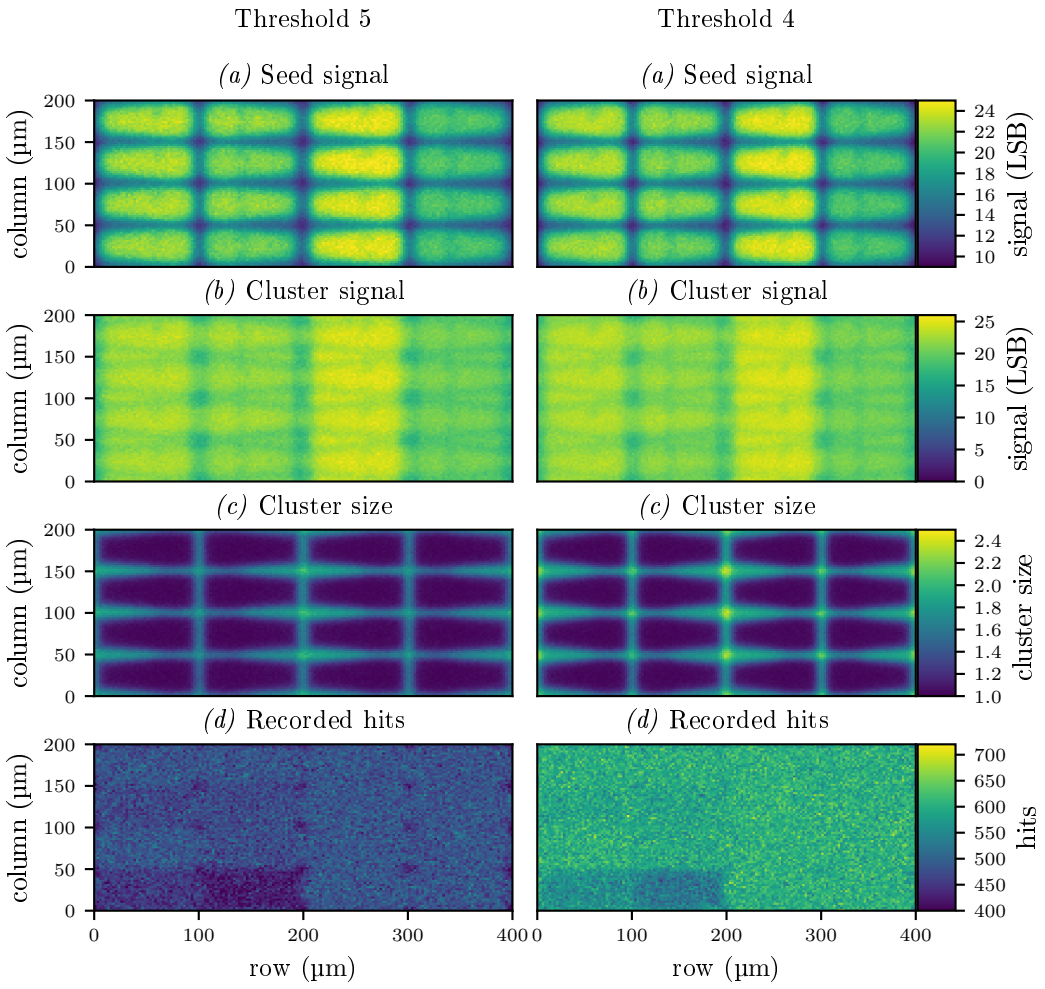


Figure 8.26: Example of beam test results taken at *capacitively coupled clear gate* = −2 V, *clear low* = 3 V, *drift* = −3 V,*depletion* = −20 V. The *left* plots show result for measurements with threshold of 5 LSB, the right plots a measurement with threshold 4 LSB.

of the signal is at about 17 LSB. When sharing this signal between 3 or 4 pixels, some charge can be below threshold of 3–5, thus the charge is lost. This can even lead to inefficiency when no pixel is above threshold. A hint towards the efficiency can be seen in figure 8.26 *(d)*, where the number of recorded hits with tracks is shown with respect to the reconstructed track position. In the pixel edges, less hits are registered when using threshold 5.

The sensor has 26 broken drain lines, which can be seen from the repeating pixels with low pedestals in 8.13 *(c)*. Ten of these are already present in the measured pixel area, which spans from row 50 to row 200. Thus, some of the pixels in the super pixel show less recorded hits[29]. In addition on the edge of 4 pixels less hits were recorded, due to the threshold of 5 LSB during this measurement. A measurement at the same voltages with 4 LSB does not show this effect. A more close analysis of the sensor efficiency at optimal voltage is performed in the next chapter. Figure 8.26 *(c)* show the mean cluster size, where

[29] As stated previously, only row 1 and row 2 in the gate show broken drain lines. In addition, the probability of drain lines to be broken is different for even and odd columns, with 23 to 3 broken drain lines each. This is probably due to small differences in the layout of the drain lines.

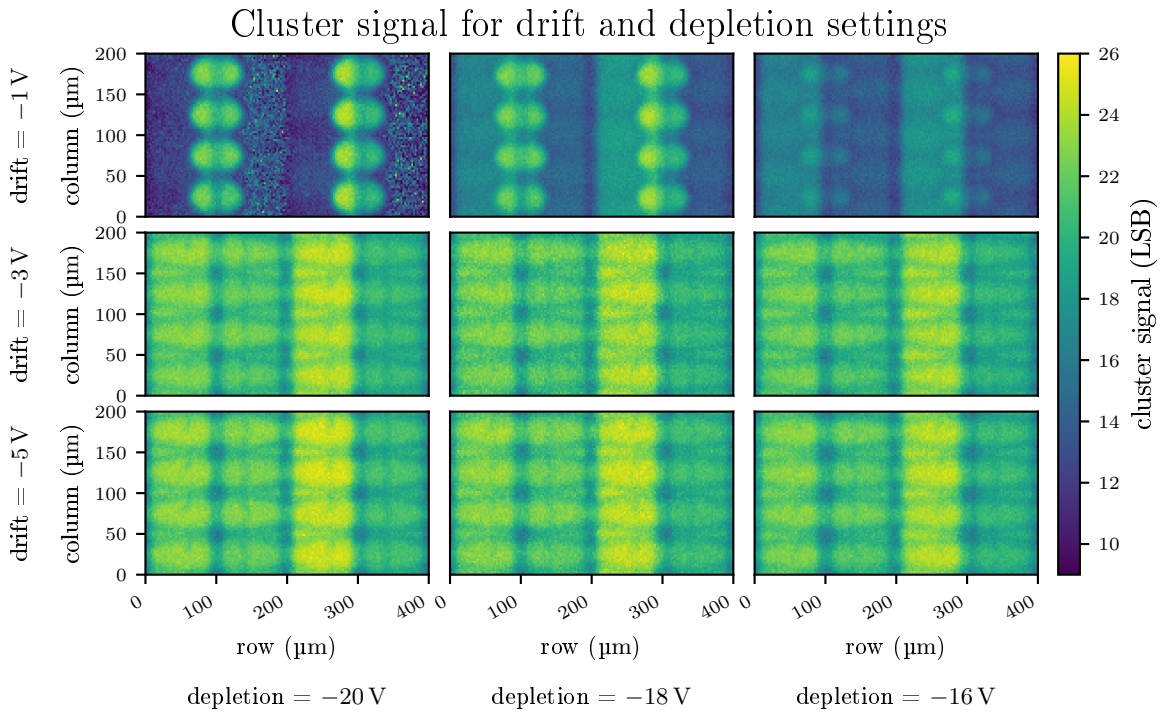


Figure 8.27: Cluster signal taken at different bias voltages for *drift* and *depletion*, with *capacitively coupled clear gate* = −2 V and *clear low* = 3 V. The setting *drift* = −1 V and *depletion* = −20 V has large inefficient areas between 130 to 200 µm and 330 to 400 µm in row direction. They result in a very low statistics and the observable strong fluctuations of the reconstructed signal. Seed signal, cluster size and recorded statistic can be found in C.3, C.4 and C.5

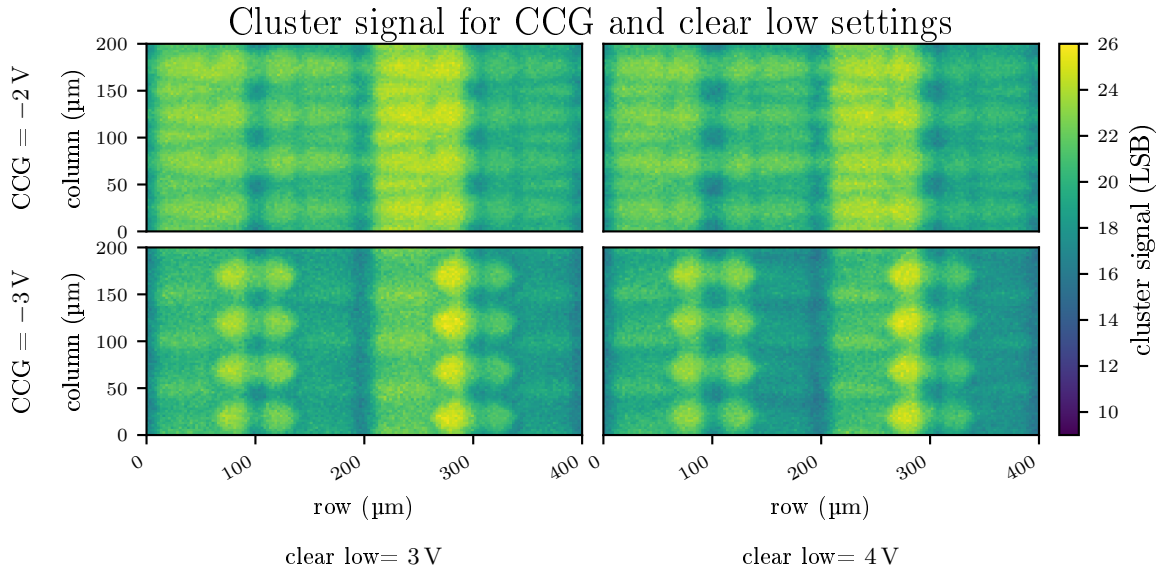


Figure 8.28: Cluster signal taken at different bias voltages for *capacitively coupled clear gate* and *clear low*, with *drift* = −3 V and *depletion* = −20 V. Seed signal, cluster size and recorded statistic can be found in C.6, C.7 and C.8

charge sharing regions can be identified.

Drift and Depletion The above described measurement was performed for several bias voltages. Figure 8.27 shows the result for *drift* and *depletion* at nominal voltages for *capacitively coupled clear gate* and *clear low*. A *drift* voltage of −1 V can be excluded: Charge collection works in the inner region, but charge from the drift region is lost (especially for *depletion* =−20 V, where every other row is almost blind) and a bad charge separation, resulting in large cluster sizes. The other settings look quite comparable, with slightly higher signal for both more negative *drift* and *depletion* potentials. Due to the threshold of 5 LSB, some charge is lost in the pixel corner. This effect is reduced in other measurements, which use lower thresholds. Some charge loss is visible in the pixel at row 70 µm, 130 µm, 270 µm and 330 µm. This happens at the clear gate which separates the clear and drift region of the DEPFET. This effect is more pronounced for more negative *depletion* potential. The observed effect is smaller than the charge loss due to the readout threshold, making all clear voltages Thus, a wide parameter space for both voltages is available.

Common Clear Gate and Clear Low Due to time limitations, only 4 points could be taken for *capacitively coupled clear gate* and *clear low*. Since some parts of the matrix are not responsive for *capacitively coupled clear gate* = −1 V, this setting was dropped. The recommended *clear low* voltage is 3 V, so the setting for *clear low* = 5 V was dropped. With default voltages for *drift* and *depletion*, beam test measurements were taken. During these measurements, the system was run with a threshold of 4 LSB. The results are shown in 8.28. The optimal point is *capacitively coupled clear gate* = −2 V and *clear low* = 3 V, it yields both the highest an most homogeneous signal. Higher *clear low* values are possible and yield comparable results, a more negative *capacitively coupled clear gate* potential worsens the result. Charge injected in the drift region does not directly drift into the internal gate due to the wrong potential under the clear gate, which acts as a separator between the drift region and the pixel center. Drifting first between two pixel centers, most charge can still reach the internal gate but takes longer to do so. Thus, the cluster size in the drift region is larger. Charge arriving in the drift region at column positions between two pixel centers (e.g. at position Row=50 µm, Column=50 µm) is less influenced by this effect.

Only one good value for *capacitively coupled clear gate* is found. The *capacitively coupled clear gate* potential is expected to be one of the potentials changing most with irradiation [63], thus a larger operation window would be beneficial. This was improved in the next matrix generation by changing the clear deep-p implantation process from a mask to a self aligning process at the clear gate to clear border. This results in lower adjustment tolerances and better defined barriers at the clear gate. [36]

8.5.4 Comparison between Laser Measurements and Beam Test Measurements

The sensor was characterized both using data from a beam test and a laser setup. While both measurement methods are very different, they show very similar results in terms of in-pixel response. For a detailed comparison a measurement at optimal voltages is shown in figure 8.29 with seed signal, cluster signal and cluster size for both methods side by side. One obvious difference is that the beam test measurement has less pronounced variations compared to the laser measurement. This can best be seen in the cluster size and is in part due to the limited telescope resolution of ≈ 4 µm. Tracks with the same reconstructed in-pixel position can originate from tracks with different real hit positions, thus smearing out some features. The laser system has a spot size of a similar size, but always hits the same area. Another reason for the smeared out differences is the signal distribution. The laser injects a very similar charge in each frame, while the charge created by a ionizing particle follows a Landau distribution. When charge

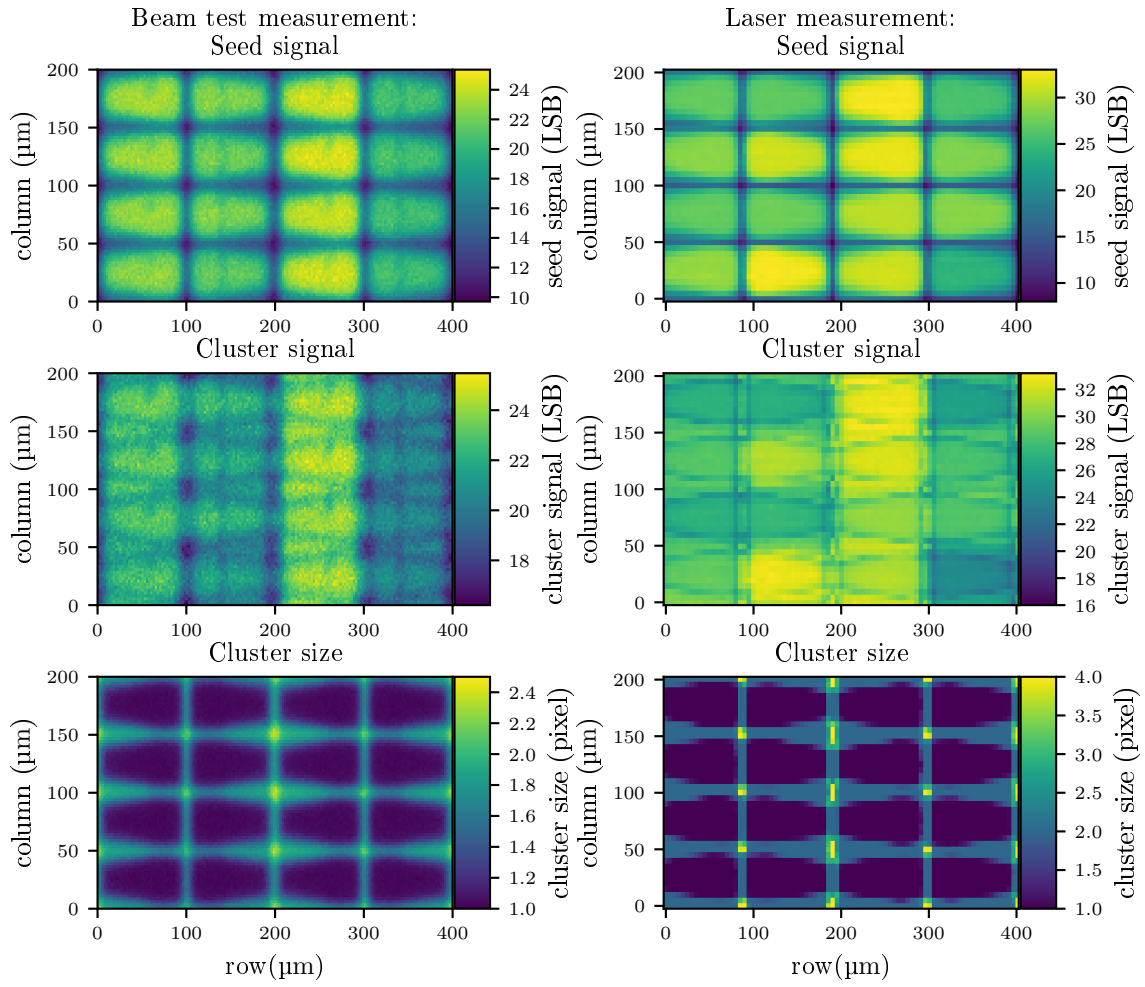


Figure 8.29: Comparison of laser and beam test data at standard voltages (*clear low* =3 V, *capacitively coupled clear gate* =−2 V, *drift* =−3 V, *depletion* =−20 V). *Left:* In-pixel results from beam test. The seed signal, cluster signal and cluster shape are shown. *Right:* In-pixel results from laser data.

sharing occurs near a pixel border, some charge can be lost if the fraction of shared charge creates a signal below the readout threshold. This is more unlikely to happen for large initial charges than for small charges. Thus the cluster size distribution is different for different injected charges with larger charges showing more charge sharing. The resulting cluster size distribution for beam test data is a mix of those distributions. For laser data, the injected charge varies only minimal between injections, strongly reducing smearing due to this effect.

The measurement results show many similar features:

- The seed signal distribution is asymmetric for each pixel and mirrored for pixel neighboring rows. Each pixel consists of a pixel center featuring the DEPFET and a drift region. Pixel from even and odd rows are mirrored, so that both DEPFETs are close together and two pixels share a single drift region. In the drift region charge sharing between columns is more pronounced.

- Both measurements show the charge sharing pattern in column direction. This can be seen in the cluster signal. Between two pixels is an area where charge is completely reconstructed. Those

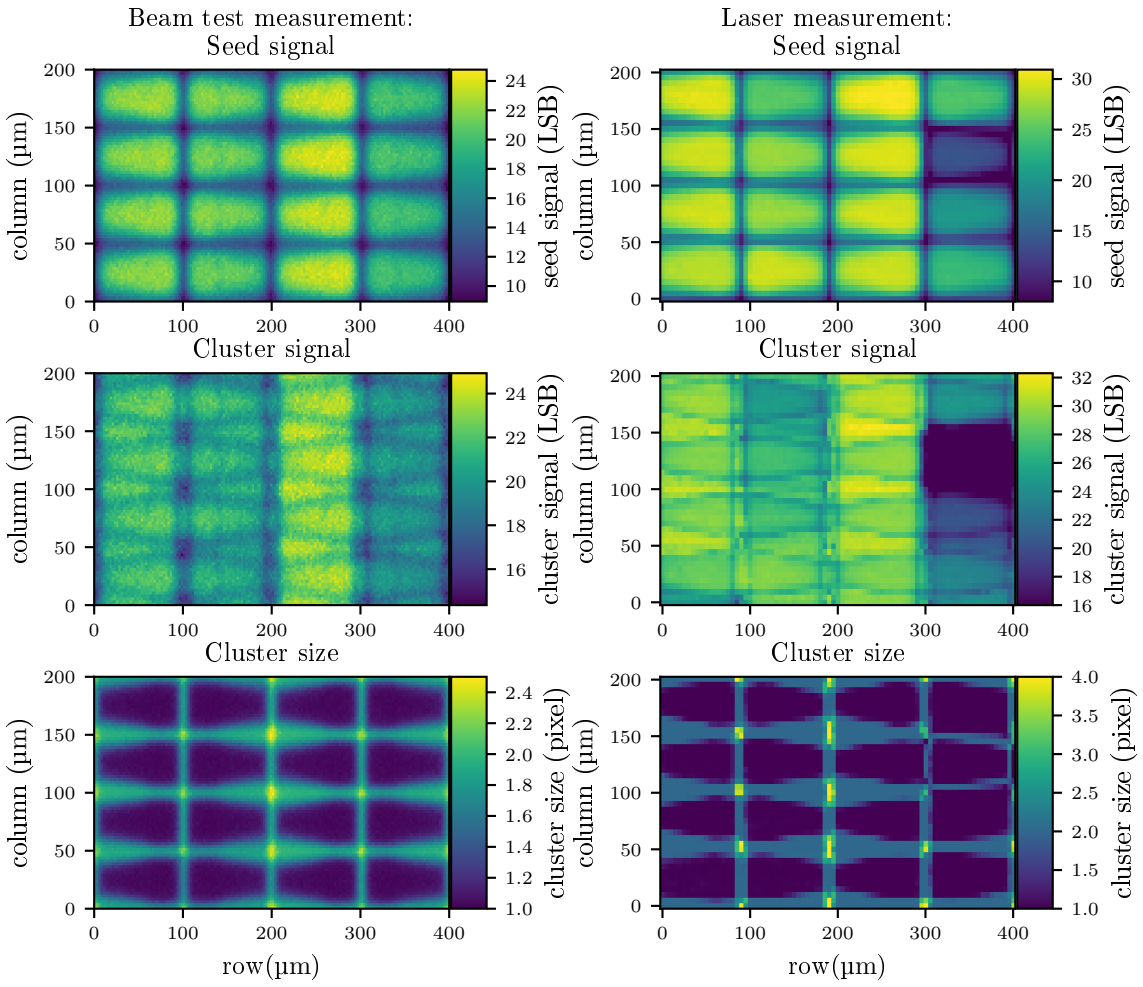


Figure 8.30: Comparison of laser and beam test data at *clear low* =3 V, *capacitively coupled clear gate* =−2 V, *drift* =−3 V, *depletion* =−16 V. At these potentials the sensor has a larger fraction of multi-pixel clusters. *Left:* In-pixel results from beam test. The seed signal, cluster signal and cluster shape are shown. *Right:* In-pixel results from laser data.

areas are separated by 'trenches' of reduced signal, where charge sharing occurs but the fraction of shared charge is below the threshold and thus lost.

- The laser plot shows the signal from two gates, the beam data shows a super pixel which is one gate wide. Both measurements show a row pattern (from left to right): two rows with a 'normal' signal, then one row with a higher signal and one row with a lower signal. Due to pixel to pixel variation this effect is less pronounced in the laser measurement.
- The cluster size distribution of both measurements is very similar.

Some differences can be observed between both measurements

- The laser measurement shows pixel to pixel variations which are averaged out in the super pixel.
- At pixel edges, the laser measurement shows trenches which separate an area where 4 pixel cluster

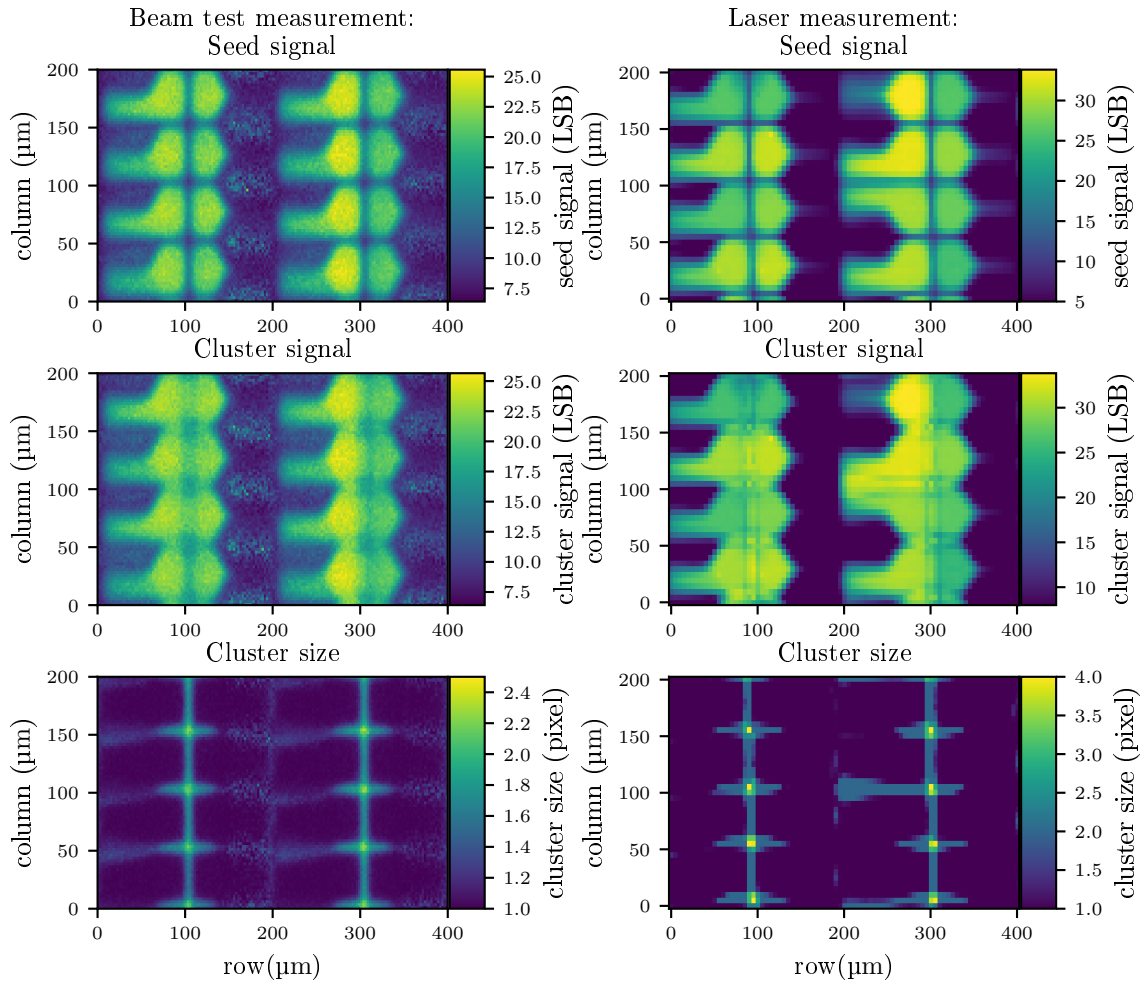


Figure 8.31: Comparison of laser and beam test data at *clear low* =3 V, *capacitively coupled clear gate* =−2 V, *drift* =−3 V, *depletion* =−24 V. The sensor is over depleted and looses charge in the drift region. *Left:* In-pixel results from beam test. The seed signal, cluster signal and cluster shape are shown. *Right:* In-pixel results from laser data.

are received and the reconstructed signal is comparable to the expected cluster signal. In the super pixel, pixel edges show a reduced signal due to charge loss.

- The super pixel shows areas in the pixel center where the charge is lower than anticipated, visible in both seed and cluster signal around ≈ 70 µm, 130 µm, 270 µm and 330 µm in row direction. The reduced signal occurs in the pixel center where only single pixel cluster are expected. It is not visible in the laser measurement. The position of this effect is roughly at the interface between clear gate and the drift area.

Figure 8.30 and 8.31 show comparisons for further measurement settings: Figure 8.30 shows the response at *depletion* =−16 V, figure 8.31 shows the response at *depletion* =−24 V. At *depletion* =−16 V the sensor shows larger charge sharing regions resulting on more multi-pixel cluster, which can be seen in both in laser and super pixel data. In the cluster signal two trenches can be observed between neighboring rows which separate the charge sharing region. This is best visible at 100 µm in row direction.

In the laser measurement, two pixel with a significantly reduced signal are observed. These pixels are an exception - as can be seen in figure 8.17, where larger areas of the laser measurements are shown. Single pixel effects are not visible in the super pixel but are visible in other beam test control plots like per pixel gain or efficiency measurement (chapter 8.5.8 and 8.5.6).

At *depletion* =−24 V, some areas of the sensor are very inefficient, which can be seen directly in the laser data, where no signal is received. This can be seen between 130 to 200 µm and 330 to 400 µm in seed and cluster . The super pixel still shows signal in this area but with much lower statistics. For this, three reasons could be found:

- Some particles deposit a large charge which still can be detected.
- In rare cases, tracks can have a large reconstruction error, so that they are reconstructed in the inefficient region while the particle hit a efficient region[30].
- Primary particles can create δ-electrons which can traverse the sensor. If a δ-electron traverse an efficient region, the charge it deposits can lead to detection.

In this picture even and odd rows react very different. By counting from left to right, odd rows are more efficient than even rows. The charge reconstruction pattern on even rows is very similar for all pixel and thus similar between the super pixel and the laser measurement. For pixel in odd rows is very different between pixels, some are mirror images of their neighbors, some show the same pattern.

Charge injected close to the DEPFET always reaches the internal gate. Charge outside of the surrounding clear gate sometimes is lost. Due to the way the sensors were produced, differences between even and odd are expected: Implantations are created by shooting ions into the silicon bulk under a small angle with respect to the sensor normal. This results in an effect called 'shadowing' where depending on the geometry of the sensor the implantation strength and position can slightly vary. The DEPFET generation used for the Belle II experiment will be produced using quad implantations, a technique using four implantation steps where in-between the waver is rotated by 90° to reduce shadowing [36].

8.5.5 Resolution

The sensor resolution of the DEPFET sensor in u can be determined using the residual between the hit position measured by the sensor u_{hit} and the reconstructed track intersection with the sensor plane u_{tel}. The residual track distribution $u_{res} = u_{hit} - u_{tel}$ is mainly governed by the convolution of two error sources; the sensor resolution $\sigma_{u\,hit}$ and the telescope pointing resolution $\sigma_{u\,tel}$. It can be increased by suboptimal alignment constants and problems with the Kalman filter when wrong particle momenta and multiple scattering contributions for the sensor planes were used. The telescope pointing resolution can be estimated by the uncertainty of the Kalman filter at the track intersect with the DUT plane. Most measurements were performed with the geometry shown in 8.24, which results in a telescope pointing resolution of (4.72 ± 0.50) µm in u and v. Since the telescope pointing error and the sensor reconstruction error are independent, the residual is a convolution of both so that $\sigma^2_{u\,res} = \sigma^2_{u\,hit} + \sigma^2_{u\,tel}$. This holds true for v as well, so $\sigma^2_{v\,res} = \sigma^2_{v\,hit} + \sigma^2_{v\,tel}$. By measuring the residual distribution in u and v, the sensor resolution can be calculated as $\sigma_{u\,hit} = \sqrt{\sigma^2_{u\,res} - \sigma^2_{u\,tel}}$ and $\sigma_{v\,hit} = \sqrt{\sigma^2_{v\,res} - \sigma^2_{v\,tel}}$. The residuals of

[30] This can be deduced from figure 8.34 *(b)*, where the probability to find a hit is shown against the search distance around the track. The steep increase part below 50 µm is due to the DUT resolution. The probability further increases for larger search distances, even above distances larger than a pixel, which can only be explained by some tracks being reconstructed in a certain pixel while the particle hit one of its neighbors. If this can happen. This effect can not be due to mismatching with noise hits since the increase stops at a search distance of ≈ 250 µm. For mismatching with noise hits, the effect would be expected to further increase with larger search distances.

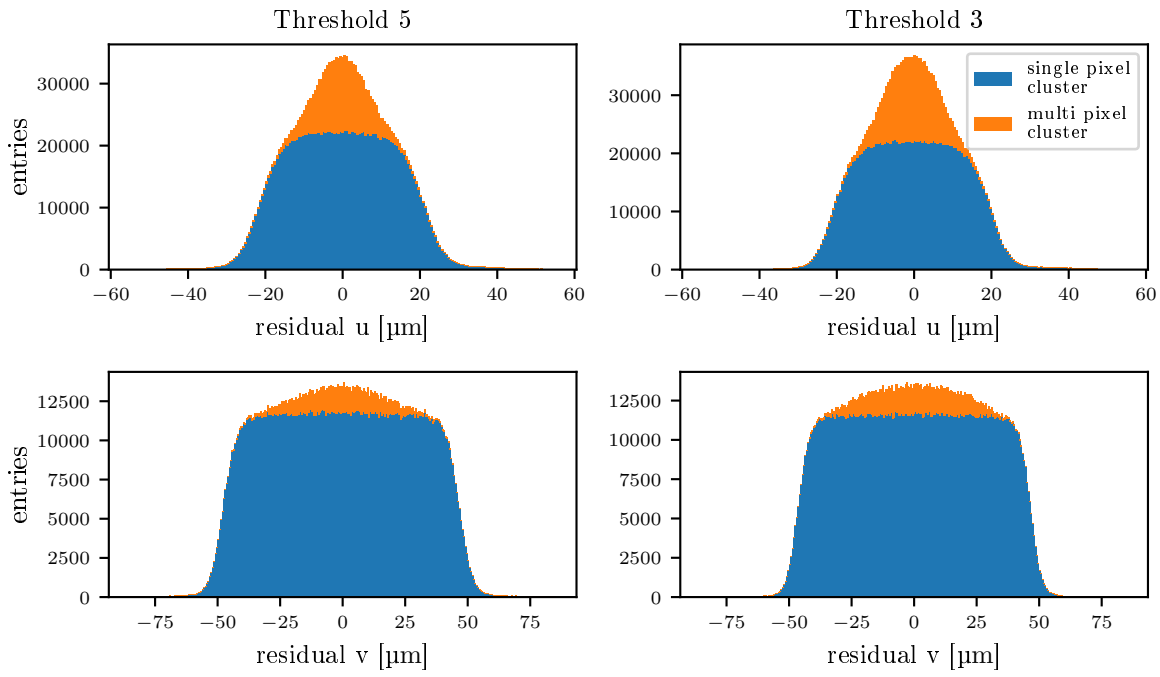


Figure 8.32: Residual distributions at different thresholds in both u and v. The right distributions are taken using lower threshold, resulting in more two pixel cluster and a lower residual width. The higher number of two pixel cluster is more prevalent in u direction as the pixels are larger in v with a smaller fraction of the pixel area sharing charge with their neighbors. Measurements were taken at default voltages.

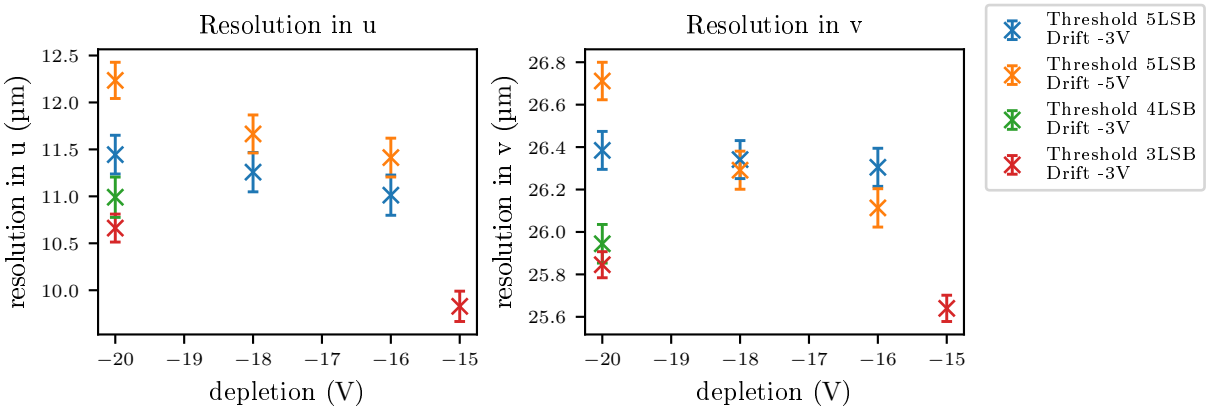


Figure 8.33: DEPFET resolution for different *depletion* and threshold settings.

two distributions are shown in figure 8.32 in u and v for two different thresholds. In these plots the clusters are separated by the cluster size in the respective direction. Single pixel clusters have a box-shaped distribution, especially in v where the DEPFET has a pixel pitch of 100 µm. A single pixel cluster is created when a particle passes in the pixel center. Particles passing close to the pixel border will create two pixel clusters due to charge sharing. This allows to determine their position more exactly. For this analysis, the position of a two pixel cluster was calculated using the center of gravity; a weighted average of the pixel position with weights according to the signal each individual pixel received. The center of

gravity method is not optimal, as it assumes charge sharing to be linear to the position between pixels, which is not the case. Better hit position estimations are explained and investigated in [87], albeit for thick DEPFET sensors with a different readout. As a result of this, resolutions determined in this thesis are only upper limits; using more complex algorithms, the residual width can be decreased resulting in a better resolution.

The left and right part of figure 8.32 show the residuals at the same voltages for different thresholds. Hits close to the pixel border share charge between two pixels. If the charge in one pixel creates a signal below the threshold, this information will be lost and the pixel will be seen as a single pixel, resulting in a larger residual. Thus, a lower threshold will create a higher number of two pixel clusters which will decrease the residual distribution[31].

The sensor resolution was determine by subtracting the telescope resolution from the residual distribution width. This was performed for several different settings and is shown in 8.33 for both u and v against the *depletion* potential. Charge sharing happens by diffusion of the charge cloud created by the ionizing particles.

A more negative *depletion* potential decreases the drift time into the potential minimum below the sensor surface, thus reducing charge sharing. This can be seen in both u and v for *drift* potentials of 3 V and 5 V. The more negative *drift* potential increases resolution in u. This can be explained by faster collection: A more negative drift field creates a higher gradient towards the internal gate, limiting the charge sharing between columns. For v, a more negative *drift* potential increases the dependence of the resolution on the *depletion* potential. The interplay between the *drift* and *depletion* potential and the drift implantation makes the drift path of the charge complicated, further simulations of the charge sharing process are needed to explain the results. An obvious decrease in resolution comes from lowering the detection threshold from 5 LSB to 3 LSB. This is especially useful when using more positive *depletion* potentials which yield a larger charge sharing region. Changing the standard setting of *depletion* $=-20$ V with threshold 5 LSB to *depletion* $=-15$ V with threshold 3 LSB decreases the resolution from $\sigma_{u\ hit} = (11.4 \pm 0.2)\,\mu\text{m}$ to $\sigma_{u\ hit} = (9.80 \pm 0.15)\,\mu\text{m}$ and $\sigma_{v\ hit} = (26.38 \pm 0.08)\,\mu\text{m}$ to $\sigma_{v\ hit} = (25.63 \pm 0.06)\,\mu\text{m}$. As comparison: The theoretical resolution of a single pixel binary detector which is perfectly efficient and only shows single pixel hits is $\frac{\text{pixel pitch}}{\sqrt{12}}$, which for the pixel size of the used DEPFET would be $\sigma_{u\ hit\ theoretical} = 14.43\,\mu\text{m}$ and $\sigma_{v\ hit\ theoretical} = 28.86\,\mu\text{m}$. Simulations in [89] show a significant performance increase for Belle II even with resolutions of only 15 µm. Using better reconstruction algorithms and DEPFETs with a larger g_q, resolutions below $\sigma_{u\ hit} = 10\,\mu\text{m}$ should be feasible.

8.5.6 Efficiency

For particle physics, the detection efficiency of the sensor is one of the most crucial performance numbers. It is defined as

$$\epsilon = \frac{n_{det}}{n_{tot}},$$

where n_{tot} is the number of particles passing the DUT which should be seen and n_{det} is the number of particles registered by the DUT. During a beam test, n_{tot} is given by the number of good tracks passing the DUT and n_{det} is given by the number of correctly detected hits. A hit is correctly detected if it was caused by the same particle which created the track. Since the telescope can only measure tracks, some assumptions are made about the hit/track pair. A hit is detected if

[31] The residual distribution for threshold of 3 is also smaller, since the telescope had a different geometry resulting in a better pointing resolution of $(3.9 \pm 0.4)\,\mu\text{m}$. The geometry can be found in appendix C.1

- It is above the detection threshold.
- It is in the same event as a good track.
- It is close to the extrapolated track intersect of a good track.

A track is good if

- It is the only track that intersects the active area of the DUT sensor
- Its χ^2 is small
- It does not intersect a broken/masked pixel or the neighbor of a broken/masked pixel
- The event it appears in is not broken[32]
- The track is far away from other tracks.
- The track is created during the integration time of the DUT.

A hit/track pair which fits all these requirements is assumed to be produced by the same particle.

Tracks can be separated in two sets: Trigger tracks and background tracks. A trigger track is the track belonging to a particle that went through the scintillator (and the FE-I4 trigger plane) and started the readout. Thus, trigger tracks have a fixed phase between the arrival of their particle and the start of the readout. Tracks from any other particle in an event are background tracks. They can have an arbitrary phase between the arrival of their particle and the start of the readout. The DUT should always see the trigger track, but since the integration time of the DUT is smaller than the telescope integration time, background tracks may be passing through the DUT outside its integration time window and may not be seen by it. Using background tracks in the sample used for DUT efficiency determination would artificially degrade the measured DUT efficiency. The above 'good' track cut tries to mitigate this effect by just using single track events. Events with a single track are assumed to only contain a trigger track, which arrives in the integration time of the DUT and is far away from other tracks, thus it is assumed as good.

If the track reconstruction efficiency of the telescope ϵ_{tele} is not 1, some tracks can be lost during the reconstruction, resulting in some multi-track events being reconstructed as single track events. If their track intersects the DUT, there are three possibilities:

1. The reconstructed track is the trigger track, so it must be detected by the DUT.
2. The reconstructed track is not the trigger track, but the track arrives during the DUT's integration time, so the DUT must detect it.
3. The reconstructed track is not the trigger track and the track arrives outside the DUT's integration time, so the DUT can not detect it.

The third point will artificially degrade the measured DUT efficiency ϵ_{DEPFET}, adding fake good tracks to the sample used for DUT efficiency determination, biasing the measurement towards the lower value and making the DUT efficiency depend on the telescope track reconstruction efficiency.

[32] The used firmware in the DHE sometimes dropped events or parts of events. The dropped and damaged events were noticed by software and replaced by empty DHE dummy data which is even smaller than empty real DHE events. If a EUDET event contains this empty DHE dummy data, it is flagged as broken and is ignored in the analysis

8.5.6.1 Determination of Fake Good Tracks

The number of fake good tracks in the track sample can be estimated as

$$N_{fake} = \sum_{n>1} P_1(n)(1 - P_2(n))(1 - P_3)P_4 t_n, \tag{8.2}$$

with:

- $P_1(n)$, the probability of reconstructing one track in an event with n real tracks. $P_1(n)$ can be calculated as
$$P_1(n) = \binom{n}{1} \cdot \epsilon_{tele} \cdot (1 - \epsilon_{tele})^{n-1},$$
where ϵ_{tele} is the track reconstruction efficiency of the telescope which is calculated in the next paragraph.

- $P_2(n)$, the probability that the reconstructed track is the trigger track. An n-track event contains a single trigger track, so $P_2(n)$ can be calculated as
$$P_2(n) = \frac{1}{n}.$$
$(1 - P_2(n))$ denotes the probability that the track is a background track.

- P_3, the probability that the reconstructed background track passes the DUT during the integration time of the DUT.

- P_4, the probability for a background track to survive the 'good' track cut performed by the efficiency analysis.

- t_n, the number of events with n real tracks. This can be estimated from the measured track distribution $k_0, \ldots, k_m$ where k_j is the number of reconstructed events with j tracks. Assuming a known real track distribution, the expected k_j can be calculated as
$$k_j = \sum_{i>=j} \binom{i}{j} \cdot \epsilon_{tele}^{j} \cdot (1 - \epsilon_{tele})^{i-j} \cdot t_i.$$
Creating the formulas for all $k_0, \ldots, k_m$ results in an $m \times m$ system of linear equations which can be solved to obtain $t_0, \ldots, t_m$

The above statements assume, that the telescope reconstruction efficiency identical for background and trigger tracks and is independent from the track multiplicity in an event. There is no physical difference between background and trigger tracks, so the first point is a valid assumption. Only events with 2 ,3 or 4 real tracks have a measurable contribution to N_{fake}, so the second point needs only to hold true for low track multiplicities. On a large sensor with 4 or less tracks, the possibility of a background track being close enougth to the trigger track to be falsely associated to the hit is very small. Thus, the point seems like a valid assumption as well.

Estimation of P_3 The MIMOSA sensor has a longer integration time than the DEPFET sensor, so it will detect more background particles. Due to the different way the sensors are read out, the fraction

of particles passing the DEPFET during its integration time is not exactly the same as the fraction of readout times.

- The MIMOSA sensor has an integration time of 115.2 µs per frame, it is read out in rolling shutter mode along its rows. In the setup at DESY, rows are oriented along the y axis of the telescope. When a trigger arrives, the currently read out frame and the next frame are both stored. Thus, every pixel is sensitive for twice the integration time, but the time it is sensitive depends on the row of the pixel. There can be an arbitrary phase between the trigger and the start of the readout, since the trigger can happen any time in the first frame.

- The DEPFET sensor has a shorter integration time of 30.7 µs per frame. It is read out along its rows, 4 rows (1 gate) at a time. In the setup at DESY, rows are oriented along the x axis of the telescope. When a trigger arrives, a frame is read out starting with the current gate, called start gate. All gates are read out once, except the start gate which is read out a second time and thus has a longer integration time[33].

Due to the different readout schemes, the phase between the integration time of both sensors can vary. The fraction $P_3 = \frac{\text{\#tracks in DEPFET and MIMOSA integration time}}{\text{\#tracks in MIMOSA integration time}}$ can be determined by (numerical) integration over

1. all phases a trigger signal can have with respect to MIMOSA frame start

2. all time differences a background particle can have with respect to the trigger signal[34]

3. all DEPFET gates the particle can arrive at. Since DEPFET readout can start at any gate, it is not important which gates are in the sensitive area of the MIMOSA

4. all MIMOSA rows the particle can arrive at. Since MIMOSA readout always start at row 0, it is important which MIMOSA rows cover the sensitive area of the DEPFET. From correlation data, this can be calculated to be Row 92-267. [35]

For each point it is determined if the DEPFET and/or the MIMOSA would see the particle. Using this, P_3 can be calculated to $P_3 = (13.44 \pm 0.01)\,\%$. In addition, the fraction of particles being read out by the DEPFET sensor which are not visible for the MIMOSA can be determined to be $(0.026 \pm 0.010)\,\%$. Errors given for these numbers were calculated by varying the simulation parameters and estimating the sensitivity of the result on these parameters. Varied parameters were:

- The trigger delay difference between DEPFET and MIMOSA. If a trigger arrives, both systems should start readout at the same time. The trigger delay modifies that behavior. An error of 100 ns was assumed.

- The size of the overlap between DEPFET and MIMOSA. This should not change if all planes are parallel. An error of 100 µm was assumed.

- The position of the DEPFET relative to the MIMOSA. This was determined using correlations between the first MIMOSA sensor and the DEPFET. An error of 100 µm was assumed.

The largest error contribution in both cases is the position of the DEPFET relative to the MIMOSA.

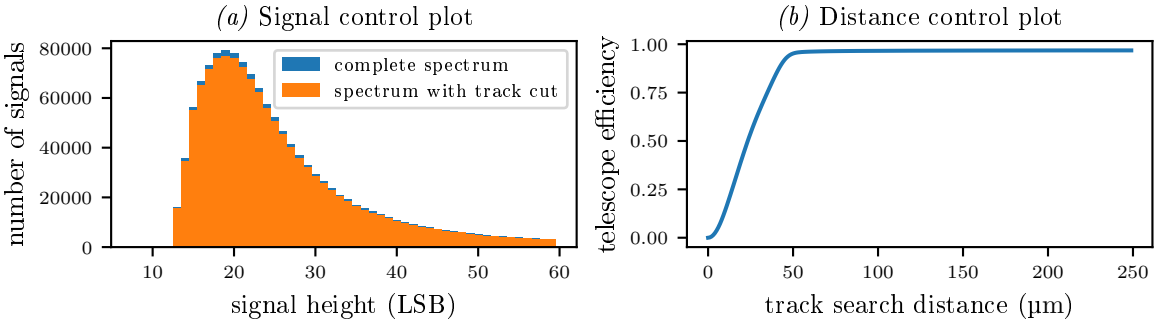


Figure 8.34: Control plots for telescope track reconstruction efficiency

Estimation of Telescope Track Reconstruction Efficiency The telescope reconstruction efficiency depends on the efficiency of the sensors, multiple scattering between telescope planes and at the DUT, track finding efficiency in software, requirements for a track[36] and many others[37]. With this amount of parameters, a simulation was not practicable. Instead, hits in the DEPFET Sensor were used: The DEPFET DUT has a shorter integration time than the EUDET telescope and DUT area used for analysis is well within the sensitive area of the EUDET telescope. Assuming perfect telescope efficiency, all particles passing through the DEPFET DUT should be recorded by the EUDET telescope. Using this, the telescope efficiency can be calculated as:

$$\epsilon_{tele} = \frac{N_{\text{DUT hits with track}}}{N_{\text{DUT hits}}}.$$

This measurement is sensitive to noise in the DUT, so strong cuts on minimum seed and cluster signal are performed to get an accurate number of DUT Hits $N_{\text{DUT hits}}$ without noise contribution[38]. As control, the signal of hits surviving the noise cut and the signal of hits with an corresponding track which survive the noise cut are investigated. This is shown in figure 8.34 *(a)*. Both show a similar spectrum; the spectrum after track cut is lower due to the track reconstruction efficiency, but shows the same distribution.

A similar analysis was performed using only two-pixel clusters to further reduce potential noise. This showed a compatible result with less statistics.

The control plot 8.34 *(b)* shows the dependence of ϵ_{tele} on the maximum allowed distance between a track and a hit. Above 50 µm, the efficiency remains almost constant, reaching the maximum value at 274 µm. Thus, the maximum search radius of 500 µm for track finding does not limit the telescope efficiency.

Using the cluster signal cut results in an efficiency of (97.07 ± 0.02) %, the cluster size cut results in (96.81 ± 0.03) %. The final number needs to be corrected, since in rare occasions the DEPFET sensor can detect particles which are out of the integration time for the MIMOSA telescope. In the previous paragraph this was estimated to occur for (0.026 ± 0.010) % of the background tracks, changing the determined

[33] This was performed since the delay of the readout chain was only known to ≈ 100 ns during the beam test.
[34] A background particle can have an arbitrary time between its arrival and the trigger signal, but it can be limited to ± twice the MIMOSA integration time, since out of that window, no particle can be detected by either of the sensors
[35] The integration assumes all hits have perpendicular incidence. This is a good approximation to the test beam setup.
[36] For this analysis, the track residual cut was $\chi^2 < 100$ and only tracks with at least 3 hits were considered.
[37] sensor occupancy, beam energy, etc.
[38] Cluster cut: 10 LSB, Seed cut 7 LSB

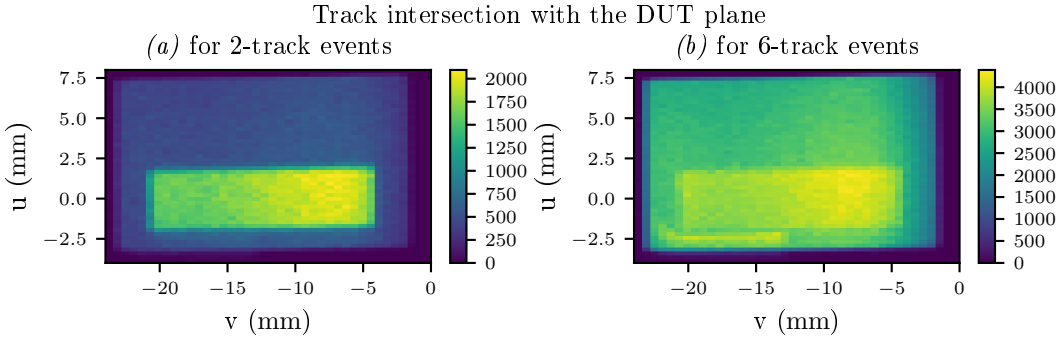


Figure 8.35: Distribution of track intersections with the DUT plane for 2- and 6-track events. The trigger window is visible in the 2-track events as a yellow rectangle, the 6-track events give good estimation for the background track event distribution. Tracks shown here do not neccesarily need to intersect the DUT, the coordinate of their intersection with the DUT plane is shown.

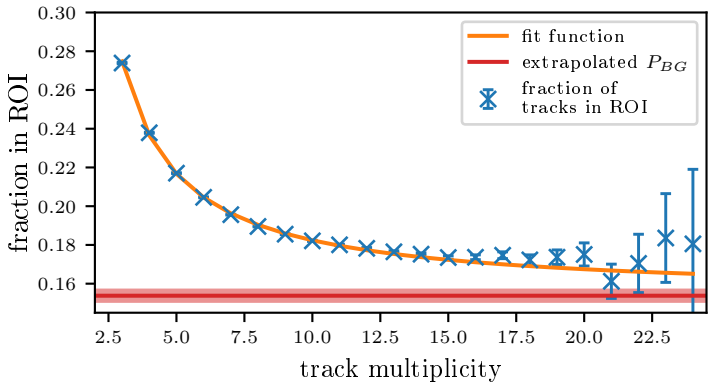


Figure 8.36: Probability of a track to be in the region of interest and to survive quality cuts, divided by track multiplicity of the event. Using a reciprocal function, the limit of this probability is determined.

track reconstruction efficiency to (97.11 ± 0.02) % using cluster signal cuts and (96.84 ± 0.03) % using cluster size cuts. For further calculations the weighted mean of both calculations will be used: ϵ_{tele} = (97.01 ± 0.03) %. The standard deviation of both values is used as error estimation.

Estimation of P_4 The probability P_4 describes if a particle survives the 'good track' cut. This can be split in two factors:

- P_R, which describes the probability of not containing a bad DHE event and matching the χ^2 cut. This is the same for background and trigger tracks
- P_{bg}, the probability for a background track to be in the region of interest. Similar to P_{bg}, P_{tt} can be defined for trigger tracks

Both P_{tt} and P_{bg} cannot be directly measured since each event contains both trigger tracks and background tracks. Figure 8.35 shows the coordinates in u and v, where tracks intersect the DUT plane. The rectangle with high track multiplicity in *(a)* is the trigger window, trigger tracks will be distributed only inside this area, while background tracks may be both inside and outside the trigger window. An estimation of the

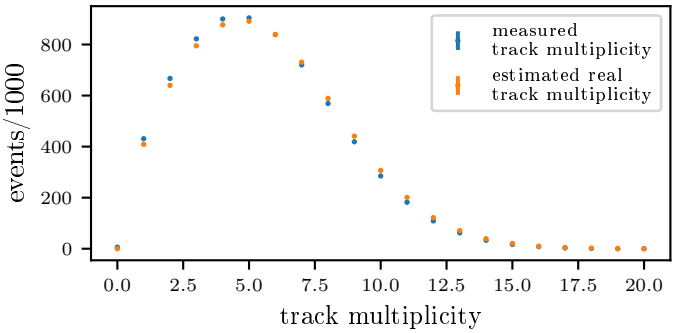


Figure 8.37: Control plots for telescope track reconstruction efficiency. Due to the huge statistic, the error bars are smaller than the points and not visible.

background track distribution can be seen in figure 8.35 *(b)*. Here only 6-track events are shown, so the background distribution is dominating. The region of interest used for DUT efficiency determination is completely inside the the trigger window. Track distributions of events with high track multiplicity are a close approximation of the background track distributions. This can be used by measuring the probability for tracks of an n-track event to be in the region of interest and survive the cuts specified by P_R. Figure 8.36 shows this probability separated against the track multiplicity. Fitting a reciprocal function the data allows an estimation of the limit and thus an estimate for $P_R \times P_{bg}$ of $(15.4 \pm 0.3)\,\%$, with a $\chi^2/_{d.o.f.} = 0.51$. The resulting $P_R \times P_{bg}$ value seems quite low, but since it is only needed for the estimation of a lower limit of N_{fake}, a systematic error making P_{bg} smaller will lead to an underestimation of the DUT efficiency. The error on $P_R \times P_{bg}$ was increased by a factor of 3 to take uncertainties due to the extrapolation into account.

P_R should not vary with the track multiplicity. This was verified by measuring P_R for different track multiplicities. The result is in agreement with being constant and can be found in appendix C.2.

Estimation of $t_0, \ldots, t_m$ To obtain the real track distribution $t_0, \ldots, t_m$ from the measured track distribution $k_0, \ldots, k_m$, one can use the formula

$$k_j = \sum_{i>=j} \binom{i}{j} \cdot \epsilon_{tele}^{j} \cdot (1 - \epsilon_{tele})^{i-j} \cdot t_i.$$

which describes the expected number of tracks with j measured tracks given a telescope efficiency ϵ_{tele} and a real $t_0, \ldots, t_m$. Using

$$t = \begin{bmatrix} t_0 \\ \vdots \\ t_m \end{bmatrix}, \; k = \begin{bmatrix} k_0 \\ \vdots \\ k_m \end{bmatrix}, \; A = \begin{bmatrix} a_{00} & \ldots & a_{0m} \\ \vdots & \ddots & \vdots \\ a_{m0} & \ldots & a_{mm} \end{bmatrix}, \text{ with } a_{ji} = \begin{cases} \binom{i}{j} \cdot \epsilon_{tele}^{j} \cdot (1 - \epsilon_{tele})^{i-j}, & \text{for } i \geq j \\ 0, & \text{for } i < j \end{cases} \tag{8.3}$$

this can be written as $A \cdot t = k$, where A is invertible and depends only on ϵ_{tele}. The real track distribution can be calculated to be $t = A^{-1} \cdot k$. Errors on t are propagated using a Monte-Carlo simulation. The result is shown in figure 8.37, which shows the measured track multiplicity and the estimated real multiplicity.

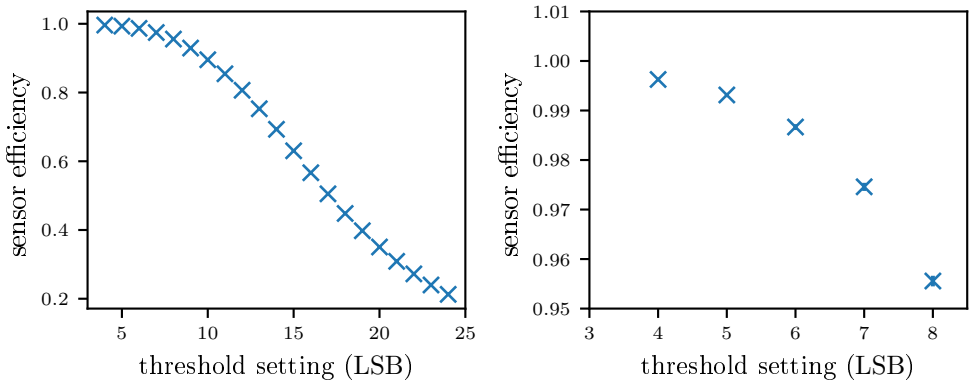


Figure 8.38: Hit efficiency against threshold setting. High thresholds reduce the detection efficiency. *Right* shows a zoomed in version. Each LSB corresponds to $(230 \pm 20)\,e$, thus the lowest setting shown here corresponds to around 1000 electrons.

Result and Uncertainty Putting the results of the previous points together, the expected number of fake single track events can be calculated. Formula 8.2 can be rewritten as

$$N_{fake} = \sum_{n>1} P_1(n)(1 - P_2(n))(1 - P_3)P_4 t_n = \sum_{n>1} \binom{n}{1} \cdot \epsilon_{tele} \cdot (1 - \epsilon_{tele})^{n-1}(1 - \frac{1}{n})(1 - P_3)P_R P_{bg} t_n, \quad (8.4)$$

with $\epsilon_{tele} = (97.01 \pm 0.03)\,\%$, $P_3 = (13.89 \pm 0.01)\,\%$, $P_R \times P_{bg} = (15.4 \pm 0.3)\,\%$ and $t_0, \ldots, t_m$ like shown in figure 8.37. This results in an estimation of $N_{fake} = (2\,520 \pm 60)$ events. Several parameters in the equation are not statistically independent, for example both $P_1(n)$ and $t_0, \ldots, t_m$ depend on ϵ_{tele}. Thus, the error was calculated using a Monte-Carlo simulation. In each step of the Monte-Carlo simulation, all values except P_3, $P_R \cdot P_{bg}$ and the telescope efficiency correction were recalculated and their differences propagated.

8.5.6.2 Efficiency Estimate

Without subtracting fake single track events, the efficiency determined for the sensor is $\epsilon_{DEPFET} = (98.81 \pm 0.03)\,\%$ using a settings of *clear low* =3 V, *capacitively coupled clear gate* =−2 V, *drift* =−3 V, *depletion* =−20 V and a threshold setting of 4 LSB. Using the calculated value for N_{fake} and subtracting it from the number of recorded events results in an efficiency of $\epsilon_{DEPFET} = (99.82 \pm 0.03)\,\%$. As above, the error was calculated using a Monte-Carlo simulation. In each step of the Monte-Carlo simulation, all values except P_3, $P_R \cdot P_{bg}$ and the telescope efficiency correction were recalculated and their differences propagated. Using each N_{fake}, the expected number of tracks was calculated. Together with the number of tracks with hits, the efficiency distribution was reconstructed using Wilson intervals, a method described in [90] and recommended by [91]. The resulting efficiency distributions were added for all steps performed in the Monte-Carlo simulation. From the resulting distribution, expectation value and uncertainty are extracted. The distribution (and thus the uncertainty) is not symmetric, but rounds to the same value.

The expected efficiency of a DEPFET sensor is determined by its dead time: Charge which arrives in the pixel when it is cleared will travel to the clear contact and is lost. Charge which arrives in a pixel after the DCD sampled the current is lost as well, charge arriving after the first sample of the ADC has a smaller chance of being reconstructed.

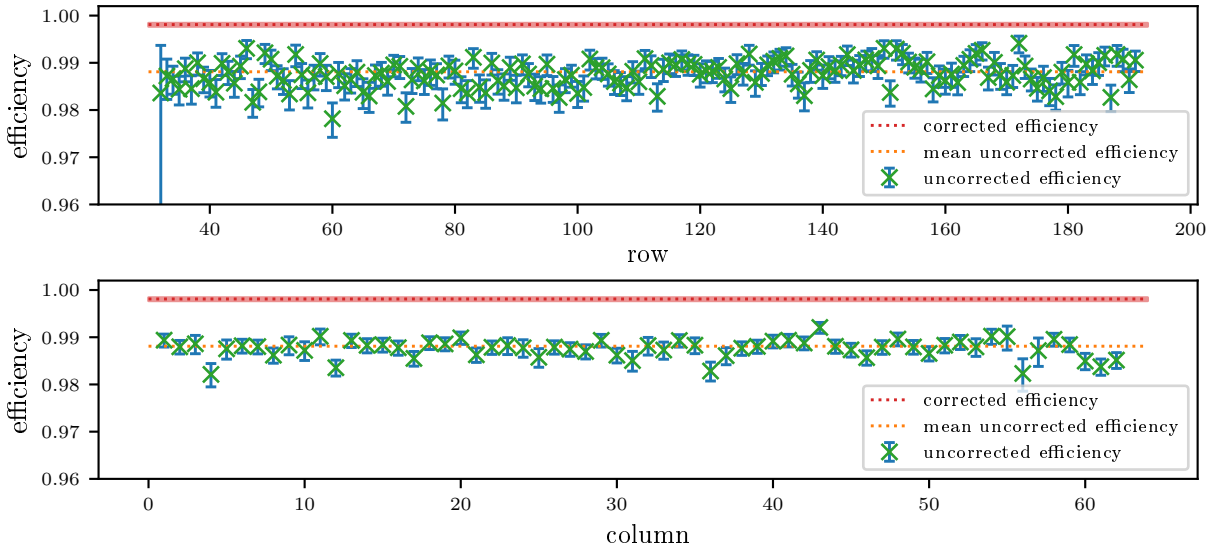


Figure 8.39: Hit efficiency (without correction) for individual rows and columns. The calculated uncorrected mean efficiency is shown as dashed line. After correction, the efficiency should be distributed around the second line shown.

Together, the dead time of the system is estimated to be 32 ns, small in comparison to the frame time of 30 720 ns, but the dead time is large enough to explain 0.10 % missing efficiency — a large part of the efficiency loss. The effective dead time of the DEPFET is further increased by second order effects: Charge arriving in the internal gate changes the current flowing on the drain line - but the rise time on the drain line and on the DCDs TIA are not instant. Thus, charge arriving shortly before the dead time may not be seen. With previous readout systems, effects from particles arriving in the first gate while it is read out could be mitigated by cutting out these events to get a better understanding on sensor performance. With the DHE firmware available during the beam test campaign, this was not possible.

The threshold has a large impact on the efficiency. This is shown in figure 8.38, where the efficiency is shown versus the zero suppression threshold setting. At larger thresholds, more hits are lost. Unfortunately, no large data set with a threshold setting of 3 LSB and optimal voltages is available, thus it can not be verified if a lower threshold would further increase the efficiency.

Figure 8.39 shows the efficiency for individual rows and columns. For this, subtracting the fake events directly from the data set is not possible, thus the uncorrected efficiency is calculated and shown. Additional lines in the plot show the corrected efficiency value. No gradient can be seen in the efficiency along rows and columns. The two columns (4 and 56) with the lowest efficiency (and large error bars) each contain a broken drain line.

An efficiency map can be seen in figure 8.40, where *(a)* shows the uncorrected efficiency and *(b)* shows the statistics available. The statistic is very low, thus large fluctuations in the measured efficiency are visible. For the efficiency measurement pixels were masked if they or one of their neighbors is known to be bad or noisy; thus many 3x3 areas are masked. Several broken drain lines are visible in this plot. A few pixel with low efficiency are visible. This can be due to bad pedestal calibration leading to artificially increased threshold or nonlinear behavior of the ADC at this point. In other runs, most of them work fine (compare with C.9, same bias voltages, higher threshold, less noisy pixels), thus they are included in the efficiency measurement.

To investigate charge loss in the pixels, an in-pixel efficiency plot can be created by projecting all

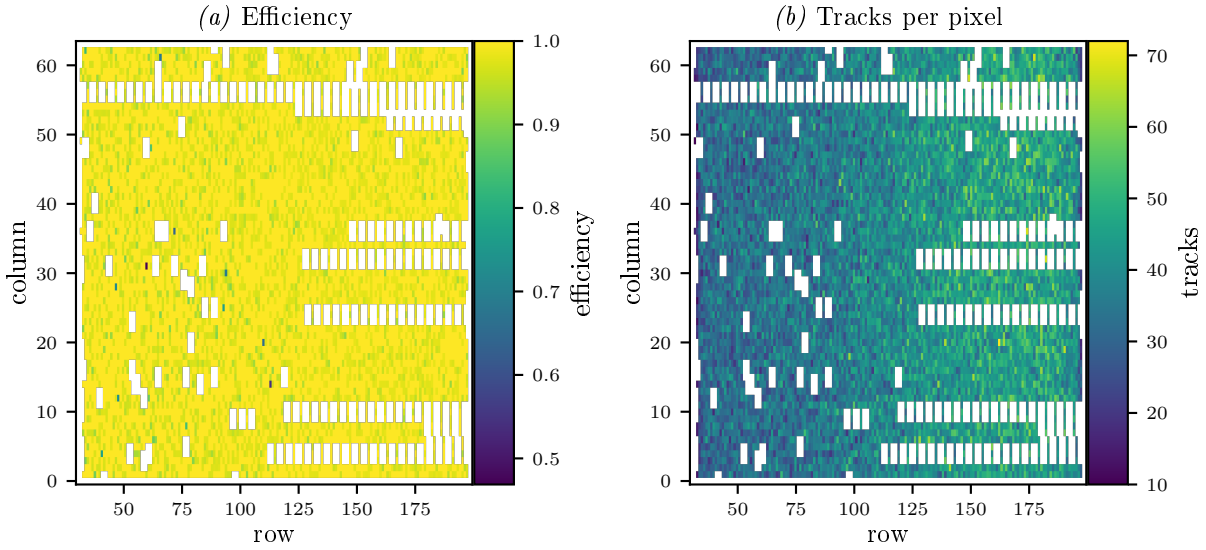


Figure 8.40: Efficiency (without correction) for individual pixels. In mean, efficiencies are expected to be 1 % better than shown here. As shown in *(b)*, the number of hits per pixel is low, so large variations in the measured efficiency are expected.

signals onto a super-pixel like explained in 8.5.3. This results in figure 8.41, where *(b)* shows the uncorrected efficiency for a threshold of 4 LSB. The pixel form is shown by the seed signal distribution shown in *(a)*. At the edges of the pixels where charge is shared between 4 pixels, the efficiency seems to be lower. This effect increases significantly when increasing the threshold to 5 LSB like shown in figure *(c)*. The operation of the DEPFET with a threshold of 3 LSB is possible with reasonable noise occupancy and would improve the efficiency at pixel edges.

Estimation of Systematic Effects The model built to estimate N_{fake} makes some assumptions, which could result in systematic errors. These will be discussed in the following part.

Fake Trigger One assumption is, that each event has a trigger-track. In the real setup, noise in the trigger plane and the scintillators could lead to fake trigger, which results in events without trigger track. These are not handled by the calculation above. However, the FE-I4 trigger plane was used at a high threshold and only inner pixels were used. Used in coincidence with a scintillator, the system showed a very low fake rate. No specific measurement was done for this but during the beam test the trigger counter would stay constant over several tens of seconds. Thus, the fake trigger rate can be assumed to be below 0.1 Hz, while the trigger rate was above 1 kHz for the run, resulting in a fake event fraction below 0.01 %. Some tracks from fake trigger events could arrive in time or will be removed by the good pixel cut, so the fraction of fake events will be even smaller in the single track event sample. In total, this contribution is negligibly small. It decreases the measured DUT efficiency, thus the real DUT efficiency can be assumed to be larger.

It is worth noting that the determination of ϵ_{tele} is not influenced by fake triggers.

Variation of the Telescope Reconstruction Efficiency The telescope reconstruction efficiency is assumed to be constant over the whole telescope area, however this is not necessarily the case.

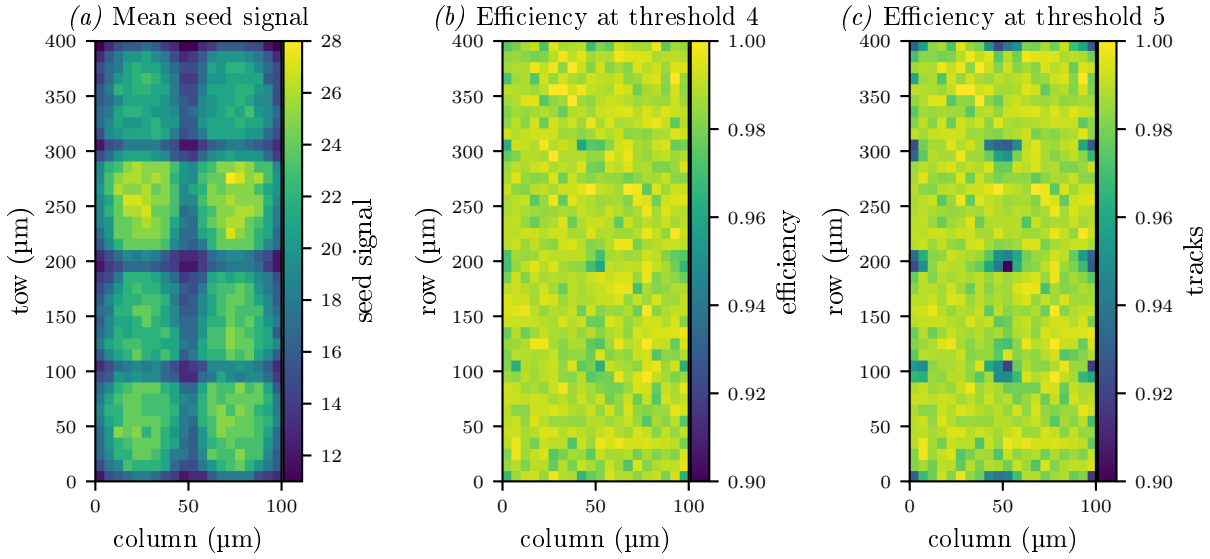


Figure 8.41: In-pixel efficiency (without correction). In mean, efficiencies are expected be to 1 % better than shown here. *(a)* shows the expected seed signal to give an indication where pixel borders and edges are. *(b)* and *(c)* show the efficiency for two different thresholds. Increasing threshold reduces efficiency at the pixel edges.

Telescope reconstruction efficiency is influenced by several parameters, like multiple scattering in the DUT and the hit detection efficiency of the telescope sensor. The reconstruction does only need hits in 4 of the 6 planes so reconstruction efficiency variations due to hit detection efficiency variations in the MIMOSA should be strongly suppressed[39]. The reconstruction efficiency can depend on the radiation length of the DUT. More radiation length results in more multiple scattering, scattering angles which are larger than assumed by the track finder/track fitter and thus a lower reconstruction efficiency. The measurement of the reconstruction efficiency was performed where tracks pass the DUT sensor, i.e where the DUT is thinnest. Thus the telescope efficiency at that position is expected to be highest and is (slightly) overestimated.

An overestimated telescope reconstruction efficiency results in a too small estimation of N_{fake} and thus an underestimation of the DUT efficiency.

Correction Factor used in Telescope Reconstruction Efficiency The measurement of the telescope track reconstruction efficiency used a correction factor to correct for the rare cases where due to integration time the DEPFET can detect a particle but the telescope cannot. However, this is only true for particles with an arbitrary phase between trigger and their arrival (i.e. background tracks). Trigger tracks would always reach the telescope in its integration time and should be seen. Using the correction on all hits assumes that all hits in the DEPFET were due to background tracks, not correcting the hit sample assumes all hits were due to trigger tracks. Since the ratio of trigger and background tracks in the sample is unknown, all tracks are assumed to be background tracks, which results in an overestimated track reconstruction efficiency and an underestimated DUT efficiency. Using the underestimated track reconstruction efficiency would result in an overestimated DUT efficiency of $(99.84 \pm 0.02)\,\%$.

The correction factor is strongly dependent on the DEPFET position relative to the MIMOSA. In a

[39] The expected MIMOSA hit detection efficiency is above 98.5 % for a threshold of 8 [92]. During the beam test a threshold of 7 was used which will result in a higher efficiency.

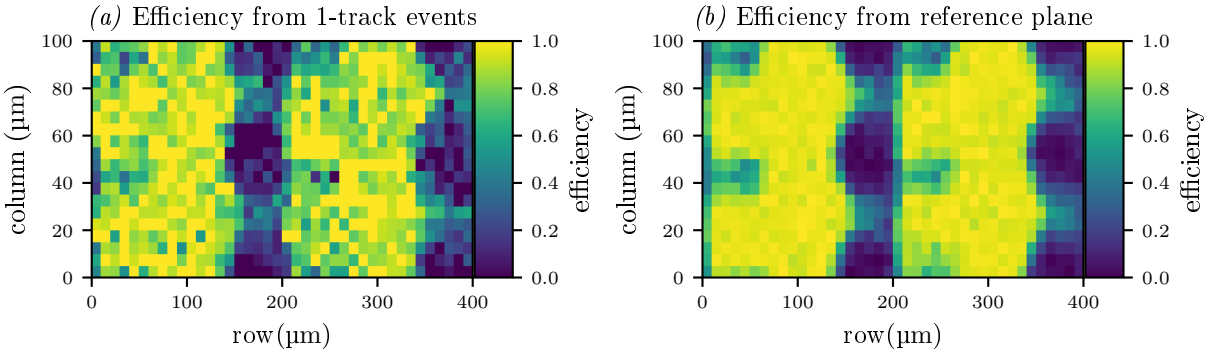


Figure 8.42: In pixel efficiency using different selection criteria. *a* shows the efficiency using a single track events, while *(b)* shows the efficiency using tracks with a hit in a fast reference plane.

simulation it was varied by 1.2 mm up and by 0.8 mm down, resulting in total DUT efficiencies between $\epsilon_{DEPFET} = (99.67 \pm 0.03)\,\%$ (up) and $\epsilon_{DEPFET} = (99.84 \pm 0.02)\,\%$ (down). Thus, the effect on ϵ_{DEPFET} is limited.

8.5.7 Alternative Efficiency Determination

As shown above, the efficiency can be influenced by the long integration time, a limited track reconstruction efficiency and fake triggers. The estimation of N_{fake} could be omitted by using a better experimental setup. This could be achieved by

- using a lower beam intensity. N_{fake} mainly consists of wrong reconstructed 2-track events. Using a beam intensity which produces mainly one-track events would reduce the effect of N_{fake}.
- using a fast reference plane to identify the track which triggered the system. Efficiency studies can then be performed using only tracks with a hit in the reference plane.

A FE-I4 was used as trigger plane during the beam test performed with this module. With a time resolution of 25 ns, the FE-I4 could be used as such a device [84, 93], but due to the lack of expertise, the FE-I4 could not be integrated into the EUDAQ data stream. For future beam test this would be strongly recommended.

During some runs, a small DEPFET sensor was present in the data stream. With its readout time of 1.6 µs it can work as a time reference. Unfortunately, during the runs with the small DEPFET sensor present, the DUT had a non optimal *depletion* potential of −24 V or worse. The bad performance at this voltage was already shown in figure 8.31 for laser measurements.

In this run, the system was triggered using only the FE-I4 without coincidence, which resulted in a high rate of fake triggers[40]. Still, an effect can be seen. Figure 8.42 *(a)* shows the in-pixel efficiency of the DUT determined using single track events. Figure *(b)* shows the in-pixel efficiency using tracks with a hit in the second DEPFET plane. The overall efficiency at this known bad setting raises from

[40] The runs show more events without reconstructed tracks than single-track event. This cannot be explained due to telescope efficiency since it would require an efficiency of below 50 %, but a rough estimation of the track reconstruction efficiency in this measurement shows an efficiency of at least (95.7 ± 0.2) %. The FE-I4 shows a low noise rate, fake trigger may be created from particles which are scattered into the ROI on the FE-I4 but did not pass enough telescope planes to be registered as a particle. A prime suspect for this is the thick copper cooling block on the DUT, which is close to the ROI unsed on the FE-I4.

(65.7 ± 1.1) % to (69.7 ± 0.3) %. The efficiency analysis use the same pixel in both cases to minimize systematic effects. The small DEPFET matrix covers only a small part of the large DUT; thus only a small fraction of the single track events was used for the analysis, resulting in a large uncertainty. For the second analysis track multiplicity cut was not needed, resulting in a higher statistic for this measurement and smaller uncertainty. Due to fake triggers the increase in measured efficiency is quite large[41], but it shows that a reference plane is quite essential.

Another important point was the usage of coincidences between a FE-I4 and a scintillator. Even if noise hits on the FE-I4 could be neglected, it can be triggered by scattered particles which will not create a track in the telescope. Requiring a detection of the particle before and after the telescope suppresses this effect. When using the FE-i4 as a reference plane, the above mentioned effect would be suppressed even when triggering only with an FE-I4, because the reconstructed tracks are unlikely to be matched with a stray hit and are thus being discarded.

8.5.8 Signal to Noise and Pixel Gain Spread

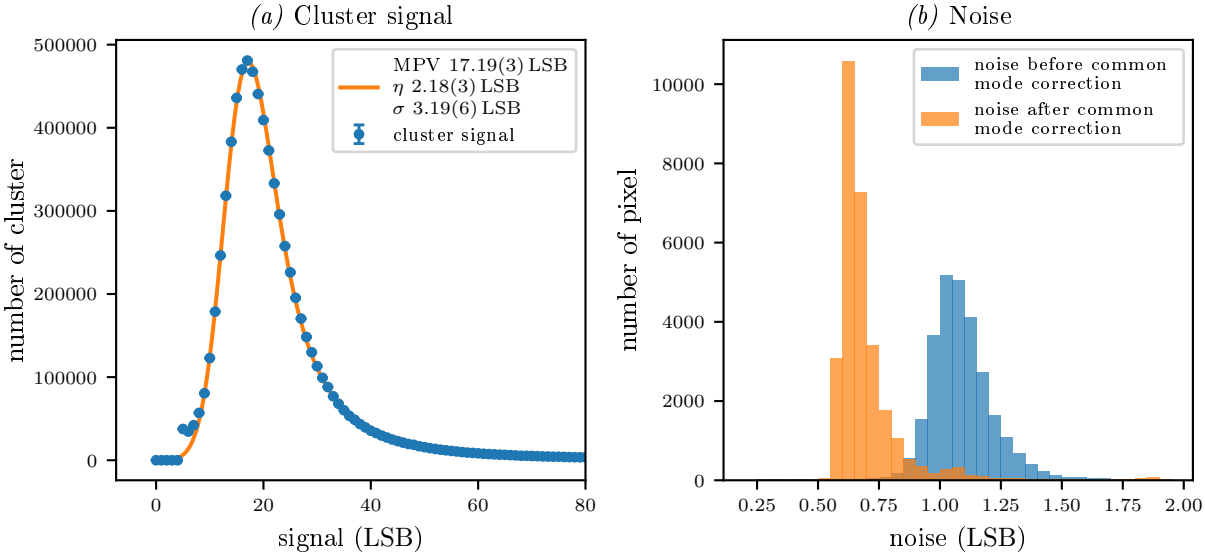


Figure 8.43: Cluster signal and sensor noise *(a)* shows the expected cluster signal and a langau distribution. *(b)* shows noise before and after digital common mode correction.

The **S**ignal to **N**oise **R**atio (SNR) is one of the key parameters of a detector system. A high SNR allows good detection efficiency without large noise occupancy on the detector. Figure 8.43 *(a)* shows the spectrum measured by the DUT. Only hits with corresponding tracks are used, so the spectrum is virtually free of noise hits. The MPV of the spectrum is at (17.19 ± 0.03) LSB, the mean noise after common mode correction is (0.68 ± 0.13) LSB. The given error is the standard deviation of the noise

[41] The calculation for N_{fake} needs to be changed to accommodate fake trigger events:

$$N_{fake} = \sum_{n>1} P_1(n)(1-P_2(n))(1-P_3)P_4 t_n + \sum_{n\geq 1} P_1(n)(1-P_3)P_4 f_n,$$

where t_n is the number of correctly triggered events with n tracks and f_n is the number of fake triggered events with n tracks. The rest of quantities is defined like in 8.2. N_{fake} increase especially due to fake trigger events with a correctly reconstructed single track.

distribution resulting in an

$$\mathrm{SNR} = 25 \pm 5,$$

where the error is an indication of the distribution width. Assuming linear charge response of the sensor with no offset (i.e. a measured signal of 0 corresponds to a charge of 0), this results in a

$$g_q = (380 \pm 30)\,\mathrm{pA}/e.$$

The DCD was used with the same settings as in previous measurements, but no transfer curves could be taken using Hybrid 6. Thus, the measurement results from Hybrid 4 and Hybrid 5 were used to estimate the ADC gain. Potential differences due to the different powering scheme could influence the exact response, thus large errors were assumed for the g_q determination.

The noise measured by the pedestal calculation a large tail to higher values. Noise values above 1.5 LSB were ignored in the analysis, since this is (in part) due to the way pedestals are taken: Every time the system is started or stopped, a random part of the offset memory is overwritten, resulting in incorrectly applied 2-bit DAC settings in some pixel. Pedestals are then taken with this part broken. To get good pedestals from all pixel, the above is repeated ≈ 80 times so that many more correct values are available for every pixel. Common mode corrected pedestals are calculated in two iterations:

1. Pedestal without common mode corrections are calculated by calculating the mean value for each pixel.

2. The coarse pedestals are used to calculate common mode corrected pedestal

   a) The common mode is calculated using a two-pass algorithm similar to the one presented in 5.3 (page 42), by calculating a coarse common mode using the coarse pedestal and the coarse common mode to detect pixel which are hit, then calculating the second pass common mode without hit pixel.

   b) Using the hit information and the fine common mode from above, the common mode corrected pixel signal is calculated for all pixels without hit in this frame.

   c) Using the common mode corrected pixel signal, the pedestal for all pixels are calculated, ignoring frames where the pixel is hit.

The algorithm does not cope perfectly with broken data like the one mentioned above: The coarse pedestals are almost correct, even for pixels which had broken offsets during one pedestal taking, since only $1/80$ of the data is biased.

Too high signals from pixel with broken offsets are filtered out, but too low signals are kept. Since up to 25 % of the pixel in a gate can be influenced by broken offsets, they can influence the calculated common mode. The effect on the mean pedestal value is negligible, since the common mode is only a few LSB off in a small fraction of the the frames, but the effect is visible in the noise, which is higher for some gates which contained broken pixel, as can be seen in figure 8.44, which shows the noise map of the sensor both with and without common mode correction. Yellow dots are due to pixels which had broken offsets at one point, so they received very different ADC values. Some gates with broken offsets show an increased noise.

The spectrum in 8.43 *(a)* can be approximated by a LanGau distribution. For a perfect detector, the spectrum is expected to be a Landau distribution, real detectors will result in a LanGau; a Landau distribution folded with a Gaussian distribution to simulate the detector resolution, readout noise and gain spread. The resulting width of the Gaussian distribution is $\sigma_{gauss} = (3.19 \pm 0.06)\,\mathrm{LSB}$. At least $\sigma_{noise} = (0.68 \pm 0.13)\,\mathrm{LSB}$ of this are due to noise. The noise given above was obtained using offline

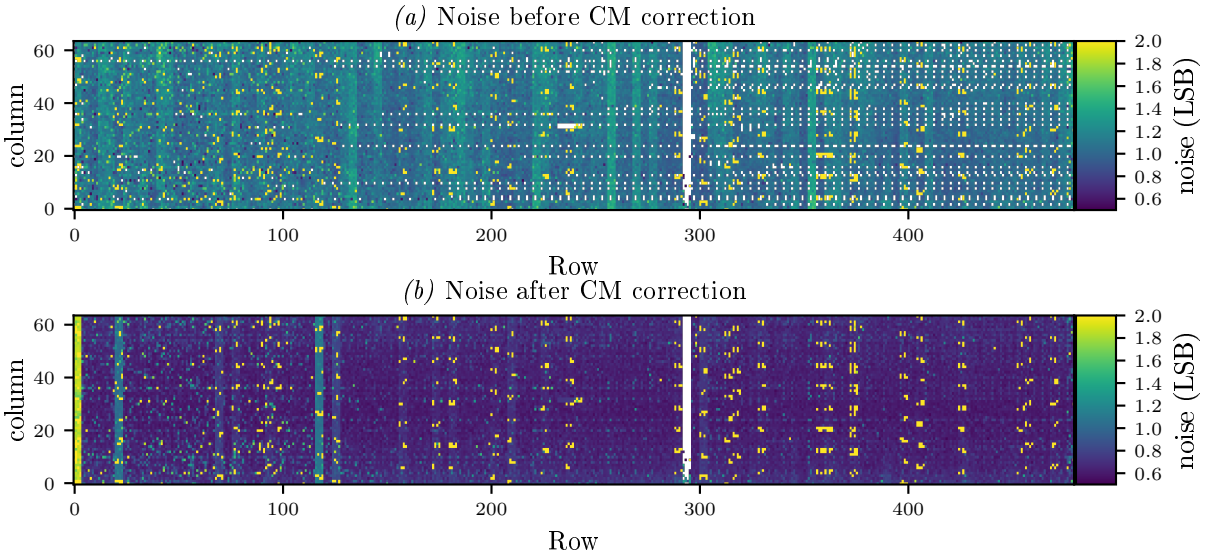


Figure 8.44: Noise maps of the DUT. *(a)* shows the noise map before common mode correction. Pixel belonging to a broken drain line have a noise of 0 as has the broken gate. Yellow pixel received some broken data during pedestal taking. *(b)* shows noise after digital common mode correction. The noise of most pixel is reduced. Unconnected channel show noise now — an artifact of the common mode correction.

common mode correction. The online common mode correction by the DHP is less accurate due to integer arithmetic, resulting in a slightly higher noise. The other main effect on this is the gain spread of the pixels.

The pixel to pixel gain spread can be estimated using beam test data. For each pixel a signal histogram is created and filled with the signal deposited. To get the unbiased gain of a single pixel, only hits with an associated track which hits the pixel in its center are used. The center is defined as the inner $30 \times 80\,\mu m^2$, so that the outer $10\,\mu m$ at each pixel border are not used. Due to the limited pointing resolution, some particles hitting the pixel border can be reconstructed in the pixel center. To limit the effect of these tracks, only single pixel hits are used. The MPV of the distribution is determined by fitting a Langau distribution to the data. The resulting MPV is shown as color code against the pixel position in figure 8.45 *(b)*.

Using the large laser scan performed on the module, a gain can be extracted from laser scans where the pixel center is hit. A cut on the cluster size is not sufficient here since one could hit a trench close to the pixel border where the signal is lower due to the charge sharing but the shared charge is below the threshold and the cluster size is still 1. Thus only laser measurements are taken which

- have a cluster size of 1 in both directions.
- have only neighbors which have the same seed pixel.
- whose neighbors in row direction have a row cluster size close to 1.
- whose neighbors in column direction have a column cluster size close to 1.

For most pixels this results in at least one measurement position which hit the pixel center. The signal of this laser position is used as an estimation of the relative pixel gain. If multiple laser position are available for a laser position, the mean of their signals is used. The resulting gain map is shown in figure

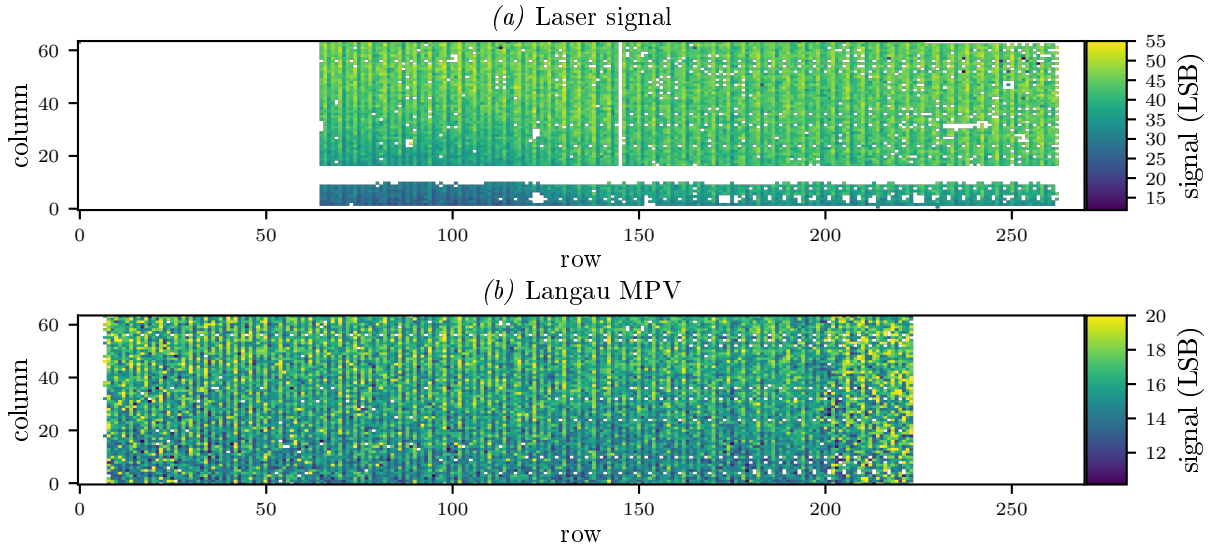


Figure 8.45: Per pixel gain. *(a)*: Gain determined by a large data laser scan. A gradient to lower columns is visible. *(b)*: Gain determined by beam test measurements. Pixel below row 40 and above row 200 have a large statistical error since they were not hit often.

8.45 *(a)*, pixel without a good laser setting are shown as white. Most white pixels are due to broken drain lines or backside metalization blocking the light. Pixel below row 65 could not be illuminated since the laser optic would collide with the metal cooling block. A gradient is visible in the laser signal. Pixel at lower column indices receive a lower signal, an effect which also can seen in the LanGau MPV, albeit less pronounced. The laser signal is especially low for small row and small columns, an effect which can not be seen in the LanGau MPV. This could point to a surface effect, since the absorption length of the laser is short.

For both gain determinations, the gain fluctuation within a gate follows the same pattern: Two rows with a medium gain, then one row with large gain and one row with low gain. The exact reason for the this is unknown.

The measured gain spread for the laser data is $(13.8 \pm 0.5)\,\%$, the beam test data results in a spread of $(14.2 \pm 0.5)\,\%$. For beam test data, all pixels above row 190 and below row 65 were omitted, as they have only very low statistics which would artificially widen the gain distribution. The gain spread of the beam test is expected to be wider, since the gain calculation there has a larger error due to statistics. The gain spread results in a spread of the expected MPV signal of about $\sigma_{gain} = (2.4 \pm 0.1)\,\mathrm{LSB}$, the bulk part observed by the LanGau fit.

8.6 Measurement Results

In this chapter, the pedestal compression algorithm and the performance of a large DEPFET matrix were investigated. The pedestal compression algorithm proved to be stable under different situations, both using simulated data and measurement data. As a result of the simulation, the pDAC width for the production DCD version for Belle II was adjusted to $\approx 0.5\,\mu\mathrm{A}$ in order to increase performance. The operational expertise gained by working with the wide pedestal spread of this matrix together with transistor level current measurements of a final DEPFET prototype matrix resulted in optimized input

current ranges for the DCD production version.

Using the first large PXD6 DEPFET matrix, good results could be obtained: The matrix showed an efficiency of

$$\epsilon_{DEPFET} = (99.83 \pm 0.02)\,\% \quad \text{with an SNR of } 25 \pm 5.$$

Large operation windows of several volt for *drift* and *depletion* were found using both laser and beam data, *clear low* had an operation window of 1 V, *capacitively coupled clear gate* an operation window of only 0.5 V. The result for

$$g_q = (380 \pm 30)\,\mathrm{pA}\,e^{-1}$$

is very low, compared with the smaller matrix. Some issues were seen on the matrix. For operation a very negative *gate-on* = −4.3 V voltage was needed, still resulting in only about ⅔ of the expected drain current and producing a very wide pedestal distribution.

Compared to previous works, the large pixel matrix performed worse. In [83] DEPFET matrices with shorter gate length[42] higher drain current and different pixel layouts are used. This results in g_q values above $500\,\mathrm{pA}\,e^{-1}$. In addition the matrices are read without zero suppression, allowing lower thresholds. This results in a superior resolution of 9.6 µm in u at the same gate pixel pitch, without increasing the *depletion* voltage. The determined efficiency in [83] is better than 99.5 %[43] for a threshold of 525 e. The efficiency against threshold is comparable. Both large and small matrices show an efficiency below 99 % for thresholds above 1 200 e. In the large PXD6 matrix this results in a maximal threshold of 5 LSB, in small PXD6 matrices in [83] a larger threshold (in LSB) would be possible, though the DCD used a lower gain there. For large Belle II modules, the low signal shown by the large PXD6 matrix is not an issue, since they will feature shorter (5 µm) gates and a thickness of 75 µm, resulting in 50 % more charge in the internal gate *and* a higher amplification.

The comparison between laser measurement and beam test measurements showed that both obtained largely the same results: A setting which results in bad performance when measuring with a laser shows also bad perfromance when measuring ionizing particles. However, some small like charge loss below the *capacitively coupled clear gate* could only be observed at the beam test. This effect were small and did not influence the efficiency, thus they will not impair the performance for a tracking detector. For further DEPFET generations this response could be improved by an optimization of *drift* and *capacitively coupled clear gate*, which needs to be performed at a beam test.

The efficiency measurement required the determination of fake single track events in the data sample; events that contained more than one real track but were reconstructed as single track events. Several systematic errors were investigated and their effect on the number of fake single track events was estimated. As an alternative to this estimation, a fast time reference was used in some measurements. The improvement of the measured efficiency resulting from such a time reference was shown.

[42] 5 µm vs 6 µm used in the large PXD6 matrix

[43] No correction for N_{fake} was performed. A lower beam intensity was used producing mainly single track events. The DUT was small and at the edge of the beam spot, so the factor P_4 is small. The given efficiency was calculated ignoring effects in the first and last gate in each frame but including pixel at the matrix border which were masked in Hybrid 6.

CHAPTER 9

Conclusion and outlook

This thesis presents several key measurements which were performed in the development of large DEPFET pixel detectors for Belle II.

The characterization and irradiation of the DCDBv2 unveiled several issues, like the non-temperature stable reference current and DACs with non-optimal strength. Between 20 kGy and 60 kGy the DCD shows a much higher current on its digital part, at 20 kGy and 35 kGy its analog part could not be switched off using the configuration bits. This is due to theshold shift of the nMOS structures being largest at these irradiation levels. Reference current source, DAC strength and radiation susceptible 'off' switch were fixed in subsequent DCD versions, the higher current consumption seems to be an issue due to the high dose rates applied and due to incomplete annealing. The DCD performance after 200 kGy and at different temperatures was found to be excellent; in noise and linearity it is comparable to an unirradiated DCD. The ADC gain increased by $(10 \pm 3)\,\%$, which can be reversed by different $\text{Source}_1/\text{Source}_2$ settings. The increase was due to anealing of some damage over several days. Measurements at doses between 20 kGy and 200 kGy show a difference in $\text{Source}_1/\text{Source}_2$ strength, both in gain and linearity. Since they stayed at default values, the result for bias voltage measurements is not optimal.

A detailed investigation of the communication between DCD and DHP revealed issues on both chips which were addressed in subsequent versions.

The characterization of the first ever produced full scale system demonstrator (Hybrid 5) yielded good results: Determined optimal voltages (*drift* −3 V, *depletion* −19 V, *clear low* 3 V, *cleargate* −2 V) were expected from simulation. Source measurements resulted in $g_q = (453 \pm 5)\,\frac{\text{pA}}{e}$., a value in the expected range for DEPFETs with 6 µm gate length. The charge calibration showed a good linearity between deposited charge and measured signal with deviations of 1 LSB, but has a larger than expected offset. A possible explanation of this was found; newer systems do not show this behavior. After the characterization, the full scale system demonstrator was successfully tested in a beam test.

Further, measurements on the first large DEPFET matrix of generation PXD6 were shown; the first large matrix ever to be used in a beam test. On this, voltage measurements were performed using both beam test and laser data; investigating the difference. Due to the way the DCD samples DEPFET current, every gate needs to be sampled twice to get good performance. While voltages producing bad laser measurement results implicate bad beam test results, some minor features could only be seen in beam test data. Thus, final Belle II modules need to be investigated in beam tests to ensure a good understanding of potential charge loss mechanisms.

All large matrices of PXD6 generation needed an unexpectedly low *gate-on* potential, showed a wide pedestal distribution and a low drain current. This resulted in a low g_q of $(380 \pm 30)\,\frac{\text{pA}}{e}$. The issue with *gate-on* could be due to system issues on the Hybrid 6 board or on the metal routing on the matrix, as

small matrices from the same generation do not show similar issues. Due to this, the SNR of the matrix was only at 25 ± 5, where the large error is due to the noise distribution.

The wide pedestal distribution of the large DEPFET modules made it mandatory to use of the 2-bit DACs for pedestal compression. For this, the algorithm presented in [47] was improved and systematic investigations of its functionality were performed. The algorithm was then successfully used on real devices, reducing their pedestal spread and making beam test measurements possible.

In beam test measurements, resolutions of $\sigma_{u\ hit} = 9.80 \pm 0.15$ to $11.4 \pm 0.2\,\mu\text{m}$ were observed using perpendicular incidence for the pixel pitch of 50 µm, which is identical to the pitch of final modules. Along the pixel pitch of 100 µm, resolution of $\sigma_{v\ hit} = 25.63 \pm 0.06$ to $26.38 \pm 0.08\,\mu\text{m}$ were observed using perpendicular incidence. Final modules will feature smaller pixel in this direction.

The observed efficiency of the detector is $(99.82 \pm 0.03)\,\%$ at default voltages using a threshold of 4 LSB. To arrive at this result, an extensive calculation was performed to estimate the number of tracks passing the DEPFET sensor outside of its integration window but surviving all track cuts. In the sensor, hints for charge loss in the pixel edges are visible due to the rather low signal of (17.19 ± 0.03) LSB at a threshold of 4 LSB. The efficiency measurements are comparable to [83], though some cuts were different in the analysis.

Due to the input from measurements performed in the scope of this thesis, several issues were fixed on the prototype ASICs and several fixes were done to increase their performance. The developed power supply control software is used in virtually all lab setups and beam test of the DEPFET collaboration to control primary power supplies. Before the availability of the custom made DEPFET power supply, the software was used to provide control of the multi power supply setups needed for matrix operation. The readout software and data interpreters developed as part of the thesis are used by the collaboration as the de-facto standard and will be used for configuration and data quality monitoring for Belle II. Despite the limitations resulting from the use of prototype ASICs and a prototype matrix, the obtained results are very promising for the performance of a future Belle II pixel detector.

Appendix

APPENDIX A

DCD Irradiation

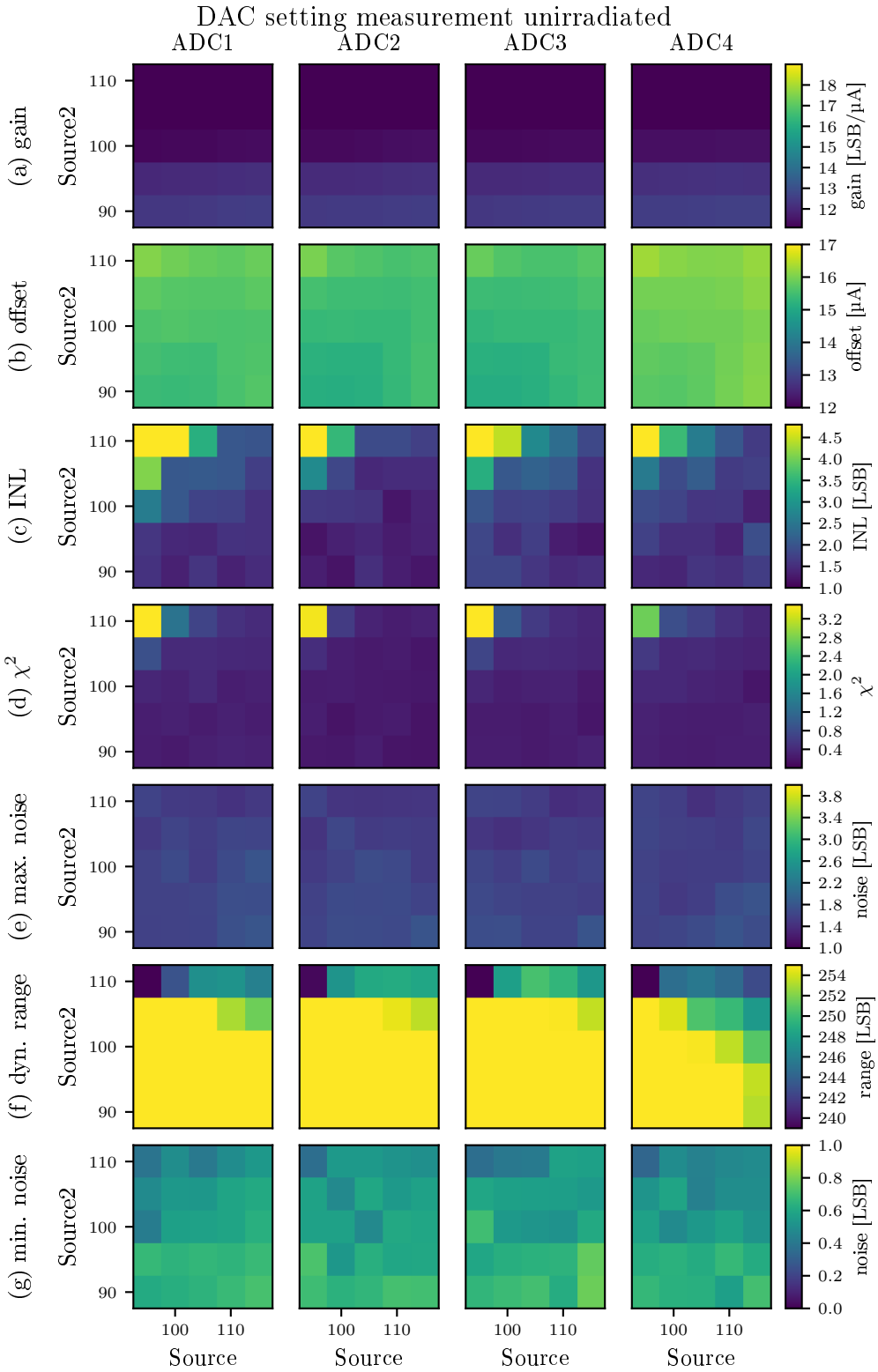


Figure A.1: $\text{Source}_1/\text{Source}_2$ measurement before irradiation using ADC values −110 to 110 LSB.
(a) and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

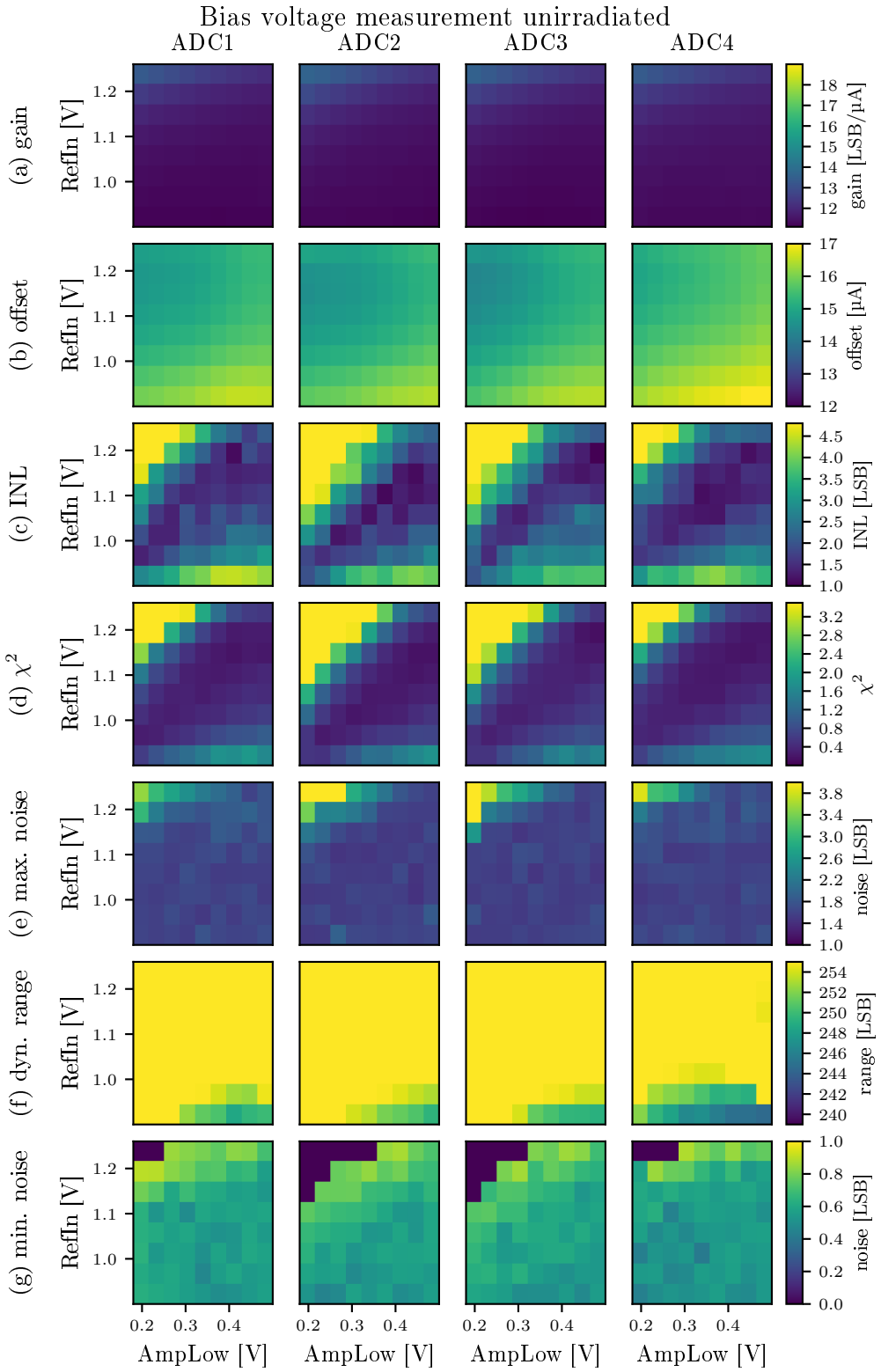


Figure A.2: *RefIn/AmpLow* measurement results before irradiation using ADC values −110 to 110 LSB. *(a)* and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

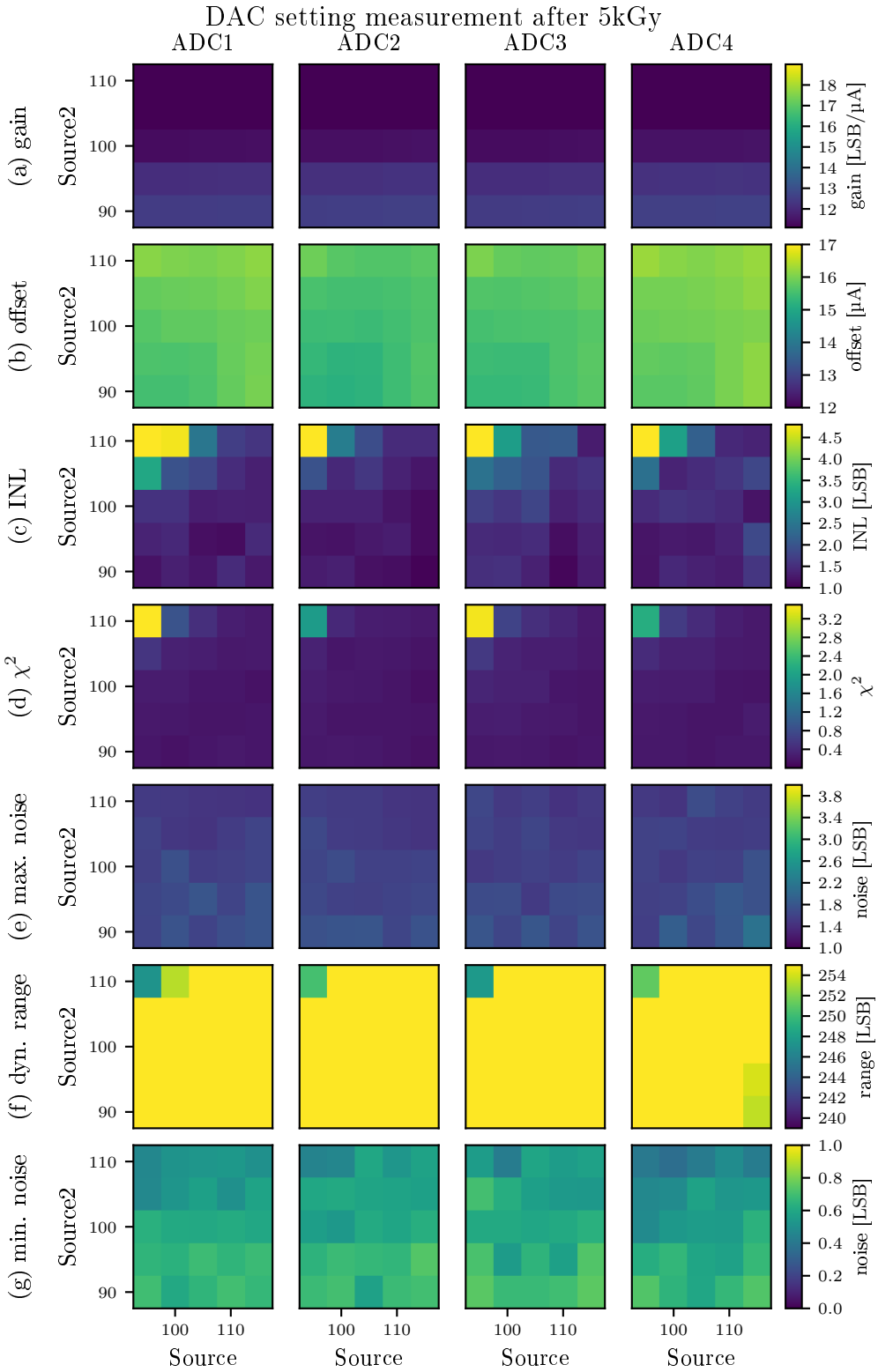


Figure A.3: $\text{Source}_1/\text{Source}_2$ measurement results after 5 kGy using ADC values −110 to 110 LSB.
(a) and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

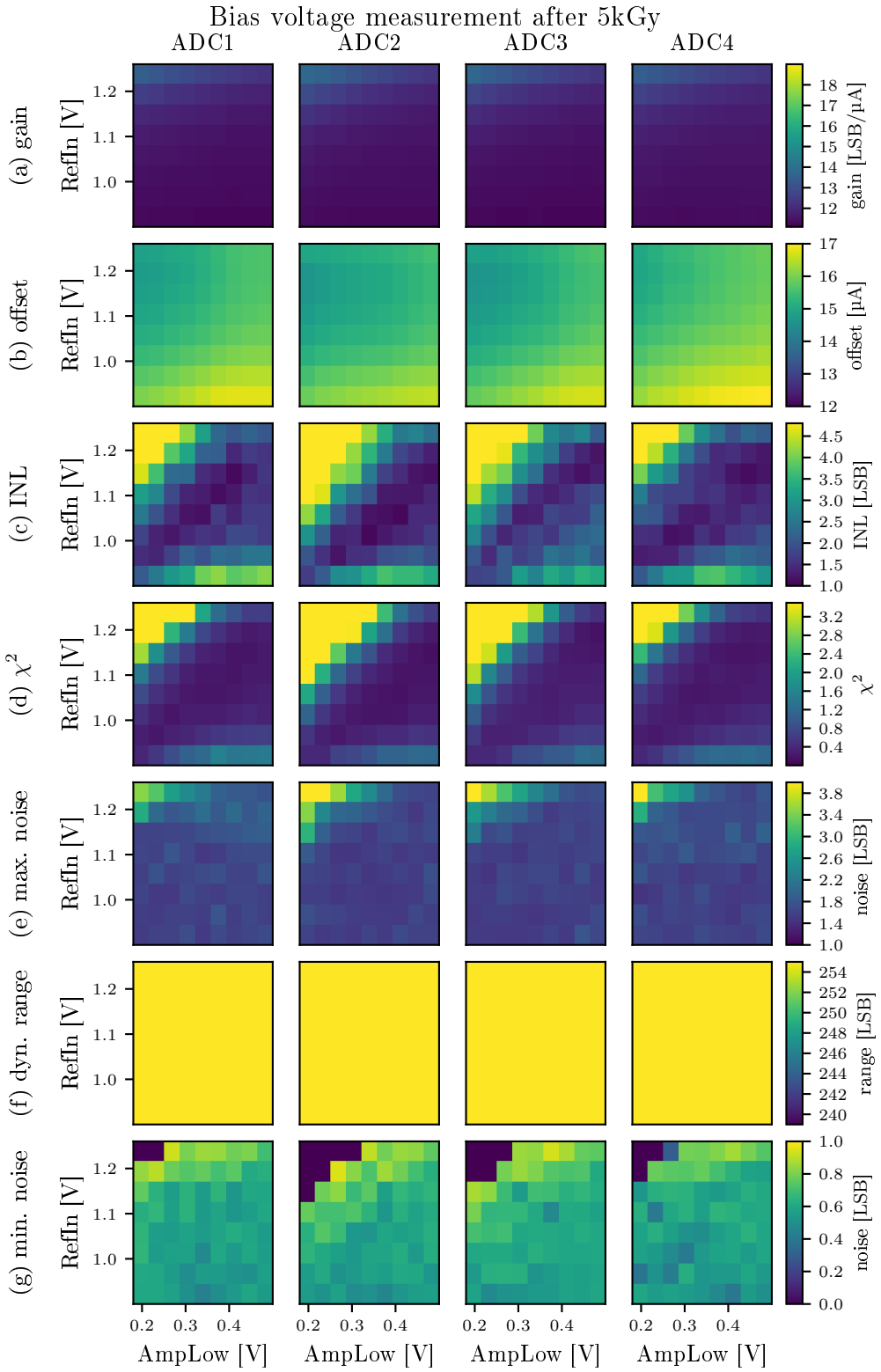


Figure A.4: *RefIn/AmpLow* measurement results after 5 kGy using ADC values −110 to 110 LSB.
(a) and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

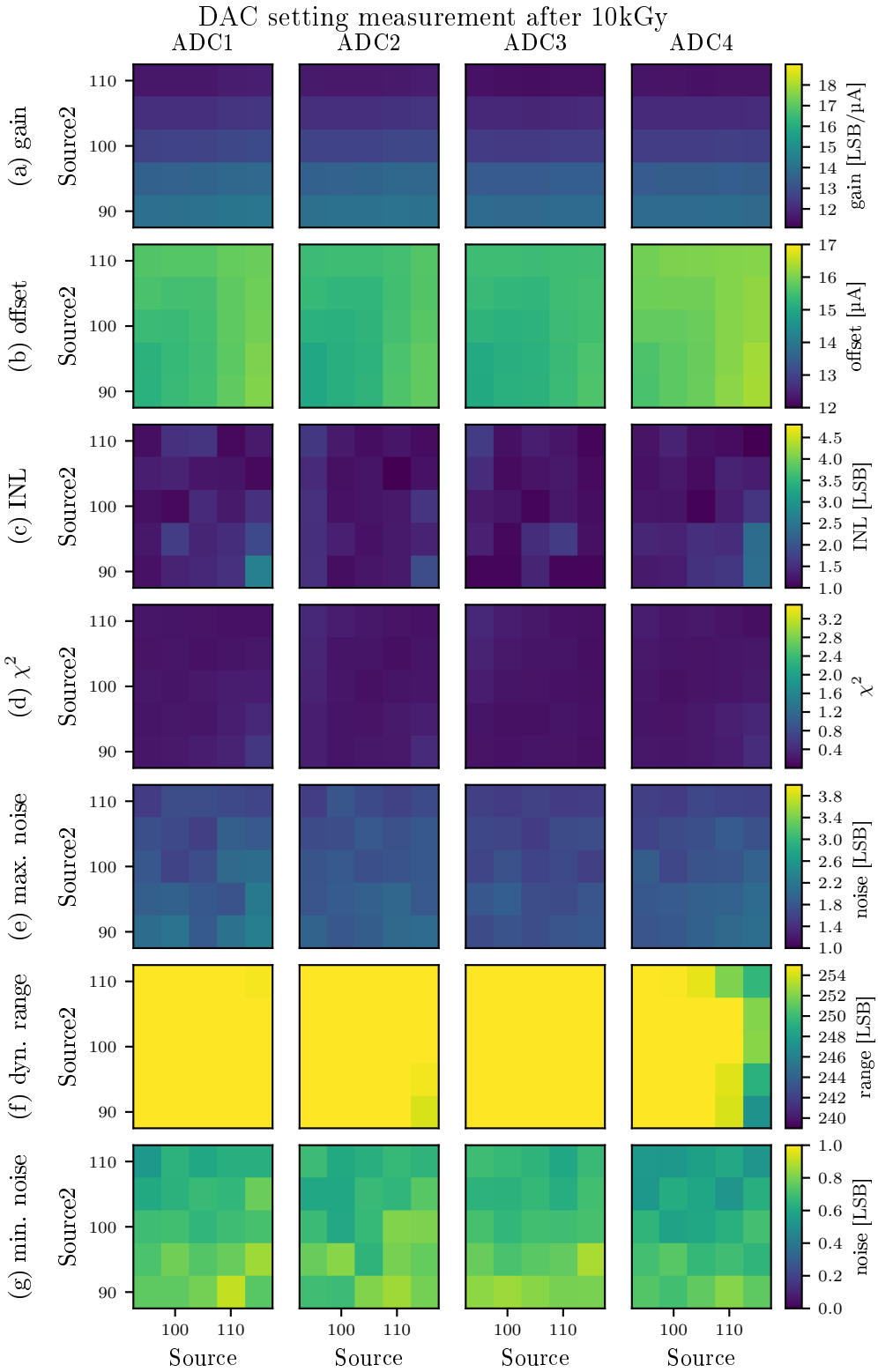


Figure A.5: $\text{Source}_1/\text{Source}_2$ measurement results after 10 kGy using ADC values −110 to 110 LSB.
(a) and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

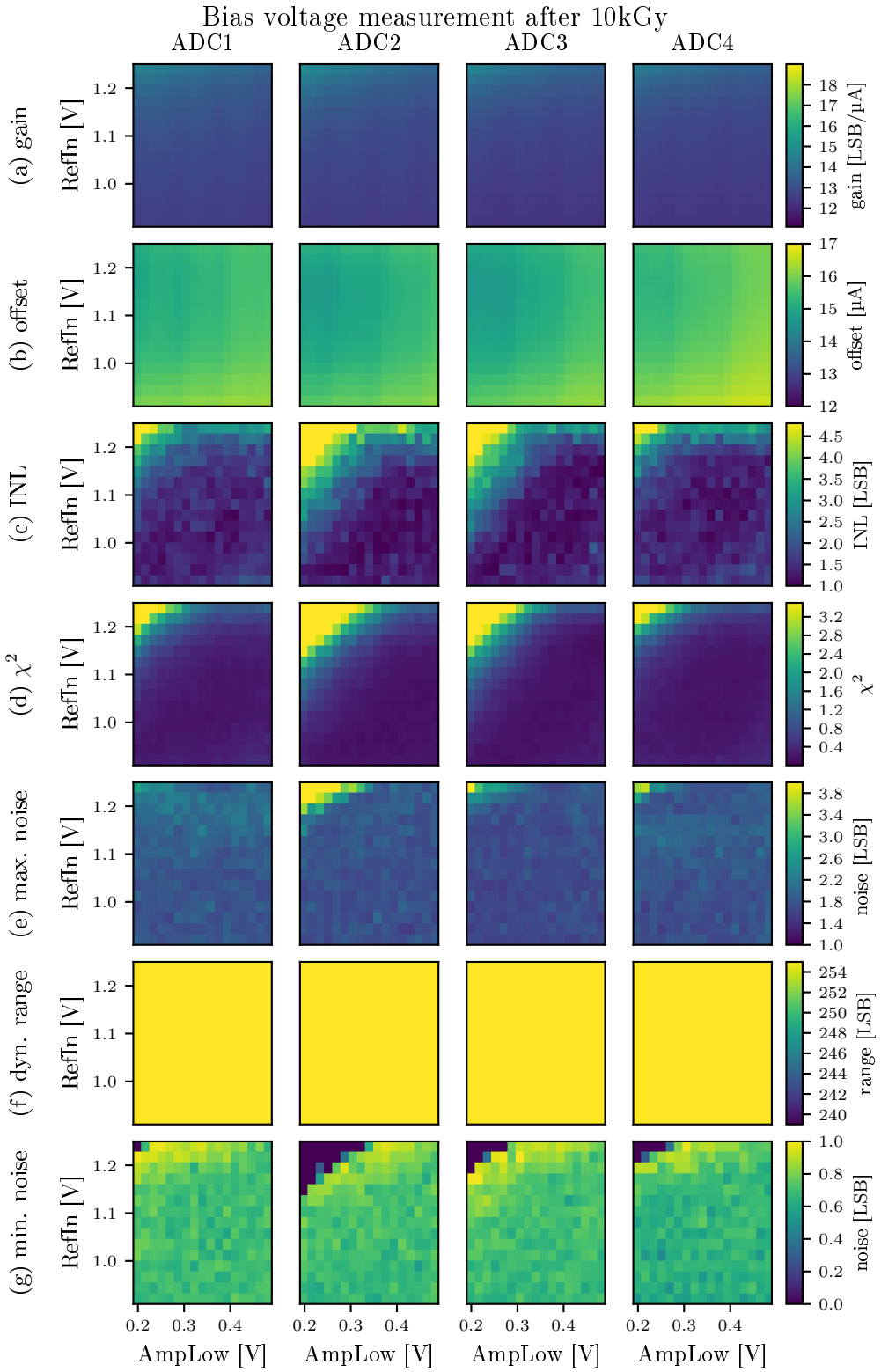


Figure A.6: *RefIn/AmpLow* measurement results after 10 kGy using ADC values −110 to 110 LSB.
(a) and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

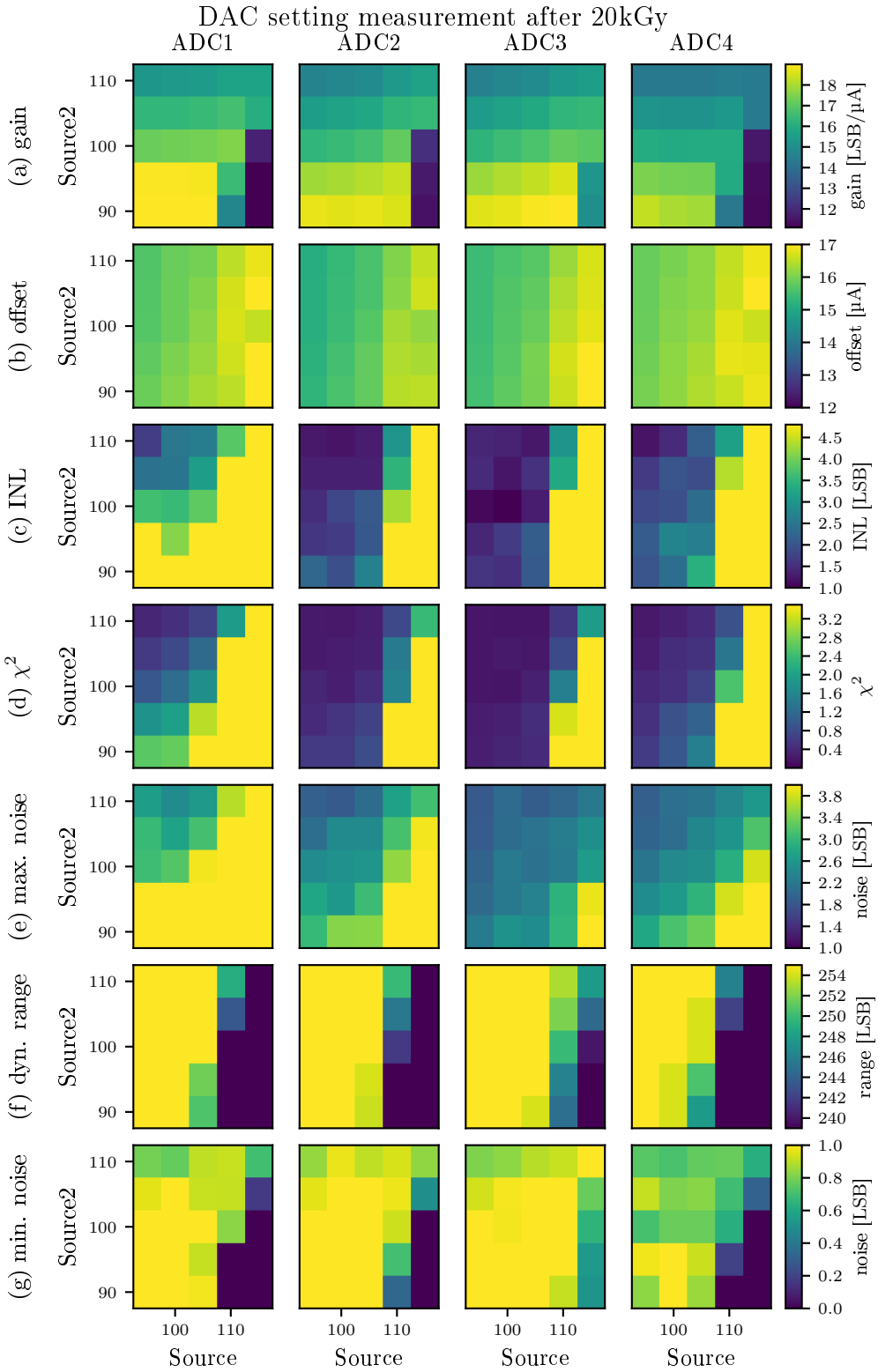


Figure A.7: $\text{Source}_1/\text{Source}_2$ measurement results after 20 kGy using ADC values −110 to 110 LSB.
(a) and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

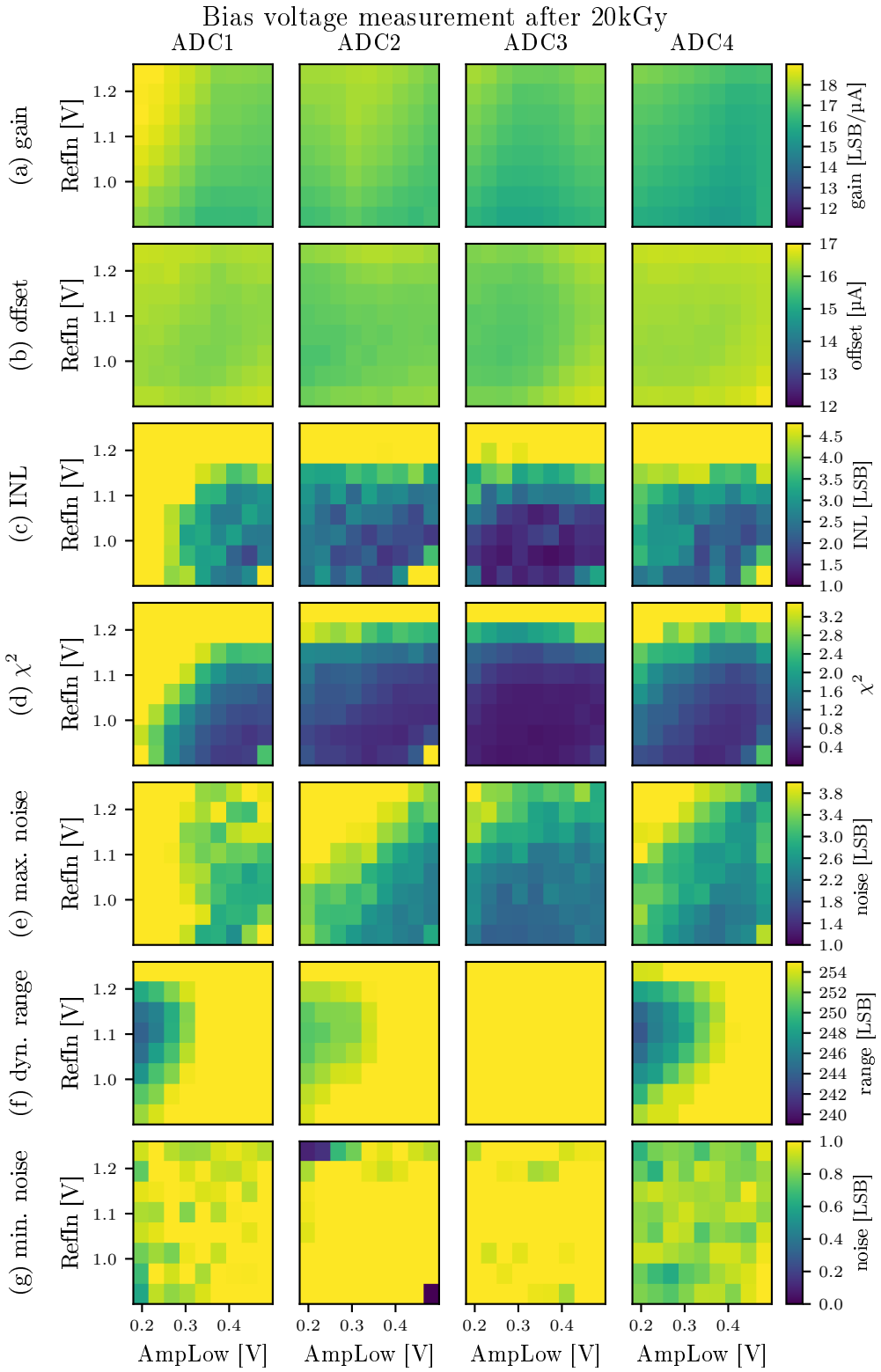


Figure A.8: *RefIn/AmpLow* measurement after 20 kGy using ADC values −110 to 110 LSB.
(a) and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

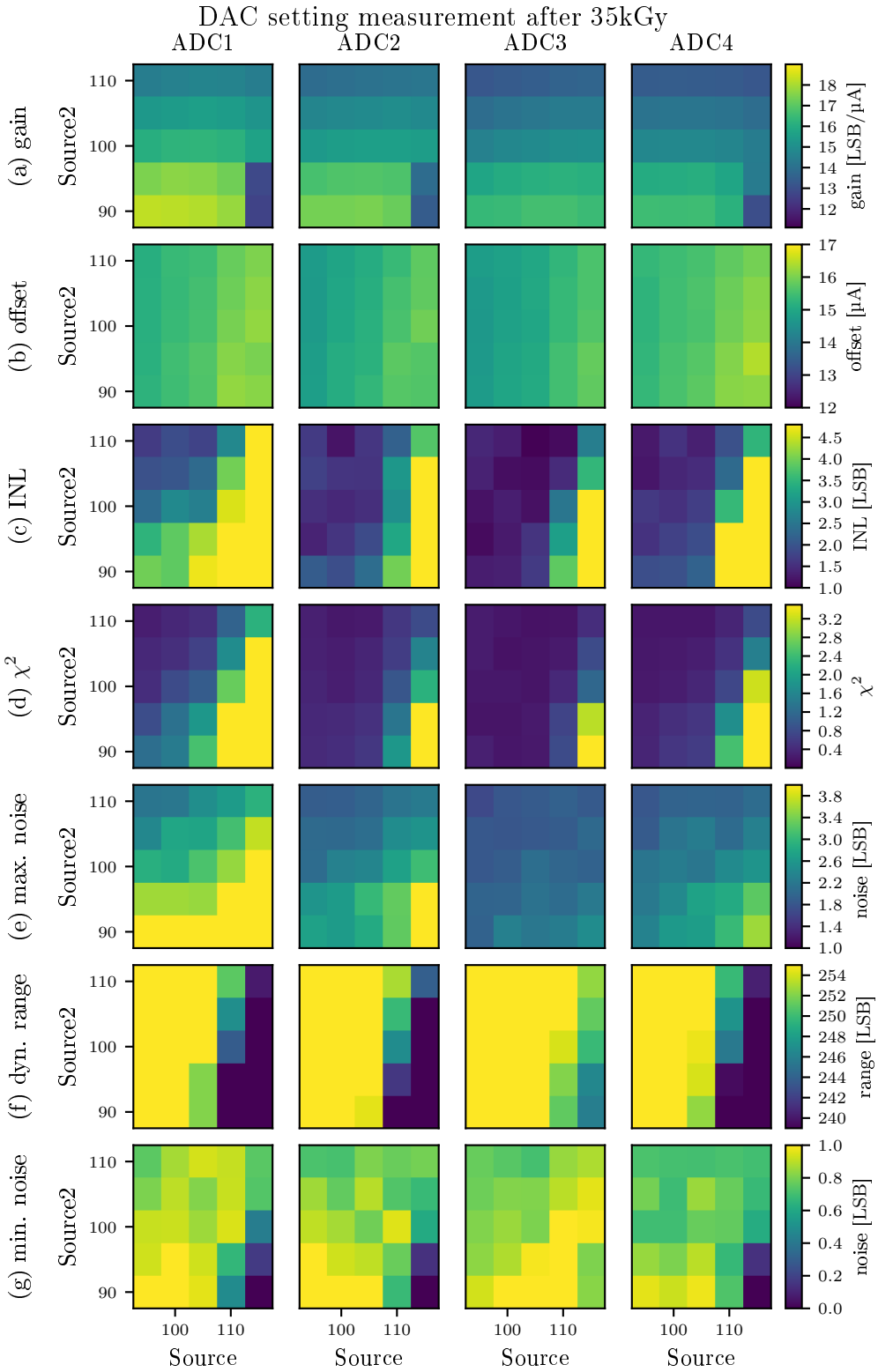


Figure A.9: $\text{Source}_1/\text{Source}_2$ measurement results after 35 kGy using ADC values −110 to 110 LSB.
(a) and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

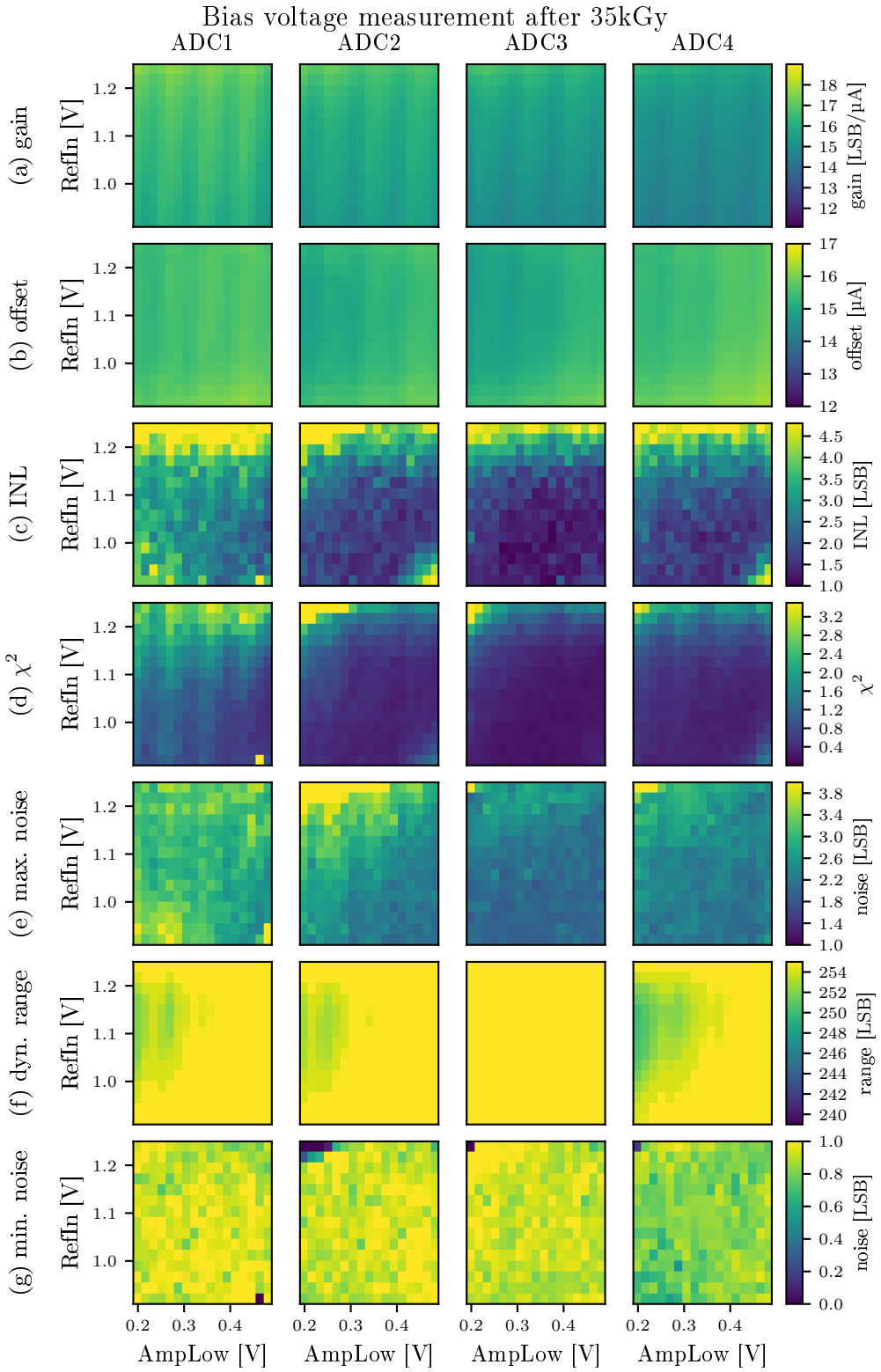


Figure A.10: *RefIn/AmpLow* measurement results after 35 kGy using ADC values −110 to 110 LSB.
(a) and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

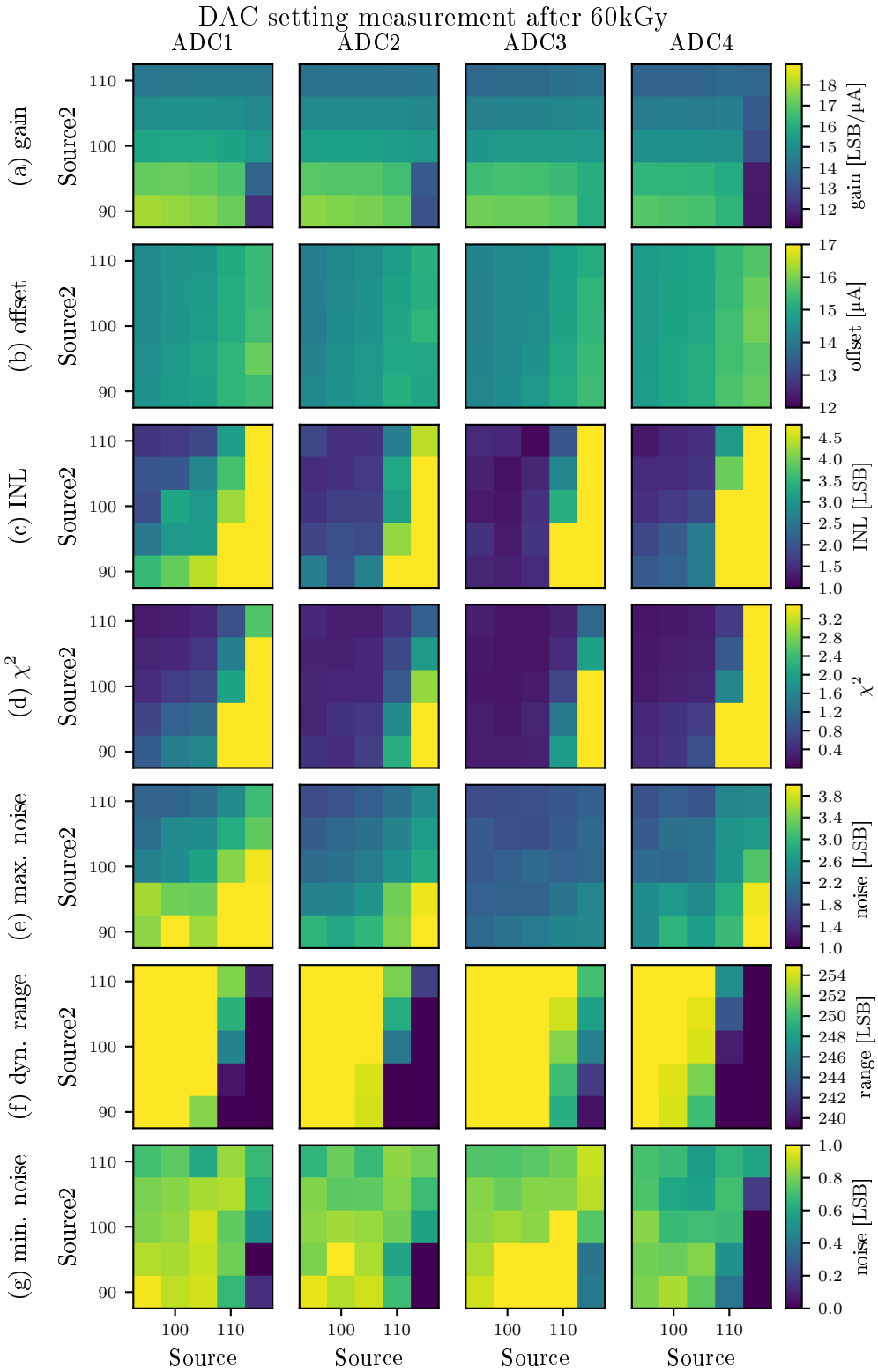


Figure A.11: $Source_1$/$Source_2$ measurement results after 60 kGyusing ADC values −110 to 110 LSB. *(a)* and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

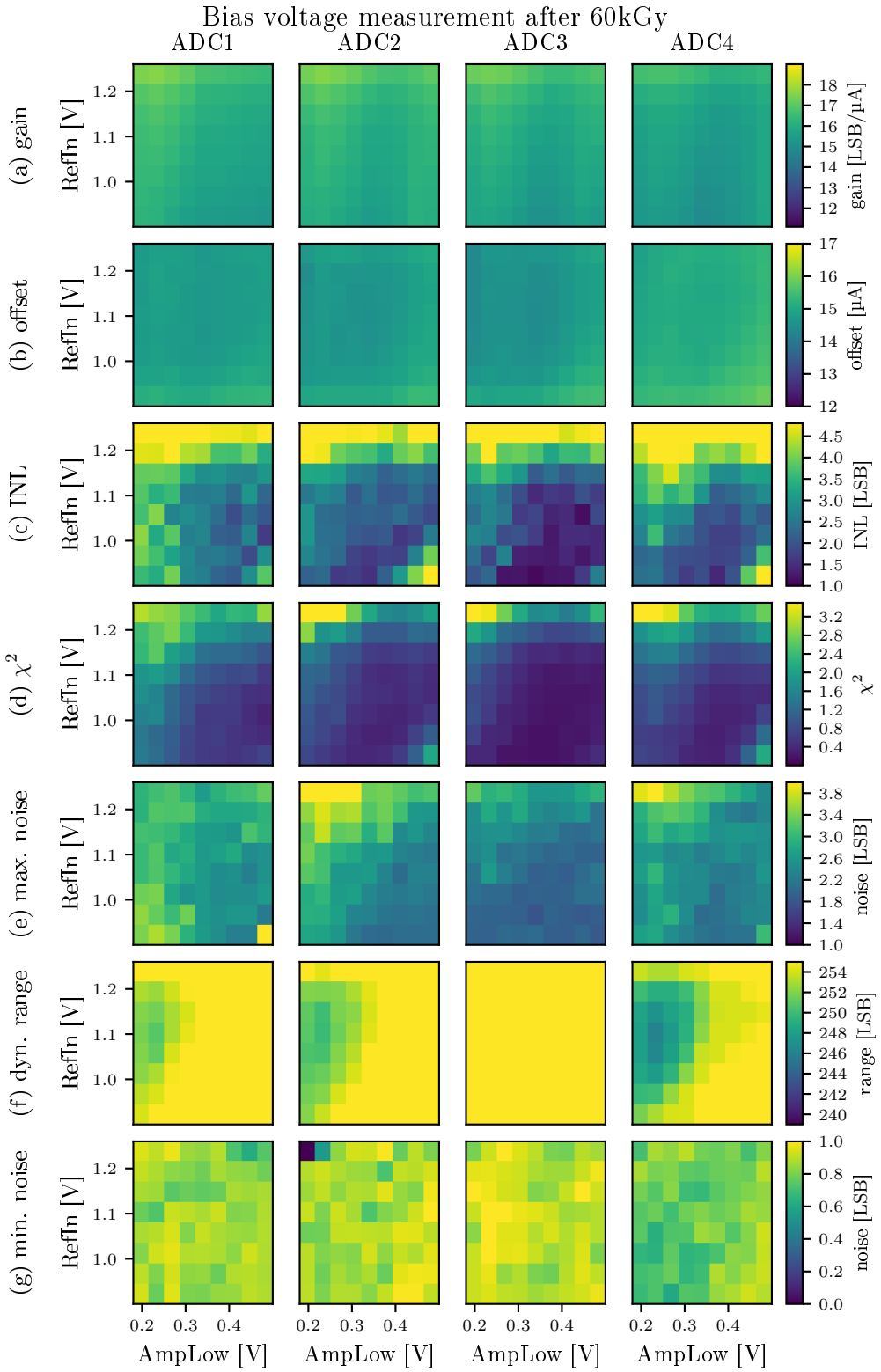


Figure A.12: *RefIn/AmpLow* measurement results after 60 kGy using ADC values −110 to 110 LSB.
(a) and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

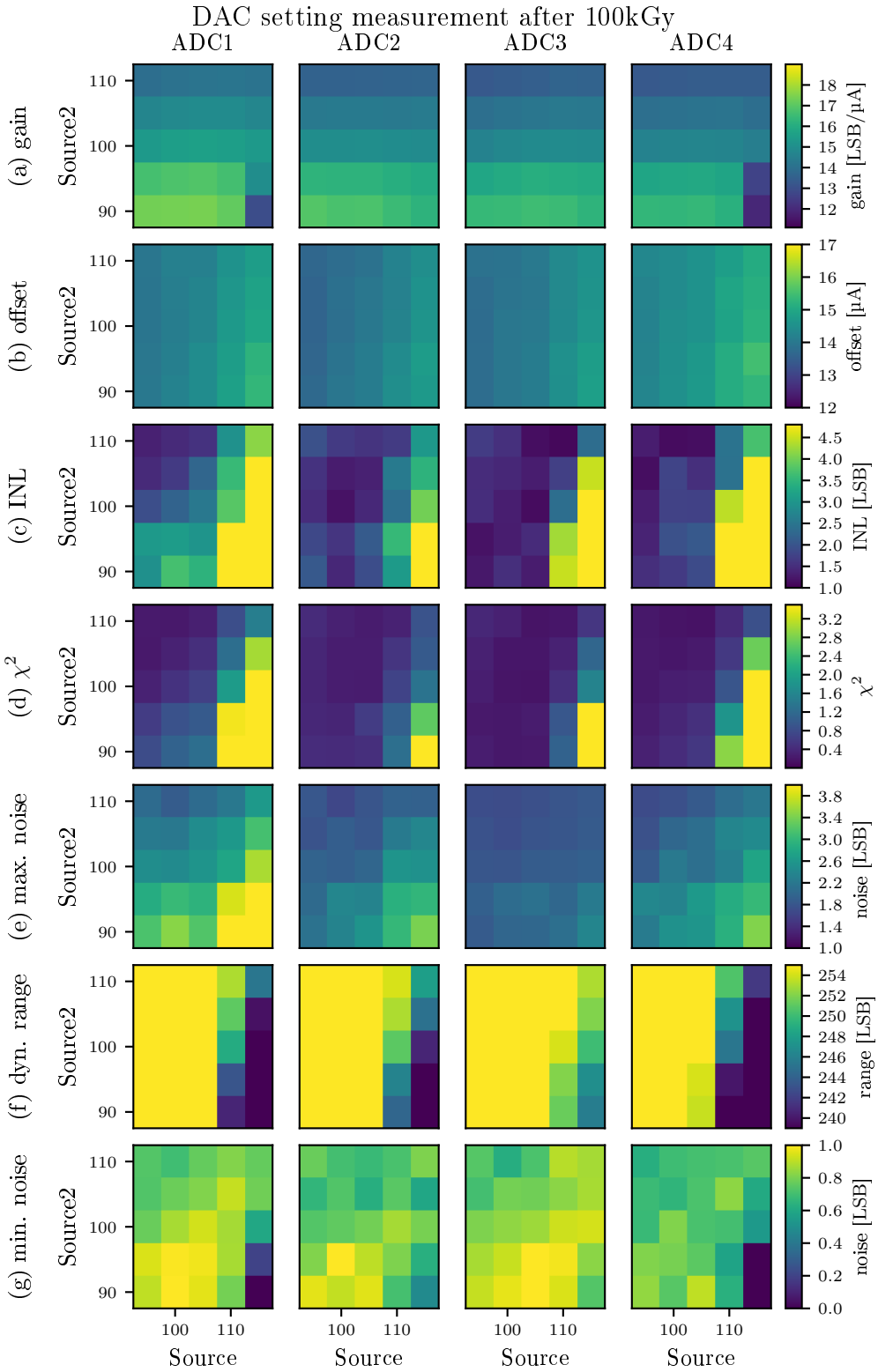


Figure A.13: $\text{Source}_1/\text{Source}_2$ measurement results after 100 kGy using ADC values −110 to 110 LSB. *(a)* and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

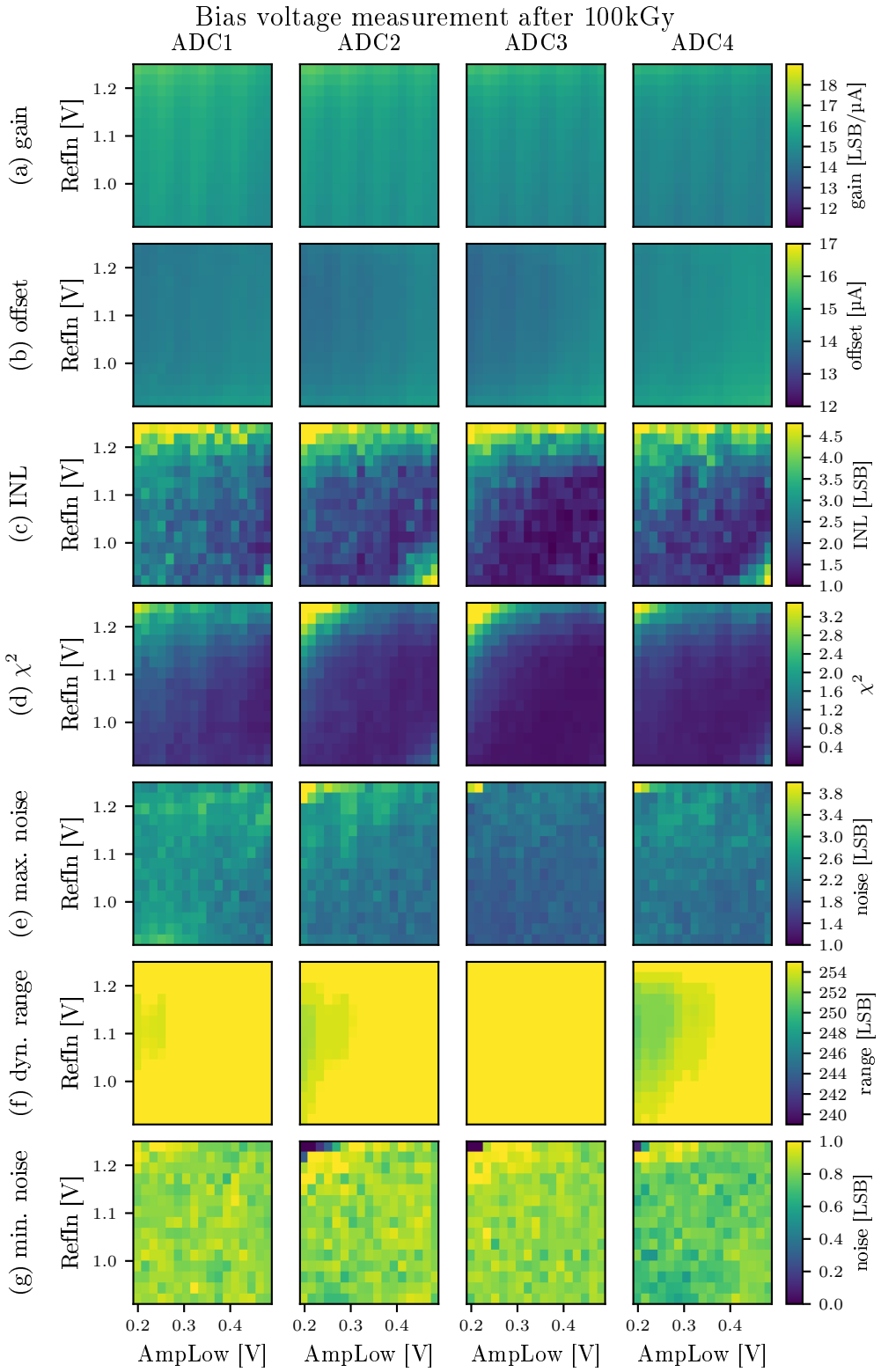


Figure A.14: *RefIn/AmpLow* measurement results after 100 kGy using ADC values −110 to 110 LSB.
(a) and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

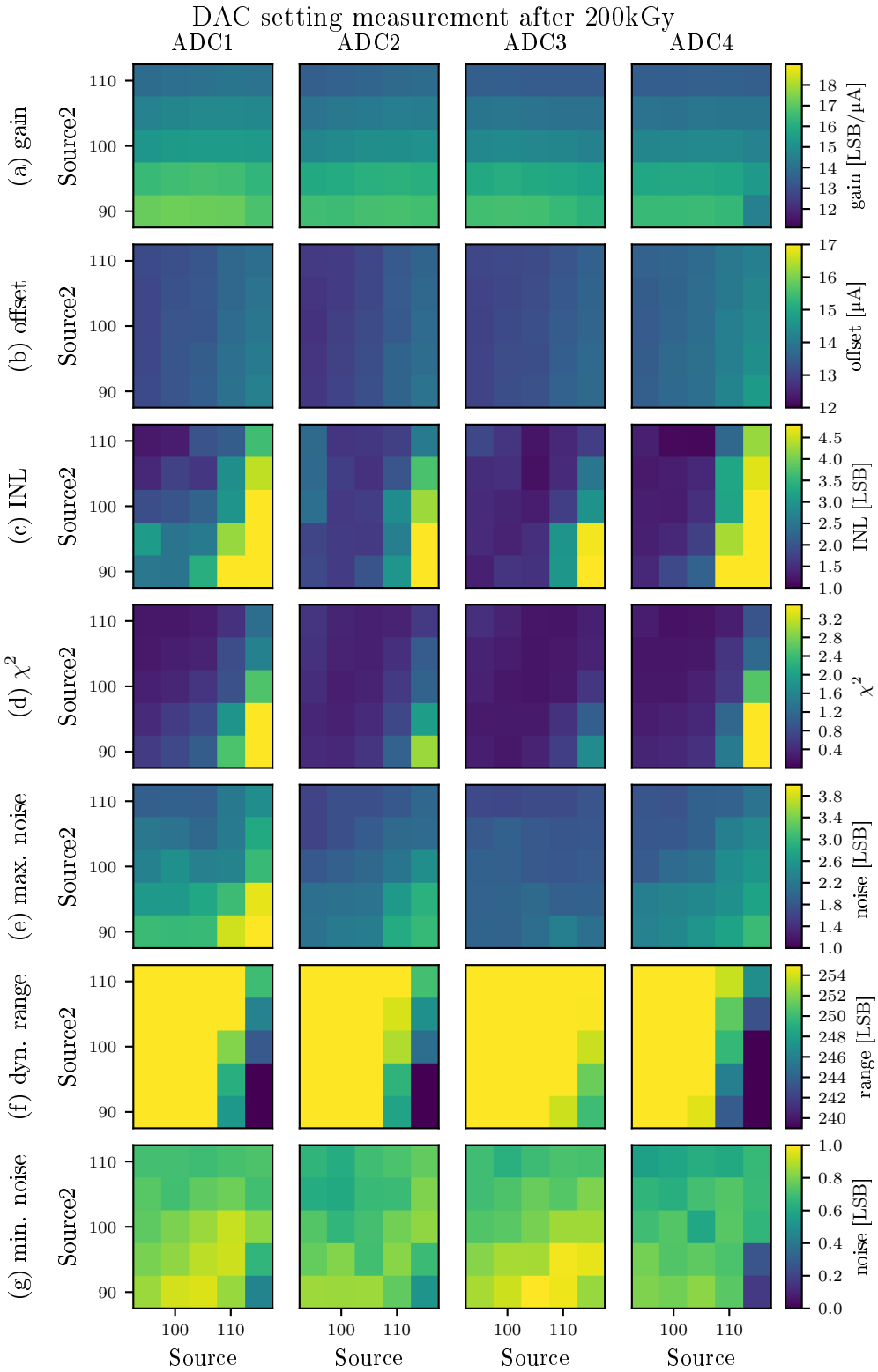


Figure A.15: $Source_1$/$Source_2$ measurement results after 200 kGy using ADC values −110 to 110 LSB. *(a)* and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

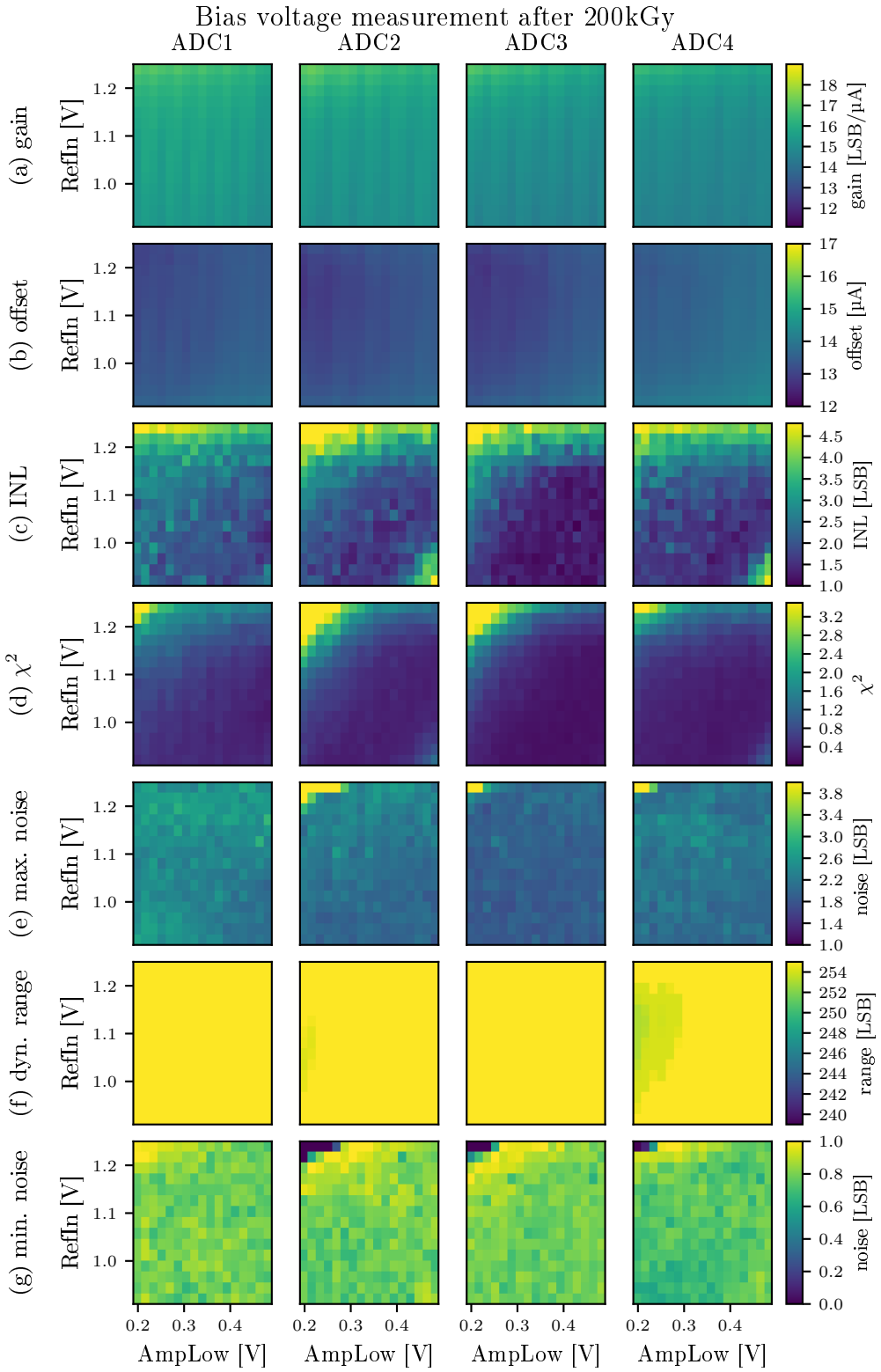


Figure A.16: *RefIn/AmpLow* measurement results after 200 kGy using ADC values −110 to 110 LSB.
(a) and *(b)*: Gain and offset. *(c)* and *(d)* INL and χ^2. *(e)* Maximum noise, *(f)* Dynamic range *(g)* minimum noise

APPENDIX B

Hybrid 5

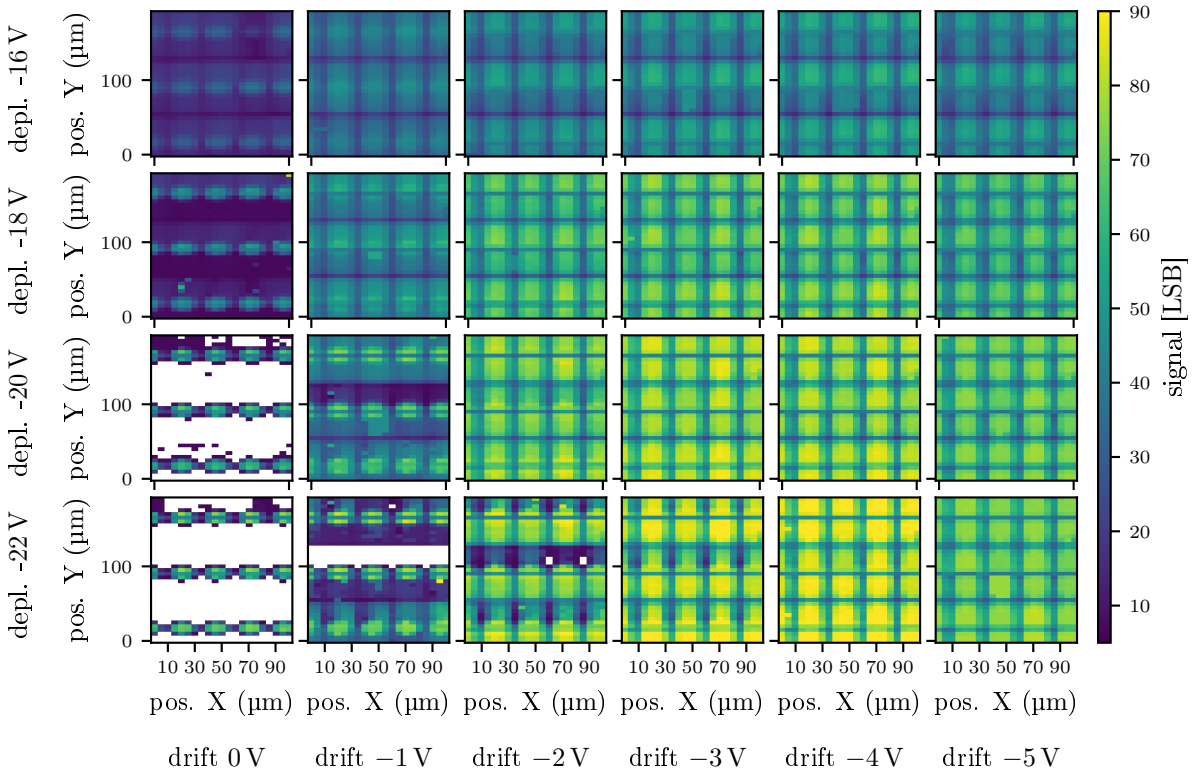


Figure B.1: Laser measurement results on Hybrid 5 showing the seed signal against the laser injection position for different *drift* and *depletion* potentials.

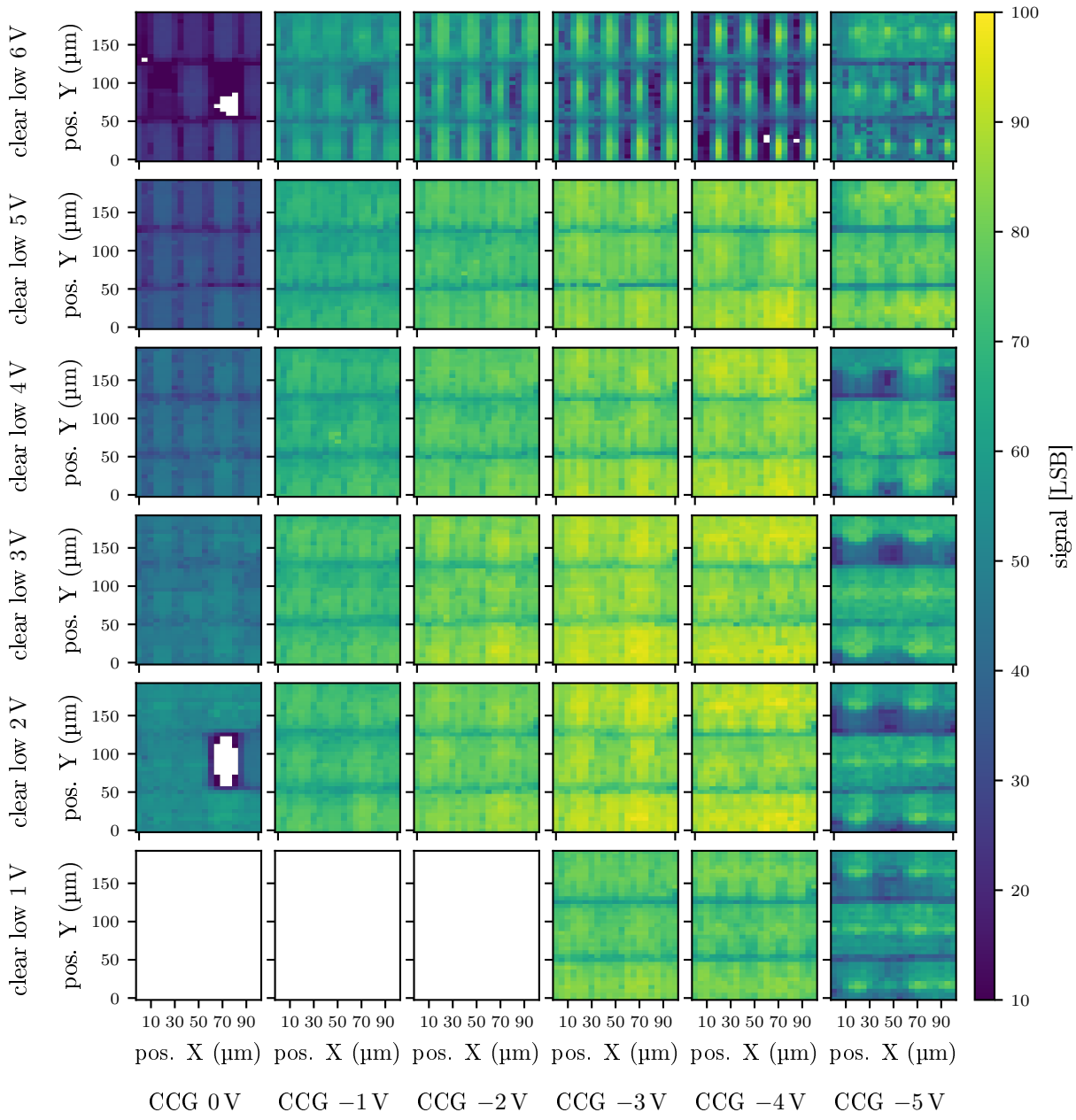


Figure B.2: Laser measurement results on Hybrid 5 showing the cluster signal against the laser injection position for different *cleargate* and *clear low* potentials. These measuremnt data are used to determine figure7.7.

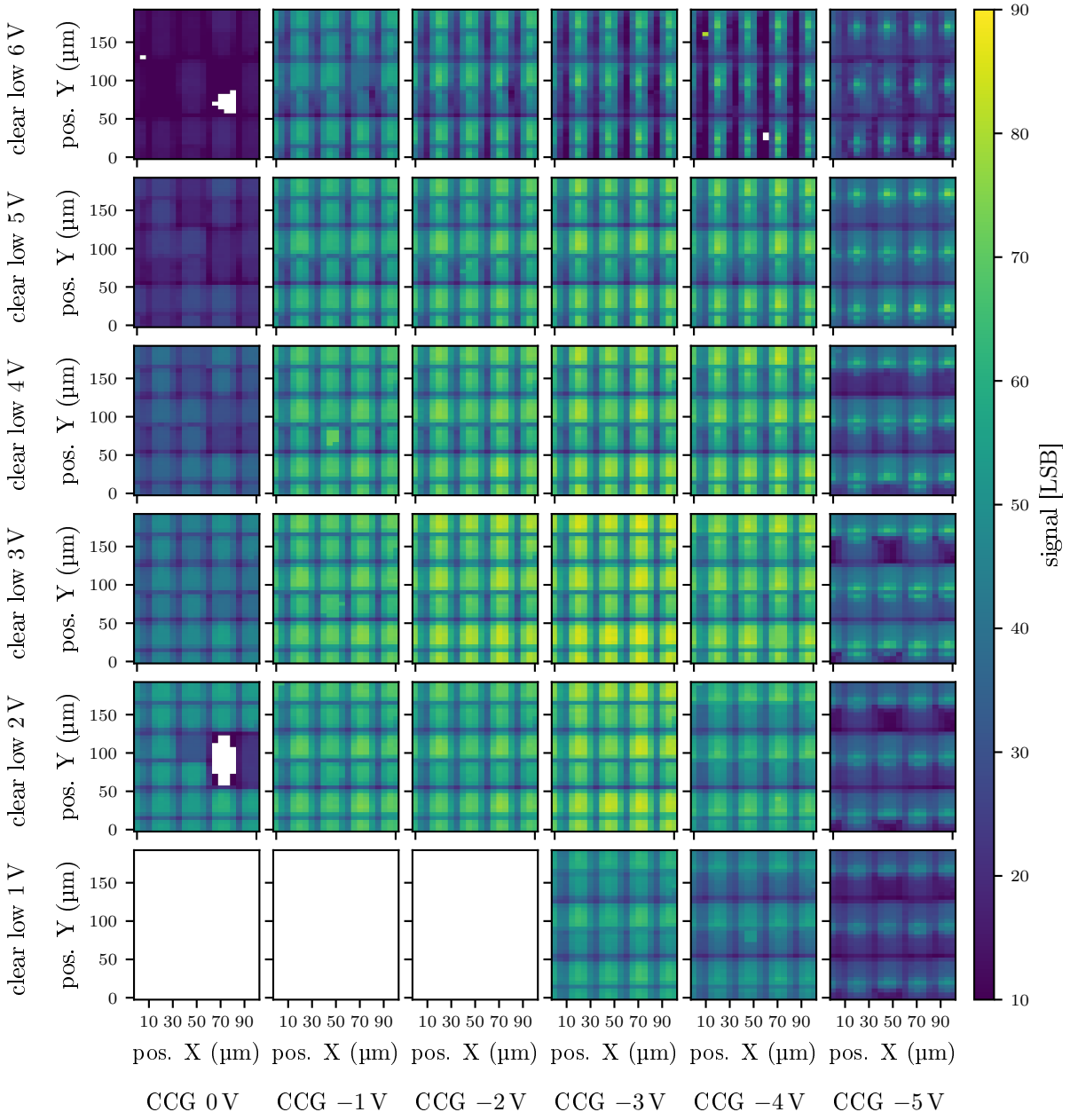


Figure B.3: Laser measurement results on Hybrid 5 showing the seed signal against the laser injection position for different *cleargate* and *clear low* potentials.

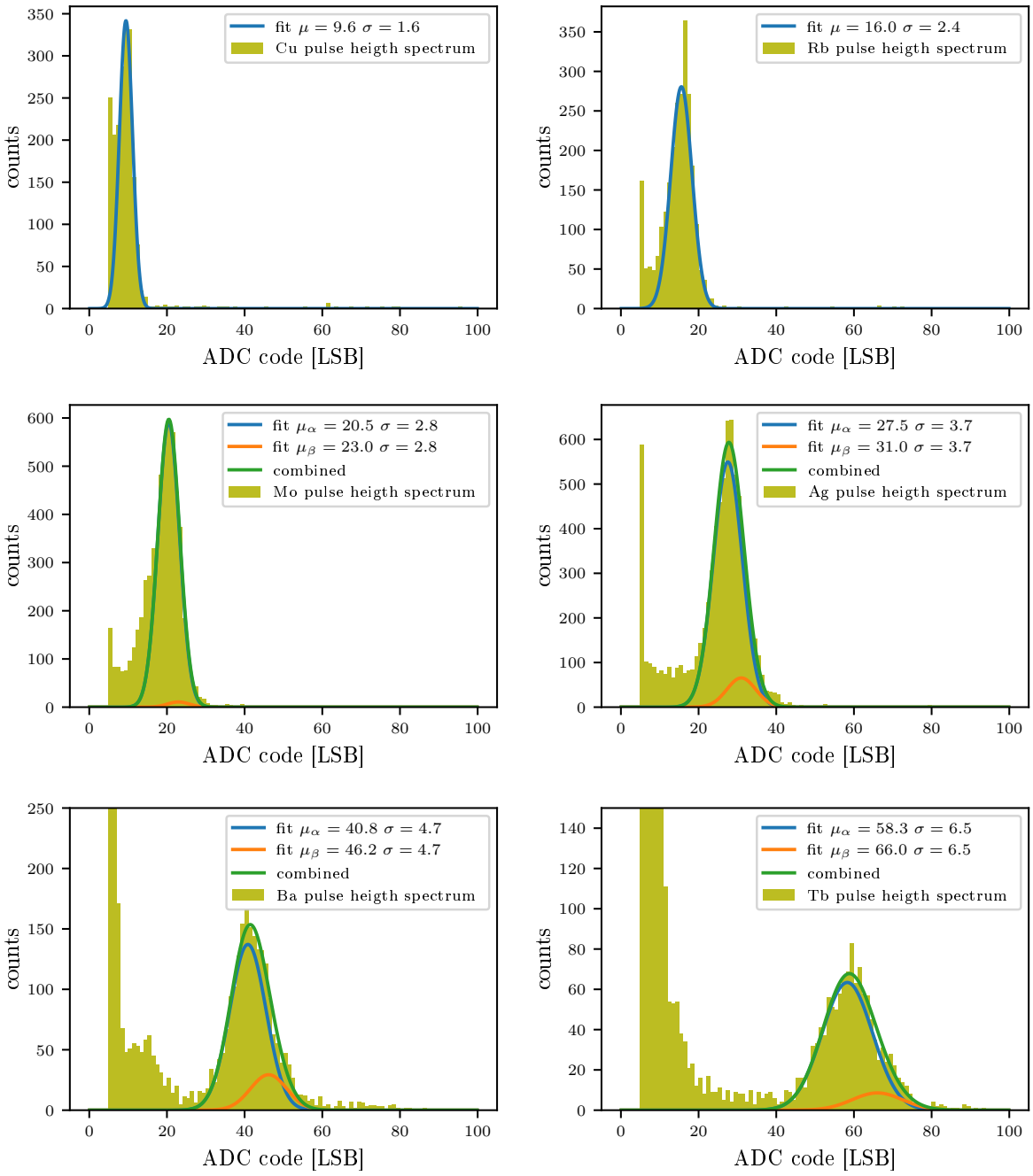


Figure B.4: Measurement results for different K_α and K_β lines from an variable X-ray source with exit windows made of Cu, Rb, Mo, Ag, Ba and Tb. Corresponding Energies can be found in table B.1. For Cu and Rb a single Gaussian distribution was used, for the other elements two overlapping Gaussian functions were used, where both distributions have the same width σ and the peak position of the K_β peak is set to $\mu_\beta = {}^{K_\beta}/_{K_\alpha}\mu_\alpha$. The position of the K_β peak can't for energy linearity (since its position is determined assuming a linear response), but the σ given by this fit is not artificially broadened. The height ratio ${}^{I(K_\beta)}/_{I(K_\beta)}$ of both peaks after the fit is between 12 % and 21 % for Ba, Ag, Tb, which is in the order of the expected 11 to 18 % [94]. For the Mo spectrum K_α and K_β lines are too close to be distinguished, thus the second peak is very small.

Source	E_{K_α}	E_{K_β}	E_γ
Cu	8.05 keV	8.9 keV	-
Rb	13.39 keV	14.96 keV	-
Mo	17.47 keV	19.6 keV	-
Ag	24.94 keV	24.16 keV	-
Ba	32.2 keV	36.38 keV	-
Tb	44.5 keV	50.4 keV	-
^{241}Am	-	-	59.54 keV

Table B.1: Energies of the used x-ray fluorescence and γ photons.

Width due to variations in column direction (LSB)	Width due to variations in row direction (LSB)	Width due to variations repeating each gate (LSB)	Width due to random variations (LSB)	Total width (LSB)
74	106	0	315	387
223	53	0	200	380
74	106	0	200	290
74	212	0	195	399
74	106	158	187	347
149	212	146	66	433
74	212	130	180	422
149	106	162	196	422
223	196	234	197	600
74	196	261	191	480
74	196	130	198	417
74	98	123	193	330
37	106	90	126	249
74	53	86	127	231
37	53	89	127	202
0	0	118	368	413

Table B.2: Width of the pedestal distributions used for simulations, split by effect. The width is given as the distance between the 99.9 % percentile and the 0.1 % percentile.

APPENDIX C

Hybrid 6

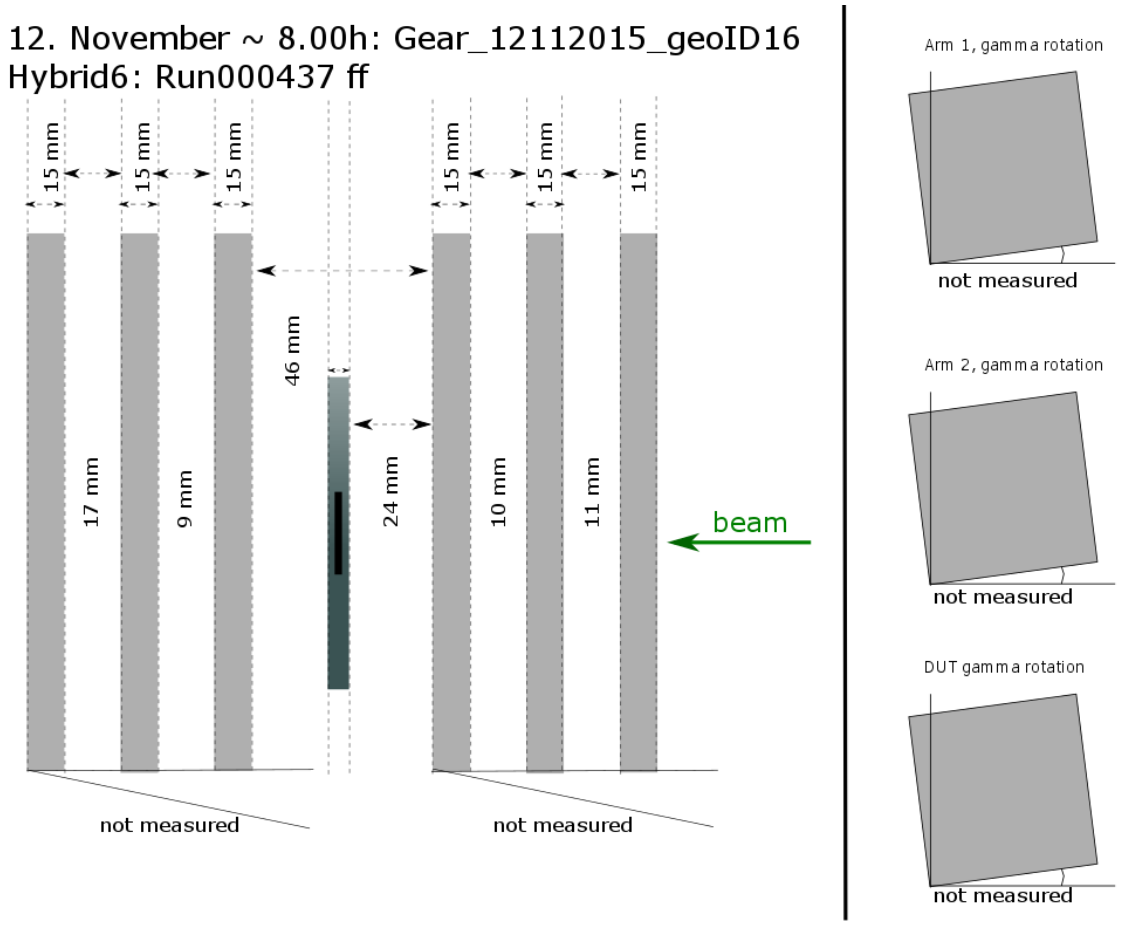


Figure C.1: Sketch of the measurement setup geometry for second part of the testbeam. The setup consists of two telescope arms with three planes each and the DEPFET sensor in the middle. In this setup the telescope planes and the DUT are closer together, resulting in a lower telescope pointing resolution of (3.9 ± 0.4) µm in u and v at the DUT plane.

Name	Voltage	Name	Voltage
DHP IO	1.8 V	*source*	7 V
DHP Core	1.2 V	*bulk*	10 V
DCD DVDD	1.8 V	*clear high*	1.2 V
DCD AVDD	1.9 V	*clear low*	7 V
AmpLow	0.4 V	*cleargate*	0 V
RefIn	1.2 V	*gate-off*	3 V
SW_{sub}	0 V	*gate-on*	−4.3 V
SW_{VDD}	1.8 V	*depletion*	−20 V
SW_{Vref}	1.8 V	*drift*	−3 V

Table C.1: Voltages used for Hybrid 6 with Matrix I00. Deviations from these voltages are explicitly stated

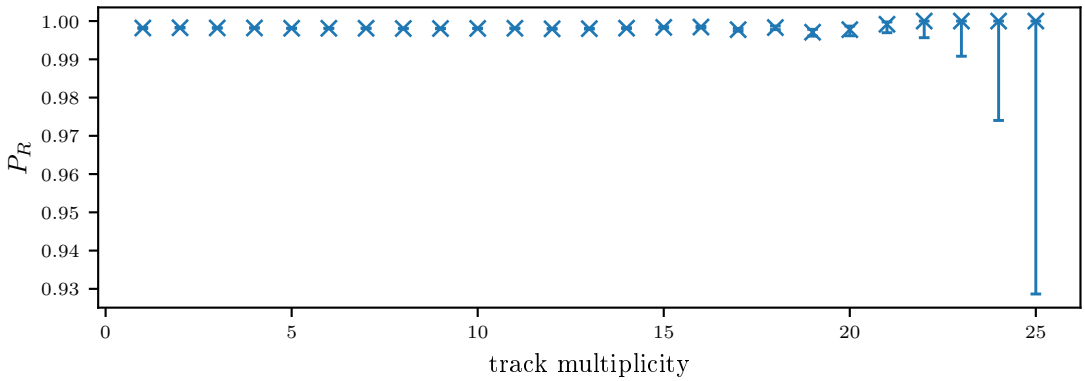


Figure C.2: Probability of a track to survive quality cuts, performed for different track multiplicity of the event. Like expected, the data is in agreement with P_R being constant. The quality cuts need the track to be in a good DEPFET event and to survive the track χ^2 cut. Different to figure 8.36, the track does not need to pass the region of interest cut.

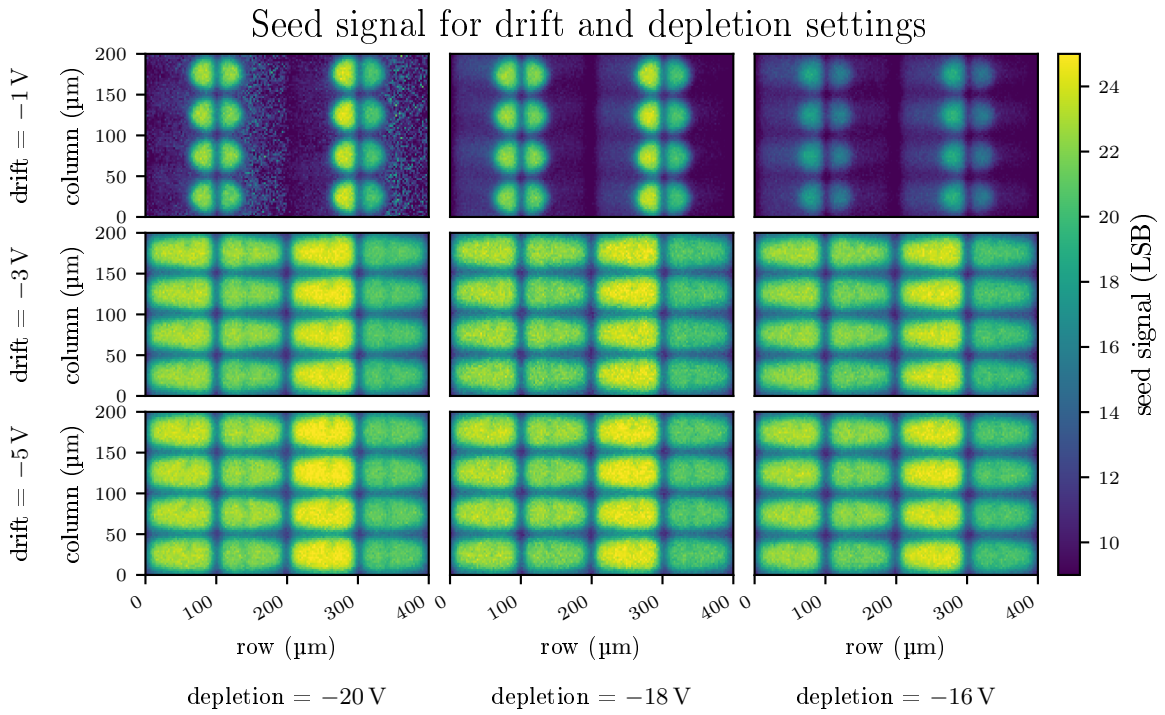


Figure C.3: Beam test results: Seed signal for different *drift* and *depletion* potentials, other voltage at default value.

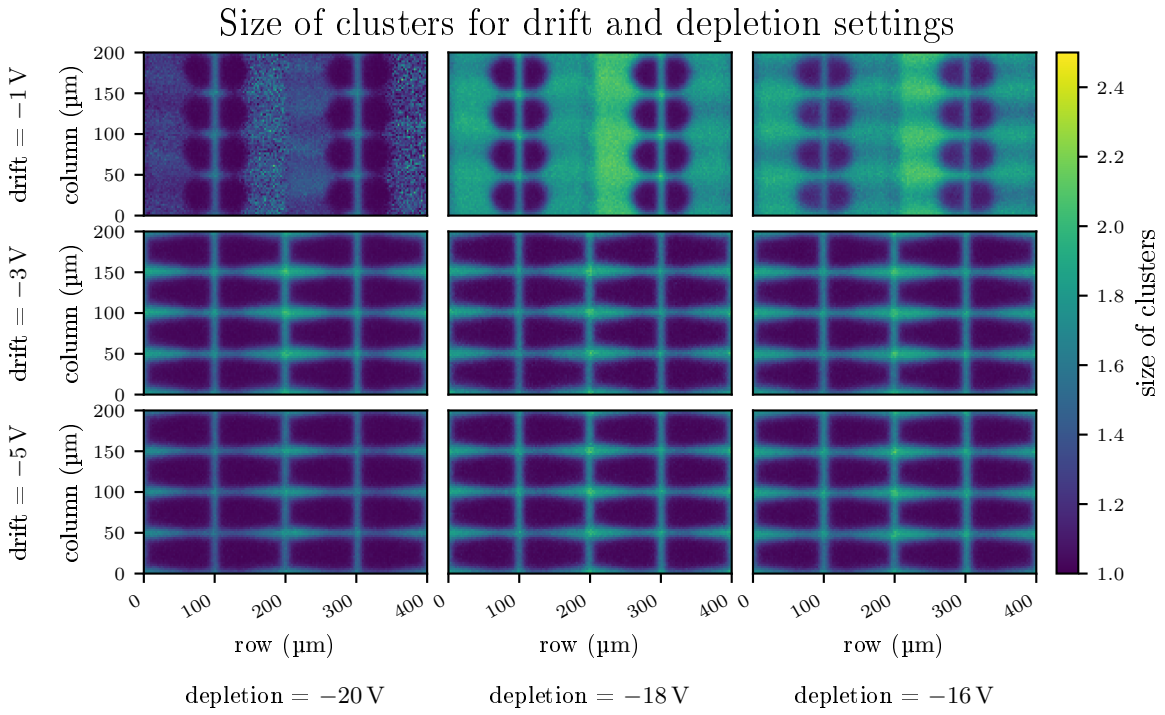


Figure C.4: Beam test results: Cluster size for different *drift* and *depletion* potentials, other voltage at default values

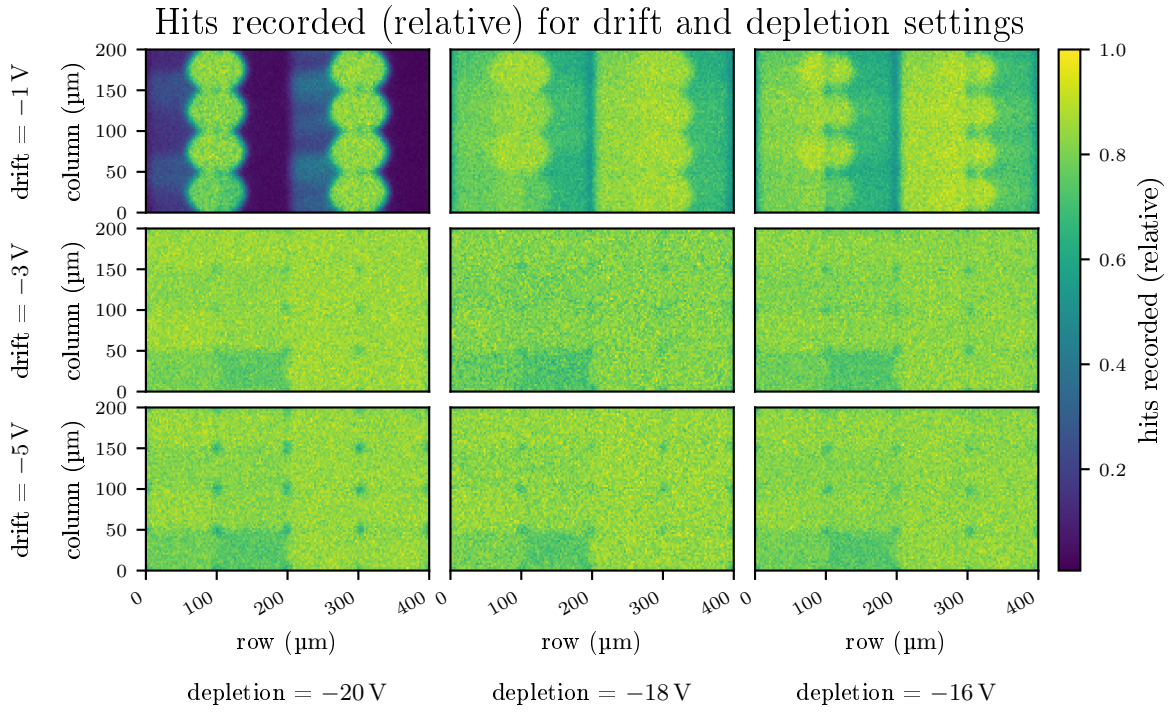


Figure C.5: Beam test results: Recorded hits for different *drift* and *depletion* potentials, other voltage at default values. Inefficiencies can be due to broken drain lines or sensor deficiencies.

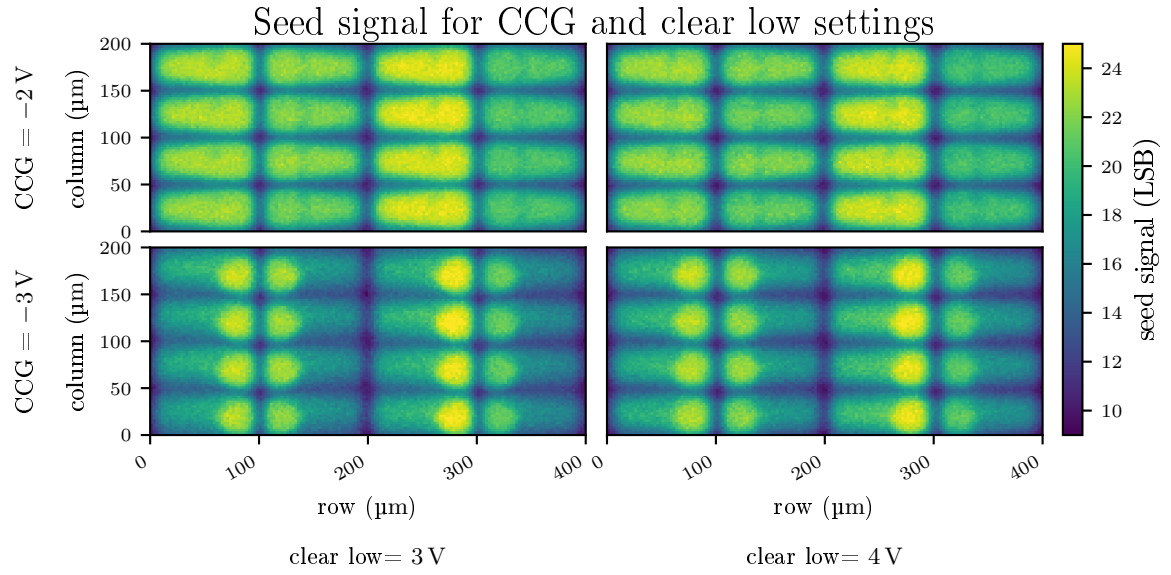


Figure C.6: Beam test results: Seed signal for different *cleargate* and *clear low* potentials, other voltage at default value.

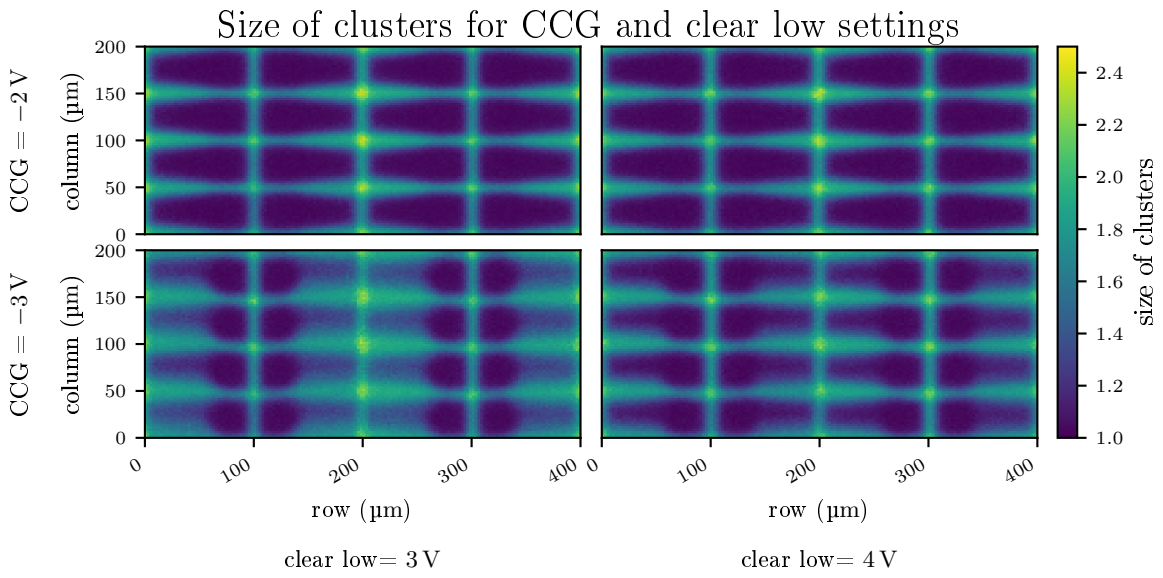


Figure C.7: Beam test results: Cluster size for different *cleargate* and *clear low* potentials, other voltage at default values

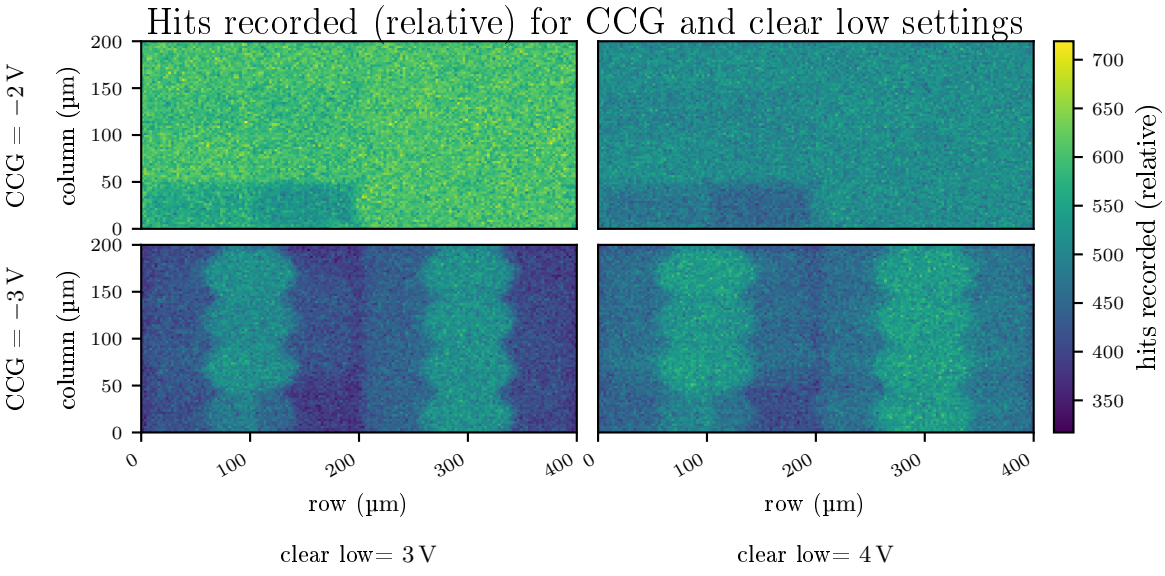


Figure C.8: Beam test results: Recorded hits for different *cleargate* and *clear low* potentials, other voltage at default values. Inefficiencies can be due to broken drain lines or sensor deficiencies.

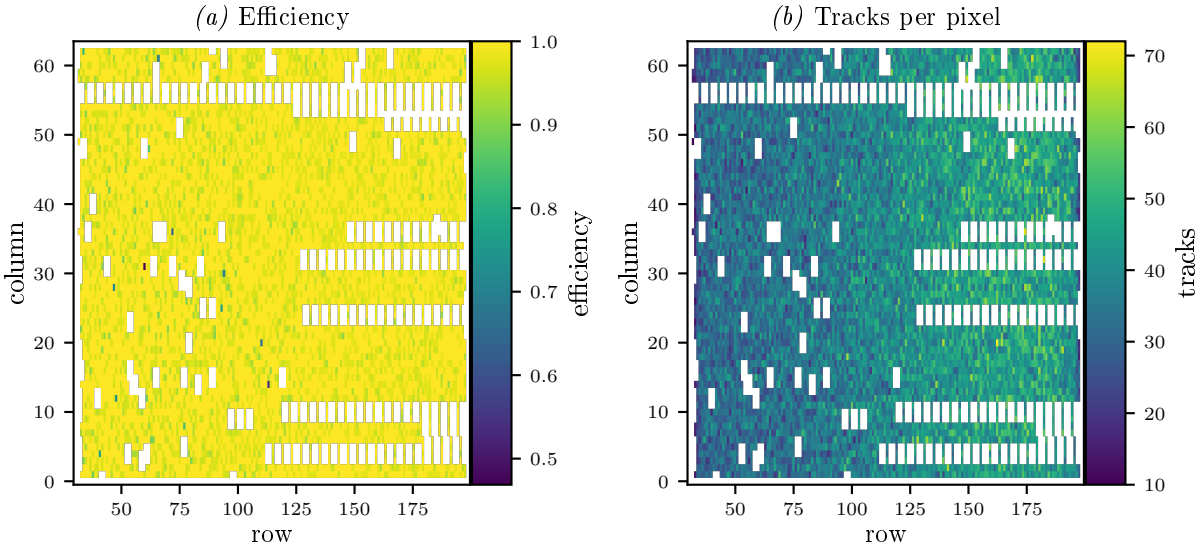


Figure C.9: Hit detection efficiency (without correction) for default bias voltages and threshold 5. In this run, less noisy pixel were observed and pixel which showed a bad efficiency in the lower threshold run (see 8.40) show a good efficiency.

APPENDIX D

Data Formats

BonnDAQ receives data from the DHE or DHC over UDP. An event contains several DHE/DHC frames, beginning with an DHE/DHC start of event frame and ending with a corresponding DHE/DHC end of

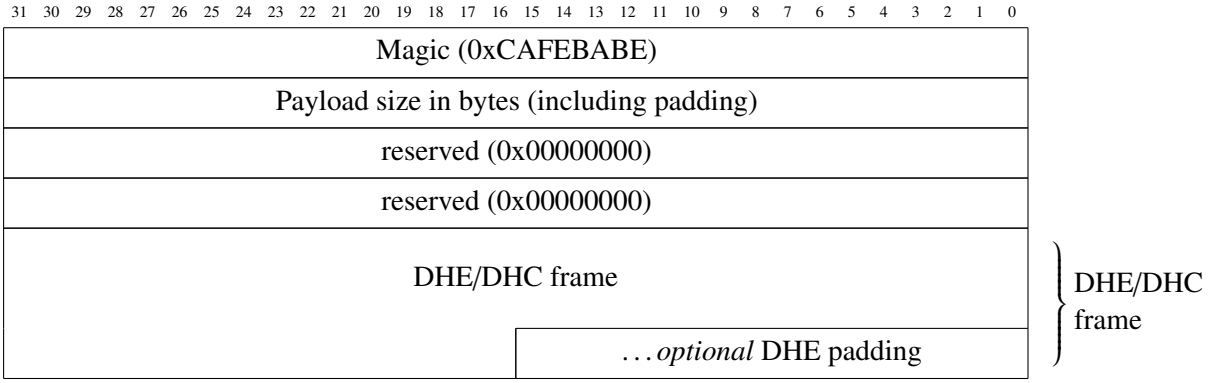


Figure D.1: Single DHE/DHC frame with stream header

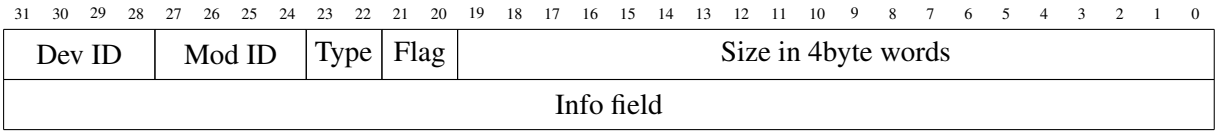


Figure D.2: Format used for BonnDAQ headers

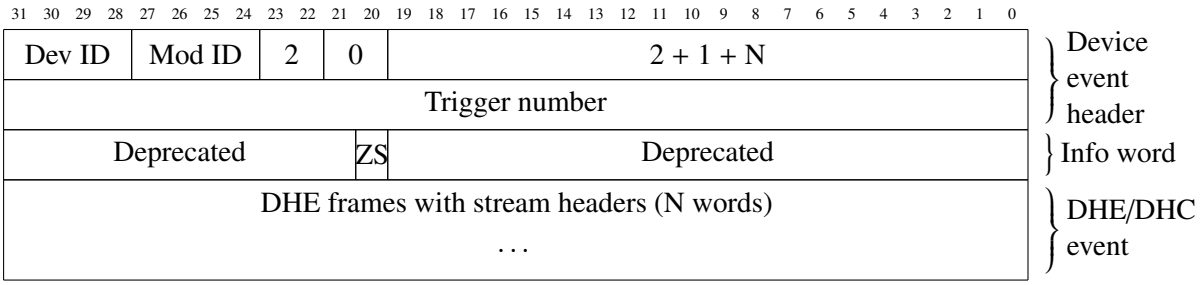


Figure D.3: Device event containing header, info word and payload. The info word contains a ZS field, where 0 denotes raw data and 1 denotes ZS data. This info word is an remanent of older test system like Hybrid 4, Virtex 4 or DHHemulator readout, where multiple of its fields were used.

event frame. DHE/DHC frames can be split over several UDP frames. BonnDAQ collects all frames belonging to a single event and then saves it to a data stream. DHE/DHC frames do not contain their own size, so a 16 byte stream header is added as shown in figure D.1. This format was used by ONSEN in the 2013 beam test and was chosen to be compatible with the tools developed at that time. The payload data of an event contains all DHE/DHC frames with header concatenated.

Figure D.2 shows the header structure used by BonnDAQ. The Dev ID separates different device types. Dev ID 7 is DHE data, Dev ID 8 is DHC data. Two Dev IDs are reserved: 0 (used for group headers) and 14 (used for Info events). 16 ModIDs are used to indicate different modules in the data stream for each device type. The type specifies the frame of the module. Valid types are 0 for begin of run (BOR) events, 1 for end of run (EOR) events and 2 indicating device data. Each module is required to send an BOR before sending device data and to send an EOR before changing its run number. 2 bits for flags are available in the header. The size field is the size of the header and payload in 4 byte words. The Info field contains data specific to the event type.

Event types

- **Run Number event**: Dev ID 0xE, Mod ID 0x1, Type 2 (data), Flag 0, Size 2, Info field: Run Number. Must appear before BOR or between EOR and BOR.
- **BOR event**: Dev ID like the device, Mod ID like the device, Type 0 (BOR), Flag like the device, Size 2, Info field: BOR Trigger 0x55555555
- **EOR event**: Dev ID like the device, Mod ID like the device, Type 1 (EOR), Flag like the device, Size 2, Info field: EOR Trigger 0xAAAAAAAA
- **Device event**: Dev ID , Mod ID , Type 2 (Data), Flag 0, Size 2 + Payload, Info field: Trigger Number.
- **Group event**: Dev ID 0 , Mod ID 0, Type like grouped events, Flag 2, Size 2 + Payload (all events belonging to this group), Info field like grouped events. Appears only in files.
- **File Type event**: Dev ID 0xE , Mod ID 0x2, Type 2 (data), Flag 2 or 3, Size 2, Info field: Number of device events in the file. Appears only in files.

Device events for Dev ID 7 and 8 (DHE and DHC) contain an info word between the header and the DHE/DHC payload like shown in D.3. This word is currently mostly unused. It reports, whether data is zero suppressed (1) or raw (0).

File format Data in files is saved as sequence of 4byte integers, stored as little endian. Multiple modules can be stored in a single file by creating event groups, consisting of a group event header followed by one event per module. All events in the group need to have the same event type and the same info field. The group event header shares this type and info field. The size given in the group header is the size of the group header plus the size of all events in the group. An example for a event group is given in D.4.

A BonnDAQ file starts with a File Type event. The Flag 2 denotes a compressed file, Flag 3 denotes an uncompressed file. The Info field gives the number of device events in the file or 0, if data taking stopped without properly closing BonnDAQ.

A compressed file consists of several data blocks, whose structure is explained in the next paragraph. After decompression, the structure of the data stream in a compressed file is equal to the structure of the data stream

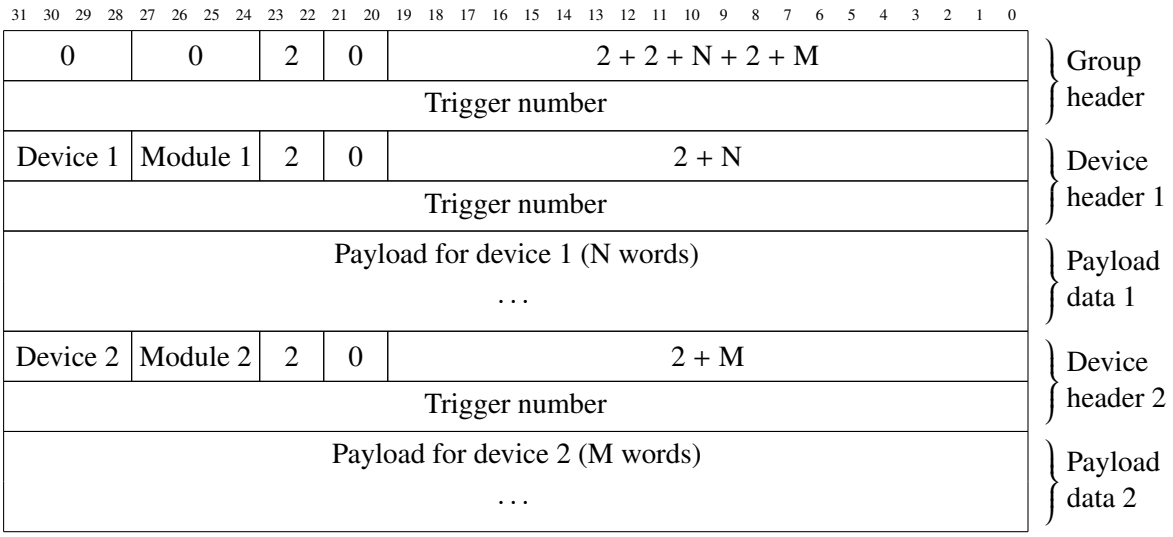


Figure D.4: Group event containing two devices with N and M words of payload data

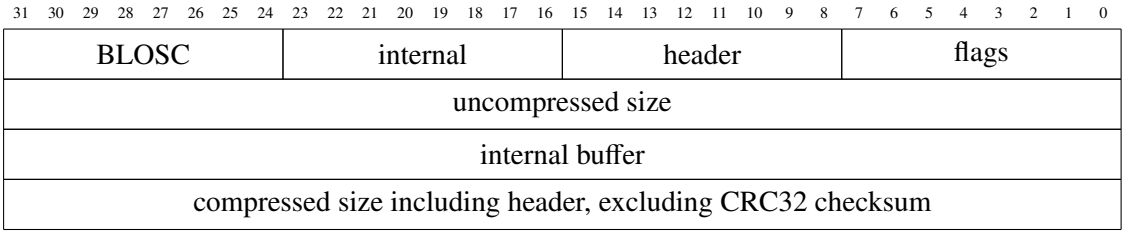


Figure D.5: BLOSC header Version 1.0.

The second event in the file is a Run Number event which contains the run number of this measurement. Old files do not start with a File Type event, but with a Run Number event to denote the old file format. The old file format does not feature compression and can be read like an uncompressed file.

The rest of the file contains event groups, starting with a BOR event group which consists of a group header and a BOR event for each device in the data stream. All devices which want to send data need to sent an BOR event first. The BOR event group is followed by zero or more device group events containing detector data. Each device group event contains a group header and zero or more device events. The last event in a file should be a EOR event group, analog to the BOR group. All devices a BOR event was sent for must send an EOR event. The EOR event may be missing if data taking stopped without properly closing BonnDAQ.

Compression Compression is preformed using the BLOSC metacompressor with format version 1.0[1]. The file contains one or more compressed blocks. Blocks are compressed respecting the underlying group event structure. This guarantees, that each group event is completely contained in a compressed block.

Each compressed block consists of a 16 byte header, the compressed data and a 4byte CRC32 checksum[2]. The blosc header is shown in figure D.5. From it, the length of the compressed block

[1] `https://github.com/Blosc/c-blosc`

[2] width: 32, polynom: 0x04c11db7, RefIn: false, RefOut: false, XorOut: 0. Used Init value: 0. Same as DHE/DHC use.Yields same result as gdb remote protocol qCRC, (that protocol uses init value 0xffffffff, we use 0)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1. request token
2. Message type
3. Size of payload excluding network header in 4 byte words
4. Reserved
5. trigger number
6. Number of events in event group
7. Index of event in the event group
8. Reserved
9. Reserved
10. Reserved

Figure D.6: BonnDAQ network header

including the header can be read. The given compressed size does not include the 4 bytes needed for the CRC checksum.

Network format Clients can request live data from BonnDAQ. This is done by connecting to the data_server_thread using TCP. All messages between server and client consist of a 40 byte header and optional payload. The communication uses a word size of 4 bytes, so the payload must be a multiple of this. The network header is shown in D.6. Four messages exist:

- The client can test the connection. For this, it sends a message with message type 0xABCDEF00 and no payload to the server
- The server replies to a connection test. For this, it sends a message with message type 0xABCDEF11 and no payload to the client.
- The client can request events. For this, it sends a message with message type 0xAABBCCDD and a request token to the server. Request tokens can be 0x0 (No request, stop request), 0x2 (request single event), 0x3 (request continuous event stream) and 0x13 (request continuous exclusive event stream[3]). In the request, the client gives the maximum event size it can receive as payload.
- The server sends an event to the client. For this, it sends one or more messages with message type 0xAABBCCDD to the client. The server fills the fields as described in D.6. Each message is followed by payload. For each device in the group, a single packet is sent. The number of expected messages is sent in field 6: "Number of events in event group". The number of the current message in the event is sent in field 7: "Index of event in the event group". Numbers in field 7 are counted from 0 to (field 6) -1

All values which are not mentioned for the above messages are expected to be zero.

After initialization of the connection, the client will first receive a run number event, then a BOR event, before device events can be sent. The payload is formated as given in above chapters. In network packets,

[3] This forces BonnDAQ to wait on the client if it is not fast enough.

only BOR, EOR, Run number and device events are transmitted. There are no event groups as payload. The network format always sends data uncompressed.

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