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Development of depleted monolithic active pixel sensors for high rate and high radiation experiments at HL-LHC

Toko Hirono

Depleted monolithic active pixel sensors (DMAPS) are developed to demonstrate their suitability for high energy particle physics experiments in high radiation and high hit-rate environments. In this thesis, characterization of DMAPS prototypes in the large fill factor design using highly resistive wafers has been performed. Three prototypes, including a large-scale and fully-monolithic prototype, were fabricated using 150 nm CMOS technology on highly resistive (>2 kΩ cm) wafers. The results of the characterization indicate that the DMAPS has capabilities to fulfill the requirements for the outer layers of the ATLAS ITk Pixel Detector. DMAPS prototypes coupled with an additional readout chip are also tested for future applications.

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Contents

CHAPTER 1

Introduction

New detectors played important roles in the discovery of new physical phenomena. In particle physics, for example, the existence of the Higgs boson has been experimentally proven [1, 2] with the help of two novel detectors: A Toroidal Large Hadron Collider (LHC) ApparatuS (ATLAS) [3] and Compact Muon Spectrometer (CMS) [4]. A theory of particle physics called Standard Model predicted the existence of the Higgs boson in the 1960's [5]. However, one had to wait for this discovery until the construction of ATLAS and CMS detector in addition to the particle accelerator, which accelerates particles to energis of the order of TeV. In 2010, ATLAS and CMS started operation, and four years later, in 2012, the discovery of Higgs boson lead to the researches being awarded the Nobel Prize in 2013.

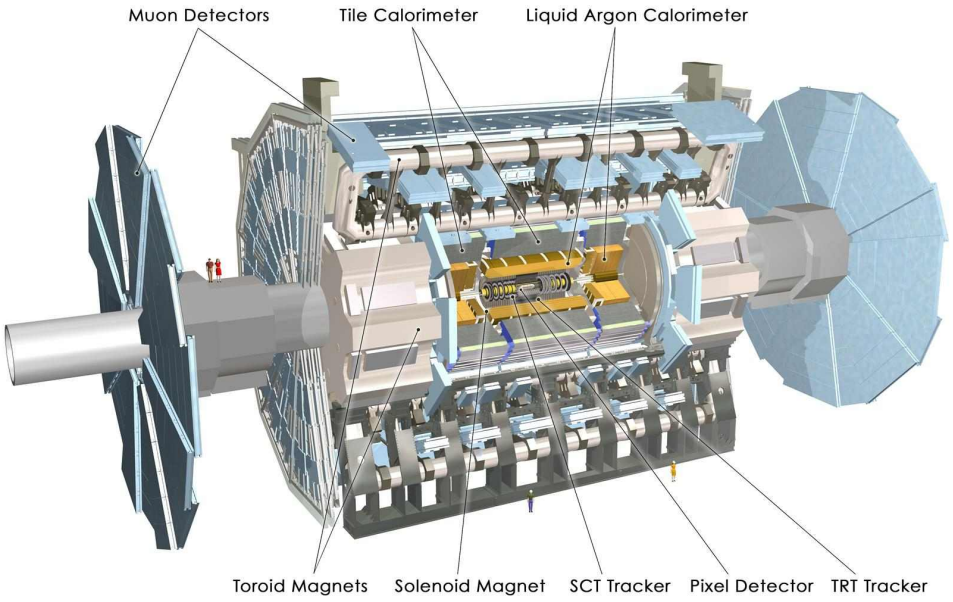


Figure 1.1: Layout of ATLAS detector [6]. The innermost detectors are pixel detectors.

The ATLAS detector not only searches for the Higgs bosons but also performs many other physics programs [7]. It is a general-purpose high-energy particle detector that is installed in

a particle accelerator named LHC [8]. Protons collide in the center of mass energy of 14 TeV at the center of the ATLAS detector. It consists of many sub-detectors (Figure 1.1), and each of them detects different physical values, such as creation point, energy, and momentum of different types of particles.

Pixel detectors are placed at the innermost layers of the ATLAS detector. They are segmented in two dimension and able to detect the position of particles, of which the granularity corresponds the size of the pixel [9]. Specifications of the pixel detector, such as the spatial and timing resolution and the detection efficiency, have successfully fulfilled the requirements coming from the ATLAS experiment [10].

The success of the ATLAS and CMS experiments motivated further experiments which required higher detector performances, such as higher granularity, more complex triggering scheme, and higher production throughput. Detectors using new concepts have been proposed to realized the future experiments. Particularly, monolithic CMOS active pixel sensor (MAPS) has been proposed [11] as a novel pixel detector. MAPS is a pixel detector which has sensing volume and signal processing electronics in a single chip. The study of MAPS as high energy particle detector was started [12, 13], and MAPS has been or will be adopted in the many projects (e.g. [14, 15]). However, MAPS degrades its performance after irradiation with high energy particles used in the LHC experiments [16, 17]. This crucial disadvantage has been solved in depleted monolithic CMOS active pixel sensor (DMAPS). DMAPS maintains high detection efficiency if a strong electric field can be yield in its sensitive volume after irradiation [18].

This thesis discusses suitability of DMAPS as a pixel detector in upgraded LHC experiments that will be starting from the year 2026. The discussion is based on the characterizations of DMAPS which was performed in this study. In particular, radiation hardness of DMAPS prototypes in realistic chip scale is characterized and compared to the requirements of the ATLAS Pixel Detector. In addition, the possibility of 3D implementation by combining DMAPS with readout chip for future applications is discussed.

Chapter 2 of thesis clarifies the requirements of the pixel detector for the future LHC experiments. In Chapter 3, the design of DMAPS is discussed regarding the requirements. Subsequently, the principle of particle detection by silicon pixel detector is also described in order to understand the behavior of DMAPS using the measurement results shown in the later chapter. Since the effect of the radiation on DMAPS is one of the main concerns, overview of the radiation effects on silicon is also briefly mentioned in this chapter. Chapter 4 shows detailed specification of DMAPS prototypes characterized in this thesis. In Chapter 5, the measurement setups and methods used in the characterization are described. The results of characterization is shown in Chapter 6 followed by the discussions in Chapter 7. Finally, Chapter 8 provides the conclusion.

This thesis is partially based on the author's publications [19–21], with some passages copied verbatim.

CHAPTER 2

Requirements for next generation pixel detectors

In this chapter, the requirements to the pixel detectors in the future ATLAS experiments are described. Since detector performances must be matched to the properties of particle accelerator, where the detector is installed, this chapter starts with the upgrade plan of LHC (Section 2.1). Fundamental parameters of pixel detectors and radiation damage are introduced in Section 2.2. In this section, the actual requirement values are also given. In Section 2.3, the requirements of pixel detectors are summarized and compared to other projects.

2.1 LHC and its upgrade

The center-of-mass energy of a collider corresponds to the ability to create a phenomenon that has never been observed in lower center-of-mass energy colliders. The center-of-mass energy of LHC is the highest worldwide. The LHC consists of a 27-kilometer ring Two beams travel in opposite directions in the ring and collide at four points. LHC is operating at the center-of-mass energy of 13 TeV and will be operated at the designed value of 14 TeV in 2019 [8].

LHC is a proton-proton collider. Acceleration of protons up to TeV order in a cyclic particle accelerator is easier than that of electrons or positions. The energy of charged particle is partially emitted by the synchrotron radiation and lost, which inversely proportional to the static mass of the particle. Thus, the loss of protons is a factor of 2000 less than that of electrons or positrons.

The disadvantage of the proton-proton collider is that a proton is not elementary particle and compound of multiple elementary particles, such as quarks. Average energies of quarks inside a proton are usually approximately 0.1-0.2 of the proton energy, and the probability that a quarks has an energy close to the proton's is small. This leads to the center-of-mass energy of colliding quarks is as 0.01-0.2 of that of protons [22]. Most of these collisions occur in low energies and are not interested by the ATLAS physics programs. The occurrence of interesting high energy scattering interaction is rare. For example, the cross section of Higgs production is 100 pb, whereas that of proton-proton collision is 100 mb [22].

The rate of interactions, R_{inter}, can be written as follows:

$$R_{inter} = \sigma_{inter} \cdot L$$

where σ_{inter} is the cross section of the interactions and L is luminosity. L is a value expressed only with parameters of the collider as follows:

$$L = f\frac{n_1 n_2}{A}$$

where f is repetition rate of collisions, n_i is the number of particles in a bunch of the two-colliding beams, and A is the cross sectional area of the beam. Since σ_{inter} is determined by the properties of the particle and cannot be increased, high luminosity is required especially in proton-proton colliders to obtain sufficient number of interesting interactions. The luminosity of current LHC at the collision point is $1 \times 10^{34}\,\mathrm{cm^{-2}\,s^{-1}}$ [8].

The luminosity has been improved since LHC started its operation. In addition, large upgrade of LHC has been proposed [23, 24]. The proposed project is called High Luminosity LHC (HL-LHC) and aims to achieve L factor of 10 higher than the designed value of current LHC. The operation of HL-LHC is planned to start from 2026. Figure 2.1 shows the forecast of peak L of the collider [24]. The design value of HL-LHC is $L = 5 \times 10^{34}\,\mathrm{cm^{-2}\,s^{-1}}$. All systems of the collider will be designed with some margin. If those margins are considered, the final L will be $7.5 \times 10^{34}\,\mathrm{cm^{-2}\,s^{-1}}$. With integrated L of $250\,\mathrm{fb^{-1}}$ year^{-1}, $3\,000\,\mathrm{fb^{-1}}$ will be obtained in about 12 years after the upgrade.

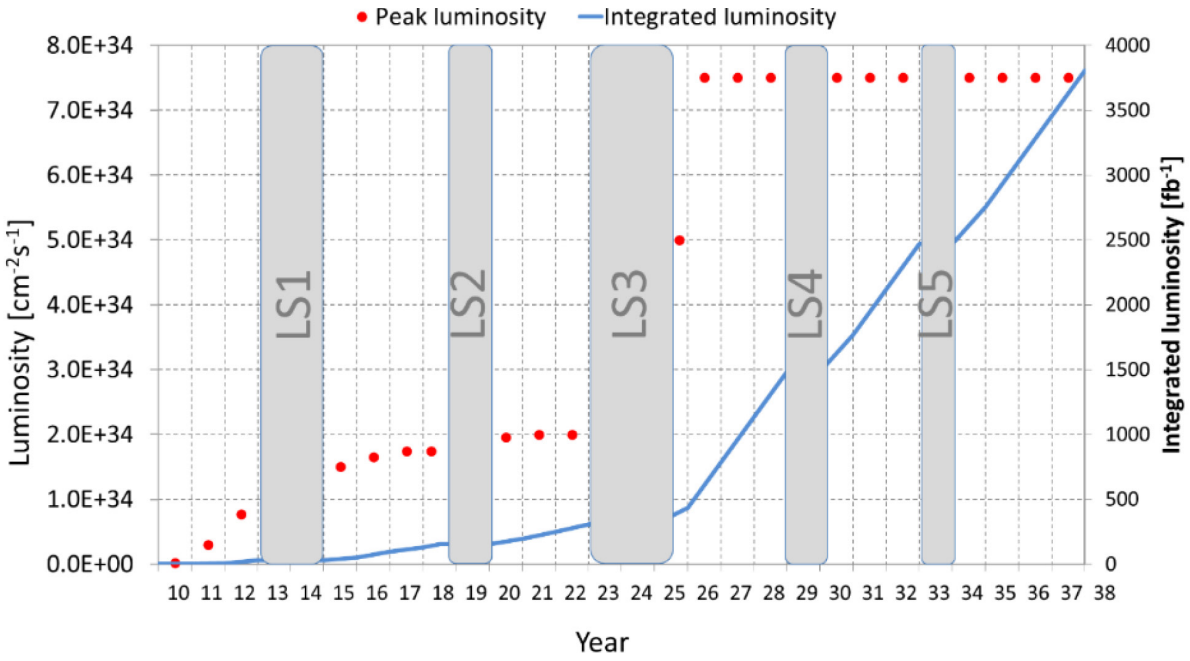


Figure 2.1: Possible peak luminosity (red dots) and integrated luminosity (blue line) in the LHC, for the case of ultimate HL-LHC parameters [24]. LS1-5 indicates long shutdown of LHC (gray blocks). HL-LHC starts after LS3. No learning curve for luminosity after LS3 is considered for simplicity.

2.2 ATLAS ITk Pixel Detector

Upgrade of the ATLAS detector has been planned corresponding to the HL-LHC operation schedule. The current ATLAS detector consists of four major components: the Inner Detector (ID), the Calorimeter, the Muon Spectrometer, and the Magnet System. ATLAS ID is a tracker, which is the innermost component among the four. Figure 2.2 (a) shows the drawing of the ATLAS ID. Trajectories of charged particles are obtained by the tracker. Three types of position-sensitive detectors are situated in cylindrical and concentric fashion around the interaction point: Pixel Detector, Semiconductor Tracker, and Transition Radiation Tracker. The Pixel Detector is installed in the innermost four layers of ATLAS ID.

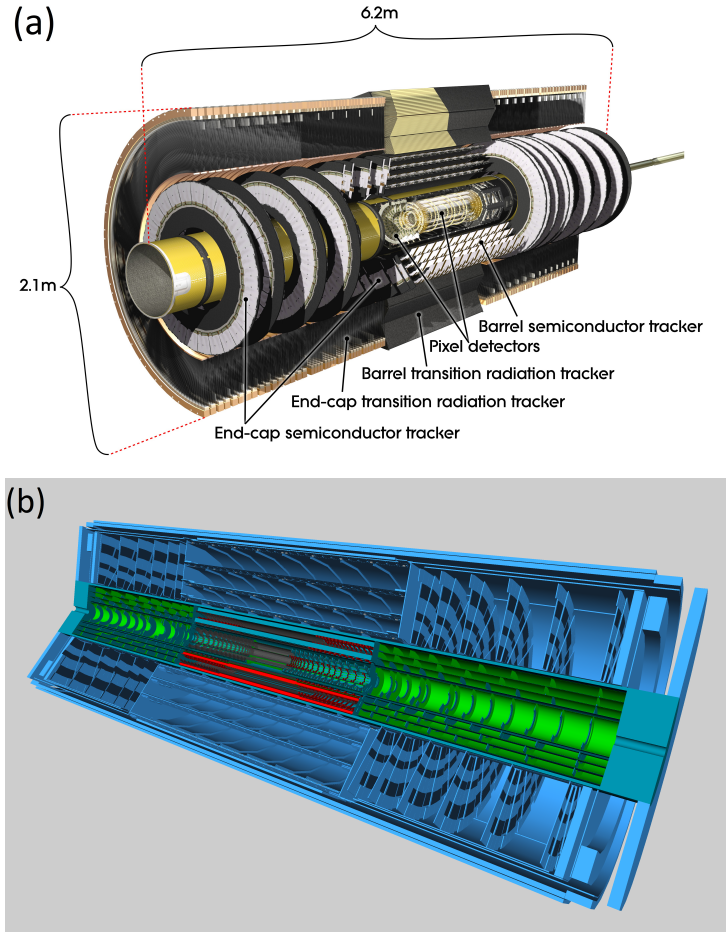


Figure 2.2: A drawing of the (a) ATLAS ID [25] and (b) ATLAS ITk [26]. Pixel detectors are placed in the innermost part of ATLAS ID and ATLAS ITk. The Strip Detector is shown in blue and Pixel Detector is shown in red or green in (b). The diameter and length of ATLAS ITk is 2 m and 6 m, respectively.

2.2.1 Hit rate

In a detector's point of view, L should be translated to hit rate, namely number of pixels responding to particles per area and time. The current hit rate at the innermost cylindrical

layer is as high as 1 MHz/mm^2 [27]. All trajectories, including particles from low-energy uninteresting interactions, need to be detected and distinguished from each other for further analysis. The granularity of the pixel detector is high, so that the probability of two or more particles passing through the same pixel is low even if the hit rate is high. The pixel detector is installed in the highest hit rate region, namely the innermost layers, where they are closest to the proton-proton collision point.

According to the HL-LHC operation, ATLAS ID will be replaced by ATLAS inner tracker (ITk) during the period shown as LS3 in Figure 2.1 [28]. Figure 2.2 (b) shows a drawing of ATLAS ITk [26].

Since the ATLAS Calorimeter is surrounding the tracker and that it will not be replaced for HL-LHC operation, the size of ATLAS ITk is about as same as that of ATLAS ID. Pixel and strip detectors will be situated cylindrically and concentrically around the interaction point. The hit rate of the pixel detector, of which the position is closest to the interaction point, is expected to be 10 MHz/mm^2/s [26]. The number of pixel detector layers has been planned to be increased from four to five in order to cope with the high hit rate. DMAPS have been proposed to be installed on the outer layers, particularly the fourth layer, of those five-pixel detector layers [26].

2.2.2 Area covered by pixel detectors

The proton-proton collision scatters particles in all directions. However, it is impossible to layout pixel detectors in the way to accept all particles because of the actual geometrical limitation, such as the existence of the beam pipe. The pseudorapidity is a geometrical parameter usually used to discuss the acceptance of detectors. It is expressed as follows:

$$\eta = -ln(tan\frac{\theta}{2})$$

where θ is the angle with respect to the beam. The range of pseudorapidity will be increased from ATLAS ID ($|\eta| < 2.5$) to ATLAS ITk ($|\eta| < 4.0$) [26]. Figure 2.3 shows one of the layout candidates. The ATLAS ITk Pixel Detector will be arranged in layers of cylindrical barrels and disks covering the forward and backward regions. More pixel detectors will be placed along the beam pipe than in ATLAS ID to accept particles up to high $|\eta|$ in high hit rate. Although the layout of the pixel detector has not been finalized yet, the area covered by pixel detector in total is estimated to be as large as 12–14 m^2 [26]. Mass production capability is one of the requirements for the ATLAS ITk Pixel Detector.

2.2.3 Detector response time

The repetition frequency of proton-proton collisions in LHC is 40 MHz and it will be kept the same in the HL-LHC operation [24]. Fluctuation of hit detection time related to one collision must be smaller than 25 ns. Hits detected later than 25 ns will not be assigned to the collision, and it will be assigned to the next collision; thus the detector will lose its efficiency. Furthermore, in the next collision, the delayed hits will be counted as noise because it is not the signal from the corresponding collision. The allowed noise frequency is defined as noise

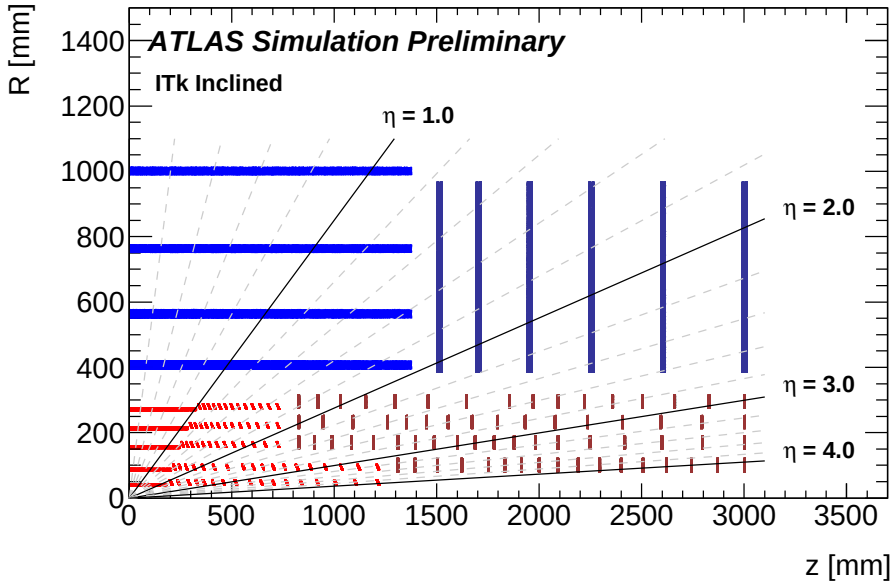


Figure 2.3: Quadrant cross sectional layout of the ATLAS ITk with the Strip (blue) and Pixel (red, brown) Detectors [26]. Only active elements of the detector are shown and inactive elements, such as support structure, are omitted from the layout. The horizontal axis is along the beam pipe with zero being the interaction point. The vertical axis is the radius measured from the interaction point.

occupancy, which is number of noise hits per bunch crossing per pixel. In ATLAS ITk Pixel Detector, the required hit-finding efficiency is $\geq 97\,\%$, and the noise occupancy is required to be lower than $<1 \times 10^{-6}$ /25 ns/pixel for the ATLAS ID Pixel detector [26].

2.2.4 Radiation hardness

In the HL-LHC operation, a large number up to 2×10^{16} /cm of high energy particles are expected to pass through and damage the pixel detector. The radiation hardness of detectors is a major concern in high energy physics experiments in a hadron collider. In the following paragraphs, the estimated amount of radiation is shown by the mean of two values because the radiation damage can be categorized into two types [29], namely surface and bulk damage. In this chapter, only the estimated amount of radiation in HL-LHC are introduced, and the radiation damage mechanism is explained in Section 3.5.

The ionization of material by charged particles or photons is the main cause of the surface damage. The damage is known to be proportional to the absorbed energy which is used in the ionization process, namely total ionizing dose (TID). The relevant unit is Gy; 1 Gy means energy of 1 J is absorbed by 1 kg material. In this thesis, rad is also used, and 1 rad equals to 0.01 Gy. The simulated TID after the HL-LHC lifetime is shown in Figure 2.4 [30]. The outer layers of the ITk Pixel Detector are expected to be exposed to TID of 50–80 Mrad with safety factors.

NON-IONIZING ENERGY LOSS (NIEL) mainly causes bulk damages due to displacement of atoms from lattice sites in detector material. The damage is known to be dependent on the

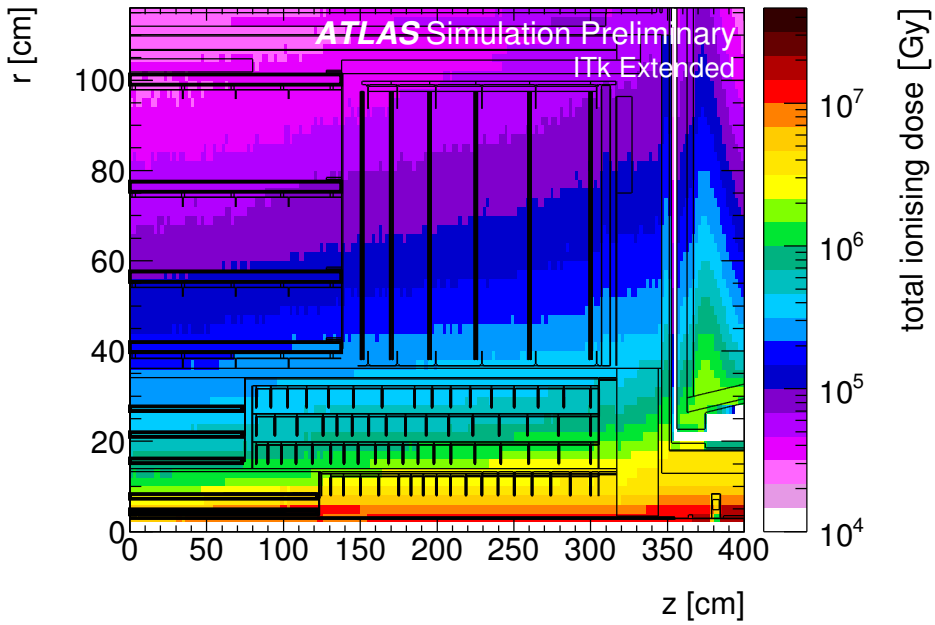


Figure 2.4: The simulated TID in the ITk region normalized to 3 000 fb^{-1} of proton-proton collisions at 14 TeV [30]. The plot is a quadrant cross section of the region using same horizontal and vertical axis units as given in Figure 2.3. The active detector elements are overlapped in black bold lines. The TID unit in the plot is Gy. 1 rad is equal to 0.01 Gy. No safety factor is included in the simulation.

type and energy of particles [31]. Various types of particles with wide range in energy are created in the environment of HL-LHC. A normalizing factor, which is called hardness factor with respect to 1 MeV neutrons, is defined to compare bulk damages between different radiation environments (described more in Section 3.5). The unit of the radiation damage normalized to 1 MeV is written as n_{eq}/cm^2. Figure 2.5 shows the simulated 1 MeV neutron equivalent fluence after 3 000 fb^{-1} of proton-proton collisions at 14 TeV. The outer layers of the ITk Pixel Detector are expected to be exposed to a radiation of 1–2 $\times$ 10^{15} n_{eq}/cm^2 including safety factors.

2.3 Summary of the ATLAS Pixel Detector requirements

Table 2.1 summarizes the environment where ATLAS ITk Pixel Detector is expected to be installed. ATLAS ITk Pixel Detector should keep its hit finding efficiency of >97 % with noise occupancy of $<1 \times 10^{-6}$ /25 ns/pixel in the environment. Since the target application of DMAPS is the outer layers of the ATLAS ITk Pixel Detector, the requirements of the inner and outer layers are listed separately. Table 2.1 also shows the specification of the current ATLAS ID Pixel Detector for comparison. The requirements of outer layers of ATLAS ITk Pixel Detector are similar to that of the ATLAS ID Pixel Detector. If the performance of DMAPS is equivalent to that current ATLAS ID Pixel Detector, DMAPS could be applied to the outer layers of the ATLAS ITk Pixel Detector. Table 2.1 shows the requirements of other projects that adopted or plan to adopt MAPS. As the table shows, the required radiation hardness and hit rate of DMAPS

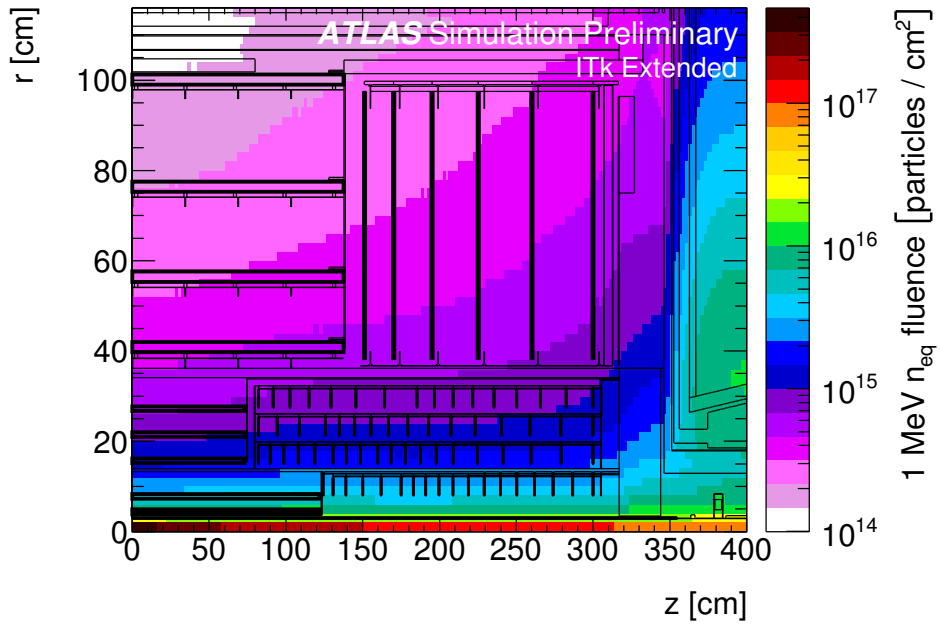


Figure 2.5: Simulated 1 MeV neutron equivalent fluence in the ITk region normalized to3 000 fb^{-1} of proton-proton collisions at 14 TeV [30]. The plot is a quadrant cross section of the region using same horizontal and vertical axis units as given in Figure 2.3. The the active detector elements are overlapped in black bold lines. No safety factor is included in the simulation.

is more than one order higher than those of MAPS. The requirements from the up-coming high-luminosity experiments motivated the development of DMAPS.

Table 2.1: Requirements for pixel layers of detector in high energy particle physics

	STAR	ALICE	ILC	ATLAS-LHC	ATLAS-LH-LHC Outer	ATLAS-LH-LHC Inner
Response time [ns]	110	20000	350	25	25	25
Hit rate [kHz/mm^2]	3.8	10	250	1,000	1,000	10,000
TID [Mrad]	0.09/year	0.7	0.4	80	50-80	>500
NIEL [n_{eq}/cm^2]	$> 10^{12}$	$> 10^{13}$	$> 10^{12}$	2×10^{15}	$1\text{-}2 \times 10^{15}$	$> 2 \times 10^{16}$

CHAPTER 3

Signal generation and development in DMAPS

This chapter describes the concept of DMAPS and their fundamental characteristics which are concerned to fulfill the requirements presented in Chapter 2. First, the structure of DMAPS is described in Section 3.1. Since DMAPS is a semiconductor detector made of silicon, behavior of silicon as a particle detector are briefly introduced in Section 3.2. Several equations which are employed to understand the behaviors of DMAPS in later chapter is given with short explanations because those equations and their derivation are found in many literature [9, 29, 32, 33]. In Sections 3.3 and 3.4, fundamental values which describe the performance of pixel detectors are introduced and how those parameters are related to the ATLAS requirements are discussed. Sensor properties are mainly presented in Section 3.3 and readout electronics are presented in Section 3.4. Radiation damage on DMAPS is described in Section 3.5, and the way to minimize the detector performance degradation due to the radiation has also been discussed. Finally, the specification of DMAPS is summarized in Section 3.6 in order to develop radiation hard and high-rate-capable DMAPS.

3.1 Structure of pixel detectors

Figure 3.1 illustrates the structure of DMAPS and a hybrid pixel detector [34, 35], which is current ATLAS ID Pixel Detector [27]. In addition, Figure 3.1 also shows another type of pixel detector that is a combination of DMAPS and hybrid pixel detector. The pixel detectors has two functionalities: one is the signal generation and transport in a sensitive part (indicated as a symbol of diode in Figure 3.1), and the other one is the signal development in the readout electronics (indicated as symbols of amplifier and digital logic components in Figure 3.1). Pixel detectors can be categorized to one of three types based on where those functionalities are implemented.

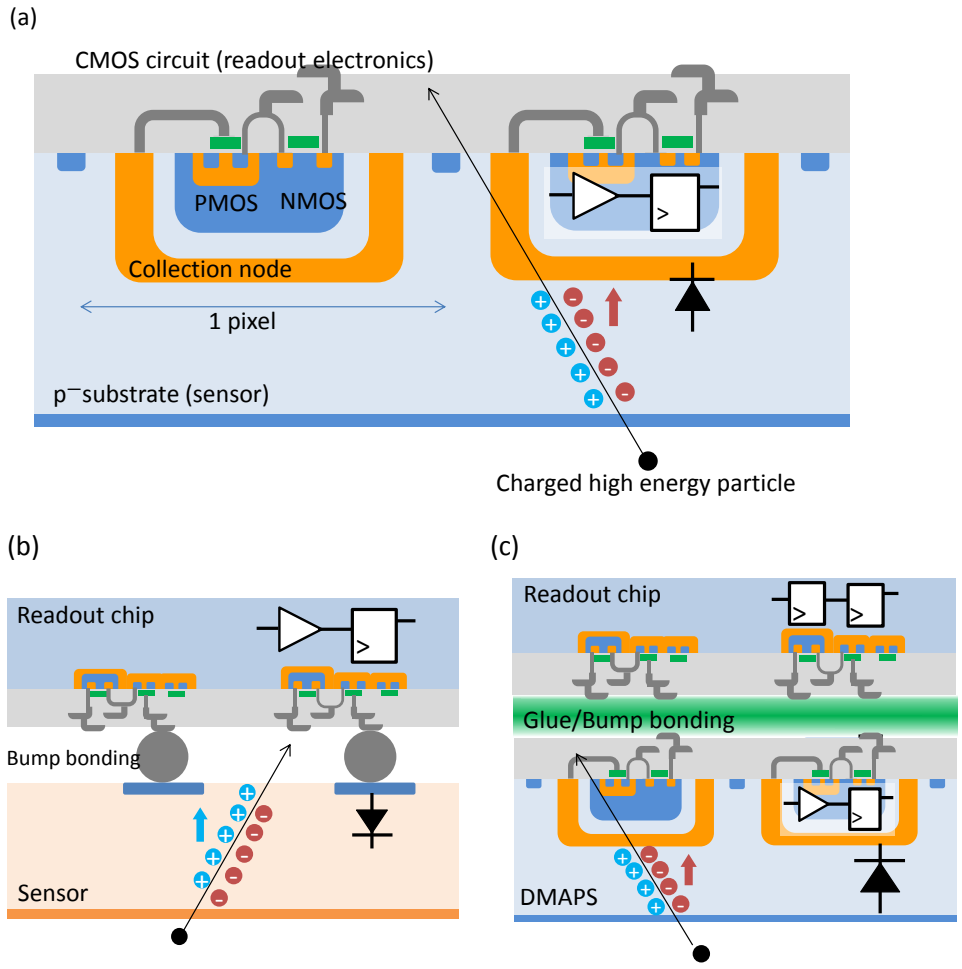


Figure 3.1: Cross sectional view of a (a) DMAPS, (b) hybrid detector, and (c) DMAPS coupled with a readout chip

3.1.1 Hybrid pixel detector

Figure 3.1 (b) shows the cross sectional view of a hybrid pixel detector. It is made up of two parts: one is highly resistive sensor with 2D segmented electrode pads. The other one has pixelated readout electronics with input pads created by a CMOS fabrication process. Connections between the sensor electrodes and readout input pads are made by pixel-to-pixel bump bondings. Signal charges created in the sensor device are sent to the connected input pad of the readout chip and amplified in the readout electronics.

The pixel pitch size of ATLAS ITk Pixel Detector at the layers where the hit rate is highest is considered to be either 50 µm × 50 µm or 50 µm × 100 µm, for instance [28]. As 25 µm bump bonding pitch is available [36], it is possible to realize sufficiently small pixel size which is required from the HL-LHC operation. Although the hybridization technology is matured and the bump bonding does not limit the pixel size, fine-pitch bump bonding is cost intensive. Moreover, the hybridization is a bottleneck of the production speed. DMAPS has an advantage on mass

production compared to a hybrid pixel detector because the fine-pitch bump bonding is not needed in the DMAPS production.

3.1.2 DMAPS

Figure 3.1 (a) shows the cross sectional view of DMAPS. In MAPS, including DMAPS, signal generation and signal development are performed in a single silicon chip. A CMOS fabrication process creates pixelated signal collection electrodes and circuit components, such as metal-oxiside-silicon (MOS) transistors, resistors, and capacitor, on a single silicon wafer. The sensor diodes are formed at the interfaces between the wafer substrate and the collection electrodes, and the collection electrodes and the electronics are connected using a metal layers fabricated during the CMOS process.

3.1.3 DMAPS coupled with a readout chip (DMAPS + R/O)

Figure 3.1 (c) shows the structure of another possible pixel detector using DMAPS. It is a combination of DMAPS and hybrid pixel detector concepts. In the developments of current pixel detector, the smallest size of the pixel is limited by the size of CMOS electronics in a pixel [37]. In this design concept, the area where readout electronics can be implemented, in principle, is a factor of 2 larger than that of the simple standalone DMAPS or the conventional hybrid pixel detector.

In addition, the feature size of a CMOS technology used for the DMAPS fabrication is usually not the finest. For example, prototype chips investigated in this thesis are fabricated in the 150 nm CMOS process, whereas the latest hybrid detector readout chip has been developed in 65 nm CMOS process [38]. The CMOS feature size affects the circuitry size more effectively when the circuitry works as digital logic than analog amplifiers. In order to get the most of this benefit, signal can be digitized in DMAPS and the additional readout chip can be mainly digital logic in the finest CMOS feature size.

The connection between DMAPS and the additional readout chip does not have to be pixel-to-pixel bump bonding because signal charges from the sensor is already amplified and, in the most of the cases, it is digitized in DMAPS. Two options are proposed to avoid the fine-pitch bump bonding: one is capacitive coupling [39] and the other is pixel en/decording [40]. Glue can be used for connection between the DMAPS and the additional readout chip instead of bump bonding in capacitively coupled pixel detector (CCPD). As an alternative or in addition, signals from multiple pixels can be merged in DMAPS and send to a single pixel of the readout chip. Then, the position of the pixel will be encoded in DMAPS and decoded in the readout chip.

The DMAPS + R/O detector is for future applications. Although this thesis mainly characterized the standalone-type DMAPS shown in Figure 3.1 (a), the feasibility of this type of pixel detector (Figure 3.1 (c)) is also included in this thesis.

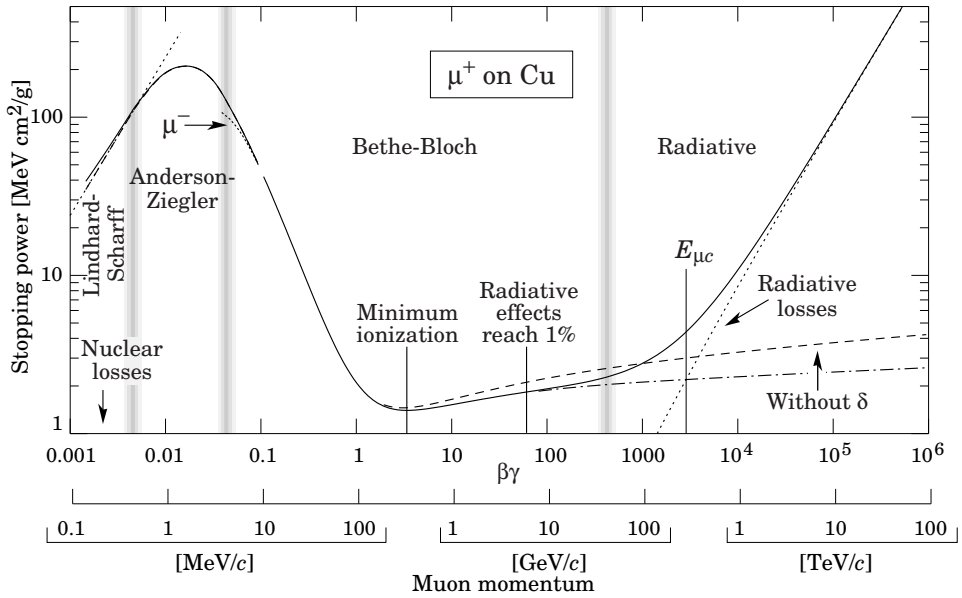


Figure 3.2: Mass stopping power for positive muons in copper as a function of $\beta\gamma$ [29]. Solid curves indicate the total mass stopping power. Vertical blue bands indicate boundaries between the different approximations. The MIP energy is included in the region where Bethe-Bloch approximation is valid.

3.2 Fundamentals of silicon sensors

3.2.1 Energy deposition of charged particles

When a high energy charged particle is passing through the sensing part of DMAPS (indicated by the diode symbol in Figure 3.1 (a)), the particle loses its energy along its traversing path. Figure 3.2 shows the overview of a mass stopping power of material as a function of $\beta\gamma$ of the traversing particle [29]. The mass stopping power is the energy loss per unit of the path length and mass of the absorbing material. β is the velocity of the traversing particle in units of the light speed, and γ is Lorentz factor.

A particle which has the mean rates of energy loss at the minimum is said to be the minimum ionizing particle (MIP). $\beta\gamma$ of MIP is approximately 3, which does not depend on the type of particle [29]. Figure 3.3 shows the mass stopping power of muon and electron in silicon. $\beta\gamma$ of MIP is also approximately 3.

The mass stopping power increases moderately in the region of energy that is higher than the MIP energy. Testing DMAPS using particles at MIP energy or higher (lower than energy range where radiation process is dominant) represents the worst case of the signal generation.

As shown in Figure 3.2, the MIP energy is included in the region where the Bethe-Bloch approximation is valid. The dominant energy losing process in this energy region is inelastic collisions between the traversing particle and atoms in the sensor materials [29]. Statistical fluctuations occurs in the number of inelastic collisions and in the energy transferred in each collision. The fluctuation of energy loss for silicon pixel sensor, whose thickness is typically 50–300 μm, follows Landau distribution [44] convoluted with Gaussian function [45]. The

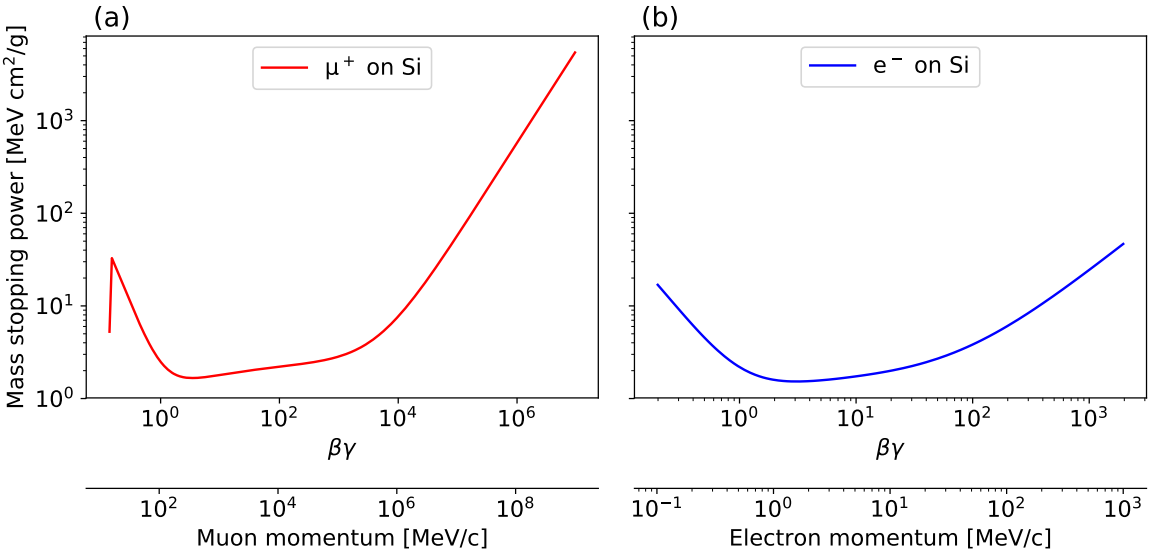


Figure 3.3: Mass stopping power for (a) positive muons and (b) electron in silicon as a function of $\beta\gamma$. The MIP energy is also approximately $\beta\gamma = 3$. Data are taken from [41, 42] and [43] for (a) and (b), respectively.

function can be expressed as follows:

$$f(x,\Delta) = \frac{1}{\sigma\sqrt{2\pi}} \int_{-\infty}^{\infty} f_L(x,\Delta-\tau) e^{-\frac{\tau^2}{2\sigma}} d\tau, \tag{3.1}$$

where $f_L(x,\Delta)$ is the Landau function, σ is standard deviation of the Gaussian function. Furthermore, x and Δ in f_L is the mass thickness (i.e., a product of the density of the material and its thickness) of the sensor and particle energy loss, respectively. The expresssion of Landau function can be found in [32]. The Landau distribution as a function of Δ/x for various thicknesses of silicon sensor is shown in Figure 3.4 [29].

The energy deposition peak is called the most probable value (MPV) and can be expressed as follows [29]:

$$\Delta_p = \xi \left[ln\frac{2m_e c^2\beta^2\gamma^2}{I^2} + ln\frac{\xi}{I} + 0.2 - \beta^2 - \delta \right], \tag{3.2}$$

where:

$$\xi = 2\pi N_a r_e^2 m_e c^2 \frac{Z}{A}\left(\frac{z}{\beta}\right)^2 x,$$

with:

- N_a = Avogadoro's number = $6.022 \times 10^{23}\,\mathrm{mol}^{-1}$,
- r_e = classical electron radius = 2.817×10^{-13} cm,
- $m_e c^2$ = electron mass $\times c^2$ = 0.510999 MeV,

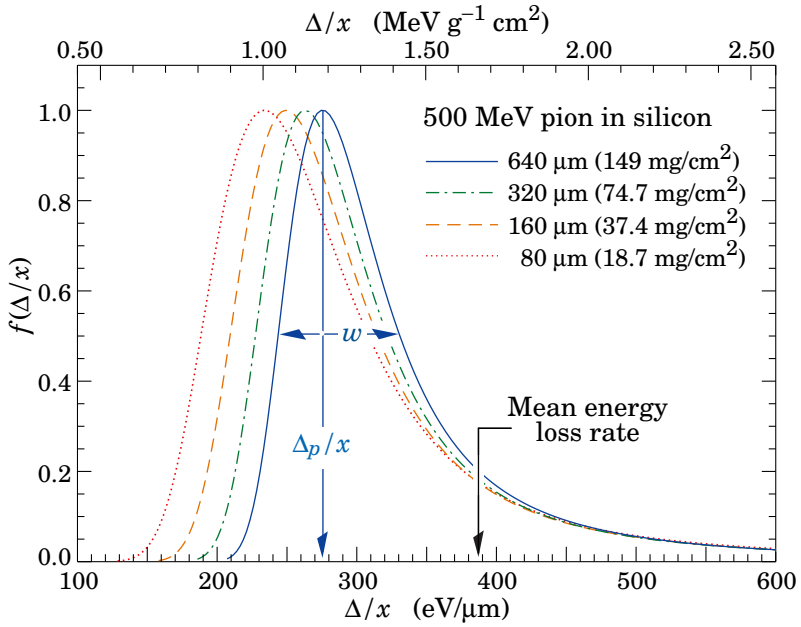


Figure 3.4: Distribution of energy loss for 500 MeV pions in silicon, normalized to unity at the peak [29]. The horizontal axis is energy loss normalized by the mass thickness.

- Z = atomic number of sensor material,
- A = atomic mass of sensor material, and
- z = charge mass of incident particle.

Table 3.1 shows the silicon properties used in Equation (3.2) or introduced in later sections.

3.2.2 Charge generation

The energy deposition due to the inelastic collisions results in the excitation or ionization of sensor atoms in the silicon sensor. Electron-hole pairs are created along the particle's trajectory. The number of generated electron-hole pairs N_{e-h} is related to Δ_p by:

$$N_{e-h} = \frac{\Delta_p}{E_{e-h}} \approx 80 \cdot d \ [\mathrm{e}^-], \tag{3.3}$$

where E_{e-h} is the average energy needed to produce an electron-hole pair, namely radiation ionization energy. It is proportional to the energy gap between conduction and valence band of the semiconductor. In addition, E_{e-h} is 3.65 eV in the case of silicon [46], and d is the sensor thickness in μm. The approximation has been made with the MPV of 265 eV/μm (Figure 3.4 green dashed line). Equation (3.3) leads to roughly 24 ke^- for 320 μm silicon sensor. It is noteworthy that creation of charges per unit sensor length moderately depends on the sensor thickness because MPV scales as $xcdot(a\ ln(x)+b)$. Equation (3.3) gives only a rough estimation for the sensor thickness of approximately 250 μm.

Table 3.1: Properties of silicon [29, 41, 46–49].

Atomic number	14
Atomic weight	28.0855(3)
Density	2.329 g/cm^3
Relative permittivity ϵ_{Si}	11.68
Average energy loss of MPV	1.66 MeV cm/g
Mean excitation energy	172.0 MeV
Energy gap E_g	1.12 eV
Radiation ionization energies E_{e-h}	3.65 eV
Radiation legth X_0	21.82 g/cm^2
Effective mass (Longitudinal) m^*	1.06 m_e (electron), 0.59 m_e (hole)
Mobility μ	1 416 cm^2/V s (electron), 425 cm^2/V s (hole)
Mobility parameters	μ_{min}: 68.5 cm^2/V s (electron) 44.9 cm^2/V s (hole)
	μ_{max}: 1 414 cm^2/V s (electron) 470.5 cm^2/V s (hole)
	N_r: 9.20×10^{16} /cm^3 (electron) 2.23×10^{17} /cm^3 (hole)
	α: 0.711 (electron) 0.719
Fano factor	0.12 at 300 K

Although a thick sensor generates large signals, there is a disadvantage of thick sensors related to a phenomenon called multiple scattering. Elastic collisions between the traversing particle and the nuclei of sensor atoms occur even though the dominant energy loss process is inelastic collisions. Multiple scattering is the accumulation of the elastic collisions, for example, Coulomb scatterings, which deflects a trajectory of the traversing particle. The multiple scattering degrades the spatial resolution of the tracker.

The scattering angle follows the Gaussian distribution roughly with a root mean square θ_{ms}:

$$\theta_{ms} = \frac{13.6MeV}{\beta pc} z \sqrt{\frac{x}{X_0}} \left[1 + 0.038 ln \left(\frac{x}{X_0} \right) \right], \tag{3.4}$$

where X_0 is the radiation length and p is the incident particle momentum in MeV [32]. X_0 is defined as the mean distance over which a high-energy electron loses all but 1/e of its energy by bremsstrahlung. As multiple scattering scales as $1/p$, it is severe when the traversing particle energy is low.

The thickness of the sensor is usually limited by the acceptable multiple scattering angles when the experiments performed with rather low-energy particles or large z. MAPS are used as pixel detectors in such projects (Table 2.1) because MAPS can omit additional multiple scattering in the readout chip and bump bonding. the bump bonding is usually formed with heavy metals of which X_0 is small. In case of the ATLAS experiments, the particle energy is high; therefore, multiple scattering due to the thick sensor are not the main concerns.

3.2.3 Velocity of charge carriers

The signal charges generated in DMAPS should be collected by 2D segmented electrodes, so that DMAPS function as a pixel detector. There are two mechanism for charge movement: diffusion and drift [9]. Diffusion involves a charge moving in response to a concentration gradient; it is due to thermal random walk of charges and spreading of the charge cloud is slow. Only partial charges reach the collection electrode before recombination if the signal charges are collected by diffusion only.

Drift is charge movement caused by an electric field. The velocities of electrons and holes are given by:

$$\begin{aligned} \vec{v}_e &= -\mu_e \vec{E} \\ \vec{v}_h &= \mu_h \vec{E}, \end{aligned} \tag{3.5}$$

where $\vec{E}$ is electric field; μ_e and μ_h are mobilities of electron and hole, respectively. A strong electric field and large mobilities realize fast charge collection.

A collision occurs every 25 ns at the interaction point of the ATLAS detector. All the signal charges produced by particles in a collision must be collected before the next collision occurs, namely, fast charge collection is required. Figure 3.5 shows simulated charge collection in 25 ns mainly by drift and diffusion. The percentage of signal charges collected in 25 ns is only 60 % when the sensor is not fully depleted, whereas a charge collection efficiency of almost 100 % is expected when the charges are collected by drift. Therefore, signal charges in the ATLAS ITk Pixel Detector should be collected by drift, and this motivates the development of "D(epleted)"MAPS.

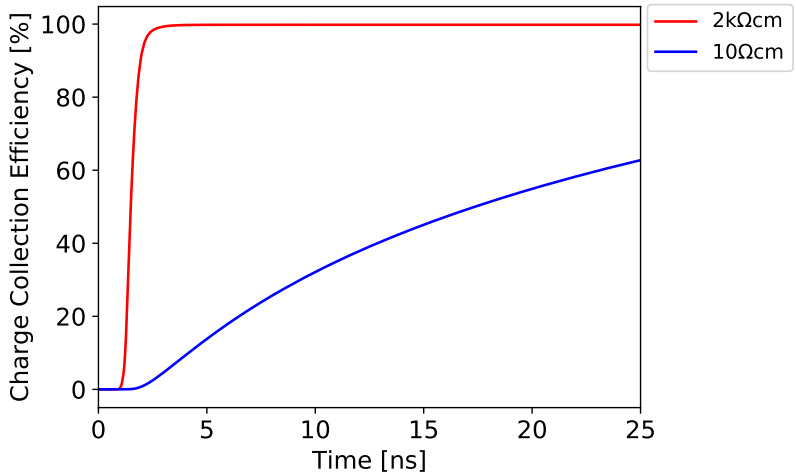


Figure 3.5: Simulated charge collection mainly by drift(red) and diffusion (blue). The collection node of the simulated sensor is n-type and segmented in one direction with a pitch of 20 µm and node width is 3 µm (collection node fill factor of 15 %). The simulation are performed with the bias voltage of 20 V on p-type wafers of 2 kΩ cm and 10 Ω cm. The sensor thickness is 18 µm for both cases and 1490 e-h pairs are generated. The data was take from [50].

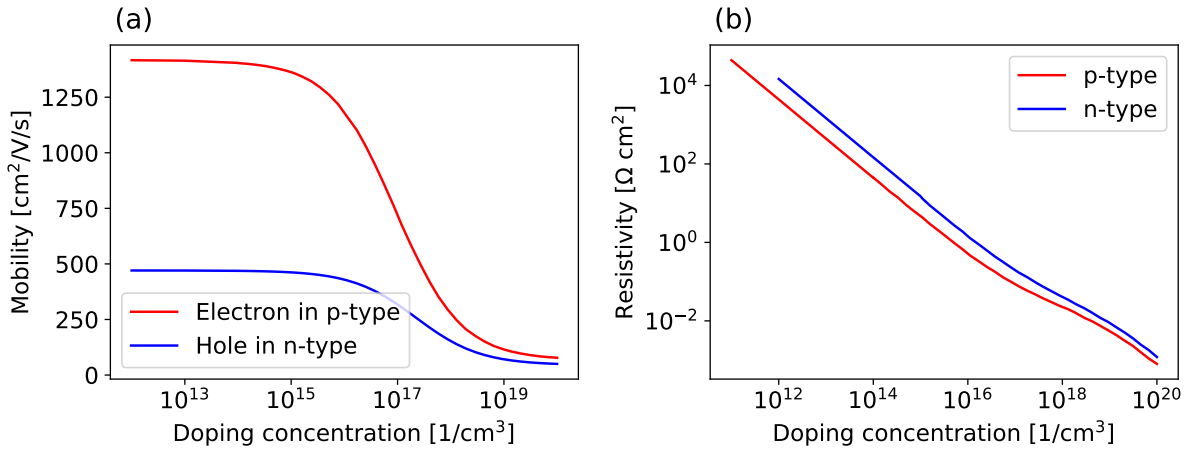


Figure 3.6: (a) Mobilities of electron and hole as minor carrier and (b) resistivity versus doping concentration for silicon. Data was taken from [49].

μ_e is empirically expressed as follows [49, 51]:

$$\mu_e = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + ((N_A + N_D)/N_r)^{\alpha}}, \tag{3.6}$$

where μ_{max}, μ_{min}, N_r, and α are fitted parameters. They are shown in Table 3.1 The empirical expression of μ_h is omitted because it is similar to that of μ_e. Figure 3.6 (a) shows electron and holes mobilities for different doping concentrations. μ_e and μ_h are 1 416 and 425 $\mathrm{cm}^2/\mathrm{V/s}$ when the doping concentration is lower than $1 \times 10^{16}/\mathrm{cm}^3$. The p-type sensor is preferred for the fast charge collection because the minor carrier of p-type sensor is electron and μ_e is a factor of 3 larger than μ_h.

The resistivity (Figure 3.6 (b)) is defined by μ_e and μ_p as follows:

$$\rho = \frac{1}{e(N_D\mu_n + N_A\mu_p)}. \tag{3.7}$$

If the wafer resistivity is 10 Ω cm or higher, the velocities of signal charges depend only on $\vec{E}$. Applying a strong electric field to the sensor is important for fast charge collection.

3.2.4 Depletion of silicon sensor

A p-n junction yields an electric field inside the semiconductor. Figure 3.7 shows free carriers, space charge, electric field, and potential in a planner p-n junction [52]. Electrons from the n-type region and holes from the p-type region diffuse to the opposing side due to concentration gradient (Figure 3.7 (a)) and recombine with each other. Thus, space charge appears near the p-n junction (Figure 3.7 (b)) and this phenomenon called depletion. An electron and hole pair created in the depleted area moves toward the n-type and p-type un-depleted regions, respectively, by drift, due to the electric field in the depleted region (Figure 3.7 (c)).

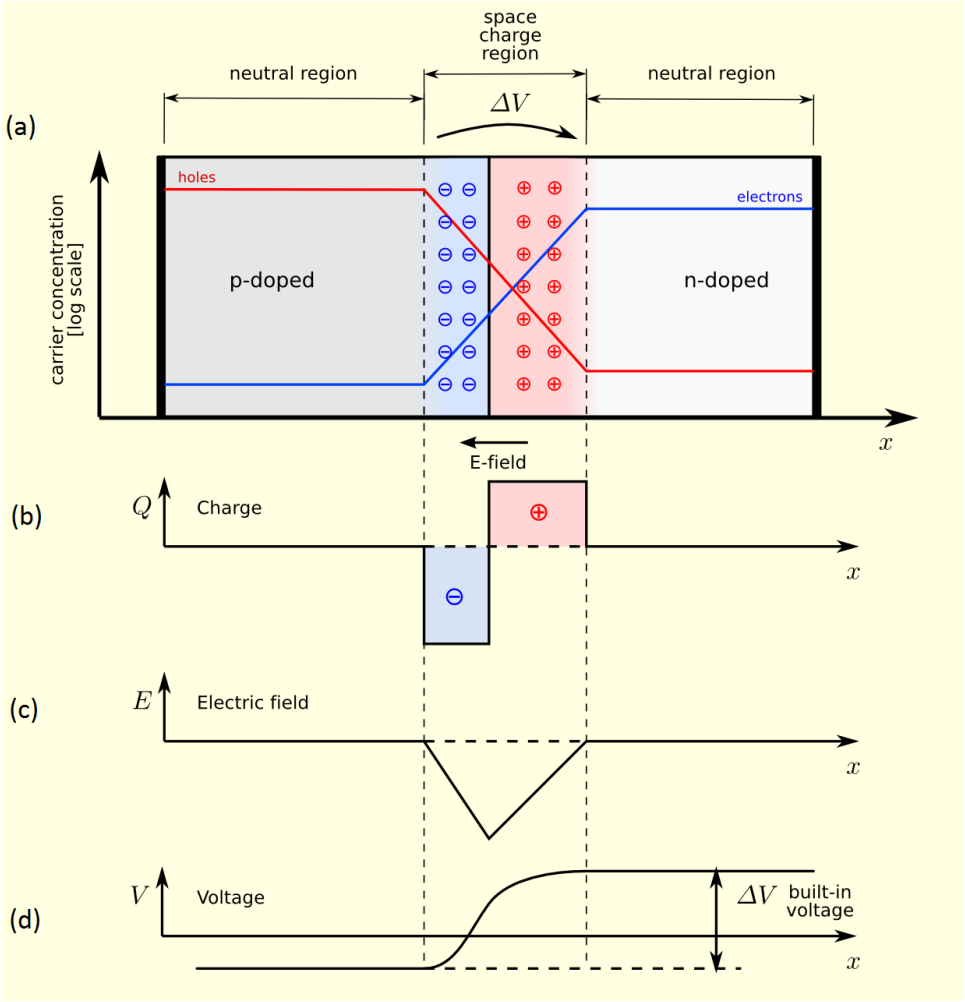


Figure 3.7: Distribution of (a) free carriers, (b) space charge, (c) electric field, and (d) potential at the p-n junction of the planner diode [52]

The potential between n-type and p-type silicon with doping concentrations of N_D and N_A, respectively, are expressed as:

$$V_{bi} = \frac{k_B T}{e} ln\left(\frac{N_D N_A}{n_i^2}\right), \tag{3.8}$$

where T is the sensor temperature, k_B is the Boltzmann constant, and n_i is intrinsic carrier concentration.

$$\begin{aligned} n_i &= 2\left(\frac{2\pi k_B T}{h^2}\right)^{2/3} (m_e^* m_h^*)^{3/4}\, exp\left(-\frac{E_g}{2k_B T}\right) \\ &= 5.2 \times 10^{15} \cdot T^{2/3} exp\left(-\frac{E_g}{2k_B T}\right) \\ &= 1.08 \times 10^{10} \quad [\mathrm{e^-/cm^3}] \ \text{at 300K}, \end{aligned} \tag{3.9}$$

where h is the Plank constant, and E_g is the band gap energy. Furthermore, m_e^* and m_h^* is the effective mass of an electron and hole, respectively. The values of m_e^*, m_h^*, and E_g for silicon are listed in Table 3.1. The potential difference between the n-type and p-type side (Figure 3.7 (c)) is V_{bi}.

The depletion area can be extended by applying a reverse bias voltage to the p-n junction. The depletion width of the planner p-n junction can be expressed as:

$$\begin{aligned} w &= \sqrt{\frac{2\epsilon_0\epsilon_{Si}}{e}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_b+V_{bi})} \\ &\approx 0.3\sqrt{\rho\ [\Omega\,\mathrm{cm}^2]\cdot V_b + 0.6\ [\mathrm{V}]} \quad [\mu\mathrm{m}], \end{aligned} \tag{3.10}$$

where V_b is externally applied reverse bias voltage, ϵ_0 is the vacuum permittivity, and ϵ_{Si} is the relative permittivity of silicon. The second expression in Equation (3.10) is the approximated depletion width for a p-type sensor. The N_D of n-type collection node is usually several orders of magnitude higher than the N_A of p-type sensor. In this case the depletion region extends mainly in the p-type sensor side. V_{bi} of typical p-n silicon diode is also approximated as 0.6 V at 300 K.

Figure 3.8 shows the depletion width in a planar p-type silicon sensor as a function of the reverse bias voltage in a material of varying resistivity. A high bias voltage and highly resistive wafer is important to obtain a sufficient depletion area in DMAPS. For example, a reverse bias voltage of about 55 V should be applied to a 2 kΩ cm wafer for a depleted depth of 100 µm to be obtained.

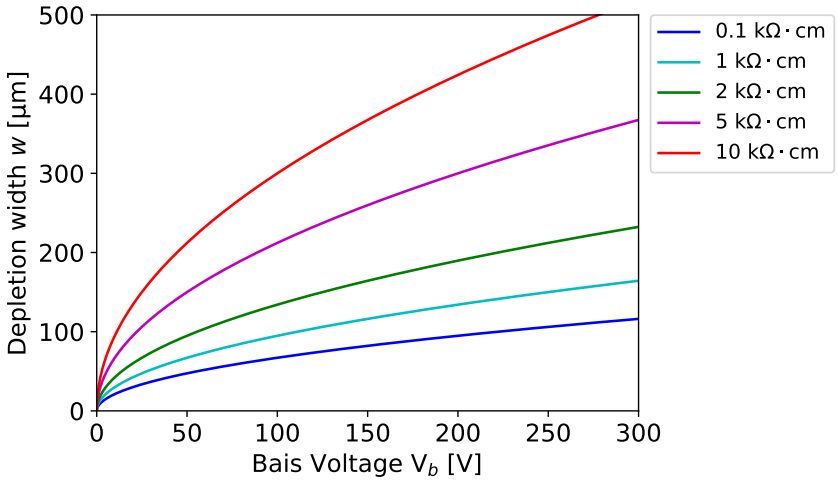


Figure 3.8: The depth of the depletion area of planner p-type silicon sensor of various resistivities. The curves are calculated from Equation (3.10).

As shown in Figure 3.9 (a), the electric field in the depletion region has a triangular profile up to the depletion voltage, V_d, where w equals the thickness of the sensor, d [53]. Increasing V_b beyound V_d increases the electric field uniformly. The electric filed inside the depleted region

can be written as:

$$E(x) = \begin{cases} \dfrac{2(V_b + V_{bi})}{w}\left(1 - \dfrac{x}{w}\right), & V_b \leq V_d \\ \dfrac{2(V_b + V_{bi})}{d}\left(1 - \dfrac{x}{d}\right) + \dfrac{V_b - (V_d + V_{bi})}{d}, & V_b > V_d, \end{cases} \tag{3.11}$$

where

$$V_d = \frac{eN_A w^2}{2\epsilon} - V_{bi},$$

and x is distance from the p-n junction. The strong field is obtained if a thin sensor is over-depleted.

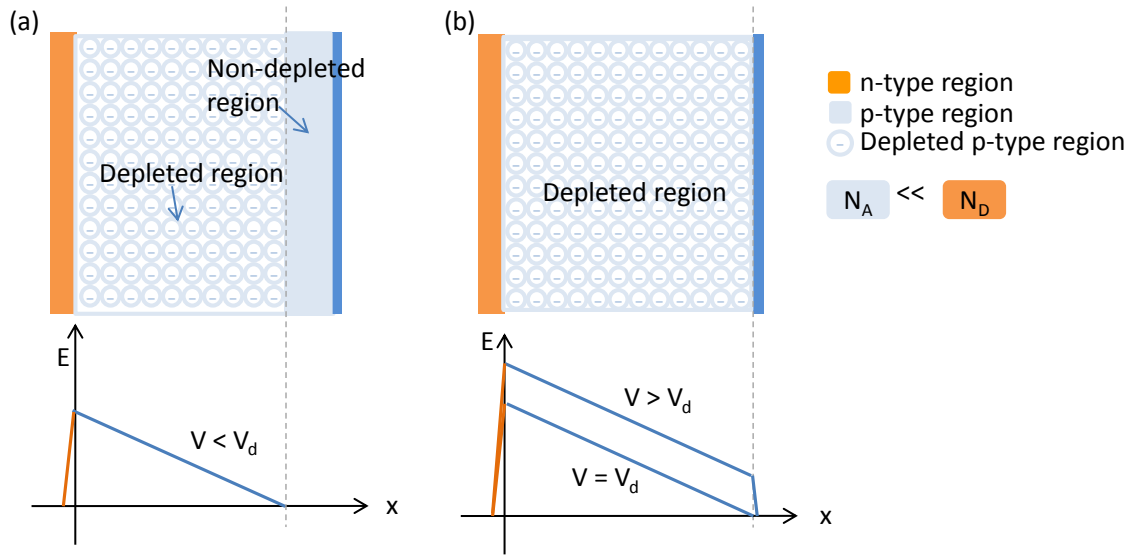


Figure 3.9: Electric field inside the (a) partially depleted and (b) fully deplete p-type sensor. When the sensor is over-depleted, the electric field is increased uniformly due to the voltage higher than the depletion voltage, V_d.

From the perspective of depletion width and strength of the electric field, a high bias voltage is desirable. However, breakdown occurs when the electric field is too strong. When the reverse bias voltage exceeds the breakdown voltage, a large current flows between the p-n junction. Thus, the breakdown voltage limits the possible bais voltage. The breakdown voltage depends on the structure of the p-n junction and wafer properties. The DMAPS breakdown voltage should be characterized by measurements.

3.3 Collection nodes

3.3.1 Signal current at a collection node and charge sharing

The electric current induced by a charge moving in the depleted region is expressed as follows:

$$i_s(t) = \sum_i^N e_i \vec{v_i}(t) \cdot \vec{E_w}(t), \tag{3.12}$$

where e_i is the charge of a carrier i, $\vec{v_i}$ is its velocity, and $\vec{E_w}$ is the weighting field of the Shockley–Ramo theorem [54, 55]. The total signal charge emerged on the collection node can be written as follows:

$$Q = \int_0^T i_s(t)dt, \tag{3.13}$$

where T is the integration time.d

The signal emerges on the collection node soon after the electron-hole pair starts moving towards the collection node.

The collection node of pixel detectors are segmented into two directions. When an particle is injected between two nodes (Figure 3.10 (a)) the signal is split into two, and detected by two pixel nodes because the created charges diffuse while charges are drifting toward the collection nodes. This phenomenon is called charge sharing, and the charge seen in each pixel becomes small if charge sharing occurs. The response of two pixels form a cluster of the signals which corresponds to the particle. The charge sharing also occurs when a particle trajectory is tilted (Figure 3.10 (b)).

Charge sharing at the corner of four pixels should be considered in the pixel detector. In the worst case, only one force of the full current emerges at each of the four collection nodes. The pixel whose signal is the largest among the responded pixels is called the seed pixel. If the readout electronics are not sensitive to the current at the seed pixel, an incident particle passing the corner of the pixels cannot be detected. In order to guarantee the hit efficiency, the readout electronics should be designed to be sensitive to at least the seed pixel.

The charge sharing should be considered when determining the sensor thickness. In both cases shown in Figure 3.10 (a) and (b), the charge sharing is more obvious in a thicker sensor. Charge sharing increases the actual hit rate in the pixel detector by a factor given by the average cluster size. The sensor should be thick enough to generate sufficient signal but should not be too thick, especially for the ATLAS ITk Pixel Detector, which is required to handle a high hit rate.

3.3.2 Fill factor of collection nodes

Figure 3.11 shows the cross sectional view of two different DMAPS designs. Figure 3.11 (a) has CMOS circuit inside the collection well and is isolated from the substrate. This design is called the "large-fill-factor" design since the fill factor of the collection well is high. The other possible design is shown in Figure 3.11 (b). This is the design used for the typical visible light

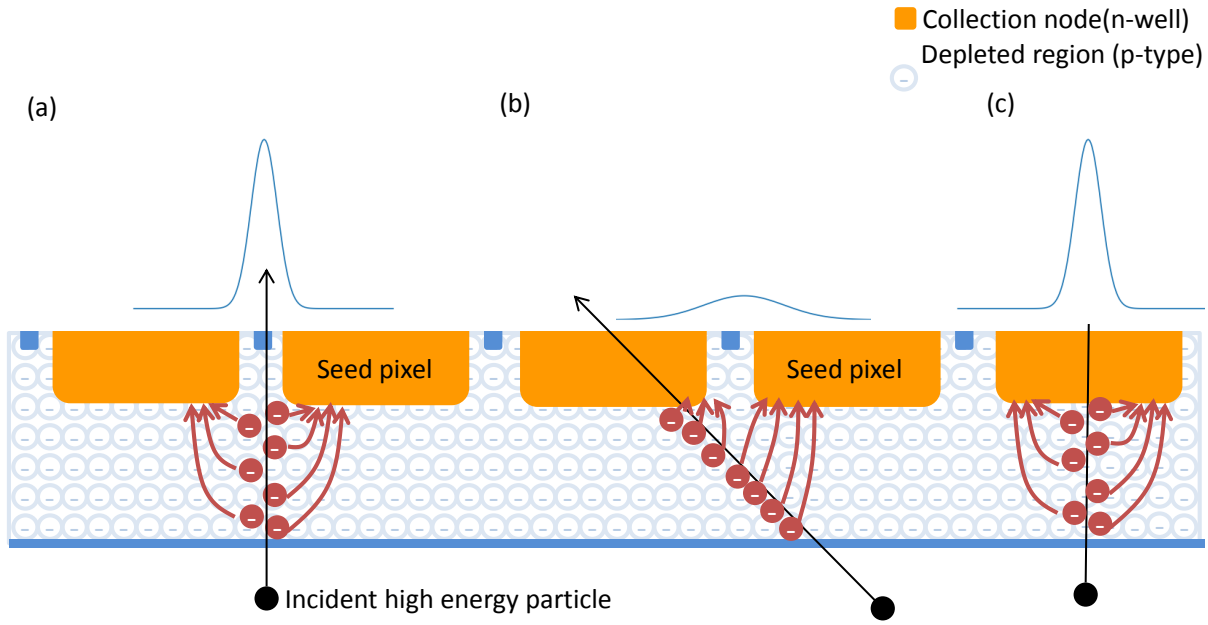


Figure 3.10: Charge sharing in a pixel detector when (a) an incident particle transverses between two nodes and (b) the particle trajectory is tilted. In (c), the charge sharing does not occur. The cluster size of (a) and 2, and that of (c) is 1. The blue curves indicate the distribution of the charge cloud near the collection nodes. Holes are also generated due to the high energy particle but they are omitted in the figure.

CMOS sensor. Collection nodes are placed between readout electronics. This design is called the "small-fill-factor" design. Note that the "fill factor" here is not the fill factor of the sensitive area. The detection efficiency of the pixel detector is required to be homogeneously close to 1 for high energy particle physics experiments.

This thesis mainly investigates the large-fill-factor design. The important advantages of the large-fill-factor DMAPS is that high voltage, (for instance, 100 V) can be applied to the substrate without damaging the CMOS circuit. This helps to create large depleted area and yield a strong electric field by over-depletion.

Another advantage of the large-fill-factor design is the small gap between the two collection nodes. The distance between the charge creation point and collection well is short even if the pixel size is large. On the other hand, the pixel size of the small-fill-factor DMAPS is limited because the long charge path causes inefficient charge collection, especially in the irradiated sensor (see Section 3.5.2).

Moreover, several CMOS foundries can fabricate large-fill-factor DMAPS. Various prototypes have been developed in multiple CMOS fabrication processes from different foundries [19, 56–59]. The collection well is needed to shield the readout electronics from high bias voltage, and readout electronics is needed to be implemented inside the well. Mandatory requirements for fabricating a large-fill-factor DMAPS is a high voltage tolerance and a multi-well CMOS process. CMOS processes with high voltage tolerance are commercially available due to

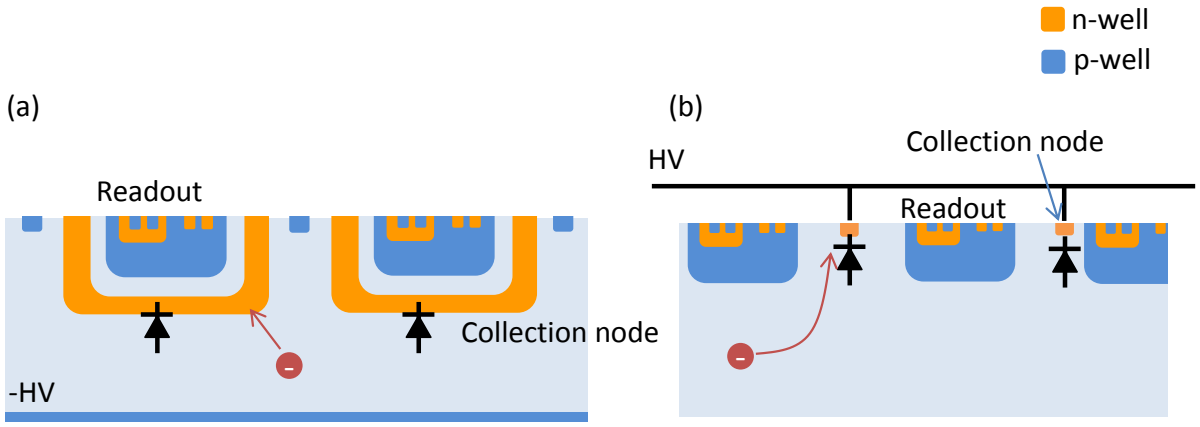


Figure 3.11: Cross section of two possible DMAPS designs. (a) is the large-fill-factor design, and the small-fill-factor design. The substrate (light blue) is p-type. The diode symbol indicates diodes formed by the reverse bias voltage.

automotive industry requirements. The multi-well process can be selected in many modern CMOS processes, and even 4-well CMOS processes are available. The 4-well CMOS process realizes NMOS and PMOS implementation which are isolated from the collection well. This helps to implement logic elements inside the collection well.

A disadvantage of the large-fill-factor design is that the parasitic detector capacitance is larger than that of the small-fill-factor design. Figure 3.12 displays the parasitic capacitance of the large-fill-factor DMAPS. The detector capacitance of a large-fill-factor DMAPS can be written as:

$$C_{det} = C_{sensor} + C_{interpixel} + C_{pw-bottom} + C_{pw-side}, \tag{3.14}$$

where C_{sensor} is the capacitance of the sensor diode and $C_{interpixel}$ is the parasitic capacitance between two neighboring collection wells. $C_{pw-bottom}$ and $C_{pw-side}$ are the parasitic capacitances between the collection well and the bottom and side of the p-well inside the collection well, respectively. The most dominant parasitic capacitance is $C_{pw-bottom}$ because the distance between the p-well and collection well is small, and the area is large [50]. The capacitance detector is typically 400 fF [60] for 50 µm × 250 µm pixel, which is larger than that of the hybrid detector ($\simeq$ 100 fF) [61]. The $C_{pw-bottom}$ and $C_{pw-side}$ directly couple to the collection node. Fluctuation of the p-well potential, which is usually the ground potential of the electronics, may cause false signal. Careful layout and low noise circuitry are needed to avoid cross coupling.

3.4 Readout electronics

3.4.1 Analog front-end circuit

Figure 3.13 shows the typical analog front-end circuit in a single pixel of a pixel detector when high hit rate capability is required. The signal waveforms at each point is shown in Figure 3.14. All DMAPS prototypes tested in this thesis have analog front-ends similar to Figure 3.13. The

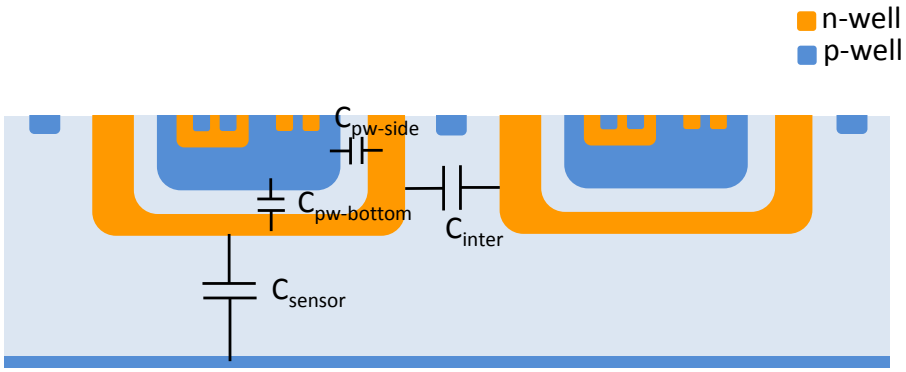


Figure 3.12: Detector capacitance of the large-fill-factor DMAPS. C_{sensor} is the capacitance of the sensor diode. C_{inter} is the parasitic capacitance between two neighboring collection wells. $C_{pw-bottom}$ and $C_{pw-side}$ are the parasitic capacitances between the collection well and the bottom and side of the p-well inside the collection well, respectively.

signal current induced in each segmented collection node is converted to a voltage signal in a charge sensitive amplifier (CSA). The CSA output is compared to a reference voltage, which defines the threshold. Then, a discriminator produces a digital square signal.

In addition, a test pulse input and a capacitor is usually implemented parallel to the sensor diode for calibration. When a voltage pulse is injected to the input port, a current induced at the input of CSA through the C_{inj}. This can simulate particle hits electrically, and hence, the readout electronics can be tested without particles.

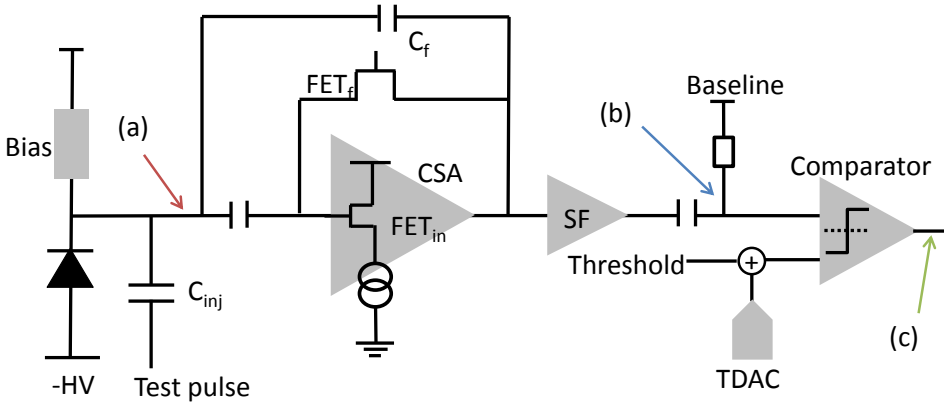


Figure 3.13: Block diagram of the typical analog front-end circuit in a pixel. The signal current is converted to voltage by the CSA and digitized by the discriminator.

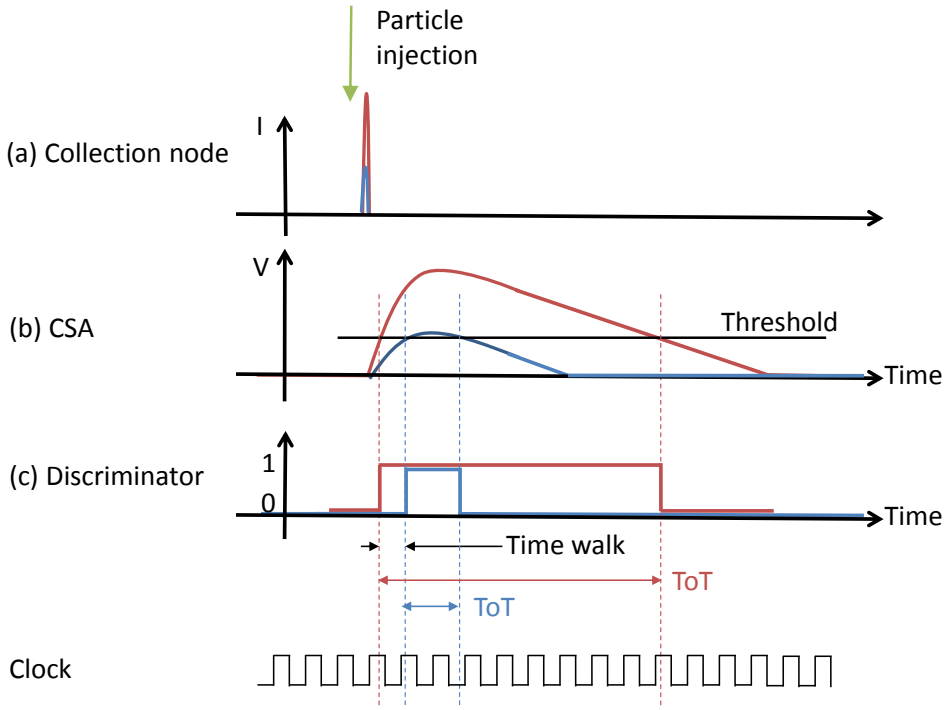


Figure 3.14: Drawing of signal waveforms at (a), (b), and (c) in Figure 3.13. Waveforms of the readout clock are also shown below (c). The blue and red lines describe the waveforms when the signals are large and small, respectively. The ToTs and time walk of the readout is indicated in (c).

3.4.2 Time walk

The waveforms at CSA and discriminator output of the two different signal amplitudes are shown in Figure 3.14 (2) and (3), respectively. The discriminator responds earlier when the signal is larger. The fluctuation of the latency between particle injection and signal detection in readout electronics is called time walk. The time walk of DMAPS must be smaller than the LHC's collision interval time of 25 ns.

The CSA rise time is a function of the input transconductance (g_m) and C_{det} as follows:

$$\tau_r = \frac{1}{g_m}\frac{C_{det}}{C_f}, \tag{3.15}$$

where C_f is the feedback capacitance of the CSA indicated in Figure 3.13. As Equation (3.15) shows, one of the disadvantages of large-fill-factor design is that it requires large g_m for fast τ_r, because the C_{det} of the design is large, resulting in increased power consumption.

The actual time walk also depends on the waveform of the CSA output near its peak and the discriminator response time. The details of the CSA and discriminator's architecture affects the time walk.

3.4.3 Equivalent noise charge

Equivalent noise charge (ENC) is introduced to evaluate readout noise. The ENC is defined as follows:

$$\mathrm{ENC} = \frac{\sigma_{rms}}{v_o}, \tag{3.16}$$

where σ_{rms} is the root mean square of the signal output voltage fluctuation, and v_0 is the signal output voltage for the input charge of one electron. ENC indicates the readout noise in units of electron charge. The ENC of the analog front-end circuit shown in Figure 3.13 is a combination of different noise sources. It is expressed as follows:

$$\mathrm{ENC}^2 = \mathrm{ENC}^2_{themal} + \mathrm{ENC}^2_{1/f} + \mathrm{ENC}^2_{shot}, \tag{3.17}$$

where $\mathrm{ENC}_{thermal}$ is the thermal noise in the transistor channel, $\mathrm{ENC}_{1/f}$ is the $1/f$ noise, and ENC_{shot} is related to the fluctuation of charge carrier creation. They are the three sources of CSA noise.

$\mathrm{ENC}_{thermal}$ is the most dominant noise source among the three. It depends on C_{det} as follows:

$$\mathrm{ENC}^2_{themal} \propto \frac{3}{4}\frac{kT}{g_m}\frac{C^2_{det}}{\tau_r}. \tag{3.18}$$

Large g_m is necessary to accomplish the required ENC with the large C_{det} collection node. The $\mathrm{ENC}_{1/f}$ of a typical CSA is inversely proportional to the square root of its input transistor size and can be reduced by using the appropriate input transistor size. In most cases, it is negligible compared to ENC_{themal}.

Another noise source that should be discussed here is shot noise. In addition to the signal charge generation, electron-hole pairs are generated in the sensor diode when electrons in silicon atoms are excited thermally. This causes the shot noise and it has a white spectrum and the CSA filters the noise according to its band width. The electron-hole pairs generation is microscopically observed as leakage current of the sensor diode, I_{leak}. The shot noise is approximated as follows [9]:

$$\mathrm{ENC}_{shot} = 56\sqrt{I_{leak}[\mathrm{nA}] \cdot \tau_f[\mu\mathrm{s}]} \quad [\mathrm{e}^-], \tag{3.19}$$

where τ_f is the fall time of the CSA. The temperature dependence can be expressed as follows [9]:

$$I_{leak} \propto T^2 e^{-\frac{E_g}{2kT}}. \tag{3.20}$$

Since leakage current decreases exponentially by lowering the sensor temperature, cooling of the sensor can keep the ENC_{shot} lower than $\mathrm{ENC}_{thermal}$.

3.4.4 Discriminator threshold

The discriminator threshold is an important value for the analog front-end circuit shown in Figure 3.13. The discriminator outputs a state of "1" only when the CSA output voltage exceeds

the threshold voltage (Figure 3.14 (3)). The discriminator distinguishes a signal from the noise and digitizes it.

If the threshold is too low, the discriminator counts a noise voltage as a signal. The minimum threshold voltage is derived from the allowed noise occupancy. Since the amount of charge created by a particle has the distribution shown in Equation (3.1) and some of signal charges are shared between multiple pixels, the charge collected by a pixel is sometimes smaller than MPV. The threshold of the discriminators must be set to several factors lower than the MPV, otherwise, the discriminator cannot detect some of the particles, causing an inefficiency of DMAPS. The maximum threshold is derived from the MPV and the required hit efficiency.

The gain and noise of the CSA in each pixel are not identical to those of other pixels, even if the CSAs have identical schematics and layout, because of the inherent fluctuation in the CMOS process and wafer properties. The baseline voltage of the CSA output and the threshold voltage at the inputs of the discriminator in each pixel are also not identical. Thus, the noise occupancy differs from pixel to pixel, even if a baseline and threshold voltage are globally distributed to all pixels in the chip.

In order to attain uniform noise occupancy by setting an optimum threshold for each pixel, the discriminator has a digital-to-analog converter (DAC), namely trim DAC (TDAC). TDAC adds an offset to the global threshold voltage at the discriminator of each pixel. The thresholds can be tuned for uniform noise occupancy by setting the TDAC value individually in each pixel [62].

The uniformity of the tuned threshold is a function of the voltage step given by TDAC, and the optimum voltage step is a function of the original threshold distribution and the number of bits in the TDAC. If the threshold distribution follows the Gaussian function, and more than 99.9 % (=$2 \cdot 3.1\sigma$) of the pixels in a chip is needed to be tuned, the tuned threshold range will be:

$$\sigma_{tuned-threshold} = \frac{2 \cdot 3.1 \cdot \sigma_{threshold}}{2^{n_{\mathrm{TDAC}}}}, \tag{3.21}$$

where and n_{TDAC} is the number of TDAC bits and $\sigma_{threshold}$ is the original threshold dispersion. If the threshold is $5 \cdot \mathrm{ENC}$ or higher to fulfill the noise occupancy requirement, the lowest threshold can be ideally estimated as follows:

$$th = \sqrt{(5 \cdot \mathrm{ENC})^2 + \sigma^2_{tuned-threshold}}, \tag{3.22}$$

The n_{TDAC} must be large enough that the $\sigma_{tuned-threshold}$ does not significantly increase the lowest threshold.

In the real chip, the voltage that corresponds to 1 bit of the TDAC also has a distribution, the TDAC tuning algorithm is not perfect, and ENC also has a distribution. The actual lowest threshold is usually larger than that calculated by Equation (3.22).

3.4.5 Time over threshold

The signal amplitude can be obtained from the width of the discriminator output. Figure 3.14 (c) shows outputs of the discriminator for small and large signals. Time over threshold (ToT) value is equal to the number of instances in which the discriminator's state is "1" and in which

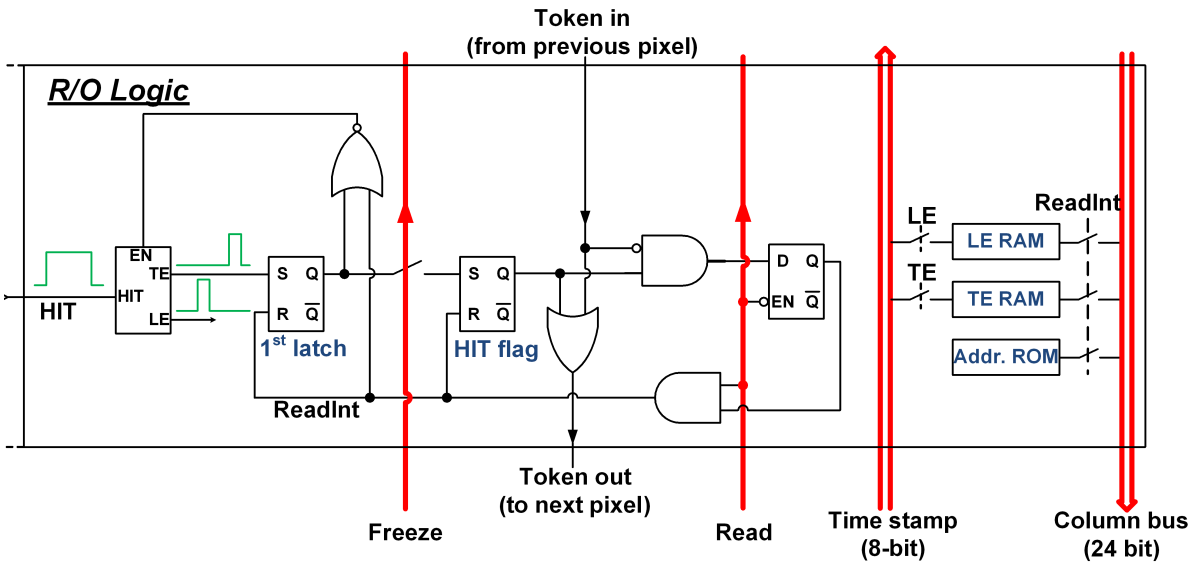


Figure 3.15: Block diagram of the column drain architecture that is employed in a DMAPS prototype [64].

the clock signal changes from "0" to "1". For example, the ToT value of the red pulse in Figure 3.14 (c) is 9 and that of the blue pulse is 1. Thus, the amplitude of the signal is digitized, and the frequency of the clock defines the amplitude resolution. The method of this digitization is called ToT.

The main usage of the ToT value in the ATLAS ITk Pixel Detector is the discrimination of small signals. When the hits of a small ToT value can be excluded from the signals, the effective threshold will be higher than the threshold of the discriminator but the time walk will be shortened since the small hit has a large delay and dominates the time walk. Furthermore, ToT value can be used for the time walk compensation. If the relation between the ToT value and the latency between the signal injection and discriminator response is calibrated, hit-arrival time can be corrected using the ToT value. The time walk compensation eases the requirement of τ_r and can save the power consumption, which is especially helpful for the large-fill-factor DMAPS.

3.4.6 Fast readout

The column drain architecture has been used in FE-I3, which is the original ATLAS ID Pixel Detector readout chips [63]. The block diagram of in-pixel logic is depicted in Figure 3.15 [64]. Column drain architecture can be used for the fast readout of DMAPS for ATLAS ITk Pixel Detector, since the hit rate requirement is similar to that of the current ALAS ID Pixel Detector.

3.4.7 CMOS fabrication process

The CMOS technology is used to implement the circuitry of the analog front-end (Figure 3.13) and the column drain architecture (Figure 3.15) in pixels. FE-I4, which is another one of the

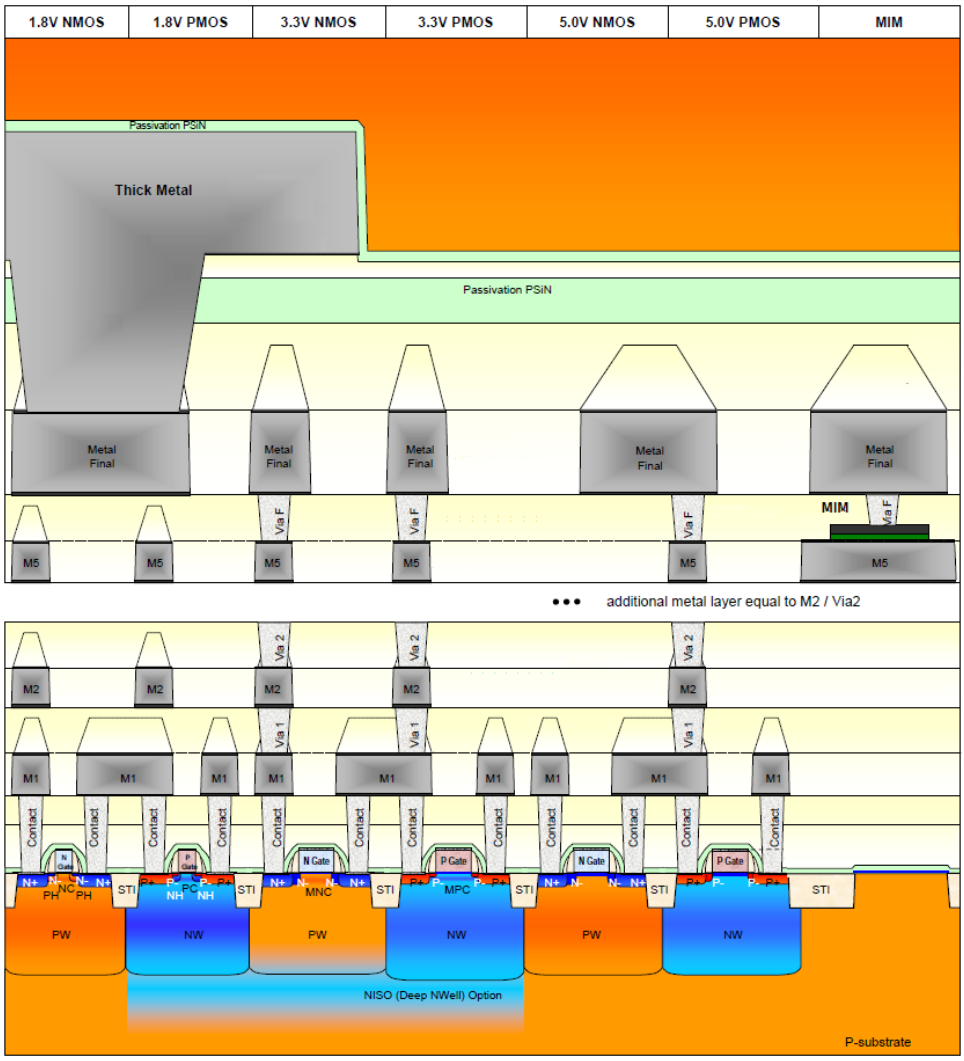


Figure 3.16: The cross section of the CMOS circuit fabricated by LFoundry 150 nm CMOS process [66]

two ATLAS ID Pixel Detector readout chips, was designed in a 130 nm feature size CMOS process [65]. The experience of FE-I4 suggests that the feature sizes of 130–180 nm is small enough to implement circuitry needed to handle the hit rate of 1 MHz/mm^2 in the pixel size of 50 µm × 250 µm, which is the pixel size of FE-I4.

Figure 3.16 illustrates a cross sectional view of a typical CMOS circuit [66]. MOS transistors are formed on the surface of p-type wafer and each component is connected using the metal layers and vias between them.

3.5 Radiation damages

Although there are many detailed studies on the radiation effect (e.g. [67–70]) in silicon sensor and readout electronics, this section only focuses on the phenomena that are especially important to DMAPS characterizations.

3.5.1 Surface damage

Surface damage occurs due to the charge buildup which is caused by ionization generated by photons and charged particles. Since the mobility of holes is six orders of magnitude lower than that of electrons in dielectric materials, positive space charge accumulates in the dielectric materials. CMOS circuits are affected by surface damage because there are many dielectric materials (e.g., gate oxide, shallow trench isolation (STI) oxide, and gate spacers shown in Figure 3.16) involved in modern CMOS process. CMOS structures, which mainly causes degradation of the readout electronics performances, differ from process to process [70].

In the CMOS circuits with the feature sizes 130–180 nm, commercial layout libraries are known to be usable at TID up to 250 Mrad [37, 71]. This is far beyond the requirement for the ATLAS ITk Pixel Detector. The commercial libraries consist of well-tested layouts of digital logic elements provided by CMOS fabrication companies, and designers can save time for the layout. CMOS processes with the feature size range of 130–180 nm suit for the DMAPS fabrication when DMAPS are required the TID hardness of 50 Mrad.

To minimize the degradation of analog front-end performance, in contrast to digital logics, it is necessary to consider the layout of the CMOS circuit. In the CMOS feature size range of 130–180 nm, gate oxides are only a few nanometers thick. Ionized charges can tunnel through the gate oxide and, as a result, will not accumulate. In contrast, the thickness of the STI layer is a few hundred nanometers thick and positive charges will accumulate in the STI region. Figure 3.17 (a) shows a layout of a typical linear transistor, i.e. a standard MOS transistor. Parasitic channels are created at the edges of the linear transistor because radiation-induced space charges in the STI region near the source and drain nodes (indicated with red symbols in Figure 3.17 (a)) result in an electric field at the edges of the MOS transistor. The current between the drain and source nodes is increased by the parasitic channels. They also cause threshold shifts of the transistor.

To mitigate the parasitic channels, the size of the transistor can be increased. When the width of the linear transistor is large enough, the increase in the leakage current from the parasitic channels can be ignored. Another solution is using an enclosed layout transistor (ELT) [72], which is shown in Figure 3.17 (b). There is no current path from the source node to drain in the ELT because the source node does not interface with STI. However, an ELT occupies more area than the standard linear transistor. Only transistors that are sensitive to the radiation-induced parasitic channels should be implemented as ELTs.

Moreover, the charge buildup induces additional leakage current in the DMAPS sensor diode and alters the electric field inside the sensitive volume. Thus, the breakdown voltage is affected. This effect depends on the geometry of the sensor diode, properties of the wafer, and the CMOS process used to fabricate the p-n junction.

3.5.2 Bulk damage

In the HL-LHC environment, many types of particles, including non-charged particles, pass through the DMAPS. Elastic scatterings and nuclear reactions sometimes occur between the traversing particle and the nucleus of the silicon crystal in DMAPS. For certain probabilities, an atom in the silicon crystal is displaced from the crystal lattice, and an interstitial atom and

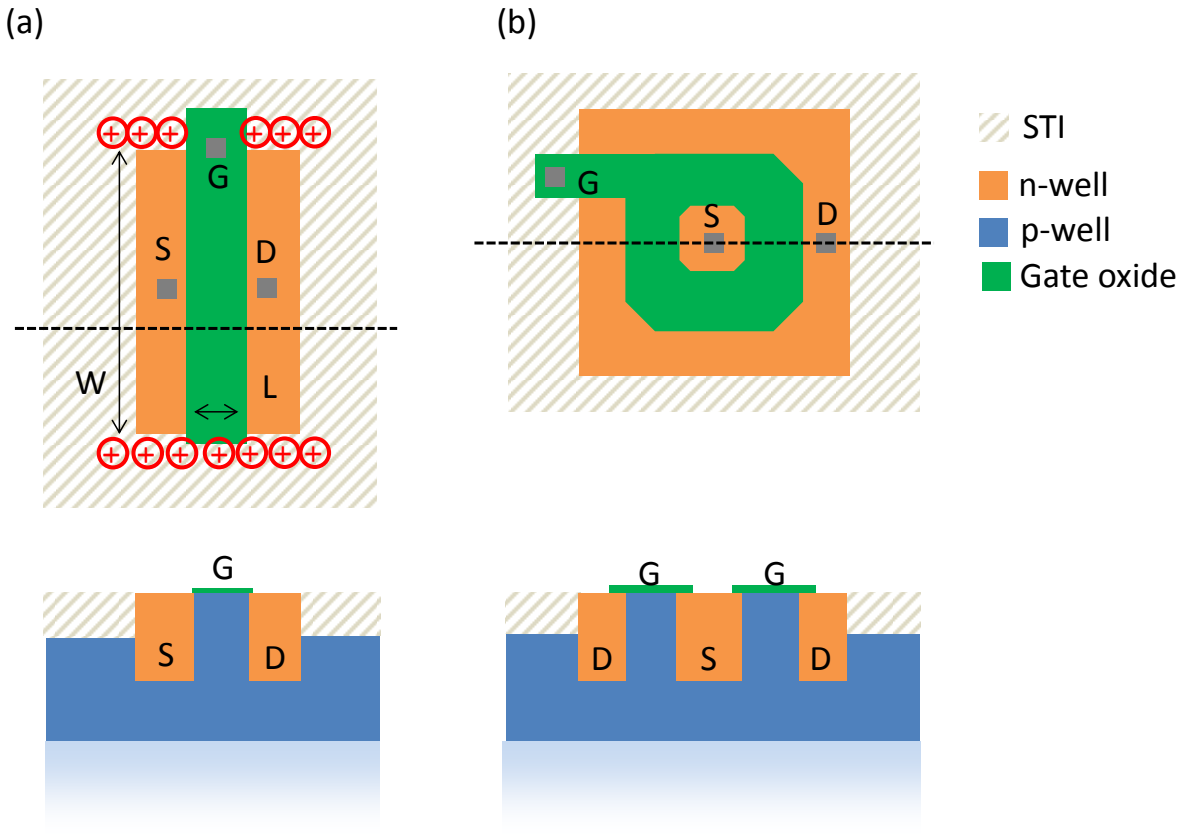


Figure 3.17: Layout of (a) an NMOS linear transistor and (b) an NMOS ELT. A corresponding cross sectional view across the dashed lines are shown below each layout. Drain, source, and gate terminals are indicated as D, S, and G, respectively. The arrows marked W and L indicate the width and length of the linear transistor, respectively. The positive charge buildup that causes parasitic channels are indicated by the red symbols.

vacancy pair is created at the lattice. This distortion of the crystal lattice is a unit of the bulk damage. As briefly mentioned in Section 2.2, the probability of the displacement, is known to be dependent on the type and energy of the traversing particle [31].

Figure 3.18 shows the displacement damage functions normalized to 95 MeV mb [67]. Due to this normalization, y-axis shows the displacement damage equivalent to the 1 MeV neutron. The type and energy of the particles in an environment used for the irradiation test are not equal to those in the HL-LHC. In order to estimate the radiation hardness of DMAPS in HL-LHC environment from the irradiation test results, a scaling parameter, hardness factor (κ), can be introduced. The amount of NIEL radiation can be expressed by κ as follows:

$$\text{NIEL} = \sum_i \kappa_i \int \phi_i(E)\, dE, \tag{3.23}$$

where κ_i and ϕ_i are the hardness factor and energy spectrum of particle i, respectively. The κ_i

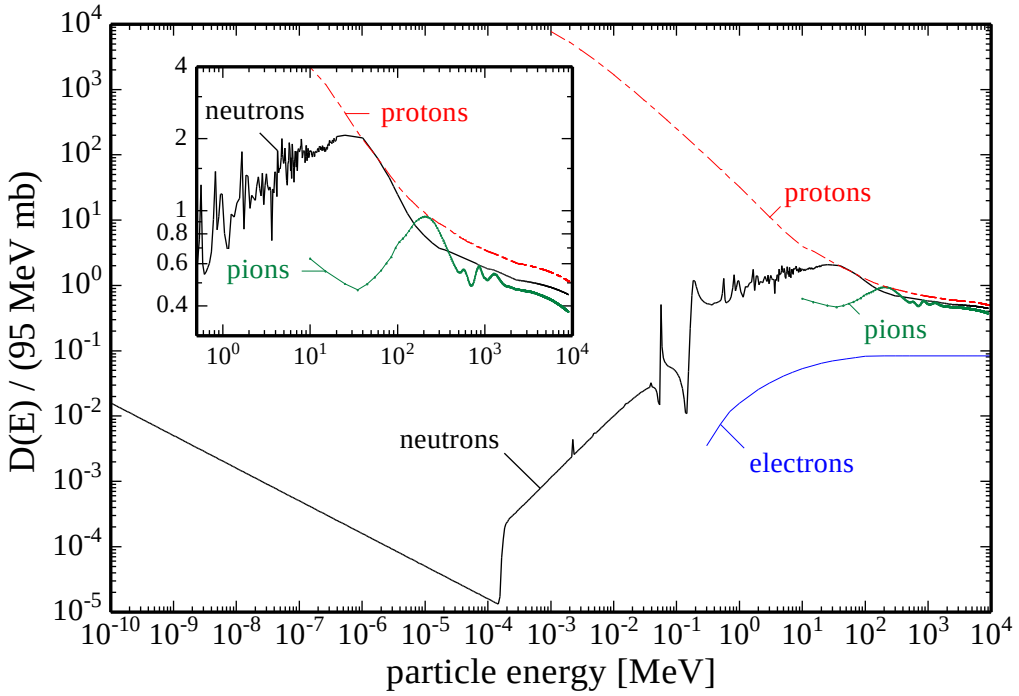


Figure 3.18: Displacement damage functions normalized to 95 MeV mb. [67]

can be defined as follows:

$$\kappa_i = \frac{1}{D_{neutron}(1MeV)} \cdot \frac{\int D_i(E)\,\phi_i(E)\,dE}{\int \phi_i(E)\,dE}, \tag{3.24}$$

where $D_i(E)$ is displacement damage cross section for particle i at energy E.

The distortion in silicon crystal produces additional states between the conduction and valence bands of the silicon sensor. Thus, effective doping concentration (N_{eff}) of the silicon sensor will be altered. Figure 3.19 shows N_{eff} variation due to the NIEL irradiation [73]. More accepter-like states tend to be formed. Thus, type inversion occurs in n-type silicon when the doping concentration is low.

The additional states close to the valence or conduction band capture signal charges and their release time constant is usually longer than the CSA rise time. The signal charges are "trapped" in those states will not be induce signal. The signal charges should be collected before the trapping occurs to avoid the decrease of charge collection efficiency. This can be realized by increasing bias voltage and shorten the gap between collection nodes. Figure 3.5 show the simulated signal charge in a p-type silicon sensor after NIEL irradiation of 1×10^{15} n_{eq}/cm^2 fluence [50]. The resistivities before the irradiation are 2 kΩ cm. The irradiation effect was modeled assuming the N_{eff} change shown in Figure 3.19. The simulation was performed for the cases when the sensor was partially (bias voltage of 1 V) and fully (bias voltage of 20 V) depleted. The sensor geometry and particle trajectory is equivalent to that in Section 3.2.3 except the size of collection nodes. The size of the collection node was set as 3 µm or 15 µm for

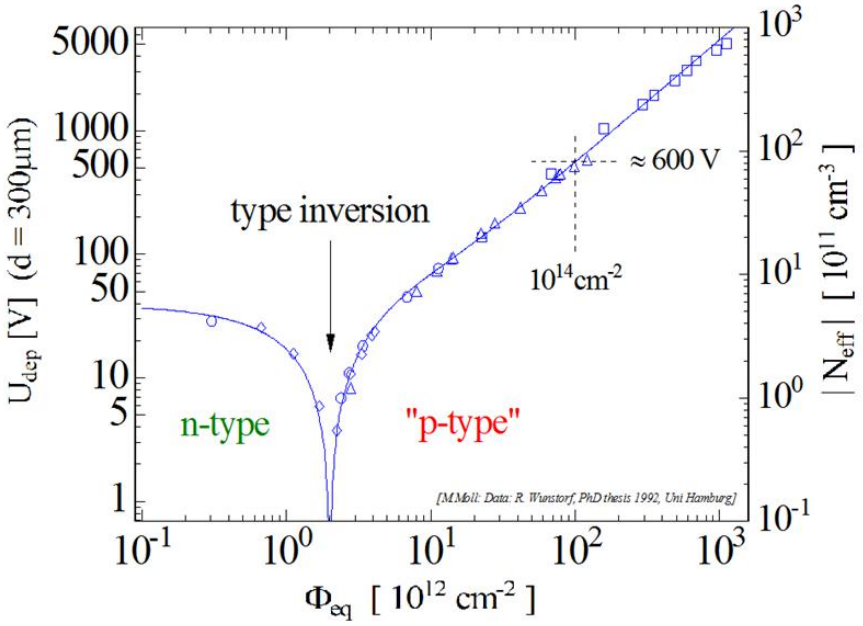


Figure 3.19: N_{eff} variation due to the NIEL radiation [67, 73].

each bias setting.

In all cases, the degradation of charge collection efficiency is expected. However, 79.8 % of the created charges are expected to be detected, even after the NIEL irradiation, when the bias voltage is high and the fill factor of the collection nodes are high, whereas only 11.5 % of the signal charges are expected to be detected when the bias voltage and the fill factor are low. As the simulation indicates, high voltage and small gaps between pixels are mandatory to maintain the signal amplitude.

Formation of mid-gap states leads an increase in the leakage current. It causes the increase of readout noise, because ENC_{shot} is proportional to the square root of the leakage current (Equation (3.19)). In addition, the leakage current heats the chip up, which increases the leakage current since it depends exponentially on the sensor temperature (Equation (3.20)). In this way, thermal run away can occur. However, the increase of leakage current can be suppressed by cooling the chip. Another phenomena is change of the breakdown voltage because N_{eff} affected the distribution of the space charge in the sensor. The breakdown voltage after irradiation should be obtained by measurements.

3.6 Summary of high hit-rate capable radiation hard DMAPS design

The design of the DMAPS discussed in this section is summarized as follows:

- Highly resistive sensor material results in adequately large depletion width.
- High breakdown voltage is also desired.

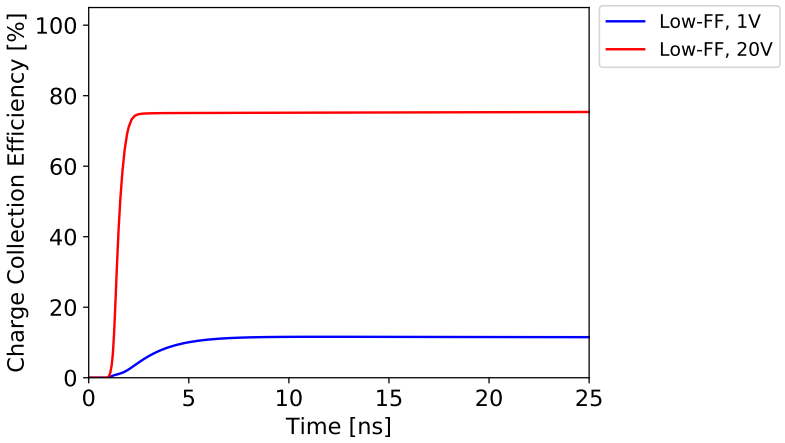


Figure 3.20: The simulated signal charge in a p-type silicon sensor after NIEL irradiation of 1×10^{15} n_{eq}/cm^2 fluence. The resistivities before the irradiation are 2 kΩ cm. The sensor geometry and particle trajectory is equivalent to that in Section 3.2.3 except the size of collection nodes. The size of the collection node set as 3 µm or 15 µm for each bias setting. The beam was injected between the two collection nodes, the pitch of which is 20 µm. The data was take from [50]

- The thickness of the sensor must be optimized with respect to the signal amplitude and cluster size (namely, hit rate). A strong electric field can be obtained by over-depleting a thinned sensor.
- A large-fill-factor design can lead to high radiation hardness because of the corresponding high voltage tolerance and the small gap between collection nodes. However, the detector capacitance for large-fill-factor design is large. Readout electronics must be carefully designed and should consider the cross coupling, ENC, and time walk.
- The column drain architecture should match the hit rate requirement. The feature size of 130–180 nm is small enough to include fast readout handling 1 kHz/mm^2 in 50 µm × 50 µm pixel.
- Although the 130–180 nm CMOS circuit with the radiation-hard option is expected to be TID hard, analog front-end must be tested after the irradiation.

CHAPTER 4

DMAPS prototypes

Three DMAPS prototypes, named CCPD_LF, LF-CPIX, and LF-Monopix, were characterized to discussed the suitability of the DMAPS as the ATLAS ITk Pixel Detector. They are all DMAPS prototypes fabricated on highly resistive wafers. The chapter starts with the details and feature of the CMOS process used for the prototype fabrication (Section 4.1). The specifications of the prototypes are presented in Section 4.2 and Section **??**. There are many variants of in-pixel readout electronics implemented in the prototype chips. In addition, several types of the sensing volume are designed for CCPD_LF and LF-CPIX. Only the variants used in the measurements are introduced in those section.

4.1 CMOS process for prototype fabrications

The 150 nm CMOS process offered by LFoundry [74] is selected because of the following features:

- The manufacture provides an option to use highly resistive wafers of Czochralski p-type with a the guaranteed resistivity of >2 kΩ cm,
- The n-wells implanted as the collection nodes has high voltage tolerance,
- Back-side thinning of wafer is allowed as a part of the fabrication process,
- The process is a 4-wells-process with 7 metal layers, allowing the NMOS and PMOS to be flexibly positioned inside the collection node, and
- It is a process with a small feature size of 150 nm.

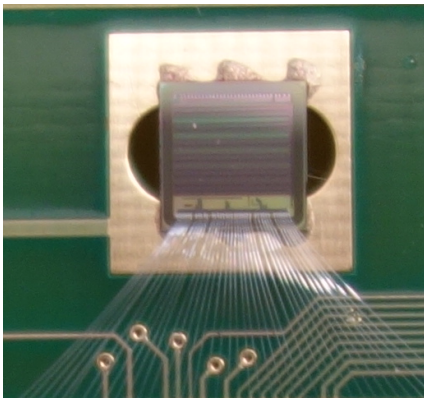
CCPD_LF, LF-CPIX, and LF-Monopix were fabricated using this process.

4.2 Specifications of the prototypes

4.2.1 CCPD_LF

CCPD_LF is the first large-fill-factor DMAPS on a highly resistive wafer. The main purposes of CCPD_LF is to test sensing and analog front-end performance of DMAPS. The specifications of CCPD_LF are shown in Table 4.1.

Table 4.1: Specifications of CCPD_LF.



Chip size	4.77 mm × 4.85 mm
Pxiel size	33.3 μm × 125 μm
Number of pixels	114 rows × 24 columns
Sensor structure	2 variants of collection node realized in separate chips Large-FF: standard large-fill-factor Small-FF: modified small-fill-factor (See Figure 4.2)
Analog front-end	3 types of CSA FET_f-S: 0.35 μm ×0.9 μm linear transistor FET_f-L: 0.35 μm ×1.5 μm linear transistor FET_f-ELT: ELT Discriminator w/ 4-bit TDAC
Fast readout	Coupled to FE-I4 with pixel en/decoding (Slow standalone readout is also possible)
Design	Uni. Bonn, CPPM, KIT
Submission date	Sep 2014

The actual DMAPS consists of many structures in addition to the pixelated collection wells; these structures are the p-stop, the end of row circuitry, the chip periphery, I/O pads, a bias

contact, and guard rings. Figure 4.1 (a) is a picture of a CCPD_LF chip imposed with of the layout of p- and n-well rings. Figure 4.1 (b) is a representative of an area near the edge of the chips. Nine p-well rings surround the whole chip and n-well ring surround each of the pixel matrices, the end of column circuitry, the periphery, and the test structures. The outermost p-well ring works as a bias contact for the sensor; it sets the electrical potential of the side edges and back side of the substrate. The other eight p-well rings and n-well rings function as guard rings. The guard rings are structures that protect the chip from high injection currents from the edge of the chip. The p-stop is a p-well implanted between the collection wells. It isolates each collection node, which is an n-well, from neighboring collection nodes. Without the p-stop, the diffusion of the donor implants of n-wells might create electrical shorts to the neighboring nodes.

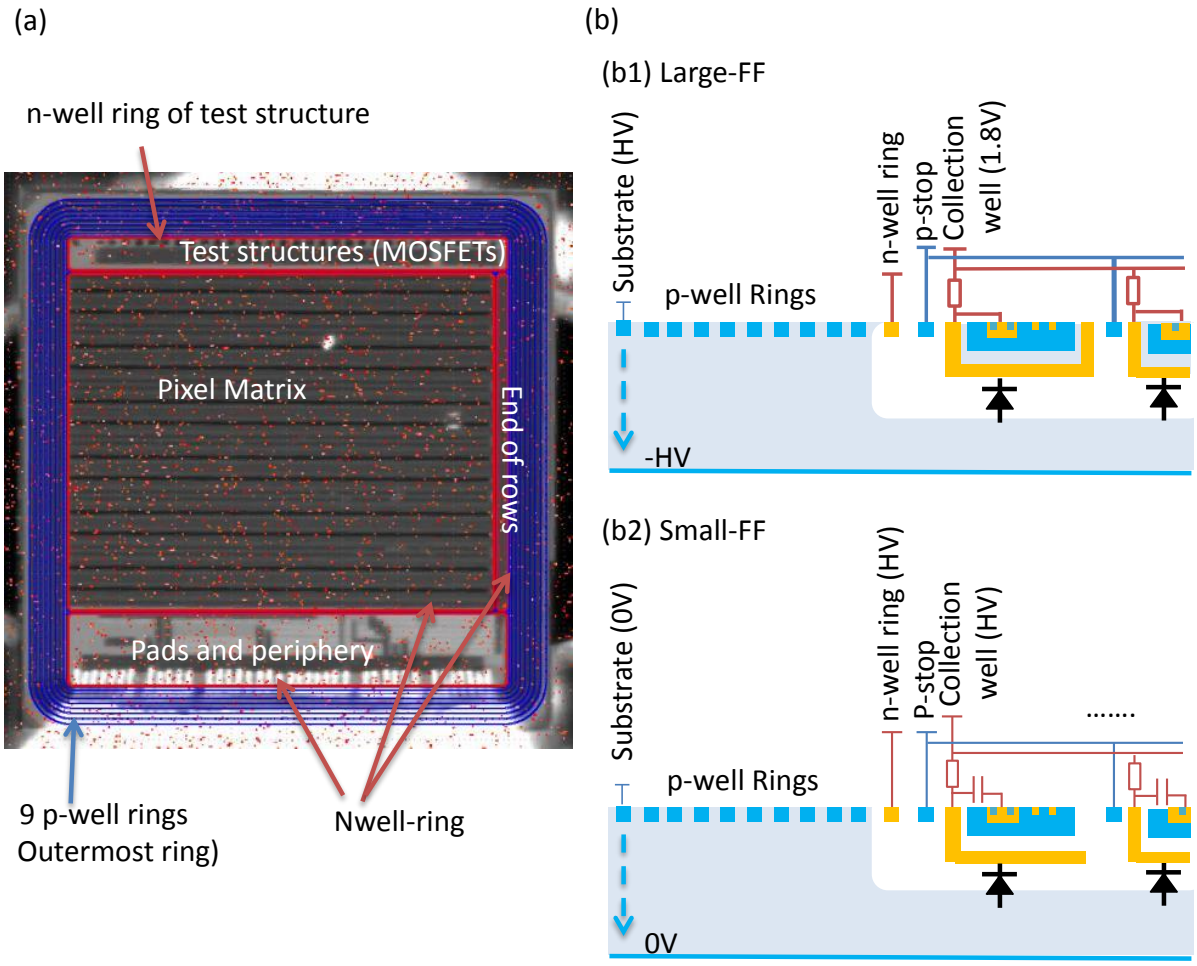


Figure 4.1: The (a) top view and (b) cross sectional schematic of CCPD_LF. A picture of CCPD_LF Large-FF is shown in (a). The p- and n-well rings are indicated in red and blue. (b1) and (b2) are simplified drawings of CCPD_LF Large-FF and Small-FF, respectively. The diode symbols indicate where pn-diodes are formed.

Two variants of CCPD_LF were realized in separate chips, namely Large-FF and Small-FF. Figure 4.2 shows a pixel from each variant. Figure 4.2 (a) and (b) show the illustrations of a pixel in Large-FF and Small-FF chips, respectively. Large-FF is a standard large-fill-factor DMAPS (Figure 4.2 (a)). As explained in Section 3.3.2, a high bias voltage can be applied to the substrate in this version, and the gap between the collection nodes is as small as 13 µm. However, the detector capacitance is large. The Small-FF is a modified small-fill-factor DMAPS (Figure 4.2 (b)). A bar structure is placed underneath the readout electronics as a part of the collection node. Due to the bar structure, the largest gaps between the collection nodes in Small-FF are as short as 26 µm, whereas the pixel pitch of the long side is 125 µm. The detector capacitance of Small-FF is expected to be smaller than that of Large-FF because the collection node partially covers the readout circuit. This results in small parasitic capacitance between the collection node and the p-well where the readout circuitry are implemented (indicated as $C_{pw-bottom}$ and $C_{pw-side}$ in Figure 3.12).

The disadvantage of the Small-FF is that the maximum bias voltage for CCPD_LF Small-FF is limited to 30 V. As readout electronics are placed on the p-type substrate, the potential of the substrate must be kept at 0 V. Hence, positive high voltage should be applied to the n-type collection wells so that a reverse bias voltage is applied between the substrate and the collection wells. The each collection well is alternating current (AC) coupled to the in-pixel CSA through a capacitor (indicated in Figure 4.1 (b2)). This capacitor's high voltage tolerance, which is 30 V for the Small-FF pixels, limits the bias voltage.

Another disadvantage is that only passive elements can be used to bias the collection electrode because of required high potential difference. A diode or resistor is the only choices for the biasing circuitry for Small-FF. In comparison, the Large-FF has a basing circuitry using PMOSs. The biasing circuitry optimizes the discharge of sensor even though the leakage current is increased by irradiation.

Pixel readout consists of a CSA, a discriminator with a 4-bit TDAC, a register (HIT register), and an output stage which modulates the height of the output pulse. Three types of pixels are implemented in a CCPD_LF Large-FF chip to test TID radiation hardness. They are named FET_f-S, FET_f-L, and FET_f-ELT. The feedback transistor (indicated as FET_f in Figure 3.13) in CSA is known to be sensitive to TID irradiation from previous work [75]. The feedback transistor in the FET_f-S type pixel is a linear transistor (Figure 3.17 (a)) with a length and width of 0.35 µm and 0.9 µm, respectively. The FET_f of the other two types have TID radiation-hard layouts. The feedback transistor in FET_f-ELT is an ELT (Figure 3.17 (b)), and the FET_f-L type pixel has a linear transistor, whose width is wider than that of the FET_f-S. The length and width are 0.35 µm and 1.5 µm, respectively.

The fast readout logic is not implemented in CCPD_LF. There are two options to obtain data from this chip. Using the HIT register is the first option. The HIT register in a pixel stores hit/no-hit binary information coming from the discriminators. All HIT registers in the pixel matrix are daisy chained and form a shift register. Thus, hit/no-hit information in the pixels can be read out by shifting out the bits in the shift register. In this readout option, only position of particles during the integration time (namely, time when the HIT resisters are able to accumulate signal from the discriminators) can be obtained and the timing information will not be obtained.

The second option is using another readout chip. The connection scheme is described in Figure 4.3. The pixel size of CCPD_LF and FE-I4 is 33.3 µm × 125 µm and 50 µm × 250 µm,

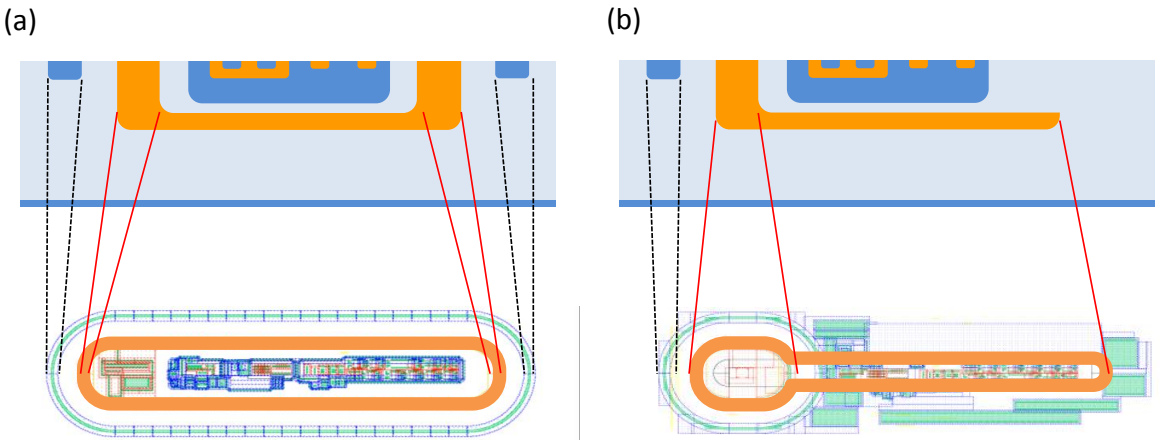


Figure 4.2: Cross sectional and top views of CCPD_LF (a) Large-FF and (b) Small-FF pixels. The top views show the actual layouts, and the cross sectional views are simplified drawings. Readout circuitry of Large-FF is isolated from the substrate. In Small-FF, the collection node is extended as a bar underneath the readout electronics to minimize the gap between the neighboring collection nodes.

respectively. The size of 2×3 CCPD_LF pixels equals that of 1×2 FE-I4 pixels, and those, namely, 6 CCPD_LF pixels and 2 FE-I4 pixels, form a unit of connections pattern. The output of three CCPD_LF pixels is summed and connected to one output pad. The pattern of the CCPD_LF output pads geometrically matches that of the FE-I4 bonding pads. With FE-I4 as a readout chip, CCPD_LF has the capability to test the DMAPS + R/O configuration. In contrast to HIT resister, FE-I4 can assign timestamp in 40 MHz to the hits detected in the CCPD_LF pixels.

The output stage in CCPD_LF encodes the pixel position in the three pixels connected to the same output pad. Figure 4.4 shows the block diagram of the connection between CCPD_LF and FE-I4 pixels. Hit information, namely the high status of the discriminator, from each of the three CCPD_LF pixels is modulated into three different amplitudes according to the pixel position. FE-I4 pixel has ToT circuitry and is used to decode the pixel position. The three different pulse heights can be distinguished by the ToT value of the FE-I4. In this way, the positions of the three pixels are encoded in CCPD_LF and decoded in FE-I4. Thus, the bump bonding pitch can be larger than the granularity of CCPD_LF. The feasibility of this concept was shown in the previous studies by decoding single-pixel hits (i.g. [76–78]). The range of ToT is from 1 to 14 [79]. The combination of the three different pulse heights is distinguished (only theoretically) by eight values. In the case of two (or three) pixels are forming a cluster and response at the same time, the output of LF-CPIX is a sum of two (or three) different pulse heights. Even in this case, the positions of the two (or three) pixels are possible to be decoded by the FE-I4 ToT circuit.

A pixel has a test pulse capacitor and two output ports for debugging and calibration purposes. The output ports are implemented at the output of the CSA and the output stage of each pixel (indicated as (1) and (2) in Figure 3.13, respectively). One can select one pixel and monitor

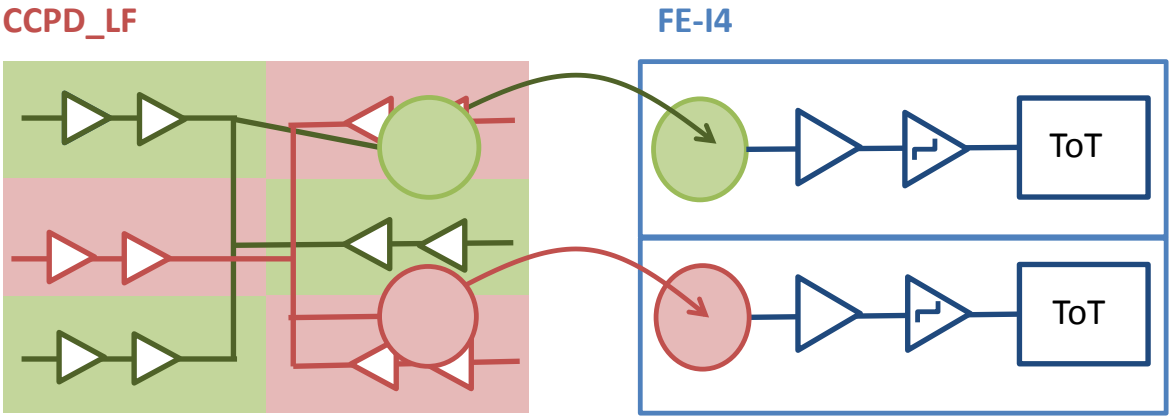


Figure 4.3: Connection scheme of a CCPD_LF + FE-I4 chip. A unit of connection pattern consists of 2 columns × 3 rows of CCPD_LF pixels and it is connected 1 column × 2 rows of FE-I4 pixels. The output of three CCPD_LF pixels is summed and connected to one pad and those of the other three pixels are connected to the other pad according to a chessboard pattern. The pattern of the CCPD_LF output pads geometrically matches that of the FE-I4 bonding pads.

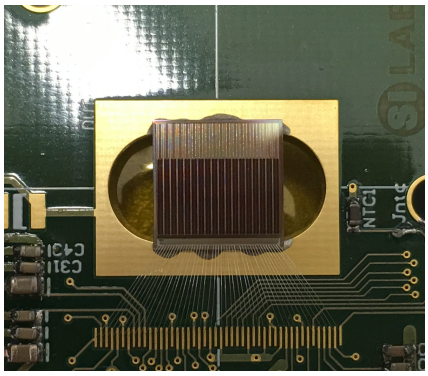
the signal waveforms inside the pixel via the output ports. The biases for the analog front end circuit are generated internally with global DACs in chip periphery. Optimization of analog front end circuity is possible using those DACs. The features listed in this paragraph are also iterated on LF-CPIX, LF-Monopix, and H35DEMO.

4.2.2 LF-CPIX

LF-CPIX is the second prototype chip, and its chip area is a factor of 4 larger than that of CCPD_LF. The sensor design and readout electronics are modified [80] regarding the characterization results of CCPD_LF [20] (see Chapter 6). LF-CPIX is meant for testing sensor and analog front-end properties in large chips. There are two variants of guard ring layout, named G-5.5 µm and G-10.5 µm. The details of the variants are explained in Section 6.1.1. The specifications of LF-CPIX are listed in Table 4.2. Similar to CCPD_LF, the pixel readout of LF-CPIX consists of a CSA, a discriminator with a 4-bit TDAC, a HIT register, an output stage, monitoring ports, and a test pulse capacitor.

Twelve types of pixels are implemented in the LF-CPIX [81]. They can be grouped into three according to their CSA type, and are named CSA_{in}-CMOS, CSA_{in}−PMOS, and CSA_{in}-NMOS. The layout of the feedback transistor in all types is identical to that of the FET_f-L in CCPD_LF, namely a 0.35 µm long and 1.5 µm wide linear transistor. Figure 4.5 shows the schematics of the input device (indicated as CSA_{in} in Figure 3.13) of the CSA in each type [81]. The input device of the CSA in CSA_{in}-CMOS consists of one NMOS transistor and one PMOS transistor, and its gain (expressed as g_m in Equation (3.15) and (3.18)) is the largest among the three types if the power consumption of three types is set to be the same. The CSA_{in}-PMOS has a PMOS transistor for the CSA input device. It has been tested in many previous DMAPS prototypes, including CCPD_LF, and is confirmed to have acceptable TID radiation hardness [18, 20] (see

Table 4.2: Specifications of LF-CPIX.



Chip size	G-5.5 µm: 9.84 mm ×9.49 mm G-10.5 µm: 9.53 mm ×9.49 mm
Pxiel size	50 µm ×250 µm
Number of active pixels	106 rows ×21 columns
Sensor structure	large-fill-factor design w/ 2 variants of guard rings realized in separated chips G-5.5 µm: Guard ring gap = 5.5 µm G-10.5 µm: Guard ring gap = 10.5 µm (See Figure 6.3)
Analog front-end	3 flavors of CSA, CSA_{in}-PMOS: Input device = PMOS + load transistor CSA_{in}-NMOS: Input device = NMOS + load transistor CSA_{in}-CMOS: Input device = PMOS and NMOS (See Figure 4.5) Discriminator w/ 4-bit TDAC
Fast readout	Coupled to FE-I4 with pixel en/decoding, (Slow standalone readout is also possible)
Design	Uni. Bonn, CPPM, Irfu
Submission date	Mar 2016

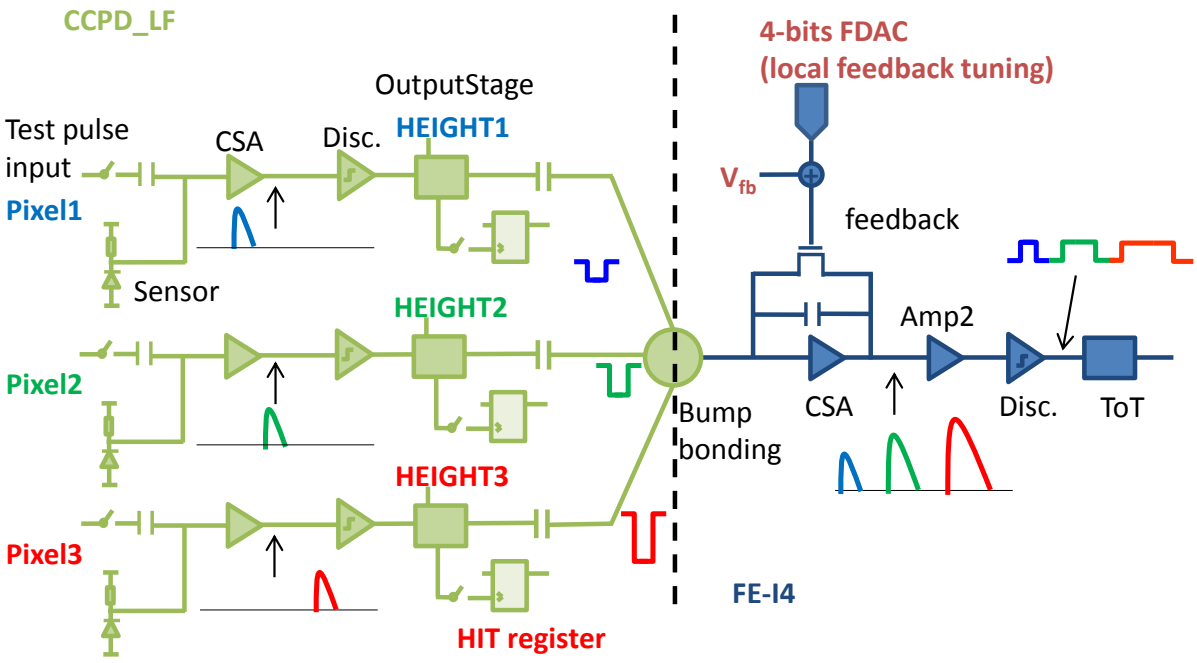


Figure 4.4: Pixel en/decoding scheme of CCPD_LF and FE-I4. The block diagram of readout electronics in CCPD_LF and FE-I4 is shown with a signal waveform at each point. Each color (blue, green, and red) of the waveform indicates each pixel. The output of three CCPD_LF pixels is connected to one FE-I4 pixel. A hit pulse from the discriminator is modulated to indicate the pixel position, and it is decoded in FE-I4 using the ToT value.

Chapter 6.5). The input device of CSA_{in}-NMOS is an NMOS transistor and complimentary to that of CSA_{in}-PMOS. It is implemented for a comparison.

Fast readout logic is also not implemented on LF-CPIX. The hit position can be obtained using the HIT registers. Each pixel has output pulse modulation circuitry and an output pad, and the geometrical pattern of the output pads matches to that of the bonding pads of FE-I4. The pixel size of LF-CPIX is 50 µm × 50 µm, which is 3 times larger than that of CCPD_LF and equal to that of FE-I4. One LF-CPIX pixel can be connected to one FE-I4 pixel. No pixel en/decoding scheme are implemented in this prototype.

4.2.3 LF-Monopix

LF-Monopix is a fully monolithic DMAPS prototype. The primary objective of this prototype development is to show the feasibility of DMAPS with many digital logic elements integrated inside pixels. The in-pixel readout also contains a CSA and a discriminator with a 4-bit TDAC. There are 18 variants of pixel readout, and the variants with a CSA identical to that in the LF-CPIX CSA_{in}-CMOS type pixel are tested in this thesis. Two discriminator designs are realized in those tested variants. One of them is identical to that of LF-CPIX, and its structure is the typical two-stage open loop. The pixel with a discriminator of this type is named D1.

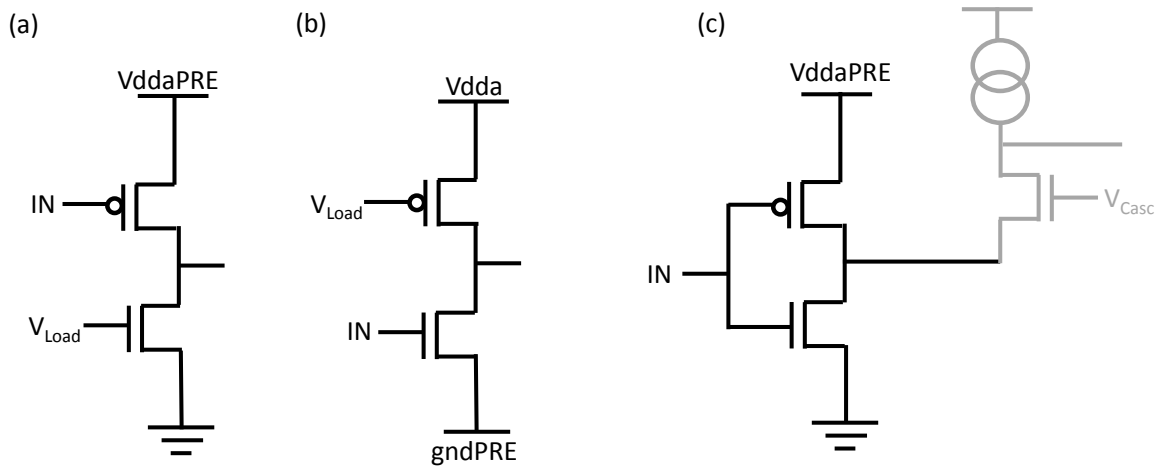
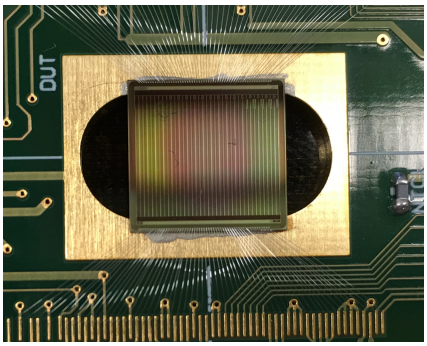


Figure 4.5: Schematic of the CSA input device of (a) CSA_{in}-PMOS, (b) CSA_{in}-NMOS, and (c) CSA_{in}-CMOS. The CSA_{in}-PMOS are based on a folded cascode PMOS-input common source preamplifier with a NMOS load transistor used to bias the input transistor [81], and CSA_{in}-NMOS is the complimentary version. CSA_{in}-CMOS has two input transistors. The circuitry following to the input device is common for the three types and are shown in gray in (c)

The other one is designed to reduce the time walk, and it consists of a self-biased differential amplifier followed by an inverter [64]. This type is named D2. The delay of the discriminator response is shortened, especially when the input signal (namely output of the CSA) pulse height is close to the threshold. Each pixel type consist of 4×129 pixels. In this thesis, D1 is mainly used for characterization because it is placed in the center of the LF-Monopix chip. When results are shown without the indication of the pixel type, the results are from D1 type pixels.

The in-pixel readout electronics of LF-CPIX contains fast readout logic in addition to the analog front-end circuitry. The column drain readout architecture (Figure 3.15) is adopted and carefully designed to avoid cross coupling between electronics and sensor [82]. A pixel sends its row-wise position in 8 bits and timestamps of leading and trailing edges of the discriminator in 8 bits each when it receives a signal. Then, periphery adds column-wise position in 6 bits and serialized data (30 bits in total) is send out from the chip. As a measure of the signal charge, the ToT value is calculated from the difference between the two timestamps outside the chip. The timestamp and readout clock frequencies were set to 40 MHz. The specifications of this chip are shown in Table 4.3 in comparison to FE-I3.

Table 4.3: Specifications of LF-Monopix in comparison to FE-I3.

	LF-Monopix	FE-I3
		
Chip size	9.84 mm ×9.49 mm	
Active area†	6.45 mm ×9 mm	6.4 mm ×8 mm
Pxiel size	50 µm ×250 µm (FE-I4: 50 µm ×250 µm)	50 µm ×400 µm
Pixel matrix	129 rows ×36 columns	160 rows ×18 columns
Sensor structure	Large fill factor design	Without sensitive volume
Analog readout	CSA, Discriminator w/ 4-bit TDAC D1: Two-stage open loop structure D2: a self-biased differential amplifier followed by a inverter	CSA, Discriminator w/ 6-bits TDAC
Fast readout	Column drain R/O architecture	Column drain R/O architecture
Design	Uni. Bonn, CPPM, Irfu	[63]
Submission date	Aug 2016	———

†Total area of pixels excluding chip periphery

CHAPTER 5

Test systems and measurement methods

This chapter describes the test setup and measurement methods used to characterize the DMAPS prototypes shown in Chapter 4. In Section 5.1, the control and data acquisition (DAQ) system for the prototype chips is shown. The system is used in all of the measurements. The measurements are performed using electrical test pulses, shining a laser spot onto the DMAPS as well as injecting high energy particles. Section 5.2 explains the calibration of the electrical test pulses and measurement methods using the test pulses. Measurement setups using the laser and electrons are shown in Section 5.3 and 5.4, respectively. The procedures of the TID and NIEL irradiation are described in Section 5.5.

5.1 Prototype test systems

Chip control and DAQ system was developed for each prototype. Most parts were re-used to minimize development time. Figure 5.1 shows system hardware for LF-CPIX as an example. The hardware consists of 3 parts: a multi I/O board (MIO) [83], a general propose analog card (GPAC) [84] and a device under test (DUT) DUT printed circuit board (PCB) on which the prototype chip is mounted (DUT-PCB). MIO and GPAC are used in all test systems of the prototypes; the DUT-PCB is the only hardware developed exclusively for each prototype.

A prototype chip is glued on a DUT-PCB, and the inputs and outputs of the chip are wire bonded to the DUT-PCB. The DUT-PCB is equipped mainly with decoupling capacitors and terminal resistors. Only a few active components are mounted on the DUT-PCB because active components are mostly provided by the GPAC.

The GPAC is equipped with various types of input and output channels, such as power supplies, DACs, analog digital converters (ADCs), constant current sources, and digital input/outputs (DIOs) with level shifters. The configuration of those components on the GPAC has an I^2C interface [85] that is controlled by the MIO.

The DIO and ADC data output channels are connected to a field programmable gate array (FPGA) on the MIO. The MIO is equipped with Xilinx Spartan3 [86] FPGA and it has a USB2.0 interface [87]. The Multi I/O board 3.0 (MIO3) [88] is a board similar to the MIO.

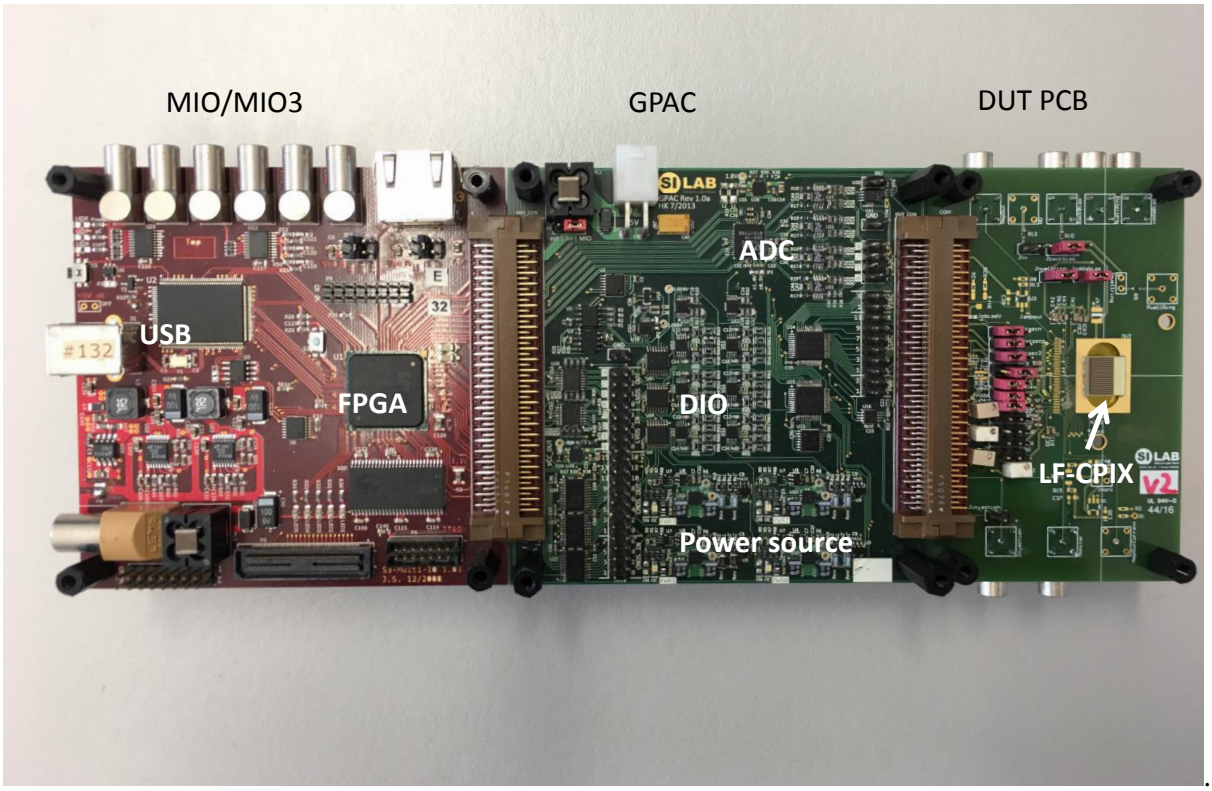


Figure 5.1: Photograph of the test system for LF-CPIX consisting of the MIO, the GPAC, and the DUT-PCB. A LF-CPIX chip is mounted on the DUT-PCB.

The FPGA on the MIO3 is Xilinx Kintex7 [89] and can be connected to a computer via gigabit Ethernet interface using SiTCP [90]. According to the data rate needed in the measurements, the LF-Monopix test system was developed using the MIO3 and the other prototype test systems were developed using MIO.

Firmware and software were developed based on the Basil framework [91]. It is a data acquisition framework written in Python [92] and Verilog [93]. Basil provides firmware modules and relevant Python classes that control the firmware modules. Figure 5.2 shows the block diagram of the firmware of LF-CPIX as an example. It consists of several simple modules from Basil, such as a pulse generator and serializer that are configured using Python scripts. Data from some modules, such as de-serializer or the ADC controller, are connected to one first-in first-out (FIFO) module implemented in the firmware, and data from the prototype is recorded in a computer via USB2.0 or gigabit Ethernet interface. Combining Basil modules, the test system realizes advanced functionalities, such as setting configurations to the prototype and reading out particle hit information from the prototype chip. Furthermore, the test system can synchronize with external equipment like a beam telescope (details in Section 5.4.2) or receive data from FE-I4 attached to H35DEMO and CCPD_LF. PyBAR [94] is used for the FE-I4 chip operation, because it is also based on Basil and can be easily merged with the software for H35DEMO and CCPD_LF.

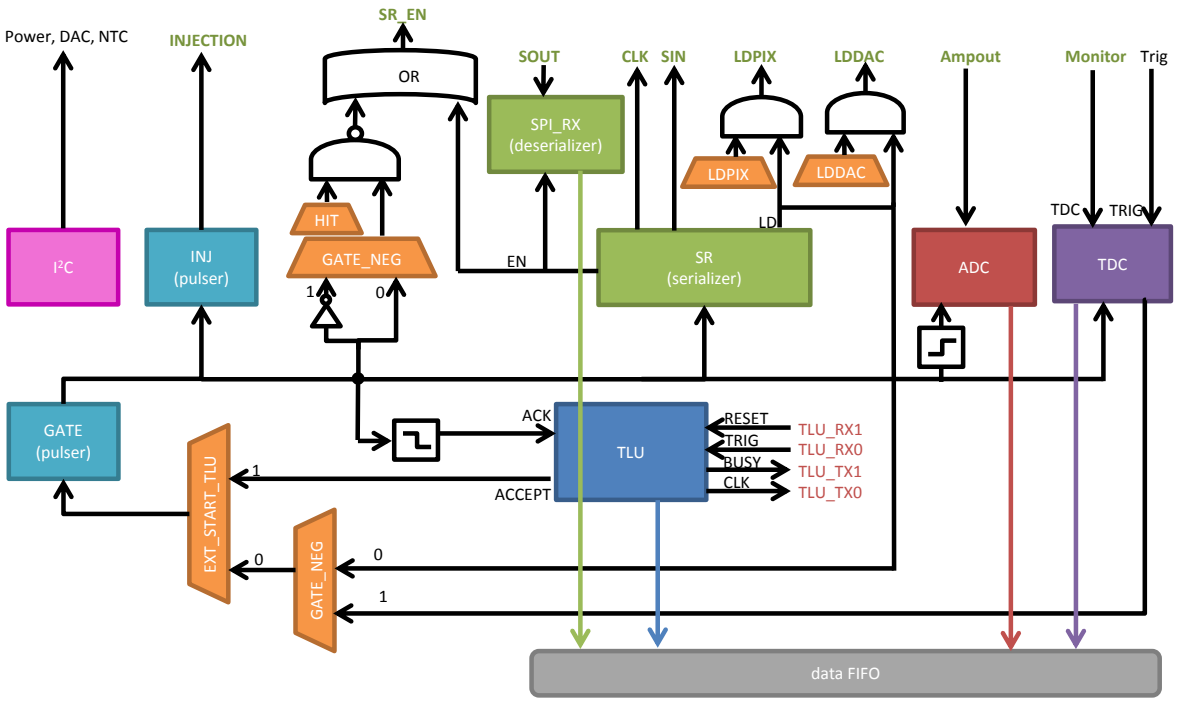


Figure 5.2: Block diagram of the firmware for the LF-CPIX test system. Signals shown in green are connected to the LF-CPIX chip. The rectangles indicate Basil modules, which are connected to a local bus, that is not visible in the diagram. Using Python scripts, the modules are configured through the local bus, and data from the modules are collected through the FIFO.

5.2 Readout electronics testing methods

5.2.1 Calibration procedure

The number of charges induced at the input of CSA by injecting a voltage pulse to the capacitor shown as C_{inj} in Figure 3.13 can be written as follows:

$$N_{inj} = C_{inj} \cdot V_{inj}/e, \tag{5.1}$$

where V_{inj} is the amplitude of the test pulse injected into the injection capacitor. C_{inj} should be calibrated in the following method using X-rays.

The photoelectric effect dominates the interaction between a photon and the sensor material in the photon energy range of 1–100 keV. In the photoelectric effect, full energy of the photon is absorbed by the sensor material, and electron-hole pairs are created. Different from the charged particles case shown in Section 3.2, the number of electron-hole pairs, N_{e-h}, induced by a single photon is independent of the sensor thickness and is expressed as follows:

$$N_{e-h} = \frac{E_{photon}}{E_{e-h}}, \tag{5.2}$$

Table 5.1: Types and energies of particles from radioactive sources and an accelerator [96, 97].

Source	Particle	Energy
^{55}Fe	photon	5.90 keV (also 6.40 keV is used in Section 6.2.3)
^{109}Cd	photon	22.163 keV
^{241}Am	photon	59.54 keV
^{90}Sr	electron	$\leq$ 2.279 MeV†
ELSA	electron	2.5 GeV or 3.5 GeV

†Endpoint of continuous spectrum

where E_{photon} is the photon energy. The fluctuation of N_{e-h} follows the Gaussian distribution and its deviation in the case of a semiconductor is expressed as follows:

$$\sigma_{e-h} = \sqrt{F \cdot N_{e-h}}, \tag{5.3}$$

where F is the Fano factor [95]. The E_{e-h} and F of silicon are listed in Table 3.1. In the case of a 5.90 keV X-ray in silicon at 300 K, N_{e-h} is 1 620 e^- and σ_{e-h} is 14 e^-. Since ENC of the analog front-end of the prototypes is approximately 150 e^- (see Section 6.3.1), σ_{e-h} is negligible.

The X-ray sources listed in Table 5.1 are used for calibration. In Table 5.3, only the energies used for measurements are listed, although the X-ray spectra of those sources have several peaks. The values of N_{e-h} are the same order of magnitude as the MPV of DMAPS (Section 3.2.2) without observable fluctuation.

The Figure 5.3 shows spectra of X-ray sources measured using LF-CPIX. The discriminator output in a LF-CPIX pixel is connected to the FPGA input via the debugging output port. The signal amplitude is recorded as pulse width of the discriminators output, which is measured in a time digital converter (TDC) module in the FPGA firmware of the LF-CPIX test system. The width of peak repents the noise from the pixel readout circuit and measurement system since the fluctuation from the Fano noise is the negligible.

In Figure 5.4, is a plot of the spectrum peaks in Figure 5.3 together with ToT response to test pulse injection is shown. When the ToT value of the test pulse matches the peak of an X-ray source, the amplitude of the test pulse is equivalent to the charges created by that X-ray. The value of C_{inj} can be obtained from the Equation (5.1). In the case of the CSA$_i n$-CMOS type pixel in LF-CPIX, C_{inj} was calibrated as 1.8 fF. Knowing the actual C_{inj} allows the gain and noise of the analog front-end circuit to be valuated using the test pulse response. In addition, the threshold of the discriminator can be tuned to the desired value electrically, namely without any particle sources.

5.2.2 ENC and gain measurement method

Since the CCPD_LF and LF-CPIX have binary readout systems (like that shown in Figure 3.13), ENC can be measured using the s-curve method. The response of the discriminator of multiple signal injections with various amplitudes is expected to follow a convolution of the Gaussian

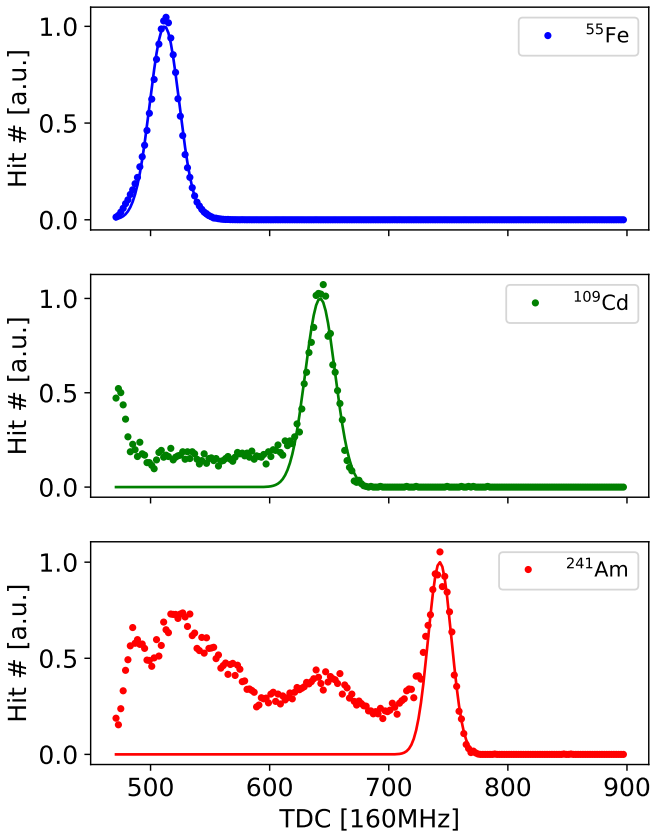


Figure 5.3: X-ray spectra measured using LF-CPIX. X-ray sources are indicated in the legends. The horizontal axis has units of the TDC value, where the clock is 160 MHz. The solid line in each plot is a fitted Gaussian function. The width of the peak represents the noise from the pixel readout circuit and the measurement system.

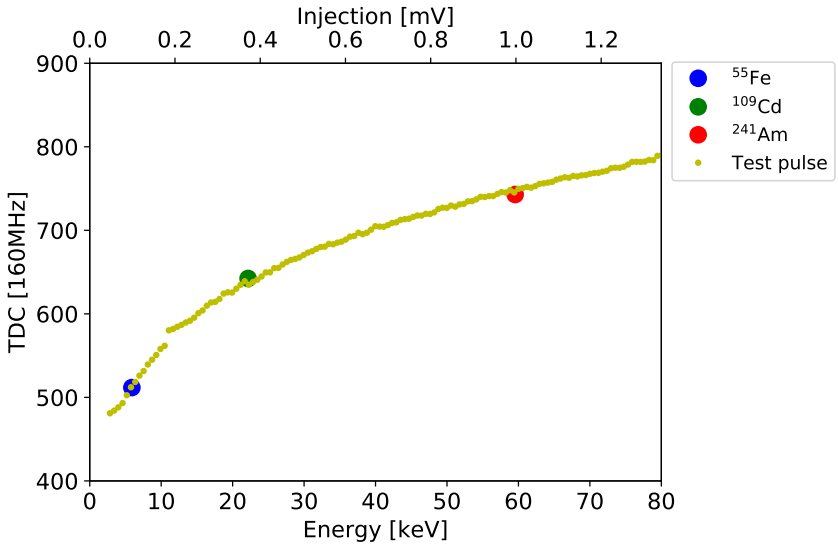


Figure 5.4: Signal amplitude against the test pulse amplitude (upper axis) and X-ray energy (lower axis). The vertical axis has units of TDC value, where the clock is 160 MHz. The lower axis is scaled to the upper axis applying Equation (5.1) with C_{inj} being 1.8 fF.

and step functions, namely an s-curve function. The s-curve function is expressed as follows:

$$S(inj, th) = \frac{1}{2} erf\left(\frac{inj - th}{\sqrt{2}\sigma}\right) + \frac{1}{2}, \tag{5.4}$$

where σ is the deviation of the Gaussian function and $erf(x)$ is the error function. The inj and th are variables representing the injected signal charge and the discriminator threshold, respectively. Either inj or th can be swept at fixed th or inj, respectively, to obtain gain and ENC.

Figure 5.5 shows results of the s-curve method when sweeping th. The σ withs units of the threshold voltage can be obtained by fitting Equation (5.4) to the measurement data. The gain is calculated from the inj for several th values. Figure 5.5 (b) shows the relationship between the inj and th of a CSA_{in}-CMOS type pixel in the LF-CPIX. The slope of the linear fit in the test pulse voltage range of 0–1.2 V_{inj} is 0.170 V_{th} /V_{inj} and the averaged σ is 2.24mV. Knowing C_{inj} is 1.8 nF, the gain of the pixel is 15 µV/e^-, and ENC is 148 e^-.

5.3 Laser response tests

Figure 5.6 shows the laser setup. The laser has a wavelength of 680 nm, and its attenuation length is 4 µm. When the laser is injected from the back side (the side opposite the surface where the collection wells are implanted), the laser response indicates how the charges are distributed across the sensitive volume, since most of the photons are absorbed near the back side surface. The laser response at various points in a pixel can be measured by moving the laser position using an X-Y stage. In-pixel homogeneity and cross talk induced by interpixel

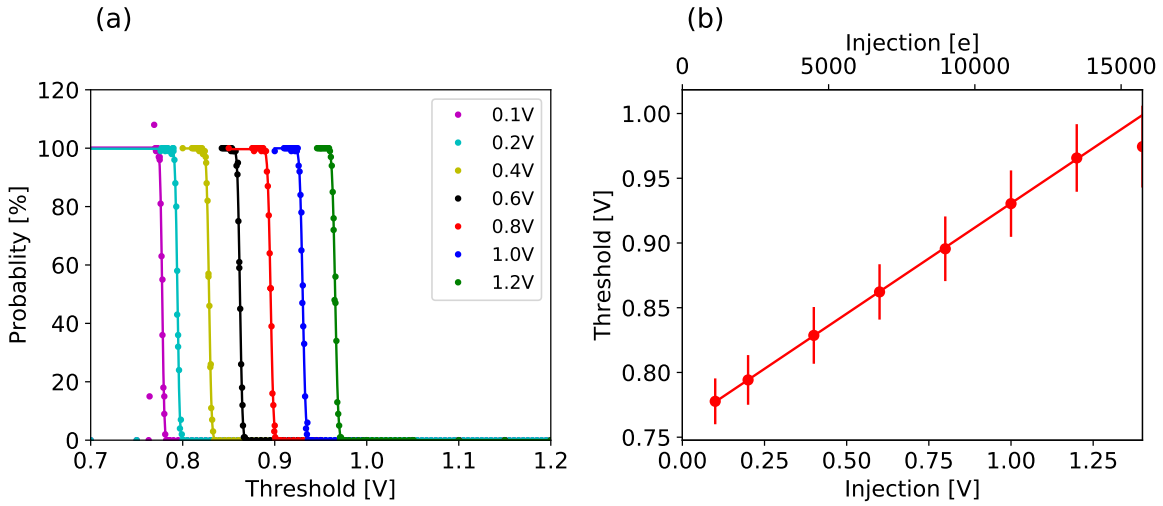


Figure 5.5: (a) The response fraction of the discriminator at various *inj* and (b) fitted *th* value (red points) extracted from (a) for each *inj*. The s-curve method were performed using a LF-CPIX CSA_{in}-CMOS type pixel. In (a), results of each test pulse amplitude is indicated by a different color, where the dots are the data points and the line in the same color shows the fit of the s-curve. In (b), *inj* in volts and electron charge are shown in the lower and upper axis, respectively. The error bars indicate the fitted σ; σ here is multiplied by 10 so that the error bars are discernible. The red line is a linear fit in the range of *inj* = 0–1.2 V_{inj}.

parasitic capacitance (indicated as C_{inter} in Figure 3.12) are tested with this setup because the spacial resolution of this setup is high.

The laser is focused by lenses. Figure 5.7 (a) shows the laser response of 100 µm thinned LF-CPIX with a bias voltage of 200 V. The distance between the focusing lens and the back surface of LF-CPIX has been varied to find the focal point. The X-Y stage was moved along the short side of the pixel (namely, the side which pixel pitch is 50 µm or more shortly, row-wise direction). Some of the results are asymmetry. These can be *explain*ed by asymmetric profiles of the defocused laser spot.

The measured profile was fitted by a convolution of the box and Gaussian functions. The fit function is expressed as follows:

$$\begin{aligned} B(x,w) &= \frac{A}{\sigma_{box}\sqrt{2\pi}} \int f_{box}(\tau,w) e^{-\frac{x-\tau^2}{2\sigma_{box}}} d\tau, \qquad f_{box}(\tau,w) = \begin{cases} 1 : |\tau| \le w \\ 0 : |\tau| > w \end{cases} \\ &= \frac{A}{2} erf\left(\frac{x+w/2}{\sqrt{2}\,\sigma_{box}}\right) + \frac{A}{2} erf\left(\frac{-x+w/2}{\sqrt{2}\,\sigma_{box}}\right), \end{aligned} \tag{5.5}$$

where w is the pixel width and σ_{box} is the standard deviation of the Gaussian function. Here, σ_{box} involve the laser spot size, σ_{laser}, and the diffusion size of the charge cloud in row-wise direction, σ_{pixel}. It can be expressed as follows:

$$\sigma_{box} = \sqrt{\sigma_{laser}^2 + \sigma_{pixel}^2}, \tag{5.6}$$

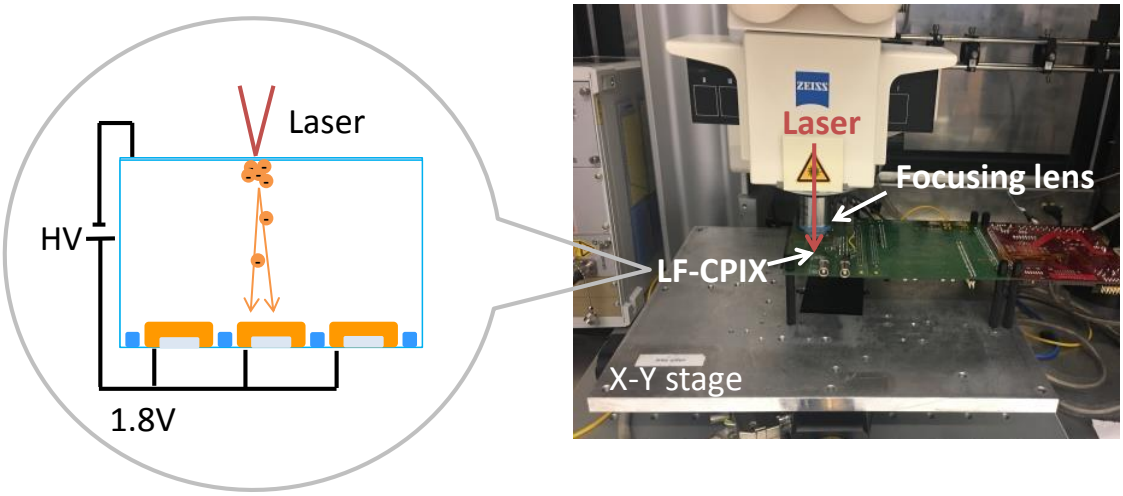


Figure 5.6: Drawing and picture of the laser setup. The 680 nm laser is focused by lenses and injected from the back side of a DMAPS prototype chip. The DMAPS prototype chip is mounted on an X-Y stage, and the position of the laser on the chip is moved by the X-Y stage

Figure 5.7 (b) shows σ_{box} of the laser response profiles calculated from the fit. Although the minimum value was measured to be 1.7 µm, the laser spot was readjusted to obtain a round laser spot on the surface of DMAPS. The σ_{box} was 2.5 µm for the readjusted laser spot. This implies that the σ_{pixel} value is smaller than 1.7 µm, and the σ_{box} is dominated by σ_{laser} if the laser spot with a σ_{box} value of 2.5 µm is used for measurement.

5.4 Electron beam tests

Electrons from ^{90}Sr and ELectron Stretcher and Accelerator (ELSA) at the University of Bonn [97] were used to characterize the DMAPS prototypes. ELSA provides 2.5 or 3.5 GeV electrons according to the accelerator operation, and ^{90}Sr emits electrons with a continuous spectrum with the endpoint of 2.3 MeV and the maximum intensity at 500 keV [98]. This section describe the characterization methods using the electron sources.

5.4.1 Timing measurement

The setups for time walk measurements are illustrated in Figure 5.8. A scintillator is used for time reference. Low energy electrons from ^{90}Sr lose all of their energy and stop in the middle of the DMAPS chip, whereas most of the particles pass through the DMAPS chip in HL-LHC experiments. To exclude this effect from the measured data, a scintillator is set downstream of the DMAPS and triggers events only when an electron reaches the scintillator.

Timing information is recorded in either of the two ways shown in Figure 5.8 (a) and (b). In Figure 5.8 (a), waveforms of the CSA and discriminator output pulse are recorded by an oscilloscope. In this measurement, timing precision is as high as the time resolution of the oscilloscope. However, only one pixel can be measured at a time.

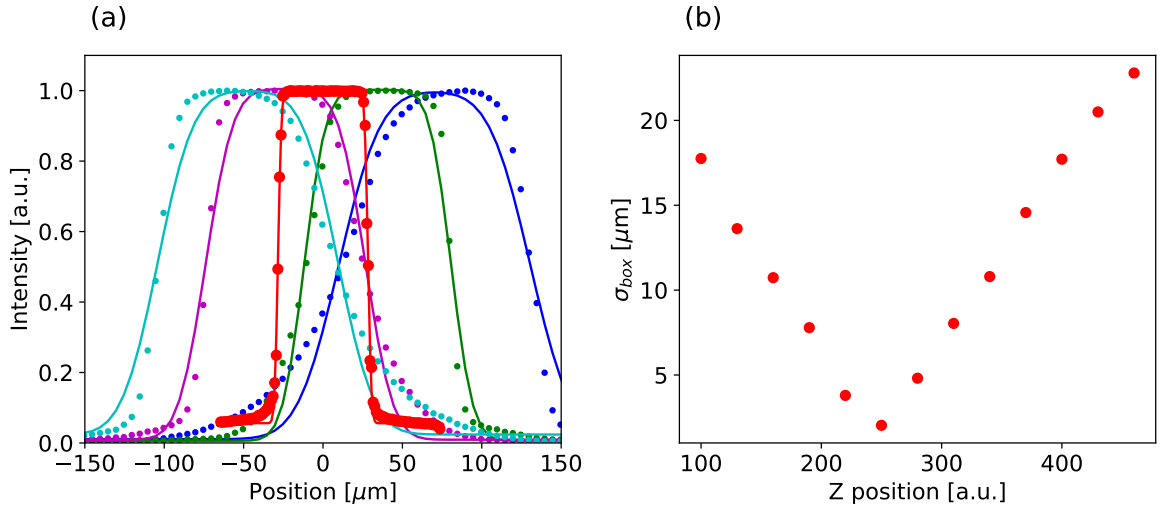


Figure 5.7: (a) Laser response and (b) fit value of the σ_{box} for 100 µm thinned LF-CPIX at various distances from the focal point. Dots in each color in (a) are measured data, and the line in the same color is the fit of Equation (5.5). Red dots show the profile at the position where the σ_{box} is minimum. The horizontal axis of the relative distance between the lens and the LF-CPIX in arbitrary units. The minimum value of σ_{box} is 1.7 µm.

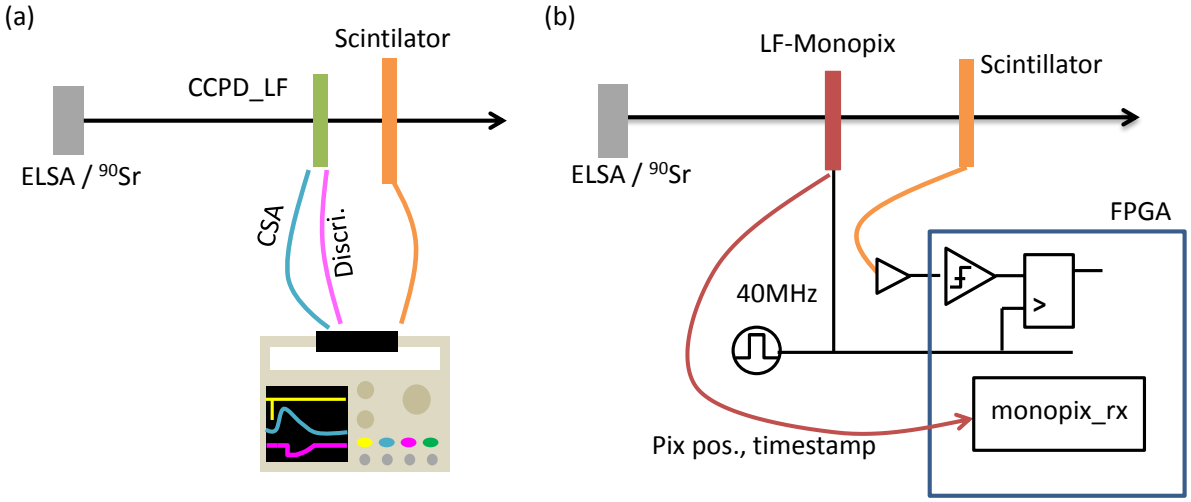


Figure 5.8: Time walk setup using ^{90}Sr or an electron beam. A scintillator is situated downstream of the prototype to trigger valid events. (a) is the setup monitoring the CSA and discriminator output to obtain the signal amplitude and response time, respectively. The waveforms of those are recorded with the scintillator output using oscilloscope. In (b), data from fast readout logic are recorded using FPGA. The ToT value and the timestamp of the leading edge are used to obtain the signal amplitude and response time, respectively. The scintillator signals are synchronized by the 40 MHz clock, which is also used for the LF-Monopix fast readout.

The oscilloscope used in the measurements has a sampling frequency of 5 GHz. The time walk setup in Figure 5.8 (b) involves LF-Monopix. The timestamps of the leading and trading edges of the discriminator response are recorded. The timing precision is not high as in the setup shown in Figure 5.8 (a) because the clock frequency of the timestamps is 40 MHz. In addition, the jitter of the measurement setup is 25 ns because the electron beam is not synchronized with the timestamp clock. But this setup can measure all pixels in the chip in parallel. Information about the cluster is only available from the setup in Figure 5.8 (b).

5.4.2 Hit efficiency measurement

Hit efficiency of a detector can be defined as the ratio of the number of hits (to be precise, the number of clusters) detected by the detector to the number of particles passing through the active area of the detector. One has to know when and where each particle passes through the detector. That information can be obtained by a device called a beam telescope. A Nice EUDET Mimosa BONn tElescope (ANEMONE), which is an EUDET-type beam telescope [99], was used for the the hit efficiency measurement of DMAPS prototypes. The block diagram of the beam telescope is depicted in Figure 5.9. It consists of six MIMOSA26 [100] planes, one FE-I4 plane, and one scintillator with a trigger logic unit (TLU), which digitize the scintillator output and distributes the scintillator signals to multiple DAQ systems simultaneously [101]. The beam telescope has a dedicated DAQ system using the MIO3 [102].

MIMOSA26 is a MAPS that has the small pixel size (18.2 µm ×18.2 µm) for high spatial resolution and thin sensor thickness (100 µm) for minimized multiple scattering [100]. The active area of the MIMOSA26 is as large as 21 mm × 10.5 mm. A particle track is reconstructed by fitting a linear line to the six hit positions obtained from the MIMOSA26 planes and interpolating onto the DUT planes (here, they are DMAPS prototypes) that are installed between the third and fourth MIMOSA26 planes. In this way, it is possible to know where the particles are passing through the prototypes. The arrival times of particles are not obtained by MIMOSA26 because its readout is a rolling shutter with a readout period of 115.2 µs and the time resolution of MIMOSA26 is not high.k A reference plane is introduced according to the readout type of DUT plane.

With the LF-CPIX planes acting as a DUT plane, two LF-CPIXs were installed between the third and fourth MIMOSA26 planes. Both LF-CPIXs are DUT planes, and each LF-CPIX is used as a reference plane of the other plane. The timing information cannot be obtained from the slow readout with the HIT resistors (Section 4.2.1). Integration time of the reference plane has been synchronized to that of DUT plane, and the reconstructed tracks that has a corresponding hit on the reference plane were used to calculate the hit efficiency. In this way, the particles that pass the DUT plane when its HIT registers are enabled are selected. Hits on the LF-CPIXs were integrated in the HIT registers for 115.2 µs and data in the HIT registers are read out in 345.6 µs, which correspond to the one and three frames of the MIMOSA26, respectively. Integration time of two LF-CPIXs are also synchronized to a MIMOSA26 frame. Thus particle tracks calculated from the MIMOSA26 data are correlate to the corresponding reference hits.

With the LF-Monopix planes acting as a DUT plane, hit information from the LF-Monopix can be continuously read out with timestamps at 40 MHz. FE-I4 readout, which is triggered by the TLU, is also operated at 40 MHz. FE-I4 is used as the reference plane, and FE-I4 hits are

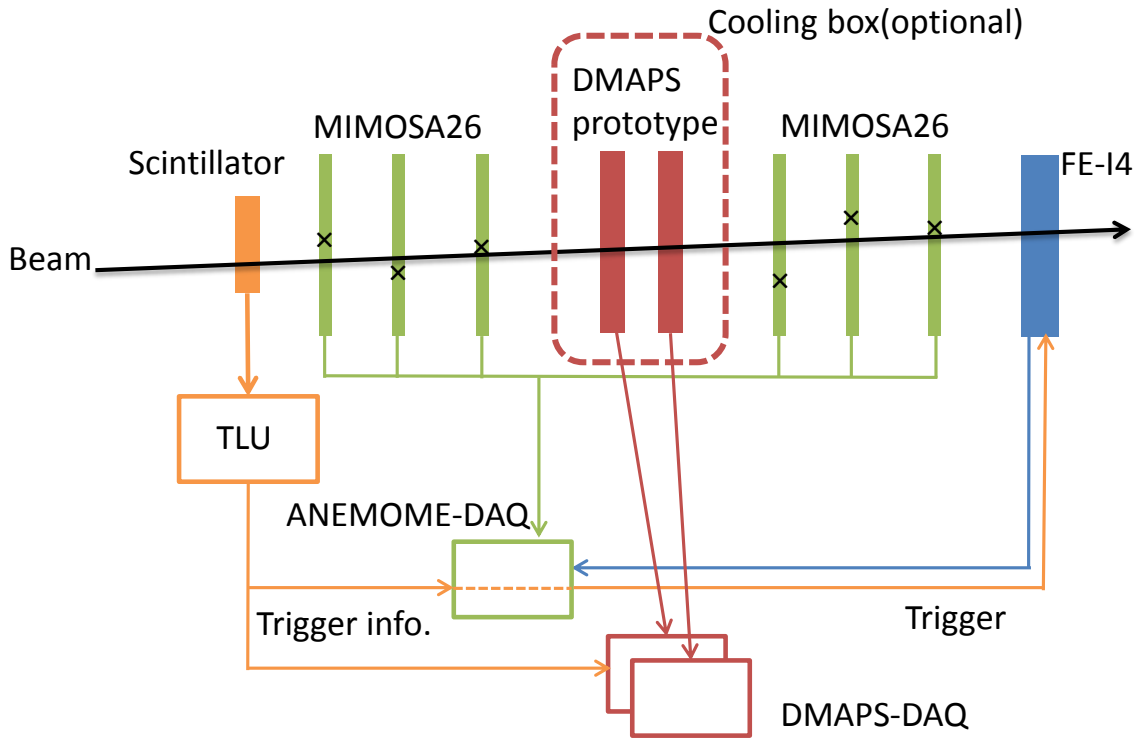


Figure 5.9: Block diagram of ANEMONE with a newly developed DAQ system. The flow of data is shown in different corresponding colors. Data from MIMOSA26 are collected continuously in 8 681 kfps. DMAPS prototype test system described in Section 5.1 is shown as DMAPS-DAQ in a separate block, although it is directly attached to the DUT-PCB. The TLU distributes the scintillator signal to the ANEMONE-DAQ and DMAPS-DAQ systems. It is also forwarded to the FE-I4 as a trigger signal.

correlated to the MIMOSA tracks in a frame that the corresponding trigger has arrived during the MIMOSA's 115.2 µs integration time. In this way, a timestamp of FE-I4 data is assigned as a timestamp of reconstructed tracks.

The track reconstruction analysis software, including correlating the tracks to hits in the DUT plane, is developed in this thesis. It is partially derived from TestBeam Analysis [103], which is software delicate to the data analysis of the beam telescope. Figure 5.10 shows a track occupancy map of 10 million tracks. The two rectangular areas with low occupancy correspond to disabled pixels in the reference plane.

Figure 5.11 shows the distributions of the differences between the particle position calculated from the reconstructed track and the hit position obtained by the DUT plane in the column- and row-wise directions, of which the pixel pitch are 250 µm and 50 µm, respectively. These residual profiles are fitted by Equation (5.5). The σ^2_{box} is a sum of the squared of the spatial resolution of the reconstructed tracks and the squared of the charge cloud size. The σ_{box} in the column- and row-wise directions are 22 µm and 20 µm, respectively, and are one order of magnitude larger than the upper limit of the charge cloud size measured by the visible laser (Section 6.2.1). This implies that the spatial resolution of the reconstructed tracks is approximately 20 µm. The main

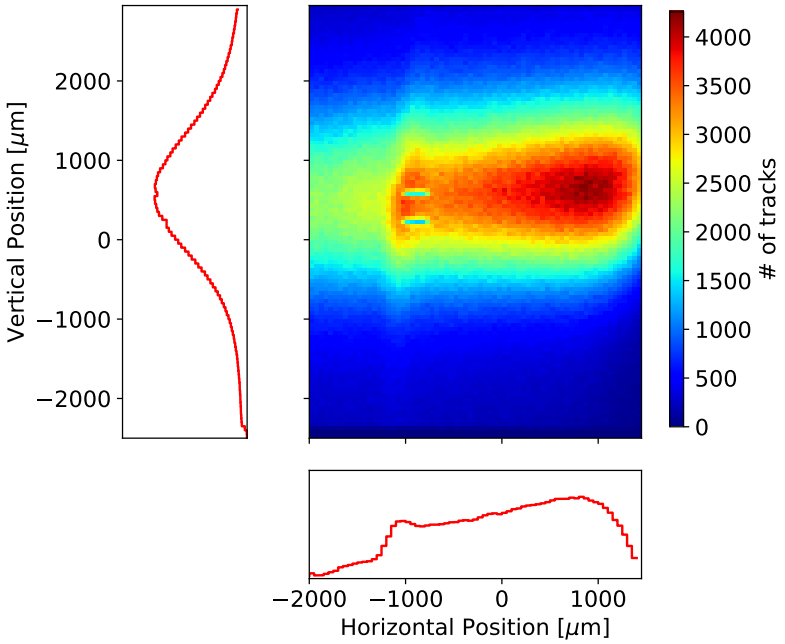


Figure 5.10: Occupancy map of reconstructed tracks on LF-CPIX plane. The map is the accumulation of 10 million tracks and shows the ELSA beam profile. The two rectangular areas, within which the number of tracks are less than the surrounding region, correspond to disabled pixels in the reference LF-CPIX plane. The horizontal and vertical projection of the map are also plotted in the bottom and left panel, respectively.

reason for the low spatial resolution is that reconstruction of the tracks is assuming that a particle trajectory is a straight-line, and multiple scattering is not considered. The spacial resolution can be improved by taking the multiple scattering into account [104, 105]. Moreover, σ_{box} can also be minimized by selecting tracks which are close to a straight-line [104]. The muliple scattering occurs by a chance, some of incident particles are less affected by the multiple scattering than others. However, the hit efficiency measurements in this thesis is included the all tracks where the residual between the track position and the hit position on the reference plane is smaller than 300 µm in both directions, i.e., column- and row-wise direction.

The long tail in the residual profile indicates that some hits are found 1 mm away from the reconstructed track position. This can also be explained by multiple scattering occurring in the DMAPS prototypes. In order to include the scattered hits into the efficiency calculation, the search path is set to 1 mm, and hits found in the range of 1 mm in both directions are counted as hits induced by the correlated tracks.

The finite baseline offset of the residual profile is caused by correlating a track to a DUT noise hit or DUT hit from another particle which passed the DUT during the corresponding integration time. This incorrect correlation occurs randomly in the chip. Thus, it is distributed uniformly in the residual distribution. It can be partially eliminated by limiting the hit search path. However, the incorrectly correlated hits still remain in the range of the search path. Assuming a uniform residual distribution of the incorrectly correlated hits, the number of hits in the baseline region is 0.1 % of all of the tracks in the search path. This limits the precision of the hit efficiency

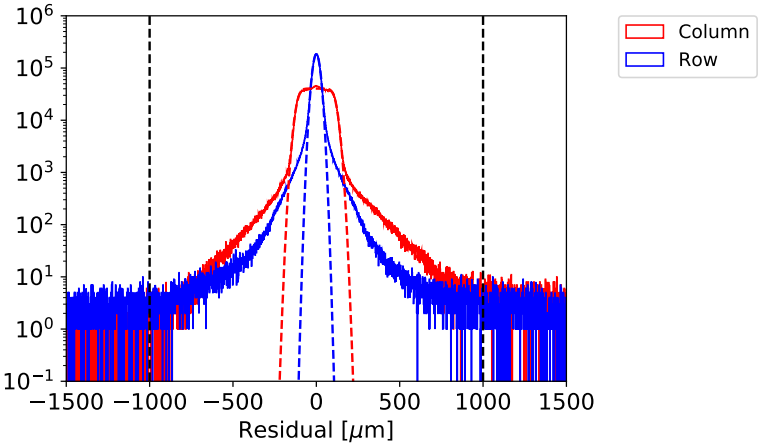


Figure 5.11: Residual profile of the column and row-wise direction on DUT plane, which here is a 100 µm thinned LF-CPIX. The profiles are fit by a convolution of Gaussian and box functions (Equation (5.5)). The fitted σ_{box} are 22 µm and 20 µm for the column- and row-wise direction, respectively. Dashed black lines indicate the search path, which is set to 1 mm. The baseline results from the incorrectly correlated tracks.

measurement. Incorrect collation occurs more often when the beam intensity is high, though high beam intensity allows the measurement time to be short. The beam intensity is set to obtain the precision of approximately 0.1 % since the required hit efficiency is >99.7 % and the precision of interest is 0.1 %.

5.5 Irradiation tests

5.5.1 TID irradiation

The TID radiation effect was tested using a 2 kW tungsten X-ray tube. The Institute of Experimental Nuclear Physics Irradiation Center at the Karlsruhe Institute for Technology (KIT) provided the X-ray tube [106].

As mentioned in Section 3.5.1, the STI layer, which is deposited beneath metal layers (Figure 3.16), is the main structure affected by TID irradiation in CMOS circuitry having a feature size of 150 nm. Figure 5.12 shows the energy spectrum of X-ray tube [106] and the calculated spectrum at the STI layer in the two cases: one case is when the main material of the metal layers is aluminum and the other case is when it is copper. In the calculation, the values of the attenuation coefficients are taken from [107, 108] and the metal layers were assumed to cover the whole chip, whereas absorption at vias placed between the metal layers are ignored. Since the K-edge of copper is at 8.979 keV, the X-ray spectrum at the STI layer is significantly different from that at the surface of the DMAPS prototype. In comparison, the K-edge of aluminum is 1.560 keV. The peak energy of the X-ray tube is 8.5 keV and the intensity rapidly drops at the lower energy side of the peak. Thus, the effect of absorption in the aluminum metal layers is small.

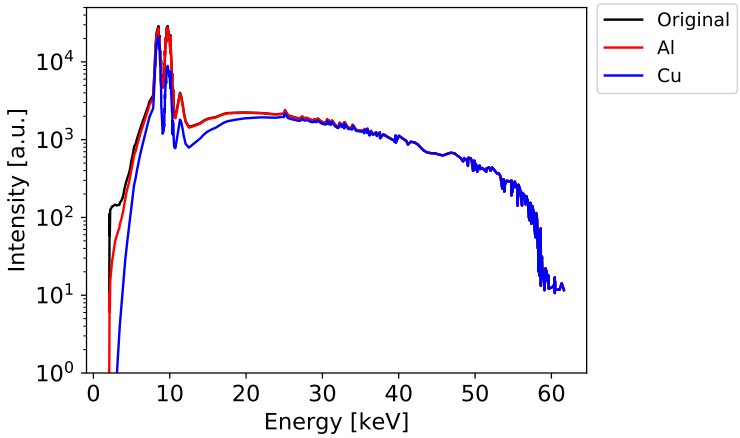


Figure 5.12: X-ray energy spectra at the DMAPS chip surface and at the STI layer. The black line is the original spectrum of the X-ray tube (the data was taken from [106]). The red and blue lines are the calculated x-ray energy spectra underneath aluminum and copper metal layers of typical CMOS circuits, respectively. The metal layers are assumed to cover the whole chip so that the maximum influence from the metal layers can be calculated.

The metal layers of LFoundry 150 nm CMOS are aluminum. The TID in the STI structure underneath the metal layers is 92 % of TID without the metal layers. TID values shown in this thesis do not take the absorption of metal layers into account because the STI is not the only structure affected by the TID, the collection factor is as small as 8 % even in the worst case.

The irradiation tests were performed for CCPD_LF and LF-CPIX, respectively. X-rays were irradiated on the front side of the prototypes. The X-ray dose rate was 1 482 krad/h and 572 krad/h for CCPD_LF and LF-CPIX, respectively. Figure 5.13 shows the TID versus time during the irradiation. The X-ray irradiation was paused at each TID step and measurements were performed at room temperature. The chip temperature was not controlled, and the average chip temperature during the measurement was 27 °C.

5.5.2 NIEL irradiation

NIEL radiation effects are tested with neutrons. Irradiation was done in TRIGA Mark II Research Reactor in Jožef Stefan Institute [109]. The neutron energy from the reactor is a continuous spectrum with hardness factor of 0.9 [110–112]. It also contains TID background with a rate of approximately 1 krad per 1×10^{12} n_{eq}/cm^2 [110].

The LF-Monopix are irradiated up to a 1 MeV neutron equivalent fluence of 1×10^{15} n_{eq}/cm^2 in bare chips, namely, they were not mounted on DUT-PCB and not characterized before the irradiation. They are compared to un-irradiated chips (identical but different devices). After the irradiation, the irradiated chips were annealed at 60 °C for 80 min and then kept in a cooled environment (~ -18 °C) except during measurements preparation.

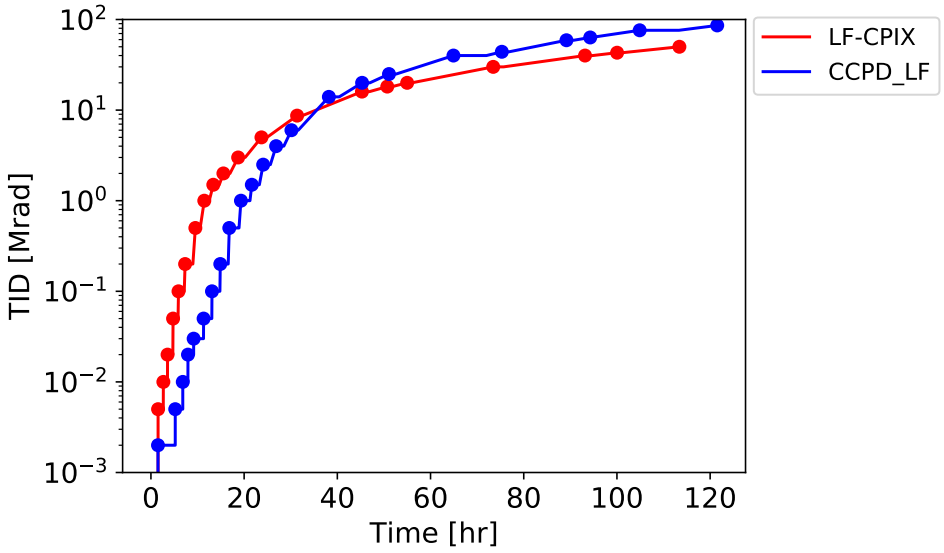


Figure 5.13: The TID rate of X-ray irradiation tests. Dots indicate a pause of the irradiation. During the irradiation pauses, measurements were performed. CCPD_LF and LF-CPIX were irradiated up to 80 Mrad and 50 Mrad, respectively.

CHAPTER 6

Characterization of DMAPS prototypes

In this chapter, the measurement results are described. Three DMAPS prototypes chips have been developed for different testing purposes, with each prototype corresponding to different functions and variations in the readout electronics or sensor structures. The best prototype of three was selected for each measurement.

6.1 Depletion of the sensor

6.1.1 Breakdown voltage

As summarized in Section 3.6, a sensor with high breakdown voltage is desired to obtain an adequately thick over-depletion region. The current-voltage (I-V) curve of CCPD_LF Large-FF was measured by sweeping a negative voltage from 0 V to −115 V on the outermost p-well ring. The leakage current between the outer most p-well ring and ground were measured. The eight other p-well guard rings and the p-stop were electrically floating. 1.8 V was applied to n-well rings that surround the pixel matrix, the periphery, and the end of the column circuitry. All electronics except those in the test structures are powered with 1.8 V. Figure 6.1 (a) shows the measured I-V curve, and the breakdown voltage of CCPD_LF Large-FF is approximately 110 V. Figure 6.1 (b) shows the I-V curve of CCPD_LF Small-FF. The highest bias voltage of the measurement results is 30 V because of the voltage tolerance of this chip (see Section 4.2.1).

The position where the breakdown occurred was investigated using a photo emission microscope (PEM) [113] in the Halbleiterlabor of the Max-Planck-Society [114]. The PEM detects photo emission and bremsstrahlung from "hot" electrons, but it is not sensitive to thermal emission from ohmic current. The PEM can specify the position where the breakdown occurs because "hot" electrons are created when breakdown occurs.

A bias voltage higher than the breakdown voltage (125 V) was applied to create a sufficient number of "hot" electrons for the PEM to detect. Figure 6.2 (a) shows the images obtained by the PEM. There are no "hot" electrons observed inside pixel matrix, namely, between the p-stop and the collection wells. The biasing circuitry of CCPD_LF Large-FF (indicated as red boxes in Figure 4.1 (b1)) is using active components, a large current due to the breakdown is expected to harm the bias circuit. In this point of view, the guardrings are working properly.

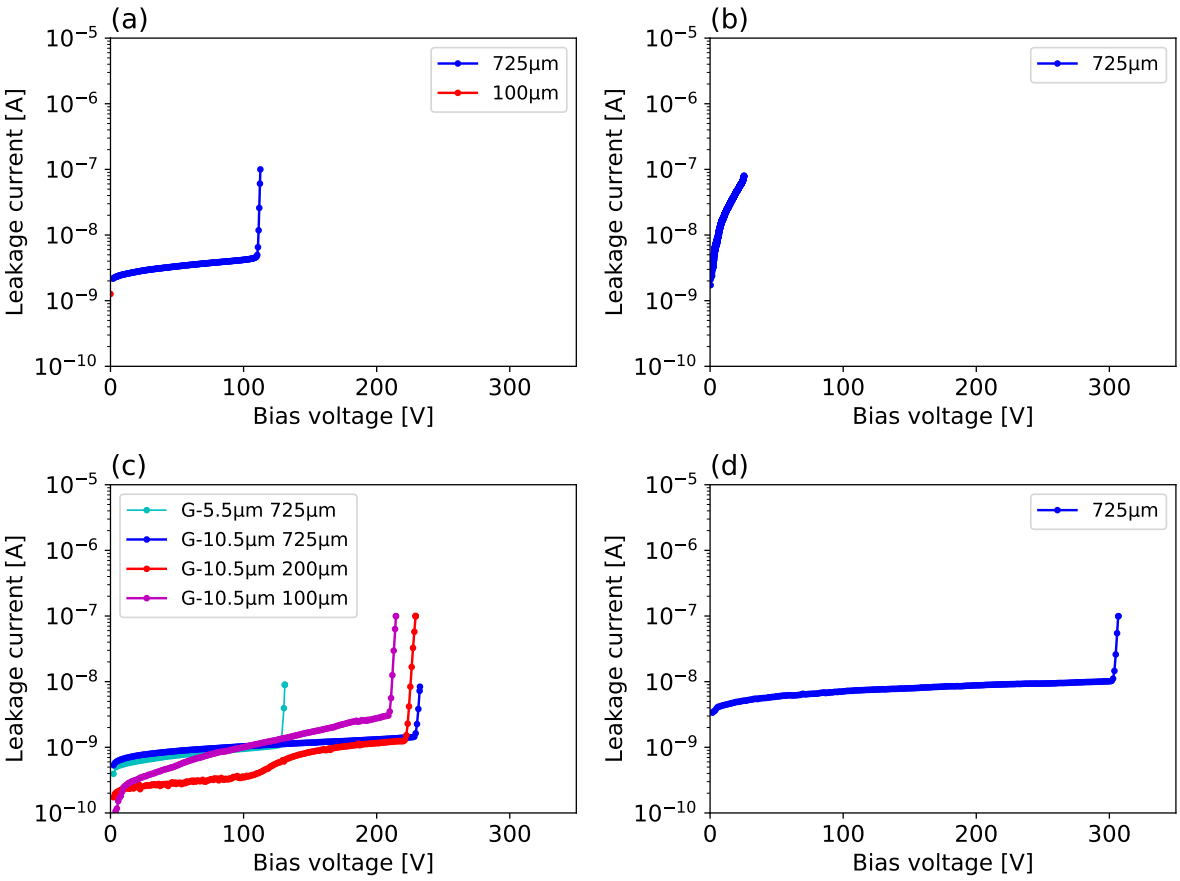


Figure 6.1: I-V curve of (a) CCPD_LF Large-FF, (b) CCPD_LF Small-FF, (c) LF-CPIX G-5.5 µm and G-10.5 µm, and (d) LF-Monopix. The thickness of each prototype chip is indicated in the legends. The chips without thinning are shown as 725 µm, which is the original wafer thickness.

In another point of view, however, the result also indicates that those guard rings limit the bias voltage. Figure 6.2 (b) shows the zoomed-in image of Figure 6.2 (a) overlaid by the layouts of the n- and p-wells. Hot electrons were created between the innermost p-well ring and the n-well ring. To increase the breakdown voltage, the distance between the inner most p-well ring and n-well ring should be increased. Two variants of LF-CPIX were fabricated to investigate the guard ring layouts, namely G-5.5 µm and G-10.5 µm. The zoomed-in layout of the guard rings of each variant is shown in Figure 6.3. The two distances between the inner most p-well ring and closest n-well ring are indicated in Figure 6.3 (a) and (b) are 5.5 µm and 10.5 µm, respectively.

The I-V curve of each layout is shown in Figure 6.1 (c). The breakdown voltage of G-5.5 µm and G-10.5 µm are 130 V and 215 V, respectively. The breakdown voltage of G-10.5 µm is higher than that of G-5.5 µm as expected, which confirmed that the distance between the innermost p-well ring and n-well ring affects the breakdown voltage. The same distance in LF-Monopix is 27.5µm, which is even longer than that of the LF-CPIX G-10.5 µm. The breakdown voltage is 300 V, which is higher than that of LF-CPIX G-10.5 µm.

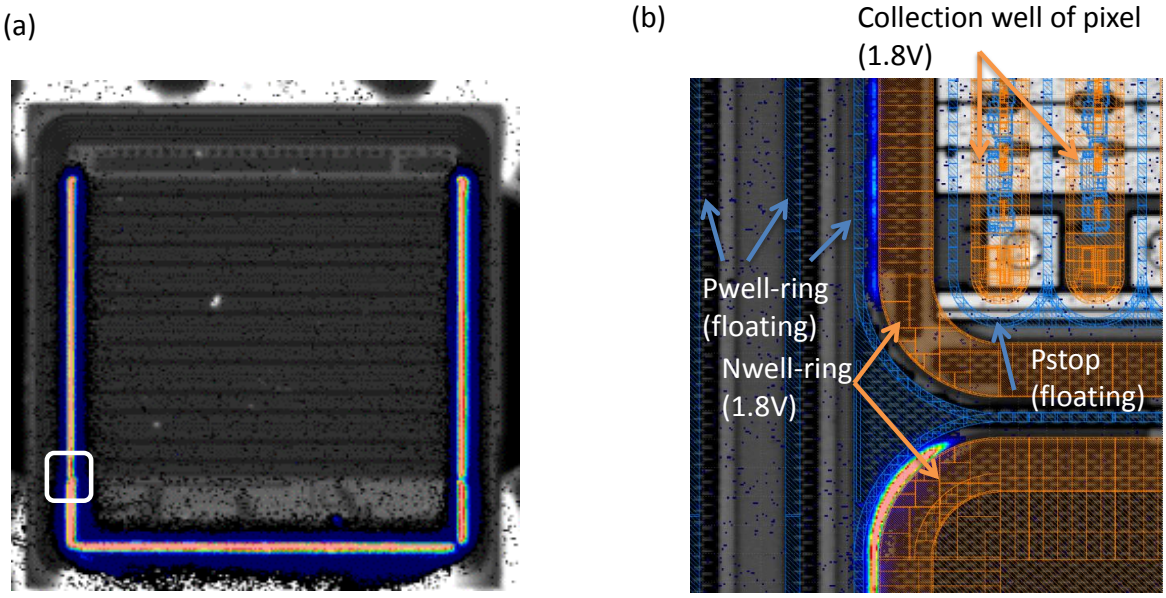


Figure 6.2: The PEM image of CCPD_LF. The bias voltage was 125 V to obtain detectable signals from the hot electrons. (a) An optical image of the chip is overlaid by the photo emission image. The optical image is shown in black and white, whereas the photo emission image is shown in color. Red indicates regions where "hot" electrons are generated. There are no "hot" electrons observed in the top part of the chip because the n-well ring surrounding the test cells is floating. (b) Zoomed-in PEM image of area enclosed in the white box in (a). The image is overlaid by the layouts of the p-well (shaded in blue) and n-well (shaded in orange) as well as the optical image.

6.1.2 Signal amplitude and depletion width

As discussed in Section 3.2.3, the signal charge will not be fully collected in 25 ns if the sensor is not depleted. In other words, the signal amplitude depends on the depletion width of the sensor. Sufficient amplitude of signal, namely the MPV, of the DMAPS confirms that bias voltages are properly applied to the sensor diodes in the DMAPS and that the sensitive area is depleted as expected.

The MPV of CCPD_LF Large-FF and Small-FF at various bias voltage was measured with a 3.5 GeV electron beam in the measurement setup shown in Figure 5.8 (a) but without the scintillator. The debugging port at the CSA output of a single pixel was recorded to obtain the signal amplitude. The results are shown in Figure 6.4. The MPV was obtained using Equation (3.1), and a library provided by pyLandau [115] was used for the fitting. Since the Landau function cannot be calculated analytically, approximation has been applied according to [116]. The MPV is larger for higher bias voltage, as expected. At the bias voltage of 110 V, the MPV is 13.3 ke^-. This corresponds to a depletion width of about 160 µm, which can be calculated from Equation (3.3).

The depletion width plotted against the bias voltage is shown in Figure 6.5. Figure 5.8 (b) shows that a depletion area is also created in Small-FF according to the bias voltage. The curves

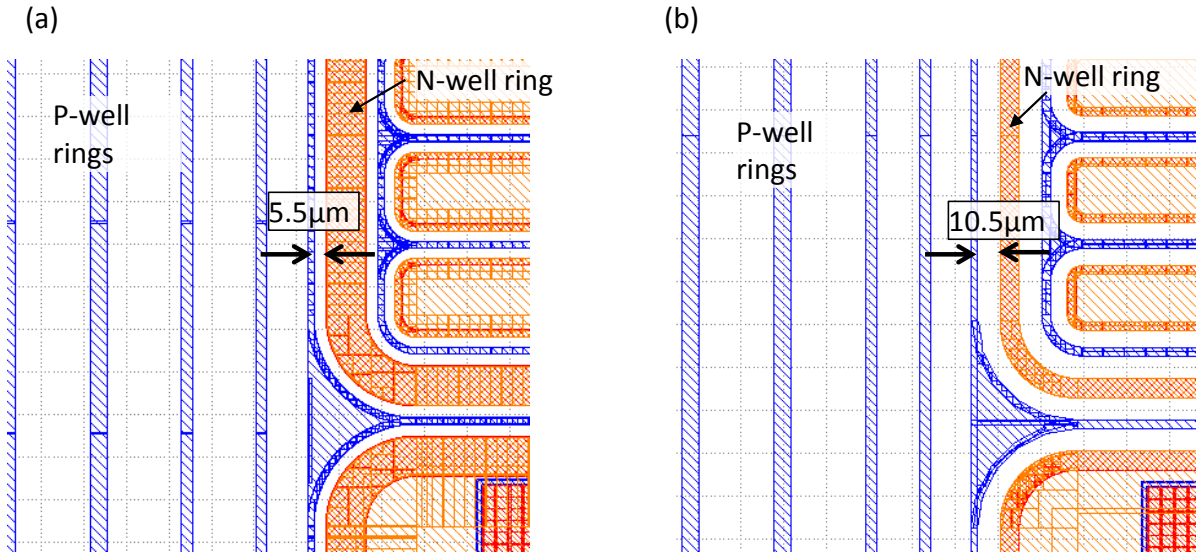


Figure 6.3: Guard ring layouts of LF-CPIX (a) G-5.5 µm and (b) G-10.5 µm. The zoomed-in region of the chip corresponds to the area enclosed in the white box in Figure 6.2 (a). The p-well and n-wells are shaded in blue and orange, respectively. The distance between the innermost p-well ring and closest n-well ring is indicated in each figure.

shown in Figure 6.5 are the calculated depletion widths of planar p-n silicon diodes shown in Figure 3.8. The measurement value is close to the calculated depletion width in a 3 kΩ cm wafer. This matches to the wafer supplier's guaranteed resistivity (≥ 2 kΩ cm) in the first order regardless of the following points: 1) the actual CCPD_LF collection well is not a planar as the calculation assumes, 2) the moderate Δ_p dependency (see Equation (3.2)) on the sensor thickness is not taken into account, and 3) charges from the non-depleted area are ignored. The difference between Small-FF and Large-FF in depletion width is explained by the different shape of the collection node and the difference between the wafers.

6.1.3 Thinning and back-side process

Thinning and back-side processing of wafers is one of technologies that have to be investigated in DMAPS development. As discussed in Section 3.3.1, the optimum thickness of the sensor can suppress the hit rate. The original thickness of the wafer is 725 µm but the thickness of the sensor required to create signal charge that is large enough to be distinguished from the noise when the readout noise is 200 e^- is know to be 100–200 µm according to the experiences in the development of the current ATLAS ID Pixel Detector [117].

Grinding of the CCPD_LF and LF-CPIX wafer was conducted from their back side after the CMOS process. The CCPD_LF wafer was thinned down to 100 µm, and LF-CPIX wafers were thinned down to 100 µm and 200 µm using TAIKO thinning process [118]. Then back-side processing was performed on the thinned back-side surface. The back-side processing consist of plasma etching, accepter ions implantation, and aluminum metallization. For CCPD_LF, the

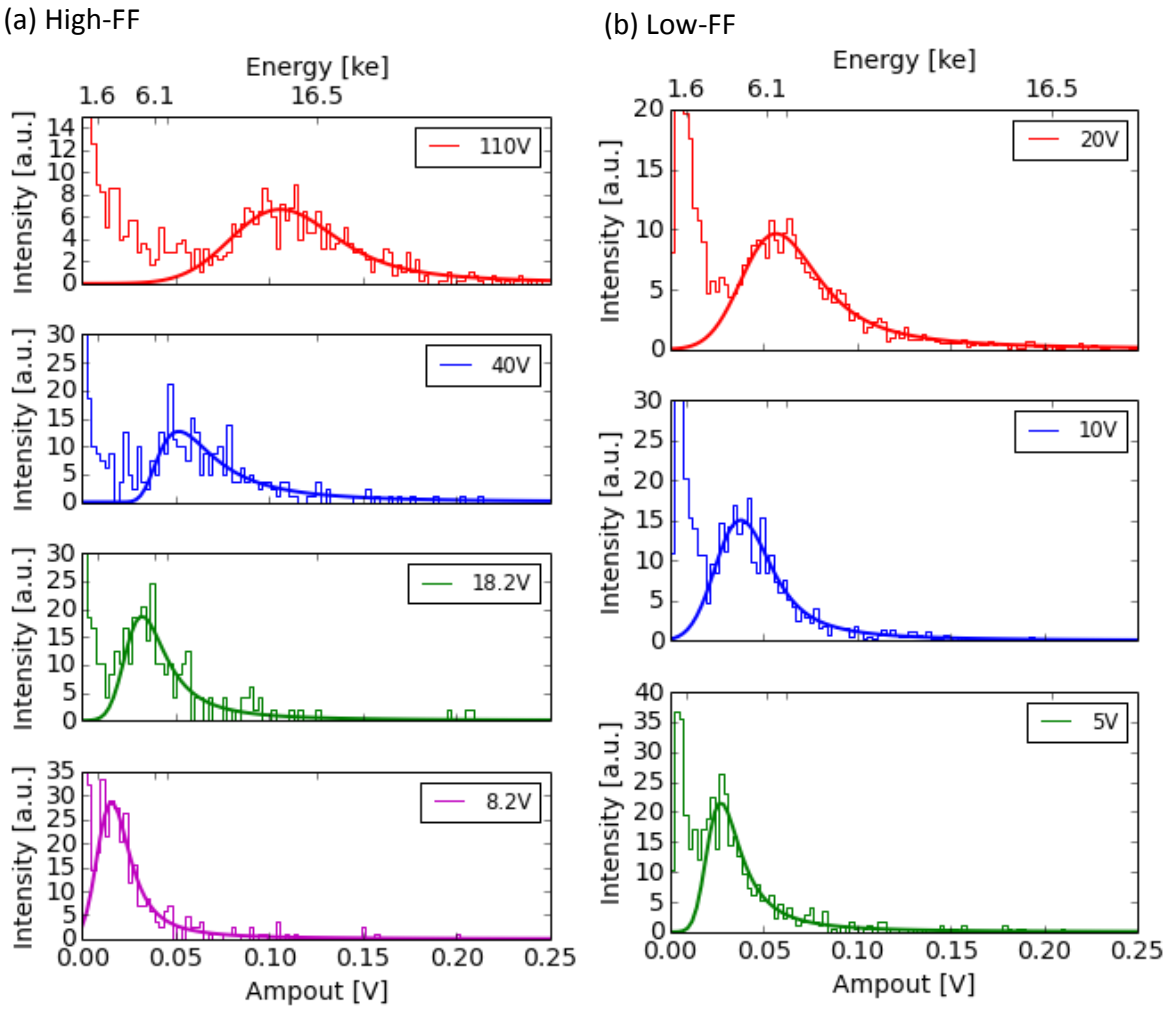


Figure 6.4: Charge spectra of a pixel of the CCPD_LF sensor. The injected beam is an electron beam of 3.5 GeV. Left plots are for Large-FF and right plots are for Small-FF. The bias voltage is shown in the upper right corner of each plot. The upper axis indicates calibrated energies in electron charge. The curve shows the fit according to Equation (3.1) by using numerical approximation.

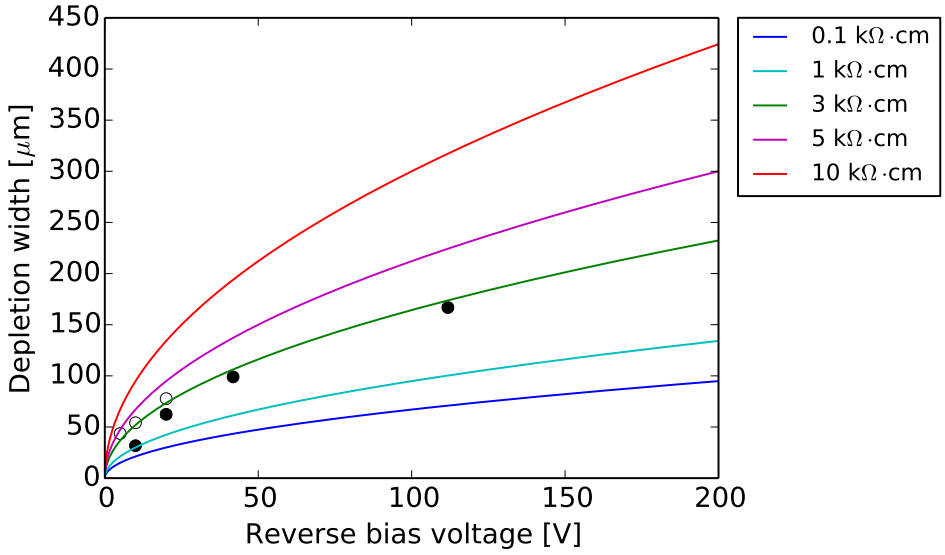


Figure 6.5: Depletion depths of the CCPD_LF sensor as calculated from the MPV. Solid and open circles indicate measurement data from Large-FF and Small-FF, respectively. The lines show the calculated depletion widths of planar silicon diodes with various resistivities.

plasma etching was skipped, and accepter ions were implanted soon after the grinding. The metallization process was omitted for the 100 µm thinned LF-CPIX.

6.1.3.1 Breakdown voltage and leakage current after the back-side process

The I-V curves of the thinned CCPD_LF and LF-CPIX are shown in red in Figure 6.1 (a) and (c), respectively. There is no obvious reduction in the breakdown voltage due to back-side processing. This is consistent with the PEM image that indicates that the breakdown is occurrs in the guard rings that are implanted on the front-side surface.

A large increase of the leakage current was observed in 100 µm thinned CCPD_LF when the bias voltage is higher than 20 V (Figure 6.1 (a)). The thickness of the sensitive volume in the 100 µm thinned CCPD_LF can be assumed to be approximately 85 µm because the CCPD_LF is estimated to consist of approximately 15 µm of insensitive regions, which correspond to the metal layers formed by the CMOS fabrication process and the conductive layer formed by the back-side processing. The 20 V is corresponds to the full depletion voltage of an 85 µm sensor with the resistivity of 4 kΩ cm (Equation (3.10)).

A small step like increase in the leakage current is also observed around 120 V of 200 µm thinned LF-CPIX. If the depletion voltage of a sensor with 185 µm is 120 V, the resistivity of the wafer should be 3–4 kΩ cm wafer. However, the amount of increase is as small as 1 nA. In 100 µm thinned LF-CPIX, no step like leakage current increase is observed around a full depletion voltage of 20 V. The increase in leakage current is also seen in silicon sensors in other studies, where they are reported to be very sensitive to the process of contact electrode [119, 120]. In contrast to the thinned CCPD_LF, plasma etching was performed on LF-CPIX before the acceptor ion implantation. The etching is effective in reducing or diminishing the increase

in the step-like leakage current around the full depletion voltage.

The chip leakage current of the 100 µm thinned LF-CPIX is 10 nA higher than that of the un-thinned and 200 µm thinned LF-CPIX at 200 V bias voltage. The breakdown voltage is slightly lower than that of un-thinned LF-CPIX. This might be due to the back-side process but also process fluctuations. However, the breakdown voltages of the thinned LF-CPIX chips is still higher than 200 µm; the 10 nA increase in the leakage current causes an increase of ENC_{shot} of 2 e^- assuming τ_f = 1 µs, which is orders of magnitude smaller than that of readout electronics (c.f. approximately 150 e^-, see Section 6.2) and can be ignored.

6.1.3.2 Full depletion voltage

The full depletion voltage of the thinned LF-CPIX chip was measured using the laser setup described in Section 5.3 . The laser can reach the sensitive volume since the chip does not have aluminum on the back-side surface, as mentioned in the beginning of this section. The laser response of a pixel in the 100 µm thinned LF-CPIX was recorded by scanning the laser along the short side of the pixel. The signal amplitude is plotted against the laser position in Figure 6.6 (a). Although there are more precise studies of the profile of partially depleted sensors can be carried out [121], the measured profiles including when the bias voltage is low are fit with the convoluted box functions (Equation (5.5)).

The standard deviation, σ_{box}, is shown in Figure 6.6 (b) as a function of the bias voltage. Since the σ_{box} is dominated by σ_{laser} when σ_{box} is >1.7 µm (see Section 5.3), σ_{pixel} is corrected, assuming σ_{laser}=2.5 µm. The σ_{box} without the correction shows the upper limit of the actual σ_{pixel}, and the corrected σ_{pixel} shows the lower limit of the actual σ_{pixel}.

If the sensor is partially depleted, most of the charges are created in the non-depleted area, and those charges move only by diffusion. Then, charges that reach the partially depleted area move toward the collection well, mainly by drift. The σ_{pixel} indicates the size of the charge cloud at the collection node, namely, the front-side of DMAPS. In other words, the σ_{pixel} represent the charge collection time because the charge movement in the row-wise direction is only due to diffusion, and it is the same in both non-depleted and depleted regions. There is a kink in the slope around 20 V bias voltage. This result shows that the depletion area reaches the back-side contact around that bias voltage. This is consistent with the increase in the step-like leakage current discussed in Section 6.1.3.1 even though the laser measurement was performed on 100 µm thinned LF-CPIX and I-V curve of 100 µm thinned CCPD_LF, which were not on the same wafer as LF-CPIX.

In the higher bias voltage region of 20 V, the σ_{pixel} slowly decreases according to the increase in the bias voltage. This can be understood in that the strength of the electric field toward the collection well increases because of the over depletion as described in Equation (3.11).

6.1.3.3 Hit efficiency of thinned DMAPS prototype

The hit efficiency of the 200 µm thinned LF-CPIX is measured and compared to that of the un-thinned LF-CPIX. Figure 6.7 (a) and (b) shows hit efficiency maps of the un-thinned and thinned LF-CPIX, respectively. The bias voltage of the chips is 200 V and 13 × 106 pixels in the LF-CPIX matrix are activated in both chips. The lowest threshold of LF-CPIX is limited

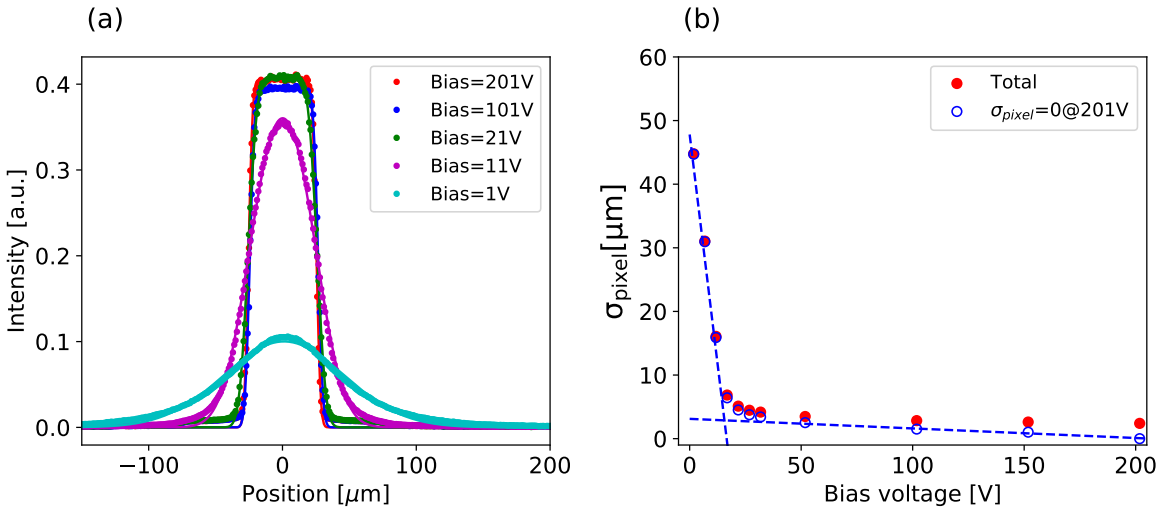


Figure 6.6: (a) Laser response of LF-CPIX pixel at various bias voltages and (b) its σ_{pixel} extracted from fitting the convoluted box function to the laser responses.

by the digital cross coupling of the slow readout, which is discussed in Section 6.2.4. The threshold was 1 700 e^- and 2 750 e^- for un-thinned and thinned LF-CPIX, respectively. The noise occupancy cannot be evaluated directly because of the cross coupling. However, the hit efficiency measurement could be performed, and the impurity derived from the hit and track position residual was 0.1 and 0.04 % for un-thinned and thinned LF-CPIX, respectively, with a track search path of 1 mm.

Considering 13 × 106 (=1378)) pixels in each chip, 2 pixels of un-thinned LF-CPIX and 4 pixels of 200 µm thinned LF-CPIX were disabled because the threshold of those pixels was out of the TDAC tuning range. The inefficient rectangular regions seen in Figure 6.7 correspond to those disabled pixels. As is shown in the track occupancy map (Figure 5.10), the electron beam is smaller than the activated LF-CPIX region. The number of tracks in the outer part of the LF-CPIX chips is not large enough to calculate the efficiency. The hit efficiency of each chip was averaged in the area enclosed in the white box, excluding areas corresponding to the disable pixels.

The average hit efficiency of the 200 µm thinned LF-CPIX is 99.5 %. Comparing to that of the un-thinned LF-CPIX, which is 99.4 %, no degradation in the hit efficiency is observed. The chip thickness of 200 µm produces a enough number of signal charges for particle detection in the DMAPS prototype of which the lowest threshold is 2750 e^-.

6.2 Collection well

6.2.1 In-pixel homogeneity of the pixel response

Sensor homogeneity of 100 µm thinned LF-CPIX pixel was measured using the laser setup described in Section 5.3. Figure 6.8 (a) and (b) shows laser response along the short and long

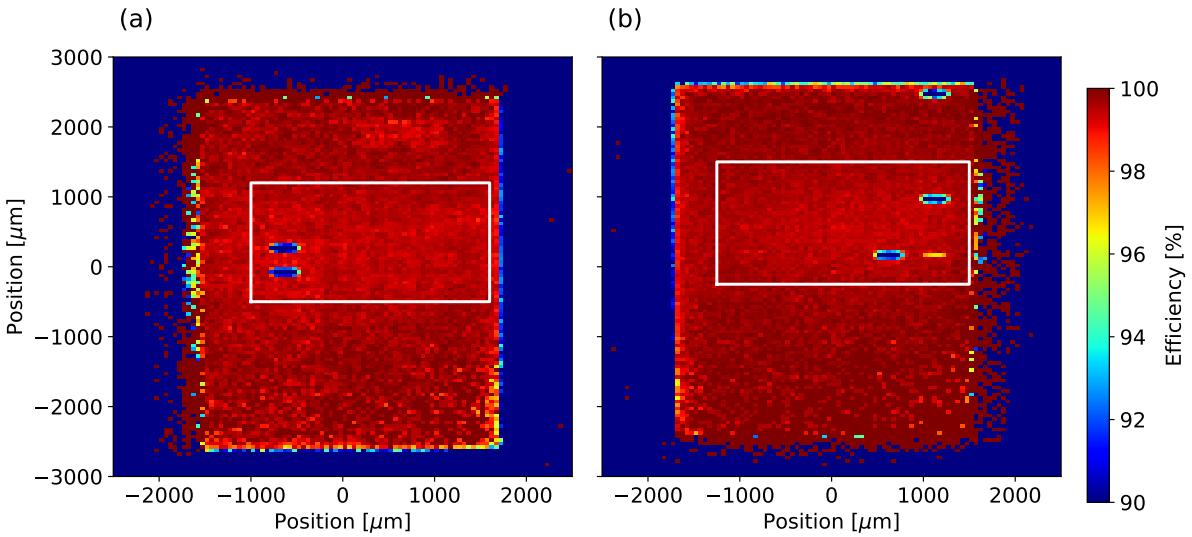


Figure 6.7: Hit efficiency of the (a) un-thinned and (b) 200 µm thinned LF-CPIX chips. The 13 × 106 pixels are activated except 2 and 4 pixels for the un-thinned and 200 µm thinned LF-CPIX, respectively. The rectangular inefficient areas are due to those disabled pixels. Average hit efficiencies in the regions the white boxes are 99.4 % and 99.5 %, respectively, when the inefficient regions due to the disabled pixels are excluded.

sides of pixel, respectively. The bias voltage is 200 V and is far higher than the full depletion voltage of 20 V according to the results of Section 6.1.3.2. The profile of each pixel is fit by Equation (5.5). The measured data were normalized by the height of the fit function to investigate the charge collection homogeneity near the pixel edges. The difference in the gain between each pixel is compensated by this normalization. The sum of the normalized pixel profile is also shown in Figure 6.8. The summed profile is uniform including the edge of the pixels. The precision of the result is limited by the laser stability during the measurement. No in-pixel structures are observed from the laser response within the obtained precision of approximately 2 %.

6.2.2 Interpixel capacitance

Interpixel cross talk between 100 µm thinned LF-CPIX pixels has also been measured with the laser setup. It is a cross talk based on the parasitic interpixel capacitance (indicated as C_{inter} in Figure 3.12). The interpixel capacitance is also shown with the top view of the LF-CPIX layout in Figure 6.10. Since the collection nodes are electrically coupled via C_{inter}, charges are induced also when the neighboring pixel collects the charge.

Figure 6.10 shows the laser response along the long side (250 µm) and short side (50 µm) of one pixel in a log scale. The charge sharing and the interpixel cross talk can be distinguished by the shape of the profiles. Charge sharing is corresponds to σ_{box} of Equation (5.5). On the other hand, the interpixel cross talk is corresponds to additional box functions of which center is equal to the pixel pitch.

The cross talk of long side and short side are calculated from the fit as 1.7 % and 0.22 %,

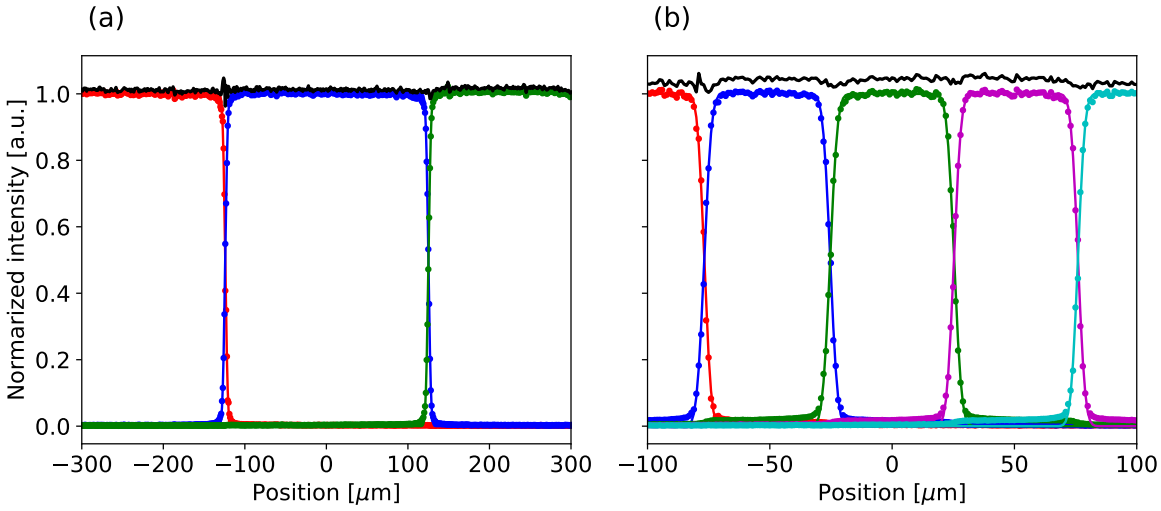


Figure 6.8: Laser response of LF-CPIX along (a) the short and (b) the long side. Red, blue, green magenta, and cyan dots shows the the normalized measured intensity of the laser response from a pixel. The fitted lines are shown in the same color as the measured dots, accordingly. Black dots show the sum of the normalized laser response.

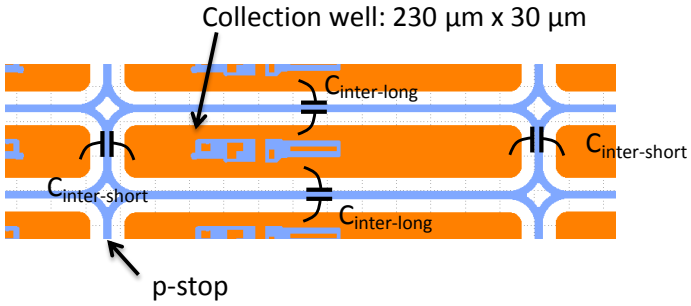


Figure 6.9: Top view of LF-CPIX layout and the parasitic interpixel capacitance, C_{inter}. C_{inter} can be divided into $C_{inter-long}$ and $C_{inter-short}$, which are the interpixel capacitance of the long and short sides of the pixel, respectively.

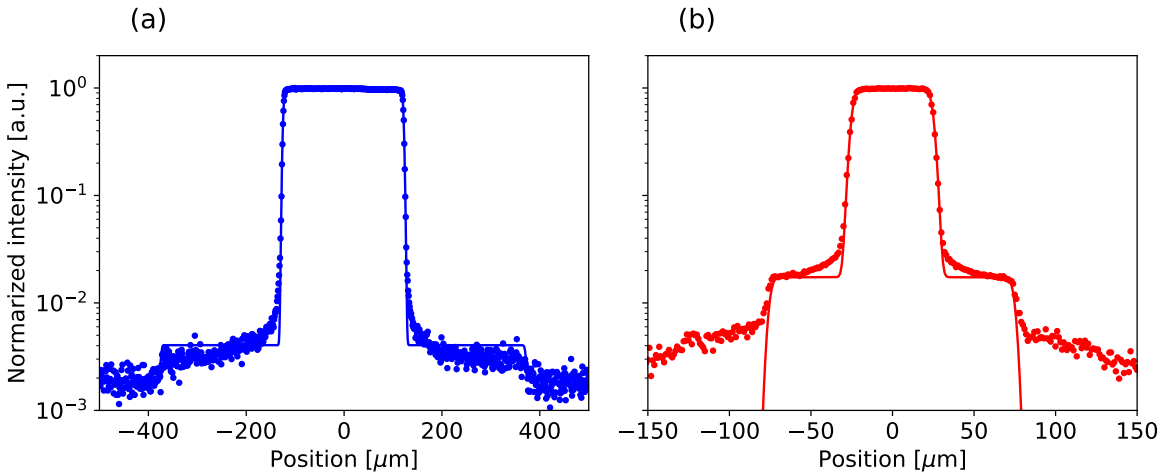


Figure 6.10: Laser response profile along (a) the long and (b) the short side of the pixel. The solid line in shows the fitting results of the sum of the two convoluted box functions with different heights and widths. The measured data is normalized by the height of the dominant box function. The height of secondary box function is 0.0022 and 0.017 for (a) and (b), respectively.

respectively. As shown in Figure 6.9, the interpixel capacitance of the long side is expected to be a factor of 7.7 larger than that of the long side when the round shape of the collection well at the pixel edge is not considered. This estimation matches the measurement results. If the threshold of the discriminator is set to higher than 1/50 of MPV, then a signal response smaller than the threshold, such as the interpixel cross talk, is negligible.

6.2.3 Size of the collection well and detector capacitance

The ENC was determined from the energy spectrum of ^{55}Fe for CCPD_LF Large-FF and Small-FF. The amplitude of the CSA output signal for one pixel is shown in Figure 6.11. The main peak corresponds to 5.9 keV. The lower tail is the effect of charge sharing, and the peak around 2 mV is an artefact caused by the noise tail passing the trigger threshold.

The peak at 5.9 keV is fit by a Gaussian function, and its deviation corresponds to the ENC. The fit results indicate that the ENC of Large-FF and Small-FF are 149 and 100 e^-, respectively. The ENC of Small-FF is smaller than that of Large-FF as expected.

6.2.4 Digital signal coupling to the analog front-end

Digital logic elements are also included in the pixel readout electronics of the prototype chips. As mentioned in Section 3.3.2, cross coupling from the digital signal to the current turbulence on the collection node is a disadvantage of the large-fill-factor design. The cross coupling of CCPD_LF and LF-CPIX were evaluated by monitoring the output of the CSA and the discriminator with an oscilloscope.

Cross coupling was indeed observed in CCPD_LF and LF-CPIX. Figure 6.12 (a) shows the

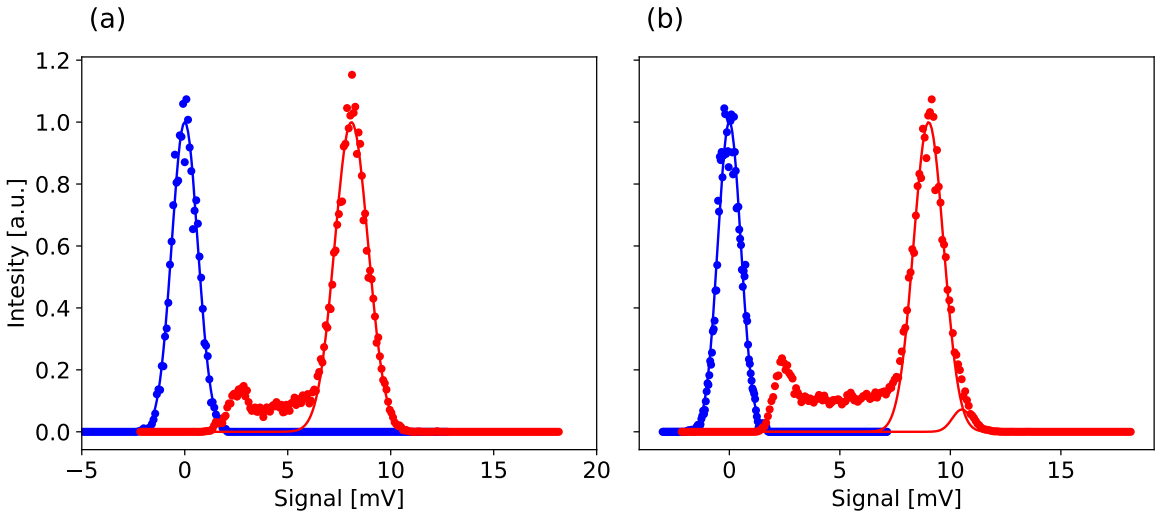


Figure 6.11: Charge spectrum of ^{55}Fe (red circle) and the baseline (blue circle). (a) is Large-FF and Small-FF. The peaks are normalized to unity. The lines are fit Gaussian functions. Since the Small-FF has smaller ENC, the ^{55}Fe spectrum of Small-FF was fit by a sum of two Gaussian, which corresponds to Mn K_α and K_β.

CSA and discriminator outputs when the state of a register is changed in a CCPD_LF pixel. The signal that produces the digital cross coupling is a switch that enables the HIT register. It has to be switched every image frame in order to accumulate particle hits and creates an image of the matrix by shifting the HIT registers. The amplitude of the cross coupling signal depends on the thresholds setting. In the actual measurement setting, the lowest threshold was limited by this cross coupling, and it is approximately 2 500 e^- for LF-CPIX with wide chip-to-chip variations.

The cross coupling of the LF-Monopix was minimized with a careful circuit design. Figure 6.12 (b) shows an oscilloscope screen capture of the waveforms at the output of the CSA and discriminator of a LF-Monopix pixel when a negative voltage pulse is injected into the injection capacitor of the pixel. The digital signals in the fast readout logics are also shown in the pixel (indicated as TOKEN, FREEZE, CLOCK, and READ). There is no cross coupling observed in the measurement, though the digital signals change their state. However, cross coupling due to the status change of the READ signal is reported in some cases [122]. Fortunately, this can be ignored by the test system of LF-Monopix.

6.3 In-pixel readout circuit

6.3.1 Gain and ENC of new type CSAs

The gain and noise of the analog front-end circuit was measured using test pulse injection by the method explained in Section 5.5. The distribution of the measured gain and ENC of LF-CPIX are shown in Figure 6.13. The average and the dispersion of the gain and ENC of each type are shown in Table 6.1 together with their design values [81]. The measured values including those

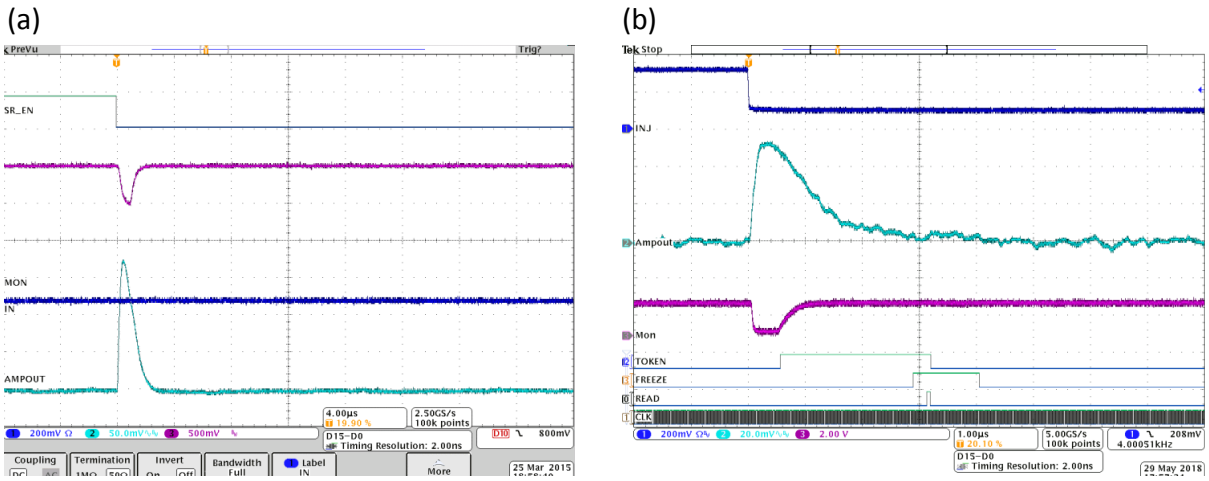


Figure 6.12: Oscilloscope screen captures of the injected test pulse (blue), CSA output (cyan), discriminator output (magenta), and digital signals (green and blue). (a) is a capture of signals from a LF-CPIX pixel when the hit register enabling switch (indicated as SR_EN) changed its state from high to low. (b) is a capture of signals from a LF-Monopix pixel when a test pulse was injected, and a signal indicated as TOKEN changed its states according to the discriminator response.

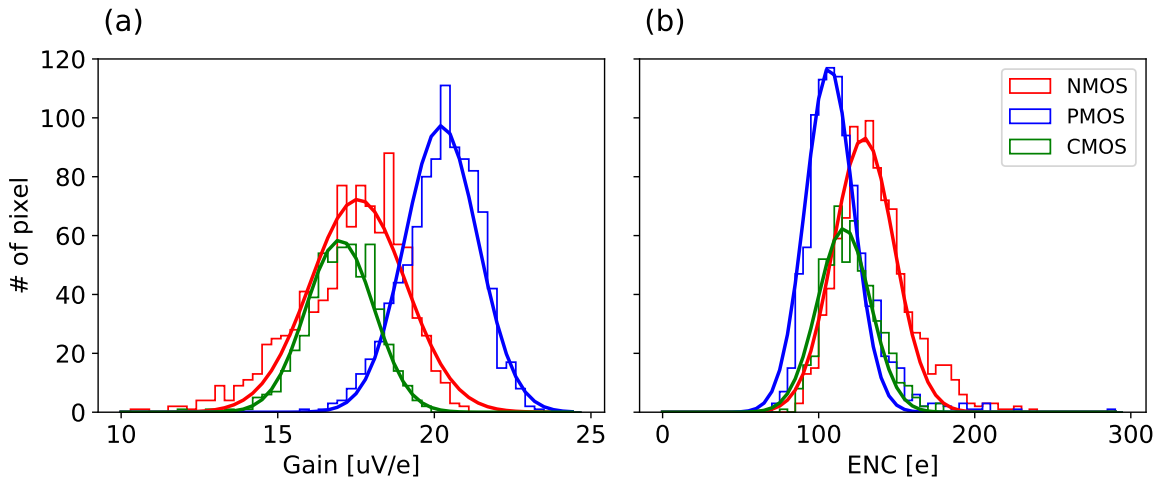


Figure 6.13: Gains and ENC of three pixel types in LF-CPIX. The results are fit by Gaussian functions. The fit parameters are listed in Table 6.1. The number of pixels in the CSA_{in}-PMOS, CSA_{in}-NMOS, CSA_{in}-CMOS types in the LF-CPIX chip is 848, 848, and 530 pixels, respectively.

of the new type of the CSAs (namely, CSA_{in}-NMOS and CSA_{in}CMOS types) are matched to the designed values.

6.3.2 Time walk

The time walk of a single CCPD_LF Small-FF pixel was measured using the setup shown in Figure 5.8 (a). The delay of the discriminator response as compared to the scintillator

Table 6.1: Gains and ENC of three pixel types in LF-CPIX. The average and dispersion of each values are shown with the simulated value [81].

Flavor	Gain [μV/e⁻]		Enc [e⁻]	
	Measured Ave. / σ	Simulated	Measured Ave. / σ	Simulated
CSA_{in}-PMOS	20.2 / 1.2	18.3	114 / 15.5	135
CSA_{in}-NMOS	17.3 / 1.5	17.0	136 / 20.6	149
CSA_{in}-CMOS	17.0 / 1.1	21.0	121 / 16.9	127

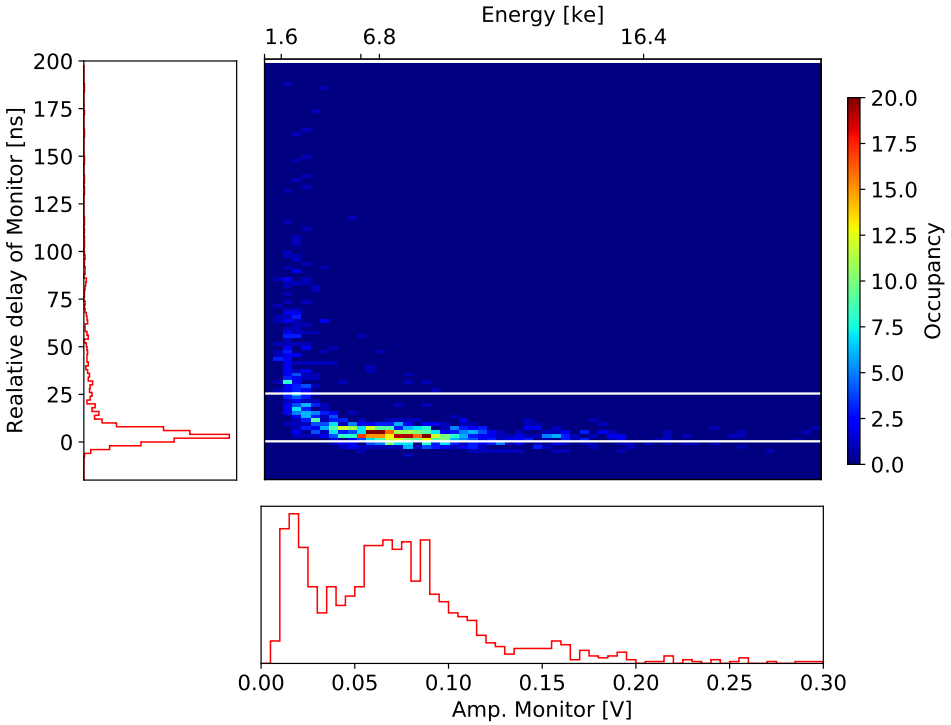


Figure 6.14: Relative discriminator response delay versus the signal amplitude of the CCPD_LF Small-FF. The top axis shows the calibrated signal amplitude in electron charge.

signal is plotted against the signal amplitude in Figure 6.14. An offset time is added to the discriminator response delay in such a way that the delay of the largest signal is assumed to be the reference time walk (i.e., 0 s). The time walk for two thresholds can be compared by applying normalization. The projection of the plot on the horizontal axis shows the charge spectrum, and that of the vertical axis shows the time walk of the CCPD_LF. The time walk is large when the signal is close to the threshold.

To discuss the in-time efficiency, time walk of seed hits is measured using LF-Monopix with the setup shown in Figure 5.8 (b). Figure 6.15 (a) shows the time between the scintillator response and the leading edge of the discriminator response of the two variants of LF-Monopix pixels, namely D1 and D2. The ratio of hits in 2 bins of a 25 ns clock is 98.7 % and 97.5 % for

Figure 6.15: (a) The distribution of the time interval between the scintillator signal and the leading edge of the in-pixel discriminator response measured with a 40 MHz clock, and (b) the threshold distribution without TDAC tuning of the LF-Monopix D1 (blue) and D2 (red). In (a), the peaks of the distributions are set to be 0 by summing delay offsets. In (b) the thick line shows the fit (Gaussian) distribution where σ is 710 and 1 020 e^- for D1 and D2, respectively.

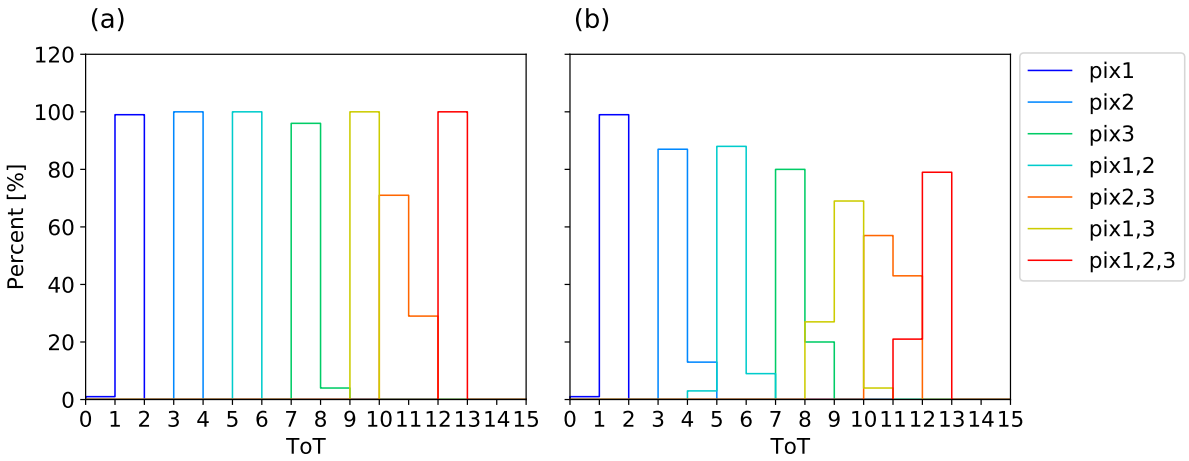


Figure 6.16: ToT values of test pulse injection. The test pulse was injected to the three CCPD_LF pixels, which are connected to one FE-I4 pixel. (a) shows an example of a good pixel. All combinations are not overlapping. (b) shows an example of a bad pixel. ToT value is 4 when the test pulse are injected to Pixel-2 but it is also 4 when a signal is produced in Pixel 1 and 2 at the same time

LF-Monopix D1 and D2, respectively. As explained in Section 5.4.1, the measurements using this setup only show the upper limits of the actual in-time efficiency.

The threshold distribution is also compared for LF-Monopix D1 and D2. Figure 6.15 (b) shows the threshold dispersion measured using test pulse injection (Section 5.2.2). The dispersion of D2 is approximately 300 e^- larger than that of D1. This difference is explained by the smaller transistor is used as the input transistor of the D2 discriminatorT. The process variation causes the dispersion of the threshold, and it is larger when the transistor size is smaller.

6.4 DMAPS + R/O chips

The CCPD_LF attached to the FE-I4 is tested to prove the feasibility of the pixel en/decoding concept using test pulse injection. Figure 6.16 shows the response to the test pulse injection in three CCPD_LF pixels connected to one FE-I4 pixel. Each ToT distribution indicates one of the combinations of the three pixels (shown as Pixel 1, 2, and 3 in Figure 4.4). In other words, test pulses were injected as follows: to Pixel 1, 2, and 3 individually, 2 pixels at the same time (Pixel 1 and 2, Pixel 2 and 3, and Pixel 1 and 3), and to 3 pixels in the same time (Pixel 1, 2, and 3).

The threshold of the FE-I4 was tuned using a standard tuning procedure by injecting test pulses into the injection capacitors of FE-I4 [94]. Then, the three global DACs of the pulse height modulator in CCPD_LF (indicated as HEIGHT1, 2, and 3 in Figure 4.3) were set to

obtain the mean ToT values of 2, 4 and 8, respectively, in active FE-I4 pixels. As the last step of the tuning, the feedback of the CSA in FE-I4 (showed as FDAC in Figure 4.3) was adjusted to obtain the distribution of ToT values that had minimal overlapping. The tuning was successful in the three pixels shown in Figure 6.16 (a). The results show the feasibility of the pixel en/decoding method when signal charge is shared with multiple pixles.

However, the ToT distributions are overlapping in some of the 3-pixel groups. An example of the overlapped ToT distribution is shown in 6.16 (b). The pulse height of the output stage circuitry is set by three global DACs. The pulse height cannot be adjusted pixel by pixel. In the FE-I4, the feedback of CSA and threshold of the discriminator influence ToT values by pixel-to-pixel using the in-pixel DACs. There are three ToT values in each pixel to be tuned, but the number of adjustable parameters in each pixel is two. The number of in-pixel adjustable parameters is not enough. Thus, some pixels cannot be adjusted as required. This is by nature of the FE-I4, which is not designed to perform a pixel decoding. Further studies with a dedicated readout chip are needed to apply this concept to the actual high energy particle experiments.

6.5 TID radiation hardness

6.5.1 Leakage current and breakdown voltage

The I-V curve of LF-CPIX was measured at various TID radiation levels. As described in Section 5.5.1, the measurement was performed at room temperature. As Figure 6.17 (a) shows, the breakdown voltage was increased by the TID irradiation. Hence, the bias voltage of 200 V can still be applied after TID irradiation.

The increase of leakage current was observed with increased TID irradiation. Figure 6.17 (b) shows the leakage current at the bias voltage of 200 V. The increase was small when the TID was lower than 100 krad and logarithmically increased when the TID was higher than 50 Mrad. The leakage current at a bias voltage of 200 V was 0.4 nA/pixel at 50 Mrad. The ENC_{shot} was calculated to be 35 e^- from Equation (3.19), assuming a τ_f of 1 µs. Considering the temperature dependency of the leakage current (Equation (3.20)), this can be remedied by cooling the chip to, for example, −20 °C.

6.5.2 Power consumption of CSA

Figure 6.18 shows the current consumption of the CSA input device of CCPD_LF at various TID levels. The CSA input device of a CCPD_LF pixel is PMOS with a load transistor (Figure 4.5 (a)). The variation was found to be approximately 15 %. The current consumption is determined by the current set to the a load transistor and it can be adjusted by a DAC implemented in the chip periphery. If the change of the current consumption observed in Figure 6.18 was caused by the property changes in the periphery and not the characteristic of the CSA input device, the current consumption can be compensated and maintained at the same value by adjusting the DAC values.

The DACs in the periphery of LF-CPIX were optimized in the way that allows for the compensation of current consumption variation. Figure 6.19 shows the current consumption of

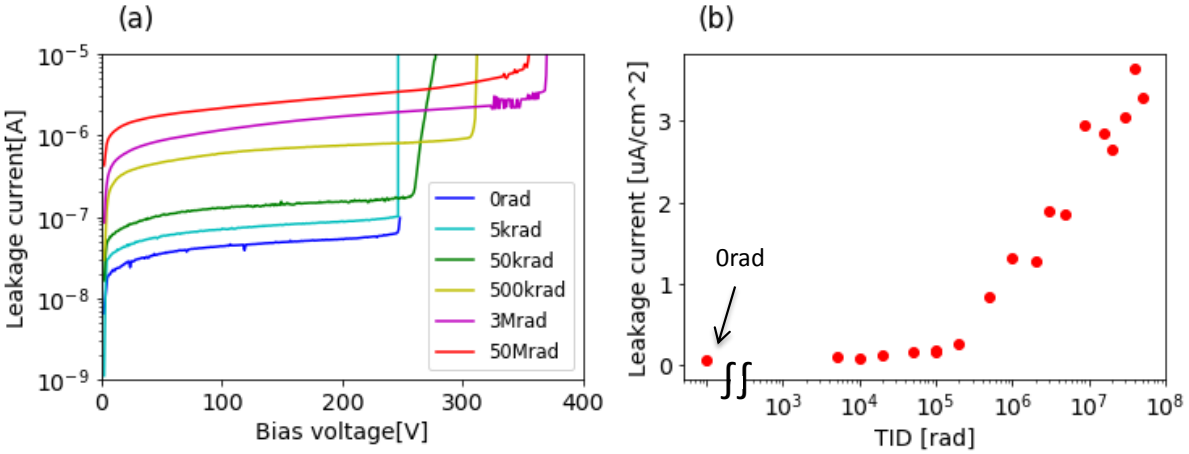


Figure 6.17: Leakage current of LF-CPIX before and after irradiation. (a) I-V curves before and after the various TID irradiation levels. (b) The leakage current per unit area at the bias voltage of 200 V. The leftmost point is the leakage current before the irradiation.

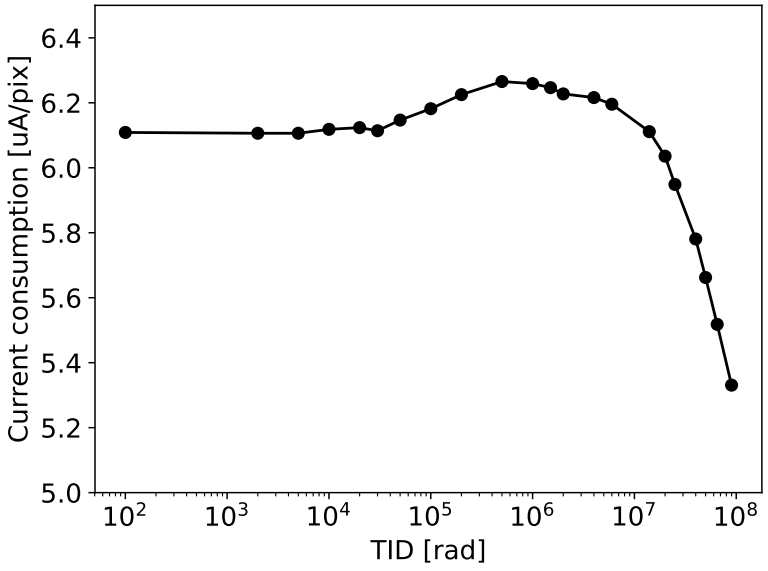


Figure 6.18: Current consumption of a CSA input device in CCPD_LF

the CSA input device according to the DAC values. Both PMOS and NMOS flavors are able to increase the power consumption from the default value by a factor of 2. The results confirm that the DAC implemented in LF-CPIX is sufficient for maintaining the current consumption.

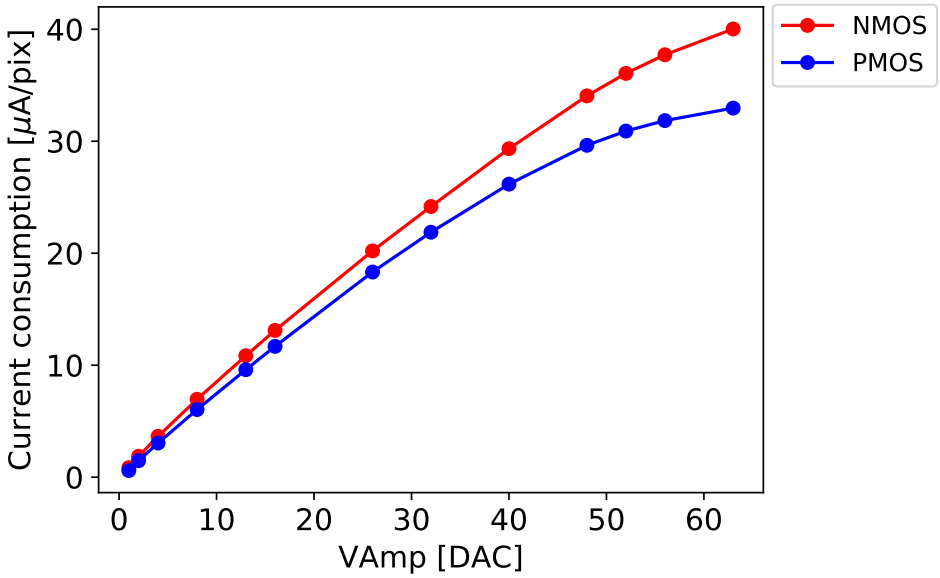


Figure 6.19: Tunable range of the current consumption of the CSA input device in LF-CPIX CSA_{in}-NMOS and CSA_{in}-PMOS. The x-axis is the value of the 6-bit DAC implemented in the chip periphery to optimize the current consumption. The DAC value of 26 is the default value.

6.5.3 Gain and noise

Figure 6.20 shows the gain and ENC of the CCPD_LF and LF-CPIX pixels at various TID levels. They were measured using test pulses as described in Section 5.5.1. The measurement results were normalized to the values before irradiation.

Figure 6.20 (a) shows the results from two pixels for each pixel type in CCPD_LF. Although the variations between pixels are large, the degradation of the gain in the pixel type of FET_f–L and FET_f-ELT was smaller than that in the pixel type FET_f-S. The maximum gain degradation in the FET_f-L pixels was approximately 20 %.

The size of the feedback transistor in the FET_f–L pixel (0.35 µm × 1.5 µm) is employed for CCPD_LF and LF-Monopix. In addition, many changes have been applied to LF-CPIX for the mitigation of the degradation observed in CCPD_LF. The modifications were applied on the biasing circuitry, input transistor size, overall of the CMOS circuitry layout, and chip periphery, including that which regulates CSA power [81].

The three types of CSA input devices, which are described in Section 4.2.2, were also tested (6.20 (b)). The decrease in the gains of CMOS-CSA and NMOS-CSA are as small as that of PMOS-CSA at approximately 5 %. Although the most effective change cannot be determined by this measurement since many changes have been made when LF-CPIX was designed, it can be concluded that the modifications were effective in mitigating the gain decrease. The noise

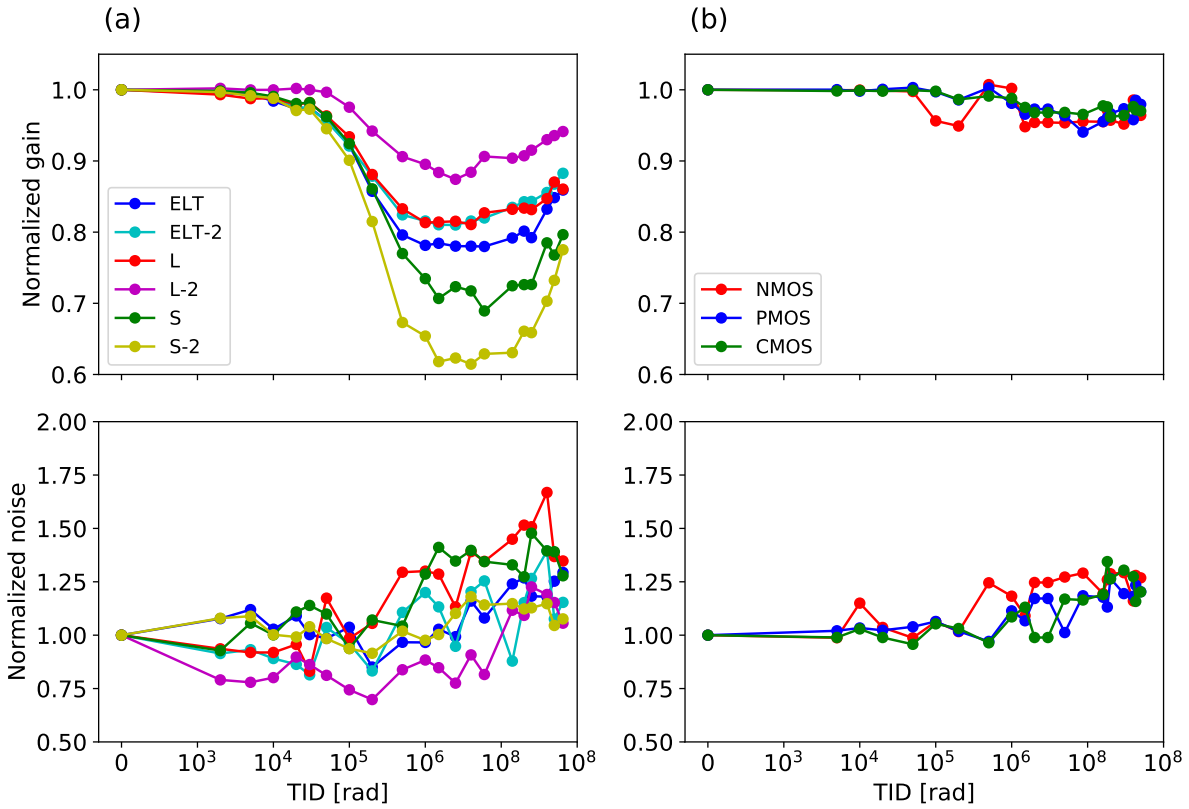


Figure 6.20: Gain and noise of (a) CCPD_LF and (b) LF-CPIX. In CCPD_LF, two pixels are plotted from each flavor. The results before irradiation have been normalized to unity. The datum shown at 100 rad is the results before irradiation, namely 1.0.

was increased by approximately 25 %. This can be understood by the leakage current increase shown in Section 6.5.1. The results imply that the radiation hardness of the new CMOS-CSA and NMOS-CSA is as high as that of the conventional PMOS-CSA.

6.5.4 Feedback current of CSA

The influence of the TID irradiation on the feedback current of the CSA in LF-CPIX CSA_{in}-CMOS pixel was measured because a large change in the feedback current after TID irradiation was observed in previous studies [75]. To evaluate the feedback current, the ratio of the width and height of the CSA output was measured. As Figure 6.22 shows, the ratio will vary depending on the strength of the feedback. The width of the CSA output was measured by the pulse width of the discriminator output at the fixed threshold voltage approximately corresponding to 3.9 ke^-, and its height was measured by the mean of the s-curve method. Figure 6.22 shows the results when the test pulse amplitude was swept. No influence of the TID irradiation on the CSA feedback current was observed.

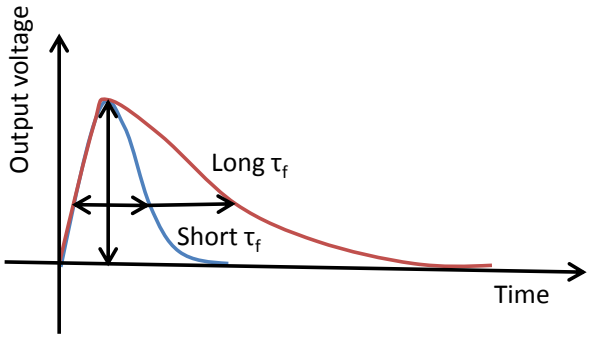


Figure 6.21: Waveform at the CSA output with short (blue) and long (red) feedback time constant, τ_f. The relation between the pulse height and width changes when the feedback current changes.

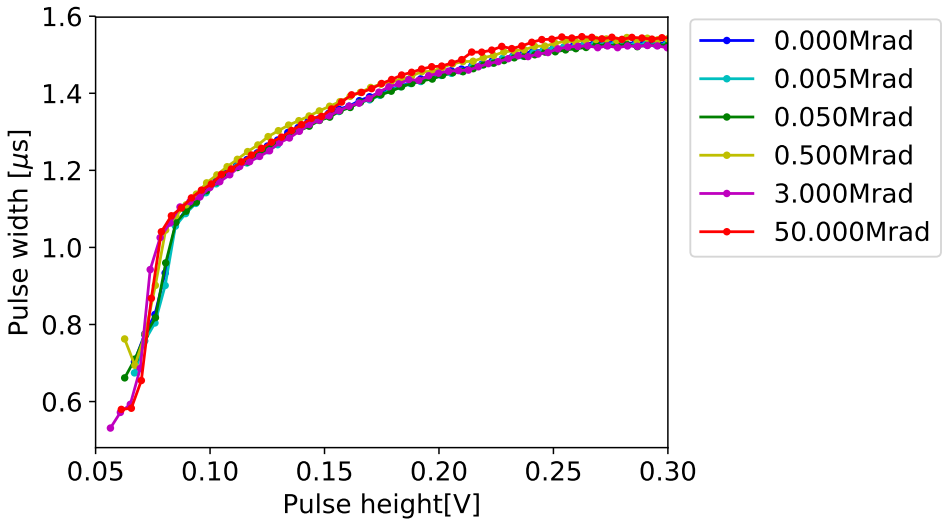


Figure 6.22: Relations between pulse height and width at various TID irradiation levels. The amplitude of the test pulse was swept, and the width and height of the CSA output were measured at each test pulse injection. The width was obtained by the pulse width of the discriminator output at the fixed threshold voltage that corresponds to approximately 3 900 e^-, and the amplitude was measured by the mean of the s-curve method changing the threshold.

6.5.5 Threshold dispersion

As discussed in Section 3.4.4, the lowest threshold that fulfill the allowed noise occupancy are defined by the ENC of the analog front-end circuitry and the threshold dispersion. The threshold distribution should not be enlarged by the TID irradiation. Figure 6.27 shows the threshold dispersion before and after the TID irradiation of 50 Mrad. The un-tuned threshold dispersion increased from 370 e^- to 420 e^- due to the irradiation. TDAC has the potential to mitigate the increased threshold distribution. The TDAC values were tuned to minimize the distribution of s-curve edge at the fixed global threshold value using test pulse injection. The dispersion of the tuned threshold were 55 e^- and 76 e^- before and after TID irradiation, respectively. An increase of only 20 e^- was observed after TDAC tuning. The influence on the lowest threshold is estimated to be small since the ENC is approximately 150 e^- rms.

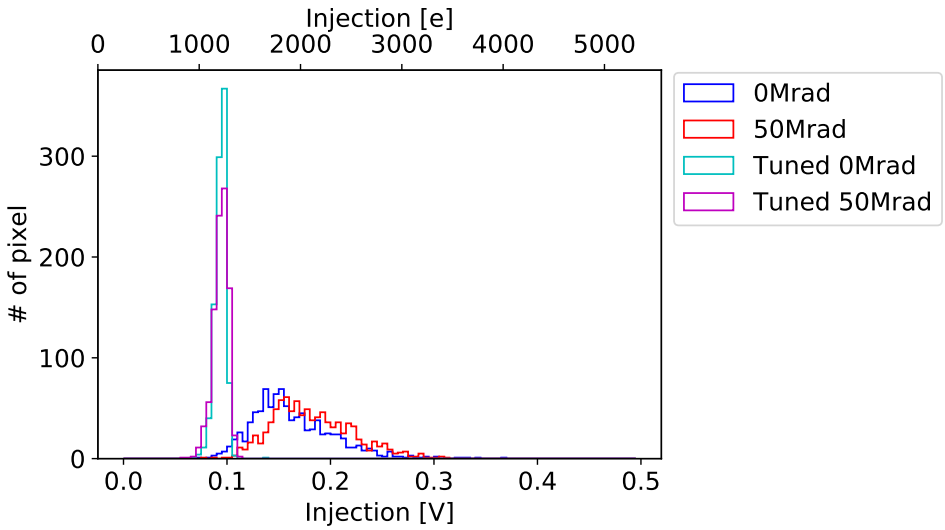


Figure 6.23: Threshold distributions before and after the TID irradiation of 50 Mrad Mrad. The threshold dispersion was calculated by fitting the Gaussian function to each distribution. The threshold dispersion before irradiation without TDAC tuning, after irradiation without TDAC tuning, before irradiation with TDAC tuning, and after irradiation with TDAC tuning are 370, 418, 55, and 76 e^-, respectively.

6.6 NIEL radiation hardness

In this section, the NIEL radiation hardness is characterized by comparing the measurement results of un-irradiated and irradiated LF-Monopix chips. Since the behaviors of the irradiated chips before irradiation are unknown (Section 5.5.1), the chip variants due to the process variations must be taken into account in the comparisons.

Three chips of different fluence, i.e., 1×10^{14} n_{eq}/cm^2, 5×10^{14} n_{eq}/cm^2, and 1×10^{15} n_{eq}/cm^2, were tested. The fast readout was employed by a 40 MHz clock for all irradiated chips.

6.6.1 Leakage current and breakdown voltage

The leakage current was measured up to the bias voltage of 200 V. Figure 6.24 shows the I-V curves of LF-Monopix irradiated chips. The atmosphere of the chip was set to −30 °C by a climate camber, and the chip temperature was approximately −25 °C. A breakdown was not observed in a measurement range up to 200 V.

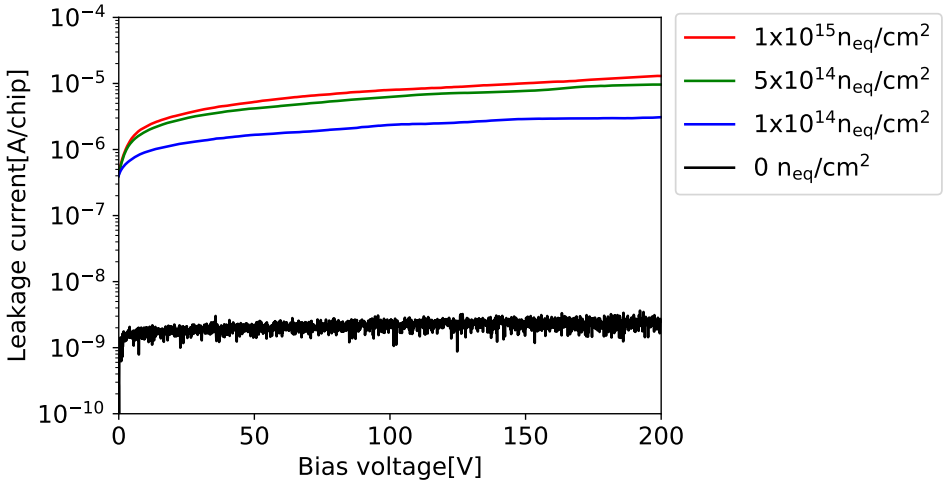


Figure 6.24: I-V curves of un-irradiated and NIEL irradiated LF-Monopix. The measurement was performed in a −30 °C atmosphere. The fluence is shown in the legend. A breakdown was not observed up to 200 V.

The leakage current after NIEL irradiation of 1×10^{15} n_{eq}/cm^2 fluence was 13.0 µA/cm^2 at the bias voltage of 200 V. The increase of leakage current measured in the NIEL irradiation test is estimated to be orders of magnitude larger than that measured in the TID irradiation test, considering the chip temperature. In the ATLAS ITk environment, both TID and NIEL damage occur throughout the lifetime of the ATLAS ITk Pixel Detector. Bulk damage is the dominant cause of the leakage current increase.

6.6.2 Charge spectrum

The charge spectrum of seed hits was measured by ToT values using a 2.5 GeV electron beam. The results of un-irradiated and irradiated LF-Monopix are shown in Figure 6.25 (a) and (b), respectively. The fluence of the irradiated chip was 1×10^{15} n_{eq}/cm^2. Both chips were cooled with dry ice, and the chip temperature was lower than −40 °C[1]. The thresholds of both pixels were 1 500 e^-. The bias voltage of the un-irradiated chip was set to 200 V. Although the breakdown voltage of the NIEL irradiated LF-Monopix was higher than 200 V (Figure 6.24), the bias voltage during the measurement was set to 130 V due to technical limitations.

The upper axes of Figure 6.25 show the calibrated signal amplitudes in units of electron charge. The calibration was performed using test pulse injection and assuming injection capacitance

[1] the thermometer was saturated at −40 °C

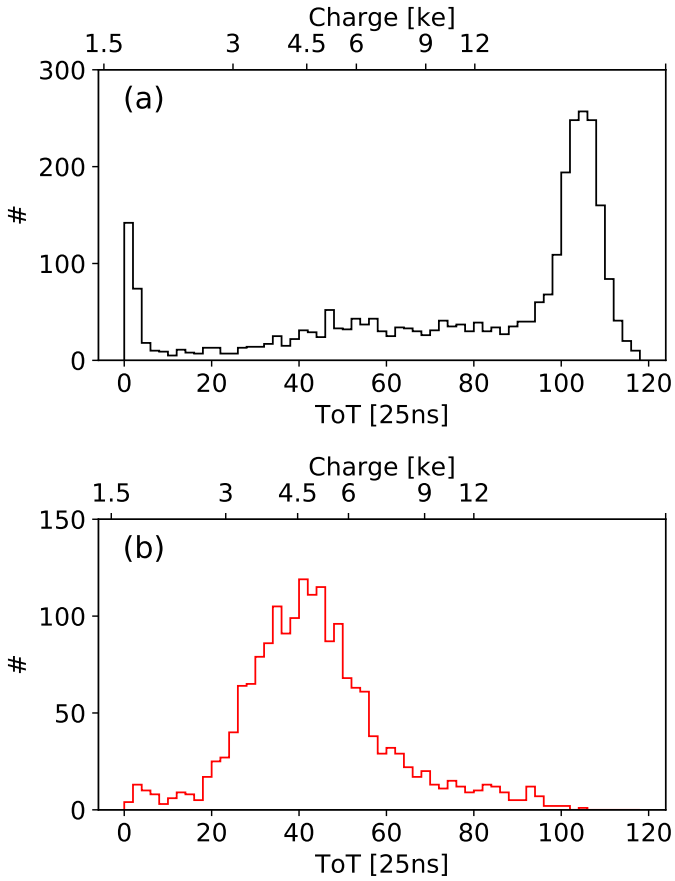


Figure 6.25: Charge spectrum of seed hits of (a) the non-irradiated and (b) irradiated LF-Monopix. The fluence of the irradiated chip is 1×10^{15} n_{eq}/cm^2. Each plot shows a spectrum of one pixel with the threshold of 1 500 e^-. The calibrated value in electrons is shown in the top axis of each plot.

of 2.7 nF [123]. ToT responses to test pulse injection, used for signal calibration, are shown in Figure 6.26 for the un-irradiated and irradiated LF-Monopix, respectively. The ToT value is not linear to the injected charge and provides higher resolution of the signal amplitude when the signal amplitude is close to the threshold. This results in the non-linear scale of the top axis in Figure 6.25 against the ToT value. This non-linearity is advantageous when it is used to compensate the time walk. This is because time walk compensation is necessary when the signal amplitudes are close to the threshold, i.e., when ToT values are small (Figure 6.14). The high resolution of the amplitude determines the amount of compensation more precisely.

Due to the non-linearity of the ToT value, the amplitude resolution of a large signal is not as high as that of a small signal. Furthermore, the test pulse circuitry starts to become saturated at the injection charge of approximately 12 ke^-, since the test pulse injection was originally designed to tune the threshold and calibrate the threshold value into the unit of charge. Since the MPV of the un-irradiated LF-Monopix is high compared to the calibration range, the actual value of MPV cannot be determined by this measurement. However, the measurement result indicates that the MPV of the un-irradiated chip is larger than 12 ke^-. Compared to the threshold,

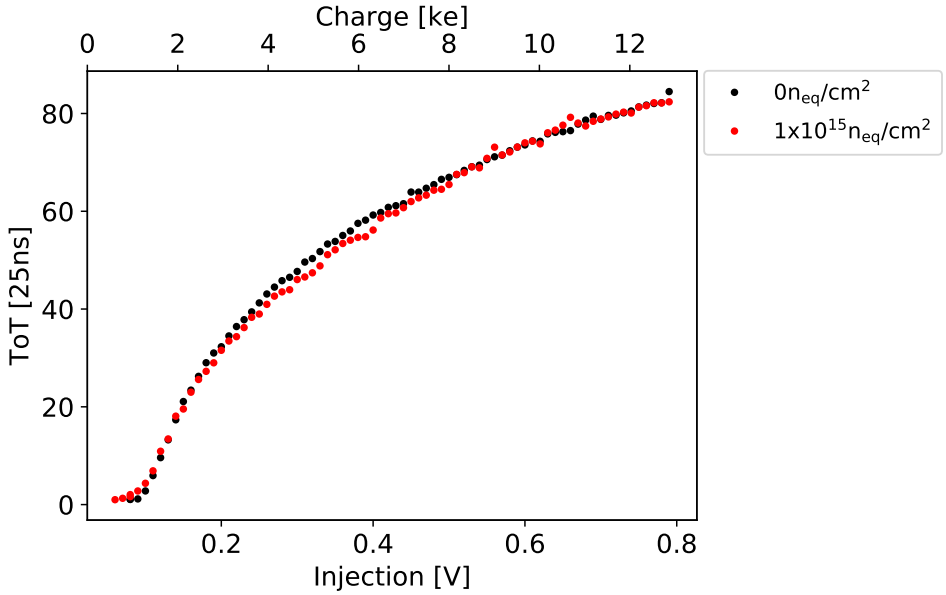


Figure 6.26: ToT response to the test pulse injection of the un-irradiated and irradiated (fluence of 1×10^{15} n_{eq}/cm^2) LF-Monopix. The top axis was calculated assuming the injection capacitance of 2.7 fF.

this is adequately high.

The MPV was decreased by a factor greater than 3 in the results shown in 6.25 (b). However, it is still as high as 4.5 ke^-. This degradation should be due to the decrease of collected charge and not the gain decrease of the electronics, since there was no significant difference between un-irradiated and irradiated chips in the ToT response to the test pulse injection (Figure 6.26).

6.6.3 Hit efficiency

The hit efficiency was measured using a 2.5 GeV electron beam with the setup shown in Section 5.4.2. The bias voltages were 200 V and 130 V for the un-irradiated and irradiated (fluence of 1×10^{15} n_{eq}/cm^2) chips, and the chip temperature was below -40 °C. These values are equivalent to those used in the charge spectrum measurement.

The measurement was performed with tuned thresholds. Figure 6.27 shows the threshold distributions of the un-irradiated and irradiated chip after the threshold tuning. The TDAC of each pixel was tuned to achieve uniform noise occupancy. The standard deviation of the threshold distribution was larger than that shown in Figure 6.27, since the threshold was not tuned to have a uniform response to the test pulse injection. The tuning of the noise occupancy includes the distribution of the gain and noise of the CSA in addition to the threshold distribution due to the finite step size of TDAC. The medians of the threshold were 1.26 ke^- and 1.6 ke^-, respectively.

Figure 6.28 shows the noise occupancy after the tuning. The noise occupancies of most of the pixels were more than 2 orders of magnitude lower than ATLAS ITk requires. 5 and 2 pixels were disabled from un-irradiated and irradiated chips because the noise occupancy of those pixels is high.

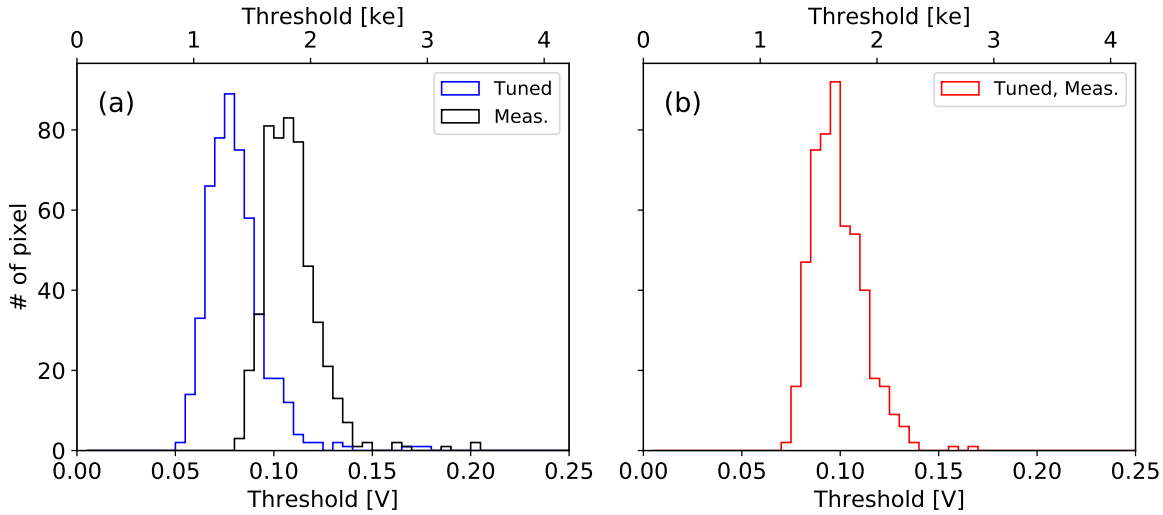


Figure 6.27: Threshold distribution of (a) un-irradiated and (b) irradiated (fluence of 1×10^{15} n_{eq}/cm^2) LF-Monopix. The threshold was tuned by the noise occupancies (blue and red) with medians 1.26 ke^- and 1.6 ke^-, respectively. The threshold has increased to the median of 1.8 ke^-.

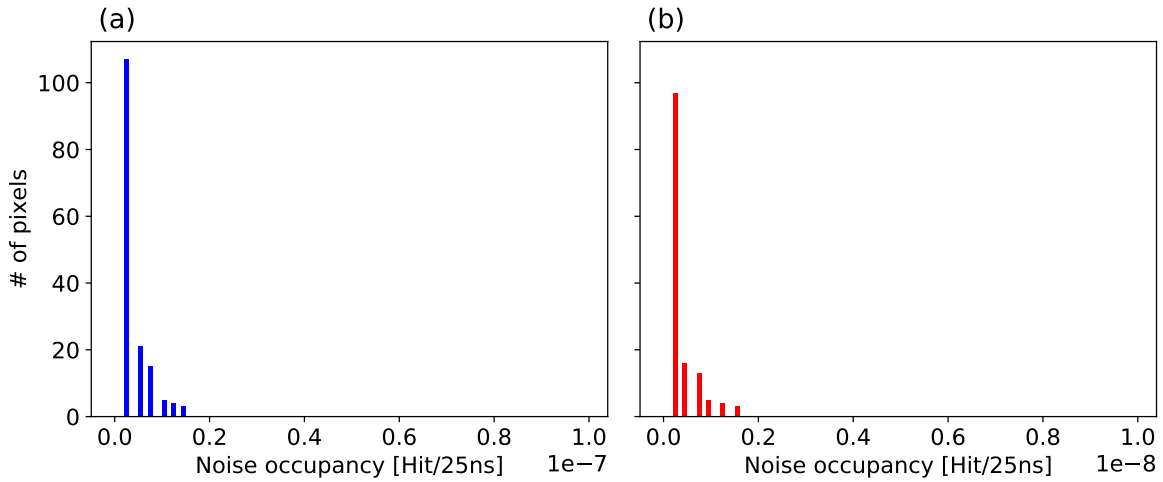


Figure 6.28: Noise occupancy after TDAC tuning for (a) un-irradiated and (b) irradiated (fluence of 1×10^{15} n_{eq}/cm^2) LF-Monopix. The ATLAS ITk Pixel Detector requires the noise occupancy to be $<1 \times 10^{-6}$ hits per proton-proton collision.

For the hit efficiency measurement, the threshold of the un-irradiated chip was set to be similar to that of the irradiated chip and higher than the threshold tuned by the noise. Figure 6.28 (a) also shows the threshold distribution during the hit efficiency measurement. The median of the threshold distribution was 1.8 ke^-.

Figure 6.29 shows the hit efficiency. Pixels from Monopix D1 type that is 4 columns × 106 rows of were activated. Background of the reconstructed track are estimated to be 0.5 % and 0.3 % for the non-irradiated and irradiated chip, respectively. These values limit the precision of the measured values. The averaged hit efficiencies of non-irradiated and irradiated chips are 99.6 % and 98.9 %, respectively, which are high enough to meet the ATLAS ITk Pixel Detector requirement of >97 % [26].

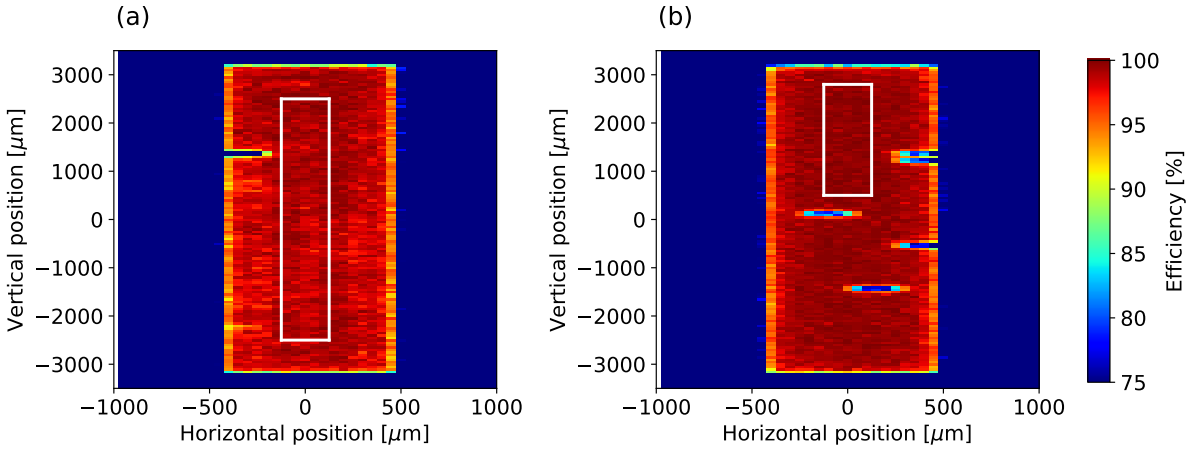


Figure 6.29: Hit efficiency of (a) un-irradiated and (b) irradiated (fluence of 1×10^{15} n_{eq}/cm^2) LF-Monopix with 4 × 129 pixels. The average efficiencies of the regions indicated by the white boxes are 99.6 % and 98.9 %, respectively.

The in-pixel hit efficiency was calculated, although the spatial resolution of the measurement was limited as 20 µm. Figure 6.30 is the accumulated data of the hit efficiency into 250 µm × 50 µm. There is a region where the hit efficiency is low in the irradiated chip, whereas the in-pixel hit efficiency is homogeneous and no in-pixel structure is seen for the un-irradiated chip. The degradation of the hit efficiency occurs near the edge of the pixel, and it can be understood by the charge sharing effect. Since the threshold of the irradiated chip was lower than 1/4 of the MPV, the signal charges of some of the hits were spread to multiple pixels and did not exceed the threshold.

6.6.4 In-time efficiency

The time walk of irradiated LF-Monopix was observed using a 2.5 GeV electron beam in the measurement setup described in Figure 5.8 (b). The fluence of the NIEL irradiated chip was 1×10^{15} n_{eq}/cm^2. The bias voltages and chip temperatures were as same as those set during the charge spectrum measurements (Section 6.6.2). Figure 6.32 shows the timing distribution of the signal response in units of 25 ns. 98.7 % of hits were found in the 2 bins of 25 ns for the

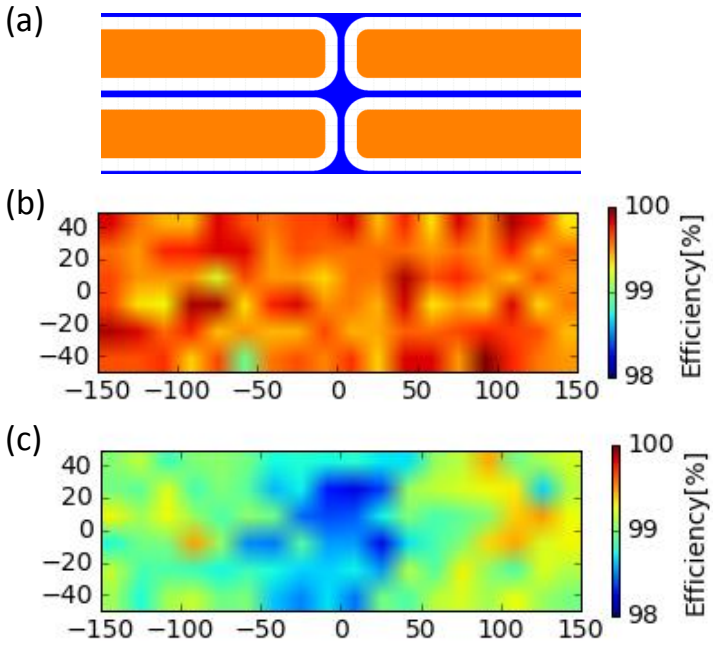


Figure 6.30: (a) The layout of the collection wells and the in-pixel hit efficiency of (b) un-irradiated and (b) irradiated LF-Monopix. The collection well is shown in orange in (a) and the blue structure is p-stop.

un-irradiated chip. The degradation of the time walk was observed, even with the low resolution of the measurement system. Only 83 % of hits were in 2 bins of the 25 ns clock period for the irradiated chip. The in-time efficiency of the irradiated chips can be estimated as 82 % because the hit efficiency is measured as 98.9 % (Section 6.6.3) and the in-time ratio is 83 %.

Figure 6.14 (a) shows the same result from the irradiated chip as shown in Figure 6.32 but plotted only when ToT value is . One can correct the relative delay according to the ToT values to compensate the time walk In Figure 6.14 (b), an offset in delay for each ToT value is added such that the largest fraction of hits would be included in the bins of 0 and 1 for each ToT value. The ratio of hits in the range of 2 bins are increased to be 98 %.

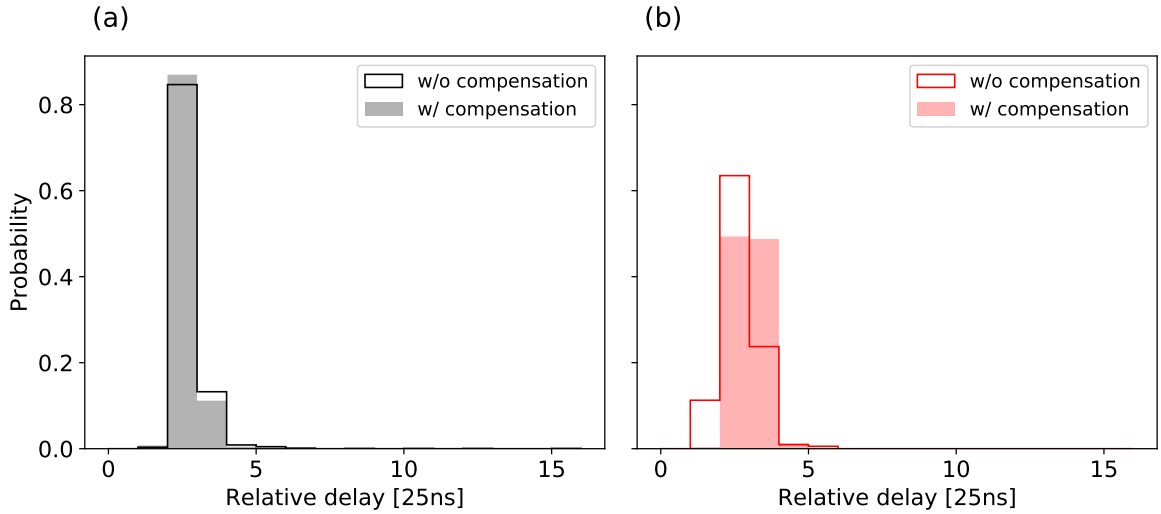


Figure 6.31: The distributions of the delay between a scintillator hit and LE timestamp of (a) un-irradiated and (b) irradiated (fluence of 1×10^{15} n_{eq}/cm^2) LF-Monopix, respectively. Each plot shows a delay of seed hits in one pixel which is in D1 flavor. The ratio of hits in 2 bins of 25 ns in the un-irradiated and irradiated LF-Monopix pixels are 98.7 % and 83 %, respectively. The time walk compensation was applied and the ratios are improved as 98.

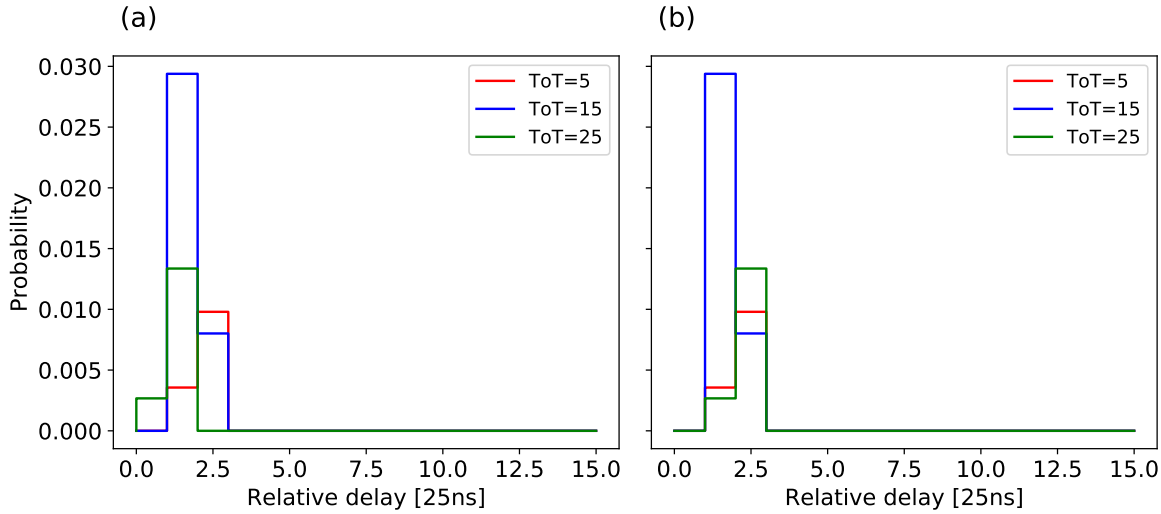


Figure 6.32: A delay between a scintillator hit and LE timestamp of the irradiated Monopix chip (a) with and (b) without ToT compensation. an offset in delay for each ToT value is added such that the largest ratio of hits would be included in the bins of 0 and 1 for each ToT value

CHAPTER 7

Discussions and outlooks

In this thesis, the suitability of a large-fill-factor DMAPS using a highly resistive sensor substrate to the ATLAS ITk Pixel Detector is investigated. One of the advantages of large-fill-factor DMAPS is its high voltage tolerance. The guard ring optimization based on the perspective of PEM measurement results increased the breakdown voltage up to 300 V. The success indicates that the n-wells implanted using the LFoundry 150 nm CMOS process has a high voltage tolerance of at least 300 V. The isolation of the pixel readout electronics from high bias voltage was succeeded. The thinning and back-side processing were applied to the LF-CPIX, and no significant degradation to the breakdown voltage, the leakage current, and the detection hit efficiency are measured. This confirms that thinning and back-side processing were applied to the wafer without damaging the DMAPS. In addition, the bias voltage of 200 V could be applied to the prototype even after the TID or NIEL irradiation. These measurement results are all encouraging, especially for DMAPS applications that are required fast charge collection and radiation hardness.

The disadvantage for the large-fill-factor DMAPS is its large detector capacitance. The cross coupling from the digital signals were the biggest concern when digital logic, such as ToT circuitry, is implemented inside the pixel. The median threshold of 1.26 ke^- can be set with a noise occupancy lower than 1×10^{-8} hit /25 ns/pixel. The results imply that the cross coupling is low enough and does not limit the possible lowest threshold. It is also confirmed by observing the waveform at CSA and discriminator output in a LF-Monopix pixel. New analog front-end circuitry are proposed to overcome the large detector capacitance, since the conventional CSA and discriminator requires large power consumption to fulfill the timing requirements. The new power-saving CSA and discriminator were tested, and the measurement results demonstrated that they are functioned as well as the conventional CSA and discriminator.

Two irradiation campaigns were performed to separately investigate the influence of surface damage and bulk damage to DMAPS. The TID irradiation hardness of the analog front-end circuit was confirmed by irradiating the prototype chips up to 50 Mrad using an X-ray tube. Since the most dominant TID effect was expected to be seen on STI, the spectrum of the X-ray tube was confirmed to reproduce the surface damage equivalent to that of the ATLAS ITk Pixel Detector environment from the estimation of dose at STI considering the X-ray absorption in the metal layers. The gain degradation was small at 5 %, and the noise increased by approximately

20 %. However, the noise measurement was performed at room temperature, and the noise increase should be caused by the increase in leakage current. During the actual ATLAS ITk Pixel Detector operation, the chip will be cooled, and the increase in leakage current due to the TID irradiation will be mitigated. In this test, the new power-saving CSA in a LF-CPIX CSA_{in}-CMOS pixel, are shown to be as hard to radiation as the conventional CSA with a PMOS input transistor.

Like the analog front-end, the digital circuitry also requires the TID irradiation study. Although former studies have already proven that the CMOS feature size of this range has sufficient TID hardness [70, 124], the irradiation tests for the actual layouts must to be presented before application to actual high energy particle physics experiments.

The influence of bulk damage to DMAPS is studied using neutron irradiated chips. The hit efficiency of the neutron irradiated chip was measured to be 98.9 %. This is higher than the requirement when the timing performance is not taken into account. Since the timing resolution of the setup was not enough, the measurement results only show the upper limit of the relative in-time efficiency. The results show that the time walk of the new power-saving type discriminator is as small as the well-tested two stage discriminator before irradiation. However the time walks of both discriminators are larger than the requirement, and the in-time efficiency is 84 %. There are two ways to improve the timing performance in addition to the ToT compensation, which is shown in Section 6.6.4. First one is to shorten the response time of the analog circuitry, namely the CSA rise time and the discriminator's response time. Second one is to increase the signal to noise ratio and lower the threshold of the discriminator.

The first one can be realized by increasing the power consumption. As discussed in Section 3.4, the rise time of the CSA depends on the g_m of the amplifier. Larger g_m increases the power consumption of the amplifier. The power consumption of the discriminator can be also increased, like that of the CSA. Since the power consumption of the CSA and discriminator can be adjusted in the periphery of the prototype chips, it is possible to investigate the relationship between the time walk and power consumption further.

For the second strategy, the bias voltage can be increased, since the bias voltage of the irradiated chip during the time walk measurement was limited to 130 V due to the trouble with the high voltage scheme. It is possible to apply a bias voltage higher than 130 V regarding the I-V curve. The drift velocity can be increased by applying higher bias voltage, hence the charge collection efficiency is possibly improved. Figure 7.1 (a) shows the PEM image of the irradiated CCPD_LF at a bias voltage of 100 V. The "hot electron" is induced but the breakdown does not occur (Figure 7.1 (b)). The results indicates that the leakage current of the "hot electron" might also be needed to be considered when increasing the voltage. The increase of the leakage current also must be concerned when the bias voltage is increased because it will induce the increase of ENC and a rise of the lowest threshold.

The thinning and back-side process might increase the charge collection efficiency. The measurement results imply that the signal from 200 µm thinned DMAPS is large enough for pixel readout with ENC of 150 e^- to have the hit efficiency of 99.5 % if the charge collection efficiency is as high as that of an un-irradiated chip. Figure 7.2 shows the MPV of the p-n diode fabricated in the LFoundry 150 nm CMOS in >2 kΩ cm [125]. The figure compares the MPV between the NIEL irradiated thinned and un-thinned chips. The results indicate that a larger MPV can be obtained if the sensor is thinned.

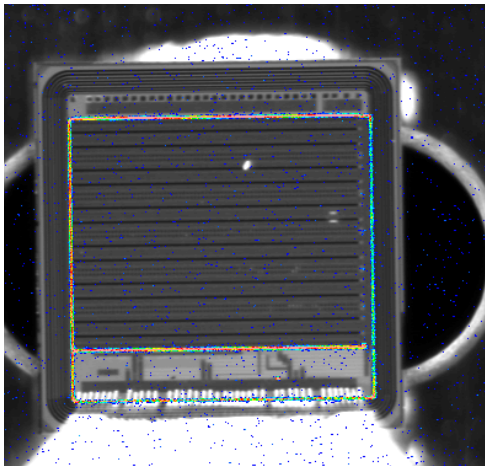


Figure 7.1: (a) PEM image and (b) I-V curve of irradiated CCPD_LF. The fluence of the chip is 1×10^{15} n_{eq}/cm^2. The PEM image was taken at the bias voltage of 100 V, which is lower than the breakdown voltage.

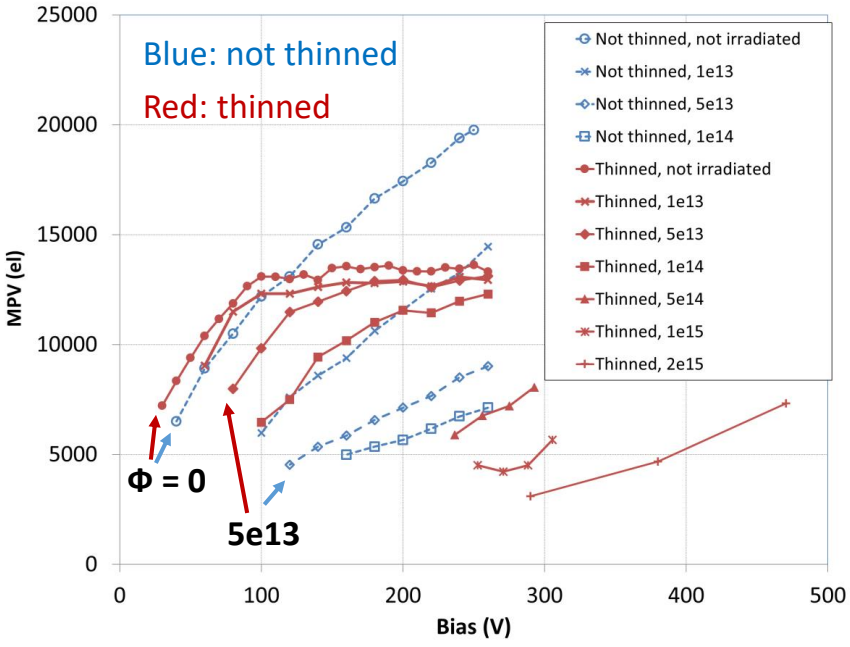


Figure 7.2: MPV of a p-n diode measured on the highly resistive wafer (>2 kΩ cm) provided by LFoundry. The fluence of NIEL irradiation is indicated in the legend [125].

In this thesis, modified small-fill-factor DMAPS for future application were also tested. The analog front-end electronics of the modified small-fill-factor DMAPS works as good as the standard large-fill-factor DMAPS with lower ENC. The bias voltage is limited by the capacitor between the collection well and CSA input. The maximum bias voltage applied to the CCPD_LF Low-FF was 30 V. This can be improved by selecting a capacitor with a higher voltage tolerance. A low noise analog front-end can be designed to maximize the advantage of a small detector capacitance. By combining the low noise analog front-end and thinning of the sensor this design has the potential to be a candidate for radiation hard DMAPS.

DMAPS + R/O chip configuration has also been tested as feature application. Pixel en/decoding have been tested to avoid fine pitch bump bonding. Although further study is required, using the pixel en/decoding scheme to distinguish charge sharing is feasible. The advantage of this configuration is that more readout electronics can be implemented in a small area. Thus, higher spatial resolution can be obtained with large area for the readout electronics. The DMAPS + R/O can be applied to future high hit rate experiments or X-ray applications, which require much higher hit rates.

CHAPTER 8

Conclusion

Three DMAPS prototypes, namely CCPD_LF, LF-CPIX, and LF-Monopix were fabricated using an LFoundry 150 nm CMOS technology on a highly resistive p-type wafer. LF-Monopix has the pixel size of 250 µm × 50 µm, active area size of 10 mm × 10 mm, and readout functionalities, including fast readout similar to that of the current ATLAS pixel readout chips. The results of characterization can be summarized as follows:

- Using a high-fill-factor design, a breakdown voltage of 300 V was realized by the optimization of the guard ring. A bias voltage of 200 V could be applied even after TID or NIEL irradiation of the HL-LHC level.
- Thinning and back-side processing were successfully applied to the LF-CPIX, and the 200 µm thinned LF-CPIX achieved a hit efficiency of 99.5 % with a threshold of approximately 2 700 e^-.
- The readout electronics of the prototypes, including fast readout logic, were confirmed to function as expected without serious cross coupling from digital signals. The new power-saving CSA and discriminator were also tested and shown to function as well as the conventional CSA and discriminator.
- The analog front-end performance (i.e., the gain, ENC, feedback current of CSA, power consumption of the CSA input device, threshold distribution) degradation caused by TID irradiation of 50 Mrad was negligible or compensable. The new type CMOS-CSA also has required TID hardness.
- Neutron irradiated (fluence of 1×10^{15} n_{eq}/cm^2) prototype also has a high hit efficiency of 98.9 % with a noise occupancy more than two orders of magnitude lower than the requirement. However, a decrease of charge collection and degradation in timing performance was observed. The charge collection after the irradiation was 4.5 ke^- for the bias voltage of 130 V. The upper limit of the in-time efficiency was estimated to be 82 %, whereas that of the un-irradiated chip was 98.4 %.

The characterization results obtained in this thesis are encouraging for the application of DMAPS in high rate and high radiation experiments in the LHC as discussed in Chapter 7.

Furthermore, the DMAPS characterized in this thesis can be applied to many experiments. The TID radiation hardness demonstrated can also be advantageous for X-ray detector applications. A large depletion region is good for hard X-ray detectors, and the thinning back-side illumination sensor can be useful for soft X-ray detectors. The results DMAPS coupling with readout chips also indicates that DMAPS is an attractive candidate for further applications with advanced readout electronics of fine granularity.

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List of Figures

List of Tables

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